CY62148GN MoBL®

4-Mbit (512K × 8) Static RAM

Features

- Very high speed: 45 ns
- Wide voltage range: 2.2 V to 3.6 V, 4.5 V to 5.5 V
- Ultra low standby power
  - Typical standby current: 3.5 µA
  - Maximum standby current: 8.7 µA
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ features
- Automatic power-down when deselected
- Complementary metal oxide semiconductor (CMOS) for optimum speed and power
- Available in Pb-free 32-pin thin small outline package (TSOP) II and 32-pin small-outline integrated circuit (SOIC) packages

Functional Description

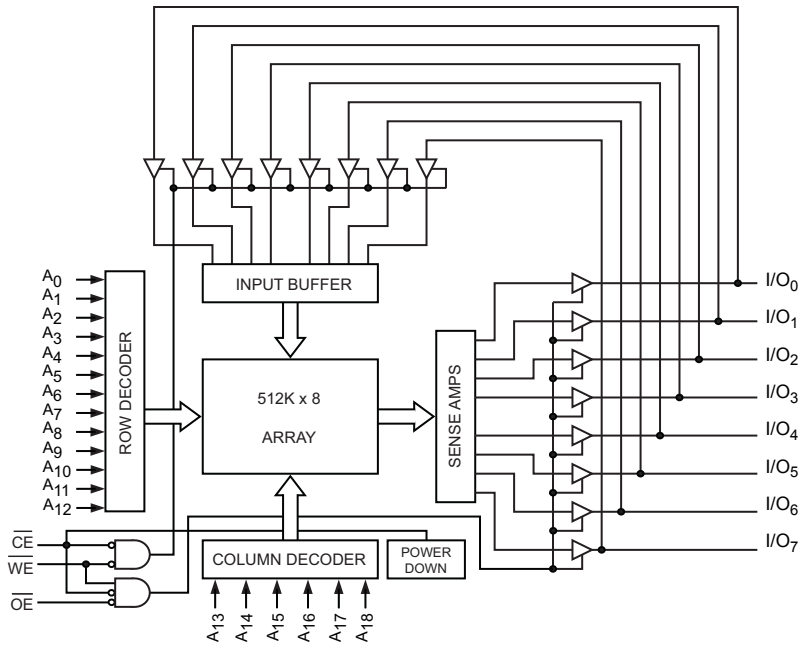
The CY62148GN is a high-performance CMOS static RAM organized as 512K words by 8-bits. This device features advanced circuit design to provide ultra low standby current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications. The device also has an automatic power-down feature that significantly reduces power consumption when addresses are not toggling. Placing the device in standby mode reduces power consumption by more than 99% when deselected ($\overline{CE}$ HIGH). The eight input and output pins (I/O_0 through I/O_7) are placed in a high-impedance state when the device is deselected ($\overline{CE}$ HIGH), Outputs are disabled ($\overline{OE}$ HIGH), or during an active Write operation ($\overline{CE}$ LOW and $\overline{WE}$ LOW).

To write to the device, take Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins (A_0 through A_{18}).

To read from the device, take Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing Write Enable ($\overline{WE}$) HIGH. Under these conditions, the contents of the memory location specified by the address pins appear on the I/O pins.

For a complete list of related documentation, click here.

Logic Block Diagram

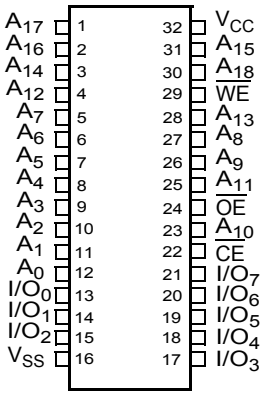


Contents

Pin Configurations

Figure 1. 32-pin SOIC/TSOP II pinout

Top View



Product Portfolio

Product	Range	V_{CC} Range (V)	Speed (ns)	Power Dissipation					
				Operating I_{CC} (mA)				Standby I_{SB2} (µA)	
				f = 1 MHz		f = f_{max}			
				Typ[1]	Max	Typ[1]	Max	Typ[1]	Max
CY62148GN30	Industrial	2.2 V–3.6 V	45	–	6	–	20	3.5	8.7
CY62148GN		4.5 V–5.5 V							

Note
1. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, T_A = 25 °C.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature ..... –65 °C to + 150 °C

Ambient temperature with power applied ..... –55 °C to + 125 °C

Supply voltage to ground potential .....–0.5 V to Vcc + 0.5 V

DC voltage applied to outputs in high Z state[2, 3] .....–0.5 V to Vcc + 0.5 V

DC input voltage[2, 3] .....–0.5 V to Vcc + 0.5 V

Output current into outputs (LOW) ..... 20 mA

Static discharge voltage (per MIL-STD-883, Method 3015) ..... > 2001 V

Latch-up current ..... > 140 mA

Operating Range

Device	Range	Ambient Temperature	V_{CC}[4]
CY62148GN	Industrial	–40 °C to +85 °C	2.2 V to 3.6 V, 4.5 V to 5.5 V

Electrical Characteristics

Over the operating range

Parameter	Description		Test Conditions	45 ns			Unit
				Min	Typ[5]	Max	
V_{OH}	Output HIGH voltage	2.2 V to 2.7 V	V_{CC} = Min, I_{OH} = –0.1 mA	2	–	–	V
		2.7 V to 3.6 V	V_{CC} = Min, I_{OH} = –1.0 mA	2.4	–	–	
		4.5 V to 5.5 V	V_{CC} = Min, I_{OH} = –1.0 mA	2.4	–	–	
		4.5 V to 5.5 V	V_{CC} = Min, I_{OH} = –0.1 mA	V_{CC} – 0.5[6]	–	–	
V_{OL}	Output LOW voltage	2.2 V to 2.7 V	V_{CC} = Min, I_{OL} = 0.1 mA	–	–	0.4	V
		2.7 V to 3.6 V	V_{CC} = Min, I_{OL} = 2.1 mA	–	–	0.4	
		4.5 V to 5.5 V	V_{CC} = Min, I_{OL} = 2.1 mA	–	–	0.4	
V_{IH}	Input HIGH voltage	2.2 V to 2.7 V	–	1.8	–	V_{CC} + 0.3[3]	V
		2.7 V to 3.6 V	–	2	–	V_{CC} + 0.3[3]	
		4.5 V to 5.5 V	–	2.2	–	V_{CC} + 0.5	
V_{IL}	Input LOW voltage	2.2 V to 2.7 V	–	–0.3[2]	–	0.6	V
		2.7 V to 3.6 V	–	–0.3[2]	–	0.8	
		4.5 V to 5.5 V	–	–0.5	–	0.8	
I_{IX}	Input leakage current		GND ≤ V_I ≤ V_{CC}	–1	–	+1	µA
I_{OZ}	Output leakage current		GND ≤ V_O ≤ V_{CC}, output disabled	–1	–	+1	µA
I_{CC}	V_{CC} operating supply current		f = f_{max} = 1/t_{RC}; V_{CC} = $V_{CC(max)}$, I_{OUT} = 0 mA CMOS levels	–	–	20	mA
			f = 1 MHz; V_{CC} = $V_{CC(max)}$, I_{OUT} = 0 mA CMOS levels	–	–	6	
I_{SB1}[7]	Automatic $\overline{CE}$ power-down current – CMOS inputs		$\overline{CE}$ ≥ V_{CC} – 0.2 V, V_{IN} ≥ V_{CC} – 0.2 V or V_{IN} ≤ 0.2 V, f = f_{max} (address and data only), f = 0 ($\overline{OE}$ and $\overline{WE}$) V_{CC} = $V_{CC(max)}$	–	3.5	8.7	µA
I_{SB2}[7]	Automatic $\overline{CE}$ power-down current – CMOS inputs		$\overline{CE}$ ≥ V_{CC} – 0.2 V, V_{IN} ≥ V_{CC} – 0.2 V or V_{IN} ≤ 0.2 V, f = 0, V_{CC} = $V_{CC(max)}$	–	3.5	8.7	µA

Notes

2. $V_{IL(min)}$ = –2.0 V for pulse durations less than 20 ns.
3. $V_{IH(max)}$ = V_{CC} + 0.75 V for pulse durations less than 20 ns.
4. Full device AC operation assumes a minimum of 100 µs ramp time from 0 to $V_{CC(min)}$ and 200 µs wait time after V_{CC} stabilization.
5. Typical values are included for reference and are not guaranteed or tested. Typical values are measured at V_{CC} = $V_{CC(typ)}$, T_A = 25 °C.
6. This parameter is guaranteed by design and not tested.
7. Chip enable ($\overline{CE}$) must be HIGH at CMOS level to meet the I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.

Capacitance

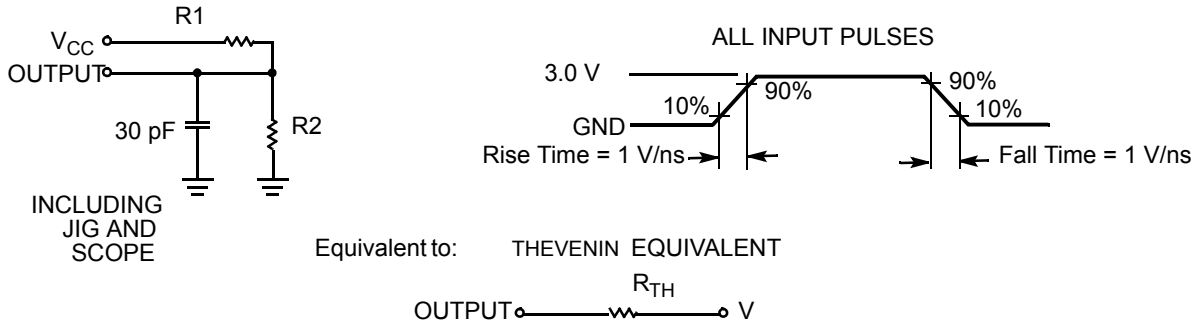
Parameter [8]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = $V_{CC(Typ)}$	10	pF
C_{OUT}	Output capacitance		10	pF

Thermal Resistance

Parameter [8]	Description	Test Conditions	32-pin SOIC Package	32-pin TSOP II Package	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	51.79	79.03	°C/W
Θ_{JC}	Thermal resistance (junction to case)		25.12	17.44	°C/W

AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms[9]



Parameter[8]	2.5 V	3.0 V	5.0 V	Unit
R1	16667	1103	1800	Ω
R2	15385	1554	990	Ω
R_{TH}	8000	645	639	Ω
V_{TH}	1.20	1.75	1.77	V

Notes
8. Tested initially and after any design or process changes that may affect these parameters.
9. Full-device operation requires linear V_{CC} ramp from VDR to $V_{CC(min)}$ > 100 µs or stable at $V_{CC(min)}$ > 100 µs.

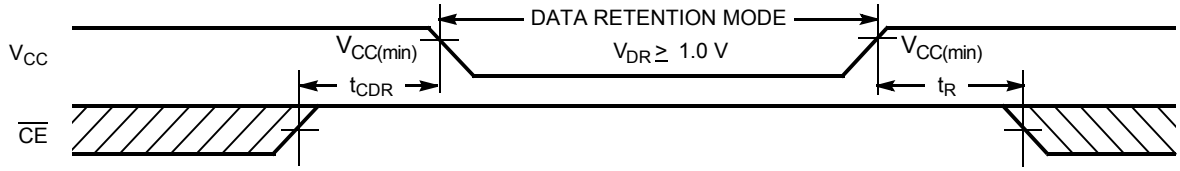
Data Retention Characteristics

Over the operating range

Parameter	Description	Conditions	Min	Typ[10]	Max	Unit
V_{DR}	V_{CC} for data retention		1	–	–	V
I_{CCDR}[11, 12]	Data retention current	V_{CC} = 1.2V, $\overline{CE} \geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V	–	–	13	µA
t_{CDR}[13]	Chip deselect to data retention time		0	–	–	ns
t_R[13, 14]	Operation recovery time		45	–	–	ns

Data Retention Waveform

Figure 3. Data Retention Waveform



Notes
10. Typical values are included for reference and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, T_A = 25 °C.
11. Chip enable ($\overline{CE}$) must be HIGH at CMOS level to meet the I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.
12. I_{CCDR} is guaranteed only after device is first powered up to $V_{CC(min)}$ and then brought down to V_{DR}.
13. These parameters are guaranteed by design.
14. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)}$ > 100 µs or stable at $V_{CC(min)}$ > 100 µs.

Switching Characteristics

Over the operating range

Parameter [15]	Description	45 ns		Unit
		Min	Max	
Read Cycle				
t_{RC}	Read cycle time	45	–	ns
t_{AA}	Address to data valid	–	45	ns
t_{OHA}	Data hold from address change	10	–	ns
t_{ACE}	$\overline{CE}$ LOW to data valid	–	45	ns
t_{DOE}	$\overline{OE}$ LOW to data valid	–	22	ns
t_{LZOE}	$\overline{OE}$ LOW to low Z[16]	5	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to high Z[16, 17]	–	18	ns
t_{LZCE}	$\overline{CE}$ LOW to low Z[16]	10	–	ns
t_{HZCE}	$\overline{CE}$ HIGH to high Z[16, 17]	–	18	ns
t_{PU}	$\overline{CE}$ LOW to power-up	0	–	ns
t_{PD}	$\overline{CE}$ HIGH to power-down	–	45	ns
Write Cycle[18, 19]				
t_{WC}	Write cycle time	45	–	ns
t_{SCE}	$\overline{CE}$ LOW to write end	35	–	ns
t_{AW}	Address setup to write end	35	–	ns
t_{HA}	Address hold from write end	0	–	ns
t_{SA}	Address setup to write start	0	–	ns
t_{PWE}	$\overline{WE}$ pulse width	35	–	ns
t_{SD}	Data setup to write end	25	–	ns
t_{HD}	Data hold from write end	0	–	ns
t_{HZWE}	$\overline{WE}$ LOW to high Z[16, 17]	–	18	ns
t_{LZWE}	$\overline{WE}$ HIGH to low Z[16]	10	–	ns

Notes

15. Test conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3 V, and output loading of the specified I_{OL}/I_{OH} as shown in the Figure 2 on page 5.
16. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any device.
17. t_{HZOE}, t_{HZCE}, and t_{HZWE} transitions are measured when the outputs enter a high impedance state.
18. The internal wre.ite time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}$ = V_{IL}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.
19. The minimum write cycle pulse width for Write Cycle No. 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) should be equal to the sum of t_{SD} and t_{HZWE}.

Switching Waveforms

Figure 4. Read Cycle No. 1 (Address Transition Controlled) [20, 21]

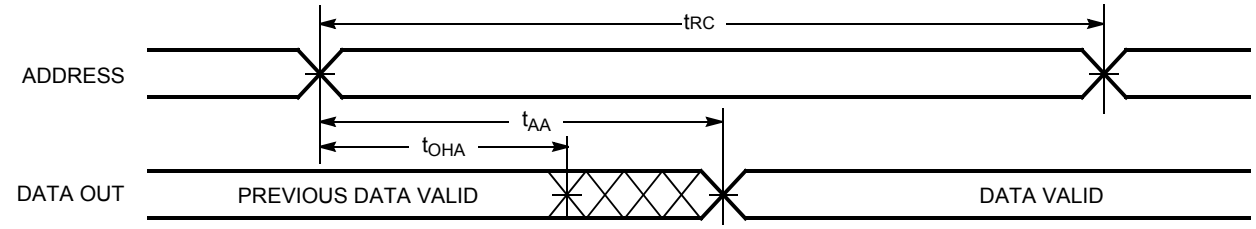


Figure 5. Read Cycle No. 2 ($\overline{OE}$ Controlled) [21, 22]

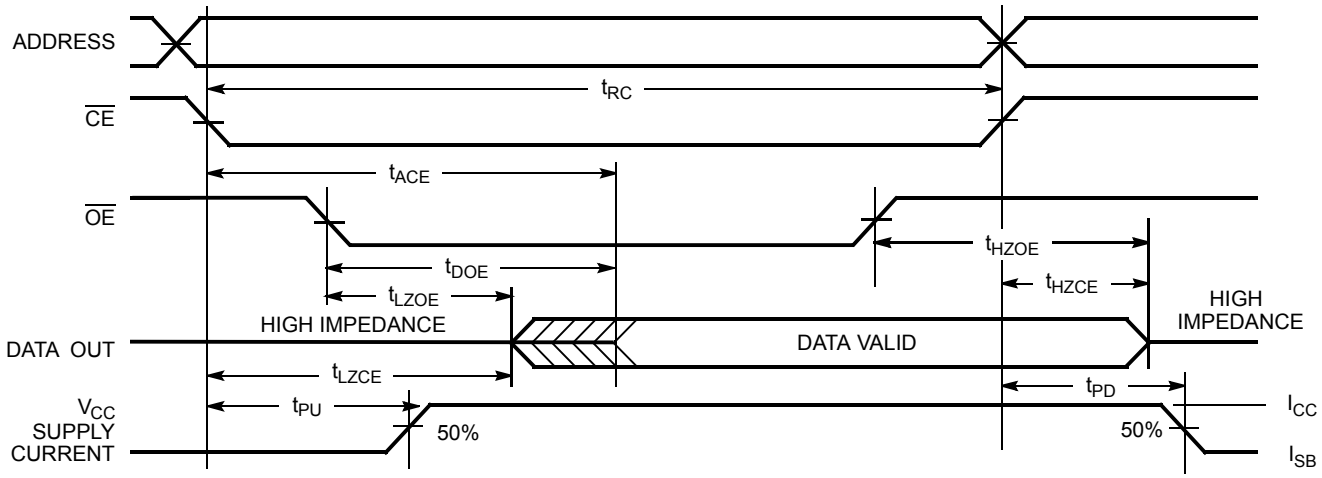
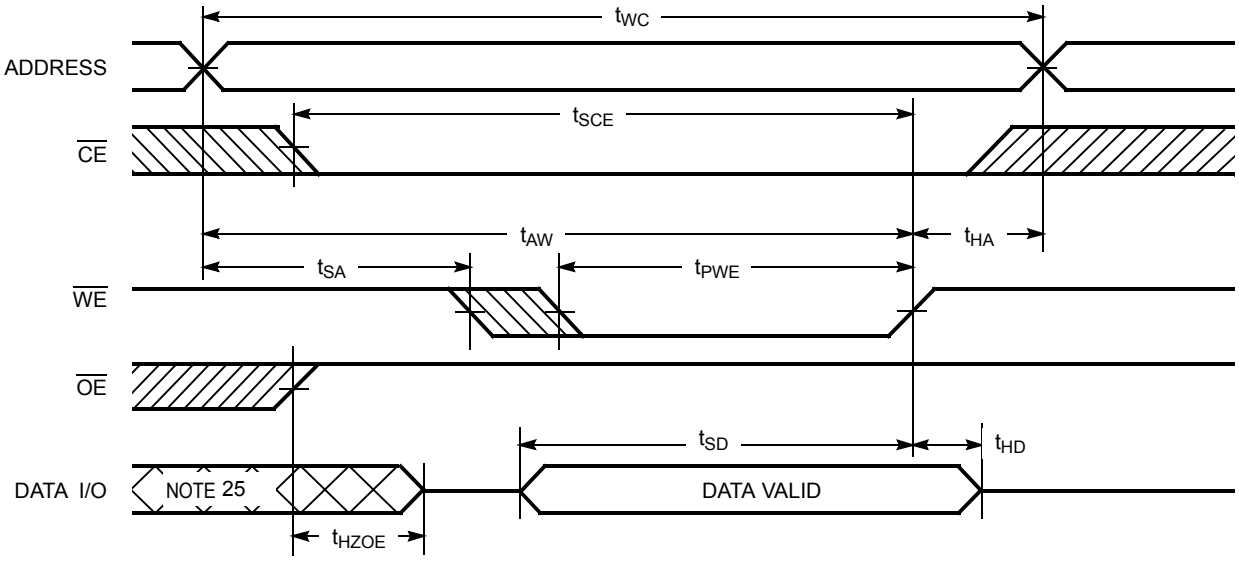


Figure 6. Write Cycle No. 1 ($\overline{WE}$ Controlled, $\overline{OE}$ HIGH During Write) [23, 24]



Notes
20. Device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}.
21. $\overline{WE}$ is HIGH for read cycles.
22. Address valid before or similar to $\overline{CE}$ transition LOW.
23. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
24. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in high impedance state.
25. During this period, the I/Os are in output state and input signals must not be applied.

Switching Waveforms (continued)

Figure 7. Write Cycle No. 2 ($\overline{CE}$ Controlled) [26, 27]

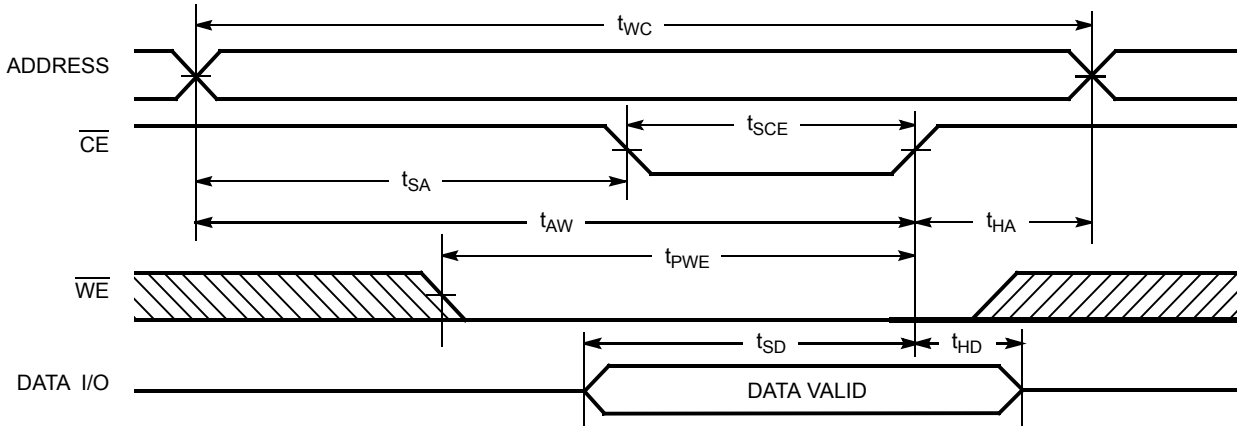
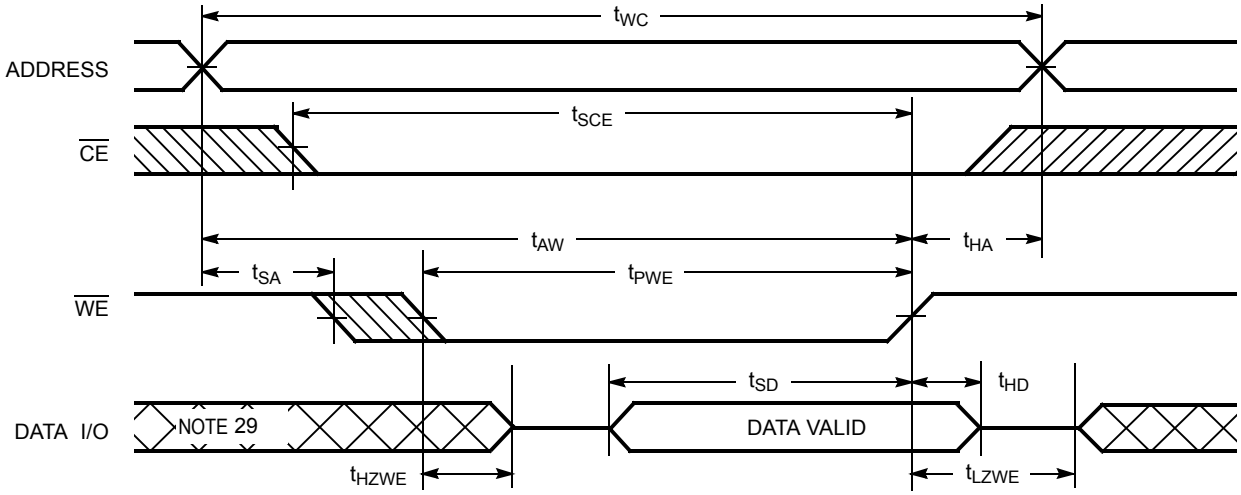


Figure 8. Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) [27, 28]



Notes

26. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
27. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in high impedance state.
28. The minimum write cycle pulse width should be equal to the sum of t_{SD} and t_{HZWE}.
29. During this period, the I/Os are in output state and input signals must not be applied.

Truth Table

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	I/O	Mode	Power
H [30]	X	X	High Z	Deselect/power-down	Standby (I_{SB})
L	H	L	Data out	Read	Active (I_{CC})
L	L	X	Data in	Write	Active (I_{CC})
L	H	H	High Z	Selected, outputs disabled	Active (I_{CC})

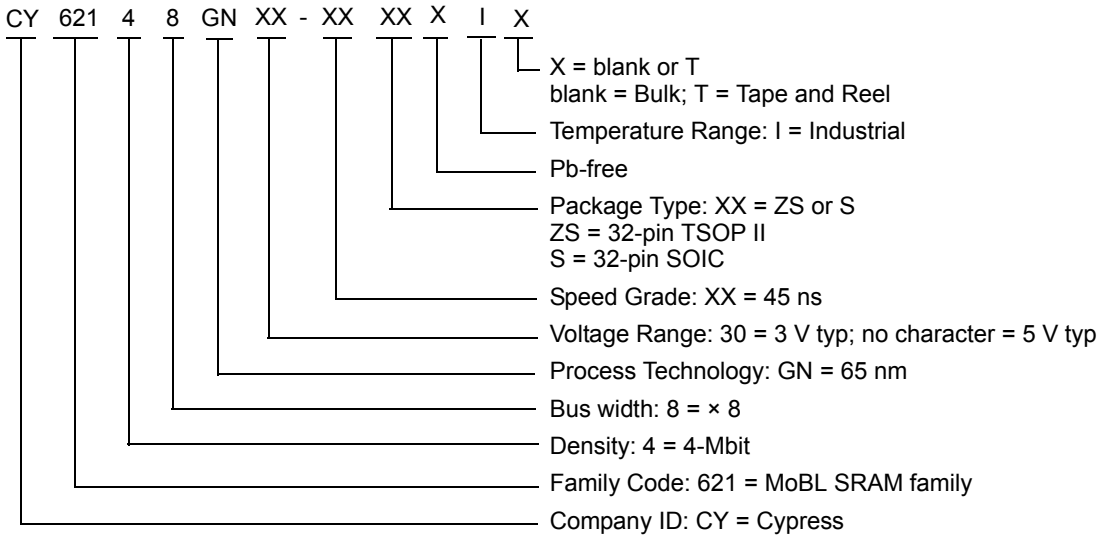
Note
30. Chip enable ($\overline{CE}$) must be HIGH at CMOS level to meet the I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.

Ordering Information

Table 1. Key features and Ordering Information

Speed (ns)	Voltage Range (V)	Ordering Code	Package Diagram	Package Type	Operating Range
45	2.2 V–3.6 V	CY62148GN30-45ZSXI	51-85095	32-pin TSOP II (Pb-free)	Industrial
		CY62148GN30-45ZSXIT	51-85095	32-pin TSOP II (Pb-free), Tape and Reel	
		CY62148GN30-45SXI	51-85081	32-pin SOIC (Pb-free)	
		CY62148GN30-45SXIT	51-85081	32-pin SOIC (Pb-free), Tape and Reel	
	4.5 V–5.5 V	CY62148GN-45ZSXI	51-85095	32-pin TSOP II (Pb-free)	
		CY62148GN-45ZSXIT	51-85095	32-pin TSOP II (Pb-free), Tape and Reel	
		CY62148GN-45SXI	51-85081	32-pin SOIC (Pb-free)	
		CY62148GN-45SXIT	51-85081	32-pin SOIC (Pb-free), Tape and Reel	

Ordering Code Definitions



Package Diagrams

Figure 9. 32-pin TSOP II (20.95 × 11.76 × 1.0 mm) ZS32 Package Outline, 51-85095

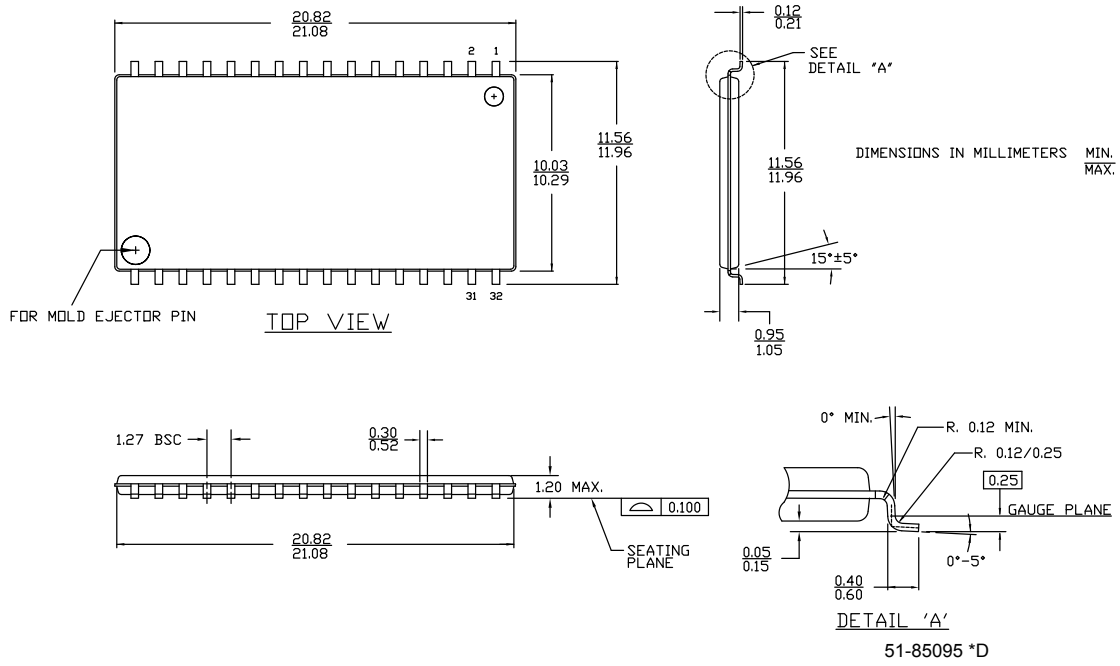
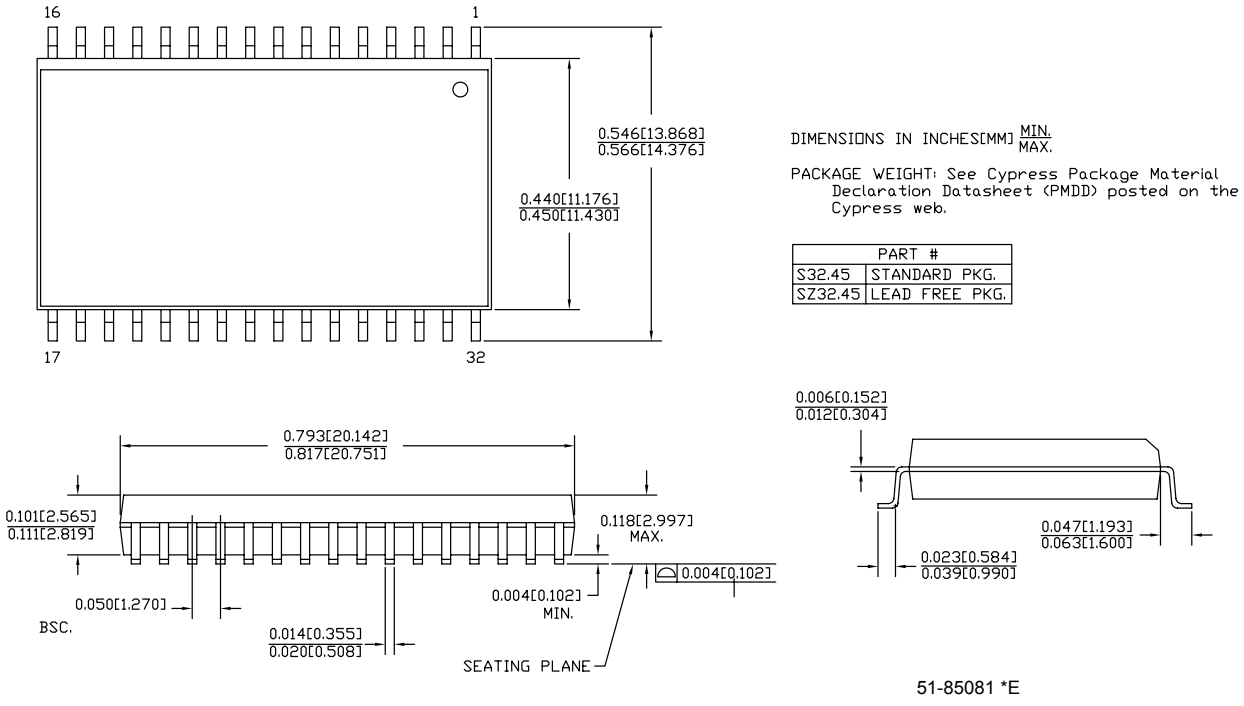


Figure 10. 32-pin SOIC (450 Mils) S32.45/SZ32.45 Package Outline, 51-85081



Acronyms

Table 2. Acronyms Used in this Document

Acronym	Description
$\overline{CE}$	chip enable
CMOS	complementary metal oxide semiconductor
I/O	input/output
$\overline{OE}$	output enable
MoBL	More Battery Life
SOIC	small outline integrated circuit
SRAM	static random access memory
TSOP	thin small outline package
$\overline{WE}$	write enable

Document Conventions

Units of Measure

Table 3. Units of Measure

Symbol	Unit of Measure
°C	Degrees Celsius
MHz	megahertz
µA	microamperes
µs	microseconds
mA	milliamperes
ns	nanoseconds
Ω	ohms
%	percent
pF	picofarads
V	volts
W	watts

Document History Page

Document Title: CY62148GN MoBL®, 4-Mbit (512K × 8) Static RAM Document Number: 001-95418				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	5056496	NILE	12/29/2015	New data sheet.
*A	5092456	NILE	01/19/2016	Added “2.2 V to 3.6 V” range related information in all instances across the document. Updated Ordering Information: Updated part numbers.
*B	5422041	NILE	09/09/2016	Updated Electrical Characteristics: Changed minimum value of V_{OH} parameter corresponding to “2.7 V to 3.6 V” from 2.2 V to 2.4 V. Changed minimum value of V_{IH} parameter corresponding to “2.2 V to 2.7 V” from 2.0 V to 1.8 V. Updated Ordering Information: Updated part numbers. Updated Disclaimer. Updated to new template.
*C	5546908	NILE	12/08/2016	Updated Ordering Information: No change in part numbers. Removed Disclaimer (text referencing to contact sales). Completing Sunset Review.
*D	6002325	AESATMP9	12/21/2017	Updated logo and copyright.

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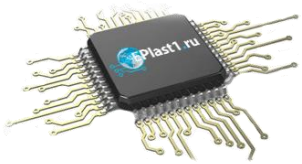
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



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