

SN54ALS373A, SN54AS373, SN74ALS373A, SN74AS373 OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

SDAS083C – APRIL 1982 – REVISED MARCH 2002

- Eight Latches in a Single Package
- 3-State Bus-Driving True Outputs
- Full Parallel Access for Loading
- Buffered Control Inputs
- pnp Inputs Reduce dc Loading on Data Lines

description

These octal transparent D-type latches feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the logic levels set up at the D inputs.

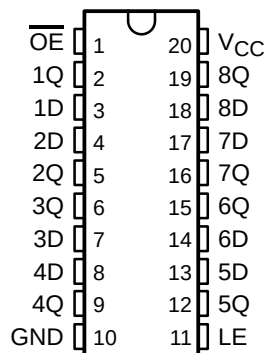
A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without interface or pullup components.

$\overline{OE}$ does not affect internal operations of the latches. Old data can be retained or new data can be entered while the outputs are off.

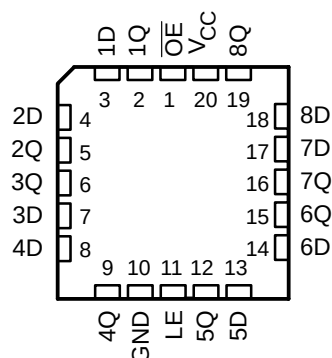
SN54ALS373A, . . . J OR W PACKAGE

SN54AS373 . . . J PACKAGE

SN74ALS373A, SN74AS373 . . . DW, N, OR NS PACKAGE
(TOP VIEW)



SN54ALS373A, SN54AS373 . . . FK PACKAGE
(TOP VIEW)



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

SN54ALS373A, SN54AS373, SN74ALS373A, SN74AS373
 OCTAL TRANSPARENT D-TYPE LATCHES
 WITH 3-STATE OUTPUTS

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ORDERING INFORMATION

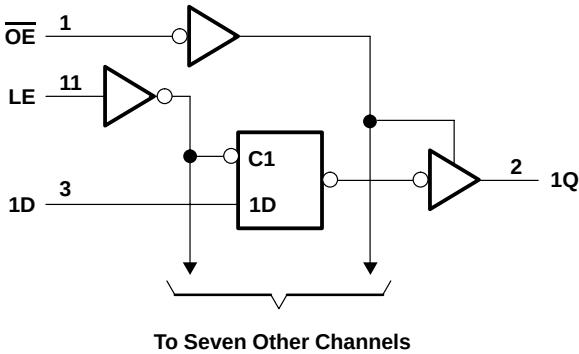
T _A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP – N	Tube	SN74ALS373AN	SN74ALS373AN
			SN74AS373N	SN74AS373N
	SOIC – DW	Tube	SN74ALS373ADW	ALS373A
		Tape and reel	SN74ALS373ADWR	
		Tube	SN74AS373DW	AS373
		Tape and reel	SN74AS373DWR	
–55°C to 125°C	SOP – NS	Tape and reel	SN74ALS373ANSR	ALS373A
			SN74AS373NSR	74AS373
	CDIP – J	Tube	SNJ54ALS373AJ	SNJ54ALS373AJ
			SNJ54AS373J	SNJ54AS373J
	CFP – W	Tube	SNJ54ALS373AW	SNJ54ALS373AW
			SNJ54ALS373AFK	SNJ54ALS373AFK
	LCCC – FK	Tube	SNJ54AS373FK	SNJ54AS373FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE
 (each latch)

INPUTS			OUTPUT Q
$\overline{OE}$	LE	D	
L	H	H	H
L	H	L	L
L	L	X	Q ₀
H	X	X	Z

logic diagram (positive logic)



SN54ALS373A, SN54AS373, SN74ALS373A, SN74AS373 OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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absolute maximum ratings over operating free-air temperature range (SN54ALS373A, SN74ALS373A) (unless otherwise noted)[†]

Supply voltage, V_{CC}	7 V
Input voltage, V_I	7 V
Voltage applied to any output in the high state or power-off state	5.5 V
Package thermal impedance, θ_{JA} (see Note 1): DW package	58°C/W
N package	69°C/W
NS package	60°C/W
Storage temperature range, T_{Stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

		SN54ALS373A			SN74ALS373A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			–1			–2.6	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	–55		125	0		70	°C

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

		SN54ALS373A		SN74ALS373A		UNIT
		MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency					MHz
t_W	Pulse duration, LE high	12		10		ns
t_{su}	Setup time, data before LE↓	10		10		ns
t_h	Hold time, data after LE↓	7		7		ns



SN54ALS373A, SN54AS373, SN74ALS373A, SN74AS373

OCTAL TRANSPARENT D-TYPE LATCHES

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS373A			SN74ALS373A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V _{IK}	V _{CC} = 4.5 V, I _I = −18 mA		−1.5			−1.5			V
V _{OH}	V _{CC} = 4.5 V to 5.5 V, I _{OH} = −0.4 mA		V _{CC} −2			V _{CC} −2			V
	V _{CC} = 4.5 V	I _{OH} = −1 mA	2.4	3.3					
		I _{OH} = −2.6 mA				2.4	3.2		
V _{OL}	V _{CC} = 4.5 V	I _{OL} = 12 mA	0.25	0.4	0.25	0.4	V		
		I _{OL} = 24 mA				0.35		0.5	
I _{OZH}	V _{CC} = 5.5 V, V _O = 2.7 V		20			20			μA
I _{OZL}	V _{CC} = 5.5 V, V _O = 0.4 V		−20			−20			μA
I _I	V _{CC} = 5.5 V, V _I = 7 V		0.1			0.1			mA
I _{IH}	V _{CC} = 5.5 V, V _I = 2.7 V		20			20			μA
I _{IL}	V _{CC} = 5.5 V, V _I = 0.4 V		−0.1			−0.1			mA
I _O ‡	V _{CC} = 5.5 V, V _O = 2.25 V		−20	−112	−30	−112	mA		
I _{CC}	V _{CC} = 5.5 V	Outputs high	9	16	9	16	mA		
		Outputs low	16	25	16	25			
		Outputs disabled	17	27	17	27			

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit output current, I_{OS} .

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R ₁ = 500 Ω, R ₂ = 500 Ω, T _A = MIN to MAX§				UNIT
			SN54ALS373A		SN74ALS373A		
			MIN	MAX	MIN	MAX	
t _{PLH}	D	Q	2	17	2	12	ns
t _{PHL}			1	19	4	16	
t _{PLH}	LE	Any Q	6	29	6	22	ns
t _{PHL}			1	27	7	23	
t _{PZH}	$\overline{\text{OE}}$	Any Q	6	22	1	18	ns
t _{PZL}			5	24	5	20	
t _{PHZ}	$\overline{\text{OE}}$	Any Q	2	16	1	10	ns
t _{PLZ}			2	24	2	12	

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

SN54ALS373A, SN54AS373, SN74ALS373A, SN74AS373

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absolute maximum ratings over operating free-air temperature range (SN54AS373, SN74AS373) (unless otherwise noted)[†]

Supply voltage, V_{CC}	7 V
Input voltage, V_I	7 V
Voltage applied to any output in the high state or power-off state	5.5 V
Package thermal impedance, θ_{JA} (see Note 1): DW package	58°C/W
N package	69°C/W
NS package	60°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 2: The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

		SN54AS373			SN74AS373			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			–12			–15	mA
I_{OL}	Low-level output current			32			48	mA
T_A	Operating free-air temperature	–55		125	0		70	°C

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

		SN54AS373		SN74AS373		UNIT
		MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency					MHz
t_W	Pulse duration, LE high	5.5*		4.5*		ns
t_{su}	Setup time, data before LE↓	2*		2*		ns
t_h	Hold time, data after LE↓	3*		3*		ns

* On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data but is not production tested.



SN54ALS373A, SN54AS373, SN74ALS373A, SN74AS373

OCTAL TRANSPARENT D-TYPE LATCHES

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54AS373			SN74AS373			UNIT
					MIN	TYP†	MAX	
V_{IK}	$V_{CC} = 4.5\text{ V}$, $I_I = -18\text{ mA}$			-1.2			-1.2	V
V_{OH}	$V_{CC} = 4.5\text{ V to } 5.5\text{ V}$, $I_{OH} = -2\text{ mA}$	$V_{CC}-2$			$V_{CC}-2$			V
	$V_{CC} = 4.5\text{ V}$	$I_{OH} = -12\text{ mA}$		2.4	3.2			
		$I_{OH} = -15\text{ mA}$				2.4	3.3	
V_{OL}	$V_{CC} = 4.5\text{ V}$	$I_{OL} = 32\text{ mA}$		0.27	0.5			V
		$I_{OL} = 48\text{ mA}$				0.32	0.5	
I_{OZH}	$V_{CC} = 5.5\text{ V}$, $V_O = 2.7\text{ V}$	50			50			μA
I_{OZL}	$V_{CC} = 5.5\text{ V}$, $V_O = 0.4\text{ V}$	-50			-50			μA
I_I	$V_{CC} = 5.5\text{ V}$, $V_I = 7\text{ V}$	0.1			0.1			mA
I_{IH}	$V_{CC} = 5.5\text{ V}$, $V_I = 2.7\text{ V}$	20			20			μA
I_{IL}	$V_{CC} = 5.5\text{ V}$, $V_I = 0.4\text{ V}$	-0.02			-0.02			mA
$I_O^\ddagger$	$V_{CC} = 5.5\text{ V}$, $V_O = 2.25\text{ V}$	-30			-112			mA
I_{CC}	$V_{CC} = 5.5\text{ V}$	Outputs high		55	90	55	90	mA
		Outputs low		55	85	55	85	
		Outputs disabled		65	100	65	100	

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit output current, I_{OS} .

switching characteristics (see Figure 1)

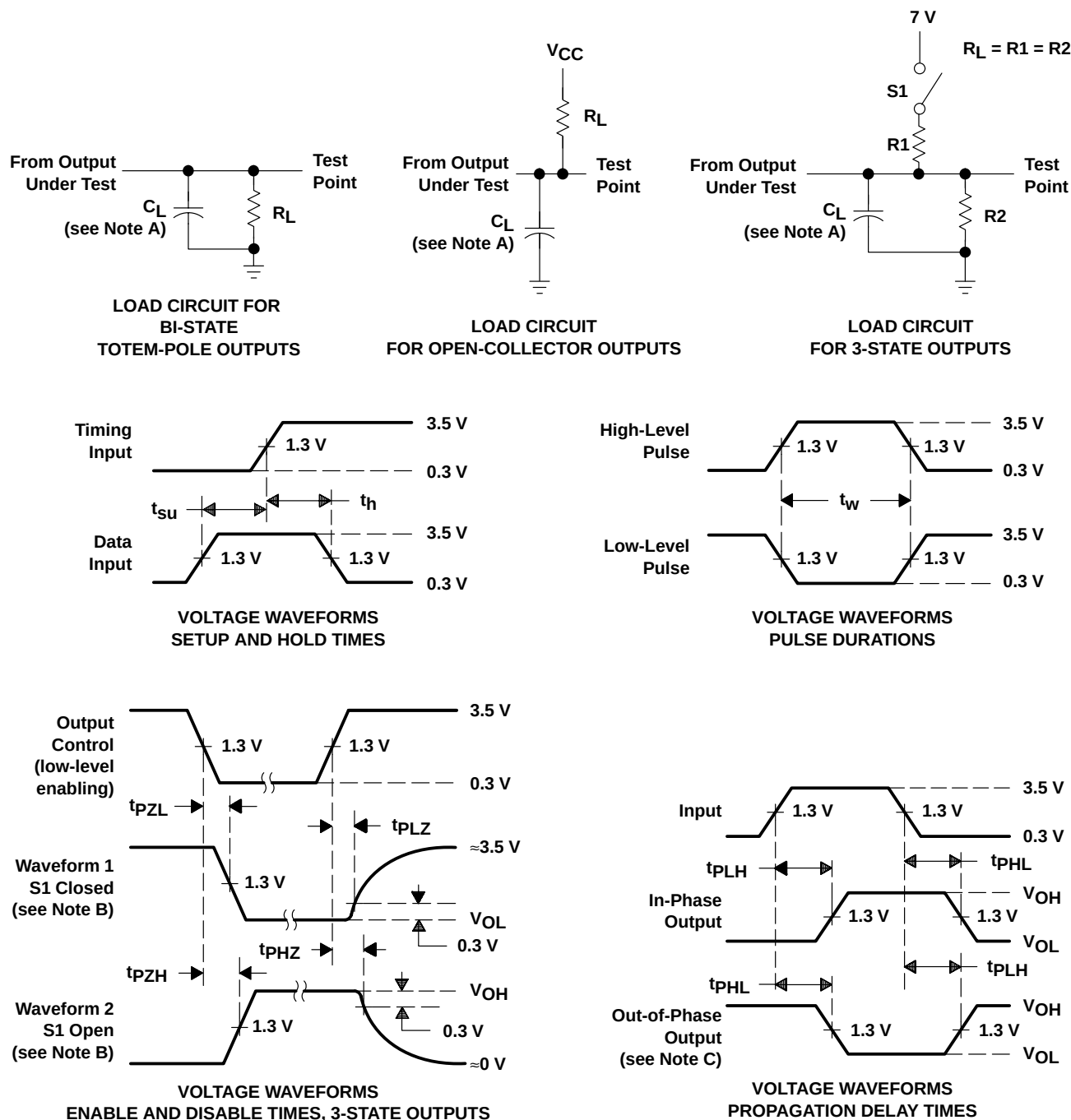
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T _A = MIN to MAX§				UNIT
			SN54AS373		SN74AS373		
			MIN	MAX	MIN	MAX	
t _{PLH}	D	Q	3	9	3.5	6	ns
t _{PHL}			3	8	3.5	6	
t _{PLH}	LE	Any Q	6.5	14.5	6.5	11.5	ns
t _{PHL}			5	9	5	7.5	
t _{PZH}	$\overline{\text{OE}}$	Any Q	2	7.5	2	6.5	ns
t _{PZL}			4.5	10.5	4.5	9.5	
t _{PHZ}	$\overline{\text{OE}}$	Any Q	3	10	3	6.5	ns
t _{PLZ}			3	8	3	7	

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

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PARAMETER MEASUREMENT INFORMATION SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
 D. All input pulses have the following characteristics: $PRR \leq 1$ MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
 E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
83020012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
8302001RA	ACTIVE	CDIP	J	20	1	TBD	Call TI	N / A for Pkg Type
8302001SA	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type
JM38510/37203B2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
JM38510/37203BRA	ACTIVE	CDIP	J	20	1	TBD	Call TI	N / A for Pkg Type
SN54ALS373AJ	ACTIVE	CDIP	J	20	1	TBD	Call TI	N / A for Pkg Type
SN54AS373J	ACTIVE	CDIP	J	20	1	TBD	Call TI	N / A for Pkg Type
SN74ALS373ADBLE	OBSOLETE	SSOP	DB	20		TBD	Call TI	Call TI
SN74ALS373ADBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS373ADBRG4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS373ADW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS373ADWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS373ADWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS373ADWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS373ADWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS373ADWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS373AN	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74ALS373AN3	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI
SN74ALS373ANE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74ALS373ANSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS373ANSRE4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS373ANSRG4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AS373DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AS373DWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AS373DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AS373DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AS373DWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AS373DWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AS373N	ACTIVE	PDIP	N	20	20	Pb-Free	CU NIPDAU	N / A for Pkg Type

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
(RoHS)								
SN74AS373N3	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI
SN74AS373NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74AS373NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AS373NSRE4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AS373NSRG4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SNJ54ALS373AFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54ALS373AJ	ACTIVE	CDIP	J	20	1	TBD	Call TI	N / A for Pkg Type
SNJ54ALS373AW	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type
SNJ54AS373FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54AS373J	ACTIVE	CDIP	J	20	1	TBD	Call TI	N / A for Pkg Type

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

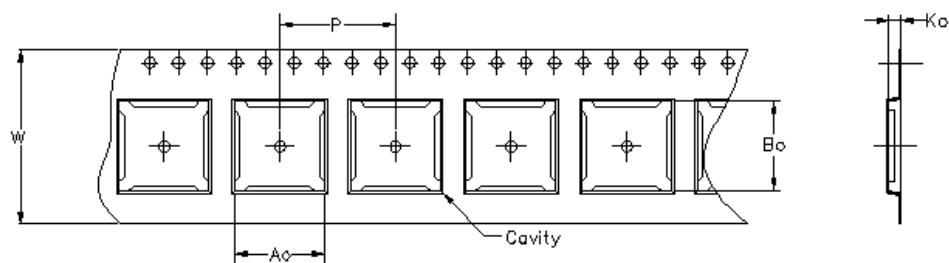
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

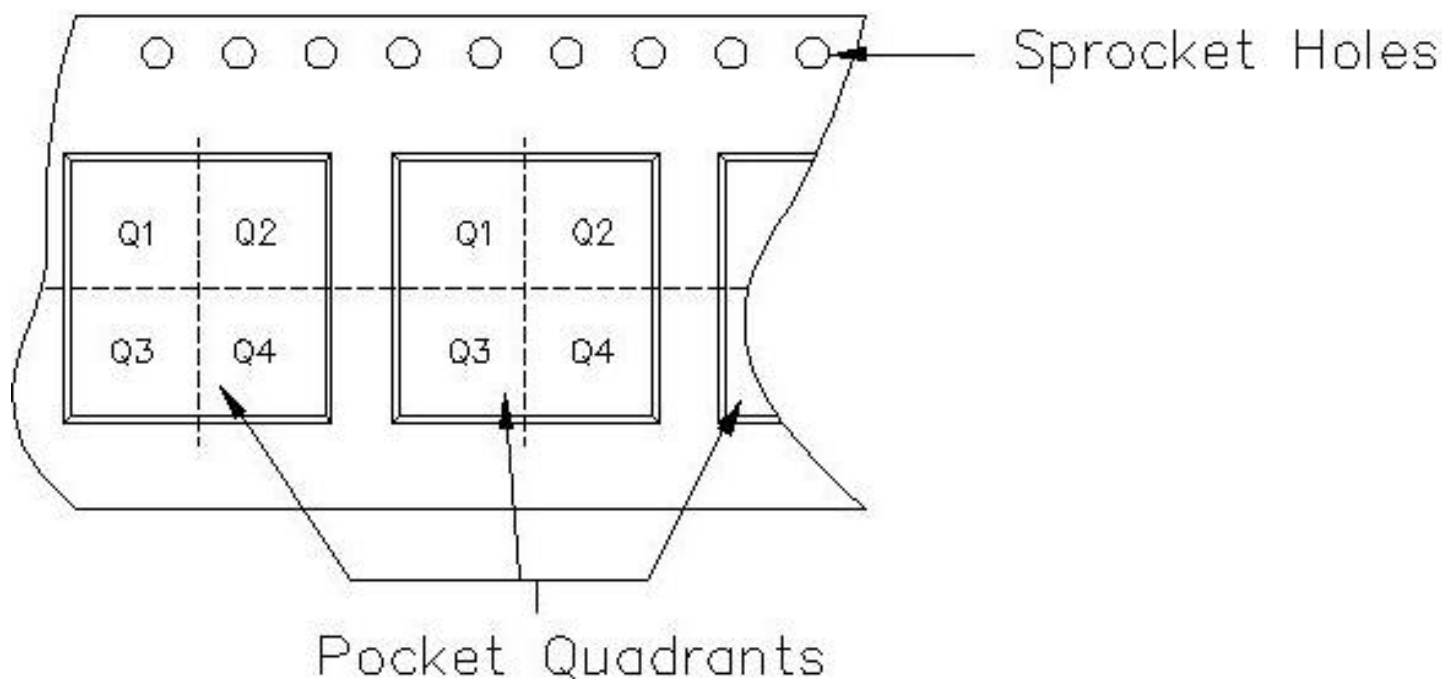
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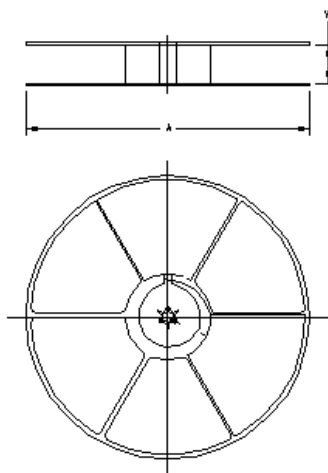
Carrier tape design is defined largely by the component length, width, and thickness.

A_o = Dimension designed to accommodate the component width.
B_o = Dimension designed to accommodate the component length.
K_o = Dimension designed to accommodate the component thickness.
W = Overall width of the carrier tape.
P = Pitch between successive cavity centers.



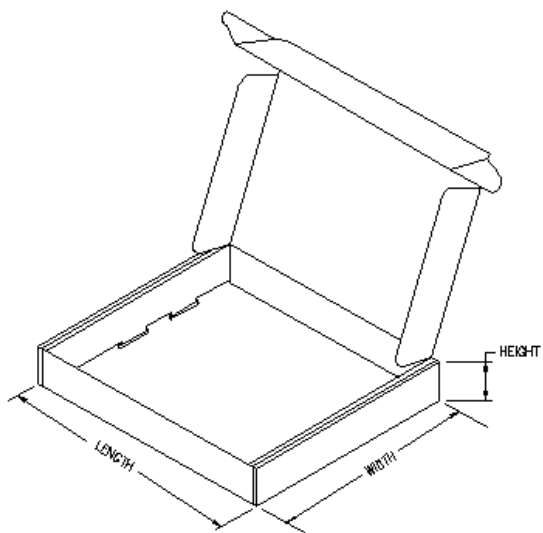
TAPE AND REEL INFORMATION

Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALS373ADBR	DB	20	MLA	330	16	8.2	7.5	2.5	12	16	Q1
SN74ALS373ADWR	DW	20	MLA	330	24	10.8	13.0	2.7	12	24	Q1
SN74ALS373ANSR	NS	20	MLA	330	24	8.2	13.0	2.5	12	24	Q1
SN74AS373DWR	DW	20	MLA	330	24	10.8	13.0	2.7	12	24	Q1
SN74AS373NSR	NS	20	MLA	330	24	8.2	13.0	2.5	12	24	Q1



TAPE AND REEL BOX INFORMATION

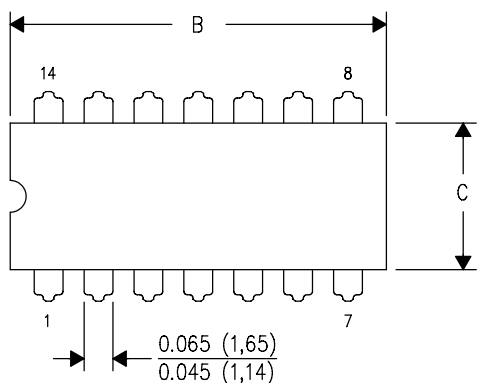
Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
SN74ALS373ADBR	DB	20	MLA	346.0	346.0	33.0
SN74ALS373ADWR	DW	20	MLA	333.2	333.2	31.75
SN74ALS373ANSR	NS	20	MLA	333.2	333.2	31.75
SN74AS373DWR	DW	20	MLA	333.2	333.2	31.75
SN74AS373NSR	NS	20	MLA	333.2	333.2	31.75



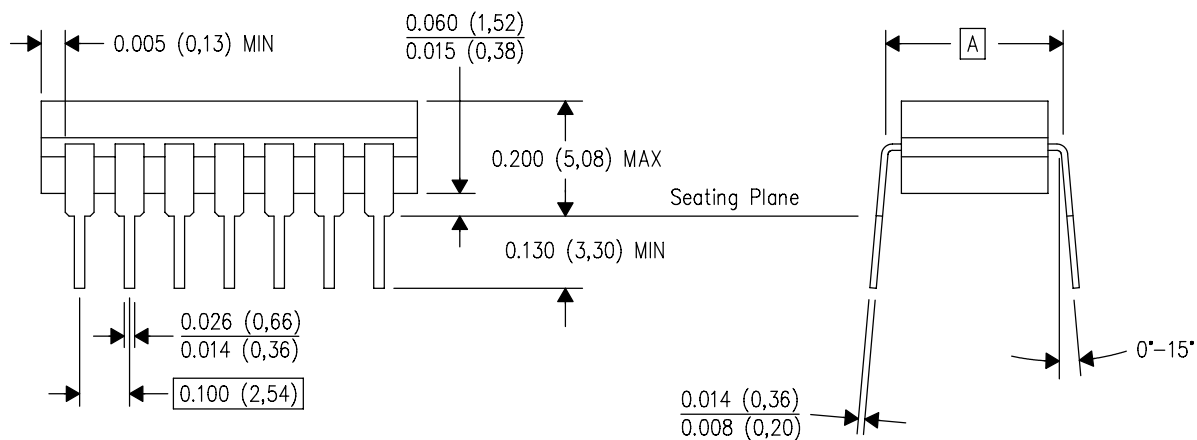
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

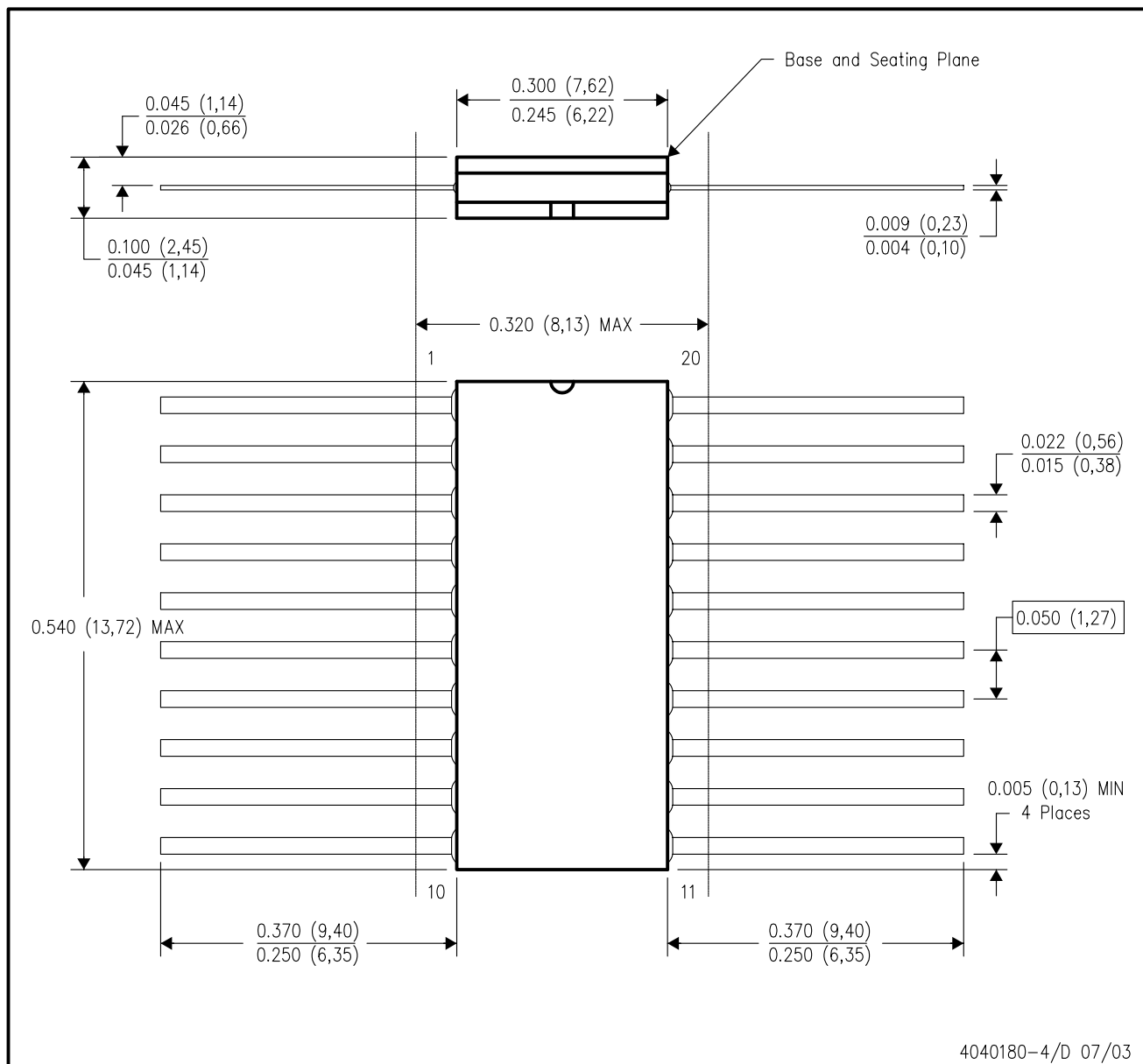


4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



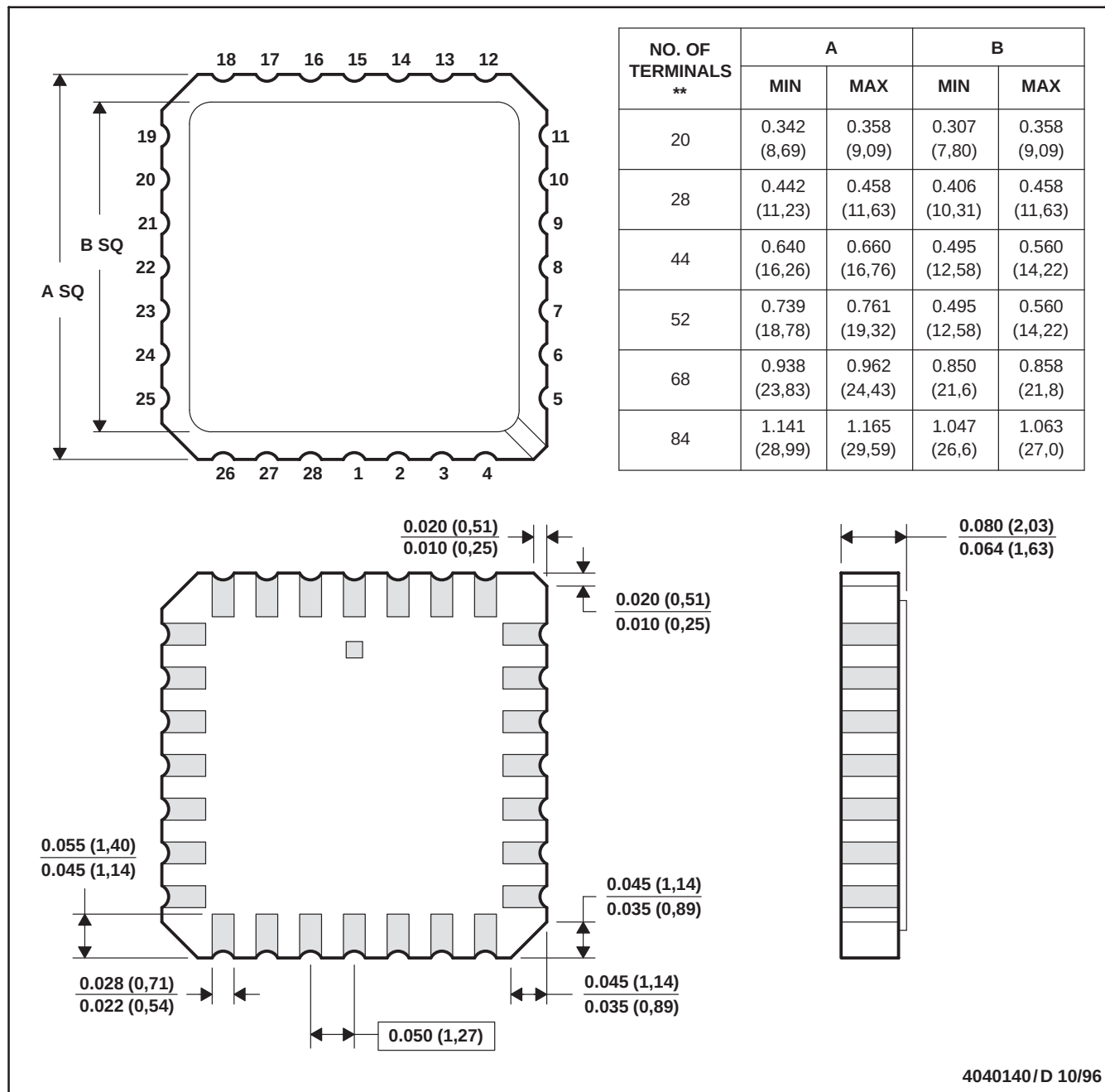
NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within Mil-Std 1835 GDFP2-F20

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN

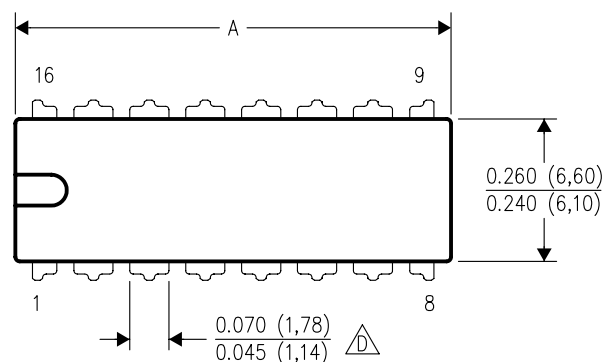


- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a metal lid.
 - D. The terminals are gold plated.
 - E. Falls within JEDEC MS-004

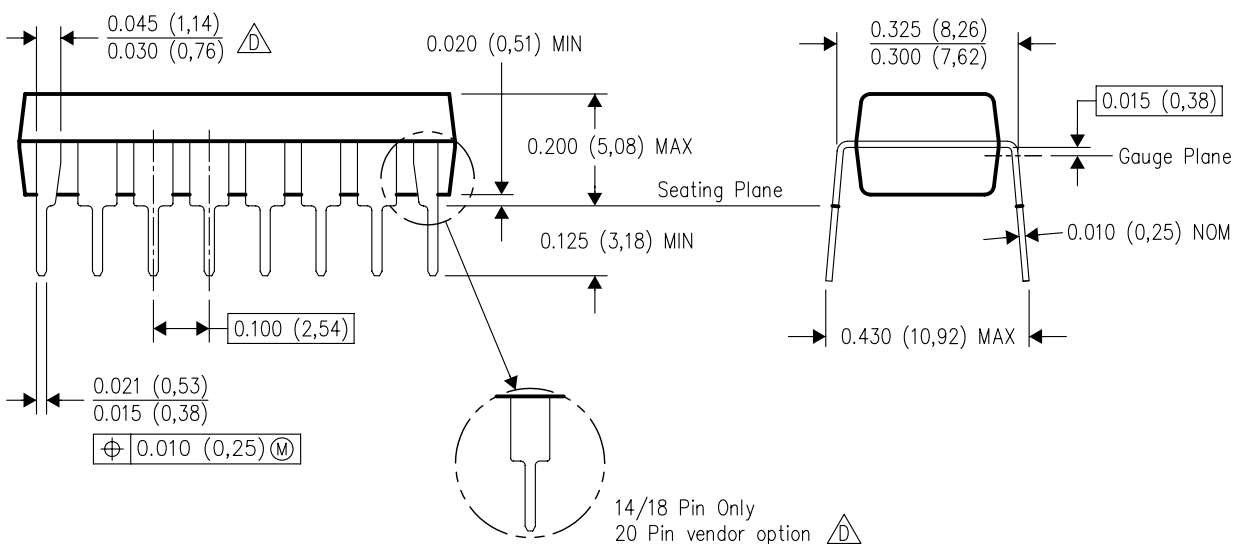
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



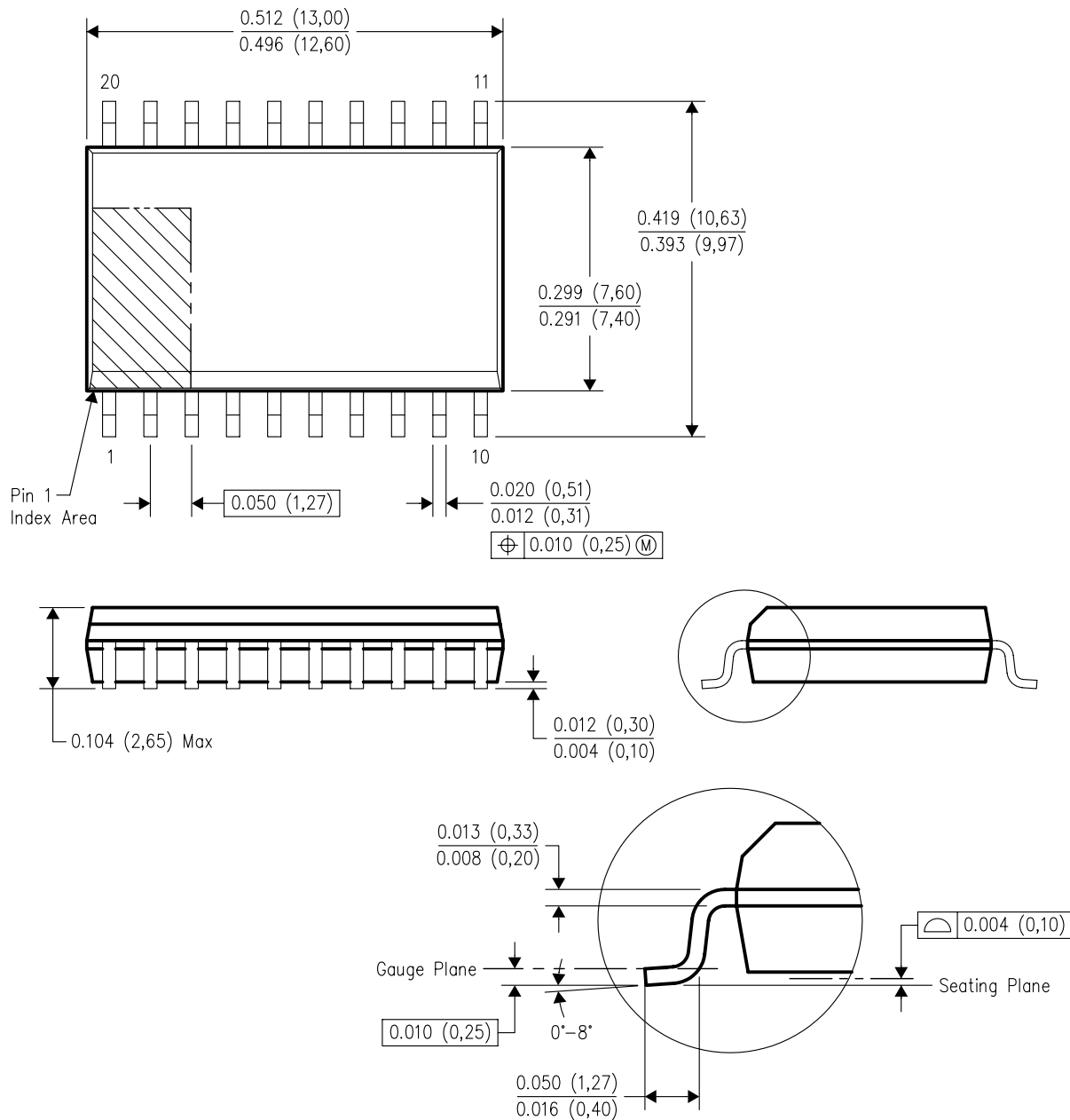
4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW (R-PDSO-G20)

PLASTIC SMALL-OUTLINE PACKAGE



4040000-4/F 06/2004

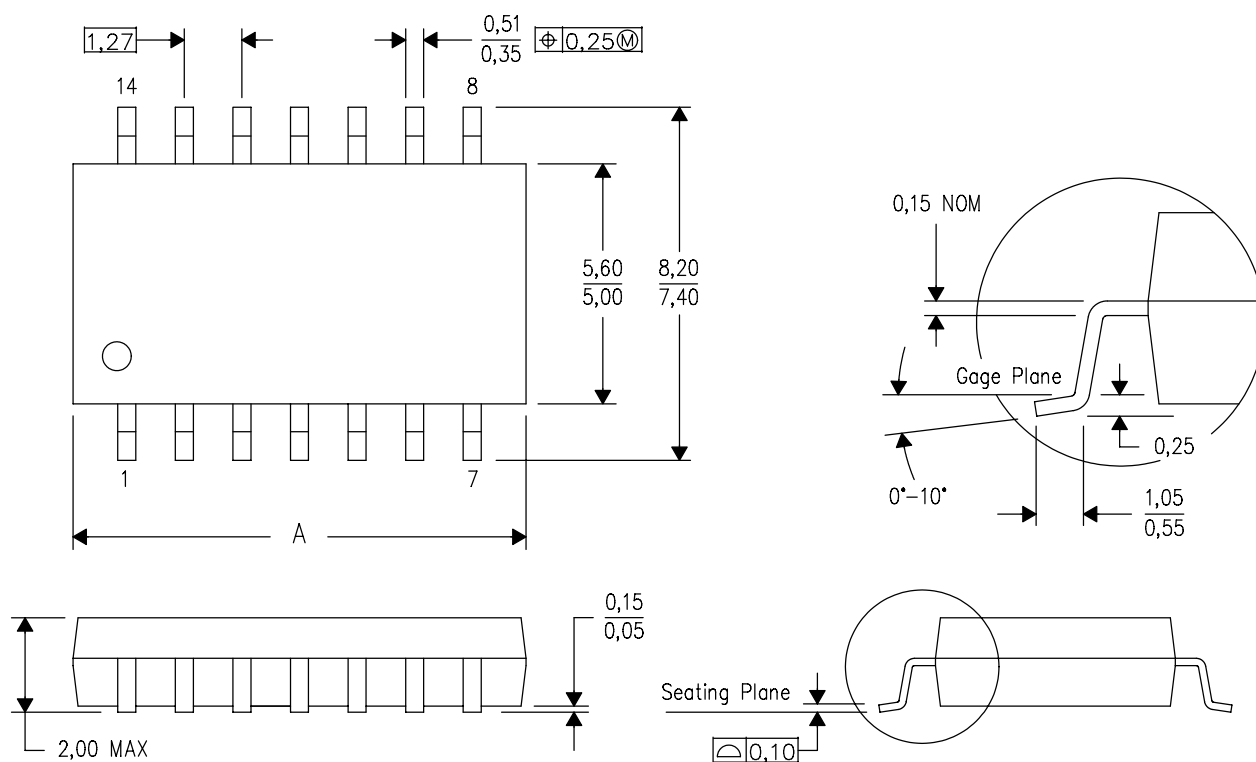
- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - Falls within JEDEC MS-013 variation AC.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

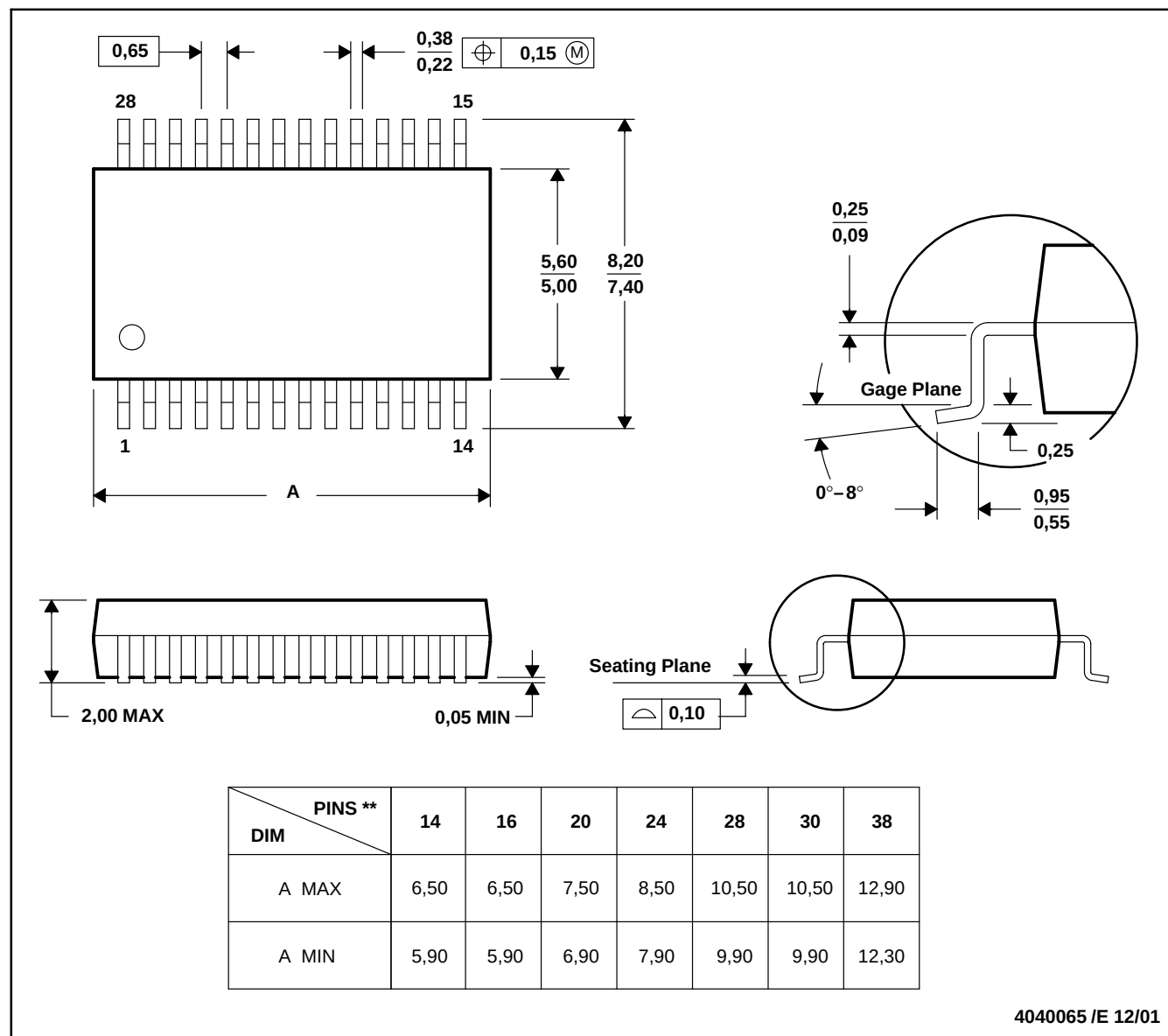
4040062/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

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- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
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