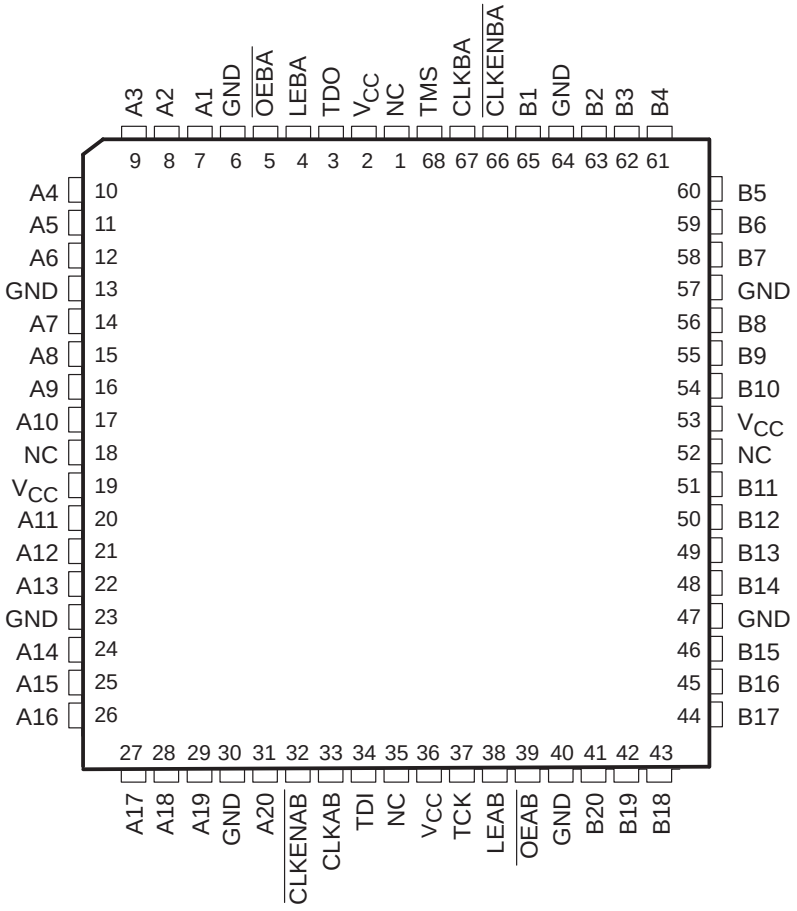
- **Members of the Texas Instruments *SCOPE*™ Family of Testability Products**
- **Members of the Texas Instruments *Widebus*™ Family**
- **Compatible With the IEEE Standard 1149.1-1990 (JTAG) Test Access Port and Boundary-Scan Architecture**
- ***UBT*™ (Universal Bus Transceiver) Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Mode**
- **Two Boundary-Scan Cells per I/O for Greater Flexibility**
- **State-of-the-Art *EPIC*-II*B*™ BiCMOS Design Significantly Reduces Power Dissipation**
- ***SCOPE*™ Instruction Set**
  - **IEEE Standard 1149.1-1990 Required Instructions, Optional INTEST, and P1149.1A CLAMP and HIGHZ**
  - **Parallel Signature Analysis at Inputs With Masking Option**
  - **Pseudo-Random Pattern Generation From Outputs**
  - **Sample Inputs/Toggle Outputs**
  - **Binary Count From Outputs**
  - **Device Identification**
  - **Even-Parity Opcodes**
- **Packaged in 64-Pin Plastic Thin Quad Flat Pack Using 0.5-mm Center-to-Center Spacings and 68-Pin Ceramic Quad Flat Pack Using 25-mil Center-to-Center Spacings**

SN54ABT18504 . . . HV PACKAGE
(TOP VIEW)



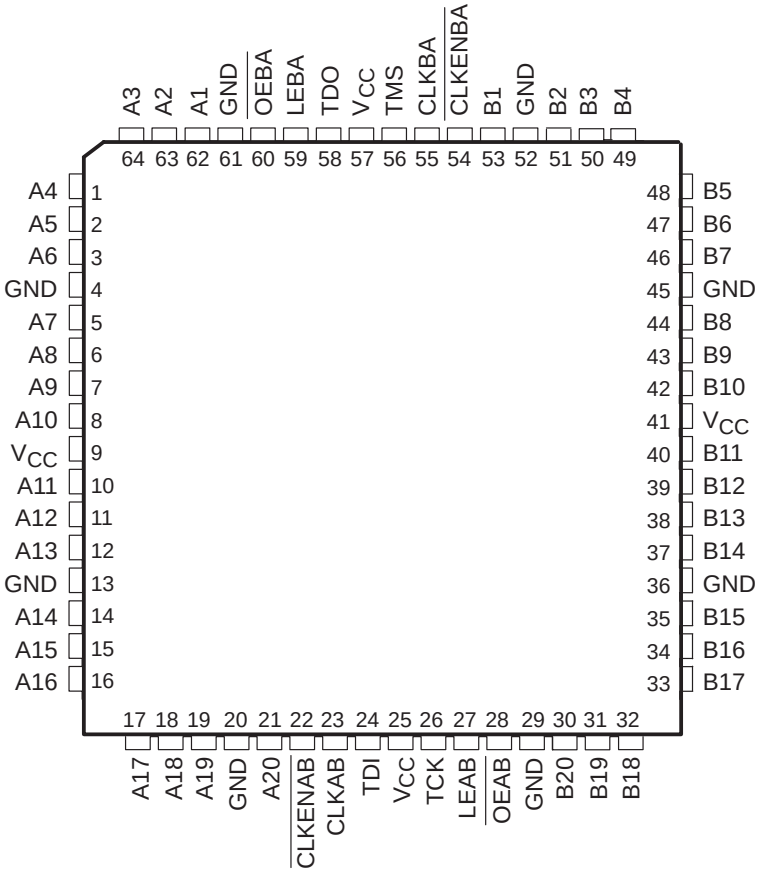
NC – No internal connection

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SN74ABT18504 . . . PM PACKAGE
(TOP VIEW)



description

The SN54ABT18504 and SN74ABT18504 scan test devices with 20-bit universal bus transceivers are members of the Texas Instruments SCOPE™ testability IC family. This family of devices supports IEEE Standard 1149.1-1990 boundary scan to facilitate testing of complex circuit board assemblies. Scan access to the test circuitry is accomplished via the 4-wire test access port (TAP) interface.

In the normal mode, these devices are 20-bit universal bus transceivers that combine D-type latches and D-type flip-flops to allow data flow in transparent, latched, or clocked modes. The test circuitry can be activated by the TAP to take snapshot samples of the data appearing at the device pins or to perform a self test on the boundary test cells. Activating the TAP in the normal mode does not affect the functional operation of the SCOPE™ universal bus transceivers.

Data flow in each direction is controlled by output-enable ($\overline{OEAB}$ and $\overline{OEBA}$), latch-enable (LEAB and LEBA), clock-enable ($\overline{CLKENAB}$ and $\overline{CLKENBA}$), and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A-bus data is latched while $\overline{CLKENAB}$ is high and/or CLKAB is held at a static low or high logic level. Otherwise, if LEAB is low and $\overline{CLKENAB}$ is low, A-bus data is stored on a low-to-high transition of CLKAB. When $\overline{OEAB}$ is low, the B outputs are active. When $\overline{OEAB}$ is high, the B outputs are in the high-impedance state. B-to-A data flow is similar to A-to-B data flow but uses the $\overline{OEBA}$, LEBA, $\overline{CLKENBA}$, and CLKBA inputs.

In the test mode, the normal operation of the SCOPE™ universal bus transceivers is inhibited, and the test circuitry is enabled to observe and control the I/O boundary of the device. When enabled, the test circuitry performs boundary scan test operations according to the protocol described in IEEE Standard 1149.1-1990.

description (continued)

Four dedicated test pins are used to observe and control the operation of the test circuitry: test data input (TDI), test data output (TDO), test mode select (TMS), and test clock (TCK). Additionally, the test circuitry can perform other testing functions such as parallel signature analysis on data inputs and pseudo-random pattern generation from data outputs. All testing and scan operations are synchronized to the TAP interface.

Additional flexibility is provided in the test mode through the use of two boundary scan cells (BSCs) for each I/O pin. This allows independent test data to be captured and forced at either bus (A or B). A PSA/COUNT instruction is also included to ease the testing of memories and other circuits where a binary count addressing scheme is useful.

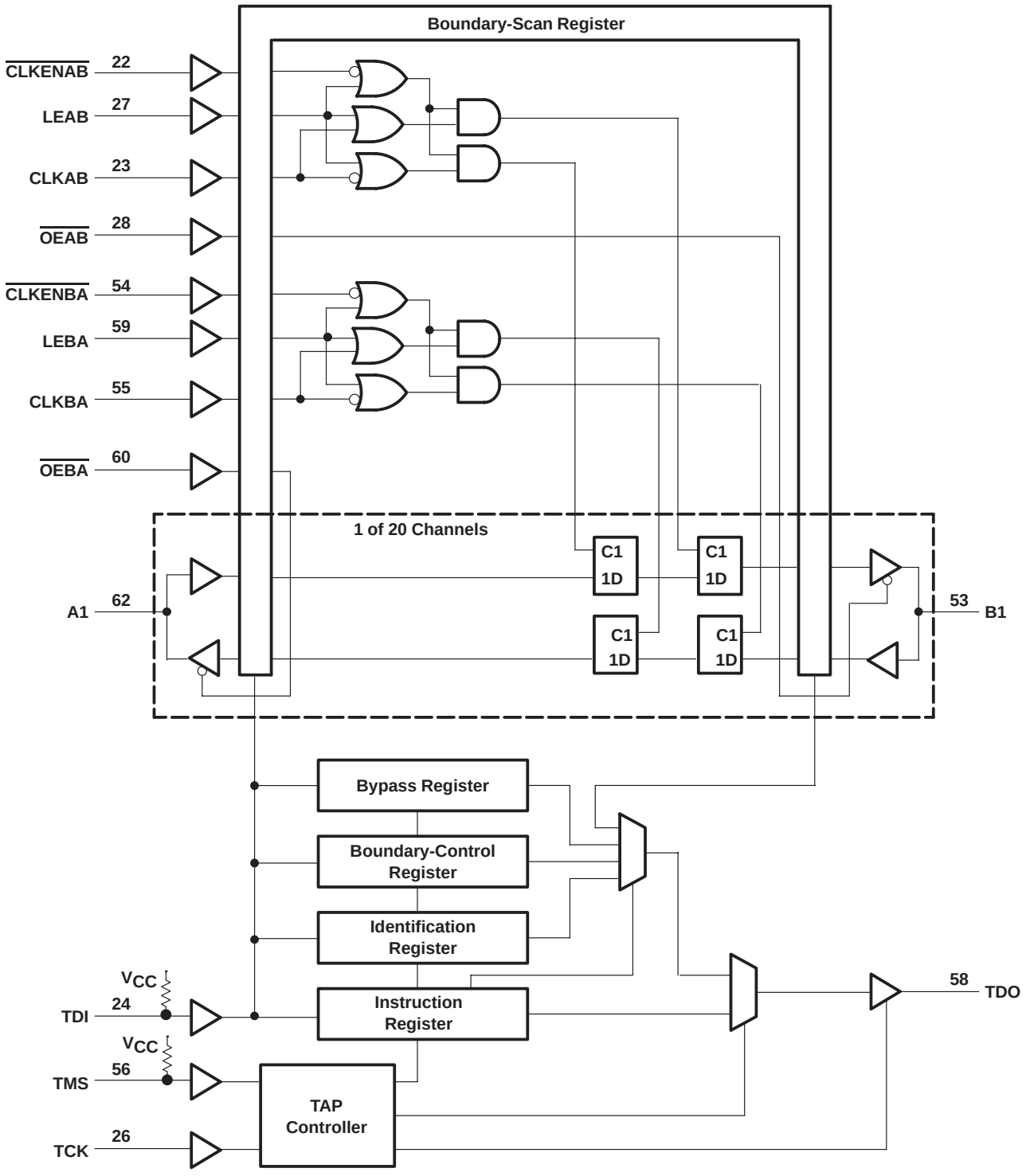
The SN54ABT18504 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ABT18504 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE†
(normal mode, each register)

INPUTS					OUTPUT
$\overline{\text{OEAB}}$	LEAB	$\overline{\text{CLKENAB}}$	CLKAB	A	B
L	L	L	L	X	B_0‡
L	L	L	↑	L	L
L	L	L	↑	H	H
L	L	H	X	X	B_0‡
L	H	X	X	L	L
L	H	X	X	H	H
H	X	X	X	X	Z

† A-to-B data flow is shown. B-to-A data flow is similar but uses $\overline{\text{OEBA}}$, LEBA, $\overline{\text{CLKENBA}}$, and CLKBA.
‡ Output level before the indicated steady-state input conditions were established.

functional block diagram



Pin numbers shown are for the PM package.

Terminal Functions

PIN NAME	DESCRIPTION
A1 – A20	Normal-function A-bus I/O ports. See function table for normal-mode logic.
B1 – B20	Normal-function B-bus I/O ports. See function table for normal-mode logic.
CLKAB, CLKBA	Normal-function clock inputs. See function table for normal-mode logic.
$\overline{\text{CLKENAB}}$, $\overline{\text{CLKENBA}}$	Normal-function clock enables. See function table for normal-mode logic.
GND	Ground
LEAB, LEBA	Normal-function latch enables. See function table for normal-mode logic.
$\overline{\text{OEAB}}$, $\overline{\text{OEBA}}$	Normal-function output enables. See function table for normal-mode logic.
TCK	Test clock. One of four pins required by IEEE Standard 1149.1-1990. Test operations of the device are synchronous to the test clock. Data is captured on the rising edge of TCK and outputs change on the falling edge of TCK.
TDI	Test data input. One of four pins required by IEEE Standard 1149.1-1990. The test data input is the serial input for shifting data through the instruction register or selected data register. An internal pullup forces TDI to a high level if left unconnected.
TDO	Test data output. One of four pins required by IEEE Standard 1149.1-1990. The test data output is the serial output for shifting data through the instruction register or selected data register.
TMS	Test mode select. One of four pins required by IEEE Standard 1149.1-1990. The test mode select input directs the device through its test access port (TAP) controller states. An internal pullup forces TMS to a high level if left unconnected.
V_{CC}	Supply voltage

test architecture

Serial test information is conveyed by means of a 4-wire test bus or test access port (TAP), that conforms to IEEE Standard 1149.1-1990. Test instructions, test data, and test control signals are all passed along this serial test bus. The TAP controller monitors two signals from the test bus, namely TCK and TMS. The function of the TAP controller is to extract the synchronization (TCK) and state control (TMS) signals from the test bus and generate the appropriate on-chip control signals for the test structures in the device. Figure 1 shows the TAP controller state diagram.

The TAP controller is fully synchronous to the TCK signal. Input data is captured on the rising edge of TCK and output data changes on the falling edge of TCK. This scheme ensures that data to be captured is valid for fully one-half of the TCK cycle.

The functional block diagram illustrates the IEEE Standard 1149.1-1990 4-wire test bus and boundary-scan architecture and the relationship between the test bus, the TAP controller, and the test registers. As illustrated, the device contains an 8-bit instruction register and four test data registers: an 88-bit boundary-scan register, a 23-bit boundary-control register, a 1-bit bypass register, and a 32-bit device identification register.

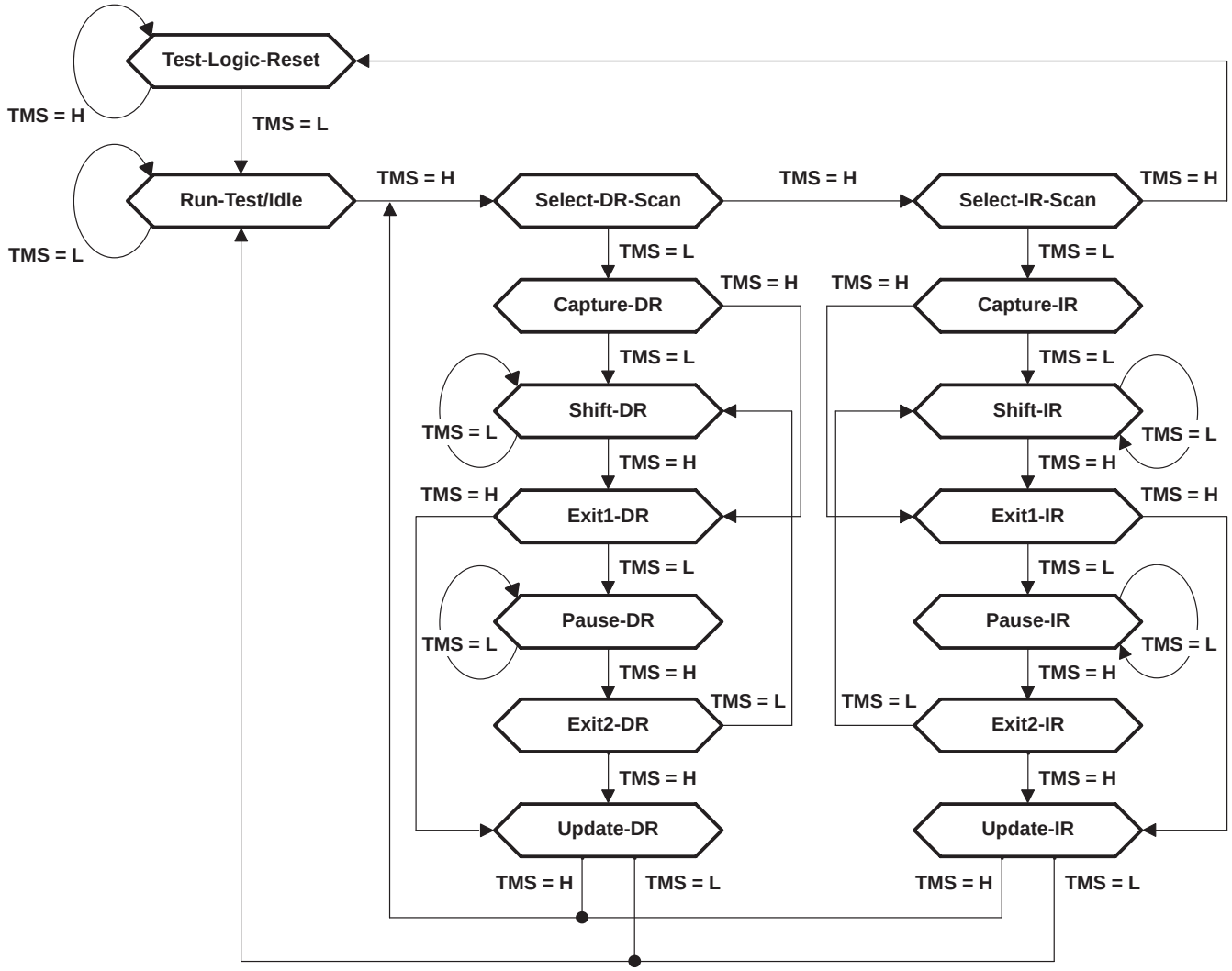


Figure 1. TAP Controller State Diagram

state diagram description

The test access port (TAP) controller is a synchronous finite state machine that provides test control signals throughout the device. The state diagram is illustrated in Figure 1 and is in accordance with IEEE Standard 1149.1-1990. The TAP controller proceeds through its states based on the level of TMS at the rising edge of TCK.

As illustrated, the TAP controller consists of sixteen states. There are six stable states (indicated by a looping arrow in the state diagram) and ten unstable states. A stable state is defined as a state the TAP controller can retain for consecutive TCK cycles. Any state that does not meet this criterion is an unstable state.

There are two main paths though the state diagram: one to access and control the selected data register and one to access and control the instruction register. Only one register can be accessed at a time.

Test-Logic-Reset

The device powers up in the Test-Logic-Reset state. In the stable Test-Logic-Reset state, the test logic is reset and is disabled so that the normal logic function of the device is performed. The instruction register is reset to an opcode that selects the optional IDCODE instruction, if supported, or the BYPASS instruction. Certain data registers may also be reset to their power-up values.

The state machine is constructed such that the TAP controller returns to the Test-Logic-Reset state in no more than five TCK cycles if TMS is left high. The TMS pin has an internal pullup resistor that forces it high if left unconnected or if a board defect causes it to be open circuited.

For the ′ABT18504, the instruction register is reset to the binary value 10000001, which selects the IDCODE instruction. Each bit in the boundary-scan register is reset to logic 0 except bits 87–86, which are reset to logic 1. The boundary-control register is reset to the binary value 00000000000000000000010, which selects the PSA test operation with no input masking.

Run-Test/Idle

The TAP controller must pass through the Run-Test/Idle state (from Test-Logic-Reset) before executing any test operations. The Run-Test/Idle state can also be entered following data register or instruction register scans. Run-Test/Idle is provided as a stable state in which the test logic may be actively running a test or can be idle.

The test operations selected by the boundary-control register are performed while the TAP controller is in the Run-Test/Idle state.

Select-DR-Scan, Select-IR-Scan

No specific function is performed in the Select-DR-Scan and Select-IR-Scan states, and the TAP controller exits either of these states on the next TCK cycle. These states are provided to allow the selection of either data register scan or instruction register scan.

Capture-DR

When a data register scan is selected, the TAP controller must pass through the Capture-DR state. In the Capture-DR state, the selected data register can capture a data value as specified by the current instruction. Such capture operations occur on the rising edge of TCK upon which the TAP controller exits the Capture-DR state.

state diagram description (continued)

Shift-DR

Upon entry to the Shift-DR state, the data register is placed in the scan path between TDI and TDO and, on the first falling edge of TCK, TDO goes from the high-impedance state to an active state. TDO enables to the logic level present in the least significant bit of the selected data register.

While in the stable Shift-DR state, data is serially shifted through the selected data register on each TCK cycle. The first shift occurs on the first rising edge of TCK after entry to the Shift-DR state (i.e., no shifting occurs during the TCK cycle in which the TAP controller changes from Capture-DR to Shift-DR or from Exit2-DR to Shift-DR). The last shift occurs on the rising edge of TCK upon which the TAP controller exits the Shift-DR state.

Exit1-DR, Exit2-DR

The Exit1-DR and Exit2-DR states are temporary states used to end a data register scan. It is possible to return to the Shift-DR state from either Exit1-DR or Exit2-DR without recapturing the data register.

On the first falling edge of TCK after entry to Exit1-DR, TDO goes from the active state to the high-impedance state.

Pause-DR

No specific function is performed in the stable Pause-DR state, in which the TAP controller can remain indefinitely. The Pause-DR state provides the capability of suspending and resuming data register scan operations without loss of data.

Update-DR

If the current instruction calls for the selected data register to be updated with current data, such update occurs on the falling edge of TCK following entry to the Update-DR state.

Capture-IR

When an instruction register scan is selected, the TAP controller must pass through the Capture-IR state. In the Capture-IR state, the instruction register captures its current status value. This capture operation occurs on the rising edge of TCK upon which the TAP controller exits the Capture-IR state.

For the ′ABT18504, the status value loaded in the Capture-IR state is the fixed binary value 10000001.

Shift-IR

Upon entry to the Shift-IR state, the instruction register is placed in the scan path between TDI and TDO and, on the first falling edge of TCK, TDO goes from the high-impedance state to an active state. TDO enables to the logic level present in the least significant bit of the instruction register.

While in the stable Shift-IR state, instruction data is serially shifted through the instruction register on each TCK cycle. The first shift occurs on the first rising edge of TCK after entry to the Shift-IR state (i.e., no shifting occurs during the TCK cycle in which the TAP controller changes from Capture-IR to Shift-IR or from Exit2-IR to Shift-IR). The last shift occurs on the rising edge of TCK upon which the TAP controller exits the Shift-IR state.

Exit1-IR, Exit2-IR

The Exit1-IR and Exit2-IR states are temporary states used to end an instruction register scan. It is possible to return to the Shift-IR state from either Exit1-IR or Exit2-IR without recapturing the instruction register.

On the first falling edge of TCK after entry to Exit1-IR, TDO goes from the active state to the high-impedance state.

state diagram description (continued)

Pause-IR

No specific function is performed in the stable Pause-IR state, in which the TAP controller can remain indefinitely. The Pause-IR state provides the capability of suspending and resuming instruction register scan operations without loss of data.

Update-IR

The current instruction is updated and takes effect on the falling edge of TCK following entry to the Update-IR state.

register overview

With the exception of the bypass and device identification registers, any test register can be thought of as a serial shift register with a shadow latch on each bit. The bypass and device identification registers differ in that they contain only a shift register. During the appropriate capture state (Capture-IR for instruction register, Capture-DR for data registers), the shift register may be parallel loaded from a source specified by the current instruction. During the appropriate shift state (Shift-IR or Shift-DR), the contents of the shift register are shifted out from TDO while new contents are shifted in at TDI. During the appropriate update state (Update-IR or Update-DR), the shadow latches are updated from the shift register.

instruction register description

The instruction register (IR) is eight bits long and is used to tell the device what instruction is to be executed. Information contained in the instruction includes the mode of operation (either normal mode, in which the device performs its normal logic function, or test mode, in which the normal logic function is inhibited or altered), the test operation to be performed, which of the four data registers is to be selected for inclusion in the scan path during data register scans, and the source of data to be captured into the selected data register during Capture-DR.

Table 4 lists the instructions supported by the ′ABT18504. The even-parity feature specified for SCOPE™ devices is supported in this device. Bit 7 of the instruction opcode is the parity bit. Any instructions that are defined for SCOPE™ devices but are not supported by this device default to BYPASS.

During Capture-IR, the IR captures the binary value 10000001. As an instruction is shifted in, this value will be shifted out via TDO and can be inspected as verification that the IR is in the scan path. During Update-IR, the value that has been shifted into the IR is loaded into shadow latches. At this time, the current instruction is updated and any specified mode change takes effect. At power up or in the Test-Logic-Reset state, the IR is reset to the binary value 10000001, which selects the IDCODE instruction.

The instruction register order of scan is illustrated in Figure 2.

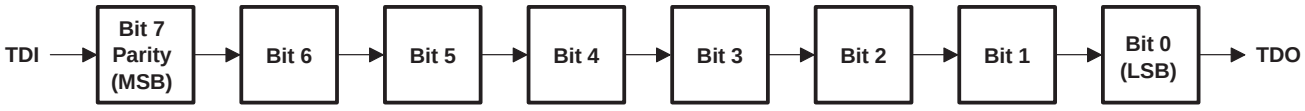


Figure 2. Instruction Register Order of Scan

data register description

boundary-scan register

The boundary-scan register (BSR) is 88 bits long. It contains one boundary-scan cell (BSC) for each normal-function input pin and two BSCs for each normal-function I/O pin (one for input data and one for output data). The BSR is used 1) to store test data that is to be applied internally to the inputs of the normal on-chip logic and/or externally to the device output pins, and/or 2) to capture data that appears internally at the outputs of the normal on-chip logic and/or externally at the device input pins.

The source of data to be captured into the BSR during Capture-DR is determined by the current instruction. The contents of the BSR can change during Run-Test/Idle as determined by the current instruction. At power up or in Test-Logic-Reset, the value of each BSC is reset to logic 0 except BSCs 87–86, which are reset to logic 1.

The boundary-scan register order of scan is from TDI through bits 87–0 to TDO. Table 1 shows the boundary-scan register bits and their associated device pin signals.

Table 1. Boundary-Scan Register Configuration

BSR BIT NUMBER	DEVICE SIGNAL	BSR BIT NUMBER	DEVICE SIGNAL	BSR BIT NUMBER	DEVICE SIGNAL	BSR BIT NUMBER	DEVICE SIGNAL	BSR BIT NUMBER	DEVICE SIGNAL
87	$\overline{\text{OEAB}}$	79	A20-I	59	A20-O	39	B20-I	19	B20-O
86	$\overline{\text{OEBA}}$	78	A19-I	58	A19-O	38	B19-I	18	B19-O
85	CLKAB	77	A18-I	57	A18-O	37	B18-I	17	B18-O
84	CLKBA	76	A17-I	56	A17-O	36	B17-I	16	B17-O
83	$\overline{\text{CLKENAB}}$	75	A16-I	55	A16-O	35	B16-I	15	B16-O
82	$\overline{\text{CLKENBA}}$	74	A15-I	54	A15-O	34	B15-I	14	B15-O
81	LEAB	73	A14-I	53	A14-O	33	B14-I	13	B14-O
80	LEBA	72	A13-I	52	A13-O	32	B13-I	12	B13-O
—	—	71	A12-I	51	A12-O	31	B12-I	11	B12-O
—	—	70	A11-I	50	A11-O	30	B11-I	10	B11-O
—	—	69	A10-I	49	A10-O	29	B10-I	9	B10-O
—	—	68	A9-I	48	A9-O	28	B9-I	8	B9-O
—	—	67	A8-I	47	A8-O	27	B8-I	7	B8-O
—	—	66	A7-I	46	A7-O	26	B7-I	6	B7-O
—	—	65	A6-I	45	A6-O	25	B6-I	5	B6-O
—	—	64	A5-I	44	A5-O	24	B5-I	4	B5-O
—	—	63	A4-I	43	A4-O	23	B4-I	3	B4-O
—	—	62	A3-I	42	A3-O	22	B3-I	2	B3-O
—	—	61	A2-I	41	A2-O	21	B2-I	1	B2-O
—	—	60	A1-I	40	A1-O	20	B1-I	0	B1-O

boundary-control register

The boundary-control register (BCR) is 23 bits long. The BCR is used in the context of the RUNT instruction to implement additional test operations not included in the basic SCOPE™ instruction set. Such operations include pseudo-random pattern generation (PRPG), parallel signature analysis (PSA) with input masking, and binary count up (COUNT). Table 5 shows the test operations that are decoded by the BCR.

During Capture-DR, the contents of the BCR are not changed. At power up or in Test-Logic-Reset, the BCR is reset to the binary value 00000000000000000000010, which selects the PSA test operation with no input masking.

data register description (continued)

The boundary-control register order of scan is from TDI through bits 22–0 to TDO. Table 2 shows the boundary-control register bits and their associated test control signals.

Table 2. Boundary Control Register Configuration

BCR BIT NUMBER	TEST CONTROL SIGNAL	BCR BIT NUMBER	TEST CONTROL SIGNAL	BCR BIT NUMBER	TEST CONTROL SIGNAL
22	MASK20	12	MASK10	2	OPCODE2
21	MASK19	11	MASK9	1	OPCODE1
20	MASK18	10	MASK8	0	OPCODE0
19	MASK17	9	MASK7	—	—
18	MASK16	8	MASK6	—	—
17	MASK15	7	MASK5	—	—
16	MASK14	6	MASK4	—	—
15	MASK13	5	MASK3	—	—
14	MASK12	4	MASK2	—	—
13	MASK11	3	MASK1	—	—

bypass register

The bypass register is a one-bit scan path that can be selected to shorten the length of the system scan path, thereby reducing the number of bits per test pattern that must be applied to complete a test operation.

During Capture-DR, the bypass register captures a logic 0.

The bypass register order of scan is illustrated in Figure 3.

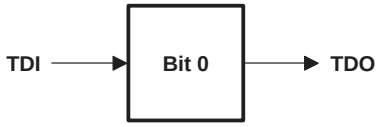


Figure 3. Bypass Register Order of Scan

device identification register

The device identification register (IDR) is 32 bits long. It can be selected and read to identify the manufacturer, part number, and version of this device.

During Capture-DR, the binary value 00000000000000000111000000101111 (0000702F, hex) is captured in the device identification register to identify this device as Texas Instruments SN54/74ABT18504, version 0.

The device identification register order of scan is from TDO through bits 31–0 to TDO. Table 3 shows the device identification register bits and their significance.

Table 3. Device Identification Register Configuration

IDR BIT NUMBER	IDENTIFICATION SIGNIFICANCE	IDR BIT NUMBER	IDENTIFICATION SIGNIFICANCE	IDR BIT NUMBER	IDENTIFICATION SIGNIFICANCE
31	VERSION3	27	PARTNUMBER15	11	MANUFACTURER10†
30	VERSION2	26	PARTNUMBER14	10	MANUFACTURER09†
29	VERSION1	25	PARTNUMBER13	9	MANUFACTURER08†
28	VERSION0	24	PARTNUMBER12	8	MANUFACTURER07†
—	—	23	PARTNUMBER11	7	MANUFACTURER06†
—	—	22	PARTNUMBER10	6	MANUFACTURER05†
—	—	21	PARTNUMBER09	5	MANUFACTURER04†
—	—	20	PARTNUMBER08	4	MANUFACTURER03†
—	—	19	PARTNUMBER07	3	MANUFACTURER02†
—	—	18	PARTNUMBER06	2	MANUFACTURER01†
—	—	17	PARTNUMBER05	1	MANUFACTURER00†
—	—	16	PARTNUMBER04	0	LOGIC1†
—	—	15	PARTNUMBER03	—	—
—	—	14	PARTNUMBER02	—	—
—	—	13	PARTNUMBER01	—	—
—	—	12	PARTNUMBER00	—	—

† Note that for TI products, bits 11 – 0 of the device identification register always contains the binary value 000000101111 (02F, hex).

Table 4. Instruction Register Opcodes

BINARY CODE† BIT 7 → BIT 0 MSB → LSB	SCOPE OPCODE	DESCRIPTION	SELECTED DATA REGISTER	MODE
00000000	EXTEST	Boundary scan	Boundary scan	Test
10000001	IDCODE	Identification read	Device identification	Normal
10000010	SAMPLE/PRELOAD	Sample boundary	Boundary scan	Normal
00000011	INTEST	Boundary scan	Boundary scan	Test
10000100	BYPASS‡	Bypass scan	Bypass	Normal
00000101	BYPASS‡	Bypass scan	Bypass	Normal
00000110	HIGHZ	Control boundary to high impedance	Bypass	Modified test
10000111	CLAMP	Control boundary to 1/0	Bypass	Test
10001000	BYPASS‡	Bypass scan	Bypass	Normal
00001001	RUNT	Boundary run test	Bypass	Test
00001010	READBN	Boundary read	Boundary scan	Normal
10001011	READBT	Boundary read	Boundary scan	Test
00001100	CELLTST	Boundary self test	Boundary scan	Normal
10001101	TOPHIP	Boundary toggle outputs	Bypass	Test
10001110	SCANCN	Boundary-control register scan	Boundary control	Normal
00001111	SCANCT	Boundary-control register scan	Boundary control	Test
All others	BYPASS	Bypass scan	Bypass	Normal

† Bit 7 is used to maintain even parity in the 8-bit instruction.
‡ The BYPASS instruction is executed in lieu of a SCOPE™ instruction that is not supported in the ′ABT18504.

instruction register opcode description

The instruction register opcodes are shown in Table 4. The following descriptions detail the operation of each instruction.

boundary scan

This instruction conforms to the IEEE Standard 1149.1-1990 EXTEST and INTEST instructions. The boundary-scan register is selected in the scan path. Data appearing at the device input pins is captured in the input BSCs, while data appearing at the outputs of the normal on-chip logic is captured in the output BSCs. Data scanned into the input BSCs is applied to the inputs of the normal on-chip logic, while data scanned into the output BSCs is applied to the device output pins. The device operates in the test mode.

bypass scan

This instruction conforms to the IEEE Standard 1149.1-1990 BYPASS instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in the normal mode.

sample boundary

This instruction conforms to the IEEE Standard 1149.1-1990 SAMPLE/PRELOAD instruction. The boundary-scan register is selected in the scan path. Data appearing at the device input pins is captured in the input BSCs, while data appearing at the outputs of the normal on-chip logic is captured in the output BSCs. The device operates in the normal mode.

control boundary to high impedance

This instruction conforms to the IEEE P1149.1A HIGHZ instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in a modified test mode in which all device I/O pins are placed in the high-impedance state, the device input pins remain operational, and the normal on-chip logic function is performed.

control boundary to 1/0

This instruction conforms to the IEEE P1149.1A CLAMP instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. Data in the input BSCs is applied to the inputs of the normal on-chip logic, while data in the output BSCs is applied to the device output pins. The device operates in the test mode.

boundary run test

The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in the test mode. The test operation specified in the boundary-control register is executed during Run-Test/Idle. The five test operations decoded by the boundary-control register are: sample inputs/toggle outputs (TOPSIP), pseudo-random pattern generation (PRPG), parallel signature analysis (PSA), simultaneous PSA and PRPG (PSA/PRPG), and simultaneous PSA and binary count up (PSA/COUNT).

boundary read

The boundary-scan register is selected in the scan path. The value in the boundary-scan register remains unchanged during Capture-DR. This instruction is useful for inspecting data after a PSA operation.

boundary self test

The boundary-scan register is selected in the scan path. All BSCs capture the inverse of their current values during Capture-DR. In this way, the contents of the shadow latches can be read out to verify the integrity of both shift register and shadow latch elements of the boundary-scan register. The device operates in the normal mode.

instruction register opcode description (continued)

boundary toggle outputs

The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. Data in the shift-register elements of the selected output BSCs is toggled on each rising edge of TCK in Run-Test/Idle, updated in the shadow latches, and applied to the associated device output pins on each falling edge of TCK in Run-Test/Idle. Data in the selected input BSCs remains constant and is applied to the inputs of the normal on-chip logic. Data appearing at the device input pins is not captured in the input BSCs. The device operates in the test mode.

boundary-control register scan

The boundary-control register is selected in the scan path. The value in the boundary-control register remains unchanged during Capture-DR. This operation must be performed prior to a boundary run test operation in order to specify which test operation is to be executed.

Table 5. Boundary-Control Register Opcodes

BINARY CODE BIT 2 → BIT 0 MSB → LSB	DESCRIPTION
X00	Sample inputs/toggle outputs (TOPSIP)
X01	Pseudo-random pattern generation/40-bit mode (PRPG)
X10	Parallel signature analysis/40-bit mode (PSA)
011	Simultaneous PSA and PRPG/20-bit mode (PSA/PRPG)
111	Simultaneous PSA and binary count up/20-bit mode (PSA/COUNT)

boundary-control register opcode description

The boundary-control register opcodes are decoded from BCR bits 2–0 as shown in Table 5. The selected test operation is performed while the RUNT instruction is executed in the Run-Test/Idle state. The following descriptions detail the operation of each BCR instruction and illustrate the associated PSA and PRPG algorithms.

In general, while the control input BSCs (bits 87–80) are not included in the toggle, PSA, PRPG, or COUNT algorithms, the output-enable BSCs (bits 87–86 of the BSR) control the drive state (active or high impedance) of the selected device output pins. These BCR instructions are only valid when the device is operating in one direction of data flow (that is, $\overline{OEAB} \neq \overline{OEBA}$). Otherwise, the bypass instruction is operated.

PSA input masking

Bits 22–3 of the boundary-control register are used to specify device input pins to be masked from PSA operations. Bit 22 selects masking for device input pin A20 during A-to-B data flow or for device input pin B20 during B-to-A data flow. Bit 3 selects masking for device input pins A1 or B1 during A-to-B or B-to-A data flow, respectively. Bits intermediate to 22 and 3 mask corresponding device input pins in order from most significant to least significant, as indicated in Table 2. When the mask bit which corresponds to a particular device input has a logic 1 value, the device input pin is masked from any PSA operation, meaning that the state of the device input pin is ignored and has no effect on the generated signature. Otherwise, when a mask bit has a logic 0 value, the corresponding device input is not masked from the PSA operation.

boundary-control register opcode description (continued)

sample inputs/toggle outputs (TOPSIP)

Data appearing at the selected device input pins is captured in the shift-register elements of the selected BSCs on each rising edge of TCK. This data is then updated in the shadow latches of the selected input BSCs and applied to the inputs of the normal on-chip logic. Data in the shift-register elements of the selected output BSCs is toggled on each rising edge of TCK and is then updated in the shadow latches and applied to the associated device output pins on each falling edge of TCK.

pseudo-random pattern generation (PRPG)

A pseudo-random pattern is generated in the shift-register elements of the selected BSCs on each rising edge of TCK, updated in the shadow latches, and applied to the associated device output pins on each falling edge of TCK. This data is also updated in the shadow latches of the selected input BSCs and applied to the inputs of the normal on-chip logic. Figures 4 and 5 illustrate the 40-bit linear-feedback shift-register algorithms through which the patterns are generated. An initial seed value should be scanned into the boundary-scan register prior to performing this operation. A seed value of all zeroes will not produce additional patterns.

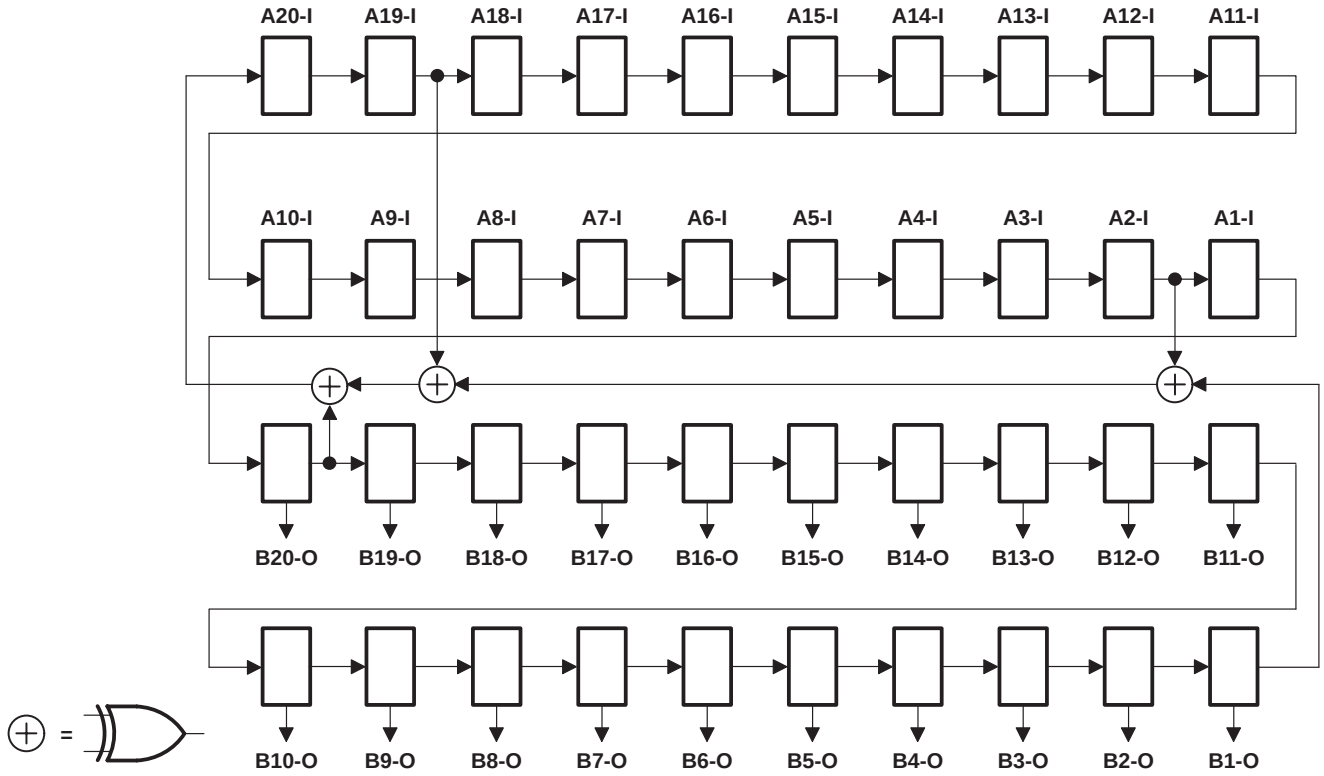


Figure 4. 40-Bit PRPG Configuration ($\overline{OEAB}$ = 0, $\overline{OEBA}$ = 1)

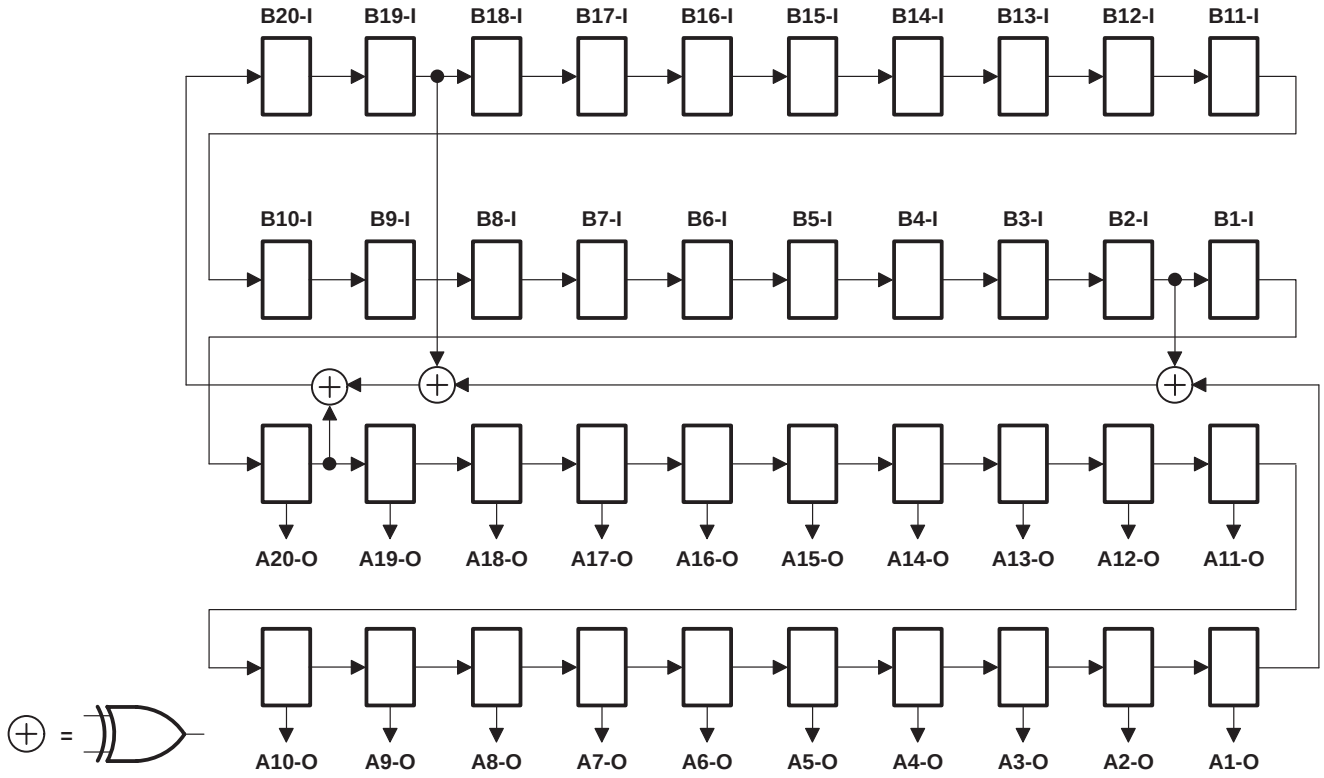


Figure 5. 40-Bit PRPG Configuration ($\overline{\text{OEAB}}$ = 1, $\overline{\text{OEBA}}$ = 0)

boundary-control register opcode description (continued)

parallel signature analysis (PSA)

Data appearing at the selected device input pins is compressed into a 40-bit parallel signature in the shift-register elements of the selected BSCs on each rising edge of TCK. This data is updated in the shadow latches of the selected input BSCs and applied to the inputs of the normal on-chip logic. Data in the shadow latches of the selected output BSCs remains constant and is applied to the device outputs. Figures 6 and 7 illustrate the 40-bit linear-feedback shift-register algorithms through which the signature is generated. An initial seed value should be scanned into the boundary-scan register prior to performing this operation.

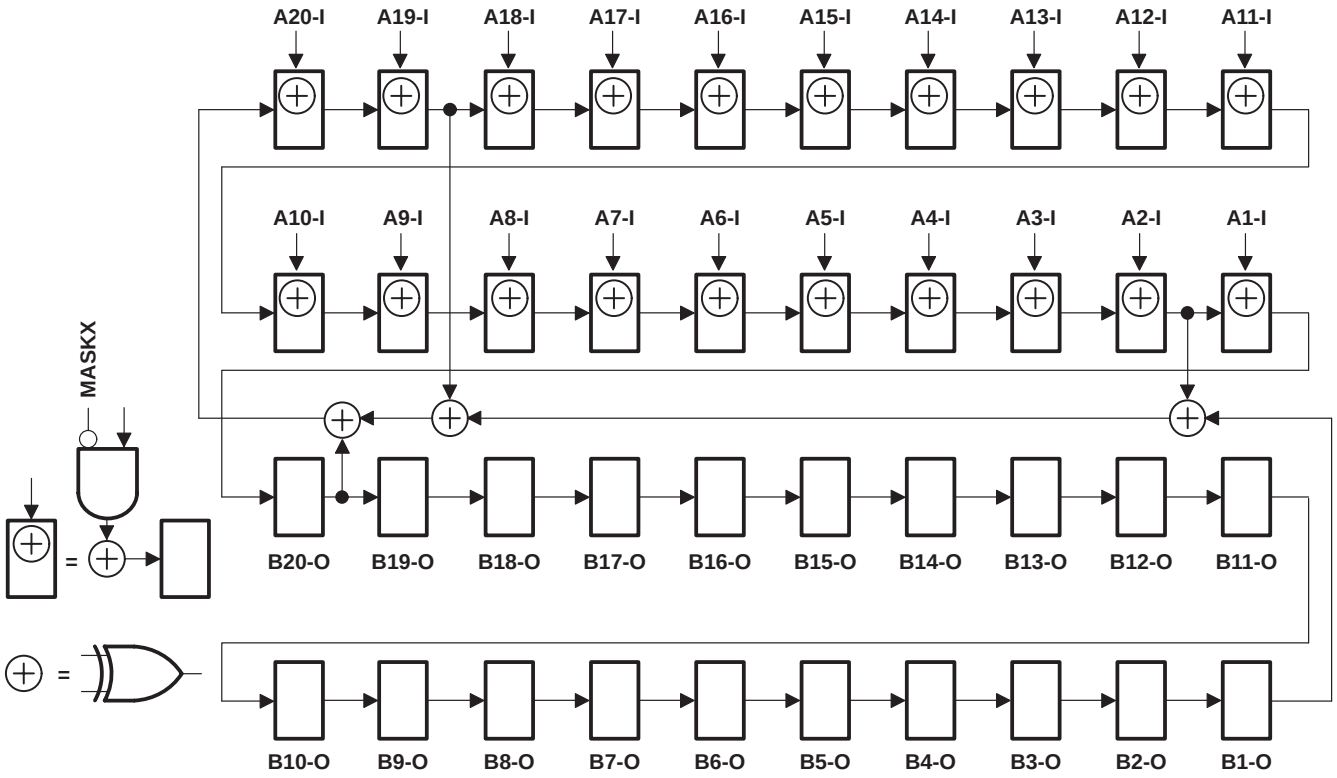


Figure 6. 40-Bit PSA Configuration ($\overline{OEAB}$ = 0, $\overline{OEBA}$ = 1)

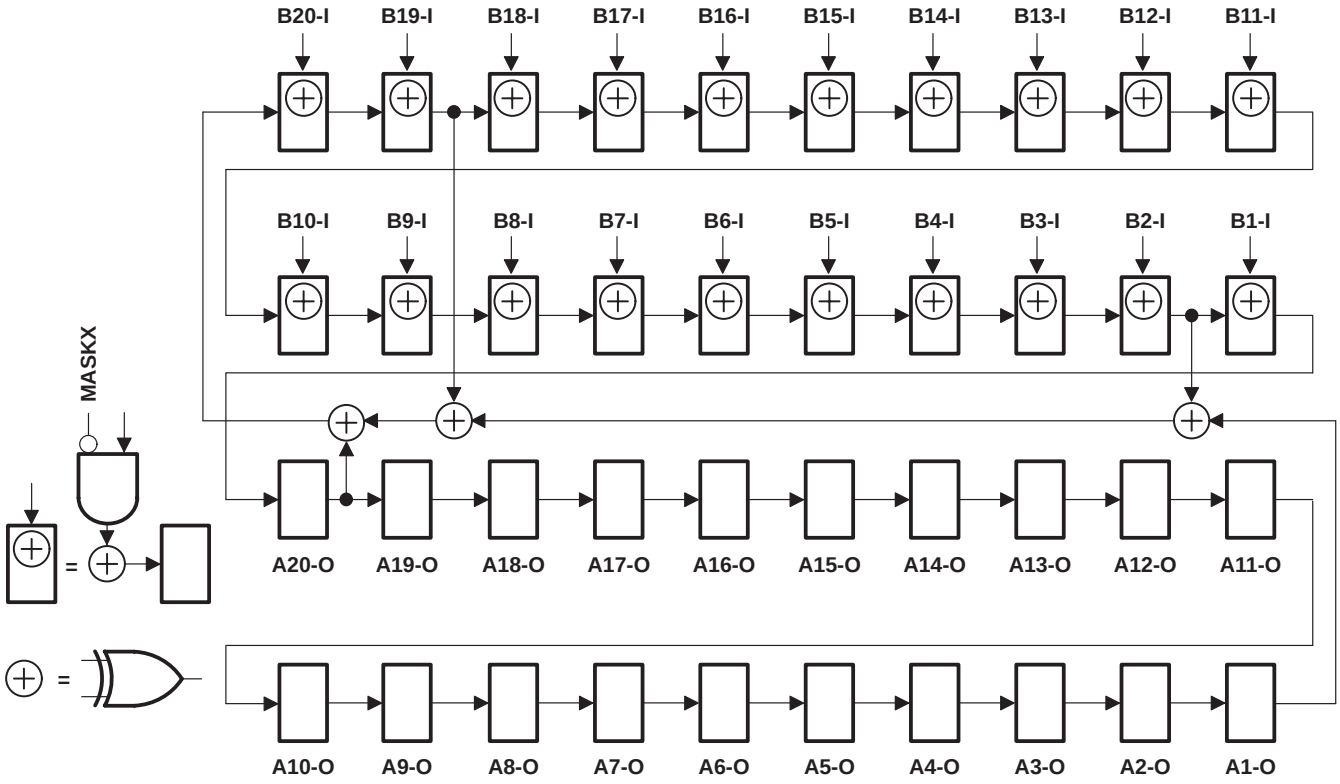


Figure 7. 40-Bit PSA Configuration ($\overline{OEAB}$ = 1, $\overline{OEBA}$ = 0)

boundary-control register opcode description (continued)

simultaneous PSA and PRPG (PSA/PRPG)

Data appearing at the selected device input pins is compressed into a 20-bit parallel signature in the shift-register elements of the selected input BSCs on each rising edge of TCK. This data is updated in the shadow latches of the selected input BSCs andapplied to the inputs of the normal on-chip logic. At the same time, a 20-bit pseudo-random pattern is generated in the shift-register elements of the selected output BSCs on each rising edge of TCK, updated in the shadow latches, and applied to the associated device output pins on each falling edge of TCK. Figures 8 and 9 illustrate the 20-bit linear-feedback shift-register algorithms through which the signature and patterns are generated. An initial seed value should be scanned into the boundary-scan register prior to performing this operation. A seed value of all zeroes will not produce additional patterns.

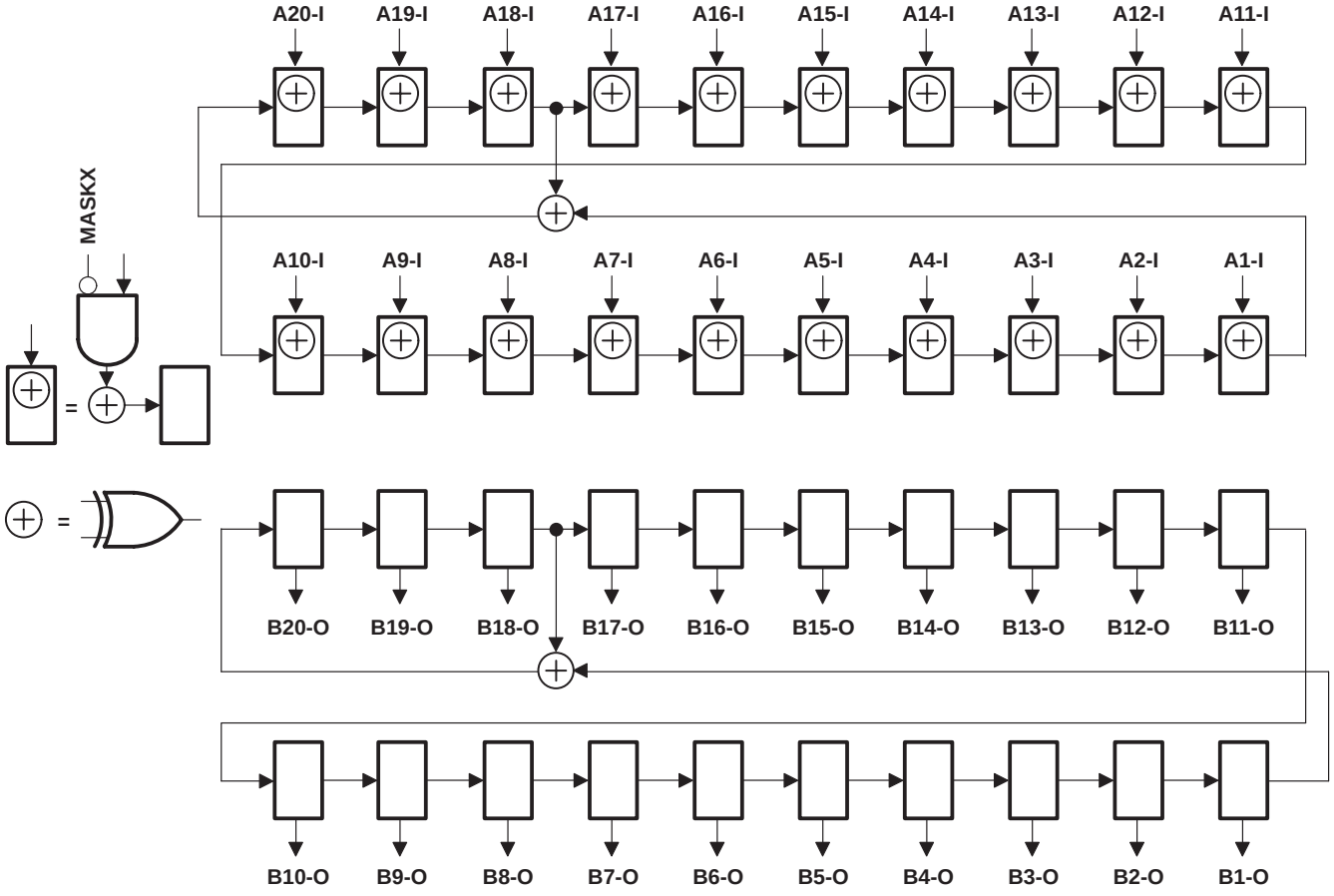


Figure 8. 20-Bit PSA/PRPG Configuration ($\overline{OEAB}$ = 0, $\overline{OEBA}$ = 1)

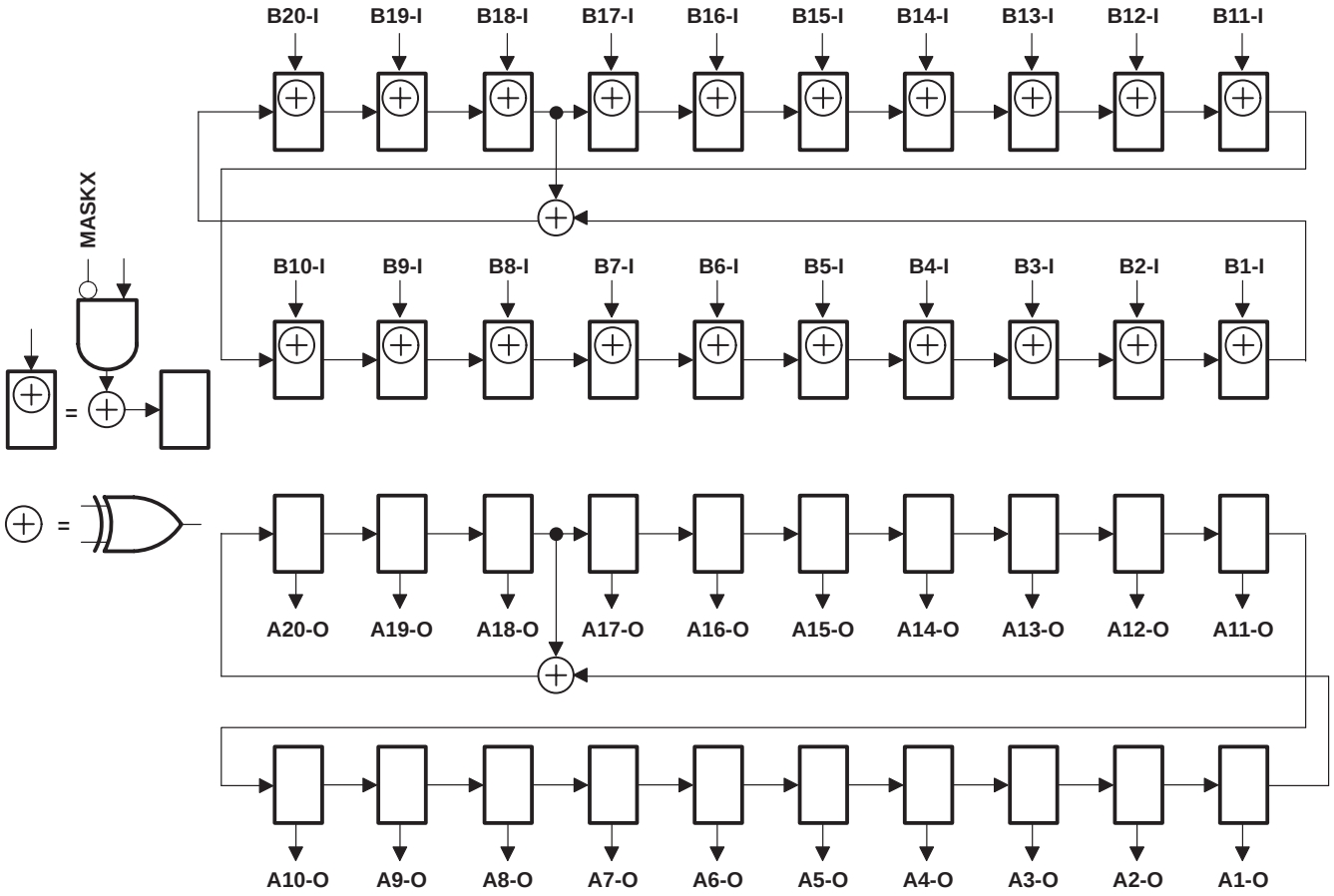


Figure 9. 20-Bit PSA/PRPG Configuration ($\overline{OEAB}$ = 1, $\overline{OEBA}$ = 0)

boundary-control register opcode description (continued)

simultaneous PSA and binary count up (PSA/COUNT)

Data appearing at the selected device input pins is compressed into a 20-bit parallel signature in the shift-register elements of the selected input BSCs on each rising edge of TCK. This data is updated in the shadow latches of the selected input BSCs and applied to the inputs of the normal on-chip logic. At the same time, a 20-bit binary count-up pattern is generated in the shift-register elements of the selected output BSCs on each rising edge of TCK, updated in the shadow latches, and applied to the associated device output pins on each falling edge of TCK. Figures 10 and 11 illustrate the 20-bit linear-feedback shift-register algorithms through which the signature is generated. An initial seed value should be scanned into the boundary-scan register prior to performing this operation.

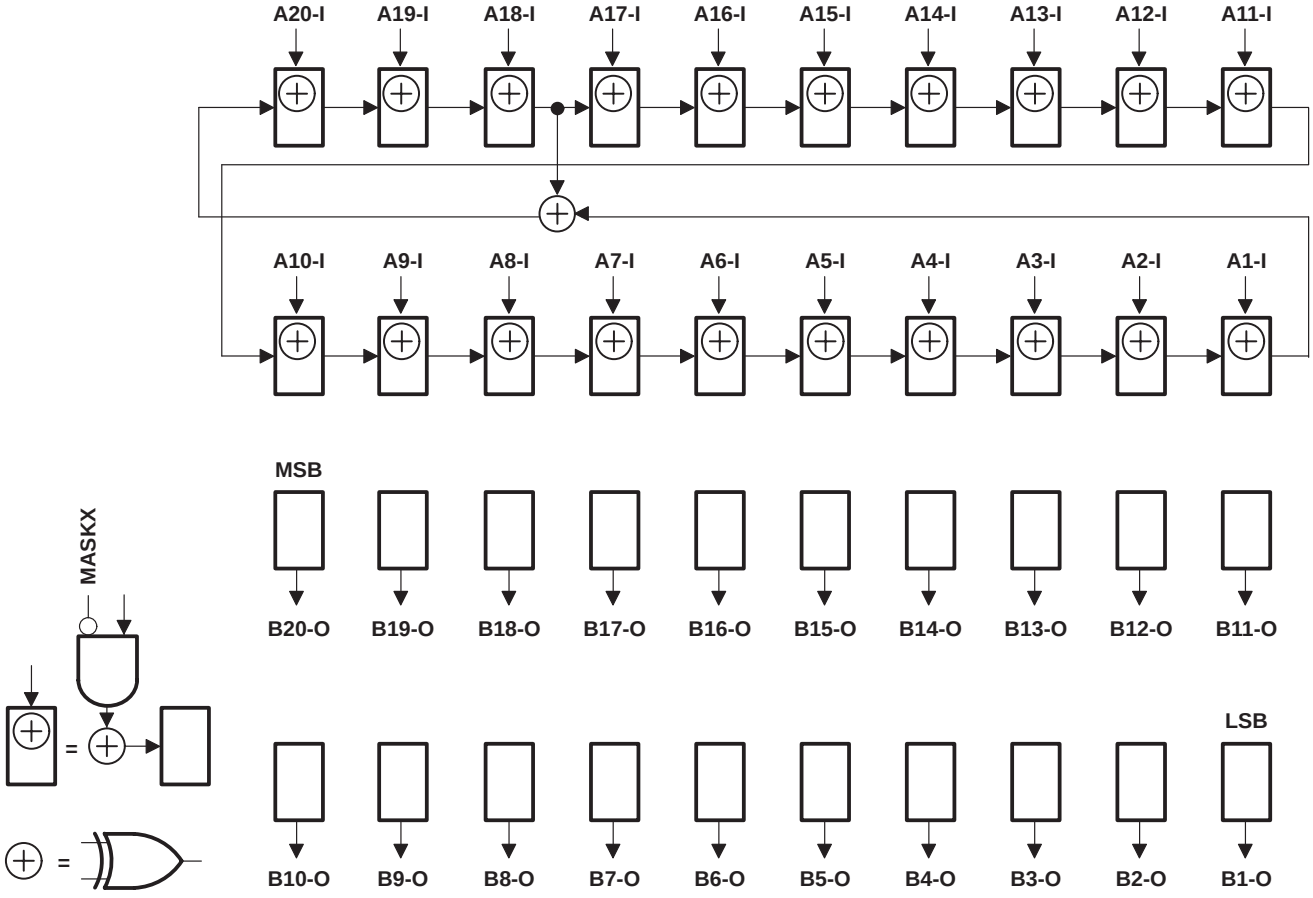


Figure 10. 20-Bit PSA/COUNT Configuration ($\overline{OEAB}$ = 0, $\overline{OEBA}$ = 1)

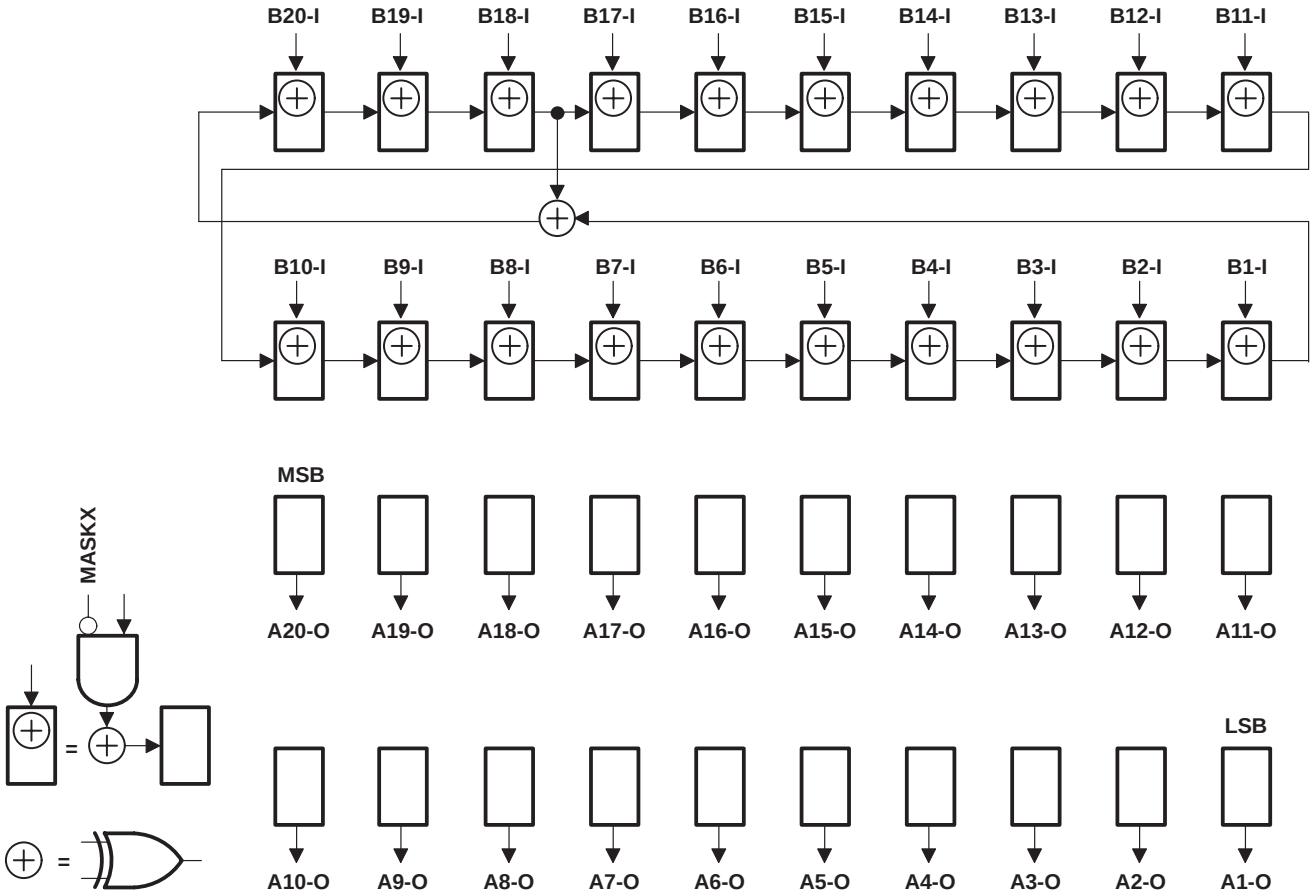


Figure 11. 20-Bit PSA/COUNT Configuration ($\overline{OEAB}$ = 1, $\overline{OEBA}$ = 0)

timing description

All test operations of the ′ABT18504 are synchronous to the test clock (TCK). Data on the TDI, TMS, and normal-function inputs is captured on the rising edge of TCK. Data appears on the TDO and normal-function output pins on the falling edge of TCK. The TAP controller is advanced through its states (as illustrated in Figure 1) by changing the value of TMS on the falling edge of TCK and then applying a rising edge to TCK.

A simple timing example is illustrated in Figure 12. In this example, the TAP controller begins in the Test-Logic-Reset state and is advanced through its states as necessary to perform one instruction register scan and one data register scan. While in the Shift-IR and Shift-DR states, TDI is used to input serial data, and TDO is used to output serial data. The TAP controller is then returned to the Test-Logic-Reset state. Table 6 explains the operation of the test circuitry during each TCK cycle.

Table 6. Explanation of Timing Example

TCK CYCLE(S)	TAP STATE AFTER TCK	DESCRIPTION
1	Test-Logic-Reset	TMS is changed to a logic 0 value on the falling edge of TCK to begin advancing the TAP controller toward the desired state.
2	Run-Test/Idle	
3	Select-DR-Scan	
4	Select-IR-Scan	
5	Capture-IR	The IR captures the 8-bit binary value 10000001 on the rising edge of TCK as the TAP controller exits the Capture-IR state.
6	Shift-IR	TDO becomes active and TDI is made valid on the falling edge of TCK. The first bit is shifted into the TAP on the rising edge of TCK as the TAP controller advances to the next state.
7–13	Shift-IR	One bit is shifted into the IR on each TCK rising edge. With TDI held at a logic 1 value, the 8-bit binary value 11111111 is serially scanned into the IR. At the same time, the 8-bit binary value 10000001 is serially scanned out of the IR via TDO. In TCK cycle 13, TMS is changed to a logic 1 value to end the instruction register scan on the next TCK cycle. The last bit of the instruction is shifted as the TAP controller advances from Shift-IR to Exit1-IR.
14	Exit1-IR	TDO becomes inactive (goes to the high-impedance state) on the falling edge of TCK.
15	Update-IR	The IR is updated with the new instruction (BYPASS) on the falling edge of TCK.
16	Select-DR-Scan	
17	Capture-DR	The bypass register captures a logic 0 value on the rising edge of TCK as the TAP controller exits the Capture-DR state.
18	Shift-DR	TDO becomes active and TDI is made valid on the falling edge of TCK. The first bit is shifted into the TAP on the rising edge of TCK as the TAP controller advances to the next state.
19–20	Shift-DR	The binary value 101 is shifted in via TDI, while the binary value 010 is shifted out via TDO.
21	Exit1-DR	TDO becomes inactive (goes to the high-impedance state) on the falling edge of TCK.
22	Update-DR	In general, the selected data register is updated with the new data on the falling edge of TCK.
23	Select-DR-Scan	
24	Select-IR-Scan	
25	Test-Logic-Reset	Test operation completed

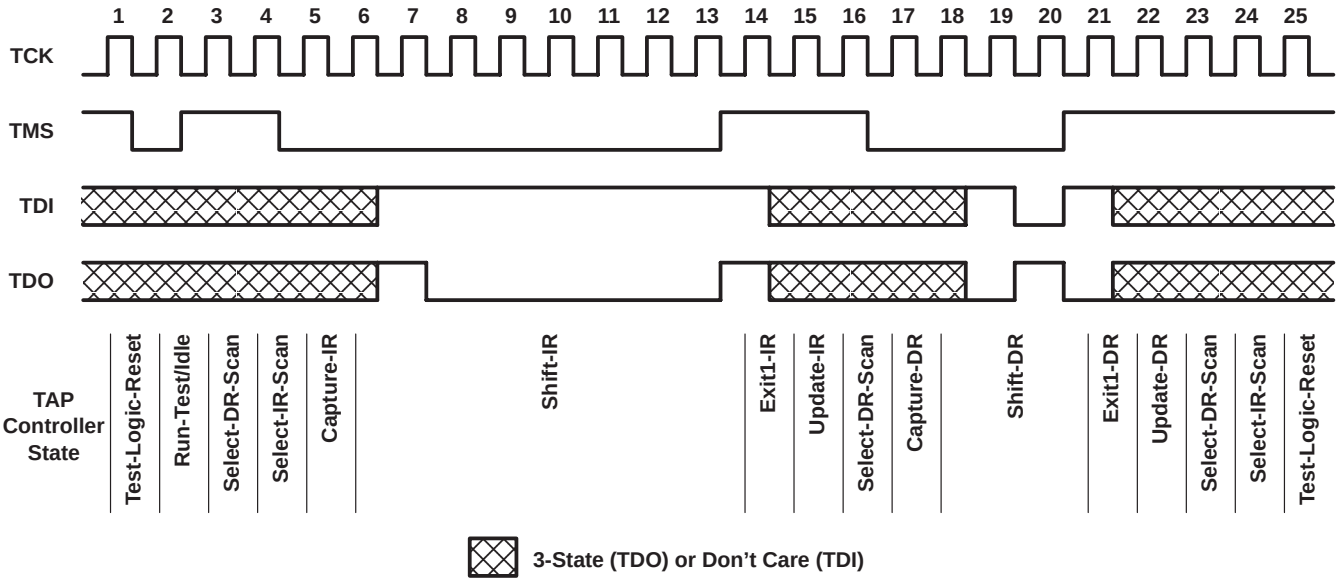


Figure 12. Timing Example

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (except I/O ports) (see Note 1)	–0.5 V to 7 V
Input voltage range, V_I (I/O ports) (see Note 1)	–0.5 V to 5.5 V
Voltage range applied to any output in the high state or power-off state, V_O	–0.5 V to 5.5 V
Current into any output in the low state, I_O: SN54ABT18504	96 mA
SN74ABT18504	128 mA
Input clamp current, I_{IK} ($V_I < 0$)	–18 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous current through V_{CC}	576 mA
Continuous current through GND	1152 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2)	885 mW
Storage temperature range	–65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings can be exceeded if the input and output clamp-current ratings are observed.
2. For the SN74ABT18504 (PM package), the power derating factor for ambient temperatures greater than 55°C is –10.5 mW/°C.

recommended operating conditions (see Note 3)

		SN54ABT18504		SN74ABT18504		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		–24		–32	mA
I_{OL}	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		10		10	ns/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

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NOTE 3: Unused or floating pins (input or I/O) must be held high or low.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			T_A = 25°C			SN54ABT18504		SN74ABT18504		UNIT
				MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = –18 mA				–1.2		–1.2		–1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = – 3 mA		2.5			2.5		2.5		V
	V_{CC} = 5 V,	I_{OH} = – 3 mA		3			3		3		
	V_{CC} = 4.5 V,	I_{OH} = – 24 mA		2			2				
	V_{CC} = 4.5 V,	I_{OH} = – 32 mA		2‡					2		
V_{OL}	V_{CC} = 4.5 V	I_{OL} = 48 mA				0.55		0.55			V
		I_{OL} = 64 mA				0.55‡				0.55	
I_I	V_{CC} = 5.5 V, V_I = V_{CC} or GND		CLK, $\overline{\text{CLKEN}}$, LE, $\overline{\text{OE}}$, TCK			±1		±1		±1	µA
			A or B ports			±100		±100		±100	
I_{IH}	V_{CC} = 5.5 V, V_I = V_{CC}		TDI, TMS			10		10		10	µA
I_{IL}	V_{CC} = 5.5 V, V_I = GND		TDI, TMS			–150		–150		–150	µA
I_{OZH}§	V_{CC} = 5.5 V,	V_O = 2.7 V				50		50		50	µA
I_{OZL}§	V_{CC} = 5.5 V,	V_O = 0.5 V				–50		–50		–50	µA
I_{OZPU}	V_{CC} = 0 to 2 V, V_O = 2.7 V or 0.5 V		$\overline{\text{OE}}$ = 0.8 V			±50		±50		±50	µA
I_{OZPD}	V_{CC} = 0 to 2 V, V_O = 2.7 V or 0.5 V		$\overline{\text{OE}}$ = 0.8 V			±50		±50		±50	µA
I_{off}	V_{CC} = 0,	V_I or V_O ≤ 4.5 V				±100		±450		±100	µA
I_{CEX}	V_{CC} = 5.5 V, V_O = 5.5 V		Outputs high			50		50		50	µA
I_O¶	V_{CC} = 5.5 V,	V_O = 2.5 V		–50	–110	–200	–50	–200	–50	–200	mA
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	A or B ports	Outputs high		3.5	5.5		5.5		5.5	mA
			Outputs low		36	40		40		40	
			Outputs disabled		2.9	5		5		5	
ΔI_{CC}#	V_{CC} = 5.5 V, Other inputs at V_{CC} or GND	One input at 3.4 V,				50		50		50	µA
C_i	V_I = 2.5 V or 0.5 V		Control inputs		3						pF
C_{io}	V_O = 2.5 V or 0.5 V		A or B ports		10						pF
C_o	V_O = 2.5 V or 0.5 V		TDO		8						pF

† All typical values are at V_{CC} = 5 V.
‡ On products compliant to MIL-STD-883, Class B, this parameter does not apply.
§ For I/O ports, the parameters I_{OZH} and I_{OZL} include the input leakage current.
¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
# This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

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timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Figure 13)

				SN54ABT18504		SN74ABT18504		UNIT
				MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency, CLKAB or CLKBA			0	100	0	100	MHz
t_w	Pulse duration	CLKAB or CLKBA high or low		4		4		ns
		LEAB or LEBA	CLK high or low	3.5		3.5		
t_{su}	Setup time	A before CLKAB↑ or B before CLKBA↑		4		4		ns
		A before LEAB↓ or B before LEBA↓	CLK high	3.5		3.5		
			CLK low	2		2		
		$\overline{CLKEN}$ before CLK↑		4		4		
t_h	Hold time	A after CLKAB↑ or B after CLKBA↑		0		0		ns
		A after LEAB↓ or B after LEBA↓	CLK high or low	2		2		
		$\overline{CLKEN}$ after CLK↑		0		0		

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Figure 13)

			SN54ABT18504		SN74ABT18504		UNIT
			MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency, TCK		0	50	0	50	MHz
t_w	Pulse duration	TCK high or low	8		8		ns
t_{su}	Setup time	A, B, CLK, LE, or $\overline{OE}$ before TCK↑	4.5		4.5		ns
		TDI before TCK↑	7.5		7.5		
		TMS before TCK↑	3		3		
t_h	Hold time	A, B, CLK, LE, or $\overline{OE}$ after TCK↑	0.5		0.5		ns
		TDI after TCK↑	0.5		0.5		
		TMS after TCK↑	0.5		0.5		
t_d	Delay time	Power up to TCK↑	50		50		ns
t_r	Rise time	V_{CC} power up	1		1		µs

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (normal mode) (see Figure 13)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT18504		SN74ABT18504		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	CLKAB or CLKBA		100	130		100		100		MHz
t_{PLH}	A or B	B or A	2	3.8	5.2	2	6.5	2	6	ns
t_{PHL}			2	3.8	6	2	7.2	2	6.5	
t_{PLH}	CLKAB or CLKBA	B or A	2.5	4.7	6.1	2.5	7.2	2.5	6.8	ns
t_{PHL}			2.5	4.7	6	2.5	7.1	2.5	6.5	
t_{PLH}	LEAB or LEBA	B or A	2.5	4.9	6.4	2.5	7.5	2.5	7.1	ns
t_{PHL}			2.5	4.9	6.5	2.5	7.8	2.5	7.2	
t_{PZH}	$\overline{OEAB}$ or $\overline{OEBA}$	B or A	2	4.9	6.3	2	7.5	2	7	ns
t_{PZL}			2.5	5.6	7.2	2.5	8.3	2.5	8	
t_{PHZ}	$\overline{OEAB}$ or $\overline{OEBA}$	B or A	3	6.1	7.8	3	9.6	3	8.8	ns
t_{PLZ}			2.5	4.8	6.5	2.5	7.4	2.5	7.3	

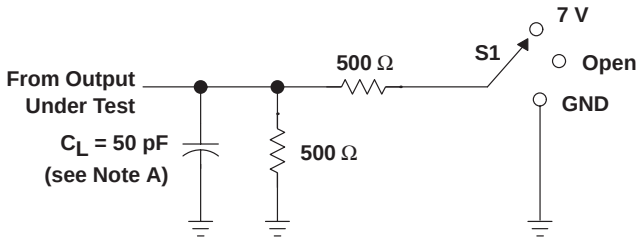
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (test mode) (see Figure 13)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			SN54ABT18504		SN74ABT18504		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}	TCK		50	90		50		50		MHz
t_{PLH}	TCK↓	A or B	2.5	9.1	11.5	2.5	14.5	2.5	13.5	ns
t_{PHL}			2.5	9.1	11	2.5	14	2.5	12.5	
t_{PLH}	TCK↓	TDO	2	3.8	5.8	2	7	2	6.5	ns
t_{PHL}			2	3.8	6	2	7	2	6.5	
t_{PZH}	TCK↓	A or B	4.5	9.5	12	4.5	14.5	4.5	13.8	ns
t_{PZL}			5	10.1	13	5	15	5	14.5	
t_{PZH}	TCK↓	TDO	2.5	4.6	6.2	2.5	7.5	2	7	ns
t_{PZL}			3	5.2	7	3	8	3	7.5	
t_{PHZ}	TCK↓	A or B	4	11.6	15	4	18	4	17	ns
t_{PLZ}			3	11.1	14.5	3	17.5	3	16	
t_{PHZ}	TCK↓	TDO	3	5.3	7.6	3	9.5	3	9	ns
t_{PLZ}			3	5.2	6.8	3	8	3	7.5	

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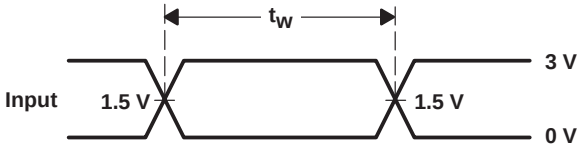
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PARAMETER MEASUREMENT INFORMATION

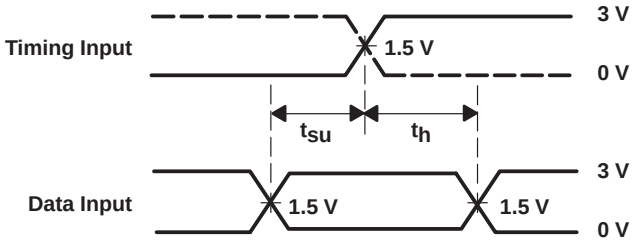


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open

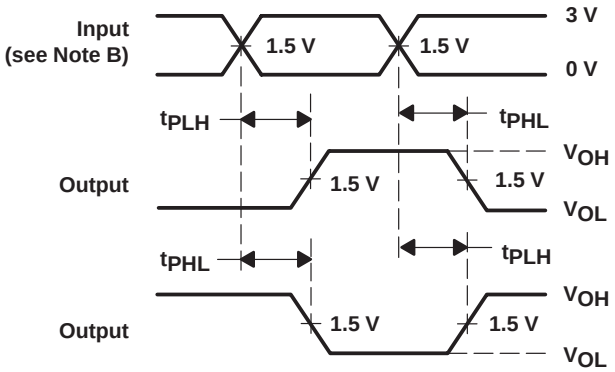
LOAD CIRCUIT FOR OUTPUTS



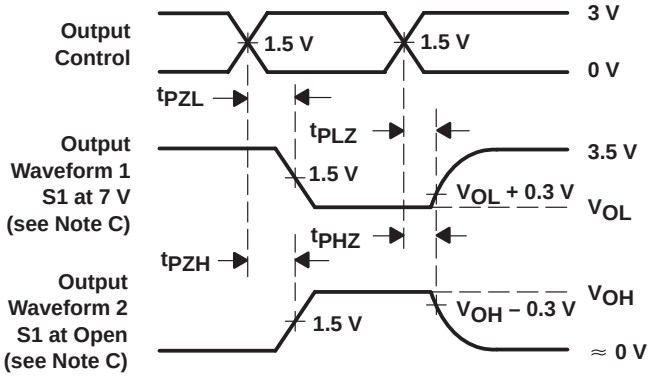
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NON-INVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 13. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
SN74ABT18504PM	ACTIVE	LQFP	PM	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
SN74ABT18504PMG4	ACTIVE	LQFP	PM	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
SN74ABT18504PMR	ACTIVE	LQFP	PM	64	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
SN74ABT18504PMRG4	ACTIVE	LQFP	PM	64	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

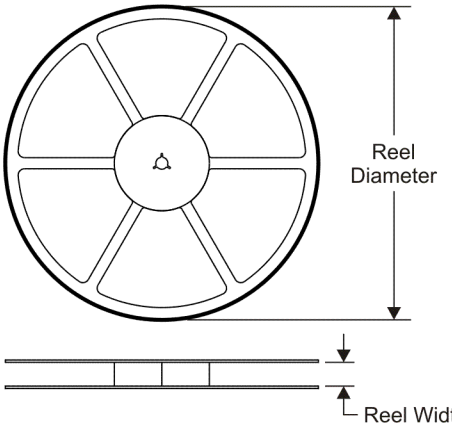
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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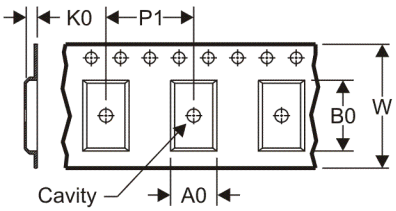
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

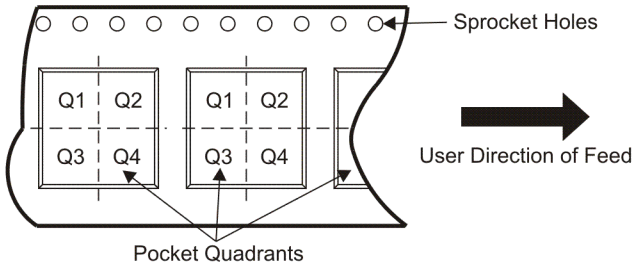


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

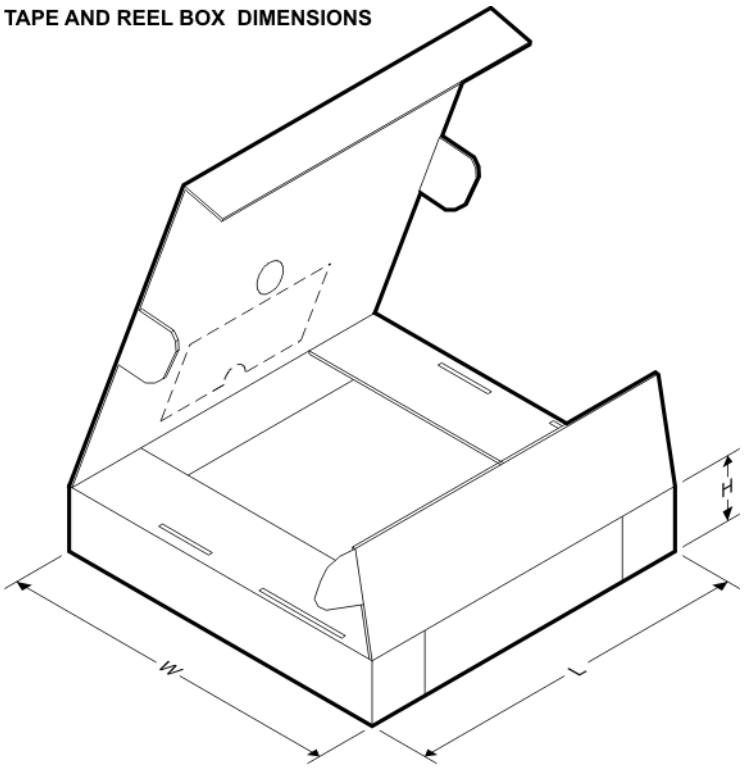
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ABT18504PMR	LQFP	PM	64	1000	330.0	24.4	12.3	12.3	2.5	16.0	24.0	Q2

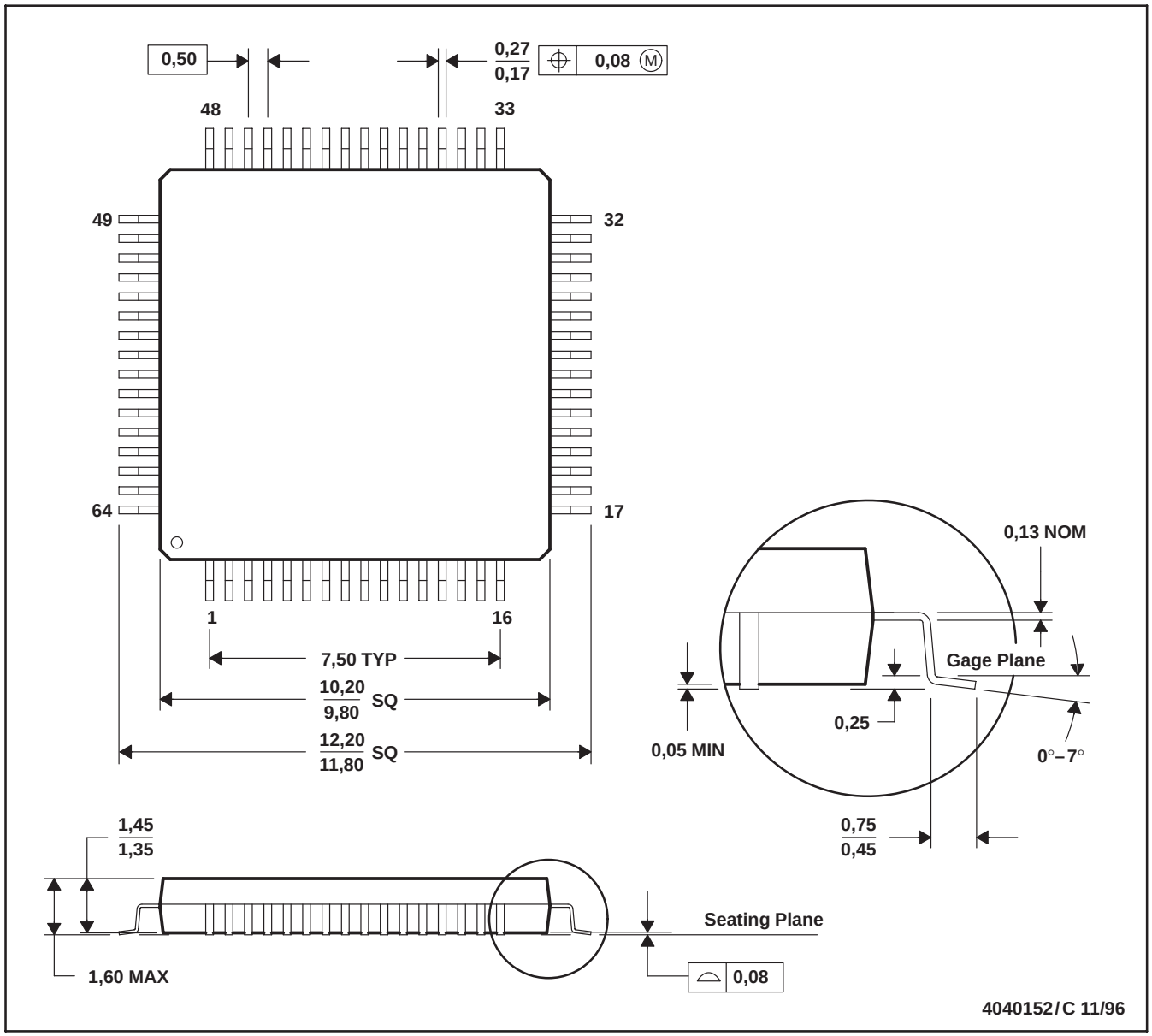
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ABT18504PMR	LQFP	PM	64	1000	346.0	346.0	41.0

PM (S-PQFP-G64) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026
D. May also be thermally enhanced plastic with leads connected to the die pads.

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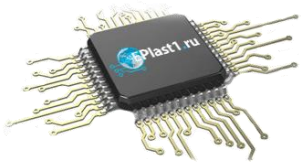
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