Quad Analog-to-Digital Converter (ADC)

Data Sheet **ADAU1978**

FEATURES

- Four 2 V rms differential inputs
- On-chip phase-locked loop (PLL) for master clock
- Low electromagnetic interference (EMI) design
- 106 dB analog-to-digital converter (ADC) dynamic range
- Total harmonic distortion + noise (THD + N): −95 dB
- Selectable digital high-pass filter
- 24-bit stereo ADC with 8 kHz to 192 kHz sample rates
- Digital volume control with autoramp function
- I²C/SPI controllable for flexibility
- Software-controllable clickless mute
- Software power-down
- Right justified, left justified, I²S, and TDM modes
- Master and slave operation modes
- 40-lead LFCSP package
- Qualified for automotive applications

APPLICATIONS

- Automotive audio systems
- Active noise cancellation systems

GENERAL DESCRIPTION

The ADAU1978 incorporates four high performance, analog-to-digital converters (ADCs) with 2 V rms capable ac-coupled inputs. The ADCs use a multibit sigma-delta (Σ-Δ) architecture with continuous time front end for low EMI. An I²C/serial peripheral interface (SPI) control port is included that allows a microcontroller to adjust volume and many other parameters. The ADAU1978 uses only a single 3.3 V supply. The part internally generates the required digital DVDD supply. The low power architecture reduces the power consumption. The ADAU1978 is available in a 40-lead LFCSP package. The on-chip PLL can derive the master clock from an external clock input or frame clock (sample rate clock). When fed with the frame clock, it eliminates the need for a separate high frequency master clock in the system.

Note that throughout this data sheet, multifunction pins, such as SCL/CCLK, are referred to either by the entire pin name or by a single function of the pin, for example, CCLK, when only that function is relevant.

FUNCTIONAL BLOCK DIAGRAM

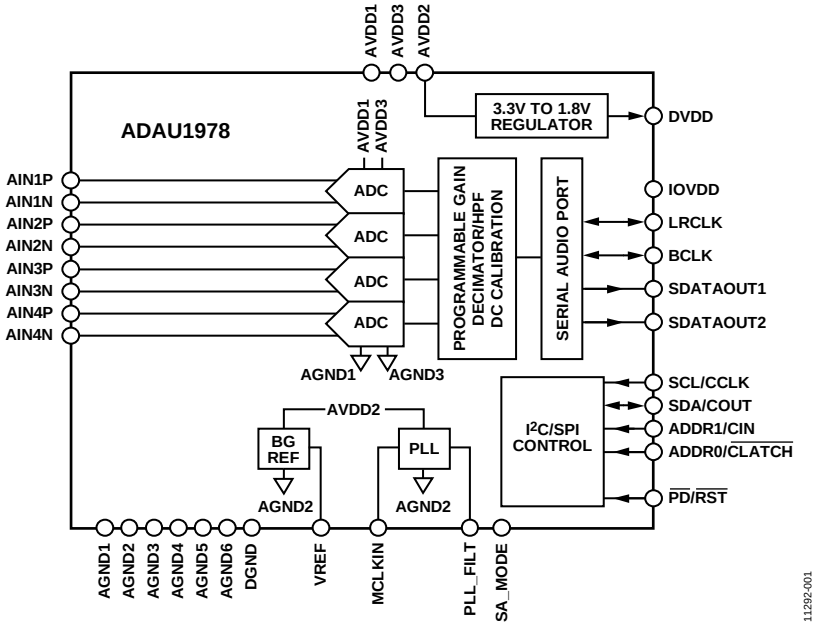


Figure 1.

Rev. 0 **Document Feedback**

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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
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REVISION HISTORY

5/13—Revision 0: Initial Version

SPECIFICATIONS

Performance of all channels is identical, exclusive of the interchannel gain mismatch and interchannel phase deviation specifications. AVDDx/IOVDD = 3.3 V; DVDD (internally generated) = 1.8 V; T_A = −40°C to +105°C, unless otherwise noted. Master clock = 12.288 MHz (48 kHz f_S, 256 × f_S mode); input sample rate = 48 kHz; measurement bandwidth = 20 Hz to 20 kHz; word width = 24 bits; load capacitance (digital output) = 20 pF; load current (digital output) = ±1 mA; digital input voltage high = 2.0 V; and digital input voltage low = 0.8 V.

ANALOG PERFORMANCE SPECIFICATIONS

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
LINE INPUT					
Full-Scale AC Differential Input Voltage			2		V rms
Full-Scale Single-Ended Input Voltage			1		V rms
Input Common-Mode Voltage	$V_{IN, cm}$ at AINxP/AINxN pins		1.5		V dc
ANALOG-TO-DIGITAL CONVERTERS					
Differential Input Resistance	Between AINxP and AINxN		28.6		kΩ
Single-Ended Input Resistance	Between AINxP and AINxN		14.3		kΩ
ADC Resolution			24		Bits
Dynamic Range (A-Weighted) Line Input[1]	Input = 1 kHz, −60 dBFS (0 dBFS = 2 V rms input)	103	106		dB
Total Harmonic Distortion + Noise (THD + N)	Input = 1 kHz, −1 dBFS (0 dBFS = 2 V rms input)		−95	−88	dB
Digital Gain Post ADC		0		60	dB
Gain Error		−10		+10	%
Interchannel Gain Mismatch		−0.25		+0.25	dB
Gain Drift			100		ppm/°C
Common-Mode Rejection Ratio (CMRR)	200 mV rms, 1 kHz	50	65		dB
	200 mV rms, 20 kHz		56		dB
Power Supply Rejection Ratio (PSRR)	100 mV rms, 1 kHz on AVDD = 3.3 V		70		dB
Interchannel Isolation			100		dB
Interchannel Phase Deviation			0		Degrees
REFERENCE					
Internal Reference Voltage	VREF pin	1.47	1.50	1.54	V
Output Impedance			20		kΩ
ADC SERIAL PORT					
Output Sample Rate		8		192	kHz

[1] This is for a sampling frequency, f_S, ranging from 44.1 kHz to 192 kHz.

DIGITAL INPUT/OUTPUT SPECIFICATIONS

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT					
High Level Input Voltage (V_{IH})		0.7 × IOVDD			V
Low Level Input Voltage (V_{IL})				0.3 × IOVDD	V
Input Leakage Current		−10		+10	µA
Input Capacitance				5	pF
OUTPUT					
High Level Output Voltage (V_{OH})	I_{OH} = 1 mA	IOVDD − 0.60			V
Low Level Output Voltage (V_{OL})	I_{OL} = 1 mA			0.4	V

POWER SUPPLY SPECIFICATIONS

AVDD = 3.3 V, DVDD = 1.8 V, IOVDD = 3.3 V, and f_S = 48 kHz (master mode), unless otherwise noted.

Table 3.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
SUPPLY					
DVDD	On-chip low dropout (LDO) regulator	1.62	1.8	1.98	V
AVDDx	AVDD	3.0	3.3	3.6	V
IOVDD	IOVDD	1.62	3.3	3.6	V
IOVDD CURRENT	Master clock = 256 × f_S				
Normal Operation	f_S = 48 kHz		450		µA
	f_S = 96 kHz		880		µA
	f_S = 192 kHz		1.75		mA
Power-Down	f_S = 48 kHz to 192 kHz		20		µA
AVDDx CURRENT					
Normal Operation	4-channel ADC, DVDD internal		14		mA
	4-channel ADC, DVDD external		9.5		mA
Power-Down			270		µA
DVDD CURRENT					
Normal Operation	DVDD external		4.5		mA
Power-Down			65		µA
POWER DISSIPATION					
Normal Operation	Master clock = 256 f_S, 48 kHz				
Analog Supply	DVDD internal		46.2		mW
	DVDD external		31		mW
Digital Supply	DVDD external		8.1		mW
Digital I/O Supply	IOVDD = 3.3 V		1.49		mW
Power-Down, All Supplies			960		µW

DIGITAL FILTER SPECIFICATIONS

Table 4.

Parameter	Mode	Factor	Min	Typ	Max	Unit
ADC DECIMATION FILTER	All modes, typical at f_S = 48 kHz					
Pass Band		0.4375 × f_S		21		kHz
Pass-Band Ripple				±0.015		dB
Transition Band		0.5 × f_S		24		kHz
Stop Band		0.5625 × f_S		27		kHz
Stop-Band Attenuation			79			dB
Group Delay	f_S = 8 kHz to 96 kHz	22.9844/f_S		479		µs
	f_S = 192 kHz			35		µs
HIGH-PASS FILTER	All modes, typical at 48 kHz					
Cutoff Frequency	At −3 dB point			0.9375		Hz
Phase Deviation	At 20 Hz			10		Degrees
Settling Time				1		sec
ADC DIGITAL GAIN	All modes		0		60	dB
Gain Step Size				0.375		dB

TIMING SPECIFICATIONS

Table 5.

Parameter	Limit at Min	Limit at Max	Unit	Description
INPUT MASTER CLOCK (MCLK)				
Duty Cycle	40	60	%	MCLKIN duty cycle; MCLKIN at 256 × f_S, 384 × f_S, 512 × f_S, and 768 × f_S
f_{MCLKIN}	See Table 9		MHz	MCLKIN frequency, PLL in MCLK mode
RESET				
Reset Pulse	15		ns	$\overline{RST}$ low
PLL				
Lock Time		10	ms	
I^2C PORT				See Figure 4
f_{SCL}		400	kHz	SCL frequency
t_{SCLH}	0.6		µs	SCL high
t_{SCLL}	1.3		µs	SCL low
t_{SCS}	0.6		µs	Setup time; relevant for repeated start condition
t_{SCH}	0.6		µs	Hold time; after this period of time, the first clock pulse is generated
t_{DS}	100		ns	Data setup time
t_{DH}	0			Data hold time
t_{SCR}		300	ns	SCL rise time
t_{SCF}		300	ns	SCL fall time
t_{SDR}		300	ns	SDA rise time
t_{SDF}		300	ns	SDA fall time
t_{BFT}	1.3		µs	Bus-free time; time between stop and start
t_{SUSTO}	0.6		µs	Setup time for stop condition
SPI PORT				see Figure 3
f_{CCLK}		10	MHz	CCLK frequency
t_{CCPH}	35		ns	CCLK high
t_{CCPL}	35		ns	CCLK low
t_{CDS}	10		ns	CIN setup to CCLK rising
t_{CDH}	10		ns	CIN hold from CCLK rising
t_{CLS}	10		ns	$\overline{CLATCH}$ setup to CCLK rising
t_{CLH}	40		ns	$\overline{CLATCH}$ hold from CCLK rising
t_{CLPH}	10		ns	$\overline{CLATCH}$ high
t_{COE}		30	ns	COUT enable from $\overline{CLATCH}$ falling
t_{COD}		30	ns	COUT delay from CCLK falling
t_{COTS}		30	ns	COUT tristate from $\overline{CLATCH}$ rising
ADC SERIAL PORT				see Figure 2
t_{ABH}	10		ns	BCLK high, slave mode
t_{ABL}	10		ns	BCLK low, slave mode
t_{ALS}	10		ns	LRCLK setup to BCLK rising, slave mode
t_{ALH}	5		ns	LRCLK hold from BCLK rising, slave mode
t_{ABDD}		18	ns	SDATAOUTx delay from BCLK falling

Timing Digrams

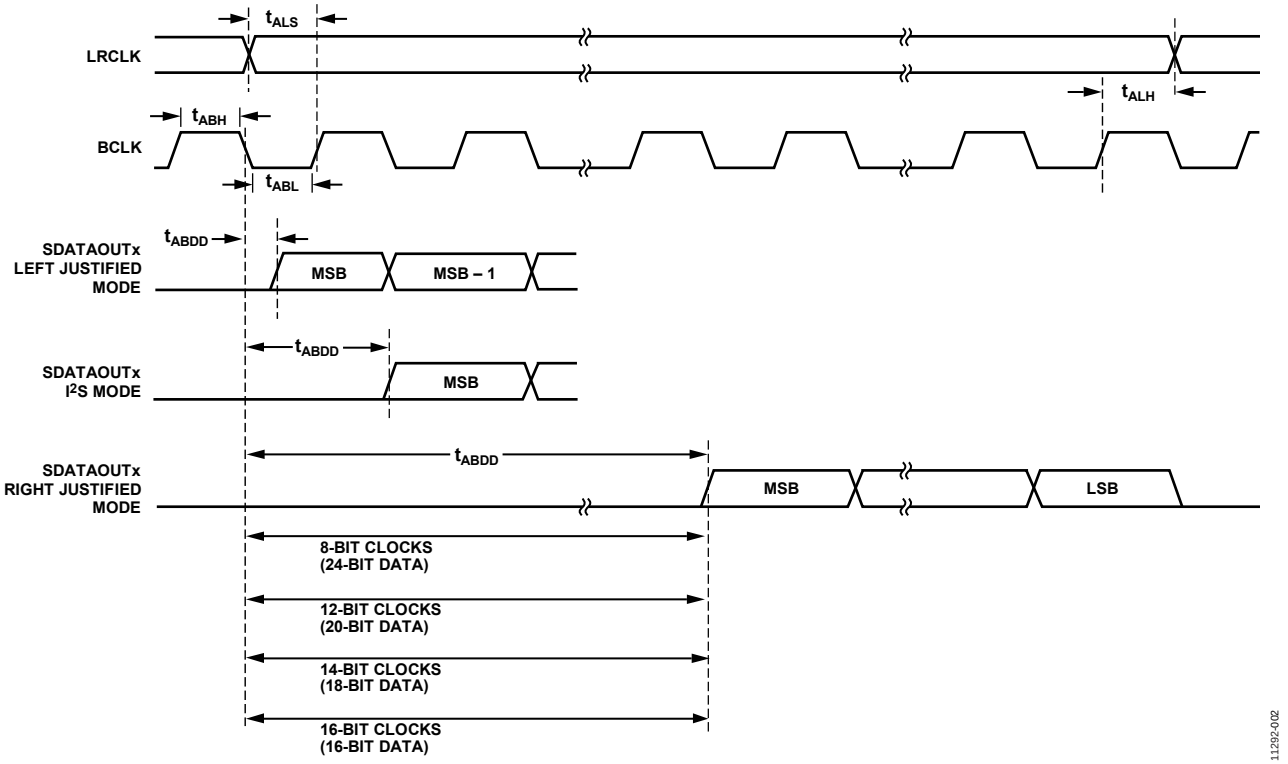


Figure 2. Serial Output Port Timing

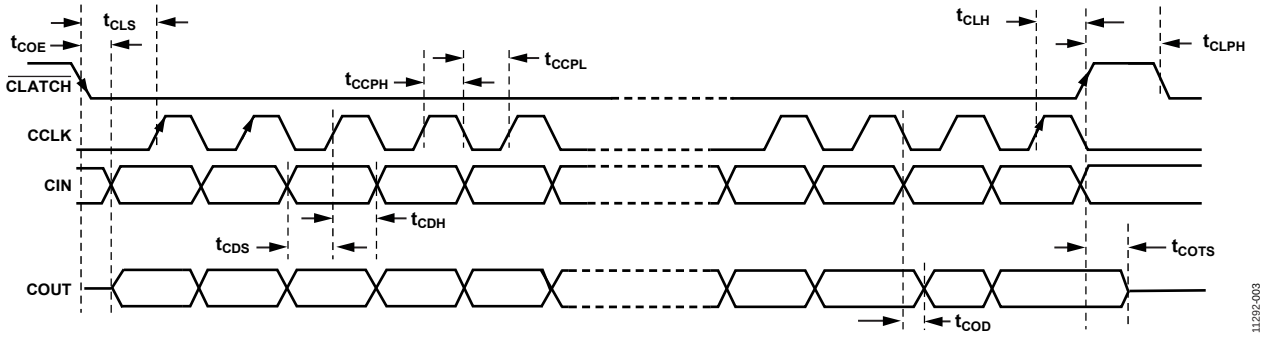


Figure 3. SPI Port Timing

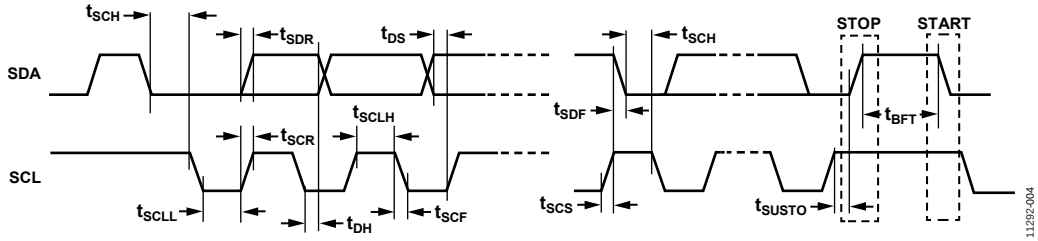


Figure 4. I²C Port Timing

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
Analog (AVDDx) Supply	−0.3 V to +3.6 V
Digital Supply	
DVDD	−0.3 V to +1.98 V
IOVDD	−0.3 V to +3.63 V
Input Current (Except Supply Pins)	±20 mA
Analog Input Voltage (Signal Pins)	−0.3 V to +3.6 V
Digital Input Voltage (Signal Pins)	−0.3 V to +3.6 V
Operating Temperature Range (Ambient)	−40°C to +105°C
Junction Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} represents junction-to-ambient thermal resistance, and θ_{JC} represents the junction-to-case thermal resistance. All characteristics are for a standard JEDEC board per JESD51.

Table 7. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
40-Lead LFCSP	32.8	1.93	°C/W

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

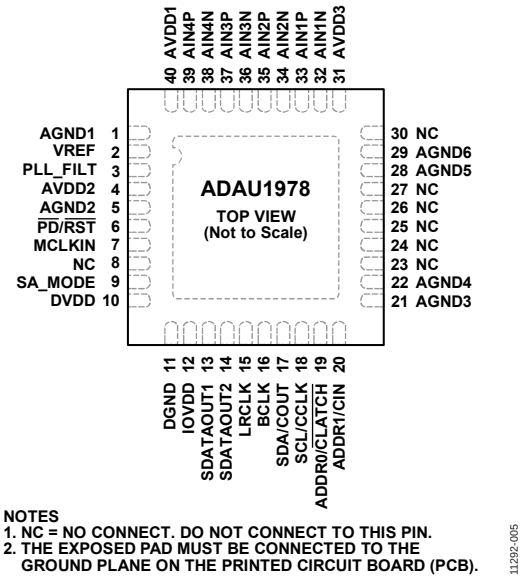


Figure 5. Pin Configuration

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
1	AGND1	P	Analog Ground.
2	VREF	O	Voltage Reference. Decouple VREF to AGND with a 10 µF capacitor in parallel with a 100 nF capacitor.
3	PLL_FILT	O	PLL Loop Filter. Return PLL_FILT to AVDD using recommended loop filter components.
4	AVDD2	P	Analog Power Supply. Connect AVDD2 to an analog 3.3 V supply.
5	AGND2	P	Analog Ground.
6	$\overline{PD}/\overline{RST}$	I	Power-Down/Reset (Active Low).
7	MCLKIN	I	Master Clock Input.
8, 23 to 27, 30	NC		No Connect. Do not connect to these pins. Leave the NC pins open.
9	SA_MODE	I	Standalone Mode. Connect SA_MODE to IOVDD using 10 kΩ pull-up resistor for standalone mode.
10	DVDD	O	1.8 V Digital Power Supply Output. Decouple to DGND with 100 nF and 10 µF capacitors.
11	DGND	P	Digital Ground.
12	IOVDD	P	Digital I/O Power Supply. Connect IOVDD to a supply from 1.8 V to 3.3 V.
13	SDATAOUT1	O	ADC Serial Data Output Pair 1 (ADC L1 and ADC R1).
14	SDATAOUT2	O	ADC Serial Data Output Pair 2 (ADC L2 and ADC R2).
15	LRCLK	I/O	Frame Clock for ADC Serial Port.
16	BCLK	I/O	Bit Clock for ADC Serial Port.
17	SDA/COUT	I/O	Serial Data Out (I^2C)/Control Data Output (SPI).
18	SCL/CCLK	I	Serial Clock Input (I^2C)/Control Clock Input (SPI).
19	$\overline{ADDR0}/\overline{CLATCH}$	I	Chip Address Bit 0 Setting (I^2C)/Chip Select Input for Control Data (SPI).
20	ADDR1/CIN	I	Chip Address Bit 1 Setting (I^2C)/Control Data Input (SPI).
21	AGND3	P	Analog Ground.
22	AGND4	P	Analog Ground.
28	AGND5	P	Analog Ground.
29	AGND6	P	Analog Ground.
31	AVDD3	P	Analog Power Supply. Connect AVDD3 to an analog 3.3 V supply.

Pin No.	Mnemonic	Type[1]	Description
32	AIN1N	I	Analog Input Channel 1 Inverting Input.
33	AIN1P	I	Analog Input Channel 1 Noninverting Input.
34	AIN2N	I	Analog Input Channel 2 Inverting Input.
35	AIN2P	I	Analog Input Channel 2 Noninverting Input.
36	AIN3N	I	Analog Input Channel 3 Inverting Input.
37	AIN3P	I	Analog Input Channel 3 Noninverting Input.
38	AIN4N	I	Analog Input Channel 4 Inverting Input.
39	AIN4P	I	Analog Input Channel 4 Noninverting Input.
40	AVDD1	P	Analog Power Supply. Connect AVDD1 to an analog 3.3 V supply.
	EP		Exposed Pad. The exposed pad must be connected to the ground plane on the printed circuit board (PCB).

[1] P = power, O = output, I = input, I/O = input/output.

TYPICAL PERFORMANCE CHARACTERISTICS

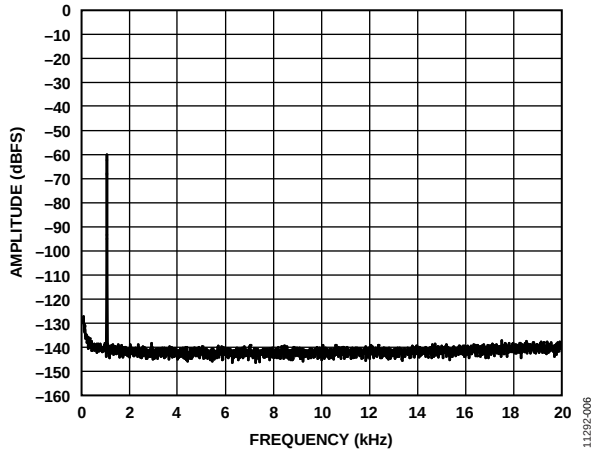


Figure 6. Fast Fourier Transform, 2 mV Differential Input at f_S = 48 kHz

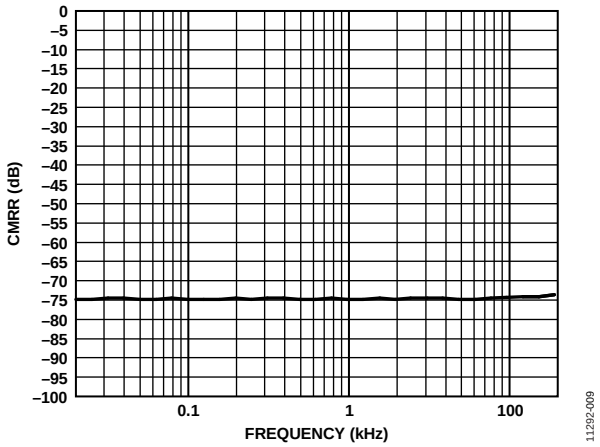


Figure 9. CMRR Differential Input, Referenced to 200 mV Differential Input

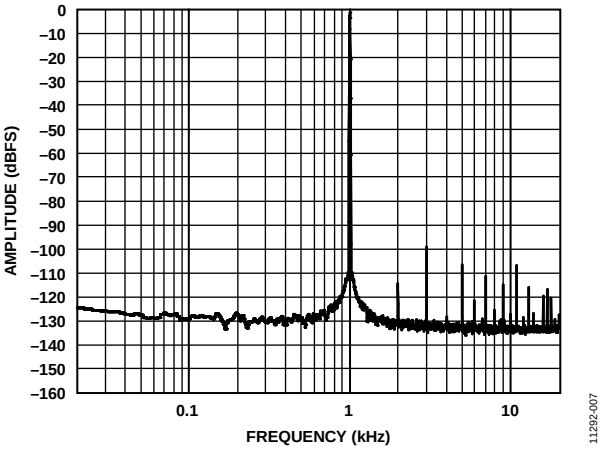


Figure 7. Fast Fourier Transform, −1 dBFS Differential Input

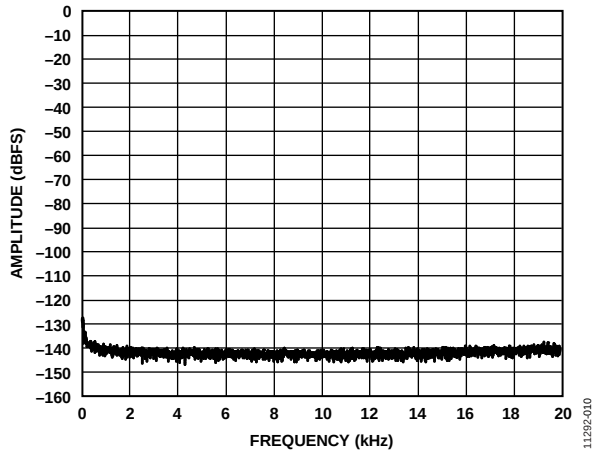


Figure 10. Fast Fourier Transform, No Input

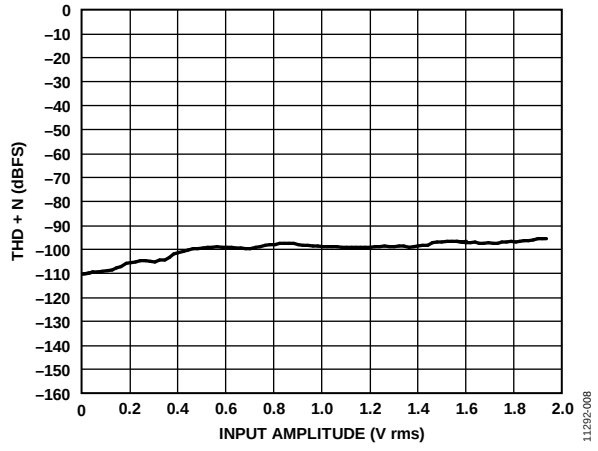


Figure 8. THD + N vs. Input Amplitude

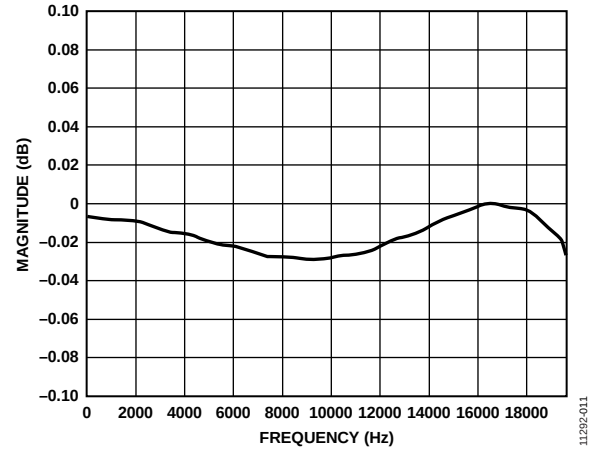


Figure 11. ADC Pass-Band Ripple at f_S = 48 kHz

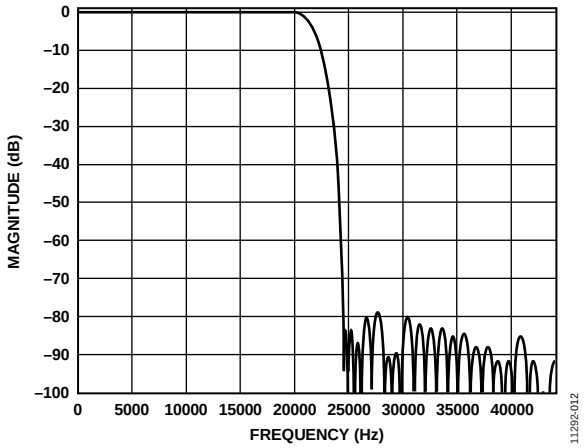


Figure 12. ADC Filter Stop-Band Response at f_S = 48 kHz

THEORY OF OPERATION

OVERVIEW

The ADAU1978 incorporates four high performance ADCs and a phase-locked loop circuit for generating the necessary on-chip clock signals.

POWER SUPPLY AND VOLTAGE REFERENCE

The ADAU1978 requires a single 3.3 V power supply. Separate power supply input pins are provided for the analog and boost converter. Decouple these pins to AGND with 100 nF ceramic chip capacitors placed as close as possible to the pins to minimize noise pickup. A bulk aluminum electrolytic capacitor of at least 10 µF must be provided on the same PCB as the ADC. It is important that the analog supply be as clean as possible for best performance.

The supply voltage for the digital core (DVDD) is generated using an internal low dropout regulator. The typical DVDD output is 1.8 V and must be decoupled using a 100 nF ceramic capacitor and a 10 µF capacitor. Place the 100 nF ceramic capacitor as close as possible to the DVDD pin.

The voltage reference for the analog blocks is generated internally and output at the VREF pin (Pin 2). The typical voltage at the pin is 1.5 V with an AVDDx of 3.3 V.

All digital inputs are compatible with TTL and CMOS levels. All outputs are driven from the IOVDD supply. The IOVDD can be in the 1.8 V to 3.3 V range. The IOVDD pin must be decoupled with a 100 nF capacitor placed as close to the IOVDD pin as possible.

The ADC internal voltage reference is output from the VREF pin and must be decoupled using a 100 nF ceramic capacitor in parallel with a 10 µF capacitor. The VREF pin has limited current capability. The voltage reference is used as a reference to the ADC; therefore, it is recommended not to draw current from this pin for external circuits. When using this reference, use a noninverting amplifier buffer to provide a reference to other circuits in the application.

In reset mode, the VREF pin is disabled to save power and is enabled only when the $\overline{\text{RST}}$ pin is pulled high.

POWER-ON RESET SEQUENCE

The ADAU1978 requires that a single 3.3 V power supply be provided externally at the AVDDx pin. The part internally generates DVDD (1.8 V), which is used for the digital core of the ADC. The DVDD supply output pin (Pin 10) is provided to connect the decoupling capacitors to DGND. The typical recommended values for the decoupling capacitors are 100 nF in parallel with 10 µF. During a reset, the DVDD regulator is disabled to reduce power consumption. After the $\overline{\text{PD}}/\overline{\text{RST}}$ pin (Pin 6) is pulled high, the part enables the DVDD regulator. However, the internal ADC and digital core reset is controlled by the internal $\overline{\text{POR}}$ signal (power-on reset) circuit, which monitors the DVDD level. Therefore, the device does not come out of a reset until DVDD reaches 1.2 V and the $\overline{\text{POR}}$ signal is released. The DVDD settling time depends on the charge-up time for the external capacitors and on the AVDDx ramp-up time.

The internal power-on reset circuit is provided with hysteresis to ensure that a reset of the part is not initiated by an instantaneous glitch on DVDD. The typical trip points are 1.2 V with $\overline{\text{PD}}/\overline{\text{RST}}$ high and 0.6 V (±20%) with $\overline{\text{PD}}/\overline{\text{RST}}$ low. This ensures that the core is not reset until the DVDD level falls below the 0.6 V trip point.

As soon as the $\overline{\text{PD}}/\overline{\text{RST}}$ pin is pulled high, the internal regulator starts charging up C_{EXT} on the DVDD pin. The DVDD charge-up time is based on the output resistance of the regulator and the external decoupling capacitor. The time constant can be calculated as

$$t_C = R_{OUT} \times C_{EXT}$$

where R_{OUT} = 20 Ω typical.

For example, if C_{EXT} is 10 µF, t_C is 200 µs and is the time that it takes to reach the DVDD voltage, within 63.6%.

The power-on reset circuit releases an internal reset of the core when DVDD reaches 1.2 V (see Figure 13). Therefore, it is recommended to wait for at least the t_C period to elapse before sending I²C or SPI control signals.

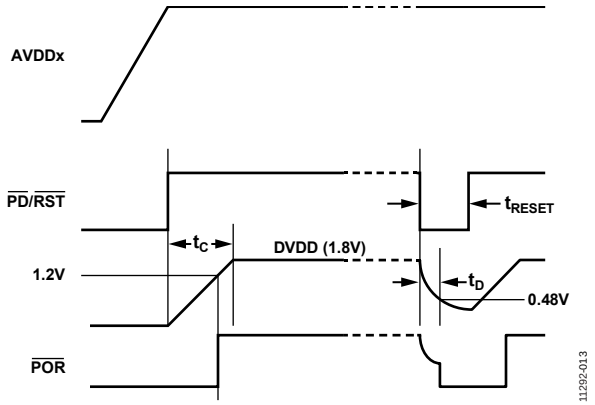


Figure 13. Power-On Reset Timing

When applying a hardware reset to the part by pulling the $\overline{\text{PD}}/\overline{\text{RST}}$ pin (Pin 6) low and then high, there are certain time restrictions. During the $\overline{\text{PD}}/\overline{\text{RST}}$ low pulse period, the DVDD starts discharging. The discharge time constant is decided on by the internal resistance of the regulator and C_{EXT}. The time required for DVDD to fall from 1.8 V to 0.48 V (0.6 V − 20%) can be estimated using the following equation:

$$t_D = 1.32 \times R_{INT} \times C_{EXT}$$

where R_{INT} = 64 kΩ typical. (R_{INT} can vary due to process by ±20%.)

For example, if C_{EXT} is 10 µF, t_D is 0.845 sec.

Depending on C_{EXT}, t_D may vary and, in turn, affect the minimum hold period for the $\overline{\text{PD}}/\overline{\text{RST}}$ pulse. The $\overline{\text{PD}}/\overline{\text{RST}}$ pulse

must be held low for the t_D time period to initialize the core properly.

The required $\overline{PD}/\overline{RST}$ low pulse period can be reduced by adding a resistor across C_{EXT}. The new t_D value can then be calculated as

$$t_D = 1.32 \times R_{EQ} \times C_{EXT}$$

where R_{EQ} = 64 kΩ || R_{EXT}.

The resistor ensures that DVDD not only discharges quickly during a reset or an AVDDx power loss but also resets the internal blocks correctly. Note that some power loss in this resistor is to be expected because the resistor constantly draws current from DVDD. The typical value for C_{EXT} is 10 µF and for R_{EXT} is 3 kΩ. This results in a time constant of

$$t_D = 1.32 \times R_{EQ} \times C_{EXT} = 37.8 \text{ ms}$$

where R_{EQ} = 2.866 kΩ (64 kΩ || 3 kΩ).

Using this equation at a set C_{EXT} value, the R_{EXT} can be calculated for a desired $\overline{PD}/\overline{RST}$ pulse period.

There is also a software reset bit (S_RST, Bit 7 of Register 0x00) available that can be used to reset the part, but note that during an AVDDx power loss, the software reset may not ensure proper initialization because DVDD may not be stable.

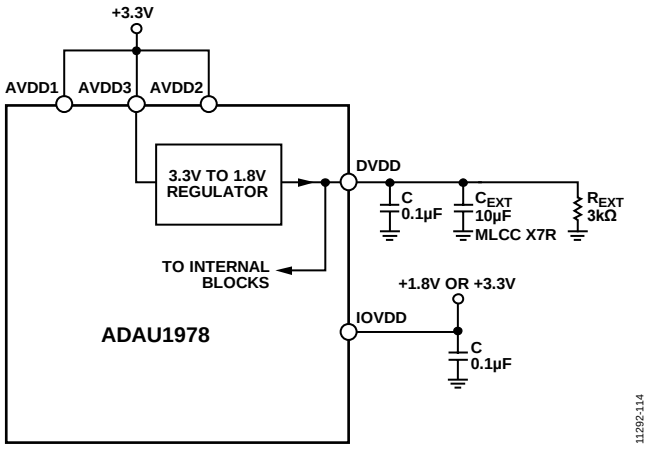


Figure 14. DVDD Regulator Output Connections

PLL AND CLOCK

The ADAU1978 has a built-in analog PLL to provide a jitter-free master clock to the internal ADC. The PLL must be programmed for the appropriate input clock frequency. The PLL_CONTROL Register 0x01 is used for setting the PLL.

The CLK_S bit (Bit 4) of Register 0x01 is used for setting the clock source for the PLL. The clock source can be either the MCLKIN pin or the LRCLK pin (slave mode). In LRCLK mode, the PLL can support sample rates between 32 kHz and 192 kHz.

In MCLK input mode, the MCS bits (Bits[2:0] of Register 0x01) must be set to the desired input clock frequency for the MCLKIN pin. Table 9 shows the input master clock frequency required for the most common sample rates and the MCS bit settings.

The PLL_LOCK bit (Bit 7) of Register 0x01 indicates the lock status of the PLL. It is recommended that after initial power-up the PLL lock status be read to ensure that the PLL outputs the correct frequency before unmuting the audio outputs.

Table 9. Required Input Master Clock Frequency for Common Sample Rates

MCS (Bits[2:0])	f_S (kHz)	Frequency Multiplication Ratio	MCLKIN Frequency (MHz)
000	32	128 × f_S	4.096
001	32	256 × f_S	8.192
010	32	384 × f_S	12.288
011	32	512 × f_S	16.384
100	32	768 × f_S	24.576
000	44.1	128 × f_S	5.6448
001	44.1	256 × f_S	11.2896
010	44.1	384 × f_S	16.9344
011	44.1	512 × f_S	22.5792
100	44.1	768 × f_S	33.8688
000	48	128 × f_S	6.144
001	48	256 × f_S	12.288
010	48	384 × f_S	18.432
011	48	512 × f_S	24.576
100	48	768 × f_S	36.864
000	96	64 × f_S	6.144
001	96	128 × f_S	12.288
010	96	192 × f_S	18.432
011	96	256 × f_S	24.576
100	96	384 × f_S	36.864
000	192	32 × f_S	6.144
001	192	64 × f_S	12.288
010	192	96 × f_S	18.432
011	192	128 × f_S	24.576
100	192	192 × f_S	36.864

The PLL can accept the audio frame clock (sample rate clock) as the input, but the serial port must be configured as a slave, and the frame clock must be fed to the part from the master. It is strongly recommended that the PLL be disabled, reprogrammed with the new setting, and then reenabled. A lock bit is provided that can be polled via the I2C to check whether the PLL has acquired lock.

The PLL requires an external filter, which is connected at the PLL_FILT pin (Pin 3). The recommended PLL filter circuit for MCLK or LRCLK mode is shown in Figure 15. Using NPO capacitors is recommended for temperature stability. Place the filter components close to the device for best performance.

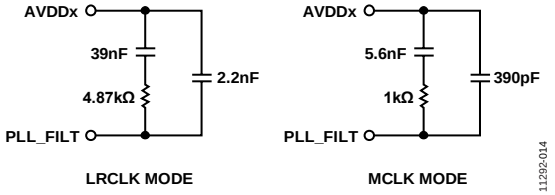


Figure 15. PLL Filter

ANALOG INPUTS

The ADAU1978 has four differential analog inputs. The ADCs can accommodate both dc- and ac-coupled input signals.

The block diagram shown in Figure 16 represents the typical input circuit.

In most audio applications, the dc content of the signal is removed by using a coupling capacitor. However, the ADAU1978 consists of a unique input structure that allows ac coupling of the input signals. The typical input resistance is approximately 14 kΩ from each input to AGND.

The high-pass filter has a 1.4 Hz, 6 dB per octave cutoff at a 48 kHz sample rate. The cutoff frequency scales directly with the sample frequency. However, care is required in dc-coupled applications to ensure that the common-mode dc voltage does not exceed the specified limit. The input required for the full-scale ADC output (0 dBFS) is typically 2 V rms differential.

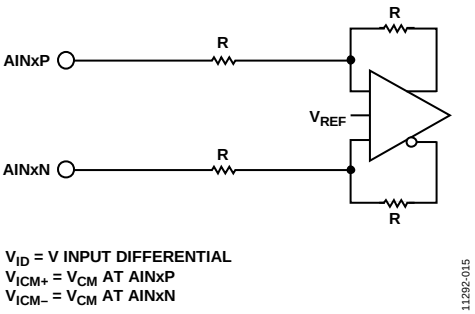


Figure 16. Analog Input Block

Line Inputs

This section describes some of the possible ways to connect the line level inputs of the ADAU1978.

Line Input Balanced or Differential Input DC-Coupled Case

For example, for an input signal of 2 V rms differential with approximately 1.5 V common-mode dc, the signal at each input pin has a 1 V rms or 2.8 V p-p signal swing. With common-mode dc of 1.5 V, the signal can swing between (1.5 V + 1.414 V) = 2.914 V to (1.5 V − 1.414 V) = 0.086 V at each input. Therefore, this is approximately 5.6 V p-p differential across AINxP and AINxN and measures close to 0 dBFS (ac only with a dc high-pass filter) at the ADC output (see Figure 17).

Line Input Balanced or Differential Input AC-Coupled Case

For connecting the ADAU1978 to a head unit amplifier output, ac coupling is recommended. In this case, the AINxP/AINxN pins are at a common-mode level of 1.5 V. The attenuator can be used to reduce the input level if it is more than 2 V rms.

The C1 and C2 values can be found for the required low frequency cutoff using the following equation:

$$C1 \text{ or } C2 = 1/(2 \times \pi \times f_C \times Input\ Resistance)$$

where the *Input Resistance* of the ADAU1978 is 14.3 kΩ typical.

Refer to Figure 18 for information about connecting the line level inputs to the ADAU1978.

Line Input Unbalanced or Single-Ended, Pseudo Differential AC-Coupled Case

For a single-ended application, reduce the signal swing by half because only one input is used for the signal with the other connected to 0 V. Doing this reduces the input signal capability to 1 V rms in the single-ended application and measures approximately −6.16 dBFS (ac only with a dc high-pass filter) at the ADC output.

See Figure 19 for additional information. The value of the C1/C2 is similar to the balanced ac-coupled case previously mentioned in the Line Input Balanced or Differential Input AC-Coupled Case section.

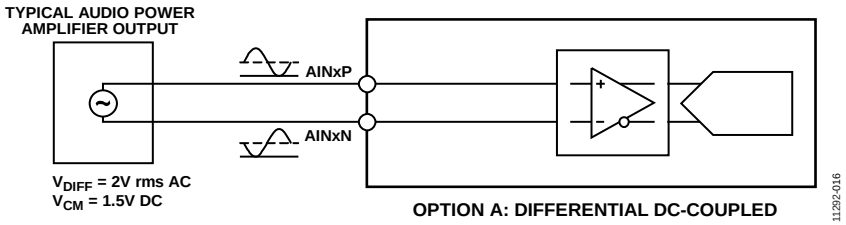


Figure 17. Connecting the Line Level Inputs—Differential DC-Coupled Case

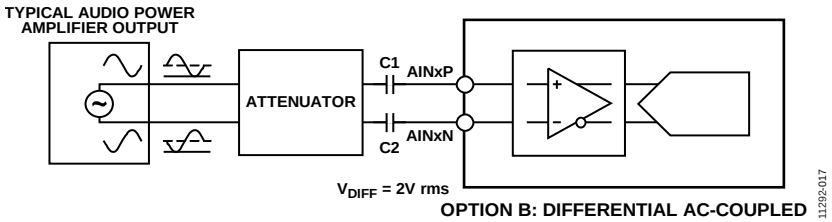


Figure 18. Connecting the Line Level Inputs—Differential AC-Coupled Case

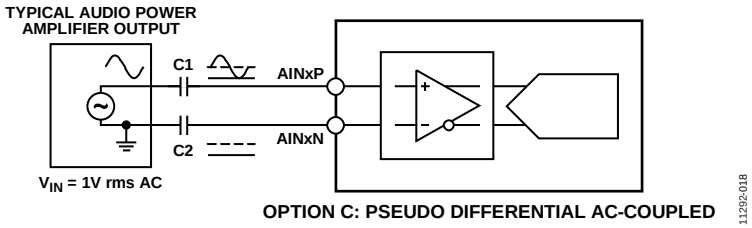


Figure 19. Connecting the Line Level Inputs—Pseudo Differential AC-Coupled Case

ADC

The ADAU1978 contains four sigma-delta (Σ-Δ) ADC channels configured as two stereo pairs with configurable differential/single-ended inputs. The ADC can operate at a nominal sample rate of 32 kHz up to 192 kHz. The ADCs include on-board digital antialiasing filters with 79 dB stop-band attenuation and linear phase response. Digital outputs are supplied through two serial data output pins (one for each stereo pair) and a common frame clock (LRCLK) and bit clock (BCLK). Alternatively, one of the TDM modes can be used to support up to 16 channels on a single TDM data line.

With smaller amplitude input signals, a 10-bit programmable digital gain compensation for an individual channel is provided to scale up the output word to full scale. Take care to avoid overcompensation (large gain compensation), which leads to clipping and THD degradation in the ADC.

The ADCs also have a dc offset calibration algorithm to null the systematic dc offset of the ADC. This feature is useful for dc measurement applications.

ADC SUMMING MODES

The four ADCs can be grouped into either a single stereo ADC or a single mono ADC to increase the SNR for the application. Two options are available: one option for summing two channels of the ADC and another option for summing all four channels of the ADC. Summing is performed in the digital block.

2-Channel Summing Mode

When the SUM_MODE bits (Bits[7:6] of Register 0x0E) are set to 01, the Channel 1 and Channel 2 ADC data are combined and output from the SDATAOUT1 pin. Similarly, the Channel 3 and Channel 4 ADC data are combined and output from the SDATAOUT2 pin. As a result, the SNR improves by 3 dB. For this mode, both Channel 1 and Channel 2 must be connected to the same input signal source. Similarly, Channel 3 and Channel 4 must be connected to the same input signal source.

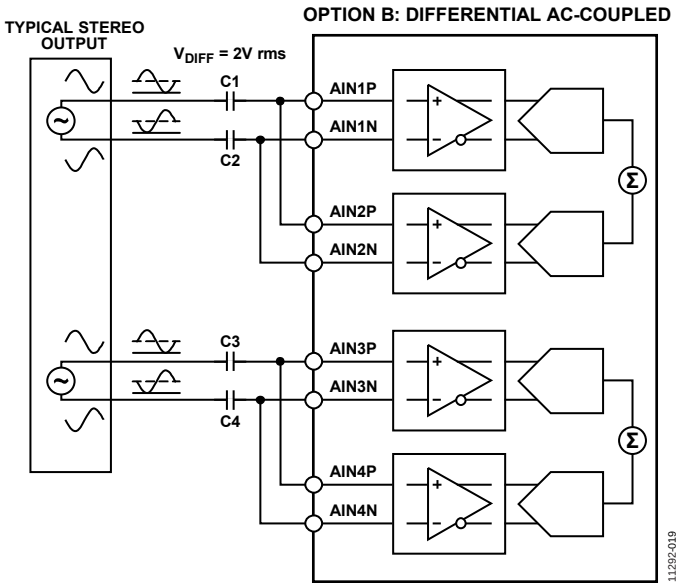


Figure 20. 2-Channel Summing Mode Connection Diagram

4-Channel Summing Mode

When the SUM_MODE Bits (Bits[7:6] of Register 0x0E) are set to 10, the Channel 1 through Channel 4 ADC data are combined and output from the SDATAOUT1 pin. As a result, the SNR improves by 6 dB. For this mode, all four channels must be connected to the same input signal source.

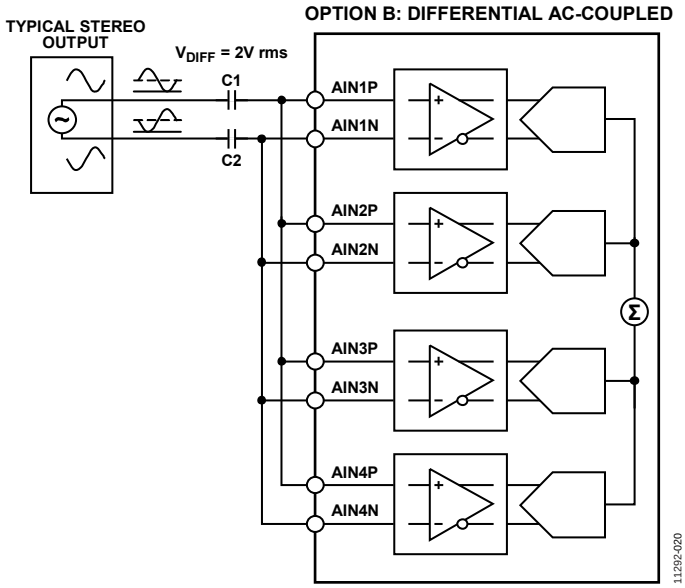


Figure 21. 4-Channel Summing Mode Connection Diagram

SERIAL AUDIO DATA OUTPUT PORTS, DATA FORMAT

The serial audio port comprises four pins: BCLK, LRCLK, SDATAOUT1, and SDATAOUT2. The ADAU1978 ADC outputs are available on the SDATAOUT1 and SDATAOUT2 pins in serial format. The BCLK and LRCLK pins serve as the bit clock and frame clock, respectively. The port can be operated as master or slave and can be set either in stereo mode (2-channel mode) or in TDM multichannel mode. The supported popular audio formats are I²S, left justified (LJ), and right justified (RJ).

Stereo Mode

In 2-channel or stereo mode, the SDATAOUT1 outputs ADC data for Channel 1 and Channel 2, and the SDATOUT2 outputs ADC data for Channel 3 and Channel 4. Figure 22 through Figure 24 show the supported audio formats.

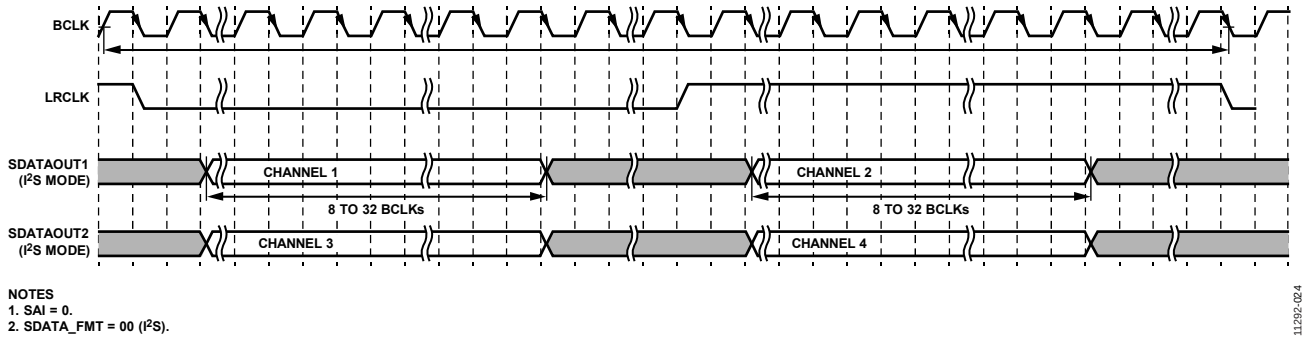


Figure 22. I²S Audio Format

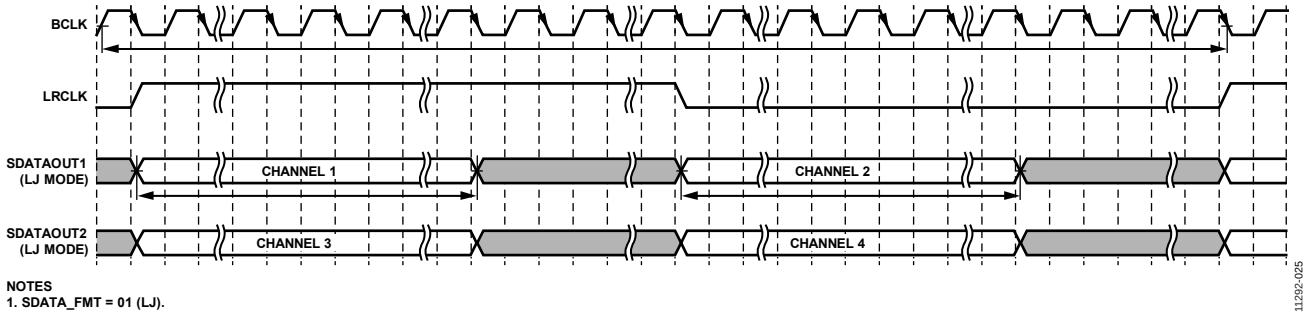


Figure 23. Left Justified Audio Format

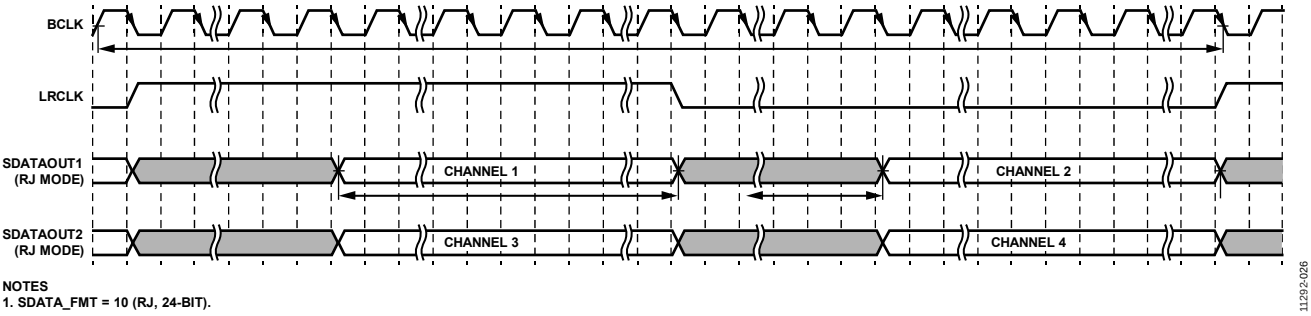


Figure 24. Right Justified Audio Format

TDM Mode

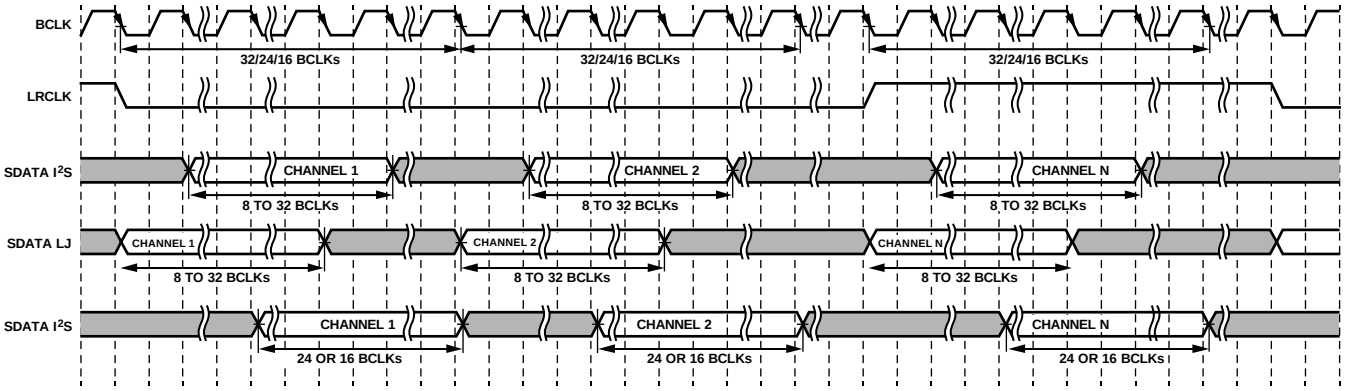
Register 0x05 through Register 0x08 provide programmability for the TDM mode. The TDM slot width, data width, and channel assignment, as well as the pin used to output the data, are programmable.

By default, serial data is output on the SDATAOUT1 pin; however, the SDATA_SEL bit (Bit 7 of Register 0x06) can be used to change the setting so that serial data is output from the SDATAOUT2 pin.

The TDM mode supports two, four, eight, or 16 channels. The ADAU1978 outputs four channels of data in the assigned slots (Figure 27 shows the TDM mode slot assignments). During the unused slots, the output pin becomes high-Z so that the same data line can be shared with other devices on the TDM bus.

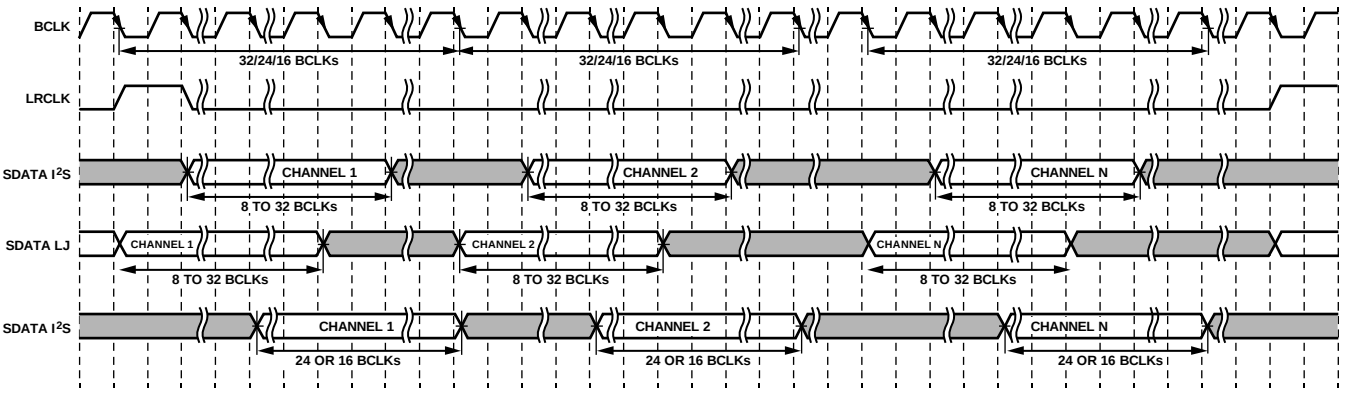
The TDM port can be operated as either a master or a slave. In master mode, the BCLK and LRCLK are output from the ADAU1978, whereas in slave mode, the BCLK and LRCLK pins are set to receive the clock from the master in the system.

Both the nonpulse and pulse modes are supported. In nonpulse mode, the LRCLK signal is typically 50% of the duty cycle, whereas in pulse mode, the LRCLK signal must be at least one BCLK wide (see Figure 25 and Figure 26).



NOTES
1. SAI = 001 (2 CHANNELS), 010 (4 CHANNELS), 011 (8 CHANNELS), 100 (16 CHANNELS).
2. SDATA_FMT = 00 (I²S), 01 (LJ), 10 (RJ, 24-BIT), 11 (RJ, 16-BIT).
3. BCLKEDGE = 0.
4. LR_MODE = 0.
5. SLOT_WIDTH = 00 (32 BCLKs), 01 (24 BCLKs), 10 (16 BCLKs).

Figure 25. TDM Nonpulse Mode Audio Format



NOTES
1. SAI = 001 (2 CHANNELS), 010 (4 CHANNELS), 011 (8 CHANNELS), 100 (16 CHANNELS)
2. SDATA_FMT = 00 (I²S), 01 (LJ), 10 (RJ, 24-BIT), 11 (RJ, 16-BIT)
3. BCLKEDGE = 0
4. LR_MODE = 1
5. SLOT_WIDTH = 00 (32 BCLKs), 01 (24 BCLKs), 10 (16 BCLKs)

Figure 26. TDM Pulse Mode Audio Format

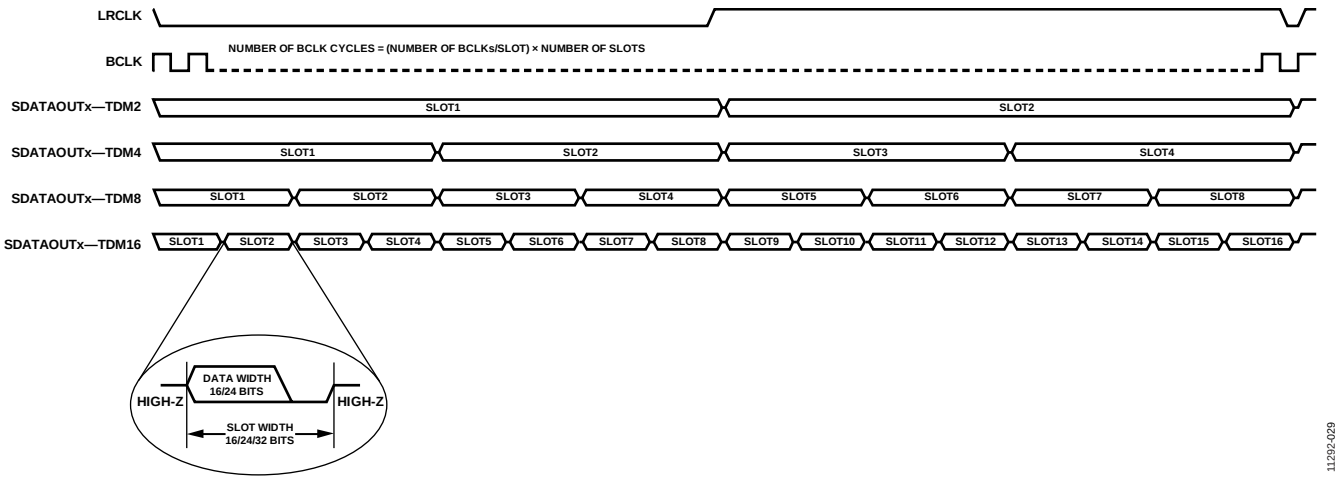


Figure 27. TDM Mode Slot Assignment

Table 10. Bit Clock Frequency TDM Mode

	BCLK Frequency		
Mode	**16-Bit Clocks Per Slot**	**24-Bit Clocks Per Slot**	**32-Bit Clocks Per Slot**
TDM2	$32 \times f_S$	$48 \times f_S$	$64 \times f_S$
TDM4	$64 \times f_S$	$96 \times f_S$	$128 \times f_S$
TDM8	$128 \times f_S$	$192 \times f_S$	$256 \times f_S$
TDM16	$256 \times f_S$	$384 \times f_S$	$512 \times f_S$

The bit clock frequency depends on the sample rate, the slot width, and the number of bit clocks per slot. Table 10 can be used to calculate the BCLK frequency.

The sample rate (f_S) can range from 8 kHz up to 192 kHz. However, in master mode, the maximum bit clock frequency (BCLK) is 24.576 MHz. For example, for a sample rate of 192 kHz, $128 \times f_S$ is the maximum possible BCLK frequency. Therefore, only 128-bit clock cycles are available per TDM frame. There are two options in this case: either operate with a 32-bit data width in TDM4 or operate with a 16-bit data width in TDM8. In slave mode, this limitation does not exist because the bit clock and frame clock are fed to the ADAU1978. Various combinations of BCLK frequencies and modes are available, but take care to choose the combination that is most suitable for the application.

Connection Options

Figure 28 through Figure 32 show the available options for connecting the serial audio port in I²S or TDM mode. In TDM mode, it is recommended to include the pull-down resistor on the data signal to prevent the line from floating when the SDATAOUTx pin of the ADAU1978 becomes high-Z during an inactive period. The resistor value should be such that no more than 2 mA is drawn from the SDATAOUTx pin. Although the resistor value is typically in the 10 kΩ to 47 kΩ range, the appropriate resistor value depends on the devices on the data bus.

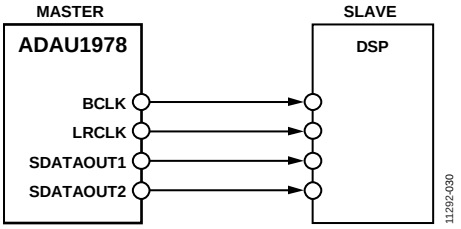


Figure 28. Serial Port Connection Option 1—I²S/Left Justified/Right Justified Modes, ADAU1978 Master

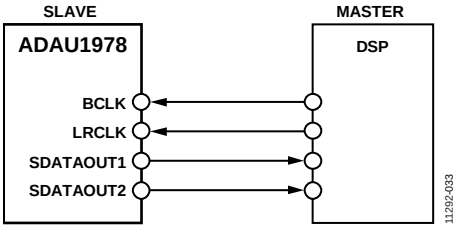


Figure 29. Serial Port Connection Option 2—I²S/Left Justified/Right Justified Modes, ADAU1978 Slave

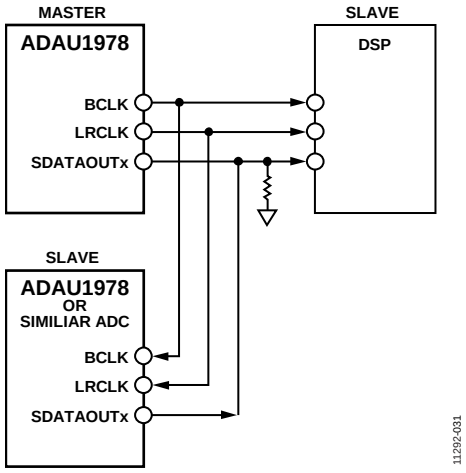


Figure 30. Serial Port Connection Option 3—TDM Mode, ADAU1978 Master

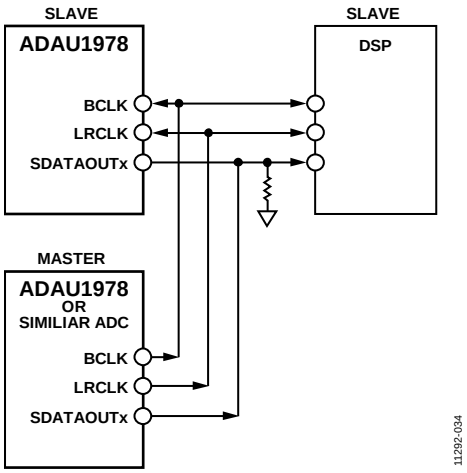


Figure 31. Serial Port Connection Option 4—TDM Mode, Second ADC Master

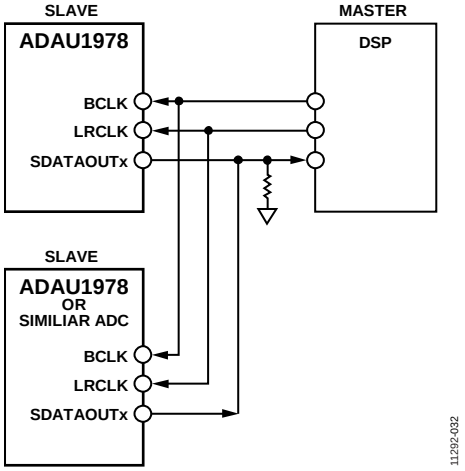


Figure 32. Serial Port Connection Option 5—TDM Mode, DSP Master

CONTROL PORTS

The ADAU1978 control port allows two modes of operation, either 2-wire I²C mode or 4-wire SPI mode, that are used for setting the internal registers of the part. Both the I²C and SPI modes allow read and write capability of the registers. All the registers are eight bits wide. The registers start at Address 0x00 and end at Address 0x1A.

The control port in both I²C and SPI modes is slave only and, therefore, requires the master in the system to operate. The registers can be accessed with or without the master clock to the part. However, to operate the PLL, serial audio ports, and boost converter, the master clock is necessary.

By default, the ADAU1978 operates in I²C mode, but the part can be put into SPI mode by pulling the $\overline{\text{CLATCH}}$ pin low three times.

The control port pins are multifunctional, depending on the mode in which the part is operating. Table 11 describes the control port pin functions in both modes.

Table 11. Control Port Pin Functions

		I²C Mode		SPI Mode	
Pin No.	**Mnemonic**	**Pin Function**	**Pin Type**	**Pin Function**	**Pin Type**
17	SDA/COUT	SDA data	I/O	COUT output data	O
18	SCL/CCLK	SCL clock	I	CCLK input clock	I
19	ADDR0/$\overline{\text{CLATCH}}$	I²C Device Address Bit 0	I	$\overline{\text{CLATCH}}$ input	I
20	ADDR1/CIN	I²C Device Address Bit 1	I	CIN input data	I

I²C MODE

The ADAU1978 supports a 2-wire serial (I²C-compatible) bus protocol. Two pins, serial data (SDA) and serial clock (SCL), are used to communicate with the system I²C master controller. In I²C mode, the ADAU1978 is always a slave on the bus, meaning that it cannot initiate a data transfer. Each slave device on the I²C bus is recognized by a unique device address. The device address and R/$\overline{W}$ byte for the ADAU1978 are shown in Table 12. The address resides in the first seven bits of the I²C write. Bit 7 and Bit 6 of the I²C address for the ADAU1978 are set by the levels on the ADDR1 and ADDR0 pins. The LSB of the first I²C byte (the R/$\overline{W}$ bit) from the master identifies whether it is a read or write operation. Logic Level 1 in the LSB (Bit 0) corresponds to a read operation, and Logic Level 0 corresponds to a write operation.

Table 12. I²C First Byte Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADDR1	ADDR0	1	0	0	0	1	R/$\overline{W}$

The first seven bits of the I²C chip address for the ADAU1978 are xx10001. Bit 7 and Bit 6 of the address byte can be set using the ADDR1 and ADDR0 pins to set the chip address to the desired value.

The 7-bit I²C device address can be set to one of four of the following possible options using the ADDR1 and ADDR0 pins:

- I²C Device Address 0010001 (0x11)
- I²C Device Address 0110001 (0x31)
- I²C Device Address 1010001 (0x51)
- I²C Device Address 1110001 (0x71)

In I²C mode, both the SDA and SCL pins require that an appropriate pull-up resistor be connected to IOVDD. Ensure that the voltage on these signal lines does not exceed the voltage on the IOVDD pin. Figure 44 shows a typical connection diagram for the I²C mode.

The value of the pull-up resistor for the SDA or SCL pin can be calculated as follows.

$$Minimum\ R_{PULL\ UP} = (IOVDD - V_{IL})/I_{SINK}$$

where:
IOVDD is the I/O supply voltage, typically ranging from 1.8 V up to 3.3 V.
V_{IL} is the maximum voltage at Logic Level 0 (that is, 0.4 V, as per the I²C specifications).
I_{SINK} is the current sink capability of the I/O pin.

The SDA pin can sink 2 mA of current; therefore, the minimum value of $R_{PULL\ UP}$ for an IOVDD of 3.3 V is 1.5 kΩ.

Depending on the capacitance of the board, the speed of the bus can be restricted to meet the rise time and fall time specifications.

For fast mode with a bit rate time of around 1 Mbps, the rise time must be less than 550 ns. Use the following equation to determine whether the rise time specification can be met:

$$t = 0.8473 \times R_{PULL\ UP} \times C_{BOARD}$$

where C_{BOARD} must be less than 236 pF to meet the 300 ns rise time requirement.

For the SCL pin, the calculations depend on the current sink capability of the I²C master used in the system.

Addressing

Initially, each device on the I²C bus is in an idle state and monitors the SDA and SCL lines for a start condition and the proper address. The I²C master initiates a data transfer by establishing a start condition, defined by a high-to-low transition on SDA while SCL remains high. This indicates that an address/data stream follows. All devices on the bus respond to the start condition and acquire the next eight bits from the master (the 7-bit address plus the R/$\overline{W}$ bit) MSB first. The master sends the 7-bit device address with the R/$\overline{W}$ bit to all the slaves on the bus. The device with the matching address responds by pulling the data line (SDA) low during the ninth clock pulse. This ninth bit is known as an acknowledge bit. All other devices withdraw from the bus at this point and return to the idle condition.

The R/$\overline{W}$ bit determines the direction of the data. A Logic 0 on the LSB of the first byte means that the master is to write information to the slave, whereas a Logic 1 means that the master is to read information from the slave after writing the address and repeating the start address. A data transfer takes place until a master initiates a stop condition. A stop condition occurs when SDA transitions from low to high while SCL is held high.

Stop and start conditions can be detected at any stage during the data transfer. If these conditions are asserted out of sequence during normal read and write operations, the ADAU1978 immediately jumps to the idle condition.

Figure 33 and Figure 34 use the following abbreviations:

ACK = acknowledge

No ACK = no acknowledge

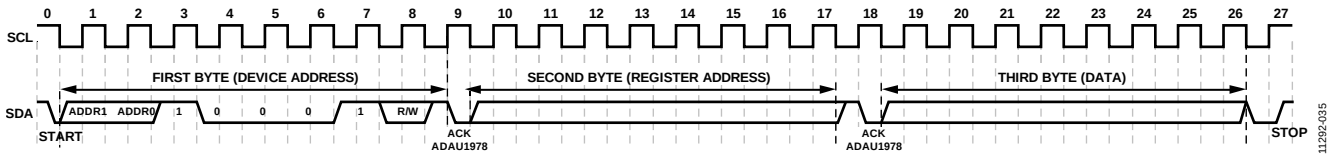


Figure 33. I²C Write to ADAU1978, Single Byte

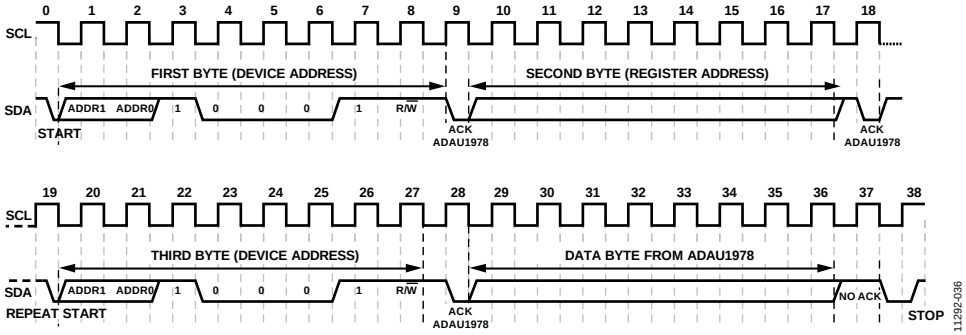


Figure 34. I²C Read from ADAU1978, Single Byte

I²C Read and Write Operations

Figure 35 shows the format of a single-word I²C write operation. Every ninth clock pulse, the ADAU1978 issues an acknowledge by pulling SDA low.

Figure 36 shows the format of a burst mode write sequence. This figure shows an example of a write to sequential single-byte registers. The ADAU1978 increments its address register after every byte because the requested address corresponds to a register or memory area with a 1-byte word length.

Figure 37 shows the format of a single-word I²C read operation. Note that the first R/$\overline{W}$ bit is 0, indicating a write operation. This is because the address still needs to be written to set up the internal address. After the ADAU1978 acknowledges the receipt of the address, the master must issue a repeated start command followed by the chip address byte with the R/$\overline{W}$ bit set to 1 (read). This causes the ADAU1978 SDA to reverse and begin driving data back to the master. The master then responds every ninth pulse with an acknowledge pulse to the ADAU1978.

Figure 38 shows the format of a burst mode read sequence. This figure shows an example of a read from sequential single-byte registers. The ADAU1978 increments its address registers after every byte because the ADAU1978 uses an 8-bit register address.

Figure 35 to Figure 38 use the following abbreviations:
S = start bit
P = stop bit
AM = acknowledge by master
AS = acknowledge by slave

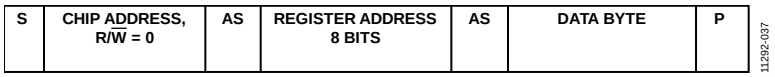


Figure 35. Single-Word I²C Write Format

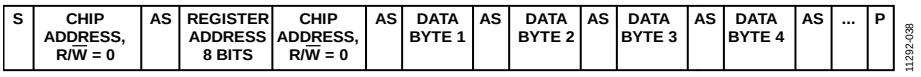


Figure 36. Burst Mode I²C Write Format

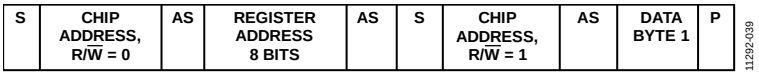


Figure 37. Single-Word I²C Read Format



Figure 38. Burst Mode I²C Read Format

SPI MODE

By default, the ADAU1978 is in I²C mode. To invoke SPI control mode, pull CLATCH low three times. This can be done by performing three dummy writes to the SPI port (the ADAU1978 does not acknowledge these three writes, see Figure 39). Beginning with the fourth SPI write, data can be written to or read from the device. The ADAU1978 can be taken out of SPI mode only by a full reset initiated by power cycling the device.

The SPI port uses a 4-wire interface, consisting of the CLATCH, CCLK, CIN, and COUT signals, and it is always a slave port. The CLATCH signal goes low at the beginning of a transaction and high at the end of a transaction. The CCLK signal latches COUT on a low-to-high transition. COUT data is shifted out of the ADAU1978 on the falling edge of CCLK and is clocked into a receiving device, such as a microcontroller, on the CCLK rising edge. The CIN signal carries the serial input data, and the COUT signal carries the serial output data. The COUT signal remains tristated until a read operation is requested. This allows direct connection to other SPI-compatible peripheral COUT ports for sharing the same system controller port. All SPI transactions have the same basic generic control word format, as shown in Table 15. A timing diagram is shown in Figure 3. Write all data MSB first.

Chip Address R/$\overline{W}$

The LSB of the first byte of an SPI transaction is a R/$\overline{W}$ bit. This bit determines whether the communication is a read (Logic Level 1) or a write (Logic Level 0). This format is shown in Table 13.

Table 13. SPI Address and R/$\overline{W}$ Byte Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	0	0	R/$\overline{W}$

Register Address

The 8-bit address word is decoded to a location in one of the registers. This address is the location of the appropriate register.

Data Bytes

The number of data bytes varies according to the register being accessed. During a burst mode write, an initial register address is written followed by a continuous sequence of data for consecutive register locations.

A sample timing diagram for a single-word SPI write operation to a register is shown in Figure 40. A sample timing diagram of a single-word SPI read operation is shown in Figure 41. The COUT pin goes from being high-Z to being driven at the beginning of Byte 3. In this example, Byte 0 to Byte 1 contain the device address, the R/$\overline{W}$ bit, and the register address to be read. Subsequent bytes carry the data from the device.

Standalone Mode

The ADAU1978 can also operate in standalone mode. However, in standalone mode, the boost converter, microphone bias, and diagnostics blocks are powered down. To set the part in standalone mode, pull the SA_MODE pin to IOVDD. In this mode, some pins change functionality to provide more flexibility (see Table 14 for more information).

Table 14. Pin Functionality in Standalone Mode

Pin Function[1]	Setting	Description
ADDR0	0	I²S SAI format
	1	TDM modes, determined by the SDATAOUT2 pin
ADDR1	0	Master mode SAI
	1	Slave mode SAI
SDA	0	MCLK = 256 × f_S, PLL on
	1	MCLK = 384 × f_S, PLL on
SCL	0	48 kHz sample rate
	1	96 kHz sample rate
SDATAOUT2	0	TDM4—LRCLK pulse
	1	TDM8—LRCLK pulse

[1] Pin functionality, not full pin names, is listed. See Table 11 for additional information.

Table 15. Generic Control Word Format

Byte 0	Byte 1	Byte 2	Byte 3[1]
Device Address[6:0], R/$\overline{W}$	Register Address[7:0]	Data[7:0]	Data[7:0]

[1] Continues to end of data.

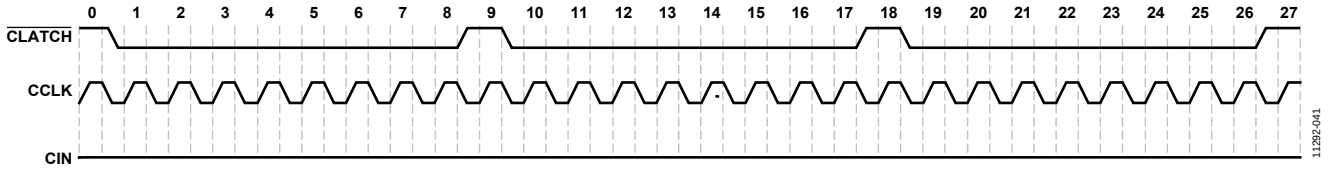


Figure 39. SPI Mode Initial Sequence

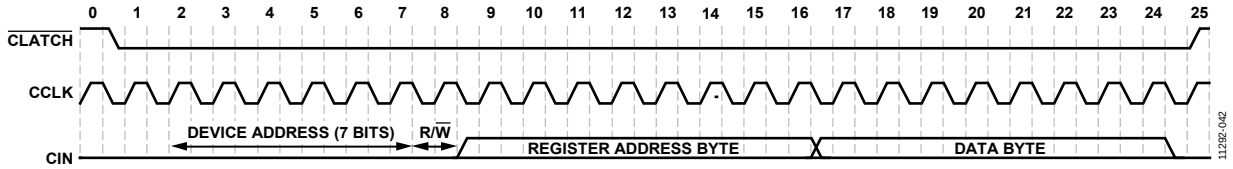


Figure 40. SPI Write to ADAU1978 Clocking (Single-Word Write Mode)

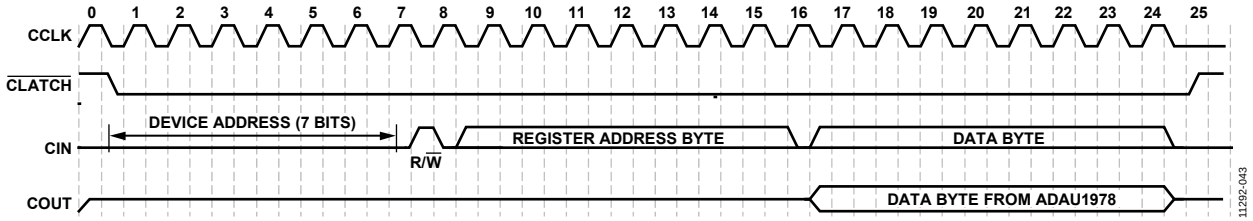


Figure 41. SPI Read from ADAU1978 Clocking (Single-Word Read Mode)

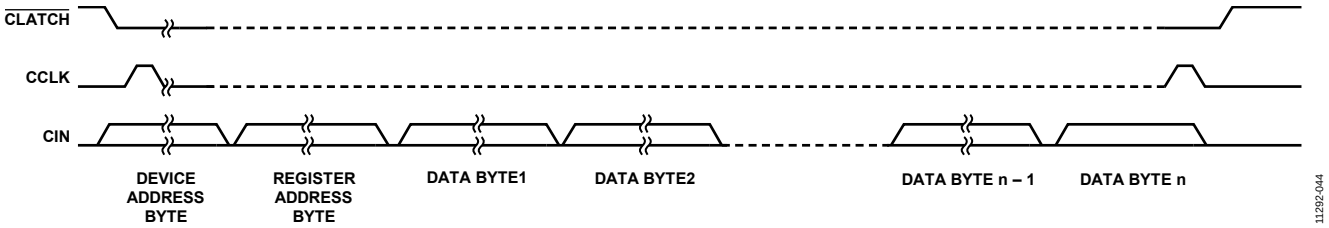


Figure 42. SPI Write to ADAU1978 (Multiple Bytes)

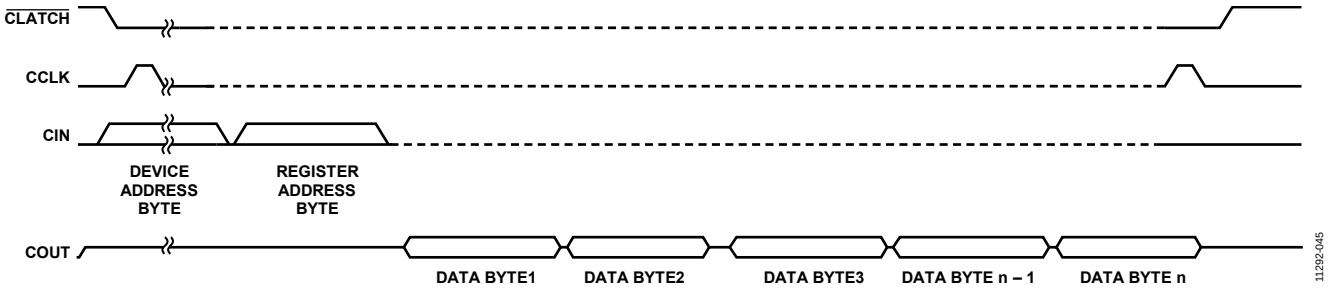


Figure 43. SPI Read from ADAU1978 (Multiple Bytes)

REGISTER SUMMARY

Table 16. REGMAP_ADAU1978 Register Summary

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x00	M_POWER	[7:0]	S_RST	RESERVED						PWUP	0x00	RW
0x01	PLL_CONTROL	[7:0]	PLL_LOCK	PLL_MUTE	RESERVED	CLK_S	RESERVED	MCS			0x41	RW
0x02	RESERVED	[7:0]	RESERVED								Reserved	Reserved
0x03	RESERVED	[7:0]	RESERVED								Reserved	Reserved
0x04	BLOCK_POWER_SAI	[7:0]	LR_POL	BCLKEDGE	LDO_EN	VREF_EN	ADC_EN4	ADC_EN3	ADC_EN2	ADC_EN1	0x3F	RW
0x05	SAI_CTRL0	[7:0]	SDATA_FMT		SAI			FS			0x02	RW
0x06	SAI_CTRL1	[7:0]	SDATA_SEL	SLOT_WIDTH		DATA_WIDTH	LR_MODE	SAI_MSB	BCLKRATE	SAI_MS	0x00	RW
0x07	SAI_CMAP12	[7:0]	CMAP_C2				CMAP_C1				0x10	RW
0x08	SAI_CMAP34	[7:0]	CMAP_C4				CMAP_C3				0x32	RW
0x09	SAI_OVERTEMP	[7:0]	SAI_DRV_C4	SAI_DRV_C3	SAI_DRV_C2	SAI_DRV_C1	DRV_HIZ	RESERVED	RESERVED	OT	0xF0	RW
0x0A	POSTADC_GAIN1	[7:0]	PADC_GAIN1								0xA0	RW
0x0B	POSTADC_GAIN2	[7:0]	PADC_GAIN2								0xA0	RW
0x0C	POSTADC_GAIN3	[7:0]	PADC_GAIN3								0xA0	RW
0x0D	POSTADC_GAIN4	[7:0]	PADC_GAIN4								0xA0	RW
0x0E	MISC_CONTROL	[7:0]	SUM_MODE		RESERVED	MMUTE	RESERVED			DC_CAL	0x02	RW
0x0F	RESERVED	[7:0]	RESERVED		RESERVED		RESERVED		RESERVED		0xFF	RW
0x10	RESERVED	[7:0]	RESERVED				RESERVED	RESERVED	RESERVED	RESERVED	0x0F	RW
0x11	RESERVED	[7:0]	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	0x00	RW
0x12	RESERVED	[7:0]	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	0x00	RW
0x13	RESERVED	[7:0]	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	0x00	RW
0x14	RESERVED	[7:0]	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	0x00	RW
0x15	RESERVED	[7:0]	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	0x20	RW
0x16	RESERVED	[7:0]	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	0x00	RW
0x17	RESERVED	[7:0]	RESERVED		RESERVED		RESERVED		RESERVED		Reserved	Reserved
0x18	RESERVED	[7:0]	RESERVED		RESERVED		RESERVED	RESERVED	RESERVED	RESERVED	Reserved	Reserved
0x19	ASDC_CLIP	[7:0]	RESERVED				ADC_CLIP4	ADC_CLIP3	ADC_CLIP2	ADC_CLIP1	0x00	RW
0x1A	DC_HPF_CAL	[7:0]	DC_SUB_C4	DC_SUB_C3	DC_SUB_C2	DC_SUB_C1	DC_HPF_C4	DC_HPF_C3	DC_HPF_C2	DC_HPF_C1	0x00	RW

REGISTER DETAILS

MASTER POWER AND SOFT RESET REGISTER

Address: 0x00, Reset: 0x00, Name: M_POWER

The power management control register is used for enabling the boost regulator, microphone bias, PLL, band gap reference, ADC, and LDO regulator.

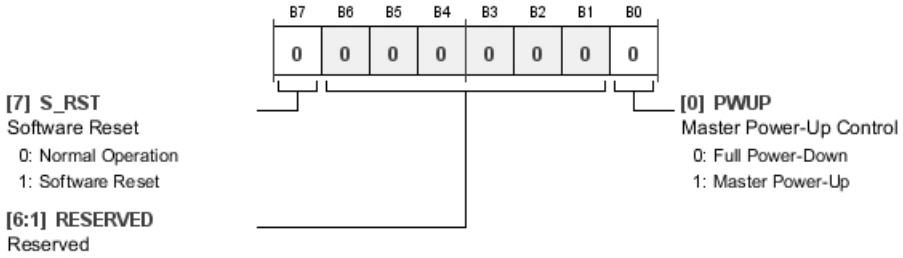


Table 17. Bit Descriptions for M_POWER

Bits	Bit Name	Settings	Description	Reset	Access
7	S_RST		Software Reset. The software reset resets all internal circuitry and all control registers to their respective default states. It is not necessary to reset the ADAU1978 during a power-up or power-down cycle.	0x0	RW
		0	Normal Operation.		
		1	Software Reset.		
[6:1]	RESERVED		Reserved.	0x00	RW
0	PWUP		Master Power-Up Control. The master power-up control fully powers up or powers down the ADAU1978. This must be set to 1 to power up the ADAU1978. Individual blocks can be powered down via their respective power control registers.	0x0	RW
		0	Full Power-Down.		
		1	Master Power-Up.		

PLL CONTROL REGISTER

Address: 0x01, Reset: 0x41, Name: PLL_CONTROL

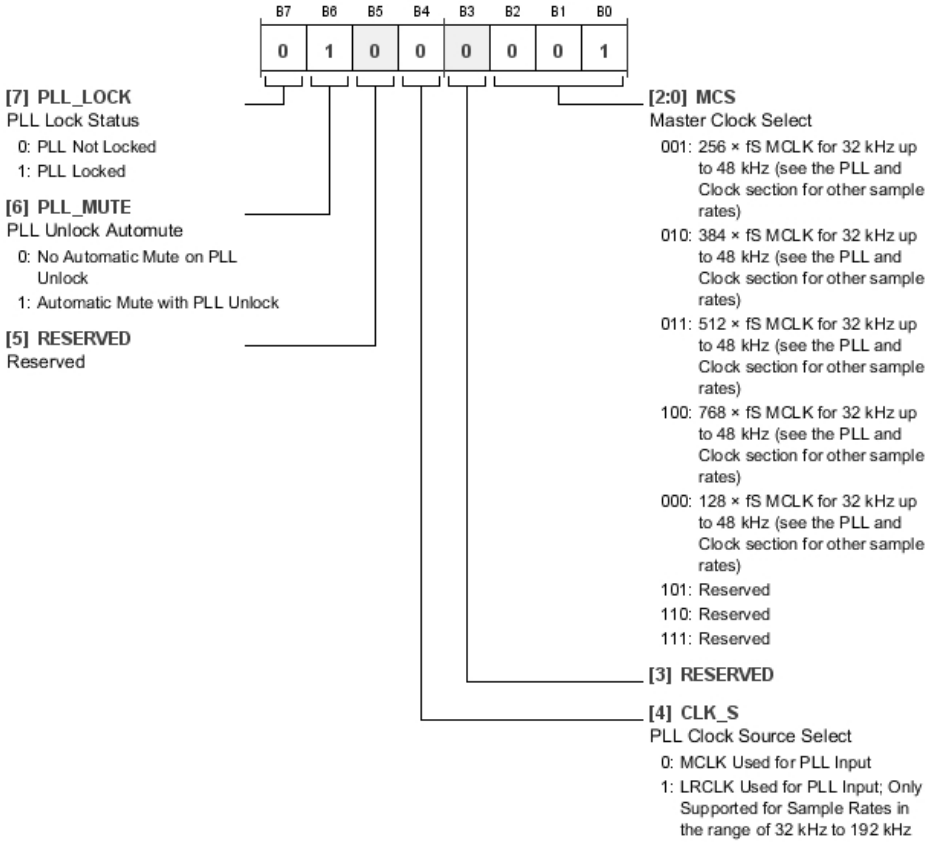


Table 18. Bit Descriptions for PLL_CONTROL

Bits	Bit Name	Settings	Description	Reset	Access
7	PLL_LOCK		PLL Lock Status. PLL lock status bit. When set to 1, the PLL is locked.	0x0	R
		0	PLL Not Locked.		
		1	PLL Locked.		
6	PLL_MUTE		PLL Unlock Automute. When set to 1, it mutes the ADC output if PLL becomes unlocked.	0x1	RW
		0	No Automatic Mute on PLL Unlock.		
		1	Automatic Mute with PLL Unlock.		
5	RESERVED		Reserved.	0x0	RW
4	CLK_S		PLL Clock Source Select. Selecting input clock source for PLL.	0x0	RW
		0	MCLK Used for PLL Input.		
		1	LRCLK Used for PLL Input; Only Supported for Sample Rates in the range of 32 kHz to 192 kHz.		
3	RESERVED		Reserved.	0x0	RW
[2:0]	MCS		Master Clock Select. MCS bits determine the frequency multiplication ratio of the PLL. It must be set based on the input MCLK frequency and sample rate.	0x1	RW
		001	256 × f_S MCLK for 32 kHz up to 48 kHz (see the PLL and Clock section for other sample rates).		
		010	384 × f_S MCLK for 32 kHz up to 48 kHz (see the PLL and Clock section for other sample rates).		
		011	512 × f_S MCLK for 32 kHz up to 48 kHz (see the PLL and Clock section for other sample rates).		
		100	768 × f_S MCLK for 32 kHz up to 48 kHz (see the PLL and Clock section for other sample rates).		
		000	128 × f_S MCLK for 32 kHz up to 48 kHz (see the PLL and Clock section for other sample rates).		
		101	Reserved.		
		110	Reserved.		
		111	Reserved.		

BLOCK POWER CONTROL AND SERIAL PORT CONTROL REGISTER

Address: 0x04, Reset: 0x3F, Name: BLOCK_POWER_SAI

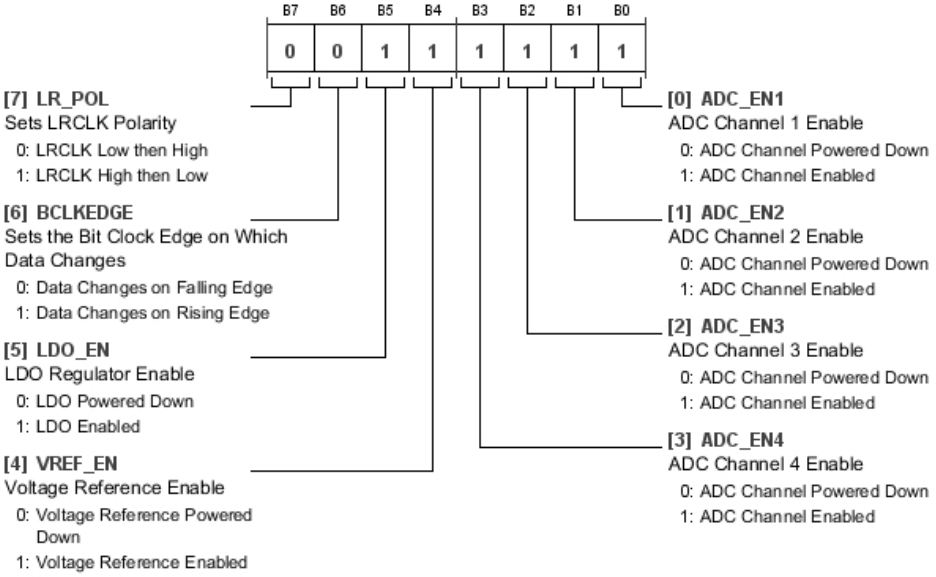


Table 19. Bit Descriptions for BLOCK_POWER_SAI

Bits	Bit Name	Settings	Description	Reset	Access
7	LR_POL		Sets LRCLK Polarity	0x0	RW
		0	LRCLK Low then High		
		1	LRCLK High then Low		
6	BCLKEDGE		Sets the Bit Clock Edge on Which Data Changes	0x0	RW
		0	Data Changes on Falling Edge		
		1	Data Changes on Rising Edge		
5	LDO_EN		LDO Regulator Enable	0x1	RW
		0	LDO Powered Down		
		1	LDO Enabled		
4	VREF_EN		Voltage Reference Enable	0x1	RW
		0	Voltage Reference Powered Down		
		1	Voltage Reference Enabled		
3	ADC_EN4		ADC Channel 4 Enable	0x1	RW
		0	ADC Channel Powered Down		
		1	ADC Channel Enabled		
2	ADC_EN3		ADC Channel 3 Enable	0x1	RW
		0	ADC Channel Powered Down		
		1	ADC Channel Enabled		
1	ADC_EN2		ADC Channel 2 Enable	0x1	RW
		0	ADC Channel Powered Down		
		1	ADC Channel Enabled		
0	ADC_EN1		ADC Channel 1 Enable	0x1	RW
		0	ADC Channel Powered Down		
		1	ADC Channel Enabled		

SERIAL PORT CONTROL REGISTER 1

Address: 0x05, Reset: 0x02, Name: SAI_CTRL0

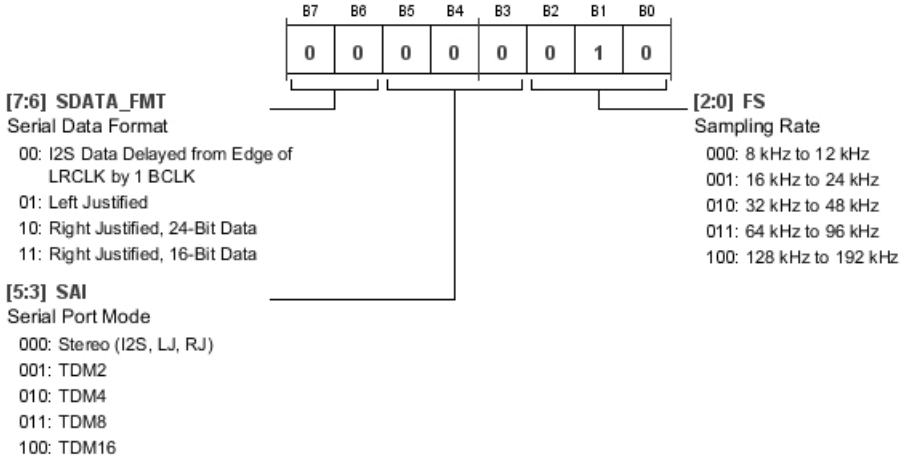


Table 20. Bit Descriptions for SAI_CTRL0

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	SDATA_FMT		Serial Data Format	0x0	RW
		00	I²S Data Delayed from Edge of LRCLK by 1 BCLK		
		01	Left Justified		
		10	Right Justified, 24-Bit Data		
		11	Right Justified, 16-Bit Data		
[5:3]	SAI		Serial Port Mode	0x0	RW
		000	Stereo (I²S, LJ, RJ)		
		001	TDM2		
		010	TDM4		
		011	TDM8		
		100	TDM16		
[2:0]	FS		Sampling Rate	0x2	RW
		000	8 kHz to 12 kHz		
		001	16 kHz to 24 kHz		
		010	32 kHz to 48 kHz		
		011	64 kHz to 96 kHz		
		100	128 kHz to 192 kHz		

SERIAL PORT CONTROL REGISTER 2

Address: 0x06, Reset: 0x00, Name: SAI_CTRL1

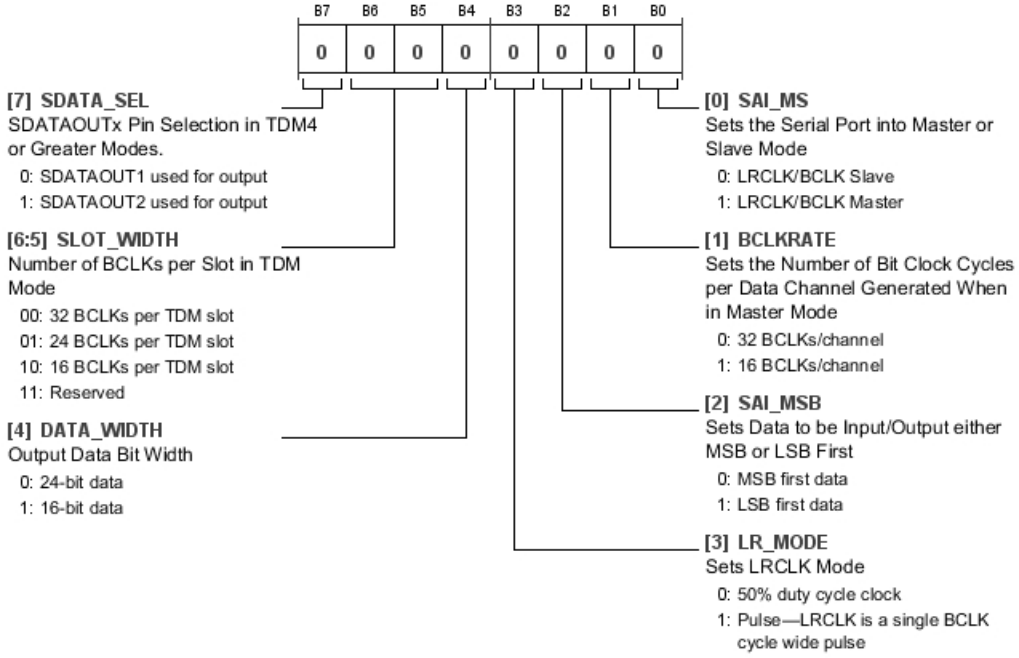


Table 21. Bit Descriptions for SAI_CTRL1

Bits	Bit Name	Settings	Description	Reset	Access
7	SDATA_SEL		SDATAOUTx Pin Selection in TDM4 or Greater Modes	0x0	RW
		0	SDATAOUT1 used for output		
		1	SDATAOUT2 used for output		
[6:5]	SLOT_WIDTH		Number of BCLKs per Slot in TDM Mode	0x0	RW
		00	32 BCLKs per TDM slot		
		01	24 BCLKs per TDM slot		
		10	16 BCLKs per TDM slot		
		11	Reserved		
4	DATA_WIDTH		Output Data Bit Width	0x0	RW
		0	24-bit data		
		1	16-bit data		
3	LR_MODE		Sets LRCLK Mode	0x0	RW
		0	50% duty cycle clock		
		1	Pulse—LRCLK is a single BCLK cycle wide pulse		
2	SAI_MSB		Sets Data to be Input/Output Either MSB or LSB First	0x0	RW
		0	MSB first data		
		1	LSB first data		
1	BCLKRATE		Sets the Number of Bit Clock Cycles per Data Channel Generated When in Master Mode	0x0	RW
		0	32 BCLKs/channel		
		1	16 BCLKs/channel		
0	SAI_MS		Sets the Serial Port into Master or Slave Mode	0x0	RW
		0	LRCLK/BCLK slave		
		1	LRCLK/BCLK master		

CHANNEL 1 AND CHANNEL 2 MAPPING FOR OUTPUT SERIAL PORTS REGISTER

Address: 0x07, Reset: 0x10, Name: SAI_CMAP12

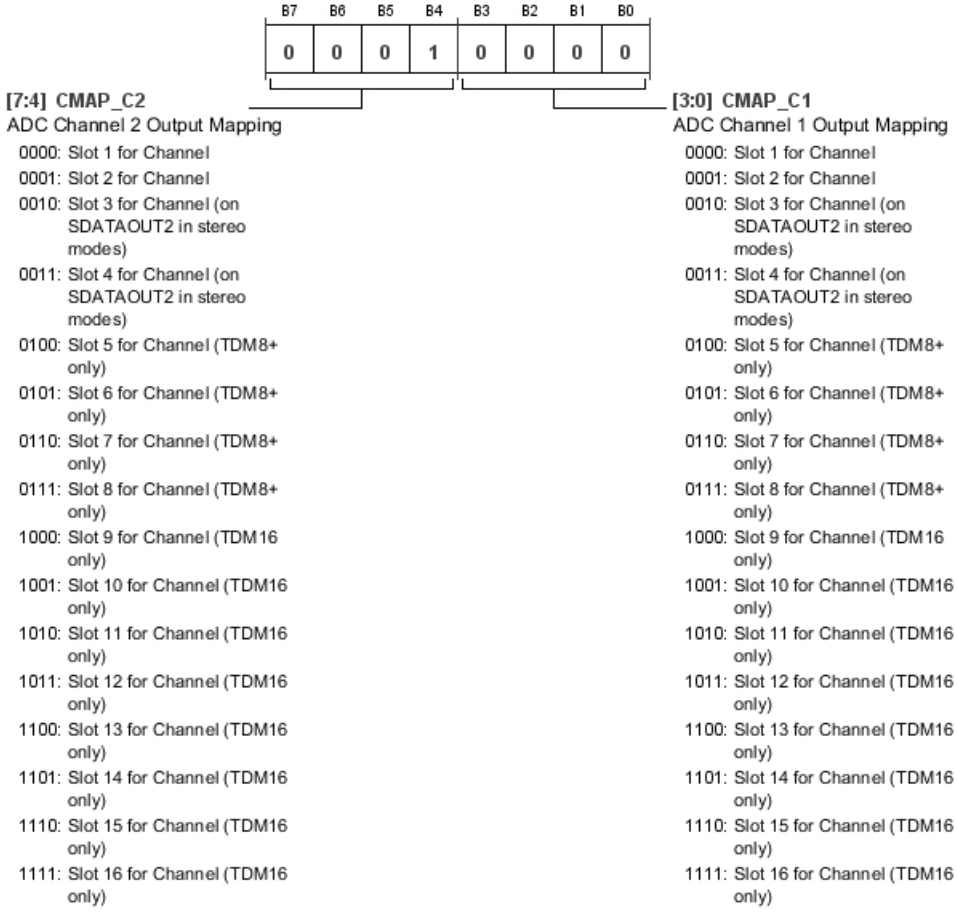


Table 22. Bit Descriptions for SAI_CMAP12

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	CMAP_C2		ADC Channel 2 Output Mapping	0x1	RW
		0000	Slot 1 for Channel		
		0001	Slot 2 for Channel		
		0010	Slot 3 for Channel (on SDATAOUT2 in stereo modes)		
		0011	Slot 4 for Channel (on SDATAOUT2 in stereo modes)		
		0100	Slot 5 for Channel (TDM8+ only)		
		0101	Slot 6 for Channel (TDM8+ only)		
		0110	Slot 7 for Channel (TDM8+ only)		
		0111	Slot 8 for Channel (TDM8+ only)		
		1000	Slot 9 for Channel (TDM16 only)		
		1001	Slot 10 for Channel (TDM16 only)		
		1010	Slot 11 for Channel (TDM16 only)		
		1011	Slot 12 for Channel (TDM16 only)		
		1100	Slot 13 for Channel (TDM16 only)		
		1101	Slot 14 for Channel (TDM16 only)		
		1110	Slot 15 for Channel (TDM16 only)		
		1111	Slot 16 for Channel (TDM16 only)		

Bits	Bit Name	Settings	Description	Reset	Access
[3:0]	CMAP_C1		ADC Channel 1 Output Mapping. If CMAP is set to a slot that does not exist for a given serial mode, that channel is not driven. For example, if CMAP is set to Slot 9 and the serial format is I²S, that channel is not driven. If more than one channel is set to the same slot, only the lowest channel number is driven; other channels are not driven.	0x0	RW
		0000	Slot 1 for Channel		
		0001	Slot 2 for Channel		
		0010	Slot 3 for Channel (on SDATAOUT2 in stereo modes)		
		0011	Slot 4 for Channel (on SDATAOUT2 in stereo modes)		
		0100	Slot 5 for Channel (TDM8+ only)		
		0101	Slot 6 for Channel (TDM8+ only)		
		0110	Slot 7 for Channel (TDM8+ only)		
		0111	Slot 8 for Channel (TDM8+ only)		
		1000	Slot 9 for Channel (TDM16 only)		
		1001	Slot 10 for Channel (TDM16 only)		
		1010	Slot 11 for Channel (TDM16 only)		
		1011	Slot 12 for Channel (TDM16 only)		
		1100	Slot 13 for Channel (TDM16 only)		
		1101	Slot 14 for Channel (TDM16 only)		
		1110	Slot 15 for Channel (TDM16 only)		
		1111	Slot 16 for Channel (TDM16 only)		

CHANNEL 3 AND CHANNEL 4 MAPPING FOR OUTPUT SERIAL PORTS REGISTER

Address: 0x08, Reset: 0x32, Name: SAI_CMAP34

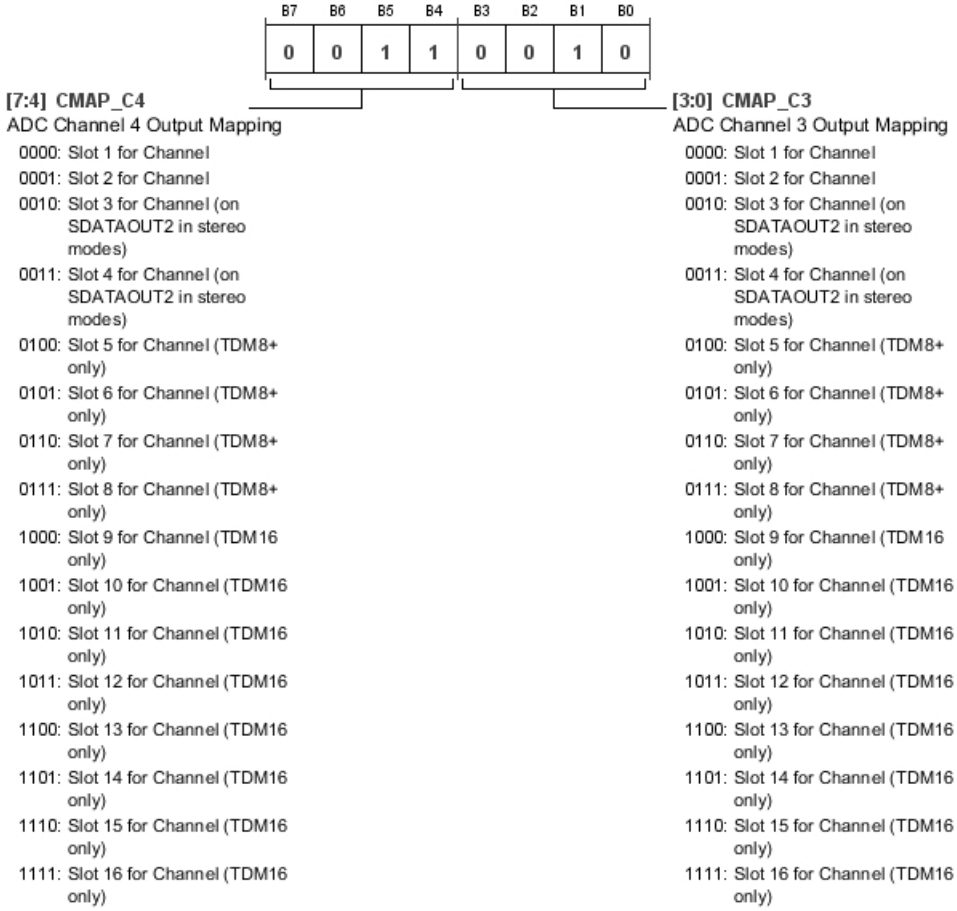


Table 23. Bit Descriptions for SAI_CMAP34

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	CMAP_C4		ADC Channel 4 Output Mapping	0x3	RW
		0000	Slot 1 for Channel		
		0001	Slot 2 for Channel		
		0010	Slot 3 for Channel (on SDATAOUT2 in stereo modes)		
		0011	Slot 4 for Channel (on SDATAOUT2 in stereo modes)		
		0100	Slot 5 for Channel (TDM8+ only)		
		0101	Slot 6 for Channel (TDM8+ only)		
		0110	Slot 7 for Channel (TDM8+ only)		
		0111	Slot 8 for Channel (TDM8+ only)		
		1000	Slot 9 for Channel (TDM16 only)		
		1001	Slot 10 for Channel (TDM16 only)		
		1010	Slot 11 for Channel (TDM16 only)		
		1011	Slot 12 for Channel (TDM16 only)		
		1100	Slot 13 for Channel (TDM16 only)		
		1101	Slot 14 for Channel (TDM16 only)		
		1110	Slot 15 for Channel (TDM16 only)		
		1111	Slot 16 for Channel (TDM16 only)		

Bits	Bit Name	Settings	Description	Reset	Access
[3:0]	CMAP_C3		ADC Channel 3 Output Mapping	0x2	RW
		0000	Slot 1 for Channel		
		0001	Slot 2 for Channel		
		0010	Slot 3 for Channel (on SDATAOUT2 in stereo modes)		
		0011	Slot 4 for Channel (on SDATAOUT2 in stereo modes)		
		0100	Slot 5 for Channel (TDM8+ only)		
		0101	Slot 6 for Channel (TDM8+ only)		
		0110	Slot 7 for Channel (TDM8+ only)		
		0111	Slot 8 for Channel (TDM8+ only)		
		1000	Slot 9 for Channel (TDM16 only)		
		1001	Slot 10 for Channel (TDM16 only)		
		1010	Slot 11 for Channel (TDM16 only)		
		1011	Slot 12 for Channel (TDM16 only)		
		1100	Slot 13 for Channel (TDM16 only)		
		1101	Slot 14 for Channel (TDM16 only)		
		1110	Slot 15 for Channel (TDM16 only)		
		1111	Slot 16 for Channel (TDM16 only)		

SERIAL OUTPUT DRIVE CONTROL AND OVERTEMPERATURE PROTECTION STATUS REGISTER

Address: 0x09, Reset: 0xF0, Name: SAI_OVERTEMP

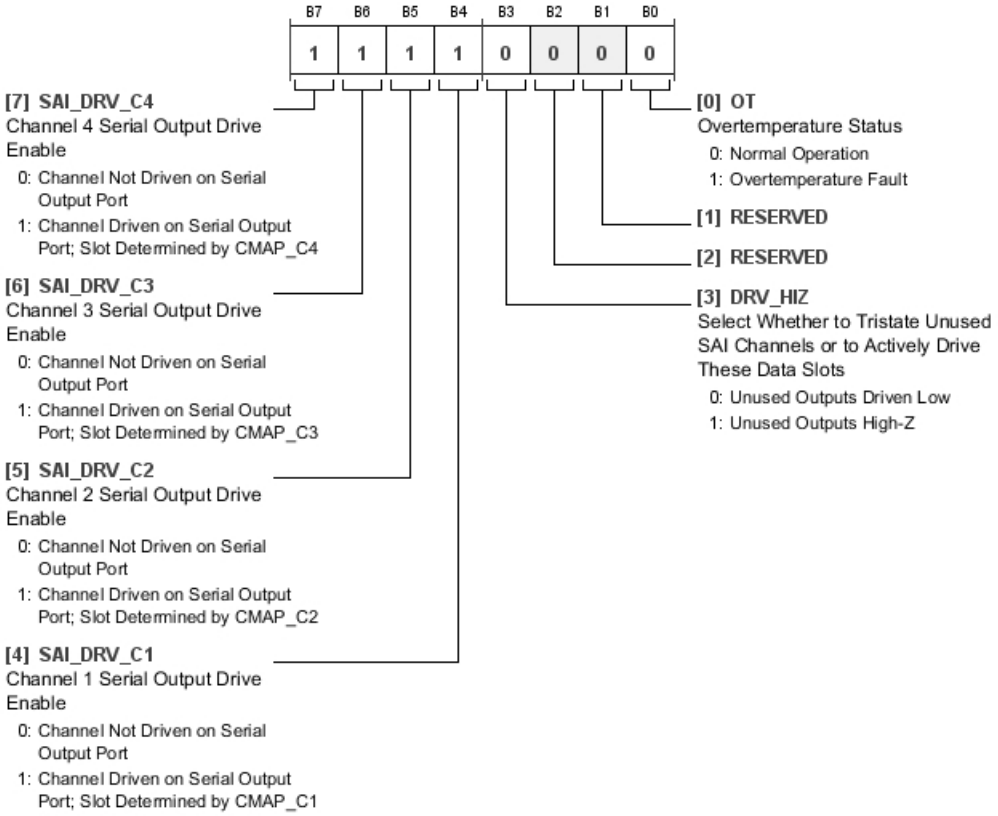


Table 24. Bit Descriptions for SAI_OVERTEMP

Bits	Bit Name	Settings	Description	Reset	Access
7	SAI_DRV_C4		Channel 4 Serial Output Drive Enable.	0x1	RW
		0	Channel Not Driven on Serial Output Port.		
		1	Channel Driven on Serial Output Port. Slot determined by CMAP_4.		

Bits	Bit Name	Settings	Description	Reset	Access
6	SAI_DRV_C3		Channel 3 Serial Output Drive Enable.	0x1	RW
		0	Channel Not Driven on Serial Output Port.		
		1	Channel Driven on Serial Output Port. Slot determined by CMAP_3.		
5	SAI_DRV_C2		Channel 2 Serial Output Drive Enable.	0x1	RW
		0	Channel Not Driven on Serial Output Port.		
		1	Channel Driven on Serial Output Port. Slot determined by CMAP_2.		
4	SAI_DRV_C1		Channel 1 Serial Output Drive Enable.	0x1	RW
		0	Channel Not Driven on Serial Output Port.		
		1	Channel Driven on Serial Output Port. Slot determined by CMAP_1.		
3	DRV_HIZ		Select whether to tristate unused SAI channels or actively drive these data slots.	0x0	RW
		0	Unused outputs driven low.		
		1	Unused outputs High-Z.		
[2:1]	RESERVED		Reserved	0x0	R
0	OT		Overtemperature Status.	0x0	R
		0	Normal Operation.		
		1	Overtemperature Fault.		

POST ADC GAIN CHANNEL 1 CONTROL REGISTER

Address: 0x0A, Reset: 0xA0, Name: POSTADC_GAIN1

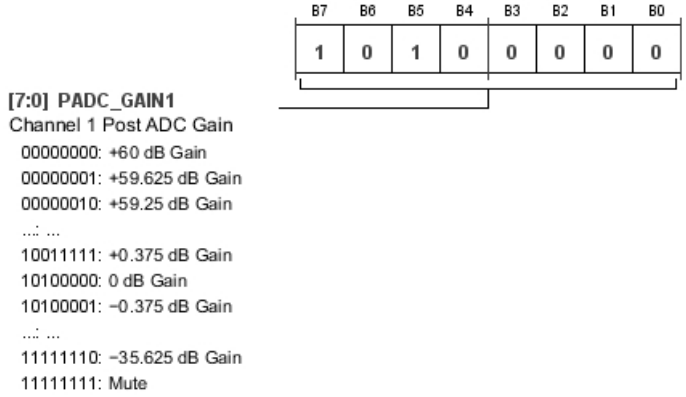


Table 25. Bit Descriptions for POSTADC_GAIN1

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	PADC_GAIN1		Channel 1 Post ADC Gain	0xA0	RW
		00000000	+60 dB Gain		
		00000001	+59.625 dB Gain		
		00000010	+59.25 dB Gain		
		...	...		
		10011111	+0.375 dB Gain		
		10100000	0 dB Gain		
		10100001	−0.375 dB Gain		
		...	...		
		11111110	−35.625 dB Gain		
		11111111	Mute		

POST ADC GAIN CHANNEL 2 CONTROL REGISTER

Address: 0x0B, Reset: 0xA0, Name: POSTADC_GAIN2

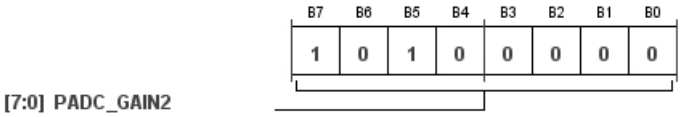


Table 26. Bit Descriptions for POSTADC_GAIN2

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	PADC_GAIN2		Channel 2 Post ADC Gain	0xA0	RW
		00000000	+60 dB Gain		
		00000001	+59.625 dB Gain		
		00000010	+59.25 dB Gain		
		...	...		
		10011111	+0.375 dB Gain		
		10100000	0 dB Gain		
		10100001	−0.375 dB Gain		
		...	...		
		11111110	−35.625 dB Gain		
		11111111	Mute		

POST ADC GAIN CHANNEL 3 CONTROL REGISTER

Address: 0x0C, Reset: 0xA0, Name: POSTADC_GAIN3

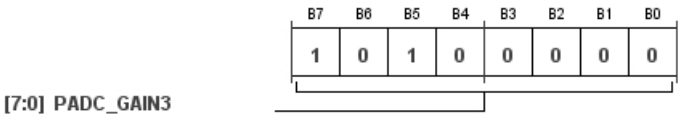


Table 27. Bit Descriptions for POSTADC_GAIN3

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	PADC_GAIN3		Channel 3 Post ADC Gain	0xA0	RW
		00000000	+60 dB Gain		
		00000001	+59.625 dB Gain		
		00000010	+59.25 dB Gain		
		...	...		
		10011111	+0.375 dB Gain		
		10100000	0 dB Gain		
		10100001	−0.375 dB Gain		
		...	...		
		11111110	−35.625 dB Gain		
		11111111	Mute		

POST ADC GAIN CHANNEL 4 CONTROL REGISTER

Address: 0x0D, Reset: 0xA0, Name: POSTADC_GAIN4

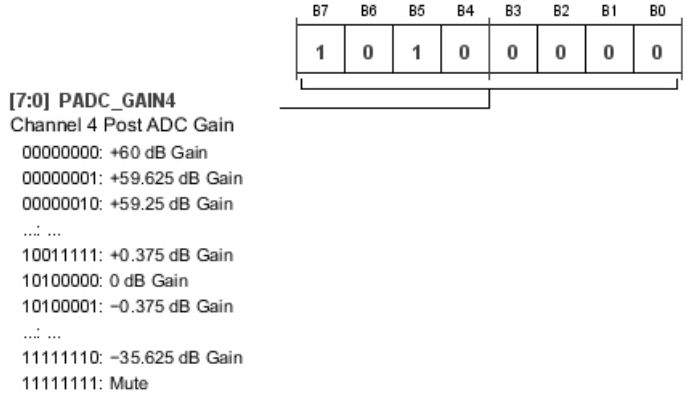


Table 28. Bit Descriptions for POSTADC_GAIN4

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	PADC_GAIN4		Channel 4 Post ADC Gain	0xA0	RW
		00000000	+60 dB Gain		
		00000001	+59.625 dB Gain		
		00000010	+59.25 dB Gain		
		...	...		
		10011111	+0.375 dB Gain		
		10100000	0 dB Gain		
		10100001	−0.375 dB Gain		
		...	...		
		11111110	−35.625 dB Gain		
		11111111	Mute		

HIGH-PASS FILTER AND DC OFFSET CONTROL REGISTER AND MASTER MUTE REGISTER

Address: 0x0E, Reset: 0x02, Name: MISC_CONTROL

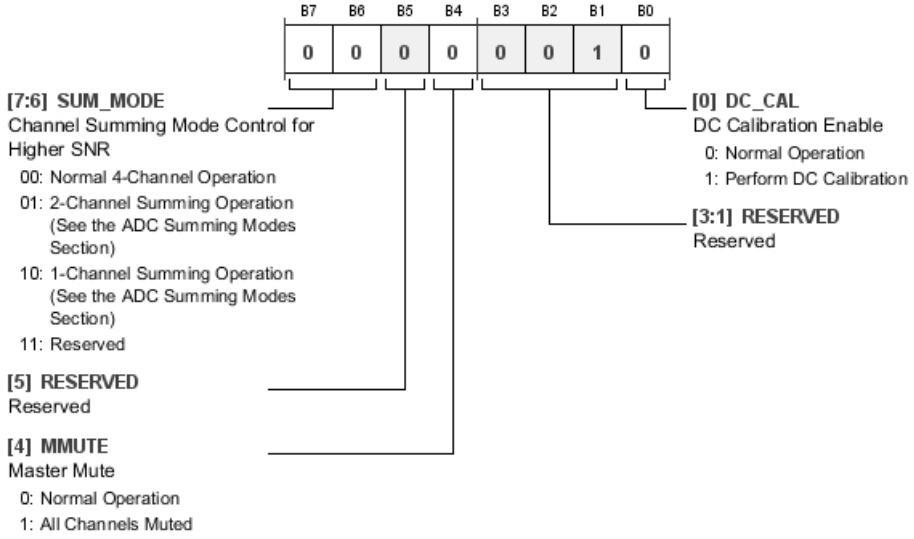


Table 29. Bit Descriptions for MISC_CONTROL

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	SUM_MODE		Channel Summing Mode Control for Higher SNR	0x0	RW
		00	Normal 4-Channel Operation		
		01	2-Channel Summing Operation (See the ADC Summing Modes Section)		
		10	1-Channel Summing Operation (See the ADC Summing Modes Section)		
		11	Reserved		
5	RESERVED		Reserved	0x0	RW
4	MMUTE		Master Mute	0x0	RW
		0	Normal Operation		
		1	All Channels Muted		
[3:1]	RESERVED		Reserved	0x0	RW
0	DC_CAL		DC Calibration Enable	0x0	RW
		0	Normal Operation		
		1	Perform DC Calibration		

ADC CLIPPING STATUS REGISTER

Address: 0x19, Reset: 0x00, Name: ASDC_CLIP

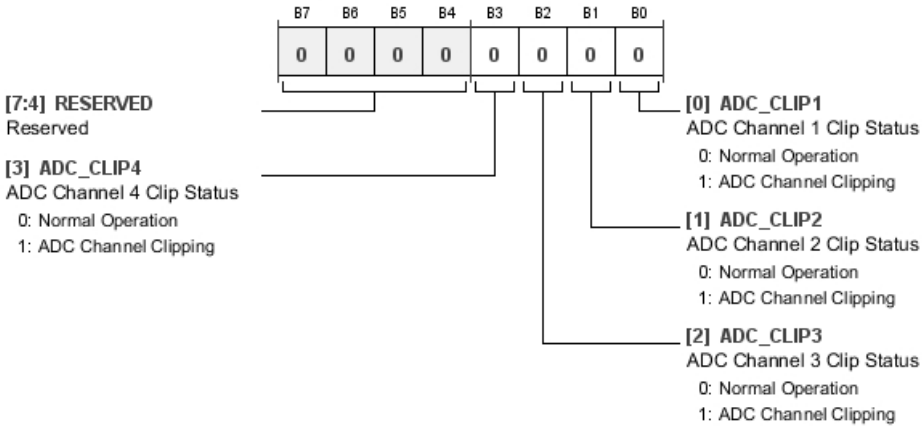


Table 30. Bit Descriptions for ASDC_CLIP

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	RESERVED		Reserved	0x0	RW
3	ADC_CLIP4		ADC Channel 4 Clip Status	0x0	R
		0	Normal Operation		
		1	ADC Channel Clipping		
2	ADC_CLIP3		ADC Channel 3 Clip Status	0x0	R
		0	Normal Operation		
		1	ADC Channel Clipping		
1	ADC_CLIP2		ADC Channel 2 Clip Status	0x0	R
		0	Normal Operation		
		1	ADC Channel Clipping		
0	ADC_CLIP1		ADC Channel 1 Clip Status	0x0	R
		0	Normal Operation		
		1	ADC Channel Clipping		

DIGITAL DC HIGH-PASS FILTER AND CALIBRATION REGISTER

Address: 0x1A, Reset: 0x00, Name: DC_HPF_CAL

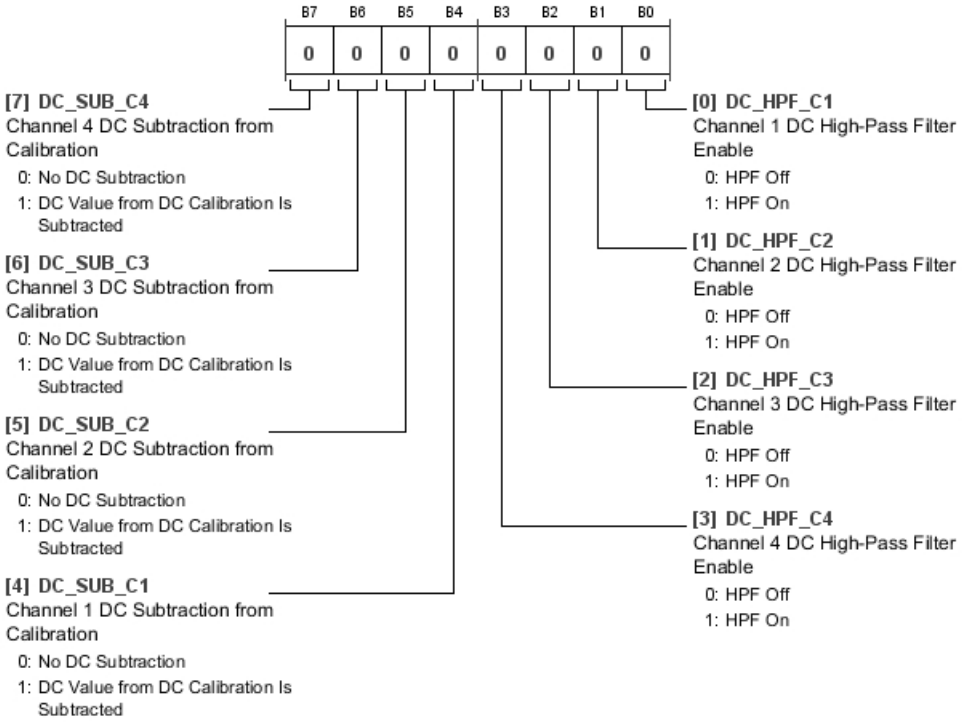


Table 31. Bit Descriptions for DC_HPF_CAL

Bits	Bit Name	Settings	Description	Reset	Access
7	DC_SUB_C4		Channel 4 DC Subtraction from Calibration	0x0	RW
		0	No DC Subtraction		
		1	DC Value from DC Calibration Is Subtracted		
6	DC_SUB_C3		Channel 3 DC Subtraction from Calibration	0x0	RW
		0	No DC Subtraction		
		1	DC Value from DC Calibration Is Subtracted		
5	DC_SUB_C2		Channel 2 DC Subtraction from Calibration	0x0	RW
		0	No DC Subtraction		
		1	DC Value from DC Calibration Is Subtracted		
4	DC_SUB_C1		Channel 1 DC Subtraction from Calibration	0x0	RW
		0	No DC Subtraction		
		1	DC Value from DC Calibration Is Subtracted		
3	DC_HPF_C4		Channel 4 DC High-Pass Filter Enable	0x0	RW
		0	HPF Off		
		1	HPF On		
2	DC_HPF_C3		Channel 3 DC High-Pass Filter Enable	0x0	RW
		0	HPF Off		
		1	HPF On		
1	DC_HPF_C2		Channel 2 DC High-Pass Filter Enable	0x0	RW
		0	HPF Off		
		1	HPF On		
0	DC_HPF_C1		Channel 1 DC High-Pass Filter Enable	0x0	RW
		0	HPF Off		
		1	HPF On		

TYPICAL APPLICATION CIRCUIT

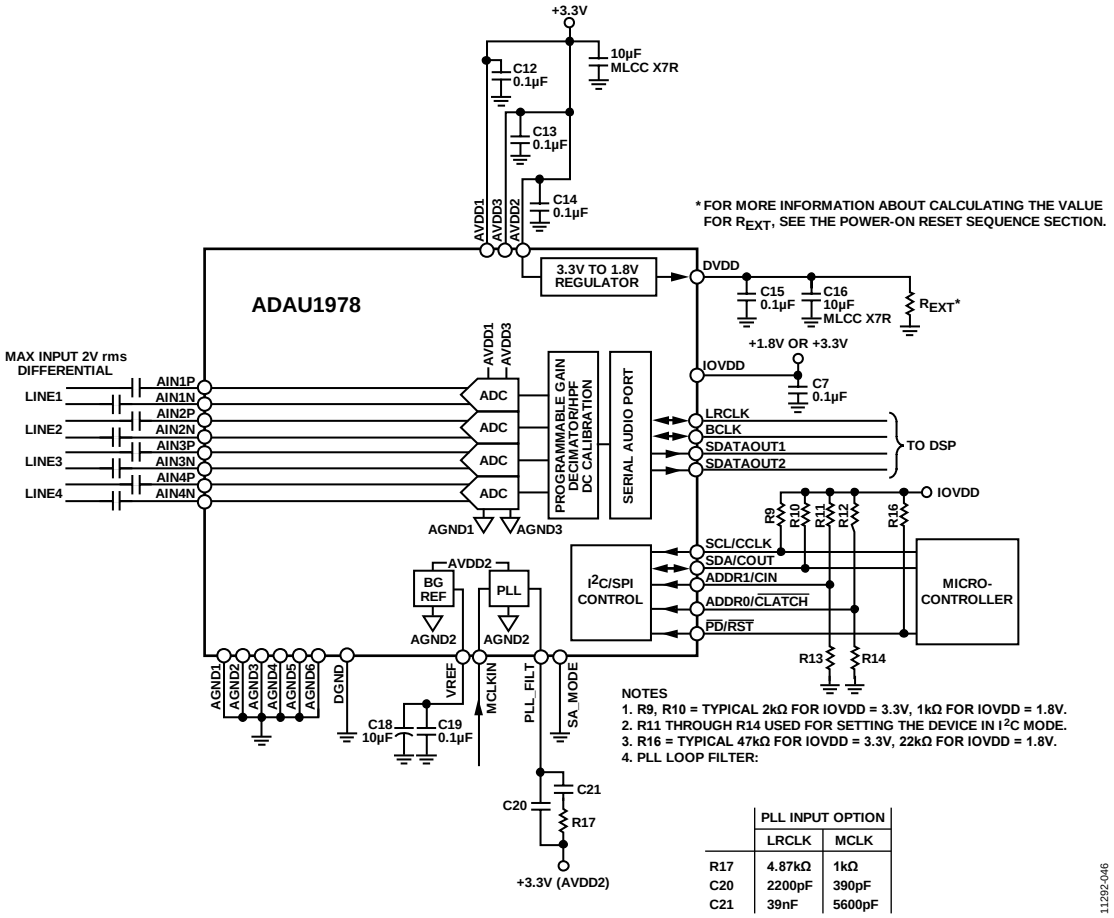


Figure 44. Typical Application Circuit, Four Inputs, I²C and I²S Mode

OUTLINE DIMENSIONS

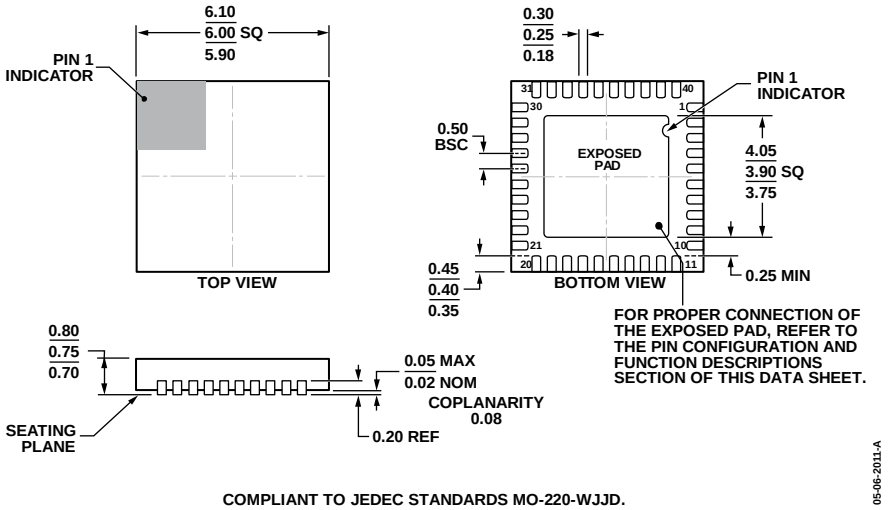


Figure 45. 40-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
6 mm × 6 mm Body, Very Very Thin Quad
(CP-40-14)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2]	Temperature Range	Package Description	Package Option
ADAU1978WBCPZ	−40°C to +105°C	40-Lead LFCSP_WQ	CP-40-14
ADAU1978WBCPZ-RL	−40°C to +105°C	40-Lead LFCSP, 13″Tape and Reel	CP-40-14
EVAL-ADAU1978Z		Evaluation Board	

[1] Z = RoHS Compliant Part.
[2] W = Qualified for Automotive Applications.

AUTOMOTIVE PRODUCTS

The ADAU1978WBCPZ models are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models; therefore, designers should review the Specifications section of this data sheet carefully. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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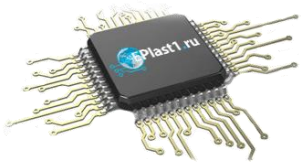
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- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
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- Техническая поддержка проекта;
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Телефон: 8 (812) 309 58 32 (многоканальный)
Факс: 8 (812) 320-02-42
Электронная почта: org@eplast1.ru
Адрес: 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.