



### FEATURES

- Triaxial, digital gyroscope,  $\pm 450^\circ/\text{sec}$  dynamic range
  - $\pm 0.018^\circ$  axis-to-axis misalignment error
  - 5.3°/hr in-run bias stability
  - 0.25°/√hr angular random walk
  - 0.045°/sec nonlinearity
- Triaxial, digital accelerometer,  $\pm 18\text{ g}$  dynamic range
- Barometer, 300 mbar to 1100 mbar
- Triaxial, delta angle and delta velocity outputs
- Factory calibrated sensitivity, bias, and axial alignment
  - Calibration temperature range:  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$
- SPI compatible
- Programmable operation and control
  - Automatic and manual bias correction controls
  - 4 FIR filter banks, 120 configurable taps
  - Digital I/O: data ready alarm indicator, external clock
  - Alarms for condition monitoring
  - Power-down/sleep mode for power management
  - Optional input sync clock: up to 2.4 kHz
  - On demand self test of inertial sensors
  - On demand flash memory test (checksum)
- Single-supply operation: 3.0 V to 3.6 V
- 2000 g shock survivability
- Parylene coating (moisture barrier for internal circuitry)
- Operating temperature range:  $-40^\circ\text{C}$  to  $+105^\circ\text{C}$

### APPLICATIONS

- Platform stabilization and control
- Navigation
- Personnel tracking
- Instrumentation
- Robotics

### GENERAL DESCRIPTION

The [ADIS16489](#) is a complete inertial system that includes a triaxis gyroscope, a triaxis accelerometer, and a barometer. Each inertial sensor in the [ADIS16489](#) combines industry leading *iMEMS*® technology with signal conditioning that optimizes dynamic performance. The factory calibration characterizes each sensor for sensitivity, bias, alignment, and linear acceleration (gyroscope bias). As a result, each sensor has its own dynamic compensation formulas that provide accurate sensor measurements.

The [ADIS16489](#) provides a simple, cost effective method for integrating accurate, multi-axis inertial sensing into industrial systems, especially when compared with the complexity and investment associated with discrete designs. All necessary motion testing and calibration are part of the production process at the factory, greatly reducing system integration time. Tight orthogonal alignment simplifies inertial frame alignment in navigation systems. The serial peripheral interface (SPI) and register structure provide a simple interface for data collection and configuration control. Parylene coating of all internal circuitry (except the barometer) provides a protective barrier against moisture exposure.

The [ADIS16489](#) uses the same footprint and connector system as the [ADIS16375](#), [ADIS16480](#), [ADIS16485](#), and [ADIS16488A](#), which greatly simplifies the upgrade process. The [ADIS16489](#) is packaged in a module that is approximately 44 mm × 47 mm × 14 mm and includes a standard connector interface.

### FUNCTIONAL BLOCK DIAGRAM

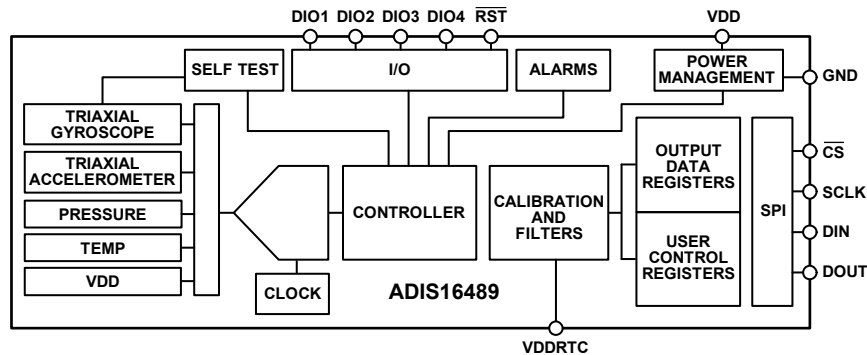


Figure 1.

**TABLE OF CONTENTS**

|  |    |   |    |
|--|----|---|----|
| Features .....                                   | 1  | Scratch Registers (USER_SCR_x) .....  | 25 |
| Applications .....                               | 1  | Flash Memory Endurance Counter (FLSHCNT_LOW,<br>FLSHCNT_HIGH).....            | 26 |
| General Description .....                        | 1  | Page 3 (PAGE_ID).....   | 26 |
| Functional block Diagram.....                    | 1  | Global Commands (GLOB_CMD).....   | 26 |
| Revision History .....                           | 2  | Auxiliary I/O Line Configuration (FNCTIO_CTRL) .....                          | 27 |
| Specifications.....                              | 3  | General-Purpose I/O Control (GPIO_CTRL) .....                                 | 28 |
| Timing Specifications .....                      | 5  | Miscellaneous Configuration (CONFIG) .....                                    | 28 |
| Absolute Maximum Ratings.....                    | 7  | Decimation Filter (DEC_RATE).....   | 29 |
| Thermal Resistance .....                         | 7  | Continuous Bias Estimation (NULL_CNFG) .....                                  | 29 |
| ESD Caution.....                                 | 7  | Power Management (SLP_CNT).....   | 30 |
| Pin Configuration and Function Descriptions..... | 8  | FIR Filter Control (FILTR_BNK_0, FILTR_BNK_1).....                            | 30 |
| Typical Performance Characteristics .....        | 9  | Alarm Configuration (ALM_CNFG_0, ALM_CNFG_1,<br>ALM_CFG_2).....               | 30 |
| Theory of Operation .....                        | 10 | X-Axis Gyroscope Alarm (XG_ALM_MAGN) .....                                    | 32 |
| Introduction .....                               | 10 | Y-Axis Gyroscope Alarm (YG_ALM_MAGN).....                                     | 32 |
| Register Structure .....                         | 10 | Z-Axis Gyroscope Alarm (ZG_ALM_MAGN) .....                                    | 32 |
| SPI Communication.....                           | 11 | X-Axis Accelerometer Alarm (XA_ALM_MAGN) .....                                | 32 |
| Device Configuration .....                       | 11 | Y-Axis Accelerometer Alarm (YA_ALM_MAGN) .....                                | 32 |
| Reading Sensor Data .....                        | 11 | Z-Axis Accelerometer Alarm (ZA_ALM_MAGN).....                                 | 33 |
| User Register Memory Map .....                   | 12 | Barometer Alarm (BR_ALM_MAGN) .....   | 33 |
| User Register Definitions.....                   | 15 | Firmware Revision (FIRM_REV) .....  | 33 |
| Page 0 (PAGE_ID).....                            | 15 | Firmware Revision Day and Month (FIRM_DM) .....                               | 33 |
| Sample Sequence Counter (SEQ_CNT).....           | 15 | Firmware Revision Year (FIRM_Y) .....   | 33 |
| Status/Error Flag Indicators (SYS_E_FLAG).....   | 15 | Page 4 (PAGE_ID).....   | 33 |
| Self Test Error Flags (DIAG_STS).....            | 15 | Part Identification Numbers (PART_ID1, PART_ID2,<br>PART_ID3, PART_ID4) ..... | 34 |
| Alarm Error Flags (ALM_STS) .....                | 16 | FIR Filters .....   | 34 |
| Internal Temperature (TEMP_OUT) .....            | 16 | Applications Information .....  | 37 |
| Gyroscope Data .....                             | 16 | Mounting Best Practices.....  | 37 |
| Acceleration Data .....                          | 17 | Evaluation Tools .....  | 38 |
| Barometer Data.....                              | 18 | Power Supply Considerations.....  | 38 |
| Delta Angles .....                               | 19 | X-Ray Sensitivity .....   | 38 |
| Delta Velocity.....                              | 20 | Packaging and Ordering Information .....                                      | 39 |
| Real-Time Clock.....                             | 21 | Outline Dimensions .....  | 39 |
| Page 2 (PAGE_ID).....                            | 22 | Ordering Guide .....  | 39 |
| Calibration.....                                 | 22 |   |    |
| Barometers.....                                  | 25 |   |    |

**REVISION HISTORY**

**11/2018—Rev. 0 to Rev. A**

|   |    |
|---|----|
| Added Endnote 4, Table 1; Renumbered Sequentially ..... | 4  |
| Added X-Ray Sensitivity Section.....                    | 39 |

**2/2017—Revision 0: Initial Version**

## SPECIFICATIONS

$T_C = 25^\circ\text{C}$ ,  $V_{DD} = 3.3\text{ V}$ , angular rate =  $0^\circ/\text{sec}$ , dynamic range =  $\pm 450^\circ/\text{sec} \pm 1\text{ g}$ , unless otherwise noted.

Table 1.

| Parameter                           | Test Conditions/Comments   | Min       | Typ                    | Max       | Unit                                     |
|-------------------------------------|--|-----------|------------------------|-----------|--|
| <b>GYROSCOPES</b>                   |  |           |                        |           |  |
| Dynamic Range                       |  | $\pm 450$ |                        | $\pm 480$ | $^\circ/\text{sec}$                      |
| Sensitivity                         | $x\_GYRO\_OUT$ and $x\_GYRO\_LOW$ (32-bit)                                     |           | $3.052 \times 10^{-7}$ |           | $^\circ/\text{sec}/\text{LSB}$           |
| Repeatability <sup>1</sup>          | $-40^\circ\text{C} \leq T_C \leq +85^\circ\text{C}$                            |           |                        | $\pm 1$   | %  |
| Sensitivity Temperature Coefficient | $-40^\circ\text{C} \leq T_C \leq +85^\circ\text{C}$ , $1\sigma$                |           | $\pm 25$               |           | $\text{ppm}/^\circ\text{C}$              |
| Misalignment Error                  | Axis to axis   |           | $\pm 0.018$            |           | Degrees                                  |
|                                     | Axis to frame (package)  |           | $\pm 1.0$              |           | Degrees                                  |
| Nonlinearity                        | Best fit straight line, full scale (FS) = $450^\circ/\text{sec}$               |           | 0.045                  |           | $^\circ/\text{sec}$                      |
| <b>Bias</b>                         |  |           |                        |           |  |
| Repeatability <sup>1,2</sup>        | $-40^\circ\text{C} \leq T_C \leq +85^\circ\text{C}$ , $1\sigma$                |           | $\pm 0.2$              |           | $^\circ/\text{sec}$                      |
| In-Run Bias Stability               | $1\sigma$  |           | 5.3                    |           | $^\circ/\text{hr}$                       |
| Angular Random Walk                 | $1\sigma$  |           | 0.25                   |           | $^\circ/\sqrt{\text{hr}}$                |
| Temperature Coefficient             | $-40^\circ\text{C} \leq T_C \leq +85^\circ\text{C}$ , $1\sigma$                |           | $\pm 0.0025$           |           | $^\circ/\text{sec}/^\circ\text{C}$       |
| Error over Temperature              | $-15^\circ\text{C} \leq T_C \leq +65^\circ\text{C}$ , $10^\circ\text{C}$ range |           | $\pm 0.0611$           |           | $^\circ/\text{sec}$                      |
| Linear Acceleration Effect          | Any axis, $1\sigma$ (CONFIG[7] = 1)  |           | 0.009                  |           | $^\circ/\text{sec}/\text{g}$             |
|                                     | Any axis, $1\sigma$ (CONFIG[7] = 0)  |           | 0.015                  |           | $^\circ/\text{sec}/\text{g}$             |
| <b>Noise</b>                        |  |           |                        |           |  |
| Output Noise                        | No filtering   |           | 0.16                   |           | $^\circ/\text{sec}$ rms                  |
| Rate Noise Density                  | $f = 10\text{ Hz}$ to $40\text{ Hz}$ , no filtering                            |           | 0.0068                 |           | $^\circ/\text{sec}/\sqrt{\text{Hz}}$ rms |
| 3 dB Bandwidth                      |  |           | 330                    |           | Hz                                       |
| Sensor Resonant Frequency           |  |           | 18                     |           | kHz                                      |
| <b>ACCELEROMETERS<sup>3</sup></b>   |  |           |                        |           |  |
| Dynamic Range                       | Each axis  | $\pm 18$  |                        |           | $g$                                      |
| Sensitivity                         | $x\_ACCL\_OUT$ and $x\_ACCL\_LOW$ (32-bit)                                     |           | $1.221 \times 10^{-8}$ |           | $g/\text{LSB}$                           |
| Repeatability <sup>1</sup>          | $-40^\circ\text{C} \leq T_C \leq +85^\circ\text{C}$                            |           |                        | $\pm 0.5$ | %  |
| Sensitivity Temperature Coefficient | $-40^\circ\text{C} \leq T_C \leq +85^\circ\text{C}$ , $1\sigma$                |           | $\pm 25$               |           | $\text{ppm}/^\circ\text{C}$              |
| Misalignment                        | Axis to axis   |           | $\pm 0.035$            |           | Degrees                                  |
|                                     | Axis to frame (package)  |           | $\pm 1.0$              |           | Degrees                                  |
| Nonlinearity                        | Best fit straight line, $\pm 10\text{ g}$                                      |           | 10                     |           | $\text{mg}$                              |
|                                     | Best fit straight line, $\pm 18\text{ g}$                                      |           | 90                     |           | $\text{mg}$                              |
| <b>Bias</b>                         |  |           |                        |           |  |
| Repeatability <sup>1,2,4</sup>      | $-40^\circ\text{C} \leq T_C \leq +85^\circ\text{C}$ , $1\sigma$                |           | $\pm 16$               |           | $\text{mg}$                              |
| In-Run Bias Stability               | $1\sigma$  |           | 70                     |           | $\mu\text{g}$                            |
| Velocity Random Walk                | $1\sigma$  |           | 0.029                  |           | $\text{m}/\text{sec}/\sqrt{\text{hr}}$   |
| Temperature Coefficient             | $-40^\circ\text{C} \leq T_C \leq +85^\circ\text{C}$ , $1\sigma$                |           | $\pm 0.1$              |           | $\text{mg}/^\circ\text{C}$               |
| <b>Noise</b>                        |  |           |                        |           |  |
| Output Noise                        | No filtering   |           | 1.29                   |           | $\text{mg}$ rms                          |
| Noise Density                       | $f = 10\text{ Hz}$ to $40\text{ Hz}$ , no filtering                            |           | 0.063                  |           | $\text{mg}/\sqrt{\text{Hz}}$ rms         |
| 3 dB Bandwidth                      |  |           | 330                    |           | Hz                                       |
| Sensor Resonant Frequency           |  |           | 5.5                    |           | kHz                                      |
| <b>BAROMETER</b>                    |  |           |                        |           |  |
| Pressure Range                      | Extended   | 300       |                        | 1100      | mbar                                     |
|                                     |  | 10        |                        | 1200      | mbar                                     |
| Sensitivity                         | BAROM_OUT and BAROM_LOW (32-bit)   |           | $6.1 \times 10^{-7}$   |           | $\text{mbar}/\text{LSB}$                 |
| Error with Supply                   |  |           | 0.04                   |           | $\%/V$                                   |
| Total Error                         |  |           | 4.5                    |           | mbar                                     |
| Relative Error <sup>5</sup>         | $-40^\circ\text{C} \leq T_C \leq +85^\circ\text{C}$                            |           | 2.5                    |           | mbar                                     |
| Nonlinearity <sup>6</sup>           | Best fit straight line, FS = 1100 mbar   |           | 0.1                    |           | % of FS                                  |
|                                     | $-40^\circ\text{C} \leq T_C \leq +85^\circ\text{C}$                            |           | 0.2                    |           | % of FS                                  |
| Linear $g$ Sensitivity              | $\pm 1\text{ g}$ , $1\sigma$   |           | 0.005                  |           | $\text{mbar}/\text{g}$                   |
| Noise                               |  |           | 0.025                  |           | $\text{mbar}$ rms                        |

| Parameter   | Test Conditions/Comments             | Min     | Typ     | Max  | Unit   |
|---|--------------------------------------|---------|---------|------|--------|
| TEMPERATURE SENSOR<br>Scale Factor                  | Output = 0x0000 at 25°C (±5°C)       |         | 0.00565 |      | °C/LSB |
| LOGIC INPUTS <sup>7</sup>                           |                                      |         |         |      |        |
| Input Voltage                                       |                                      |         |         |      |        |
| High, V <sub>IH</sub>                               |                                      | 2.0     |         |      | V      |
| Low, V <sub>IL</sub>                                |                                      |         |         | 0.8  | V      |
| $\overline{\text{RST}}$ Pulse Width                 |                                      | 1       |         |      | μs     |
| $\overline{\text{CS}}$ Wake-Up Pulse Width          |                                      | 20      |         |      | μs     |
| Input Current                                       |                                      |         |         |      |        |
| Logic 1 (High), I <sub>IH</sub>                     | V <sub>IH</sub> = 3.3 V              |         |         | 10   | μA     |
| Logic 0 (Low), I <sub>IL</sub>                      | V <sub>IL</sub> = 0 V                |         |         |      |        |
| All Pins Except $\overline{\text{RST}}$             |                                      |         |         | 10   | μA     |
| $\overline{\text{RST}}$ Pin                         |                                      |         | 0.33    |      | mA     |
| Input Capacitance, C <sub>IN</sub>                  |                                      |         | 10      |      | pF     |
| DIGITAL OUTPUTS                                     |                                      |         |         |      |        |
| Output Voltage                                      |                                      |         |         |      |        |
| High, V <sub>OH</sub>                               | I <sub>SOURCE</sub> = 0.5 mA         | 2.4     |         |      | V      |
| Low, V <sub>OL</sub>                                | I <sub>SINK</sub> = 2.0 mA           |         |         | 0.4  | V      |
| FLASH MEMORY  |                                      |         |         |      |        |
| Data Retention <sup>9</sup>                         | Endurance <sup>8</sup>               | 100,000 |         |      | Cycles |
|   | T <sub>J</sub> = 85°C                | 20      |         |      | Years  |
| FUNCTIONAL TIMES <sup>10</sup>                      | Time until data is available         |         |         |      |        |
| Power-On Start-Up Time                              |                                      |         |         | 600  | ms     |
| Back-up   |                                      |         | 1370    | 1500 | ms     |
| Reset Recovery Time <sup>11</sup>                   |                                      |         | 390     | 600  | ms     |
| Sleep Mode Recovery Time                            |                                      |         | 730     | 1000 | μs     |
| Flash Memory  |                                      |         |         |      |        |
| Update Time <sup>12</sup>                           |                                      |         | 1.05    | 6.8  | sec    |
| Test Time   |                                      |         | 50      |      | ms     |
| On Demand Self Test Time                            | Using internal clock (2460 Hz)       |         | 12      |      | ms     |
| CONVERSION RATE                                     |                                      |         |         |      |        |
| Initial Clock Accuracy                              |                                      |         | 2.46    |      | kSPS   |
| Temperature Coefficient                             |                                      |         | 0.02    |      | %      |
| Sync Input Clock <sup>13</sup>                      |                                      | 0.7     |         | 2.4  | kHz    |
| POWER SUPPLY, VDD                                   | Operating voltage range, VDD = 3.3 V | 3.0     |         | 3.6  | V      |
| Power Supply Current, I <sub>DD</sub> <sup>14</sup> | Normal mode, μ ± σ                   |         | 186     |      | mA     |
|   | Sleep mode                           |         | 12.2    |      | mA     |
|   | Power-down mode                      |         | 37      |      | μA     |
| POWER SUPPLY, VDDRTC                                | Operating voltage range              | 3.0     | 3.3     | 3.6  | V      |
| Real-Time Clock Supply Current                      | Normal mode, VDDRTC = 3.3 V          |         | 13      |      | μA     |

<sup>1</sup> The repeatability specifications represent analytical projections based on the following drift contributions and conditions: temperature hysteresis (−40°C to +85°C), electronics drift (high temperature operating life test: 110°C, 500 hours), drift from temperature cycling (JEDEC22, Method A104-C, Method N, 500 cycles, −55°C to +85°C), rate random walk (10-year projection), and broadband noise.

<sup>2</sup> Bias repeatability describes a long-term behavior over a variety of conditions. Short-term repeatability relates to the in-run bias stability and noise density specifications.

<sup>3</sup> All specifications associated with the accelerometers relate to the full-scale range of ±18 g.

<sup>4</sup> X-ray exposure can degrade this performance metric.

<sup>5</sup> The relative error assumes that the initial error, at 25°C, is corrected in the end application.

<sup>6</sup> Specification assumes a full scale (FS) of 1000 mbar.

<sup>7</sup> The digital I/O signals use a 3.3 V system.

<sup>8</sup> Endurance is qualified as per JEDEC Standard 22, Method A117, measured at −40°C, +25°C, +85°C, and +125°C.

<sup>9</sup> The data retention specification assumes a junction temperature (T<sub>J</sub>) of 85°C per JEDEC Standard 22, Method A117. Data retention lifetime decreases with T<sub>J</sub>.

<sup>10</sup> These times do not include thermal settling and internal filter response times, which may affect overall accuracy.

<sup>11</sup> The  $\overline{\text{RST}}$  line must be in a low state for at least 10 μs to ensure a proper reset initiation and recovery.

<sup>12</sup> Monitoring the data ready signal (see Table 153 for FNCTIO\_CTRL configuration) for the return of regular pulsing can help minimize system wait times.

<sup>13</sup> The device functions at clock rates below 0.7 kHz but at reduced performance levels.

<sup>14</sup> Supply current transients can reach 600 mA during initial startup or reset recovery.

**TIMING SPECIFICATIONS**

$T_c = 25^\circ\text{C}$ ,  $V_{DD} = 3.3\text{ V}$ , unless otherwise noted.

**Table 2.**

| Parameter                      | Description   | Min <sup>1</sup> | Typ | Max <sup>1</sup> | Unit          |
|--------------------------------|---|------------------|-----|------------------|---------------|
| $f_{\text{SCLK}}$              | Serial clock  | 0.01             |     | 15               | MHz           |
| $t_{\text{STALL}}^2$           | Stall period between data                                     | 2                |     |                  | $\mu\text{s}$ |
| $t_{\text{CLS}}$               | Serial clock low period                                       | 31               |     |                  | ns            |
| $t_{\text{CHS}}$               | Serial clock high period                                      | 31               |     |                  | ns            |
| $t_{\overline{\text{CS}}}$     | Chip select to clock edge                                     | 32               |     |                  | ns            |
| $t_{\text{DAV}}$               | DOUT valid after SCLK edge                                    |                  |     | 10               | ns            |
| $t_{\text{DSU}}$               | DIN setup time before SCLK rising edge                        | 2                |     |                  | ns            |
| $t_{\text{DHD}}$               | DIN hold time after SCLK rising edge                          | 2                |     |                  | ns            |
| $t_{\text{DR}}, t_{\text{DF}}$ | DOUT rise/fall times, $\leq 100\text{ pF}$ loading            |                  | 3   | 8                | ns            |
| $t_{\text{DSOE}}$              | $\overline{\text{CS}}$ assertion to data out active           | 0                |     | 11               | ns            |
| $t_{\text{HD}}$                | SCLK edge to data out invalid                                 | 0                |     |                  | ns            |
| $t_{\text{SFS}}$               | Last SCLK edge to $\overline{\text{CS}}$ deassertion          | 32               |     |                  | ns            |
| $t_{\text{DSHI}}$              | $\overline{\text{CS}}$ deassertion to data out high impedance | 0                |     | 9                | ns            |
|                                | Data ready pulse width  |                  | 11  | 15               | $\mu\text{s}$ |
| $t_1$                          | Input sync pulse width  | 5                |     |                  | $\mu\text{s}$ |
| $t_2$                          | Input sync to data invalid                                    |                  | 560 | 570              | $\mu\text{s}$ |
| $t_3$                          | Input sync period   | 417              |     |                  | $\mu\text{s}$ |

<sup>1</sup> Guaranteed by design and characterization, but not tested in production.

<sup>2</sup> See Table 3 for exceptions to the stall time rating.

**Register Specific Stall Times****Table 3.**

| Parameter   | Description                      | Min <sup>1</sup> | Typ | Max | Unit          |
|-------------|----------------------------------|------------------|-----|-----|---------------|
| STALL TIME  |                                  |                  |     |     |               |
| FNCTIO_CTRL | Configure DIOx functions         | 15               |     |     | $\mu\text{s}$ |
| FILTR_BNK_0 | Enable/select FIR filter banks   | 10               |     |     | $\mu\text{s}$ |
| FILTR_BNK_1 | Enable/select FIR filter banks   | 10               |     |     | $\mu\text{s}$ |
| NULL_CNFG   | Configure autonull bias function | 10               |     |     | $\mu\text{s}$ |
| GLOB_CMD[1] | Self test                        | 12000            |     |     | $\mu\text{s}$ |
| GLOB_CMD[2] | Flash memory test                | 50000            |     |     | $\mu\text{s}$ |
| GLOB_CMD[3] | Flash memory update              | 375000           |     |     | ms            |
| GLOB_CMD[6] | Factory calibration restore      | 75000            |     |     | sec           |
| GLOB_CMD[7] | Software reset                   | 120000           |     |     | ms            |

<sup>1</sup> Monitoring the data ready signal (see Table 153 for FNCTIO\_CTRL configuration) for the return of regular pulsing can help minimize system wait times.

Timing Diagrams

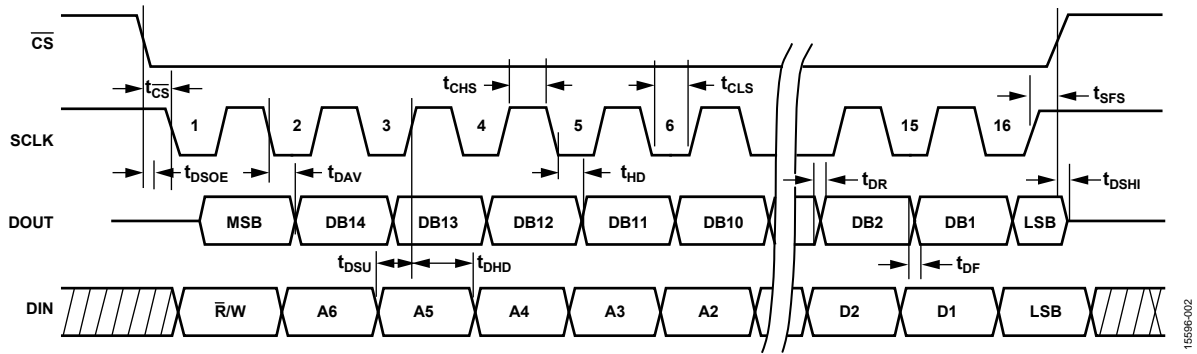


Figure 2. SPI Timing and Sequence

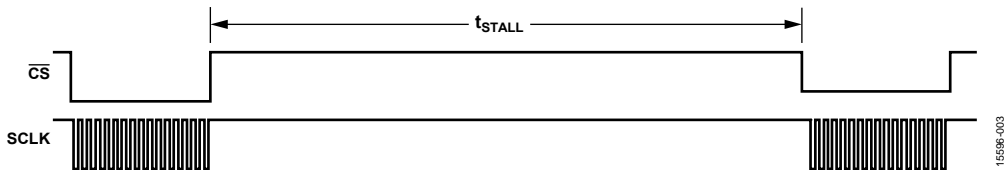


Figure 3. Stall Time and Data Rate

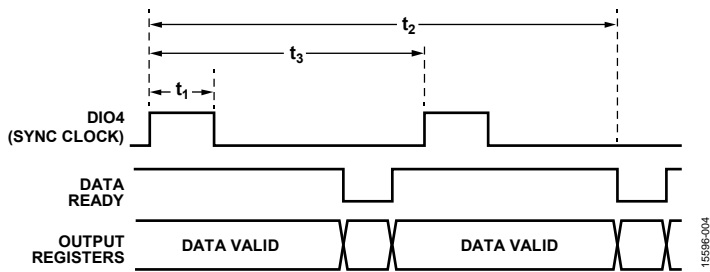


Figure 4. Input Clock Timing Diagram, FNCTIO\_CTRL[7:4] = 0xFD

## ABSOLUTE MAXIMUM RATINGS

Table 4.

| Parameter                              | Rating                |
|--|-----------------------|
| Shock Survivability                    |                       |
| Any Axis, Unpowered                    | 2000 <i>g</i>         |
| Any Axis, Powered                      | 2000 <i>g</i>         |
| VDD to GND                             | −0.3 V to +3.6 V      |
| Digital Input Voltage to GND           | −0.3 V to VDD + 0.2 V |
| Digital Output Voltage to GND          | −0.3 V to VDD + 0.2 V |
| Operating Temperature Range            | −40°C to +105°C       |
| Storage Temperature Range <sup>1</sup> | −65°C to +150°C       |
| Barometric Pressure                    | 2 bar                 |

<sup>1</sup> Extended exposure to temperatures that are lower than −55°C or higher than +105°C can adversely affect the accuracy of the factory calibration.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

$\theta_{JA}$  is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure.

$\theta_{JC}$  is the junction to case thermal resistance.

The ADIS16489 is a multichip module, which includes many active components. The values in Table 5 identify the thermal response of the hottest component inside of the ADIS16489 with respect to the overall power dissipation of the module.

This approach enables a simple method for predicting the temperature of the hottest junction, based on either ambient or case temperature.

For example, when the ambient temperature is 70°C, the hottest junction inside of the ADIS16489 is 89.1°C.

$$T_J = \theta_{JA} \times VDD \times I_{DD} + 70^\circ\text{C}$$

$$T_J = 22.8^\circ\text{C}/\text{W} \times 3.3 \text{ V} \times 0.254\text{A} + 70^\circ\text{C}$$

$$T_J = 89.1^\circ\text{C}$$

Table 5. Package Characteristics

| Package Type         | $\theta_{JA}$ | $\theta_{JC}$ | Device Weight |
|----------------------|---------------|---------------|---------------|
| ML-24-6 <sup>1</sup> | 22.8°C/W      | 10.1°C/W      | 48 g          |

<sup>1</sup> Thermal impedance simulated values come from a case when four M2 × 0.4 mm machine screws (torque = 20 inch ounces) secure the ADIS16489 to the printed circuit board.

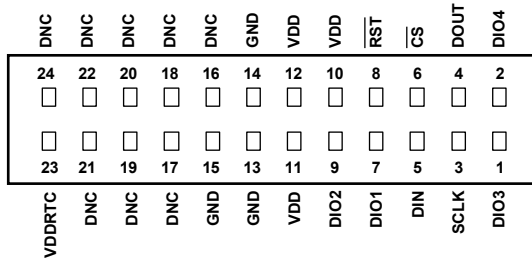
## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

ADIS16489  
TOP VIEW  
(Not to Scale)



**NOTES**

1. THIS REPRESENTATION DISPLAYS THE TOP VIEW PINOUT FOR THE MATING SOCKET CONNECTOR.
2. THE ACTUAL CONNECTOR PINS ARE NOT VISIBLE FROM THE TOP VIEW.
3. MATING CONNECTOR: SAMTEC CLM-112-02 OR EQUIVALENT.
4. DNC = DO NOT CONNECT.

Figure 5. Pin Configuration

1559B-005

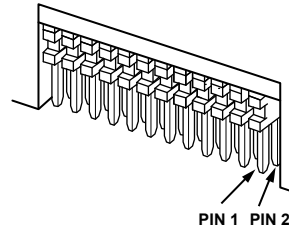
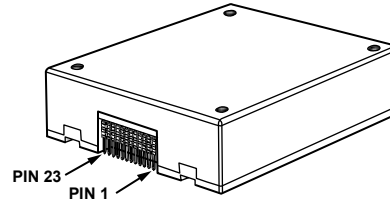


Figure 6. Axial Orientation (Top Side Facing Up)

1559B-006

Table 6. Pin Function Descriptions

| Pin No.      | Mnemonic | Type           | Description  |
|--------------|----------|----------------|--|
| 1            | DIO3     | Input/output   | Configurable Digital Input/Output 3.                     |
| 2            | DIO4     | Input/output   | Configurable Digital Input/Output 4.                     |
| 3            | SCLK     | Input          | SPI Serial Clock.  |
| 4            | DOUT     | Output         | SPI Data Output. Clocks output on the SCLK falling edge. |
| 5            | DIN      | Input          | SPI Data Input. Clocks input on the SCLK rising edge.    |
| 6            | CS       | Input          | SPI Chip Select.   |
| 7            | DIO1     | Input/output   | Configurable Digital Input/Output 1.                     |
| 8            | RST      | Input          | Reset.   |
| 9            | DIO2     | Input/output   | Configurable Digital Input/Output 2.                     |
| 10, 11, 12   | VDD      | Supply         | Power Supply.  |
| 13, 14, 15   | GND      | Supply         | Power Ground.  |
| 16 to 22, 24 | DNC      | Not applicable | Do Not Connect. Do not connect to these pins.            |
| 23           | VDDRTC   | Supply         | Real-Time Clock Power Supply.                            |



### TYPICAL PERFORMANCE CHARACTERISTICS

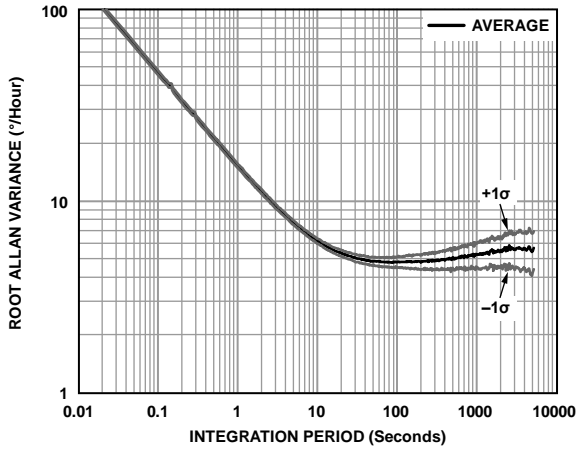


Figure 7. Gyroscope Allan Variance,  $T_c = 25^\circ\text{C}$

15596-007

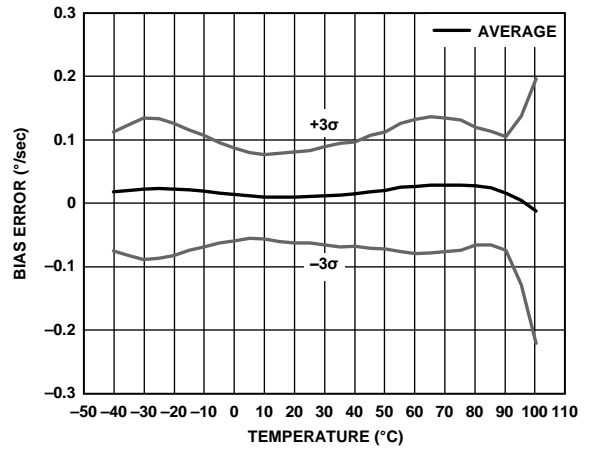


Figure 9. Gyroscope Bias Error vs. Temperature

15596-209

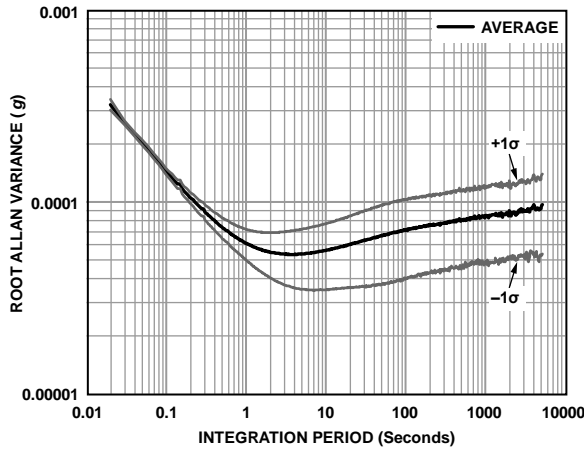


Figure 8. Accelerometer Allan Variance,  $T_c = 25^\circ\text{C}$

15596-008

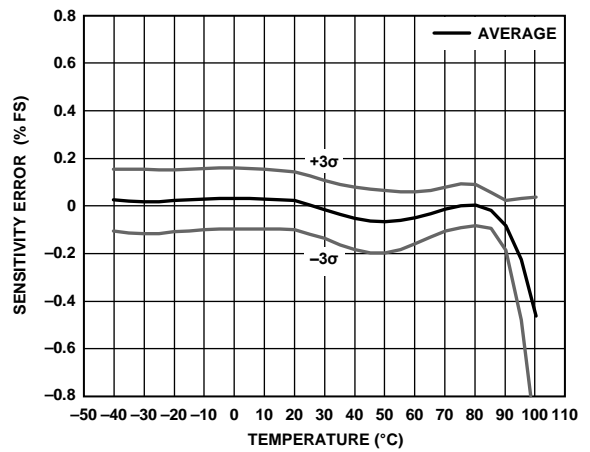


Figure 10. Gyroscope Scale (Sensitivity) Error vs. Temperature

15596-210

# THEORY OF OPERATION

## INTRODUCTION

The ADIS16489 is an autonomous sensor system that starts up on its own when it has a valid power supply. After running through its initialization process, it begins sampling, processing, and loading calibrated sensor data into the output registers, which are accessible using the SPI port. The SPI port typically connects to a compatible port on an embedded processor, using the connection diagram shown in Figure 11. The four SPI signals facilitate synchronous, serial data communication. The factory default configuration provides users with a data ready signal on the DIO2 pin to help facilitate consistent data acquisition (see Figure 31).

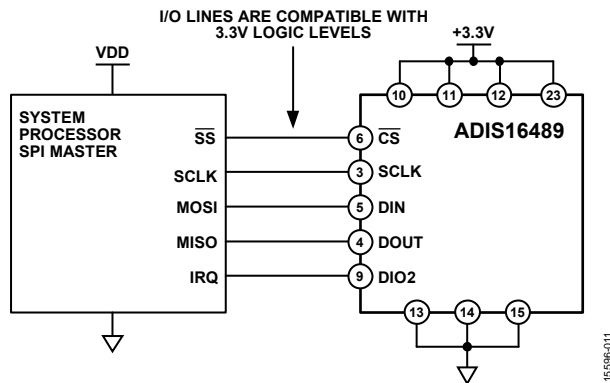


Figure 11. Electrical Connection Diagram

Table 7. Generic Master Processor Pin Names and Functions

| Mnemonic        | Function                   |
|-----------------|----------------------------|
| $\overline{SS}$ | Slave select               |
| SCLK            | Serial clock               |
| MOSI            | Master output, slave input |
| MISO            | Master input, slave output |
| IRQ             | Interrupt request          |

Embedded processors typically use control registers to configure their serial ports for communicating with SPI slave devices such as the ADIS16489. Table 8 provides a list of settings that describe the SPI protocol of the ADIS16489. The initialization routine of the master processor typically establishes these settings using firmware commands to write them into its serial control registers.

Table 8. Generic Master Processor SPI Settings

| Processor Setting  | Description                           |
|--------------------|---------------------------------------|
| Master             | ADIS16489 operates as slave           |
| SCLK $\leq$ 15 MHz | Maximum serial clock rate             |
| SPI Mode 3         | CPOL = 1 (polarity), CPHA = 1 (phase) |
| MSB First Mode     | Bit sequence                          |
| 16-Bit Mode        | Shift register/data length            |

## REGISTER STRUCTURE

The register structure and SPI port support a simple connection between the ADIS16489 and an embedded processor platform. The register structure contains both output data and control registers. The output data registers include the latest sensor data, a real-time clock, error flags, alarm flags, and identification data. The control registers include sample rate, filtering, input/output, alarms, calibration, and diagnostic configuration options. All communication between the ADIS16489 and an external processor involves either reading or writing to one of the user registers.

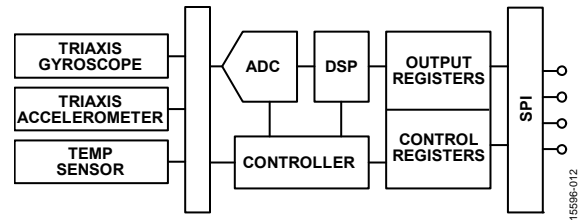
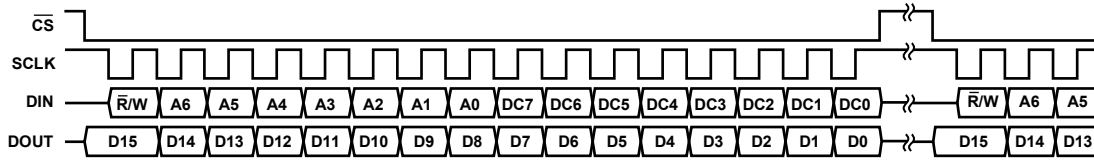


Figure 12. Basic Operation

The register structure uses a paged addressing scheme that contains 13 pages, with each page containing 64 register locations. Each register is 16 bits wide, with each byte having its own unique address within the memory map of that page. The SPI port has access to one page at a time, using the bit sequence in Figure 13. Select the page to activate for SPI access by writing its code to the PAGE\_ID register. Read the PAGE\_ID register to determine which page is currently active. Table 9 displays the PAGE\_ID contents for each page, together with their basic functions. The PAGE\_ID register is located at Address 0x00 on every page.

Table 9. User Register Page Assignments

| Page | PAGE_ID | Function   |
|------|---------|--|
| 0    | 0x00    | Output data, clock, identification                   |
| 1    | 0x01    | Reserved   |
| 2    | 0x02    | Calibration  |
| 3    | 0x03    | Control: sample rate, filtering, I/O, alarms         |
| 4    | 0x04    | Serial number  |
| 5    | 0x05    | FIR Filter Bank A, Coefficient 0 to Coefficient 59   |
| 6    | 0x06    | FIR Filter Bank A, Coefficient 60 to Coefficient 119 |
| 7    | 0x07    | FIR Filter Bank B, Coefficient 0 to Coefficient 59   |
| 8    | 0x08    | FIR Filter Bank B, Coefficient 60 to Coefficient 119 |
| 9    | 0x09    | FIR Filter Bank C, Coefficient 0 to Coefficient 59   |
| 10   | 0x0A    | FIR Filter Bank C, Coefficient 60 to Coefficient 119 |
| 11   | 0x0B    | FIR Filter Bank D, Coefficient 0 to Coefficient 59   |
| 12   | 0x0C    | FIR Filter Bank D, Coefficient 60 to Coefficient 119 |



- NOTES
1. DOUT BITS ARE PRODUCED ONLY WHEN THE PREVIOUS 16-BIT DIN SEQUENCE STARTS WITH  $\bar{R}/W = 0$ .
  2. WHEN  $\bar{CS}$  IS HIGH, DOUT IS IN A THREE-STATE, HIGH IMPEDANCE MODE, WHICH ALLOWS MULTIFUNCTIONAL USE OF THE LINE FOR OTHER DEVICES.

Figure 13. SPI Communication Bit Sequence

### SPI COMMUNICATION

Each SPI command and response is 16 bits in length and uses the digital coding from Figure 13.

### DEVICE CONFIGURATION

Each register contains 16 bits (two bytes). Bits[7:0] contain the low byte, and Bits[15:8] contain the high byte of each register. Each byte has its own unique address in the user register map (see Table 10). Updating the contents of a register requires writing to its low byte first and its high byte second. There are three parts to coding a SPI command (see Figure 13), which writes a new byte of data to a register: the write bit ( $\bar{R}/W = 1$ ), the address of the byte, [A6:A0], and the new data for that location, [DC7:DC0]. Figure 14 provides a coding example for writing 0xFEDC to the XG\_BIAS\_LOW register (see Table 109), assuming that PAGE\_ID already equals 0x0002.

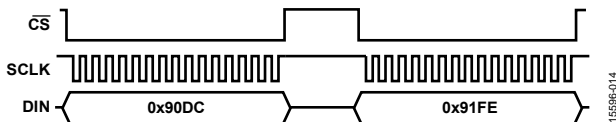


Figure 14. SPI Sequence for Writing 0xFEDC to XG\_BIAS\_LOW

### Dual Memory Structure

The ADIS16489 uses a dual memory structure (see Figure 15), in which the SRAM supports real-time operation and the flash memory provides nonvolatile storage. During the start-up process, the operating code, calibration coefficients, and user register settings load from the flash memory into the SRAM to support normal operation. The manual flash update command (GLOB\_CMD[3], see Table 151) provides a simple method for saving user register values (registers with this feature are indicated by a yes in the flash backup column of Table 10) to the flash memory. This flash backup preserves these settings for automatic recall during the next power-on or reset recovery process.

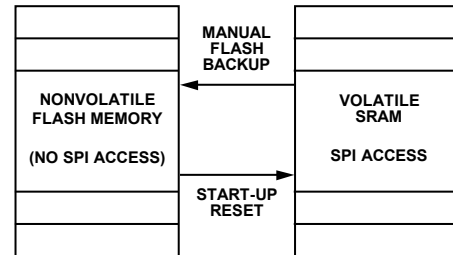


Figure 15. SRAM and Flash Memory Diagram

### READING SENSOR DATA

The 16-bit command code (see Figure 13) for a read request on the SPI has three parts: the read bit ( $\bar{R}/W = 0$ ), either address of the register, [A6:A0], and eight don't care bits, [DC7:DC0]. A read command produces the registers contents on the DOUT pin, during the following 16-bit communication cycle. Figure 16 provides an example that includes two register reads in succession. This example starts with DIN = 0x1A00, to request the contents of the Z\_GYRO\_OUT register, and follows with 0x1800, to request the contents of the Z\_GYRO\_LOW register (assuming PROD\_ID already equals 0x0000). This example illustrates the full duplex mode of operation, which means that the ADIS16489 can receive requests while transmitting the data response from the prior request (see Figure 16).

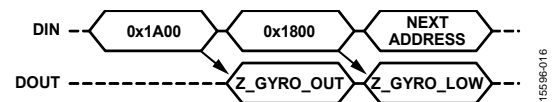


Figure 16. SPI Read Example

Figure 17 provides an example of the four SPI signals when reading the PROD\_ID register (see Table 93) in a repeating pattern. This pattern can be helpful when troubleshooting the SPI interface setup and communications, as it provides clear expectation for all signals (register contents never change).

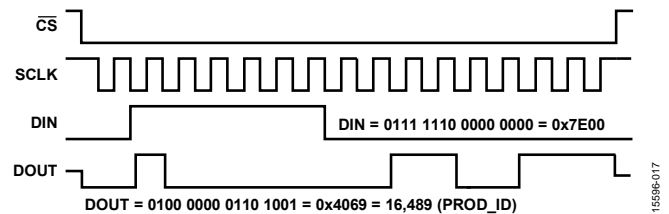


Figure 17. SPI Read Example, Second 16-Bit Sequence

## USER REGISTER MEMORY MAP

Table 10. User Register Memory Map (N/A Means Not Applicable)

| Name          | R/W | Flash Backup | PAGE_ID | Address      | Default | Register Description                     |
|---------------|-----|--------------|---------|--------------|---------|--|
| PAGE_ID       | R/W | No           | 0x00    | 0x00, 0x01   | 0x0000  | Page identifier                          |
| Reserved      | N/A | N/A          | 0x00    | 0x02 to 0x05 | N/A     | Reserved                                 |
| SEQ_CNT       | R   | No           | 0x00    | 0x06, 0x07   | N/A     | Sample sequence counter                  |
| SYS_E_FLAG    | R   | No           | 0x00    | 0x08, 0x09   | 0x0000  | Output, system error flags               |
| DIAG_STS      | R   | No           | 0x00    | 0x0A, 0x0B   | 0x0000  | Output, self test error flags            |
| ALM_STS       | R   | No           | 0x00    | 0x0C, 0x0D   | 0x0000  | Output, alarm error flags                |
| TEMP_OUT      | R   | No           | 0x00    | 0x0E, 0x0F   | N/A     | Output, temperature                      |
| X_GYRO_LOW    | R   | No           | 0x00    | 0x10, 0x11   | N/A     | Output, x-axis gyroscope, low word       |
| X_GYRO_OUT    | R   | No           | 0x00    | 0x12, 0x13   | N/A     | Output, x-axis gyroscope, high word      |
| Y_GYRO_LOW    | R   | No           | 0x00    | 0x14, 0x15   | N/A     | Output, y-axis gyroscope, low word       |
| Y_GYRO_OUT    | R   | No           | 0x00    | 0x16, 0x17   | N/A     | Output, y-axis gyroscope, high word      |
| Z_GYRO_LOW    | R   | No           | 0x00    | 0x18, 0x19   | N/A     | Output, z-axis gyroscope, low word       |
| Z_GYRO_OUT    | R   | No           | 0x00    | 0x1A, 0x1B   | N/A     | Output, z-axis gyroscope, high word      |
| X_ACCL_LOW    | R   | No           | 0x00    | 0x1C, 0x1D   | N/A     | Output, x-axis accelerometer, low word   |
| X_ACCL_OUT    | R   | No           | 0x00    | 0x1E, 0x1F   | N/A     | Output, x-axis accelerometer, high word  |
| Y_ACCL_LOW    | R   | No           | 0x00    | 0x20, 0x21   | N/A     | Output, y-axis accelerometer, low word   |
| Y_ACCL_OUT    | R   | No           | 0x00    | 0x22, 0x23   | N/A     | Output, y-axis accelerometer, high word  |
| Z_ACCL_LOW    | R   | No           | 0x00    | 0x24, 0x25   | N/A     | Output, z-axis accelerometer, low word   |
| Z_ACCL_OUT    | R   | No           | 0x00    | 0x26, 0x27   | N/A     | Output, z-axis accelerometer, high word  |
| Reserved      | N/A | N/A          | 0x00    | 0x28 to 0x2D | N/A     | Reserved                                 |
| BAROM_LOW     | R   | No           | 0x00    | 0x2E, 0x2F   | N/A     | Output, barometer, low word              |
| BAROM_OUT     | R   | No           | 0x00    | 0x30, 0x31   | N/A     | Output, barometer, high word             |
| Reserved      | N/A | N/A          | 0x00    | 0x32 to 0x3F | N/A     | Reserved                                 |
| X_DELTANG_LOW | R   | No           | 0x00    | 0x40, 0x41   | N/A     | Output, x-axis delta angle, low word     |
| X_DELTANG_OUT | R   | No           | 0x00    | 0x42, 0x43   | N/A     | Output, x-axis delta angle, high word    |
| Y_DELTANG_LOW | R   | No           | 0x00    | 0x44, 0x45   | N/A     | Output, y-axis delta angle, low word     |
| Y_DELTANG_OUT | R   | No           | 0x00    | 0x46, 0x47   | N/A     | Output, y-axis delta angle, high word    |
| Z_DELTANG_LOW | R   | No           | 0x00    | 0x48, 0x49   | N/A     | Output, z-axis delta angle, low word     |
| Z_DELTANG_OUT | R   | No           | 0x00    | 0x4A, 0x4B   | N/A     | Output, z-axis delta angle, high word    |
| X_DELTVEL_LOW | R   | No           | 0x00    | 0x4C, 0x4D   | N/A     | Output, x-axis delta velocity, low word  |
| X_DELTVEL_OUT | R   | No           | 0x00    | 0x4E, 0x4F   | N/A     | Output, x-axis delta velocity, high word |
| Y_DELTVEL_LOW | R   | No           | 0x00    | 0x50, 0x51   | N/A     | Output, y-axis delta velocity, low word  |
| Y_DELTVEL_OUT | R   | No           | 0x00    | 0x52, 0x53   | N/A     | Output, y-axis delta velocity, high word |
| Z_DELTVEL_LOW | R   | No           | 0x00    | 0x54, 0x55   | N/A     | Output, z-axis delta velocity, low word  |
| Z_DELTVEL_OUT | R   | No           | 0x00    | 0x56, 0x57   | N/A     | Output, z-axis delta velocity, high word |
| Reserved      | N/A | N/A          | 0x00    | 0x58 to 0x77 | N/A     | Reserved                                 |
| TIME_MS_OUT   | R/W | No           | 0x00    | 0x78, 0x79   | N/A     | Real-time clock: minutes/seconds         |
| TIME_DH_OUT   | R/W | No           | 0x00    | 0x7A, 0x7B   | N/A     | Real-time clock: day/hour                |
| TIME_YM_OUT   | R/W | No           | 0x00    | 0x7C, 0x7D   | N/A     | Real-time clock: year/month              |
| PROD_ID       | R   | N/A          | 0x00    | 0x7E, 0x7F   | 0x4069  | Output, product identification (16,489)  |
| Reserved      | N/A | N/A          | 0x01    | 0x00 to 0x7F | N/A     | Reserved                                 |
| PAGE_ID       | R/W | No           | 0x02    | 0x00, 0x01   | 0x0000  | Page identifier                          |
| Reserved      | N/A | N/A          | 0x02    | 0x02, 0x03   | N/A     | Reserved                                 |
| X_GYRO_SCALE  | R/W | Yes          | 0x02    | 0x04, 0x05   | 0x0000  | Calibration, scale, x-axis gyroscope     |
| Y_GYRO_SCALE  | R/W | Yes          | 0x02    | 0x06, 0x07   | 0x0000  | Calibration, scale, y-axis gyroscope     |
| Z_GYRO_SCALE  | R/W | Yes          | 0x02    | 0x08, 0x09   | 0x0000  | Calibration, scale, z-axis gyroscope     |
| X_ACCL_SCALE  | R/W | Yes          | 0x02    | 0x0A, 0x0B   | 0x0000  | Calibration, scale, x-axis accelerometer |
| Y_ACCL_SCALE  | R/W | Yes          | 0x02    | 0x0C, 0x0D   | 0x0000  | Calibration, scale, y-axis accelerometer |
| Z_ACCL_SCALE  | R/W | Yes          | 0x02    | 0x0E, 0x0F   | 0x0000  | Calibration, scale, z-axis accelerometer |

| Name         | R/W | Flash Backup | PAGE_ID | Address      | Default             | Register Description                                  |
|--------------|-----|--------------|---------|--------------|---------------------|---|
| XG_BIAS_LOW  | R/W | Yes          | 0x02    | 0x10, 0x11   | 0x0000              | Calibration, offset, gyroscope, x-axis, low word      |
| XG_BIAS_HIGH | R/W | Yes          | 0x02    | 0x12, 0x13   | 0x0000              | Calibration, offset, gyroscope, x-axis, high word     |
| YG_BIAS_LOW  | R/W | Yes          | 0x02    | 0x14, 0x15   | 0x0000              | Calibration, offset, gyroscope, y-axis, low word      |
| YG_BIAS_HIGH | R/W | Yes          | 0x02    | 0x16, 0x17   | 0x0000              | Calibration, offset, gyroscope, y-axis, high word     |
| ZG_BIAS_LOW  | R/W | Yes          | 0x02    | 0x18, 0x19   | 0x0000              | Calibration, offset, gyroscope, z-axis, low word      |
| ZG_BIAS_HIGH | R/W | Yes          | 0x02    | 0x1A, 0x1B   | 0x0000              | Calibration, offset, gyroscope, z-axis, high word     |
| XA_BIAS_LOW  | R/W | Yes          | 0x02    | 0x1C, 0x1D   | 0x0000              | Calibration, offset, accelerometer, x-axis, low word  |
| XA_BIAS_HIGH | R/W | Yes          | 0x02    | 0x1E, 0x1F   | 0x0000              | Calibration, offset, accelerometer, x-axis, high word |
| YA_BIAS_LOW  | R/W | Yes          | 0x02    | 0x20, 0x21   | 0x0000              | Calibration, offset, accelerometer, y-axis, low word  |
| YA_BIAS_HIGH | R/W | Yes          | 0x02    | 0x22, 0x23   | 0x0000              | Calibration, offset, accelerometer, y-axis, high word |
| ZA_BIAS_LOW  | R/W | Yes          | 0x02    | 0x24, 0x25   | 0x0000              | Calibration, offset, accelerometer, z-axis, low word  |
| ZA_BIAS_HIGH | R/W | Yes          | 0x02    | 0x26, 0x27   | 0x0000              | Calibration, offset, accelerometer, z-axis, high word |
| Reserved     | N/A | N/A          | 0x02    | 0x28 to 0x73 | 0x0000              | Reserved  |
| BR_BIAS_LOW  | R/W | Yes          | 0x02    | 0x40, 0x41   | 0x0000              | Calibration, offset, barometer, low word              |
| BR_BIAS_HIGH | R/W | Yes          | 0x02    | 0x42, 0x43   | 0x0000              | Calibration, offset, barometer, high word             |
| Reserved     | N/A | N/A          | 0x02    | 0x28 to 0x73 | 0x0000              | Reserved  |
| USER_SCR_1   | R/W | Yes          | 0x02    | 0x74, 0x75   | 0x0000              | User Scratch Register 1                               |
| USER_SCR_2   | R/W | Yes          | 0x02    | 0x76, 0x77   | 0x0000              | User Scratch Register 2                               |
| USER_SCR_3   | R/W | Yes          | 0x02    | 0x78, 0x79   | 0x0000              | User Scratch Register 3                               |
| USER_SCR_4   | R/W | Yes          | 0x02    | 0x7A, 0x7B   | 0x0000              | User Scratch Register 4                               |
| FLSHCNT_LOW  | R   | N/A          | 0x02    | 0x7C, 0x7D   | N/A                 | Diagnostic, flash memory count, low word              |
| FLSHCNT_HIGH | R   | N/A          | 0x02    | 0x7E, 0x7F   | N/A                 | Diagnostic, flash memory count, high word             |
| PAGE_ID      | R/W | No           | 0x03    | 0x00, 0x01   | 0x0000              | Page identifier                                       |
| GLOB_CMD     | W   | No           | 0x03    | 0x02, 0x03   | N/A                 | Control, global commands                              |
| Reserved     | N/A | N/A          | 0x03    | 0x04, 0x05   | N/A                 | Reserved  |
| FNCTIO_CTRL  | R/W | Yes          | 0x03    | 0x06, 0x07   | 0x000D              | Control, I/O pins, functional definitions             |
| GPIO_CTRL    | R/W | Yes          | 0x03    | 0x08, 0x09   | 0x00X0 <sup>1</sup> | Control, I/O pins, general purpose                    |
| CONFIG       | R/W | Yes          | 0x03    | 0x0A, 0x0B   | 0x00C0              | Control, clock, and miscellaneous correction          |
| DEC_RATE     | R/W | Yes          | 0x03    | 0x0C, 0x0D   | 0x0000              | Control, output sample rate decimation                |
| NULL_CNFG    | R/W | Yes          | 0x03    | 0x0E, 0x0F   | 0x070A              | Control, automatic bias correction configuration      |
| SLP_CNT      | W   | No           | 0x03    | 0x10, 0x11   | N/A                 | Control, power-down/sleep mode                        |
| Reserved     | N/A | N/A          | 0x03    | 0x12 to 0x15 | N/A                 | Reserved  |
| FILTR_BNK_0  | R/W | Yes          | 0x03    | 0x16, 0x17   | 0x0000              | Filter selection                                      |
| FILTR_BNK_1  | R/W | Yes          | 0x03    | 0x18, 0x19   | 0x0000              | Filter selection                                      |
| Reserved     | N/A | N/A          | 0x03    | 0x1A to 0x1F | N/A                 | Reserved  |
| ALM_CNFG_0   | R/W | Yes          | 0x03    | 0x20, 0x21   | 0x0000              | Alarm configuration                                   |
| ALM_CNFG_1   | R/W | Yes          | 0x03    | 0x22, 0x23   | 0x0000              | Alarm configuration                                   |
| ALM_CNFG_2   | R/W | Yes          | 0x03    | 0x24, 0x25   | 0x0000              | Alarm configuration                                   |
| Reserved     | N/A | N/A          | 0x03    | 0x26, 0x27   | N/A                 | Reserved  |
| XG_ALM_MAGN  | R/W | Yes          | 0x03    | 0x28, 0x29   | 0x0000              | Alarm configuration, x-axis gyroscope                 |
| YG_ALM_MAGN  | R/W | Yes          | 0x03    | 0x2A, 0x2B   | 0x0000              | Alarm configuration, y-axis gyroscope                 |
| ZG_ALM_MAGN  | R/W | Yes          | 0x03    | 0x2C, 0x2D   | 0x0000              | Alarm configuration, z-axis gyroscope                 |
| XA_ALM_MAGN  | R/W | Yes          | 0x03    | 0x2E, 0x2F   | 0x0000              | Alarm configuration, x-axis accelerometer             |
| YA_ALM_MAGN  | R/W | Yes          | 0x03    | 0x30, 0x31   | 0x0000              | Alarm configuration, y-axis accelerometer             |
| ZA_ALM_MAGN  | R/W | Yes          | 0x03    | 0x32, 0x33   | 0x0000              | Alarm configuration, z-axis accelerometer             |
| Reserved     | N/A | N/A          | 0x03    | 0x34 to 0x39 | N/A                 | Reserved  |
| BR_ALM_MAGN  | R/W | Yes          | 0x03    | 0x3A, 0x3B   | 0x0000              | Alarm configuration, barometer                        |
| Reserved     | N/A | N/A          | 0x03    | 0x3C to 0x77 | N/A                 | Reserved  |
| FIRM_REV     | R   | Yes          | 0x03    | 0x78, 0x79   | N/A                 | Firmware revision                                     |
| FIRM_DM      | R   | Yes          | 0x03    | 0x7A, 0x7B   | N/A                 | Firmware programming date: day/month                  |
| FIRM_Y       | R   | Yes          | 0x03    | 0x7C, 0x7D   | N/A                 | Firmware programming date: year                       |
| Reserved     | N/A | N/A          | 0x03    | 0x7E, 0x7F   | N/A                 | Reserved  |

| Name          | R/W | Flash Backup | PAGE_ID | Address      | Default | Register Description                                      |
|---------------|-----|--------------|---------|--------------|---------|---|
| PAGE_ID       | R/W | No           | 0x04    | 0x00, 0x01   | 0x0000  | Page identifier   |
| Reserved      | N/A | N/A          | 0x04    | 0x02 to 0x1F | N/A     | Reserved  |
| PART_ID1      | R   | N/A          | 0x04    | 0x20, 0x21   | N/A     | Part Identification 1                                     |
| PART_ID2      | R   | N/A          | 0x04    | 0x22, 0x23   | N/A     | Part Identification 2                                     |
| PART_ID3      | R   | N/A          | 0x04    | 0x24, 0x25   | N/A     | Part Identification 3                                     |
| PART_ID4      | R   | N/A          | 0x04    | 0x26, 0x27   | N/A     | Part Identification 4                                     |
| Reserved      | N/A | N/A          | 0x04    | 0x28 to 0x7F | N/A     | Reserved  |
| PAGE_ID       | R/W | No           | 0x05    | 0x00, 0x01   | 0x0000  | Page identifier   |
| Reserved      | N/A | N/A          | 0x05    | 0x02 to 0x07 | N/A     | Reserved  |
| FIR_COEF_Axxx | R/W | Yes          | 0x05    | 0x08 to 0x7F | N/A     | FIR Filter Bank A: Coefficient 0 through Coefficient 59   |
| PAGE_ID       | R/W | No           | 0x06    | 0x00, 0x01   | 0x0000  | Page identifier   |
| Reserved      | N/A | N/A          | 0x06    | 0x02 to 0x07 | N/A     | Reserved  |
| FIR_COEF_Axxx | R/W | Yes          | 0x06    | 0x08 to 0x7F | N/A     | FIR Filter Bank A: Coefficient 60 through Coefficient 119 |
| PAGE_ID       | R/W | No           | 0x07    | 0x00, 0x01   | 0x0000  | Page identifier   |
| Reserved      | N/A | N/A          | 0x07    | 0x02 to 0x07 | N/A     | Reserved  |
| FIR_COEF_Bxxx | R/W | Yes          | 0x07    | 0x08 to 0x7F | N/A     | FIR Filter Bank B: Coefficient 0 through Coefficient 59   |
| PAGE_ID       | R/W | No           | 0x08    | 0x00, 0x01   | 0x0000  | Page identifier   |
| Reserved      | N/A | N/A          | 0x08    | 0x02 to 0x07 | N/A     | Reserved  |
| FIR_COEF_Bxxx | R/W | Yes          | 0x08    | 0x08 to 0x7F | N/A     | FIR Filter Bank B: Coefficient 60 through Coefficient 119 |
| PAGE_ID       | R/W | No           | 0x09    | 0x00, 0x01   | 0x0000  | Page identifier   |
| Reserved      | N/A | N/A          | 0x09    | 0x02 to 0x07 | N/A     | Reserved  |
| FIR_COEF_Cxxx | R/W | Yes          | 0x09    | 0x08 to 0x7F | N/A     | FIR Filter Bank C: Coefficient 0 through Coefficient 59   |
| PAGE_ID       | R/W | No           | 0x0A    | 0x00, 0x01   | 0x0000  | Page identifier   |
| Reserved      | N/A | N/A          | 0x0A    | 0x02 to 0x07 | N/A     | Reserved  |
| FIR_COEF_Cxxx | R/W | Yes          | 0x0A    | 0x08 to 0x7F | N/A     | FIR Filter Bank C: Coefficient 60 through Coefficient 119 |
| PAGE_ID       | R/W | No           | 0x0B    | 0x00, 0x01   | 0x0000  | Page identifier   |
| Reserved      | N/A | N/A          | 0x0B    | 0x02 to 0x07 | N/A     | Reserved  |
| FIR_COEF_Dxxx | R/W | Yes          | 0x0B    | 0x08 to 0x7F | N/A     | FIR Filter Bank D: Coefficient 0 through Coefficient 59   |
| PAGE_ID       | R/W | No           | 0x0C    | 0x00, 0x01   | 0x0000  | Page identifier   |
| Reserved      | N/A | N/A          | 0x0C    | 0x02 to 0x07 | N/A     | Reserved  |
| FIR_COEF_Dxxx | R/W | Yes          | 0x0C    | 0x08 to 0x7F | N/A     | FIR Filter Bank D: Coefficient 60 through Coefficient 119 |

<sup>1</sup> The GPIO\_CTRL[7:4] bits reflect the logic levels on the DIOx lines and do not have a default setting.

## USER REGISTER DEFINITIONS

### PAGE 0 (PAGE\_ID)

Table 11. PAGE\_ID Register Definition

| Page | Addresses  | Default | Access | Flash Backup |
|------|------------|---------|--------|--------------|
| 0x00 | 0x00, 0x01 | 0x0000  | R/W    | No           |

Table 12. PAGE\_ID Bit Assignments

| Bits   | Description                          |
|--------|--------------------------------------|
| [15:0] | Page number, binary numerical format |

The contents in the PAGE\_ID register (see Table 11 and Table 12) contain the current page setting, and provide a control for selecting another page for SPI access. For example, set DIN = 0x8002 to select Page 2 for SPI-based user access. See Table 10 for the page assignments associated with each user accessible register.

### SAMPLE SEQUENCE COUNTER (SEQ\_CNT)

When using the internal sampling clock, the barometer output data registers (BAROM\_LOW and BAROM\_OUT, see Table 53 and Table 55) update at a rate of 51.25 SPS. When using the external clock, the barometers update at a rate that is 1/48th of the input clock frequency. Therefore, the update rates for the barometer does not change with the DEC\_RATE register settings. SYS\_E\_FLAG[9] (see Table 16) offers a new data indicator bit that indicates new, unread data is in the barometer output data registers. The SEQ\_CNT register provides a counter function to help determine when there is new data in the barometer registers. When SEQ\_CNT = 0x0001, there is new data in the barometer output registers. When beginning a continuous read loop, read SEQ\_CNT, then subtract this value from the maximum value of the range (depends on DEC\_RATE setting; see Table 14) to predict the number of internal sample cycles until the next sample update in the barometer output data registers.

Table 13. SEQ\_CNT Register Definitions

| Page | Addresses  | Default        | Access | Flash Backup |
|------|------------|----------------|--------|--------------|
| 0x00 | 0x06, 0x07 | Not applicable | R      | No           |

Table 14. SEQ\_CNT (Page 0, Base Address = 0x06)

| Bits   | Description                                    |
|--------|--|
| [15:7] | Don't care                                     |
| [6:0]  | Binary counter: range = 1 to 48/(DEC_RATE + 1) |

### STATUS/ERROR FLAG INDICATORS (SYS\_E\_FLAG)

The SYS\_E\_FLAG register (see Table 15 and Table 16) provides various error flags. Reading this register causes all of its bits to return to 0, with the exception of Bit 7. If an error condition persists, its flag (bit) automatically returns to an alarm value of 1.

Table 15. SYS\_E\_FLAG Register Definition

| Page | Addresses  | Default | Access | Flash Backup |
|------|------------|---------|--------|--------------|
| 0x00 | 0x08, 0x09 | 0x0000  | R      | No           |

Table 16. SYS\_E\_FLAG Bit Assignments

| Bits    | Description   |
|---------|---|
| 15      | Watch dog timer flag. A 1 indicates that the ADIS16489 automatically reset itself to clear an issue.  |
| [14:13] | Not used.   |
| 12      | Gyroscope saturation. A 1 indicates that the rate of rotation on one axis is equal to or greater than $\pm 480^\circ/\text{sec}$ ( $\pm 1\%$ tolerance).  |
| [11:10] | Not used.   |
| 9       | Barometer sample update. A 1 indicates that BAROM_OUT (see Table 55) and BAROM_LOW (see Table 53) registers contain new data.   |
| 8       | Not used.   |
| 7       | Processing overrun. A 1 indicates occurrence of a processing overrun. Initiate a reset to recover. Replace the ADIS16489 if this error persists.  |
| 6       | Flash memory failure. A 1 indicates that the most recent flash memory test (GLOB_CMD[2], see Table 151) failed. Repeat test and replace the ADIS16489 if this error persists.   |
| 5       | Sensor failure. A 1 indicates failure of at least one of the sensors, during its self test processes. Run the on demand self test (ODST, GLOB_CMD[1], see Table 151), when the unit is in not in motion. Replace the ADIS16489 if the error persists.                         |
| 4       | Overrange. A 1 indicates that the digital magnitude of at least one sensor has reached 99% of its maximum value. Initiate a reset to recover. Replace the ADIS16489 if this error persists.   |
| 3       | SPI communication error. A 1 indicates that the total number of SCLK cycles is not equal to an integer multiple of 16. Repeat the previous communication sequence to recover. Persistence in this error may indicate a weakness in the SPI service from the master processor. |
| [2:1]   | Not used.   |
| 0       | Alarm status flag. A 1 indicates that one of the user-programmable alarms is active. See ALM_STS for indication of which alarm is active.   |

### SELF TEST ERROR FLAGS (DIAG\_STS)

Table 17. DIAG\_STS Register Definition

| Page | Addresses  | Default | Access | Flash Backup |
|------|------------|---------|--------|--------------|
| 0x00 | 0x0A, 0x0B | 0x0000  | R      | No           |

Table 18. DIAG\_STS Bit Definitions

| Bits    | Description   |
|---------|---|
| [15:12] | Not used  |
| 11      | Self test failure, barometer (1 = failure)            |
| [10:6]  | Not used  |
| 5       | Self test failure, z-axis accelerometer (1 = failure) |
| 4       | Self test failure, y-axis accelerometer (1 = failure) |
| 3       | Self test failure, x-axis accelerometer (1 = failure) |
| 2       | Self test failure, z-axis gyroscope (1 = failure)     |
| 1       | Self test failure, y-axis gyroscope (1 = failure)     |
| 0       | Self test failure, x-axis gyroscope (1 = failure)     |

SYS\_E\_FLAG[5] (see Table 16) contains the pass/fail result (0 = pass) for on demand self test (ODST) operations, whereas the DIAG\_STS register (see Table 17 and Table 18) contains pass/fail flags (0 = pass) for each inertial sensor. Reading the DIAG\_STS register causes all of its bits to restore to 0. The bits in DIAG\_STS return to 1 if the error conditions persists.

**ALARM ERROR FLAGS (ALM\_STS)**

Table 19. ALM\_STS Register Definition

| Page | Addresses  | Default | Access | Flash Backup |
|------|------------|---------|--------|--------------|
| 0x00 | 0x0C, 0x0D | 0x0000  | R      | No           |

Table 20. ALM\_STS Bit Definitions

| Bits    | Description   |
|---------|---|
| [15:12] | Not used  |
| 11      | Barometer alarm flag (1 = alarm is active)            |
| [10:6]  | Not used  |
| 5       | Z-axis accelerometer alarm flag (1 = alarm is active) |
| 4       | Y-axis accelerometer alarm flag (1 = alarm is active) |
| 3       | X-axis accelerometer alarm flag (1 = alarm is active) |
| 2       | Z-axis gyroscope alarm flag (1 = alarm is active)     |
| 1       | Y-axis gyroscope alarm flag (1 = alarm is active)     |
| 0       | X-axis gyroscope alarm flag (1 = alarm is active)     |

The ALM\_STS register (see Table 19 and Table 20) contains the error flags for the alarm settings in the ALM\_CNFG\_0 (see Table 170) and ALM\_CNFG\_1 (see Table 172) registers. Reading the ALM\_STS register causes all bits to restore to 0. If the alarm condition is persistent, its bit restores to a 1 in the next sample cycle.

**INTERNAL TEMPERATURE (TEMP\_OUT)**

Table 21. TEMP\_OUT Register Definition

| Page | Addresses  | Default        | Access | Flash Backup |
|------|------------|----------------|--------|--------------|
| 0x00 | 0x0E, 0x0F | Not applicable | R      | No           |

Table 22. TEMP\_OUT Bit Definitions

| Bits   | Description   |
|--------|---|
| [15:0] | Temperature data; twos complement, 0.00565°C per LSB, 25°C = 0x0000 |

The TEMP\_OUT register (see Table 21 and Table 22) provides a coarse measurement of the temperature inside of the ADIS16489. This data is most useful for monitoring relative changes that influence the temperature inside of the ADIS16489.

Table 23. TEMP\_OUT Data Format Examples

| Temperature (°C) | Decimal | Hex    | Binary              |
|------------------|---------|--------|---------------------|
| +85              | +10,619 | 0x297B | 0010 1001 0111 1011 |
| +25 + 0.0113     | +2      | 0x0002 | 0000 0000 0000 0010 |
| +25 + 0.00565    | +1      | 0x0001 | 0000 0000 0000 0001 |
| +25              | 0       | 0x0000 | 0000 0000 0000 0000 |
| +25 - 0.00565    | -1      | 0xFFFF | 1111 1111 1111 1111 |
| +25 - 0.0113     | -2      | 0xFFFE | 1111 1111 1111 1110 |
| -40              | -11,504 | 0xD310 | 1101 0011 0001 0000 |

**GYROSCOPE DATA**

The gyroscopes in the ADIS16489 measure the angular rate of rotation around three orthogonal axes (x, y, and z). Figure 18 illustrates the orientation of each gyroscope axis, along with the direction of rotation that produces a positive response in each of their measurements.

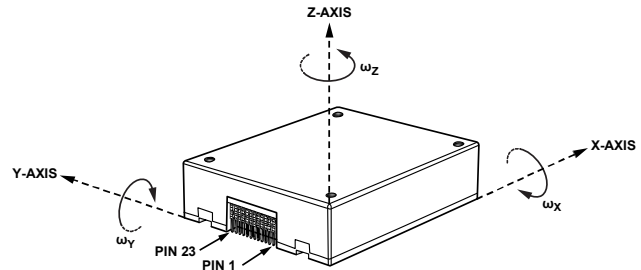


Figure 18. Gyroscope Axis and Polarity Assignments

Each gyroscope has two output data registers. Figure 19 illustrates how these two registers combine to support a 32-bit, twos complement data format for the x-axis gyroscope measurements. This format also applies to the y- and z-axes as well.

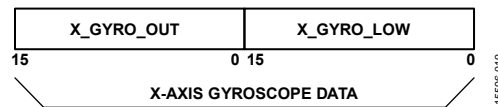


Figure 19. Gyroscope Output Data Structure

**X-Axis Gyroscope (X\_GYRO\_LOW, X\_GYRO\_OUT)**

Table 24. X\_GYRO\_LOW Register Definition

| Page | Addresses  | Default        | Access | Flash Backup |
|------|------------|----------------|--------|--------------|
| 0x00 | 0x10, 0x11 | Not applicable | R      | No           |

Table 25. X\_GYRO\_LOW Bit Definitions

| Bits   | Description                     |
|--------|---------------------------------|
| [15:0] | X-axis gyroscope data; low word |

Table 26. X\_GYRO\_OUT Register Definition

| Page | Addresses  | Default        | Access | Flash Backup |
|------|------------|----------------|--------|--------------|
| 0x00 | 0x12, 0x13 | Not applicable | R      | No           |

Table 27. X\_GYRO\_OUT Bit Definitions

| Bits   | Description  |
|--------|--|
| [15:0] | X-axis gyroscope data; high word; twos complement, ±450°/sec range; 0°/sec = 0x0000, 1 LSB = 0.02°/sec |

The X\_GYRO\_LOW (see Table 24 and Table 25) and X\_GYRO\_OUT (see Table 26 and Table 27) registers contain the gyroscope data for the x-axis.



**Y-Axis Gyroscope (Y\_GYRO\_LOW, Y\_GYRO\_OUT)**

Table 28. Y\_GYRO\_LOW Register Definition

| Page | Addresses  | Default        | Access | Flash Backup |
|------|------------|----------------|--------|--------------|
| 0x00 | 0x14, 0x15 | Not applicable | R      | No           |

Table 29. Y\_GYRO\_LOW Bit Definitions

| Bits   | Description                     |
|--------|---------------------------------|
| [15:0] | Y-axis gyroscope data; low word |

Table 30. Y\_GYRO\_OUT Register Definition

| Page | Addresses  | Default        | Access | Flash Backup |
|------|------------|----------------|--------|--------------|
| 0x00 | 0x16, 0x17 | Not applicable | R      | No           |

Table 31. Y\_GYRO\_OUT Bit Definitions

| Bits   | Description  |
|--------|--|
| [15:0] | Y-axis gyroscope data; high word; twos complement, $\pm 450^\circ/\text{sec}$ range; $0^\circ/\text{sec} = 0x0000$ , 1 LSB = $0.02^\circ/\text{sec}$ |

The Y\_GYRO\_LOW (see Table 28 and Table 29) and Y\_GYRO\_OUT (see Table 30 and Table 31) registers contain the gyroscope data for the y-axis.

**Z-Axis Gyroscope (Z\_GYRO\_LOW, Z\_GYRO\_OUT)**

Table 32. Z\_GYRO\_LOW Register Definition

| Page | Addresses  | Default        | Access | Flash Backup |
|------|------------|----------------|--------|--------------|
| 0x00 | 0x18, 0x19 | Not applicable | R      | No           |

Table 33. Z\_GYRO\_LOW Bit Definitions

| Bits   | Description                                       |
|--------|---|
| [15:0] | Z-axis gyroscope data; additional resolution bits |

Table 34. Z\_GYRO\_OUT Register Definition

| Page | Addresses  | Default        | Access | Flash Backup |
|------|------------|----------------|--------|--------------|
| 0x00 | 0x1A, 0x1B | Not applicable | R      | No           |

Table 35. Z\_GYRO\_OUT Bit Definitions

| Bits   | Description  |
|--------|--|
| [15:0] | Z-axis gyroscope data; high word; twos complement, $\pm 450^\circ/\text{sec}$ range; $0^\circ/\text{sec} = 0x0000$ , 1 LSB = $0.02^\circ/\text{sec}$ |

The Z\_GYRO\_LOW (see Table 32 and Table 33) and Z\_GYRO\_OUT (see Table 34 and Table 35) registers contain the gyroscope data for the z-axis.

**Gyroscope Resolution**

Table 36 and Table 37 offer various numerical examples that demonstrate the format of the angular rate (gyroscopes) data in both 16-bit and 32-bit formats.

Table 36. 16-Bit Gyroscope Data Format Examples

| Rotation Rate ( $^\circ/\text{sec}$ ) | Decimal | Hex    | Binary              |
|---------------------------------------|---------|--------|---------------------|
| +450                                  | +22,500 | 0x57E4 | 0101 0111 1110 0100 |
| +0.04                                 | +2      | 0x0002 | 0000 0000 0000 0010 |
| +0.02                                 | +1      | 0x0001 | 0000 0000 0000 0001 |
| 0                                     | 0       | 0x0000 | 0000 0000 0000 0000 |
| -0.02                                 | -1      | 0xFFFF | 1111 1111 1111 1111 |
| -0.04                                 | -2      | 0xFFFE | 1111 1111 1111 1110 |
| -450                                  | -22,500 | 0xA81C | 1010 1000 0001 1100 |

Table 37. 32-Bit Gyroscope Data Format Examples

| Rotation Rate ( $^\circ/\text{sec}$ ) | Decimal        | Hex        |
|---------------------------------------|----------------|------------|
| +450                                  | +1,474,560,000 | 0x57E40000 |
| +0.02/2 <sup>15</sup>                 | +2             | 0x00000002 |
| +0.02/2 <sup>16</sup>                 | +1             | 0x00000001 |
| 0                                     | 0              | 0x00000000 |
| -0.02/2 <sup>16</sup>                 | -1             | 0xFFFFFFFF |
| -0.02/2 <sup>15</sup>                 | -2             | 0xFFFFFFF8 |
| -450                                  | -1,474,560,000 | 0x73600000 |

**ACCELERATION DATA**

The accelerometers in the ADIS16489 measure both dynamic and static (response to gravity) acceleration along three orthogonal axes (x, y, and z). Figure 20 illustrates the orientation of each accelerometer axis, along with the direction of acceleration that produces a positive response in each of their measurements.

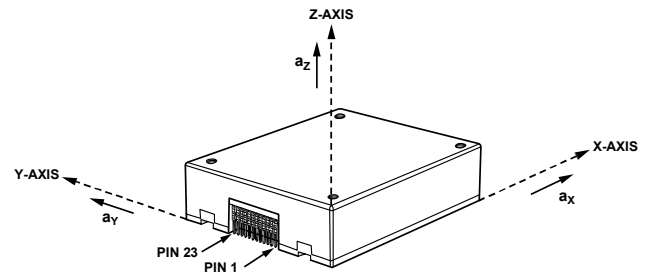


Figure 20. Accelerometer Axis and Polarity Assignments

Each accelerometer has two output data registers. Figure 21 illustrates how these two registers combine to support a 32-bit, twos complement data format for the x-axis accelerometer measurements. This format also applies to the y- and z-axes as well.

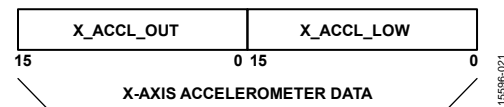


Figure 21. Accelerometer Output Data Structure

**X-Axis Accelerometer (X\_ACCL\_LOW, X\_ACCL\_OUT)**

**Table 38. X\_ACCL\_LOW Register Definition**

| Page | Addresses  | Default        | Access | Flash Backup |
|------|------------|----------------|--------|--------------|
| 0x00 | 0x1C, 0x1D | Not applicable | R      | No           |

**Table 39. X\_ACCL\_LOW Bit Definitions**

| Bits   | Description                         |
|--------|-------------------------------------|
| [15:0] | X-axis accelerometer data; low word |

**Table 40. X\_ACCL\_OUT Register Definition**

| Page | Addresses  | Default        | Access | Flash Backup |
|------|------------|----------------|--------|--------------|
| 0x00 | 0x1E, 0x1F | Not applicable | R      | No           |

**Table 41. X\_ACCL\_OUT Definitions**

| Bits   | Description  |
|--------|--|
| [15:0] | X-axis accelerometer data, high word; twos complement, $\pm 18 g$ range; $0 g = 0x0000$ , 1 LSB = 0.8 mg |

The X\_ACCL\_LOW (see Table 38 and Table 39) and X\_ACCL\_OUT (see Table 40 and Table 41) registers contain the accelerometer data for the x-axis.

**Y-Axis Accelerometer (Y\_ACCL\_LOW, Y\_ACCL\_OUT)**

**Table 42. Y\_ACCL\_LOW Register Definition**

| Page | Addresses  | Default        | Access | Flash Backup |
|------|------------|----------------|--------|--------------|
| 0x00 | 0x20, 0x21 | Not applicable | R      | No           |

**Table 43. Y\_ACCL\_LOW Bit Definitions**

| Bits   | Description                         |
|--------|-------------------------------------|
| [15:0] | Y-axis accelerometer data; low word |

**Table 44. Y\_ACCL\_OUT Register Definition**

| Page | Addresses  | Default        | Access | Flash Backup |
|------|------------|----------------|--------|--------------|
| 0x00 | 0x22, 0x23 | Not applicable | R      | No           |

**Table 45. Y\_ACCL\_OUT Bit Definitions**

| Bits   | Description   |
|--------|---|
| [15:0] | Y-axis accelerometer data; twos complement, $\pm 18 g$ range, $0 g = 0x0000$ , 1 LSB = 0.8 mg |

The Y\_ACCL\_LOW (see Table 42 and Table 43) and Y\_ACCL\_OUT (see Table 44 and Table 45) registers contain the accelerometer data for the y-axis.

**Z-Axis Accelerometer (Z\_ACCL\_LOW, Z\_ACCL\_OUT)**

**Table 46. Z\_ACCL\_LOW Register Definition**

| Page | Addresses  | Default        | Access | Flash Backup |
|------|------------|----------------|--------|--------------|
| 0x00 | 0x24, 0x25 | Not applicable | R      | No           |

**Table 47. Z\_ACCL\_LOW Bit Definitions**

| Bits   | Description                         |
|--------|-------------------------------------|
| [15:0] | Z-axis accelerometer data; low word |

**Table 48. Z\_ACCL\_OUT Register Definition**

| Page | Addresses  | Default        | Access | Flash Backup |
|------|------------|----------------|--------|--------------|
| 0x00 | 0x26, 0x27 | Not applicable | R      | No           |

**Table 49. Z\_ACCL\_OUT Bit Definitions**

| Bits   | Description  |
|--------|--|
| [15:0] | Z-axis accelerometer data, high word; twos complement, $\pm 18 g$ range; $0 g = 0x0000$ , 1 LSB = 0.8 mg |

The Z\_ACCL\_LOW (see Table 46 and Table 47) and Z\_ACCL\_OUT (see Table 48 and Table 49) registers contain the accelerometer data for the z-axis.

**Accelerometer Resolution**

Table 50 and Table 51 offer various numerical examples that demonstrate the format of the linear acceleration data in both 16-bit and 32-bit formats.

**Table 50. 16-Bit Accelerometer Data Format Examples**

| Acceleration | Decimal | Hex    | Binary              |
|--------------|---------|--------|---------------------|
| +18 g        | +20,000 | 0x4E20 | 0100 1110 0010 0000 |
| +1.6 mg      | +2      | 0x0002 | 0000 0000 0000 0010 |
| +0.8 mg      | +1      | 0x0001 | 0000 0000 0000 0001 |
| 0 mg         | 0       | 0x0000 | 0000 0000 0000 0000 |
| -0.8 mg      | -1      | 0xFFFF | 1111 1111 1111 1111 |
| -1.6 mg      | -2      | 0xFFFE | 1111 1111 1111 1110 |
| -18 g        | -20,000 | 0xB1E0 | 1011 0001 1110 0000 |

**Table 51. 32-Bit Accelerometer Data Format Examples**

| Acceleration (g)        | Decimal        | Hex         |
|-------------------------|----------------|-------------|
| +18                     | +1,310,720,000 | 0x4E200000  |
| +0.0008/2 <sup>15</sup> | +2             | 0x00000002  |
| +0.0008/2 <sup>16</sup> | +1             | 0x00000001  |
| 0                       | 0              | 0x00000000  |
| -0.0008/2 <sup>16</sup> | -1             | 0xFFFFFFFF  |
| -0.0008/2 <sup>15</sup> | -2             | 0xFFFFFFFFE |
| -18                     | -1,310,720,000 | 0xB1E00000  |

**BAROMETER DATA**

The barometer measures the atmospheric pressure. The barometer has two output data registers: BAROM\_LOW and BAROM\_OUT. Figure 22 illustrates how these two registers combine to support 32-bit, twos complement data format for the pressure measurements.

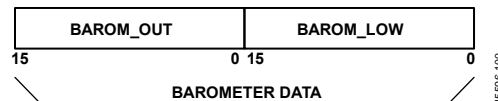


Figure 22. Barometer Output Data Structure

**Barometer (BAROM\_LOW, BAROM\_OUT)**

**Table 52. BAROM\_LOW Register Definition**

| Page | Addresses  | Default        | Access | Flash Backup |
|------|------------|----------------|--------|--------------|
| 0x00 | 0x2E, 0x2F | Not applicable | R      | No           |

**Table 53. BAROM\_LOW Bit Definitions**

| Bits   | Description              |
|--------|--------------------------|
| [15:0] | Barometer data; low word |

Table 54. BAROM\_OUT Register Definition

| Page | Addresses  | Default        | Access | Flash Backup |
|------|------------|----------------|--------|--------------|
| 0x00 | 0x30, 0x31 | Not applicable | R      | No           |

Table 55. BAROM\_OUT Bit Definitions

| Bits   | Description   |
|--------|---|
| [15:0] | Barometer data; high word; twos complement, ±1.31 range; 0 bar = 0x0000, 1 LSB = 40µbar |

The BAROM\_LOW (see Table 52 and Table 53) and BAROM\_OUT (see Table 54 and Table 55) registers contain the barometer data.

**Barometer Resolution**

Table 56 and Table 57 offer various numerical examples that demonstrate the format of the pressure (barometer) data in both 16-bit and 32-bit formats.

Table 56. 16-Bit Barometer Data Format Examples

| Pressure     | Decimal | Hex    | Binary              |
|--------------|---------|--------|---------------------|
| +1.31068 bar | +32767  | 0x3FFF | 0111 1111 1111 1111 |
| +80 µbar     | +2      | 0x0002 | 0000 0000 0000 0010 |
| +40 µbar     | +1      | 0x0001 | 0000 0000 0000 0001 |
| 0            | 0       | 0x0000 | 0000 0000 0000 0000 |
| -40 µbar     | -1      | 0xFFFF | 1111 1111 1111 1111 |
| -80 µbar     | -2      | 0xFFFE | 1111 1111 1111 1110 |
| -1.31072     | -32768  | 0x4000 | 1000 0000 0000 0000 |

Table 57. 32-Bit Barometer Data Format Examples

| Pressure                   | Decimal        | Hex        |
|----------------------------|----------------|------------|
| +1.31068 bar               | +4,294,967,295 | 0x3FFFFFFF |
| +80 µbar ÷ 2 <sup>16</sup> | +2             | 0x00000002 |
| +40 µbar ÷ 2 <sup>16</sup> | +1             | 0x00000001 |
| 0                          | 0              | 0x00000000 |
| -40 µbar ÷ 2 <sup>16</sup> | -1             | 0xFFFFFFF  |
| -80 µbar ÷ 2 <sup>16</sup> | -2             | 0xFFFFFFF  |
| -1.31072                   | -4,294,967,296 | 0x40000000 |

**DELTA ANGLES**

In addition to the angular rate of rotation (gyroscope) measurements around each axis (x, y, and z), the ADIS16489 also provides delta angle measurements that represent a computation of angular displacement between each sample update.

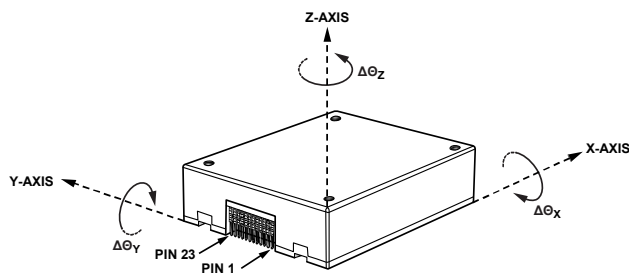


Figure 23. Delta Angle Axis and Polarity Assignments

The delta angle outputs represent an integration of the gyroscope measurements and use the following formula for all three axes (x-axis displayed):

$$\Delta\theta_{x,nD} = \frac{1}{2f_s} \times \sum_{d=0}^{D-1} (\omega_{x,nD+d} + \omega_{x,nD+d-1})$$

where:

D is the decimation rate = DEC\_RATE + 1 (see Table 159).

f<sub>s</sub> is the sample rate.

d is the incremental variable in the summation formula.

ω<sub>x</sub> is the x-axis rate of rotation (gyroscope).

n is the sample time, prior to the decimation filter.

When using the internal sample clock, f<sub>s</sub> is equal to 2460 SPS.

When using the external clock option, f<sub>s</sub> is equal to the frequency of the external clock.

The external clock frequency must be at least 700 Hz to prevent overflow in the delta angle data registers at high rotation rates.

Each axis of the delta angle measurements has two output data registers. Figure 24 illustrates how these two registers combine to support a 32-bit, twos complement data format for the x-axis delta angle measurements. This format also applies to the y- and z-axes as well.

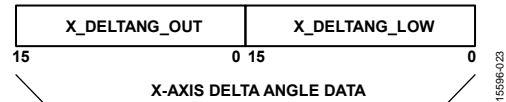


Figure 24. Delta Angle Output Data Structure

**X-Axis Delta Angle (X\_DELTANG\_LOW, X\_DELTANG\_OUT)**

Table 58. X\_DELTANG\_LOW Register Definitions

| Page | Addresses  | Default        | Access | Flash Backup |
|------|------------|----------------|--------|--------------|
| 0x00 | 0x40, 0x41 | Not applicable | R      | No           |

Table 59. X\_DELTANG\_LOW Bit Definitions

| Bits   | Description                       |
|--------|-----------------------------------|
| [15:0] | X-axis delta angle data; low word |

Table 60. X\_DELTANG\_OUT Register Definitions

| Page | Addresses  | Default        | Access | Flash Backup |
|------|------------|----------------|--------|--------------|
| 0x00 | 0x42, 0x43 | Not applicable | R      | No           |

Table 61. X\_DELTANG\_OUT Bit Definitions

| Bits   | Description  |
|--------|--|
| [15:0] | X-axis delta angle data; twos complement, ±720° range, 0° = 0x0000, 1 LSB = 720°/2 <sup>15</sup> = ~0.022° |

The X\_DELTANG\_LOW (see Table 58 and Table 59) and X\_DELTANG\_OUT (see Table 60 and Table 61) registers contain the delta angle data for the x-axis.

**Y-Axis Delta Angle (Y\_DELTANG\_LOW, Y\_DELTANG\_OUT)**

**Table 62. Y\_DELTANG\_LOW Register Definitions**

| Page | Addresses  | Default        | Access | Flash Backup |
|------|------------|----------------|--------|--------------|
| 0x00 | 0x44, 0x45 | Not applicable | R      | No           |

**Table 63. Y\_DELTANG\_LOW Bit Definitions**

| Bits   | Description                       |
|--------|-----------------------------------|
| [15:0] | Y-axis delta angle data; low word |

**Table 64. Y\_DELTANG\_OUT Register Definitions**

| Page | Addresses  | Default        | Access | Flash Backup |
|------|------------|----------------|--------|--------------|
| 0x00 | 0x46, 0x47 | Not applicable | R      | No           |

**Table 65. Y\_DELTANG\_OUT Bit Definitions**

| Bits   | Description   |
|--------|---|
| [15:0] | Y-axis delta angle data; twos complement, $\pm 720^\circ$ range, $0^\circ = 0x0000$ , $1 \text{ LSB} = 720^\circ/2^{15} = \sim 0.022^\circ$ |

The Y\_DELTANG\_LOW (see Table 62 and Table 63) and Y\_DELTANG\_OUT (see Table 64 and Table 65) registers contain the delta angle data for the y-axis.

**Z-Axis Delta Angle (Z\_DELTANG\_LOW, Z\_DELTANG\_OUT)**

**Table 66. Z\_DELTANG\_LOW Register Definitions**

| Page | Addresses  | Default        | Access | Flash Backup |
|------|------------|----------------|--------|--------------|
| 0x00 | 0x48, 0x49 | Not applicable | R      | No           |

**Table 67. Z\_DELTANG\_LOW Bit Definitions**

| Bits   | Description                       |
|--------|-----------------------------------|
| [15:0] | Z-axis delta angle data; low word |

**Table 68. Z\_DELTANG\_OUT Register Definitions**

| Page | Addresses  | Default        | Access | Flash Backup |
|------|------------|----------------|--------|--------------|
| 0x00 | 0x4A, 0x4B | Not applicable | R      | No           |

**Table 69. Z\_DELTANG\_OUT Bit Definitions**

| Bits   | Description   |
|--------|---|
| [15:0] | Z-axis delta angle data; twos complement, $\pm 720^\circ$ range, $0^\circ = 0x0000$ , $1 \text{ LSB} = 720^\circ/2^{15} = \sim 0.022^\circ$ |

The Z\_DELTANG\_LOW (see Table 66 and Table 67) and Z\_DELTANG\_OUT (see Table 68 and Table 69) registers contain the delta angle data for the z-axis.

**Delta Angle Resolution**

Table 70 and Table 71 offers various numerical examples that demonstrate the format of the delta-angle data in 16-bit and 32-bit formats.

**Table 70. 16-Bit Delta Angle Data Format Examples**

| Delta Angle (°)                   | Decimal | Hex     | Binary              |
|-----------------------------------|---------|---------|---------------------|
| $+720 \times (2^{15} - 1)/2^{15}$ | +32,767 | 0x7FFF  | 0111 1111 1110 1111 |
| $+720/2^{14}$                     | +2      | 0x0002  | 0000 0000 0000 0010 |
| $+720/2^{15}$                     | +1      | 0x0001  | 0000 0000 0000 0001 |
| 0                                 | 0       | 0x0000  | 0000 0000 0000 0000 |
| $-720/2^{15}$                     | -1      | 0xFFFF  | 1111 1111 1111 1111 |
| $-720/2^{14}$                     | -2      | 0xFFFFE | 1111 1111 1111 1110 |
| -720                              | -32,768 | 0x8000  | 1000 0000 0000 0000 |

**Table 71. 32-Bit Delta Angle Data Format Examples**

| Delta Angle (°)                   | Decimal        | Hex        |
|-----------------------------------|----------------|------------|
| $+720 \times (2^{31} - 1)/2^{31}$ | +2,147,483,647 | 0x7FFFFFFF |
| $+720/2^{30}$                     | +2             | 0x00000002 |
| $+720/2^{31}$                     | +1             | 0x00000001 |
| 0                                 | 0              | 0x00000000 |
| $-720/2^{31}$                     | -1             | 0xFFFFFFF  |
| $-720/2^{30}$                     | -2             | 0xFFFFFFF  |
| -720                              | -2,147,483,648 | 0x80000000 |

**DELTA VELOCITY**

In addition to the linear acceleration measurements along each axis (x, y, and z), the ADIS16489 also provides delta velocity measurements that represent a computation of linear velocity change between each sample update.

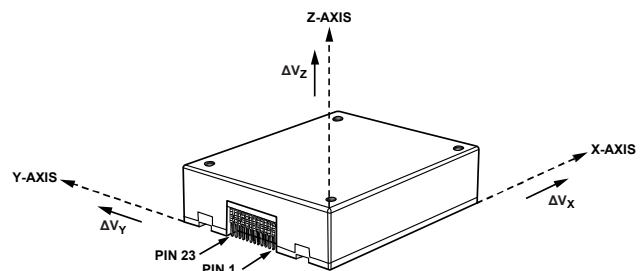


Figure 25. Delta Velocity Axis and Polarity Assignments

The delta velocity outputs represent an integration of the acceleration measurements and use the following formula for all three axes (x-axis displayed):

$$\Delta V_{x,nD} = \frac{1}{2f_s} \times \sum_{d=0}^{D-1} (a_{x,nD+d} + a_{x,nD+d-1})$$

where:

D is the decimation rate = DEC\_RATE + 1 (see Table 159).

f<sub>s</sub> is the sample rate.

d is the incremental variable in the summation formula.

a<sub>x</sub> is the x-axis acceleration (accelerometer).

n is the sample time, prior to the decimation filter.

When using the internal sample clock, f<sub>s</sub> is equal to 2460 SPS.

When using the external clock option, f<sub>s</sub> is equal to the frequency of the external clock. The frequency external of the clock must be at least 700 Hz to prevent overflow in the delta velocity data registers at high acceleration levels.

Each axis of the delta velocity measurements has two output data registers. Figure 26 illustrates how these two registers combine to support 32-bit, twos complement data format, for the x-axis delta velocity measurements. This format also applies to the y- and z-axes as well.

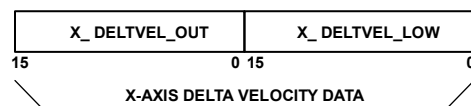


Figure 26. Delta Angle Output Data Structure

**X-Axis Delta Velocity (X\_DELTVEL\_LOW, X\_DELTVEL\_OUT)**

Table 72. X\_DELTVEL\_LOW Register Definitions

| Page | Addresses  | Default        | Access | Flash Backup |
|------|------------|----------------|--------|--------------|
| 0x00 | 0x4C, 0x4D | Not applicable | R      | No           |

Table 73. X\_DELTVEL\_LOW Bit Definitions

| Bits   | Description                       |
|--------|-----------------------------------|
| [15:0] | X-axis delta angle data; low word |

Table 74. X\_DELTVEL\_OUT Register Definitions

| Page | Addresses  | Default        | Access | Flash Backup |
|------|------------|----------------|--------|--------------|
| 0x00 | 0x4E, 0x4F | Not applicable | R      | No           |

Table 75. X\_DELTVEL\_OUT Bit Definitions

| Bits   | Description   |
|--------|---|
| [15:0] | X-axis delta velocity data; twos complement, $\pm 200$ m/sec range, 0 m/sec = 0x0000; 1 LSB = $200 \text{ m/sec} \div 2^{15} = \sim 6.104 \text{ mm/sec}$ |

The X\_DELTVEL\_LOW (see Table 72 and Table 73) and X\_DELTVEL\_OUT (see Table 74 and Table 75) registers contain the delta velocity data for the x-axis.

**Y-Axis Delta Velocity (Y\_DELTVEL\_LOW, Y\_DELTVEL\_OUT)**

Table 76. Y\_DELTVEL\_LOW Register Definitions

| Page | Addresses  | Default        | Access | Flash Backup |
|------|------------|----------------|--------|--------------|
| 0x00 | 0x50, 0x51 | Not applicable | R      | No           |

Table 77. Y\_DELTVEL\_LOW Bit Definitions

| Bits   | Description                          |
|--------|--------------------------------------|
| [15:0] | Y-axis delta velocity data; low word |

Table 78. Y\_DELTVEL\_OUT Register Definitions

| Page | Addresses  | Default        | Access | Flash Backup |
|------|------------|----------------|--------|--------------|
| 0x00 | 0x52, 0x53 | Not applicable | R      | No           |

Table 79. Y\_DELTVEL\_OUT Bit Definitions

| Bits   | Description   |
|--------|---|
| [15:0] | Y-axis delta velocity data; twos complement, $\pm 50$ m/sec range, 0 m/sec = 0x0000; 1 LSB = $50 \text{ m/sec} \div 2^{15} = \sim 1.526 \text{ mm/sec}$ |

The Y\_DELTVEL\_LOW (see Table 76 and Table 77) and Y\_DELTVEL\_OUT (see Table 78 and Table 79) registers contain the delta velocity data for the y-axis.

**Z-Axis Delta Velocity (Z\_DELTVEL\_LOW, Z\_DELTVEL\_OUT)**

Table 80. Z\_DELTVEL\_LOW Register Definitions

| Page | Addresses  | Default        | Access | Flash Backup |
|------|------------|----------------|--------|--------------|
| 0x00 | 0x54, 0x55 | Not applicable | R      | No           |

Table 81. Z\_DELTVEL\_LOW Bit Definitions

| Bits   | Description                       |
|--------|-----------------------------------|
| [15:0] | Z-axis delta angle data; low word |

Table 82. Z\_DELTANG\_OUT Register Definitions

| Page | Addresses  | Default        | Access | Flash Backup |
|------|------------|----------------|--------|--------------|
| 0x00 | 0x56, 0x57 | Not applicable | R      | No           |

Table 83. Z\_DELTVEL\_OUT Bit Definitions

| Bits   | Description   |
|--------|---|
| [15:0] | Z-axis delta velocity data; twos complement, $\pm 200$ m/sec range, 0 m/sec = 0x0000; 1 LSB = $200 \text{ m/sec} \div 2^{15} = \sim 6.104 \text{ mm/sec}$ |

The Z\_DELTVEL\_LOW (see Table 80 and Table 81) and Z\_DELTVEL\_OUT (see Table 82 and Table 83) registers contain the delta velocity data for the z-axis.

**Delta Velocity Resolution**

Table 84 and Table 85 offer various numerical examples that demonstrate the format of the delta velocity data in both 16-bit and 32-bit formats.

Table 84. 16-Bit Delta Velocity Data Format Examples

| Velocity (m/sec)                  | Decimal | Hex    | Binary              |
|-----------------------------------|---------|--------|---------------------|
| $+200 \times (2^{15} - 1)/2^{15}$ | +32,767 | 0x7FFF | 0111 1111 1110 1111 |
| $+200/2^{14}$                     | +2      | 0x0002 | 0000 0000 0000 0010 |
| $+200/2^{15}$                     | +1      | 0x0001 | 0000 0000 0000 0001 |
| 0                                 | 0       | 0x0000 | 0000 0000 0000 0000 |
| $-200/2^{15}$                     | -1      | 0xFFFF | 1111 1111 1111 1111 |
| $-200/2^{14}$                     | -2      | 0xFFFE | 1111 1111 1111 1110 |
| -200                              | -32,768 | 0x8000 | 1000 0000 0000 0000 |

Table 85. 32-Bit Delta Velocity Data Format Examples

| Velocity (m/sec)                  | Decimal        | Hex         |
|-----------------------------------|----------------|-------------|
| $+200 \times (2^{31} - 1)/2^{31}$ | +2,147,483,647 | 0x7FFFFFFF  |
| $+200/2^{30}$                     | +2             | 0x00000002  |
| $+200/2^{31}$                     | +1             | 0x00000001  |
| 0                                 | 0              | 0x00000000  |
| $-200/2^{31}$                     | -1             | 0xFFFFFFFF  |
| $-200/2^{30}$                     | -2             | 0xFFFFFFFFE |
| -200                              | -2,147,483,648 | 0x80000000  |

**REAL-TIME CLOCK**

The VDDRTC power supply pin (see Table 6, Pin 23) provides a separate supply for the real-time clock (RTC) function. Connecting the VDDTC pin to its own 3.3 V supply enables the RTC to keep track of time, even when the main supply (VDD) is off.

Configure the RTC function by selecting one of two modes in CONFIG[0] (see Table 157). The real-time clock data is available in the TIME\_MS\_OUT register (see Table 87), TIME\_DH\_OUT register (see Table 89), and TIME\_YM\_OUT register (see Table 91). When using the elapsed timer mode, the time data registers start at 0x0000 when the device starts up (or resets) and begin keeping time in a manner that is similar to a stopwatch.

When using the clock/calendar mode, write the current time to the real-time registers in the following sequence: seconds (TIME\_MS\_OUT[5:0]), minutes (TIME\_MS\_OUT[13:8]), hours (TIME\_DH\_OUT[5:0]), day (TIME\_DH\_OUT[12:8]), month (TIME\_YM\_OUT[3:0]), and year (TIME\_YM\_OUT[14:8]).

The updates to the timer become active only after a write to the TIME\_YM\_OUT[14:8] byte is complete.

The real-time clock registers reflect the newly updated values only after the next seconds tick of the clock that follows the write to TIME\_YM\_OUT[14:8] (year). Writing to TIME\_YM\_OUT[14:8] activates all timing values; therefore, always write to this location last when updating the timer, even if the year information does not require updating.

Write the current time to each time data register after setting CONFIG[0] = 1 (DIN = 0x8003, DIN = 0x8AC1, DIN = 0x8B00). This sequence preserves the factory default for other bits in the CONFIG register. After configuring the CONFIG register, set GLOB\_CMD[3] = 1 (DIN = 0x8003, DIN = 0x8204, DIN = 0x8300) to back up these settings in flash, and use a separate 3.3 V source to supply power to the VDDRTC function. While only VDDRTC needs to have power for time tracking, access to the time data in the TIME\_xx\_OUT registers requires normal operation (VDD = 3.3 V and full startup).

#### Real-Time Clock: Minutes/Seconds (TIME\_MS\_OUT)

Table 86. TIME\_MS\_OUT Register Definitions

| Page | Addresses  | Default        | Access | Flash Backup |
|------|------------|----------------|--------|--------------|
| 0x00 | 0x78, 0x79 | Not applicable | R/W    | No           |

Table 87. TIME\_MS\_OUT Bit Definitions

| Bits    | Description                           |
|---------|---------------------------------------|
| [15:14] | Not used                              |
| [13:8]  | Minutes, binary data, range = 0 to 59 |
| [7:6]   | Not used                              |
| [5:0]   | Seconds, binary data, range = 0 to 59 |

#### Real-Time Clock: Days/Hours (TIME\_DH\_OUT)

Table 88. TIME\_DH\_OUT Register Definitions

| Page | Addresses  | Default        | Access | Flash Backup |
|------|------------|----------------|--------|--------------|
| 0x00 | 0x7A, 0x7B | Not applicable | R/W    | No           |

Table 89. TIME\_DH\_OUT Bit Definitions

| Bits    | Description                         |
|---------|-------------------------------------|
| [15:13] | Not used                            |
| [12:8]  | Day, binary data, range = 1 to 31   |
| [7:6]   | Not used                            |
| [5:0]   | Hours, binary data, range = 0 to 23 |

#### Real-Time Clock: Years/Months (TIME\_YM\_OUT)

Table 90. TIME\_YM\_OUT Register Definitions

| Page | Addresses  | Default        | Access | Flash Backup |
|------|------------|----------------|--------|--------------|
| 0x00 | 0x7C, 0x7D | Not applicable | R/W    | No           |

Table 91. TIME\_YM\_OUT Bit Definitions

| Bits   | Description   |
|--------|---|
| [15]   | Not used  |
| [14:8] | Year, binary data, range = 0 to 99, relative to 2000 A.D. |
| [7:4]  | Not used  |
| [3:0]  | Month, binary data, range = 1 to 12                       |

### Product Identification (PROD\_ID)

Table 92. PROD\_ID Register Definitions

| Page | Addresses  | Default | Access | Flash Backup   |
|------|------------|---------|--------|----------------|
| 0x00 | 0x7E, 0x7F | 0x4069  | R      | Not applicable |

Table 93. PROD\_ID Bit Definitions

| Bits   | Description                     |
|--------|---------------------------------|
| [15:0] | Product identification = 0x4069 |

The PROD\_ID register (see Table 92 and Table 93) contains the numerical portion of the part number (16489). See Figure 17 for an example of how to use a looping read of this register to validate the integrity of the communication.

### PAGE 2 (PAGE\_ID)

Table 94. PAGE\_ID Register Definition

| Page | Addresses  | Default | Access | Flash Backup |
|------|------------|---------|--------|--------------|
| 0x02 | 0x00, 0x01 | 0x0000  | R/W    | No           |

Table 95. PAGE\_ID Bit Assignments

| Bits   | Description                          |
|--------|--------------------------------------|
| [15:0] | Page number, binary numerical format |

The contents in the PAGE\_ID register (see Table 94 and Table 95) contain the current page setting, and provide a control for selecting another page for SPI access. For example, set DIN = 0x8002 to select Page 2 for SPI-based user access. See Table 10 for the page assignments associated with each user accessible register.

### CALIBRATION

The signal chain of each inertial sensor (accelerometers, gyroscopes) includes application of unique correction formulas, which come from extensive characterization of bias, sensitivity, alignment, and response to linear acceleration (gyroscopes) over a temperature range of  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  for every single ADIS16489. These correction formulas are not accessible, but users do have the opportunity to adjust bias and scale factor, for each sensor individually, through user accessible registers. These correction factors follow immediately after the factory derived correction formulas in the signal chain, which processes at a rate of 2460 Hz when using the internal sample clock (see  $f_s$  in Figure 33).

#### Calibration, Gyroscope Scale (X\_GYRO\_SCALE)

Table 96. X\_GYRO\_SCALE Register Definitions

| Page | Addresses  | Default | Access | Flash Backup |
|------|------------|---------|--------|--------------|
| 0x02 | 0x04, 0x05 | 0x0000  | R/W    | Yes          |

Table 97. X\_GYRO\_SCALE Bit Definitions

| Bits   | Description  |
|--------|--|
| [15:0] | X-axis gyroscope scale correction; twos complement, $0x0000 = \text{unity gain}$ , $1 \text{ LSB} = 1 \div 2^{15} = \sim 0.003052\%$ |

The X\_GYRO\_SCALE register (see Table 96 and Table 97) provides users with the opportunity to adjust the scale factor for the x-axis gyroscopes. See Figure 27 for an illustration of how this scale factor influences the x-axis gyroscope data.

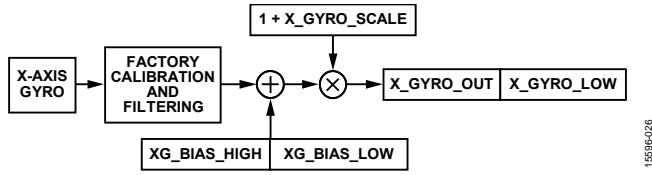


Figure 27. User Calibration Signal Path, Gyroscopes

**Calibration, Gyroscope Scale (Y\_GYRO\_SCALE)**

Table 98. Y\_GYRO\_SCALE Register Definitions

| Page | Addresses  | Default | Access | Flash Backup |
|------|------------|---------|--------|--------------|
| 0x02 | 0x06, 0x07 | 0x0000  | R/W    | Yes          |

Table 99. Y\_GYRO\_SCALE Bit Definitions

| Bits   | Description  |
|--------|--|
| [15:0] | Y-axis gyroscope scale correction; twos complement, 0x0000 = unity gain, 1 LSB = $1 \div 2^{15} = \sim 0.003052\%$ |

The Y\_GYRO\_SCALE register (see Table 98 and Table 99) allows users to adjust the scale factor for the y-axis gyroscopes. This register influences the y-axis gyroscope measurements in the same manner that X\_GYRO\_SCALE influences the x-axis gyroscope measurements (see Figure 27).

**Calibration, Gyroscope Scale (Z\_GYRO\_SCALE)**

Table 100. Z\_GYRO\_SCALE Register Definitions

| Page | Addresses  | Default | Access | Flash Backup |
|------|------------|---------|--------|--------------|
| 0x02 | 0x08, 0x09 | 0x0000  | R/W    | Yes          |

Table 101. Z\_GYRO\_SCALE Bit Definitions

| Bits   | Description  |
|--------|--|
| [15:0] | Z-axis gyroscope scale correction; twos complement, 0x0000 = unity gain, 1 LSB = $1 \div 2^{15} = \sim 0.003052\%$ |

The Z\_GYRO\_SCALE register (see Table 100 and Table 101) allows users to adjust the scale factor for the z-axis gyroscopes. This register influences the z-axis gyroscope measurements in the same manner that X\_GYRO\_SCALE influences the x-axis gyroscope measurements (see Figure 27).

**Calibration, Accelerometer Scale (X\_ACCL\_SCALE)**

Table 102. X\_ACCL\_SCALE Register Definitions

| Page | Addresses  | Default | Access | Flash Backup |
|------|------------|---------|--------|--------------|
| 0x02 | 0x0A, 0x0B | 0x0000  | R/W    | Yes          |

Table 103. X\_ACCL\_SCALE Bit Definitions

| Bits   | Description  |
|--------|--|
| [15:0] | X-axis accelerometer scale correction; twos complement, 0x0000 = unity gain, 1 LSB = $1 \div 2^{15} = \sim 0.003052\%$ |

The X\_ACCL\_SCALE register (see Table 102 and Table 103) allows users to adjust the scale factor for the x-axis accelerometers. See Figure 28 for an illustration of how this scale factor influences the x-axis accelerometer data.

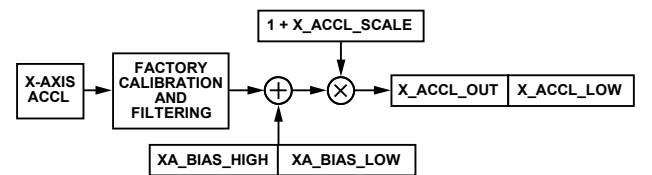


Figure 28. User Calibration Signal Path, Accelerometers

**Calibration, Accelerometer Scale (Y\_ACCL\_SCALE)**

Table 104. Y\_ACCL\_SCALE Register Definitions

| Page | Addresses  | Default | Access | Flash Backup |
|------|------------|---------|--------|--------------|
| 0x02 | 0x0C, 0x0D | 0x0000  | R/W    | Yes          |

Table 105. Y\_ACCL\_SCALE Bit Definitions

| Bits   | Description  |
|--------|--|
| [15:0] | Y-axis accelerometer scale correction; twos complement, 0x0000 = unity gain, 1 LSB = $1 \div 2^{15} = \sim 0.003052\%$ |

The Y\_ACCL\_SCALE register (see Table 104 and Table 105) allows users to adjust the scale factor for the y-axis accelerometers. This register influences the y-axis accelerometer measurements in the same manner that the X\_ACCL\_SCALE influences the x-axis accelerometer measurements (see Figure 28).

**Calibration, Accelerometer Scale (Z\_ACCL\_SCALE)**

Table 106. Z\_ACCL\_SCALE Register Definitions

| Page | Addresses  | Default | Access | Flash Backup |
|------|------------|---------|--------|--------------|
| 0x02 | 0x0E, 0x0F | 0x0000  | R/W    | Yes          |

Table 107. Z\_ACCL\_SCALE Bit Definitions

| Bits   | Description  |
|--------|--|
| [15:0] | Z-axis accelerometer scale correction; twos complement, 0x0000 = unity gain, 1 LSB = $1 \div 2^{15} = \sim 0.003052\%$ |

The Z\_ACCL\_SCALE register (see Table 106 and Table 107) allows users to adjust the scale factor for the z-axis accelerometers. This register influences the z-axis accelerometer measurements in the same manner that the X\_ACCL\_SCALE influences the x-axis accelerometer measurements (see Figure 28).

**Calibration, Gyroscope Bias (XG\_BIAS\_LOW, XG\_BIAS\_HIGH)**

Table 108. XG\_BIAS\_LOW Register Definitions

| Page | Addresses  | Default | Access | Flash Backup |
|------|------------|---------|--------|--------------|
| 0x02 | 0x10, 0x11 | 0x0000  | R/W    | Yes          |

Table 109. XG\_BIAS\_LOW Bit Definitions

| Bits   | Description                                  |
|--------|--|
| [15:0] | X-axis gyroscope offset correction, low word |

Table 110. XG\_BIAS\_HIGH Register Definitions

| Page | Addresses  | Default | Access | Flash Backup |
|------|------------|---------|--------|--------------|
| 0x02 | 0x12, 0x13 | 0x0000  | R/W    | Yes          |

Table 111. XG\_BIAS\_HIGH Bit Definitions

| Bits   | Description   |
|--------|---|
| [15:0] | X-axis gyroscope offset correction, high word twos complement, 0°/sec = 0x0000, 1 LSB = 0.02°/sec |

The XG\_BIAS\_LOW (see Table 108 and Table 109) and XG\_BIAS\_HIGH (see Table 110 and Table 111) registers combine to allow users to adjust the bias of the x-axis gyroscopes. Table 36 and Table 37 offer numerous examples of this data format, in both 16-bit and 32-bit formats. See Figure 27 for an illustration of how these two registers combine and influence the x-axis gyroscope measurements.

**Calibration, Gyroscope Bias (YG\_BIAS\_LOW, YG\_BIAS\_HIGH)**

**Table 112. YG\_BIAS\_LOW Register Definitions**

| Page | Addresses  | Default | Access | Flash Backup |
|------|------------|---------|--------|--------------|
| 0x02 | 0x14, 0x15 | 0x0000  | R/W    | Yes          |

**Table 113. YG\_BIAS\_LOW Bit Definitions**

| Bits   | Description                                  |
|--------|--|
| [15:0] | Y-axis gyroscope offset correction, low word |

**Table 114. YG\_BIAS\_HIGH Register Definitions**

| Page | Addresses  | Default | Access | Flash Backup |
|------|------------|---------|--------|--------------|
| 0x02 | 0x16, 0x17 | 0x0000  | R/W    | Yes          |

**Table 115. YG\_BIAS\_HIGH Bit Definitions**

| Bits   | Description  |
|--------|--|
| [15:0] | Y-axis gyroscope offset correction, high word; twos complement, 0°/sec = 0x0000, 1 LSB = 0.02°/sec |

The YG\_BIAS\_LOW (see Table 112 and Table 113) and YG\_BIAS\_HIGH (see Table 114 and Table 115) registers combine to allow users to adjust the bias of the y-axis gyroscopes. Table 36 and Table 37 offer numerous examples of this data format, in both 16-bit and 32-bit formats. See Figure 27 for an illustration of how these two registers combine and influence the y-axis gyroscope measurements.

**Calibration, Gyroscope Bias (ZG\_BIAS\_LOW, ZG\_BIAS\_HIGH)**

**Table 116. ZG\_BIAS\_LOW Register Definitions**

| Page | Addresses  | Default | Access | Flash Backup |
|------|------------|---------|--------|--------------|
| 0x02 | 0x18, 0x19 | 0x0000  | R/W    | Yes          |

**Table 117. ZG\_BIAS\_LOW Bit Definitions**

| Bits   | Description                                  |
|--------|--|
| [15:0] | Z-axis gyroscope offset correction, low word |

**Table 118. ZG\_BIAS\_HIGH Register Definitions**

| Page | Addresses  | Default | Access | Flash Backup |
|------|------------|---------|--------|--------------|
| 0x02 | 0x1A, 0x1B | 0x0000  | R/W    | Yes          |

**Table 119. ZG\_BIAS\_HIGH Bit Definitions**

| Bits   | Description   |
|--------|---|
| [15:0] | Z-axis gyroscope offset correction, high word twos complement, 0°/sec = 0x0000, 1 LSB = 0.02°/sec |

The ZG\_BIAS\_LOW (see Table 116 and Table 117) and ZG\_BIAS\_HIGH (see Table 118 and Table 119) registers combine to allow users to adjust the bias of the z-axis gyroscopes. Table 36

and Table 37 offer numerous examples of this data format, in both 16-bit and 32-bit formats. See Figure 27 for an illustration of how these two registers combine and influence the z-axis gyroscope measurements.

**Calibration, Accelerometer Bias (XA\_BIAS\_LOW, XA\_BIAS\_HIGH)**

**Table 120. XA\_BIAS\_LOW Register Definitions**

| Page | Addresses  | Default | Access | Flash Backup |
|------|------------|---------|--------|--------------|
| 0x02 | 0x1C, 0x1D | 0x0000  | R/W    | Yes          |

**Table 121. XA\_BIAS\_LOW Bit Definitions**

| Bits   | Description                                      |
|--------|--|
| [15:0] | X-axis accelerometer offset correction, low word |

**Table 122. XA\_BIAS\_HIGH Register Definitions**

| Page | Addresses  | Default | Access | Flash Backup |
|------|------------|---------|--------|--------------|
| 0x02 | 0x1E, 0x1F | 0x0000  | R/W    | Yes          |

**Table 123. XA\_BIAS\_HIGH Bit Definitions**

| Bits   | Description  |
|--------|--|
| [15:0] | X-axis accelerometer offset correction, high word, twos complement, 0 g = 0x0000, 1 LSB = 0.8 mg |

The XA\_BIAS\_LOW (see Table 120 and Table 121) and XA\_BIAS\_HIGH (see Table 122 and Table 123) registers combine to allow users to adjust the bias of the x-axis accelerometers. Table 50 and Table 51 offer numerous examples of data format, in both 16-bit and 32-bit formats. See Figure 28 for an illustration of how these two registers combine and influence the x-axis accelerometer measurements.

**Calibration, Accelerometer Bias (YA\_BIAS\_LOW, YA\_BIAS\_HIGH)**

**Table 124. YA\_BIAS\_LOW Register Definitions**

| Page | Addresses  | Default | Access | Flash Backup |
|------|------------|---------|--------|--------------|
| 0x02 | 0x20, 0x21 | 0x0000  | R/W    | Yes          |

**Table 125. YA\_BIAS\_LOW Bit Definitions**

| Bits   | Description                                      |
|--------|--|
| [15:0] | Y-axis accelerometer offset correction, low word |

**Table 126. YA\_BIAS\_HIGH Register Definitions**

| Page | Addresses  | Default | Access | Flash Backup |
|------|------------|---------|--------|--------------|
| 0x02 | 0x22, 0x23 | 0x0000  | R/W    | Yes          |

**Table 127. YA\_BIAS\_HIGH Bit Definitions**

| Bits   | Description  |
|--------|--|
| [15:0] | Y-axis accelerometer offset correction, high word, twos complement, 0 g = 0x0000, 1 LSB = 0.8 mg |

The YA\_BIAS\_LOW (see Table 124 and Table 125) and YA\_BIAS\_HIGH (see Table 126 and Table 127) registers combine to allow users to adjust the bias of the y-axis accelerometers. Table 50 and Table 51 offer numerous examples of data format, in both 16-bit and 32-bit formats. See Figure 28 for an illustration of how



these two registers combine and influence the y-axis accelerometer measurements.

**Calibration, Accelerometer Bias (ZA\_BIAS\_LOW, ZA\_BIAS\_HIGH)**

**Table 128. ZA\_BIAS\_LOW Register Definitions**

| Page | Addresses  | Default | Access | Flash Backup |
|------|------------|---------|--------|--------------|
| 0x02 | 0x24, 0x25 | 0x0000  | R/W    | Yes          |

**Table 129. ZA\_BIAS\_LOW Bit Definitions**

| Bits   | Description                                      |
|--------|--|
| [15:0] | Z-axis accelerometer offset correction, low word |

**Table 130. ZA\_BIAS\_HIGH Register Definitions**

| Page | Addresses  | Default | Access | Flash Backup |
|------|------------|---------|--------|--------------|
| 0x02 | 0x26, 0x27 | 0x0000  | R/W    | Yes          |

**Table 131. ZA\_BIAS\_HIGH Bit Definitions**

| Bits   | Description  |
|--------|--|
| [15:0] | Z-axis accelerometer offset correction, high word, twos complement, 0 g = 0x0000, 1 LSB = 0.8 mg |

The ZA\_BIAS\_LOW (see Table 128 and Table 129) and ZA\_BIAS\_HIGH (see Table 130 and Table 131) registers combine to allow users to adjust the bias of the z-axis accelerometers. Table 50 and Table 51 offer numerous examples of data format, in both 16-bit and 32-bit formats. See Figure 28 for an illustration of how these two registers combine and influence the z-axis accelerometer measurements.

**BAROMETERS**

**Calibration, Barometer Bias (BR\_BIAS\_LOW, BR\_BIAS\_HIGH)**

The BR\_BIAS\_LOW (see Table 132 and Table 133) and BR\_BIAS\_HIGH (see Table 134 and Table 135) registers provide a user configurable, bias correction function for the barometer measurement. See Figure 29 for the location and influence that this correction factor has in the barometer signal chain.

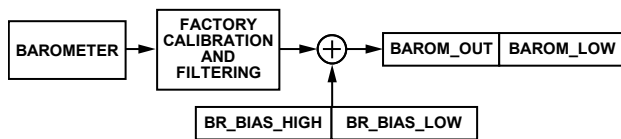


Figure 29. User Calibration Signal Path, Accelerometers

**Table 132. BR\_BIAS\_LOW Register Definitions**

| Page | Addresses  | Default | Access | Flash Backup |
|------|------------|---------|--------|--------------|
| 0x02 | 0x40, 0x41 | 0x0000  | R/W    | Yes          |

**Table 133. BR\_BIAS\_LOW Bit Definitions**

| Bits   | Description  |
|--------|--|
| [15:0] | Barometric pressure bias correction factor, low word |

**Table 134. BR\_BIAS\_HIGH Register Definitions**

| Page | Addresses  | Default | Access | Flash Backup |
|------|------------|---------|--------|--------------|
| 0x02 | 0x42, 0x43 | 0x0000  | R/W    | Yes          |

**Table 135. BR\_BIAS\_HIGH Bit Definitions**

| Bits   | Description   |
|--------|---|
| [15:0] | Barometric pressure bias correction factor, high word, twos complement, ±1.3 bar measurement range, 0 bar = 0x0000, 1 LSB = 40 μbar |

The digital format examples in Table 56 also apply to the BR\_BIAS\_HIGH register and the digital format examples in Table 57 apply to the 32-bit number that comes from combining BR\_BIAS\_LOW and BR\_BIAS\_HIGH.

**SCRATCH REGISTERS (USER\_SCR\_x)**

**Table 136. USER\_SCR\_1 Register Definitions**

| Page | Addresses  | Default | Access | Flash Backup |
|------|------------|---------|--------|--------------|
| 0x02 | 0x74, 0x75 | 0x0000  | R/W    | Yes          |

**Table 137. USER\_SCR\_1 Bit Definitions**

| Bits   | Description  |
|--------|--------------|
| [15:0] | User defined |

**Table 138. USER\_SCR\_2 Register Definitions**

| Page | Addresses  | Default | Access | Flash Backup |
|------|------------|---------|--------|--------------|
| 0x02 | 0x76, 0x77 | 0x0000  | R/W    | Yes          |

**Table 139. USER\_SCR\_2 Bit Definitions**

| Bits   | Description  |
|--------|--------------|
| [15:0] | User defined |

**Table 140. USER\_SCR\_3 Register Definitions**

| Page | Addresses  | Default | Access | Flash Backup |
|------|------------|---------|--------|--------------|
| 0x02 | 0x78, 0x79 | 0x0000  | R/W    | Yes          |

**Table 141. USER\_SCR\_3 Bit Definitions**

| Bits   | Description  |
|--------|--------------|
| [15:0] | User defined |

**Table 142. USER\_SCR\_4 Register Definitions**

| Page | Addresses  | Default | Access | Flash Backup |
|------|------------|---------|--------|--------------|
| 0x02 | 0x7A, 0x7B | 0x0000  | R/W    | Yes          |

**Table 143. USER\_SCR\_4 Bit Definitions**

| Bits   | Description  |
|--------|--------------|
| [15:0] | User defined |

The USER\_SCR\_1 (see Table 136 and Table 137), USER\_SCR\_2 (see Table 138 and Table 139), USER\_SCR\_3 (see Table 140 and Table 141), and USER\_SCR\_4 (see Table 142 and Table 143) registers provide four locations for users to store information.

**FLASH MEMORY ENDURANCE COUNTER (FLSHCNT\_LOW, FLSHCNT\_HIGH)**

Table 144. FLSHCNT\_LOW Register Definitions

| Page | Addresses  | Default        | Access | Flash Backup   |
|------|------------|----------------|--------|----------------|
| 0x02 | 0x7C, 0x7D | Not applicable | R      | Not applicable |

Table 145. FLSHCNT\_LOW Bit Definitions

| Bits   | Description                          |
|--------|--------------------------------------|
| [15:0] | Flash memory write counter, low word |

Table 146. FLSHCNT\_HIGH Register Definitions

| Page | Addresses  | Default        | Access | Flash Backup   |
|------|------------|----------------|--------|----------------|
| 0x02 | 0x7E, 0x7F | Not applicable | R      | Not applicable |

Table 147. FLSHCNT\_HIGH Bit Definitions

| Bits   | Description                           |
|--------|---------------------------------------|
| [15:0] | Flash memory write counter, high word |

The FLSHCNT\_LOW (see Table 144 and Table 145) and FLSHCNT\_HIGH (see Table 146 and Table 147) registers combine to provide a 32-bit, binary counter that tracks the number of flash memory write cycles. In addition to the number of write cycles, the flash memory has a finite service lifetime, which depends on the junction temperature. Figure 30 provides some guidance for estimating the retention life for the flash memory at specific junction temperatures. The junction temperature is approximately 7°C above the case temperature.

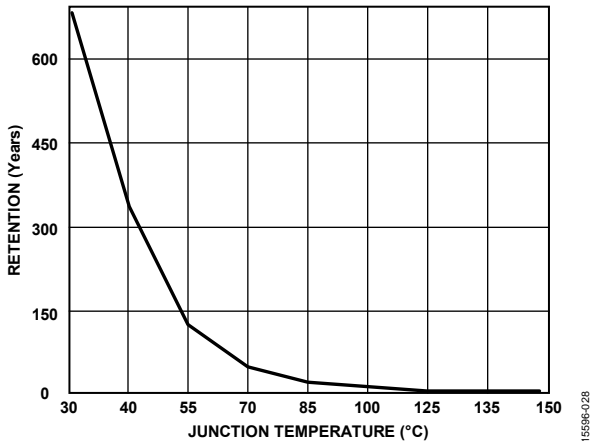


Figure 30. Flash Memory Retention

**PAGE 3 (PAGE\_ID)**

Table 148. PAGE\_ID Register Definition

| Page | Addresses  | Default | Access | Flash Backup |
|------|------------|---------|--------|--------------|
| 0x03 | 0x00, 0x01 | 0x0000  | R/W    | No           |

Table 149. PAGE\_ID Bit Assignments

| Bits   | Description                          |
|--------|--------------------------------------|
| [15:0] | Page number, binary numerical format |

The contents in the PAGE\_ID register (see Table 148 and Table 149) contain the current page setting, and provide a control for selecting another page for SPI access. For example, set DIN = 0x8002 to select Page 2 for SPI-based user access. See Table 10

for the page assignments associated with each user accessible register.

**GLOBAL COMMANDS (GLOB\_CMD)**

Table 150. GLOB\_CMD Register Definitions

| Page | Addresses  | Default        | Access | Flash Backup |
|------|------------|----------------|--------|--------------|
| 0x03 | 0x02, 0x03 | Not applicable | W      | No           |

Table 151. GLOB\_CMD Bit Definitions

| Bits   | Description                  |
|--------|------------------------------|
| [15:8] | Not used                     |
| 7      | Software reset               |
| 6      | Factory calibration restore  |
| [5:4]  | Not used                     |
| 3      | Flash memory update          |
| 2      | Flash memory test (checksum) |
| 1      | Self test                    |
| 0      | Bias correction update       |

The GLOB\_CMD register (see Table 150 and Table 151) provides trigger bits for several operations. Write a 1 to the appropriate bit in GLOB\_CMD to start a particular function.

**Software Reset**

Turn to Page 3 (DIN = 0x8003) and then set GLOB\_CMD[7] = 1 (DIN = 0x8280, DIN = 0x8300) to initiate a reset in the operation of the ADIS16489. This reset removes all data, initializes all registers from their flash settings, and restarts data sampling and processing. This function provides a firmware alternative to providing a low pulse on the RST pin (see Table 6, Pin 8).

**Factory Calibration Restore**

Turn to Page 3 (DIN = 0x8003) and then set GLOB\_CMD[6] = 1 (DIN = 0x8240, DIN = 0x8300) to initiate restoration of the factory calibration. This restoration writes 0x0000 to the following registers: X\_GYRO\_SCALE, Y\_GYRO\_SCALE, Z\_GYRO\_SCALE, X\_ACCL\_SCALE, Y\_ACCL\_SCALE, Z\_ACCL\_SCALE, XG\_BIAS\_LOW, XG\_BIAS\_HIGH, YG\_BIAS\_LOW, YG\_BIAS\_HIGH, ZG\_BIAS\_LOW, ZG\_BIAS\_HIGH, XA\_BIAS\_LOW, XA\_BIAS\_HIGH, YA\_BIAS\_LOW, YA\_BIAS\_HIGH, ZA\_BIAS\_LOW, and ZA\_BIAS\_HIGH.

**Flash Memory Update**

Turn to Page 3 (DIN = 0x8003) and then set GLOB\_CMD[3] = 1 (DIN = 0x8208, DIN = 0x8300) to initiate a manual flash update. SYS\_E\_FLAG[6] (see Table 16) identifies success (0) or failure (1) in completing this process.

**Flash Memory Test**

Turn to Page 3 (DIN = 0x8003) and then set GLOB\_CMD[2] = 1 (DIN = 0x8204, DIN = 0x8300) to initiate a checksum test on the flash memory bank. SYS\_E\_FLAG[6] = 0 (see Table 16) indicates a passing condition, which means that the most recent checksum value is the same as the checksum value, which came from the configuration of the units at the factory.

**On Demand Self Test (ODST)**

Turn to Page 3 (DIN = 0x8003) and then set GLOB\_CMD[1] = 1 (DIN = 0x8202, then DIN = 0x8300) to run the ODST routine, which executes the following steps:

1. Measure the output on each sensor.
2. Activate an internal force on the mechanical elements of each sensor, which simulates the force associated with actual inertial motion.
3. Measure the output response on each sensor.
4. Deactivate the internal force on each sensor.
5. Calculate the difference between the force on and normal operating conditions (force off).
6. Compare the difference with internal pass/fail criteria.
7. Report the pass/fail results for each sensor in DIAG\_STS (see Table 18) and the overall pass/fail flag in SYS\_E\_FLAG[5] (see Table 16).

When using an external clock, the self test execution times may vary from the 12 ms listed in Table 1. Also, false positive results are possible when the executing the ODST while the device is in motion.

**Bias Correction Update**

Turn to Page 3 (DIN = 0x8003) and set GLOB\_CMD[0] = 1 (DIN = 0x8201, then DIN = 0x8300) to update the user offset registers with the correction factors of the continuous bias estimator (CBE). Ensure that the inertial platform is stable during the entire average time for optimal bias estimates.

**AUXILIARY I/O LINE CONFIGURATION (FNCTIO\_CTRL)**

Table 152. FNCTIO\_CTRL Register Definitions

| Page | Addresses  | Default | Access | Flash Backup |
|------|------------|---------|--------|--------------|
| 0x03 | 0x06, 0x07 | 0x000D  | R/W    | Yes          |

Table 153. FNCTIO\_CTRL Bit Definitions

| Bits    | Description  |
|---------|--|
| [15:12] | Not used   |
| 11      | Alarm indicator: 1 = enabled, 0 = disabled                                     |
| 10      | Alarm indicator polarity: 1 = positive, 0 = negative                           |
| [9:8]   | Alarm indicator line selection:<br>00 = DIO1, 01 = DIO2, 10 = DIO3, 11 = DIO4  |
| 7       | Sync clock input enable: 1 = enabled, 0 = disabled                             |
| 6       | Sync clock input polarity:<br>1 = rising edge, 0 = falling edge                |
| [5:4]   | Sync clock input line selection:<br>00 = DIO1, 01 = DIO2, 10 = DIO3, 11 = DIO4 |
| 3       | Data ready enable: 1 = enabled, 0 = disabled                                   |
| 2       | Data ready polarity: 1 = positive, 0 = negative                                |
| [1:0]   | Data ready line selection:<br>00 = DIO1, 01 = DIO2, 10 = DIO3, 11 = DIO4       |

The FNCTIO\_CTRL register (see Table 152 and Table 153) provides configuration control for each input/output pin (DIO1, DIO2, DIO3, and DIO4). Each DIOx pin supports only one function at a time. In cases where a single pin has two assignments, the enable bit for the lower priority function automatically resets to zero (disabling the lower priority function). The order of priority is as follows, from highest priority to lowest priority: data ready, sync clock input, alarm indicator, and general purpose. Changing the FNCTIO\_CTRL[5:4] bit settings requires an execution time of 75 ms, whereas changing the settings of the remaining bits in the FNCTIO\_CTRL register only takes 3 ms. During this execution time (75 ms or 3 ms), the operational state and the contents of the register remain unchanged, but the SPI interface supports normal communication (for accessing other registers).

**Data Ready Indicator**

The FNCTIO\_CTRL[3:0] bits provide three configuration options for the data ready function: on/off, polarity, and DIOx line. The primary purpose this signal is to drive the interrupt control line of an embedded processor, which can help synchronize data collection and minimize latency. The factory default assigns DIO2 as a positive polarity data ready signal, which means that the data in the output registers is valid when the DIO2 line is high (see Figure 31). This configuration works well when DIO2 drives an interrupt service pin that activates on a low to high pulse.



Figure 31. Data Ready, When FNCTIO\_CTRL[3:0] = 1101 (default)

Use the following sequence to change this assignment to DIO1 with a negative polarity:

1. Turn to Page 3 (DIN = 0x8003).
2. Set FNCTIO\_CTRL[3:0] = 1000 (DIN = 0x8608, then DIN = 0x8700). The timing jitter on the pulse width of the data ready signal is typically ±1.4 μs.

**Input Sync/Clock Control**

FNCTIO\_CTRL[7:4] provide configuration options for using one of the DIOx lines as an input synchronization signal for sampling inertial sensor data. For example, use the following sequence to establish DIO4 as a positive polarity input clock pin and keep the factory default setting for the data ready function:

1. Turn to Page 3 (DIN = 0x8003).
2. Set FNCTIO\_CTRL[7:0] = 0xFD (DIN = 0x86FD).
3. Set FNCTIO\_CTRL[15:8] = 0x00 (DIN = 0x8700).

This command also disables the internal sampling clock. Therefore, no data sampling occurs if no input clock signal is present. The best performance is available when using an input clock frequency of 2400 Hz.

**Alarm Indicator**

FNCTIO\_CTRL[11:8] provide three configuration options for using one of the DIOx lines as an alarm indicator: on/off, polarity, and DIOx line. The primary purpose this signal is to provide an output signal that activates when a bit in the SYS\_E\_FLAG register = 1 (see Table 16). For example, use the following sequence to establish DIO3 as a negative polarity alarm indicator, while preserving the factory default setting for the data ready function:

1. Turn to Page 3 (DIN = 0x8003)
2. Set FNCTIO\_CTRL[7:0] = 0x0D (DIN = 0x860D).
3. Set FNCTIO\_CTRL[15:8] = 0x0A (DIN = 0x870A).

**GENERAL-PURPOSE I/O CONTROL (GPIO\_CTRL)**

**Table 154. GPIO\_CTRL Register Definitions<sup>1</sup>**

| Page | Addresses  | Default | Access | Flash Backup |
|------|------------|---------|--------|--------------|
| 0x03 | 0x08, 0x09 | 0x00X0  | R/W    | Yes          |

<sup>1</sup> The GPIO\_CTRL[7:4] bits reflect the logic levels on the DIOx lines and do not have a default setting.

**Table 155. GPIO\_CTRL Bit Definitions<sup>1</sup>**

| Bits   | Description   |
|--------|---|
| [15:8] | Don't care  |
| 7      | General-Purpose I/O Line 4 (DIO4) data level                                |
| 6      | General-Purpose I/O Line 3 (DIO3) data level                                |
| 5      | General-Purpose I/O Line 2 (DIO2) data level                                |
| 4      | General-Purpose I/O Line 1 (DIO1) data level                                |
| 3      | General-Purpose I/O Line 4 (DIO4) direction control (1 = output, 0 = input) |
| 2      | General-Purpose I/O Line 3 (DIO3) direction control (1 = output, 0 = input) |
| 1      | General-Purpose I/O Line 2 (DIO2) direction control (1 = output, 0 = input) |
| 0      | General-Purpose I/O Line 1 (DIO1) direction control (1 = output, 0 = input) |

<sup>1</sup> The GPIO\_CTRL[7:4] bits reflect the logic levels on the DIOx lines and do not have a default setting.

When FNCTIO\_CTRL does not configure a DIOx pin, GPIO\_CTRL provides register controls for general-purpose use of the pin. GPIO\_CTRL[3:0] provide input/output assignment controls for each line. When the DIOx lines are inputs, monitor their level by reading GPIO\_CTRL[7:4]. When the DIOx lines are used as outputs, set their level by writing to GPIO\_CTRL[7:4]. For example, use the following sequence to set DIO1 and DIO3 as high and low output lines, respectively, and set DIO2 and DIO4 as input lines. Turn to Page 3 (DIN = 0x8003) and set GPIO\_CTRL[7:0] = 0x15 (DIN = 0x8815, then DIN = 0x8900).

**MISCELLANEOUS CONFIGURATION (CONFIG)**

**Table 156. CONFIG Register Definitions**

| Page | Addresses  | Default | Access | Flash Backup |
|------|------------|---------|--------|--------------|
| 0x03 | 0x0A, 0x0B | 0x00C0  | R/W    | Yes          |

**Table 157. CONFIG Bit Definitions**

| Bits   | Description  |
|--------|--|
| [15:8] | Not used   |
| 7      | Linear g compensation for gyroscopes (1 = enabled)                         |
| 6      | Point of percussion alignment (1 = enabled)                                |
| [5:2]  | Not used   |
| 1      | Real-time clock, daylight savings time (1: enabled, 0: disabled)           |
| 0      | Real-time clock control (1: relative/elapsed timer mode, 0: calendar mode) |

The CONFIG register (see Table 156 and Table 157) provides configuration options for the linear g compensation in the gyroscopes (on/off), point of percussion alignment for the accelerometers (on/off), and the real-time clock function.

**Point of Percussion**

CONFIG[6] offers a point of percussion alignment function that maps the accelerometer sensors to the corner of the package identified in Figure 32. To activate this feature, turn to Page 3 (DIN = 0x8003), then set CONFIG[6] = 1 (DIN = 0x8A40, DIN = 0x8B00).

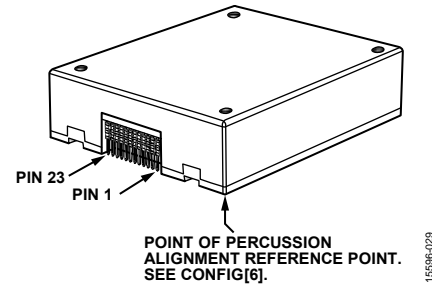


Figure 32. Point of Percussion Reference Point

**Linear Acceleration on Effect on Gyroscope Bias**

The ADIS16489 includes first-order compensation for the linear g effect in the gyroscopes, which uses the following model:

$$\begin{bmatrix} \omega_{XC} \\ \omega_{YC} \\ \omega_{ZC} \end{bmatrix} = \begin{bmatrix} LG_{11} & LG_{12} & LG_{13} \\ LG_{21} & LG_{22} & LG_{23} \\ LG_{31} & LG_{32} & LG_{33} \end{bmatrix} \times \begin{bmatrix} A_X \\ A_Y \\ A_Z \end{bmatrix} + \begin{bmatrix} \omega_{XPC} \\ \omega_{YPC} \\ \omega_{ZPC} \end{bmatrix}$$

The linear g correction factors, LG<sub>XY</sub>, apply correction for linear acceleration in all three directions to the data path of each gyroscope (ω<sub>XPC</sub>, ω<sub>YPC</sub>, and ω<sub>ZPC</sub>) at the rate of the data samples (2460 SPS when using the internal clock). CONFIG[7] provides an on/off control for this compensation. The factory default value for this bit activates this compensation. To turn it off, turn to Page 3 (DIN = 0x8003) and set CONFIG[7] = 0 (DIN = 0x8A40, DIN = 0x8B00). This command sequence also preserves the default setting for the point of percussion alignment function (on).

**DECIMATION FILTER (DEC\_RATE)**

**Table 158. DEC\_RATE Register Definitions**

| Page | Addresses  | Default | Access | Flash Backup |
|------|------------|---------|--------|--------------|
| 0x03 | 0x0C, 0x0D | 0x0000  | R/W    | Yes          |

**Table 159. DEC\_RATE Bit Definitions**

| Bits    | Description   |
|---------|---|
| [15:11] | Don't care  |
| [10:0]  | Decimation rate, binary format, maximum = 2047, see Figure 33 for the impact on sample rate |

The DEC\_RATE register (see Table 158 and Table 159) provides user control for the final filter stage (see Figure 33), which averages and decimates the accelerometers and gyroscopes data, while also extending the time that the delta angle and delta velocity track between each update. The output sample rate is equal to  $2460 / (\text{DEC\_RATE} + 1)$ . When using the external clock option (Bit 7 and Bits[5:4] of the FNCTIO\_CTRL register, see Figure 33), replace the 2460 number in this relationship with the input clock frequency. For example, turn to Page 3 (DIN = 0x8003), and set DEC\_RATE = 0x18 (DIN = 0x8C18, then DIN = 0x8D00) to reduce the output sample rate to 98.4 SPS ( $2460 \div 25$ ).

**CONTINUOUS BIAS ESTIMATION (NULL\_CNFG)**

**Table 160. NULL\_CNFG Register Definitions**

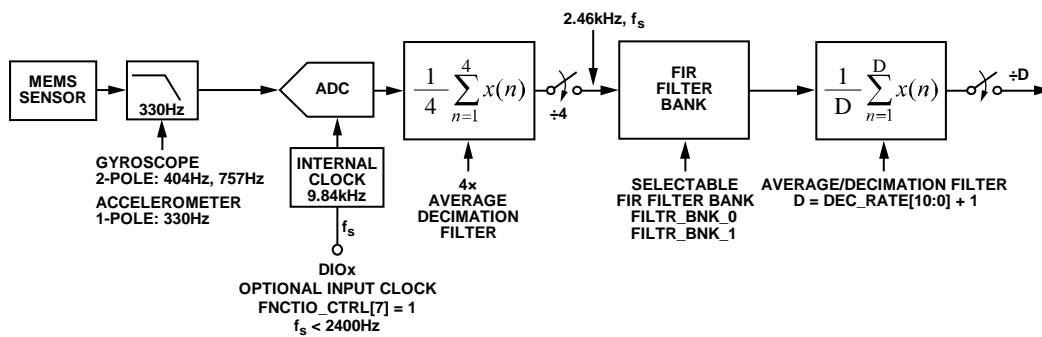
| Page | Addresses  | Default | Access | Flash Backup |
|------|------------|---------|--------|--------------|
| 0x03 | 0x0E, 0x0F | 0x070A  | R/W    | Yes          |

**Table 161. NULL\_CNFG Bit Definitions**

| Bits    | Description   |
|---------|---|
| [15:14] | Not used  |
| 13      | Z-axis acceleration bias correction enable (1 = enabled)  |
| 12      | Y-axis acceleration bias correction enable (1 = enabled)  |
| 11      | X-axis acceleration bias correction enable (1 = enabled)  |
| 10      | Z-axis gyroscope bias correction enable (1 = enabled)   |
| 9       | Y-axis gyroscope bias correction enable (1 = enabled)   |
| 8       | X-axis gyroscope bias correction enable (1 = enabled)   |
| [7:4]   | Not used  |
| [3:0]   | Time base control (TBC), range: 0 to 13 (default = 10); $t_B = 2^{\text{TBC}} / 2460$ , time base; $t_A = 64 \times t_B$ , average time |

The NULL\_CNFG register (see Table 160 and Table 161) provides the configuration controls for the CBE, which associates with the bias correction update command in GLOB\_CMD[0] (see Table 151). NULL\_CNFG[3:0] establish the total average time ( $t_A$ ) for the bias estimates and NULL\_CNFG[13:8] provide on/off controls for each sensor. The factory default configuration for NULL\_CNFG enables the bias null command for the gyroscopes, disables the bias null command for the accelerometers, and sets the average time to ~26.64 sec.

When a sensor bit in NULL\_CNFG is active (equal to 1), setting GLOB\_CMD[0] = 1 (DIN sequence: 0x8003, 0x8201, 0x8300) causes its bias correction register to automatically update with a value that corrects for its present bias error (from the CBE). For example, setting NULL\_CNFG[8] equal to 1 causes an update in the XG\_BIAS\_LOW (see Table 109) and XG\_BIAS\_HIGH (see Table 111) registers.



**NOTES**  
 1. WHEN FNCTIO\_CTRL[7] = 1, EACH CLOCK PULSE ON THE DESIGNATED DIOx LINE (FNCTIO\_CTRL[5:4]) STARTS A FOUR-SAMPLE BURST, AT A SAMPLE RATE OF 9.84kHz. THESE FOUR SAMPLES FEED INTO THE 4x AVERAGE/DECIMATION FILTER, WHICH PRODUCES A DATA RATE THAT IS EQUAL TO THE INPUT CLOCK FREQUENCY.

Figure 33. Sampling and Frequency Response Signal Flow

**POWER MANAGEMENT (SLP\_CNT)****Table 162. SLP\_CNT Register Definitions**

| Page | Addresses  | Default        | Access | Flash Backup |
|------|------------|----------------|--------|--------------|
| 0x03 | 0x10, 0x11 | Not applicable | W      | No           |

**Table 163. SLP\_CNT Bit Definitions**

| Bits    | Description  |
|---------|--|
| [15:10] | Not used   |
| 9       | Power-down mode                                      |
| 8       | Normal sleep mode                                    |
| [7:0]   | Programmable time bits; 1 sec/LSB; 0x00 = indefinite |

The SLP\_CNT register (see Table 162 and Table 163) provides controls for both power-down mode and sleep modes. The trade-off between power-down mode and sleep mode is idle power and recovery time. Power-down mode offers the best power consumption but requires the most time to recover. In addition, all volatile settings are lost during power-down, whereas sleep mode preserves these settings.

To initiate a sleep mode for a specific period of time, turn to Page 3 (DIN = 0x8003), write the amount of sleep time to SLP\_CNT[7:0] and then set SLP\_CNT[8] = 1 (DIN = 0x9101) to start the sleep period. Sleep mode begins when the  $\overline{CS}$  line goes high, after setting SLP\_CNT[8] = 1. See Table 164 for a command sequence example to place the ADIS16489 into sleep mode for 100 sec.

**Table 164. Command Sequence, Timed Sleep Mode Example**

| DIN    | Description                             |
|--------|---|
| 0x8003 | Turn to Page 3                          |
| 0x9064 | SLP_CNT[7:0] = 0x64, 100 sec sleep time |
| 0x9101 | SLP_CNT[8] = 1, start sleep mode        |

To initiate an indefinite sleep mode, set SLP\_CNT[7:0] = 0x00 (DIN = 0x9000), then set SLP\_CNT[8] = 1 (DIN = 0x9101). To initiate a power-down period of 100 sec, use the configuration sequence in Table 164, with one exception: set SLP\_CNT[9] = 1 (DIN = 0x9102) instead of setting SLP\_CNT[8] = 1 (DIN = 0x9101). To initiate an indefinite power-down, set SLP\_CNT[7:0] = 0x00 first, and then set SLP\_CNT[9] = 1 (DIN = 0x9102).

To wake the device from sleep or power-down mode, use one of the following options to restore normal operation:

- Assert  $\overline{CS}$  from high to low.
- Pulse RST low, then high again.
- Cycle the power.

If the sleep mode and power-down mode bits are both set high, the normal sleep mode bit (SLP\_CNT[8]) takes precedence.

**FIR FILTER CONTROL (FILTR\_BNK\_0, FILTR\_BNK\_1)****Table 165. FILTR\_BNK\_0 Register Definitions**

| Page | Addresses  | Default | Access | Flash Backup |
|------|------------|---------|--------|--------------|
| 0x03 | 0x16, 0x17 | 0x0000  | R/W    | Yes          |

**Table 166. FILTR\_BNK\_0 Bit Definitions**

| Bits    | Description   |
|---------|---|
| 15      | Don't care  |
| 14      | Y-axis accelerometer filter enable (1 = enabled)  |
| [13:12] | Y-axis accelerometer filter bank selection:<br>00 = Bank A, 01 = Bank B, 10 = Bank C, 11 = Bank D |
| 11      | X-axis accelerometer filter enable (1 = enabled)  |
| [10:9]  | X-axis accelerometer filter bank selection:<br>00 = Bank A, 01 = Bank B, 10 = Bank C, 11 = Bank D |
| 8       | Z-axis gyroscope filter enable (1 = enabled)  |
| [7:6]   | Z-axis gyroscope filter bank selection:<br>00 = Bank A, 01 = Bank B, 10 = Bank C, 11 = Bank D     |
| 5       | Y-axis gyroscope filter enable (1 = enabled)  |
| [4:3]   | Y-axis gyroscope filter bank selection:<br>00 = Bank A, 01 = Bank B, 10 = Bank C, 11 = Bank D     |
| 2       | X-axis gyroscope filter enable (1 = enabled)  |
| [1:0]   | X-axis gyroscope filter bank selection:<br>00 = Bank A, 01 = Bank B, 10 = Bank C, 11 = Bank D     |

**Table 167. FILTR\_BNK\_1 Register Definitions**

| Page | Addresses  | Default | Access | Flash Backup |
|------|------------|---------|--------|--------------|
| 0x03 | 0x18, 0x19 | 0x0000  | R/W    | Yes          |

**Table 168. FILTR\_BNK\_1 Bit Definitions**

| Bits   | Description   |
|--------|---|
| [15:3] | Don't care  |
| 2      | Z-axis accelerometer filter enable (1 = enabled)  |
| [1:0]  | Z-axis accelerometer filter bank selection:<br>00 = Bank A, 01 = Bank B, 10 = Bank C, 11 = Bank D |

The FILTR\_BNK\_0 (see Table 165 and Table 166) and FILTR\_BNK\_1 (see Table 167 and Table 168) registers provide the configuration controls for the FIR filter bank in the signal chain of each sensor (see Figure 33). These registers provide on/off control for the FIR bank for each inertial sensor, along with the FIR bank (A, B, C, D) that each sensor uses.

**ALARM CONFIGURATION (ALM\_CNFG\_0, ALM\_CNFG\_1, ALM\_CFG\_2)**

The ALM\_CNFG\_0 (see Table 169 and Table 170), ALM\_CNFG\_1 (see Table 171 and Table 172) and ALM\_CNFG\_2 (see Table 173 and Table 174) registers provide three configuration control options for the alarm functions of each inertial sensor and the barometer: on/off, polarity, and mode of operation (static/dynamic).

**Table 169. ALM\_CNFG\_0 Register Definitions**

| Page | Addresses  | Default | Access | Flash Backup |
|------|------------|---------|--------|--------------|
| 0x03 | 0x20, 0x21 | 0x0000  | R/W    | Yes          |

**Solving for  $\Delta X_{ACCL\_OUT}$ ,  $\Delta Z_{GYRO\_OUT}$ ,  $\Delta Y_{GYRO\_OUT}$ , and  $\Delta X_{GYRO\_OUT}$**

Use Equation 1 to Equation 4 to solve for  $\Delta X_{ACCL\_OUT}$ ,  $\Delta Z_{GYRO\_OUT}$ ,  $\Delta Y_{GYRO\_OUT}$ , and  $\Delta X_{GYRO\_OUT}$ , which the following bits provide user control for in the ALM\_CFG\_0 register (see Table 170) in Bits[13:12], Bits[9:8], Bits[5:4], and Bits[1:0].

$$\Delta X_{ACCL\_OUT} = \frac{1}{8} \left( \sum_{n=0}^7 X_A(n) - \sum_{n=0}^7 X_A(n-112) \right) \quad (1)$$

where  $X_A = X_{ACCL\_OUT}$ .

$$\Delta Z_{GYRO\_OUT} = \frac{1}{8} \left( \sum_{n=0}^7 Z_G(n) - \sum_{n=0}^7 Z_G(n-112) \right) \quad (2)$$

where  $Z_G = Z_{GYRO\_OUT}$ .

$$\Delta Y_{GYRO\_OUT} = \frac{1}{8} \left( \sum_{n=0}^7 Y_G(n) - \sum_{n=0}^7 Y_G(n-112) \right) \quad (3)$$

where  $Y_G = Y_{GYRO\_OUT}$ .

$$\Delta X_{GYRO\_OUT} = \frac{1}{8} \left( \sum_{n=0}^7 X_G(n) - \sum_{n=0}^7 X_G(n-112) \right) \quad (4)$$

where  $X_G = X_{GYRO\_OUT}$ .

**Table 170. ALM\_CNFG\_0 Bit Definitions**

| Bits    | Description  |
|---------|--|
| 15      | X-axis accelerometer; 0: alarm is off, 1: alarm is on  |
| 14      | Not used   |
| [13:12] | X-axis accelerometer polarity and mode settings; select one of the four options for the condition that triggers the alarm (ALM_STS[3] = 1, see Table 20)<br>00: $X_{ACCL\_OUT} < XA_{ALM\_MAGN}$<br>01: $\Delta X_{ACCL\_OUT} < XA_{ALM\_MAGN}$ (see Equation 1)<br>10: $X_{ACCL\_OUT} > XA_{ALM\_MAGN}$<br>11: $\Delta X_{ACCL\_OUT} > XA_{ALM\_MAGN}$ (see Equation 1) |
| 11      | Z-axis gyroscope; 0: alarm is off, 1: alarm is on  |
| 10      | Not used   |
| [9:8]   | Z-axis gyroscope polarity and mode settings; select one of the four options for the condition that triggers the alarm (ALM_STS[2] = 1, see Table 20)<br>00: $Z_{GYRO\_OUT} < ZG_{ALM\_MAGN}$<br>01: $\Delta Z_{GYRO\_OUT} < ZG_{ALM\_MAGN}$ (see Equation 2)<br>10: $Z_{GYRO\_OUT} > ZG_{ALM\_MAGN}$<br>11: $\Delta Z_{GYRO\_OUT} > ZG_{ALM\_MAGN}$ (see Equation 2)     |
| 7       | Y-axis gyroscope; 0: alarm is off, 1: alarm is on  |
| 6       | Not used   |
| [5:4]   | Y-axis gyroscope polarity and mode settings. Select one of the four options for the condition that triggers the alarm (ALM_STS[1] = 1, see Table 20)<br>00: $Y_{GYRO\_OUT} < YG_{ALM\_MAGN}$<br>01: $\Delta Y_{GYRO\_OUT} < YG_{ALM\_MAGN}$ (see Equation 3)<br>10: $Y_{GYRO\_OUT} > YG_{ALM\_MAGN}$<br>11: $\Delta Y_{GYRO\_OUT} > YG_{ALM\_MAGN}$ (see Equation 3)     |
| 3       | X-axis gyroscope; 0: alarm is off, 1: alarm is on  |

| Bits | Description   |
|------|---|
| 2    | Not used  |
| 1:0  | X-axis gyroscope polarity and mode settings; select one of the four options for the condition that triggers the alarm flag (ALM_STS[0] = 1, see Table 20)<br>00: $X_{GYRO\_OUT} < XG_{ALM\_MAGN}$<br>01: $\Delta X_{GYRO\_OUT} < XG_{ALM\_MAGN}$ (see Equation 4)<br>10: $X_{GYRO\_OUT} > XG_{ALM\_MAGN}$<br>11: $\Delta X_{GYRO\_OUT} > XG_{ALM\_MAGN}$ (see Equation 4) |

**Table 171. ALM\_CNFG\_1 Register Definitions**

| Page | Addresses  | Default | Access | Flash Backup |
|------|------------|---------|--------|--------------|
| 0x03 | 0x22, 0x23 | 0x0000  | R/W    | Yes          |

**Solving for  $\Delta Z_{ACCL\_OUT}$  and  $\Delta Y_{ACCL\_OUT}$**

Use Equation 5 and Equation 6 to solve for  $\Delta Z_{ACCL\_OUT}$  and  $\Delta Y_{ACCL\_OUT}$  in Bits[5:4] and Bits[1:0] in Table 172.

$$\Delta Z_{ACCL\_OUT} = \frac{1}{8} \left( \sum_{n=0}^7 Z_A(n) - \sum_{n=0}^7 Z_A(n-112) \right) \quad (5)$$

where  $Z_A = Z_{ACCL\_OUT}$ .

$$\Delta Y_{ACCL\_OUT} = \frac{1}{8} \left( \sum_{n=0}^7 Y_A(n) - \sum_{n=0}^7 Y_A(n-112) \right) \quad (6)$$

where  $Y_A = Y_{ACCL\_OUT}$ .

**Table 172. ALM\_CNFG\_1 Bit Definitions**

| Bits   | Description  |
|--------|--|
| [15:8] | Not used   |
| 7      | Z-axis accelerometer; 0: alarm is off, 1: alarm is on  |
| 6      | Not used   |
| [5:4]  | Z-axis accelerometer polarity and mode settings; select one of the four options for the condition that triggers the alarm (ALM_STS[5] = 1, see Table 20)<br>00: $Z_{ACCL\_OUT} < ZA_{ALM\_MAGN}$<br>01: $\Delta Z_{ACCL\_OUT} < ZA_{ALM\_MAGN}$ (see Equation 5)<br>10: $Z_{ACCL\_OUT} > ZA_{ALM\_MAGN}$<br>11: $\Delta Z_{ACCL\_OUT} > ZA_{ALM\_MAGN}$ (see Equation 5) |
| 4      | Z-axis accelerometer mode, 0: static, 1: dynamic   |
| 3      | Y-axis accelerometer; 0: alarm is off, 1: alarm is on  |
| 2      | Not used   |
| [1:0]  | Y-axis accelerometer polarity and mode settings; select one of the four options for the condition that triggers the alarm (ALM_STS[4] = 1, see Table 20)<br>00: $Y_{ACCL\_OUT} < YA_{ALM\_MAGN}$<br>01: $\Delta Y_{ACCL\_OUT} < YA_{ALM\_MAGN}$ (see Equation 6)<br>10: $Y_{ACCL\_OUT} > YA_{ALM\_MAGN}$<br>11: $\Delta Y_{ACCL\_OUT} > YA_{ALM\_MAGN}$ (see Equation 6) |

**Table 173. ALM\_CNFG\_2 Register Definitions**

| Page | Addresses  | Default | Access | Flash Backup |
|------|------------|---------|--------|--------------|
| 0x03 | 0x24, 0x25 | 0x0000  | R/W    | Yes          |

Table 174. ALM\_CNFG\_2

| Bits   | Description                                 |
|--------|---|
| [15:8] | Not used                                    |
| 7      | Barometer alarm (1 = enabled)               |
| 6      | Not used                                    |
| 5      | Barometer alarm polarity (1 = greater than) |
| 4      | Barometer dynamic enable (1 = enabled)      |
| [3:0]  | Not used                                    |

**X-AXIS GYROSCOPE ALARM (XG\_ALM\_MAGN)**

Table 175. XG\_ALM\_MAGN Register Definitions

| Page | Addresses  | Default | Access | Flash Backup |
|------|------------|---------|--------|--------------|
| 0x03 | 0x28, 0x29 | 0x0000  | R/W    | Yes          |

Table 176. XG\_ALM\_MAGN Bit Definitions

| Bits   | Description  |
|--------|--|
| [15:0] | X-axis gyroscope alarm threshold settings, twos complement, 0°/sec = 0x0000, 1 LSB = 0.02°/sec |

The XG\_ALM\_MAGN register (see Table 175 and Table 176) contains the alarm threshold for the x-axis gyroscope, when ALM\_CNFG\_0[3] = 1 (see Table 170). This alarm is associated with the alarm flag in ALM\_STS[0] (see Table 20).

**Alarm Example**

Table 177 provides a list of commands that configure the x-axis gyroscopes alarm to be active (ALM\_STS[0] = 1) when the rate of rotation around the x-axis exceeds 100°/sec. The value for the XG\_ALM\_MAGN register is 0x1388, as follows:

$$100^\circ/\text{sec} \div 0.02^\circ/\text{sec}/\text{LSB} = 5000 \text{ LSB} = 0x1388$$

Table 177. Configuration Commands, Alarm Example

| DIN    | Description              |
|--------|--------------------------|
| 0x8003 | Turn to page 3           |
| 0xA888 | XG_ALM_MAGN[7:0] = 0x88  |
| 0xA913 | XG_ALM_MAGN[15:8] = 0x13 |
| 0xA00C | ALM_CNFG_1[7:0] = 0x0C   |
| 0xA100 | ALM_CNFG_1[15:8] = 0x00  |

**Y-AXIS GYROSCOPE ALARM (YG\_ALM\_MAGN)**

Table 178. YG\_ALM\_MAGN Register Definitions

| Page | Addresses  | Default | Access | Flash Backup |
|------|------------|---------|--------|--------------|
| 0x03 | 0x2A, 0x2B | 0x0000  | R/W    | Yes          |

Table 179. YG\_ALM\_MAGN Bit Definitions

| Bits   | Description  |
|--------|--|
| [15:0] | Y-axis gyroscope alarm threshold settings, twos complement, 0°/sec = 0x0000, 1 LSB = 0.02°/sec |

The YG\_ALM\_MAGN register (see Table 178 and Table 179) contains the alarm threshold for the y-axis gyroscope, when ALM\_CNFG\_0[7] = 1 (see Table 170). This alarm is associated with the alarm flag in ALM\_STS[1] (see Table 20).

**Z-AXIS GYROSCOPE ALARM (ZG\_ALM\_MAGN)**

Table 180. ZG\_ALM\_MAGN Register Definitions

| Page | Addresses  | Default | Access | Flash Backup |
|------|------------|---------|--------|--------------|
| 0x03 | 0x2C, 0x2D | 0x0000  | R/W    | Yes          |

Table 181. ZG\_ALM\_MAGN Bit Definitions

| Bits   | Description  |
|--------|--|
| [15:0] | Z-axis gyroscope alarm threshold settings, twos complement, 0°/sec = 0x0000, 1 LSB = 0.02°/sec |

The ZG\_ALM\_MAGN register (see Table 180 and Table 181) contains the alarm threshold for the z-axis gyroscope, when ALM\_CNFG\_0[11] = 1 (see Table 170). This alarm is associated with the alarm flag in ALM\_STS[2] (see Table 20).

**X-AXIS ACCELEROMETER ALARM (XA\_ALM\_MAGN)**

Table 182. XA\_ALM\_MAGN Register Definitions

| Page | Addresses  | Default | Access | Flash Backup |
|------|------------|---------|--------|--------------|
| 0x03 | 0x2E, 0x2F | 0x0000  | R/W    | Yes          |

Table 183. XA\_ALM\_MAGN Bit Definitions

| Bits   | Description   |
|--------|---|
| [15:0] | X-axis accelerometer alarm threshold settings, twos complement, 0 g = 0x0000, 1 LSB = 0.25 mg |

The XA\_ALM\_MAGN register (see Table 182 and Table 183) contains the alarm threshold for the x-axis accelerometer, when ALM\_CNFG\_0[15] = 1 (see Table 170). This alarm is associated with the alarm flag in ALM\_STS[3] (see Table 20).

**Y-AXIS ACCELEROMETER ALARM (YA\_ALM\_MAGN)**

Table 184. YA\_ALM\_MAGN Register Definitions

| Page | Addresses  | Default | Access | Flash Backup |
|------|------------|---------|--------|--------------|
| 0x03 | 0x30, 0x31 | 0x0000  | R/W    | Yes          |

Table 185. YA\_ALM\_MAGN Bit Definitions

| Bits   | Description   |
|--------|---|
| [15:0] | Y-axis accelerometer alarm threshold settings, twos complement, 0 g = 0x0000, 1 LSB = 0.25 mg |

The YA\_ALM\_MAGN register (see Table 184 and Table 185) contains the alarm threshold for the y-axis accelerometer, when ALM\_CNFG\_1[3] = 1 (see Table 172). This alarm is associated with the alarm flag in ALM\_STS[4] (see Table 20).



**Z-AXIS ACCELEROMETER ALARM (ZA\_ALM\_MAGN)**

Table 186. ZA\_ALM\_MAGN Register Definitions

| Page | Addresses  | Default | Access | Flash Backup |
|------|------------|---------|--------|--------------|
| 0x03 | 0x32, 0x33 | 0x0000  | R/W    | Yes          |

Table 187. ZA\_ALM\_MAGN Bit Definitions

| Bits   | Description   |
|--------|---|
| [15:0] | Z-axis accelerometer alarm threshold settings, twos complement, 0 g = 0x0000, 1 LSB = 0.25 mg |

The ZA\_ALM\_MAGN register (see Table 186 and Table 187) contains the alarm threshold for the z-axis accelerometer, when ALM\_CNFG\_1[7] = 1 (see Table 172). This alarm is associated with the alarm flag in ALM\_STS[5] (see Table 20).

**BAROMETER ALARM (BR\_ALM\_MAGN)**

Table 188. BR\_ALM\_MAGN Register Definitions

| Page | Addresses  | Default | Access | Flash Backup |
|------|------------|---------|--------|--------------|
| 0x03 | 0x3A, 0x3B | 0x0000  | R/W    | Yes          |

Table 189. BR\_ALM\_MAGN Bit Definitions

| Bits   | Description  |
|--------|--|
| [15:0] | Barometer alarm threshold settings, twos complement, 0 g = 0x0000, 1 LSB = 40 μbar |

The BR\_ALM\_MAGN register (see Table 188 and Table 189) contains the alarm threshold for barometer, when ALM\_CNFG\_2[7] = 1 (see Table 174). This alarm is associated with the alarm flag in ALM\_STS[11] (see Table 20).

**FIRMWARE REVISION (FIRM\_REV)**

Table 190. FIRM\_REV Register Definitions

| Page | Addresses  | Default        | Access | Flash Backup |
|------|------------|----------------|--------|--------------|
| 0x03 | 0x78, 0x79 | Not applicable | R      | Yes          |

Table 191. FIRM\_REV Bit Definitions

| Bits    | Description  |
|---------|--|
| [15:12] | Firmware revision binary coded decimal (BCD) code, tens digit, numerical format = 4-bit binary, range = 0 to 9 |
| [11:8]  | Firmware revision BCD code, ones digit, numerical format = 4-bit binary, range = 0 to 9                        |
| [7:4]   | Firmware revision BCD code, tenths digit, numerical format = 4-bit binary, range = 0 to 9                      |
| [3:0]   | Firmware revision BCD code, hundredths digit, numerical format = 4-bit binary, range = 0 to 9                  |

The FIRM\_REV register (see Table 190 and Table 191) provides the firmware revision for the internal firmware. This register uses a BCD format, where each nibble represents a digit. For example, if FIRM\_REV = 0x1234, the firmware revision is 12.34.

**FIRMWARE REVISION DAY AND MONTH (FIRM\_DM)**

Table 192. FIRM\_DM Register Definitions

| Page | Addresses  | Default        | Access | Flash Backup |
|------|------------|----------------|--------|--------------|
| 0x03 | 0x7A, 0x7B | Not applicable | R      | Yes          |

Table 193. FIRM\_DM Bit Definitions

| Bits    | Description   |
|---------|---|
| [15:12] | Factory configuration month BCD code, tens digit, numerical format = 4-bit binary, range = 0 to 2 |
| [11:8]  | Factory configuration month BCD code, ones digit, numerical format = 4-bit binary, range = 0 to 9 |
| [7:4]   | Factory configuration day BCD code, tens digit, numerical format = 4-bit binary, range = 0 to 3   |
| [3:0]   | Factory configuration day BCD code, ones digit, numerical format = 4-bit binary, range = 0 to 9   |

The FIRM\_DM register (see Table 192 and Table 193) contains the month and day of the factory configuration date. FIRM\_DM[15:12] and FIRM\_DM[11:8] contain digits that represent the month of the factory configuration in a BCD format. For example, November is the 11<sup>th</sup> month in a year and is represented by FIRM\_DM[15:8] = 0x11. FIRM\_DM[7:4] and FIRM\_DM[3:0] contain digits that represent the day of factory configuration in a BCD format. For example, the 27<sup>th</sup> day of the month is represented by FIRM\_DM[7:0] = 0x27.

**FIRMWARE REVISION YEAR (FIRM\_Y)**

Table 194. FIRM\_Y Register Definitions

| Page | Addresses  | Default        | Access | Flash Backup |
|------|------------|----------------|--------|--------------|
| 0x03 | 0x7C, 0x7D | Not applicable | R      | Yes          |

Table 195. FIRM\_Y Bit Definitions

| Bits    | Description   |
|---------|---|
| [15:12] | Factory configuration year BCD code, thousands digit, numerical format = 4-bit binary, range = 0 to 9 |
| [11:8]  | Factory configuration year BCD code, hundreds digit, numerical format = 4-bit binary, range = 0 to 9  |
| [7:4]   | Factory configuration year BCD code, tens digit, numerical format = 4-bit binary, range = 0 to 3      |
| [3:0]   | Factory configuration year BCD code, ones digit, numerical format = 4-bit binary, range = 0 to 9      |

The FIRM\_Y register (see Table 194 and Table 195) contains the year of the factory configuration date. For example, the year, 2013, is represented by FIRM\_Y = 0x2013.

**PAGE 4 (PAGE\_ID)**

Table 196. PAGE\_ID Register Definition

| Page | Addresses  | Default | Access | Flash Backup |
|------|------------|---------|--------|--------------|
| 0x04 | 0x00, 0x01 | 0x0000  | R/W    | No           |

Table 197. PAGE\_ID Bit Assignments

| Bits   | Description                          |
|--------|--------------------------------------|
| [15:0] | Page number, binary numerical format |

The contents in the PAGE\_ID register (see Table 196 and Table 197) contain the current page setting, and provide a control for selecting another page for SPI access. For example, set DIN = 0x8002 to select Page 2 for SPI-based user access. See Table 10 for the page assignments associated with each user accessible register.

**PART IDENTIFICATION NUMBERS (PART\_ID1, PART\_ID2, PART\_ID3, PART\_ID4)**

**Table 198. PART\_ID1 Register Definitions**

| Page | Addresses  | Default        | Access | Flash Backup   |
|------|------------|----------------|--------|----------------|
| 0x04 | 0x20, 0x21 | Not applicable | R      | Not applicable |

**Table 199. PART\_ID1 Bit Definitions**

| Bits   | Description           |
|--------|-----------------------|
| [15:0] | Part Identification 1 |

**Table 200. PART\_ID2 Register Definitions**

| Page | Addresses  | Default        | Access | Flash Backup   |
|------|------------|----------------|--------|----------------|
| 0x04 | 0x22, 0x23 | Not applicable | R      | Not applicable |

**Table 201. PART\_ID2 Bit Definitions**

| Bits   | Description           |
|--------|-----------------------|
| [15:0] | Part Identification 2 |

**Table 202. PART\_ID3 Register Definitions**

| Page | Addresses  | Default        | Access | Flash Backup   |
|------|------------|----------------|--------|----------------|
| 0x04 | 0x24, 0x25 | Not applicable | R      | Not applicable |

**Table 203. PART\_ID3 Bit Definitions**

| Bits   | Description           |
|--------|-----------------------|
| [15:0] | Part Identification 3 |

**Table 204. PART\_ID4 Register Definitions**

| Page | Addresses  | Default        | Access | Flash Backup   |
|------|------------|----------------|--------|----------------|
| 0x04 | 0x26, 0x27 | Not applicable | R      | Not applicable |

**Table 205. PART\_ID4 Bit Definitions**

| Bits   | Description           |
|--------|-----------------------|
| [15:0] | Part Identification 4 |

**FIR FILTERS**

The ADIS16489 provides four FIR filter banks to configure and selection for each individual inertial sensor, using the FILTR\_BNK\_0 (see Table 166) and FILTR\_BNK\_1 (see Table 168) registers (see Figure 33). Each FIR filter bank (A, B, C, D) has 120 taps that consume two pages of memory. The coefficient associated with each tap, in each filter bank, has its own dedicated register that uses a 16-bit, twos complement format. The FIR filter has unity gain when the sum of all of the coefficients is equal to 32,768. For filter designs that require less than 120 taps, write 0x0000 to all unused registers to eliminate the latency associated with that particular tap.

**Page 5, Page 6 (PAGE\_ID)**

**Table 206. PAGE\_ID Register Definition**

| Page        | Addresses  | Default | Access | Flash Backup |
|-------------|------------|---------|--------|--------------|
| 0x05, 0x06, | 0x00, 0x01 | 0x0000  | R/W    | No           |

**Table 207. PAGE\_ID Bit Assignments**

| Bits   | Description                          |
|--------|--------------------------------------|
| [15:0] | Page number, binary numerical format |

The contents in the PAGE\_ID register (see Table 206 and Table 207) contain the current page setting, and provide a control for selecting another page for SPI access. For example, set DIN = 0x8002 to select Page 2 for SPI-based user access. See Table 10 for the page assignments associated with each user accessible register.

**FIR Filter Bank A (FIR\_COEF\_A000 to FIR\_COEF\_A119)**

**Table 208. FIR Filter Bank A Memory Map**

| Page | PAGE_ID | Addresses    | Register                       |
|------|---------|--------------|--------------------------------|
| 5    | 0x05    | 0x00, 0x01   | PAGE_ID                        |
| 5    | 0x05    | 0x02 to 0x07 | Not used                       |
| 5    | 0x05    | 0x08, 0x09   | FIR_COEF_A000                  |
| 5    | 0x05    | 0x0A, 0x0B   | FIR_COEF_A001                  |
| 5    | 0x05    | 0x0C to 0x7D | FIR_COEF_A002 to FIR_COEF_A058 |
| 5    | 0x05    | 0x7E, 0x7F   | FIR_COEF_A059                  |
| 6    | 0x06    | 0x00, 0x01   | PAGE_ID                        |
| 6    | 0x06    | 0x02 to 0x07 | Not used                       |
| 6    | 0x06    | 0x08, 0x09   | FIR_COEF_A060                  |
| 6    | 0x06    | 0x0A, 0x0B   | FIR_COEF_A061                  |
| 6    | 0x06    | 0x0C to 0x7D | FIR_COEF_A062 to FIR_COEF_A118 |
| 6    | 0x06    | 0x7E, 0x7F   | FIR_COEF_A119                  |

Table 209 and Table 210 offer detailed register and bit definitions for one of the FIR coefficient registers in Bank A, FIR\_COEF\_A071. Table 211 provides a configuration example, which sets this register to a decimal value of -169 (0xFF57).

**Table 209. FIR\_COEF\_A071 Register Definitions**

| Page | Addresses  | Default        | Access | Flash Backup |
|------|------------|----------------|--------|--------------|
| 0x06 | 0x1E, 0x1F | Not applicable | R/W    | Yes          |

**Table 210. FIR\_COEF\_A071 Bit Definitions**

| Bits   | Description                                 |
|--------|---|
| [15:0] | FIR Bank A, Coefficient 71, twos complement |

**Table 211. Configuration Example, FIR Coefficient**

| DIN    | Description                |
|--------|----------------------------|
| 0x8006 | Turn to Page 6             |
| 0x9E57 | FIR_COEF_A071[7:0] = 0x57  |
| 0x9FFF | FIR_COEF_A071[15:8] = 0xFF |

**Page 7, Page 8 (PAGE\_ID)**

Table 212. PAGE\_ID Register Definition

| Page        | Addresses  | Default | Access | Flash Backup |
|-------------|------------|---------|--------|--------------|
| 0x07, 0x08, | 0x00, 0x01 | 0x0000  | R/W    | No           |

Table 213. PAGE\_ID Bit Assignments

| Bits   | Description                          |
|--------|--------------------------------------|
| [15:0] | Page number, binary numerical format |

The contents in the PAGE\_ID register (see Table 212 and Table 213) contain the current page setting, and provide a control for selecting another page for SPI access. For example, set DIN = 0x8002 to select Page 2 for SPI-based user access. See Table 10 for the page assignments associated with each user accessible register.

**FIR Filter Bank B (FIR\_COEF\_B000 to FIR\_COEF\_B119)**

Table 214. Filter Bank B Memory Map

| Page | PAGE_ID | Addresses    | Register                          |
|------|---------|--------------|-----------------------------------|
| 7    | 0x07    | 0x00, 0x01   | PAGE_ID                           |
| 7    | 0x07    | 0x02 to 0x07 | Not used                          |
| 7    | 0x07    | 0x08, 0x09   | FIR_COEF_B000                     |
| 7    | 0x07    | 0x0A, 0x0B   | FIR_COEF_B001                     |
| 7    | 0x07    | 0x0C to 0x7D | FIR_COEF_B002 to<br>FIR_COEF_B058 |
| 7    | 0x07    | 0x7E, 0x7F   | FIR_COEF_B059                     |
| 8    | 0x08    | 0x00, 0x01   | PAGE_ID                           |
| 8    | 0x08    | 0x02 to 0x07 | Not used                          |
| 8    | 0x08    | 0x08, 0x09   | FIR_COEF_B060                     |
| 8    | 0x08    | 0x0A, 0x0B   | FIR_COEF_B061                     |
| 8    | 0x08    | 0x0C to 0x7D | FIR_COEF_B062 to<br>FIR_COEF_B118 |
| 8    | 0x08    | 0x7E, 0x7F   | FIR_COEF_B119                     |

**Page 9, Page 10 (PAGE\_ID)**

Table 215. PAGE\_ID Register Definition

| Page        | Addresses  | Default | Access | Flash Backup |
|-------------|------------|---------|--------|--------------|
| 0x09, 0x0A, | 0x00, 0x01 | 0x0000  | R/W    | No           |

Table 216. PAGE\_ID Bit Assignments

| Bits   | Description                          |
|--------|--------------------------------------|
| [15:0] | Page number, binary numerical format |

The contents in the PAGE\_ID register (see Table 215 and Table 216) contain the current page setting, and provide a control for selecting another page for SPI access. For example, set DIN = 0x8002 to select Page 2 for SPI-based user access. See Table 10 for the page assignments associated with each user accessible register.

**FIR Filter Bank C (FIR\_COEF\_C000 to FIR\_COEF\_C119)**

Table 217. Filter Bank C Memory Map

| Page | PAGE_ID | Addresses    | Register                          |
|------|---------|--------------|-----------------------------------|
| 9    | 0x09    | 0x00, 0x01   | PAGE_ID                           |
| 9    | 0x09    | 0x02 to 0x07 | Not used                          |
| 9    | 0x09    | 0x08, 0x09   | FIR_COEF_C000                     |
| 9    | 0x09    | 0x0A, 0x0B   | FIR_COEF_C001                     |
| 9    | 0x09    | 0x0C to 0x7D | FIR_COEF_C002 to<br>FIR_COEF_C058 |
| 9    | 0x09    | 0x7E, 0x7F   | FIR_COEF_C059                     |
| 10   | 0x0A    | 0x00, 0x01   | PAGE_ID                           |
| 10   | 0x0A    | 0x02 to 0x07 | Not used                          |
| 10   | 0x0A    | 0x08, 0x09   | FIR_COEF_C060                     |
| 10   | 0x0A    | 0x0A, 0x0B   | FIR_COEF_C061                     |
| 10   | 0x0A    | 0x0C to 0x7D | FIR_COEF_C062 to<br>FIR_COEF_C118 |
| 10   | 0x0A    | 0x7E, 0x7F   | FIR_COEF_C119                     |

**Page 11, Page 12 (PAGE\_ID)**

Table 218. PAGE\_ID Register Definition

| Page        | Addresses  | Default | Access | Flash Backup |
|-------------|------------|---------|--------|--------------|
| 0x0B, 0x0C, | 0x00, 0x01 | 0x0000  | R/W    | No           |

Table 219. PAGE\_ID Bit Assignments

| Bits   | Description                          |
|--------|--------------------------------------|
| [15:0] | Page number, binary numerical format |

The contents in the PAGE\_ID register (see Table 218 and Table 219) contain the current page setting, and provide a control for selecting another page for SPI access. For example, set DIN = 0x8002 to select Page 2 for SPI-based user access. See Table 10 for the page assignments associated with each user accessible register.

**FIR Filter Bank D (FIR\_COEF\_D000 to FIR\_COEF\_D119)**

Table 220. Filter Bank D Memory Map

| Page | PAGE_ID | Addresses    | Register                          |
|------|---------|--------------|-----------------------------------|
| 11   | 0x0B    | 0x00, 0x01   | PAGE_ID                           |
| 11   | 0x0B    | 0x02 to 0x07 | Not used                          |
| 11   | 0x0B    | 0x08, 0x09   | FIR_COEF_D000                     |
| 11   | 0x0B    | 0x0A, 0x0B   | FIR_COEF_D001                     |
| 11   | 0x0B    | 0x0C to 0x7D | FIR_COEF_D002 to<br>FIR_COEF_D058 |
| 11   | 0x0B    | 0x7E, 0x7F   | FIR_COEF_D059                     |
| 12   | 0x0C    | 0x00, 0x01   | PAGE_ID                           |
| 12   | 0x0C    | 0x02 to 0x07 | Not used                          |
| 12   | 0x0C    | 0x08, 0x09   | FIR_COEF_D060                     |
| 12   | 0x0C    | 0x0A, 0x0B   | FIR_COEF_D061                     |
| 12   | 0x0C    | 0x0C to 0x7D | FIR_COEF_D062 to<br>FIR_COEF_D118 |
| 12   | 0x0C    | 0x7E, 0x7F   | FIR_COEF_D119                     |

**Default Filter Performance**

The FIR filter banks have factory programmed filter designs. They are all low-pass filters that have unity dc gain. Table 221 provides a summary of each filter design, and Figure 34 shows the frequency response characteristics. The phase delay is equal to 1/2 of the total number of taps.

**Table 221. FIR Filter Descriptions, Default Configuration**

| FIR Filter Bank | Taps | -3 dB Frequency (Hz) |
|-----------------|------|----------------------|
| A               | 120  | 310                  |
| B               | 120  | 55                   |
| C               | 32   | 275                  |
| D               | 32   | 63                   |

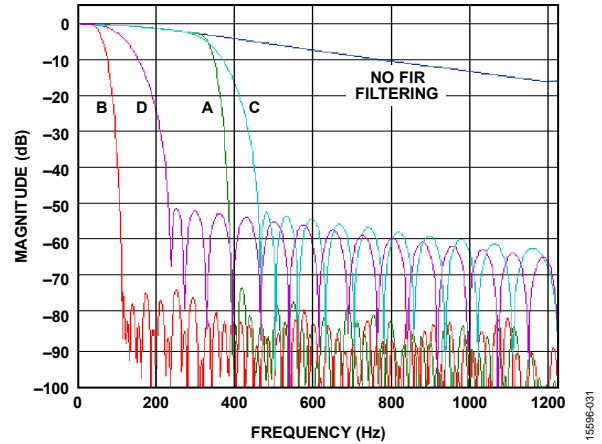


Figure 34. FIR Filter Frequency Response Curves

16586-031

# APPLICATIONS INFORMATION

## MOUNTING BEST PRACTICES

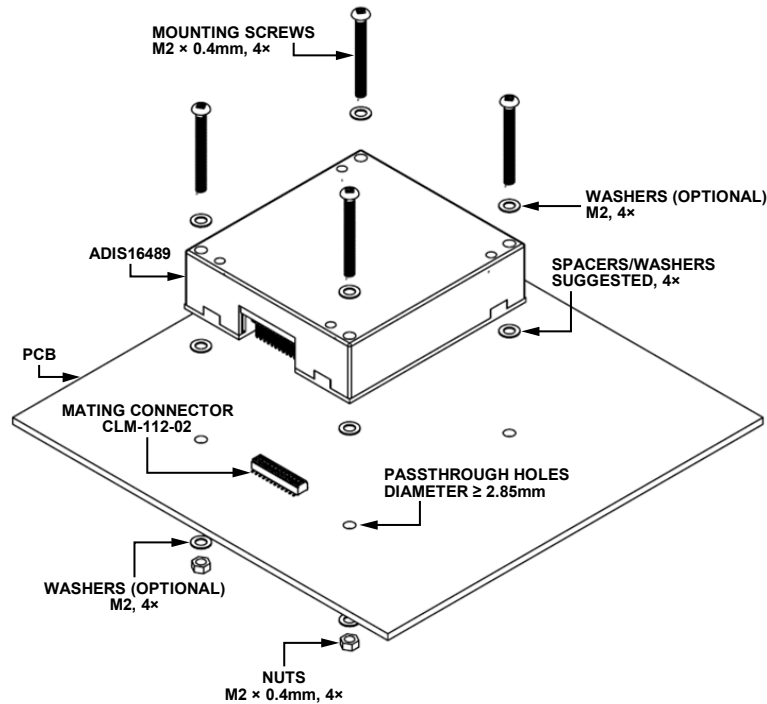


Figure 35. Mounting Example

For best performance, follow these simple rules when installing the ADIS16489 into a system:

- Eliminate opportunity for translational force (x- and y-axis direction, per Figure 20) application on the electrical connector.
- Isolate the mounting force to the four corners on the portion of the package surface that surrounds the mounting holes.
- Use uniform mounting forces on all four corners. The suggested torque setting is 40 inch ounces (0.285 Nm).

These three rules help prevent irregular force profiles, which can warp the package and introduce bias errors in the sensors. Figure 35 provides an example that leverages washers to set the package off the mounting surface and uses 2.85 mm passthrough holes and backside washers/nuts for attachment. Figure 36 and Figure 37 provide details for mounting hole and connector alignment pin drill locations.

For more information on mounting the ADIS16489, see the AN-1295 Application Note.

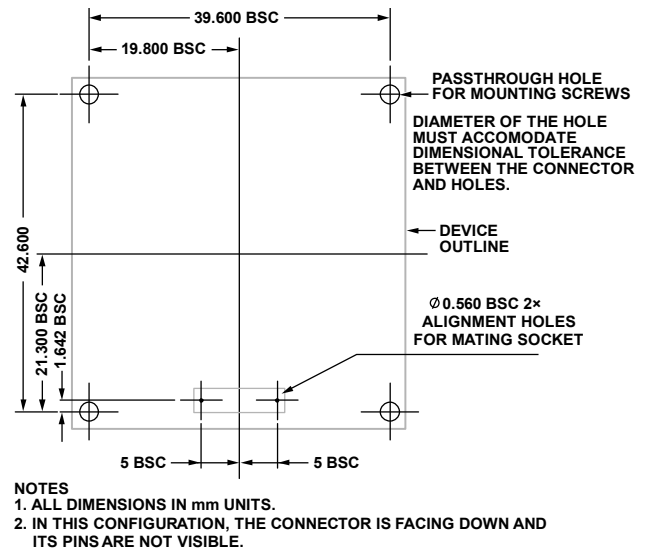


Figure 36. Suggested PCB Layout Pattern, Connector Down

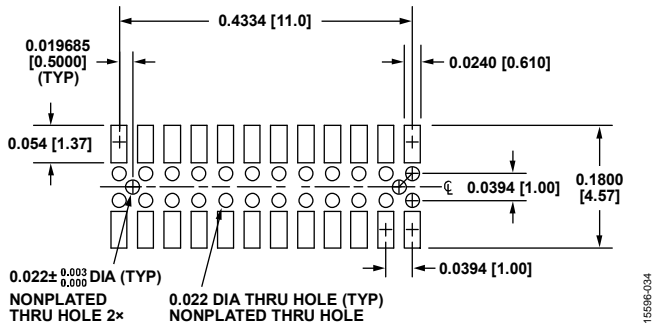


Figure 37. Suggested Layout and Mechanical Design When Using Samtec CLM-112-02-G-D-A for the Mating Connector

**EVALUATION TOOLS**

**Breakout Board, ADIS16IMU1/PCBZ**

The ADIS16IMU1/PCBZ (sold separately) provides a breakout board function for the ADIS16489, which means that it provides access to the ADIS16489 through larger connectors that support standard 1 mm ribbon cabling. It also provides four mounting holes for attachment of the ADIS16489 to the breakout board.

**PC-Based Evaluation, EVAL-ADIS**

The EVAL-ADIS provides the system support PC-based evaluation of the ADIS16489.

**POWER SUPPLY CONSIDERATIONS**

The VDD power supply must charge 24  $\mu$ F of capacitance (inside of the ADIS16489, across the VDD and GND pins) during its initial ramp and settling process. When VDD reaches 2.85 V, the ADIS16489 begins its internal start-up process, which generates additional transient current demand. See Figure 38 for a typical current profile during the start-up process. The first peak in Figure 38 relates to charging the 24  $\mu$ F capacitor bank, whereas the second peak (~360 ms after the first peak) relates to the initialization process of the ADIS16489. See Figure 39 for a close view of the current profile associated with the second peak in Figure 38.

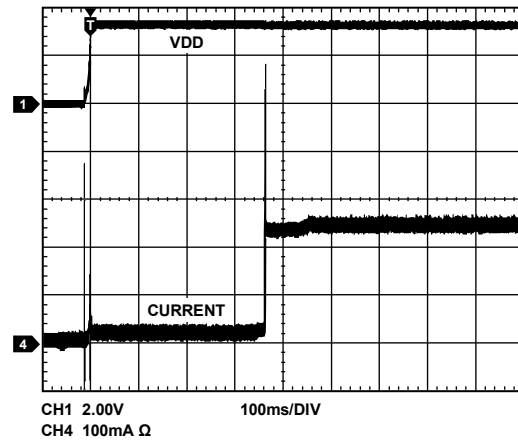


Figure 38. Transient Current Demand, Startup

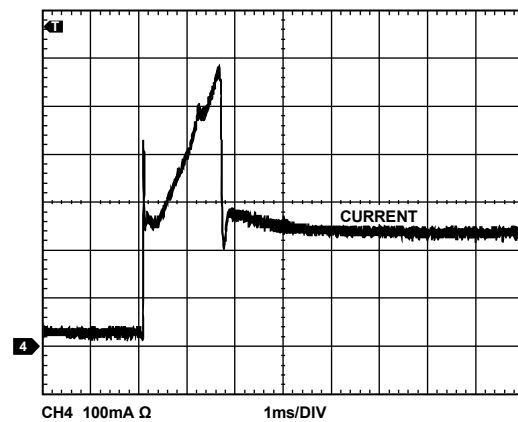


Figure 39. Transient Current Demand, Peak Demand

**X-RAY SENSITIVITY**

Exposure to high dose rate X-rays, such as those in production systems that inspect solder joints in electronic assemblies, can affect accelerometer bias errors. For optimal performance, avoid exposing the ADIS16489A to this type of inspection.

# PACKAGING AND ORDERING INFORMATION

## OUTLINE DIMENSIONS

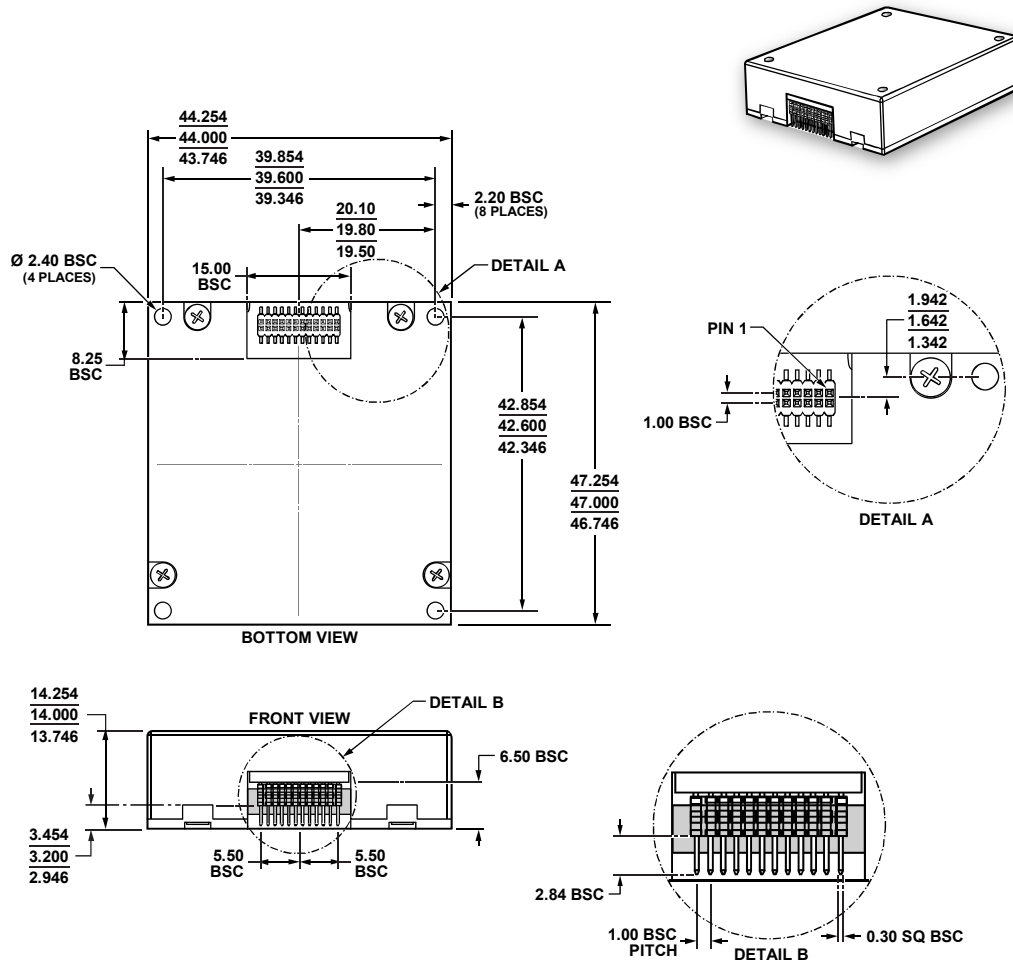


Figure 40. 24-Lead Module with Connector Interface [MODULE]  
(ML-24-6)  
Dimensions shown in millimeters

12-07-2012-E

### ORDERING GUIDE

| Model <sup>1</sup> | Temperature Range | Package Description                              | Package Option |
|--------------------|-------------------|--|----------------|
| ADIS16489BMLZ-P    | -40°C to +105°C   | 24-Lead Module with Connector Interface [MODULE] | ML-24-6        |

<sup>1</sup> Z = RoHS Compliant Part.



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- Защита от снятия компонента с производства.



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