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**HV7358DB1
User's Guide**

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Preface

NOTICE TO CUSTOMERS

All documentation becomes dated, and this manual is no exception. Microchip tools and documentation are constantly evolving to meet customer needs, so some actual dialogs and/or tool descriptions may differ from those in this document. Please refer to our website (www.microchip.com) to obtain the latest documentation available.

Documents are identified with a “DS” number. This number is located on the bottom of each page, in front of the page number. The numbering convention for the DS number is “DSXXXXA”, where “XXXX” is the document number and “A” is the revision level of the document.

For the most up-to-date information on development tools, see the MPLAB® IDE online help. Select the Help menu, and then Topics to open a list of available online help files.

INTRODUCTION

This chapter contains general information that will be useful to know before using the HV7358DB1. Items discussed in this chapter include:

- [Document Layout](#)
- [Conventions Used in this Guide](#)
- [Recommended Reading](#)
- [The Microchip Website](#)
- [Customer Support](#)
- [Document Revision History](#)

DOCUMENT LAYOUT

This document describes how to use the HV7358DB1 User's Guide as a development tool. The document is organized as follows:

- **Chapter 1. “HV7358 Overview”** – Important information about the HV7358DB1 User's Guide.
- **Chapter 2. “HV7358 Overview”** – This chapter includes a detailed description of installing the required USB driver and GUI program to your computer.
- **Chapter 3. “HV7358DB1 GUI Operation”** – This chapter includes a detailed description of each function of the demonstration board and instructions for how to begin using the HV7358 Evaluation Board.
- **Chapter 4. “MUPB002 FPGA Configuration”** – This chapter explains how to load software into the FPGA on the MPUB002.
- **Chapter 5. “PCB Design and Layout Techniques”** – The HV7358 deals with high-speed, high-frequency and high-current signals. This chapter will explain PCB layout techniques for these conditions.

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- [Appendix A. “HV7835DB1 and MUPB002 Schematics and Layouts”](#) – Shows the schematics and layouts for the HV7358DB1 and MUP002.
- [Appendix B. “Bill of Materials \(BOM\)”](#) – Lists the parts used to build the HV7358DB1 Evaluation Board.
- [Appendix C. “HV7358DB1 Waveforms”](#) – Shows sample output waveforms generated by the HV7358DB1.
- [Appendix D. “HV7358 GUI Parameter and Default”](#) – Documents GUI limits and default values.

CONVENTIONS USED IN THIS GUIDE

This manual uses the following documentation conventions:

DOCUMENTATION CONVENTIONS

| Description | Represents | Examples |
|--|---|---|
| Arial font: | | |
| Italic characters | Referenced books | <i>MPLAB[®] IDE User's Guide</i> |
| | Emphasized text | ...is the <i>only</i> compiler... |
| Initial caps | A window | the Output window |
| | A dialog | the Settings dialog |
| | A menu selection | select Enable Programmer |
| Quotes | A field name in a window or dialog | "Save project before build" |
| Underlined, italic text with right angle bracket | A menu path | <u><i>File>Save</i></u> |
| Bold characters | A dialog button | Click OK |
| | A tab | Click the Power tab |
| N'Rnnnn | A number in verilog format, where N is the total number of digits, R is the radix and n is a digit. | 4'b0010, 2'hF1 |
| Text in angle brackets < > | A key on the keyboard | Press <Enter>, <F1> |
| Courier New font: | | |
| Plain Courier New | Sample source code | <code>#define START</code> |
| | Filenames | <code>autoexec.bat</code> |
| | File paths | <code>c:\mcc18\h</code> |
| | Keywords | <code>_asm, _endasm, static</code> |
| | Command-line options | <code>-Opa+, -Opa-</code> |
| | Bit values | <code>0, 1</code> |
| | Constants | <code>0xFF, 'A'</code> |
| Italic Courier New | A variable argument | <i>file.o</i> , where <i>file</i> can be any valid filename |
| Square brackets [] | Optional arguments | <code>mcc18 [options] file [options]</code> |
| Curly brackets and pipe character: { } | Choice of mutually exclusive arguments; an OR selection | <code>errorlevel {0 1}</code> |
| Ellipses... | Replaces repeated text | <code>var_name [, var_name...]</code> |
| | Represents code supplied by user | <code>void main (void) { ... }</code> |

RECOMMENDED READING

This user's guide describes how to use the HV7358DB1 Evaluation Board. The following Microchip document is available and recommended as a supplemental reference resource.

- **HV7358 Data Sheet – “16-Channel, 3-Level HV Ultrasound Transmitter with Built-In Transmit Beamformer” (20005918)**

THE MICROCHIP WEBSITE

Microchip provides online support via our website at www.microchip.com. This website is used as a means to make files and information easily available to customers. Accessible by using your favorite Internet browser, the website contains the following information:

- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, latest software releases and archived software
- **General Technical Support** – Frequently Asked Questions (FAQs), technical support requests, online discussion groups, Microchip consultant program member listing
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Users of Microchip products can receive assistance through several channels:

- Distributor or Representative
- Local Sales Office
- Field Application Engineer (FAE)
- Technical Support

Customers should contact their distributor, representative or field application engineer (FAE) for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in the back of this document.

Technical support is available through the website at:
<http://www.microchip.com/support>.

DOCUMENT REVISION HISTORY

Revision A (January 2020)

- Initial release of this document.

NOTES:

Chapter 1. HV7358 Overview

1.1 INTRODUCTION

The HV7358DB1 Evaluation Board (ADM00732), working with the MUPB002 (ADM00900), provides a demonstration platform to test and characterize the HV7358.

The HV7358 is a 16-channel, 3 level, $\pm 80V$, 1.6A ultrasound transmit beamformer. It is designed primarily for portable medical ultrasound image applications, but it is applicable to cart-based medical ultrasound systems, as well as NDT applications. The output MOSFET transistors' maximum current can be programmed to $\pm 0.3A$, $\pm 0.5A$, $\pm 1.0A$ or $\pm 1.6A$. Each channel has a T/R switch, RX-damp switch, bleed resistor and diode clamps to V_{PP} and V_{NN} .

Internal floating power supplies generate the gate drive voltages required for the TX output FETs. These supplies function at any V_{PP}/V_{NN} voltage.

The 200 MHz clock retiming capability provides low jitter in CW, PW and B mode. The clock synchronization realigns all internal logic clock signals to a master clock, reducing the various propagation delays caused by any jitter from the external FPGA.

The HV7358 features an internal low jitter PLL clock multiplier for generating the delay clock for the digital beamformer. The clock input can accept LVDS differential signals from 30 MHz (min.) to 80 MHz (max.) in the PLL mode and from 30 MHz to 200 MHz in the non-PLL mode. At 200 MHz, the incremental delay is 5 ns. The clock multiplier is programmable by x1, x2, x3, x4, x5, x6 and x8. The transmitter outputs are synchronized with the delay clock to reduce phase noise.

Note: The HV7358DB1 Evaluation Board uses hazardous high voltages. Use caution when operating the HV7358DB1.

HV7358DB1 User's Guide

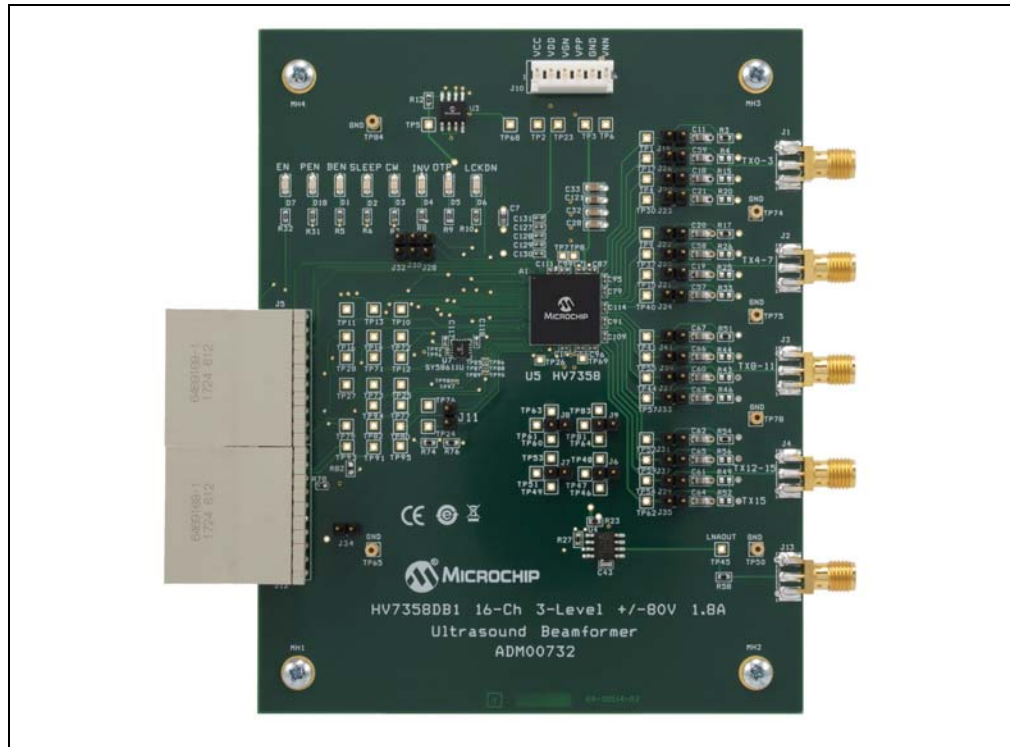


FIGURE 1-1: HV7358DB1 Board Photo.

1.2 FEATURES

- HV7358DB1 16-channel, ultrasound, beamforming transmitter
- Designed to work with the Microchip Ultrasound Platform Board (MUPB002)
- Three-level output: V_{PP} , V_{NN} and RTZ
- V_{PP}/V_{NN} up to $\pm 80V$ high voltages
- Up to $\pm 1.6A$ source and sink current capability
- On-board 330 pF||2.5K dummy load per channel
- Built-in RX damping circuit
- Built-in 200 MHz LVDS SPI clock
- Built-in LVDS TX clock, selectable from 80, 120, 160 or 200 MHz (non-PLL)
- Built-in LVDS TX clock, selectable from 30, 40, 60 or 80 MHz (PLL mode)
- Daisy-chain capable
- User-controllable per-channel beamforming delay and apodization
- Evaluates the RX echo signals with an on-board LNA emulator
- Demonstrates B mode and CW mode waveform control
- On-board SPI EEPROM for the ultrasound demonstration board ID
- Test points for convenient measurement
- On-board 5V and 3.3V voltage supplies available for user

1.3 DEVICE SUMMARY

The HV7358DB1 Evaluation Board contains the following Microchip products:

- HV7358: 16-Channel, 3-Level, $\pm 80V$, 1.6A Ultrasound TX Beamformer
- MCP1727: 1.5A Low-Voltage, Low-Quiescent Current LDO Regulator
- SY58611U: Dual 350 mV, 3.2 Gbps LVDS MUX Switch

HV7358 Overview

TABLE 1-1: HV7358DB1 TECHNICAL SPECIFICATIONS

| Parameter | Value |
|---|--|
| Modes of Operation | 16-Channel TX Beamforming B mode, PW Mode and CW Mode |
| B Mode Output Pulses Peak Voltage and Current (CW = 0) | Up to $\pm 80V$ and $\pm 1.6A$ |
| CW Output Peak Voltage and Current (CW = 1) | 16-Channel 0 to $\pm 8V$ and ± 300 mA (typical) |
| HV7358 TX Clock Input Frequency (PEN = 1) | 30 to 80 MHz in PLL Mode |
| HV7358 TX Clock Input Frequency (PEN = 0) | 80 to 200 MHz in non-PLL Mode |
| CW Frequency Range | Programmable CW Frequency from 1 MHz to 7 MHz |
| Interface of FPGA Control Signals and USB PC GUI Software | J5 and J12 Connects MUPB002 Interface Board Software |
| Logic Circuitry, 2.5V V_{LL} Voltage Supply LDO Regulator | Built-in with Optional Voltage Source from MUPB002 or J10 |
| TX R-C Test Load and User's Transducer Interface | Built-in, 330 pF 2.5K per Channel with Jumper and 50 Ω SMA |
| On-Board LED Indicator of Signals | EN, CW, INV, BEN, PEN, OTPN and LCKDN |
| Overtemperature Protection | Open-Drain Output to J5 and J12 to MUPB002 |
| Floating Gate Driver Voltage Regulators | Built-in Floating Regulators in HV7358 |
| PCB Board Dimension | 127 x 102 mm (5.0 x 4.0 Inch) |

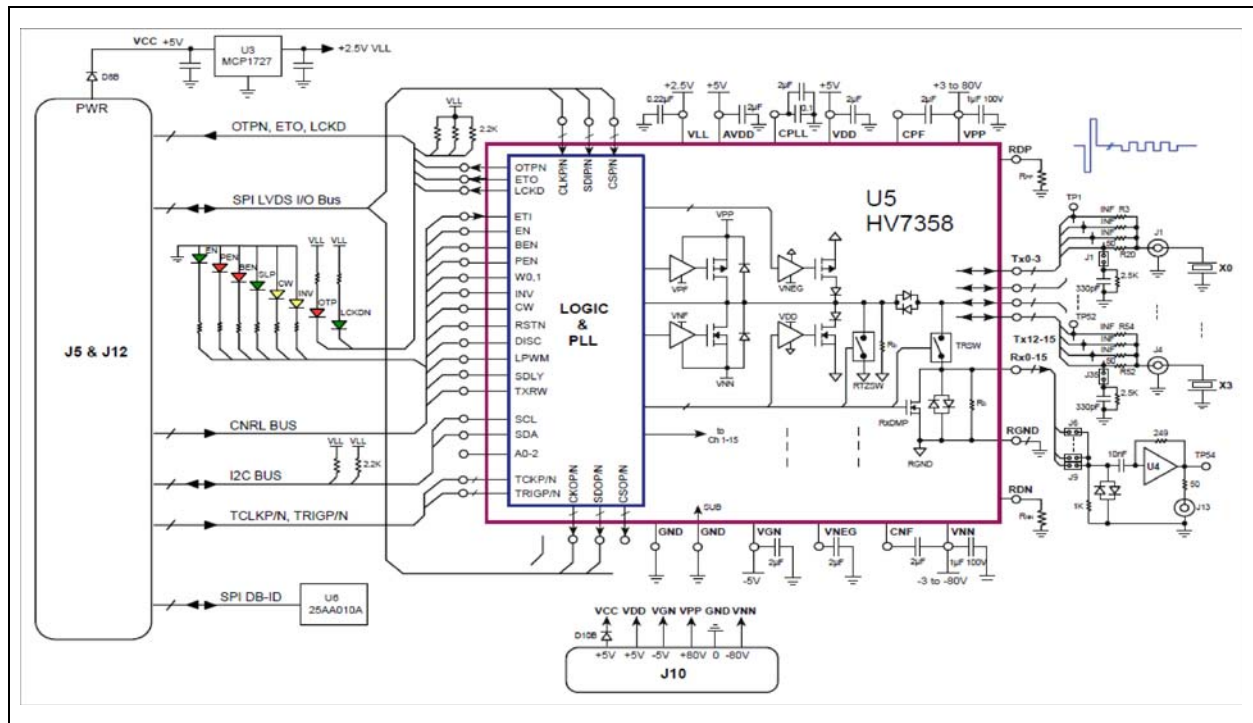


FIGURE 1-2: HV7358DB1 Block Diagram.

HV7358DB1 User's Guide

1.4 FUNCTIONAL DESCRIPTION

The HV7358DB1/MUPB002 combination demonstrates a 16-channel, 3-level, $\pm 80V$, 1.6A ultrasound transmit beamformer. Features include T/R switches with RX damping switch, diode clamps to V_{PP} and V_{NN} and programmable TX current limit, and internal voltage regulators to generate the required gate drive voltages. The HV7358 is a high-voltage, monolithic IC packaged in a 13x13 mm, 168-lead TFBGA package.

The HV7358 is applicable to medical ultrasound as well as NDT applications.

Both the HV7358DB1 and the MPUB002 boards are required. They are connected together by two high-speed, impedance matched, right-angle, backplane connectors. The HV7358DB1 contains the HV7358, LED indicators for the logic signals, and a transimpedance amplifier to emulate an LNA and an LDO. The MUPB002 contains the USB interface and an FPGA.

Each TX output has a 330 pF||2.5K load, which requires a shorting connector to be attached; without the connector, the output will be open.

The 200 MHz clock retiming provides low jitter in CWD, PW or B mode. The clock synchronization realigns the logic input signals to the master clock, which reduces various propagation delays caused by FPGA output jitter.

An SPI EEPROM on the HV7358DB1 Demonstration Board is for MUPB002 and PC GUI software to automatically identify the demonstration board ID.

All of the 16 TX outputs are accessible at test points on the HV7358DB1. There are also four SMA connectors on the board that can be connected to the TX outputs via jumper shorting plugs.

The output of any of the T/R switches can be connected to the on-board transimpedance amplifier (U4). This is done via a jumper shorting plug. The amplifier output is available at an SMA connector (J13).

1.5 WHAT THE HV7358DB1 ADM00732 KIT INCLUDES

The HV7358DB1 includes:

- HV7358DB1 ADM00732 Evaluation Board
- Important Information Sheet

Chapter 2. HV7358DB1 Software Installation

2.1 GETTING STARTED

The HV7358DB1 Evaluation Board requires the use of the MPUB002 board, PC GUI software and multiple voltage rails power supply for the full functional demonstration.

Both the MPUB002 board and the HV7358DB1 are required to test the boards.

A USB driver may need to be installed to communicate with the MPUB002. Detailed installation instructions are presented.

A GUI to program the MPUB002 is also required. Detailed installation instructions are presented.

Note: To update the latest software driver and demonstration program, go to the www.microchip.com website.

2.2 USB DRIVER INSTALLATION

To communicate with the MPUB002/HV7358DB1, the correct USB driver must be installed.

Follow the steps below to determine which USB driver to install:

1. Connect the USB cable from the lower male Micro-B connector on the MPUB002 board to any USB connector on your PC. The USB will power the board.

Note: Do not connect any other power supplies at this time.

2. Open "Device Manager". Look at "Bridge device". If it has a yellow triangle/exclamation mark as shown in [Figure 2-1](#) and [Figure 2-2](#), the correct USB driver needs to be installed.

Note: If the yellow triangle/exclamation mark does not exist, skip to [Section 2.3 "HV7358DB1 GUI Installation"](#); otherwise, complete this section.

3. Download the "MPLAB[®] Connect Configurator Tool" using the following link: <https://www.microchip.com/design-centers/usb/mplab-connect-configurator>
4. Unzip the downloaded folder titled, MPLABConnect_V2.3. This folder will be used later.
5. Right click on "Bridge device".

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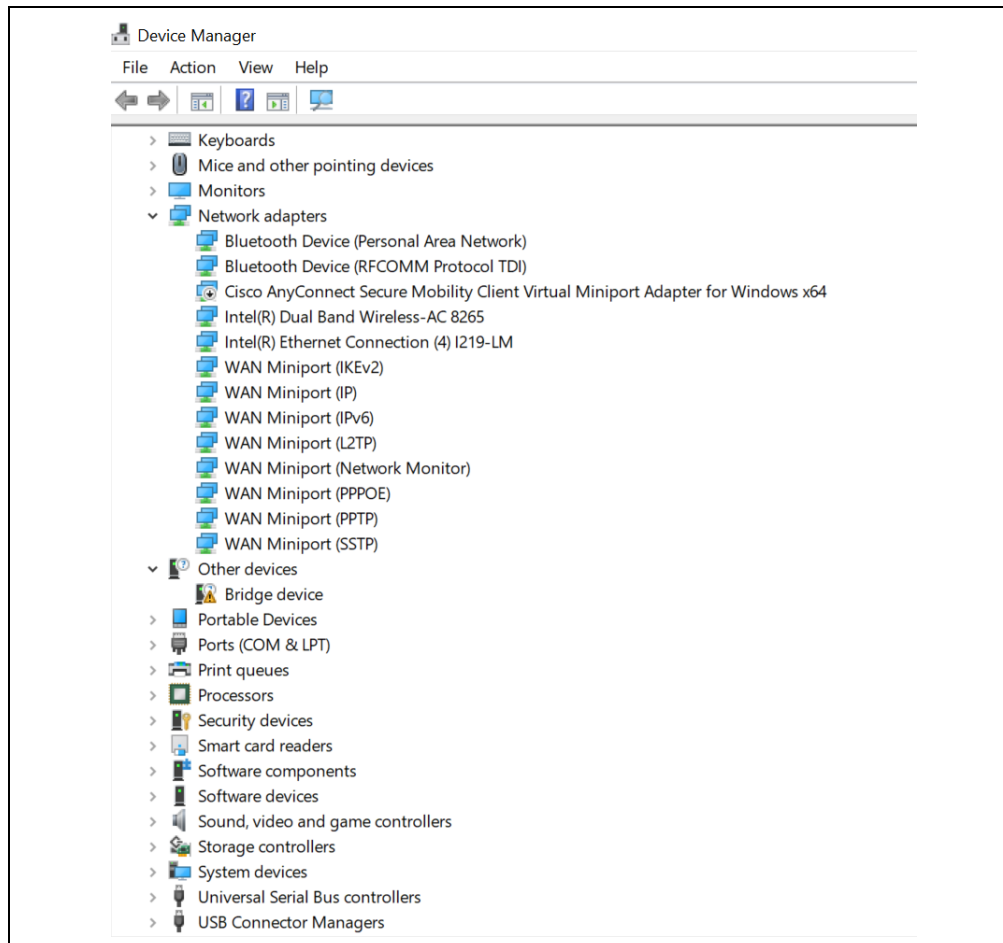


FIGURE 2-1: View of "Device Manager" Screen.

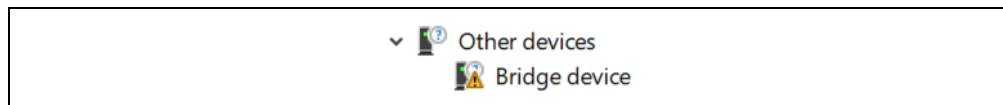


FIGURE 2-2: Close-up of "Bridge device" with Error.

HV7358DB1 Software Installation

6. A pop-up window will open as shown in [Figure 2-3](#) below. Choose “Update driver” and click on it.

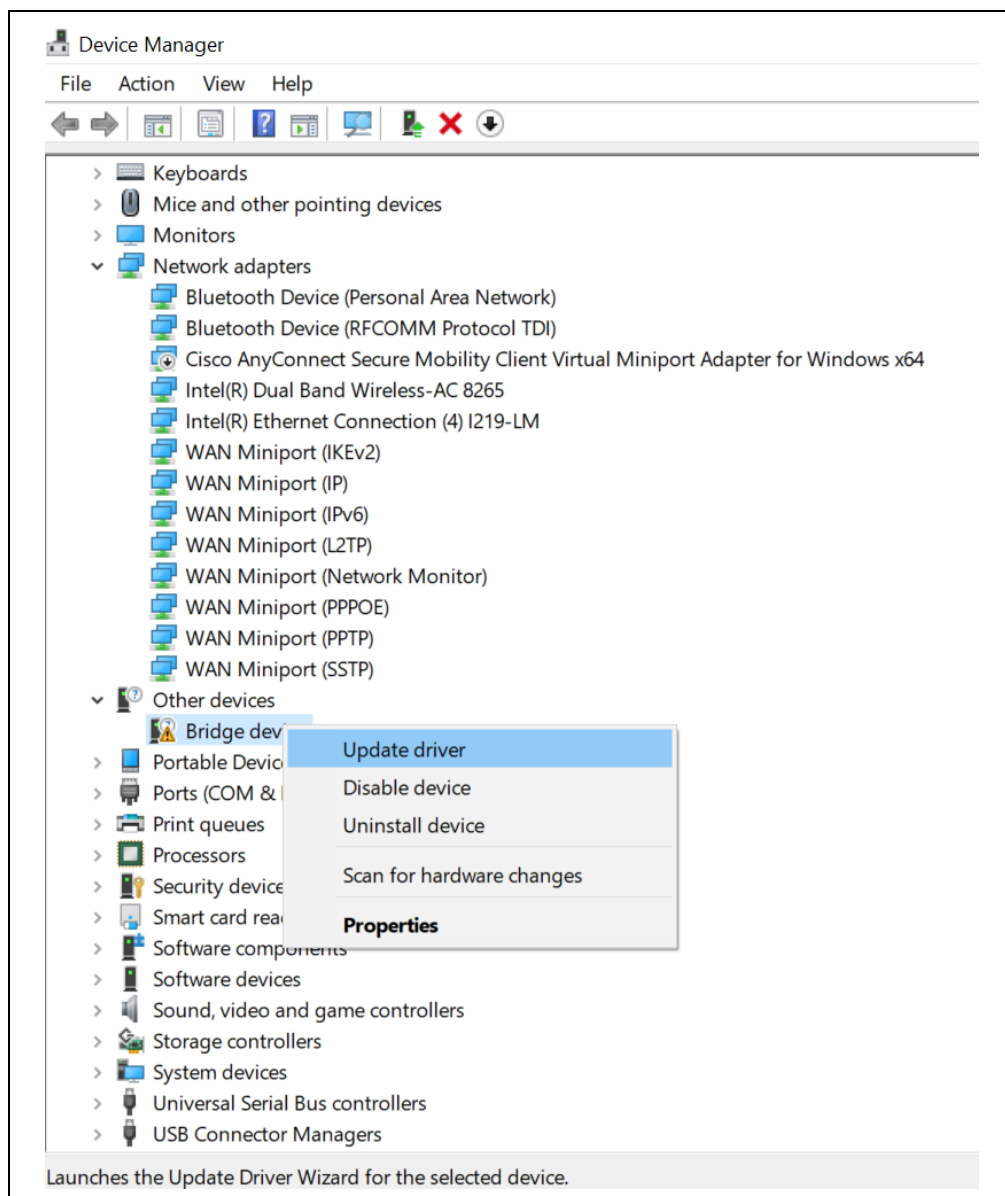


FIGURE 2-3: “Update driver” Pop-up Window.

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7. After clicking on “Update driver”, the window in [Figure 2-4](#) will appear. Choose “Browse my computer for driver software”.

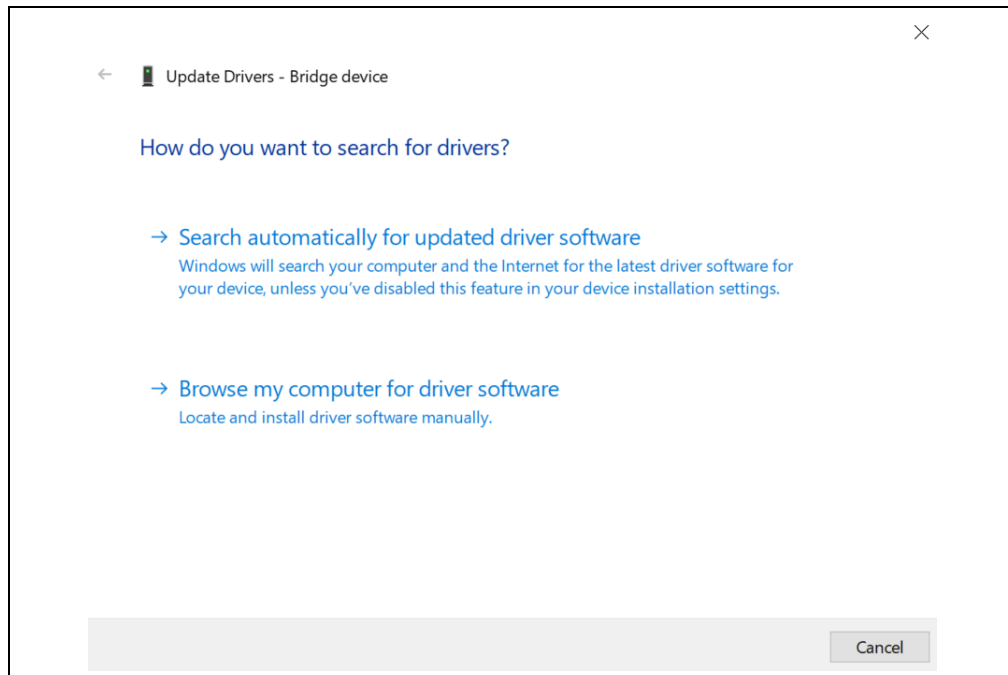


FIGURE 2-4: Driver Search Window.

8. The following window will open. Click on the **Browse** button.

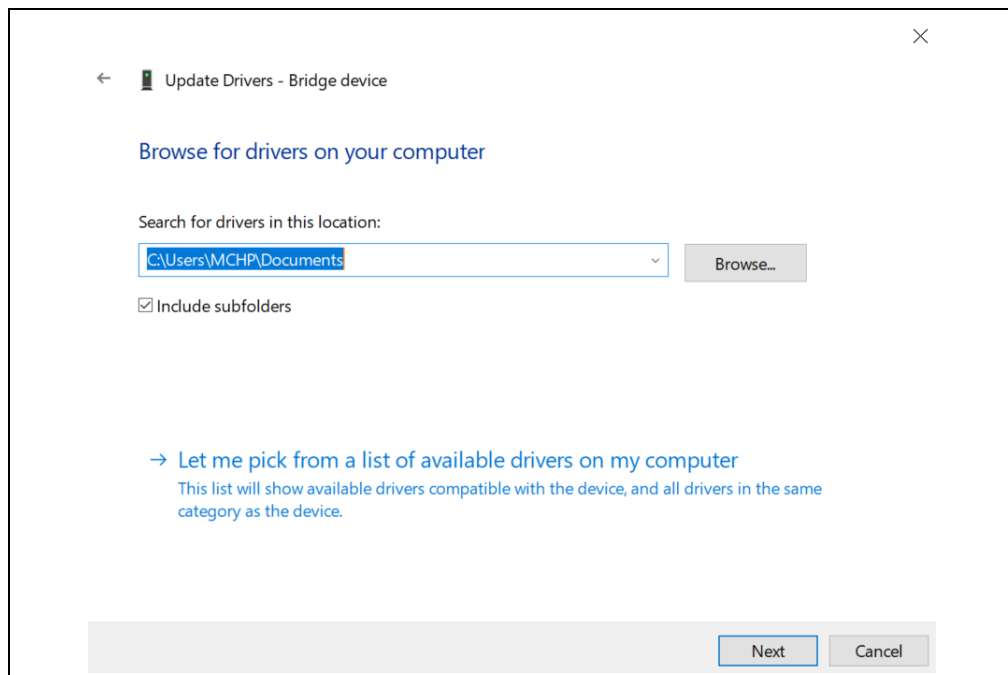


FIGURE 2-5: Driver Browse Choice Window.

HV7358DB1 Software Installation

9. The following window will open. Go to the MPLABConnect_V2.3.4 folder recently downloaded from the Microchip website and choose the “Drivers” sub-directory. Double click on “Drivers”.

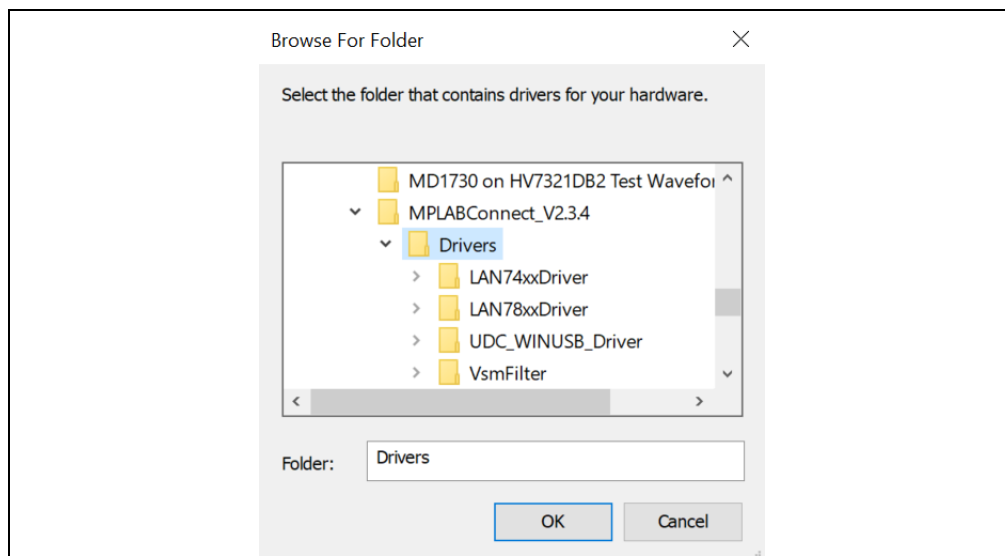


FIGURE 2-6: Browse to “Drivers” Folder Window.

The window in [Figure 2-7](#) will appear. The path shown will point to the drivers used by the MPLABConnect tool.

10. Click the **Next** button.

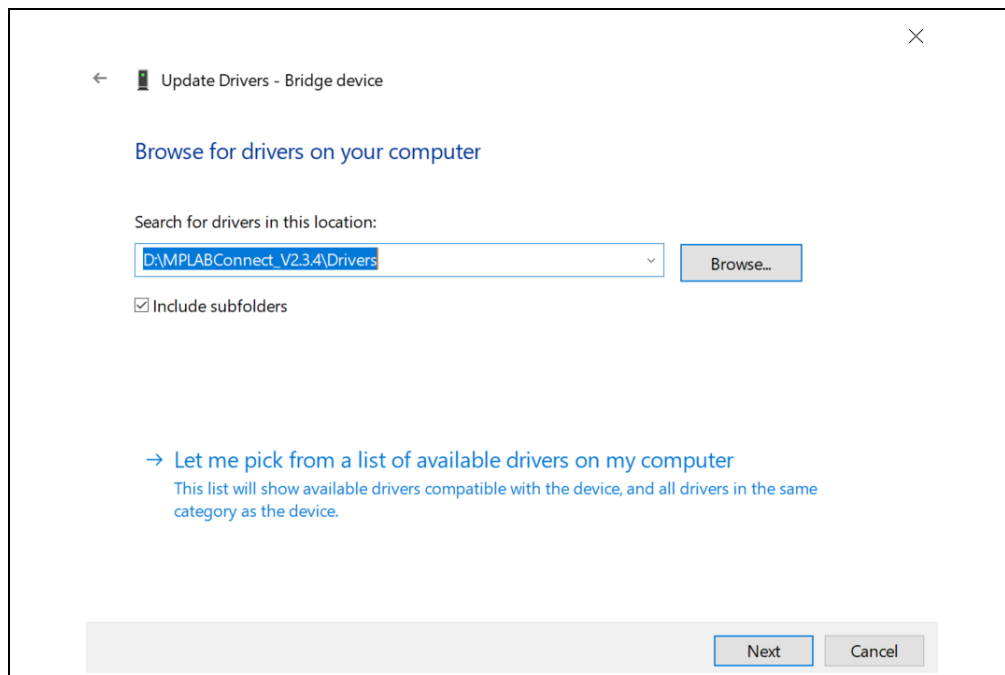


FIGURE 2-7: Browse for Drivers Screen.

The window shown in [Figure 2-8](#) will appear.

11. Click the **Install** button.

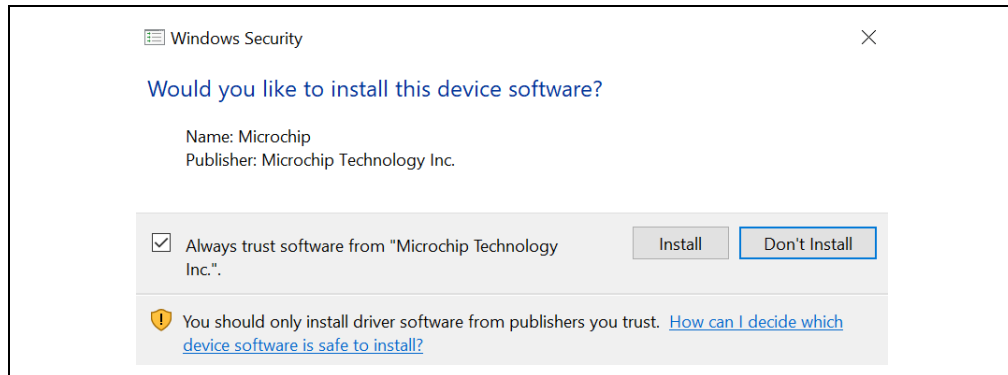


FIGURE 2-8: *Install Verification Screen.*

12. After successful installation, the window shown in [Figure 2-9](#) will appear. This verifies that you have installed the USB driver.

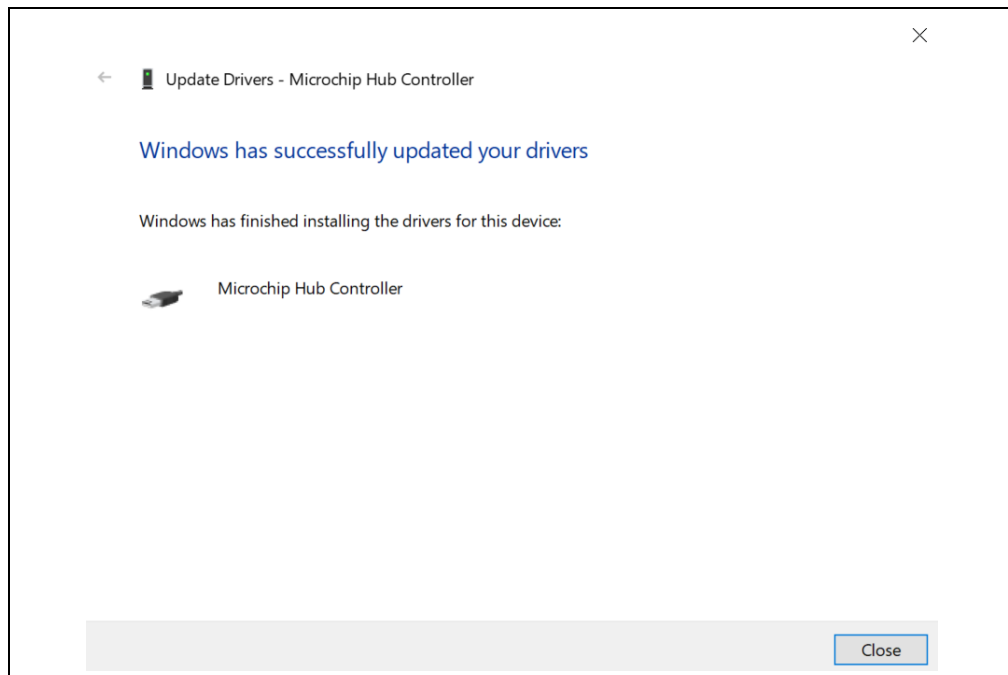


FIGURE 2-9: *USB Driver Installation Verification Screen.*

2.3 HV7358DB1 GUI INSTALLATION

Download the MUPB002/HV7358DB1 GUI Installation tool from the Microchip website. The HV7358 GUI program will require about 2.6 MB hard drive space.

1. Double click on the file named, MUPB002 – HV7358 GUI Setup. The window in [Figure 2-10](#) below will pop up.
2. Click **Next**.

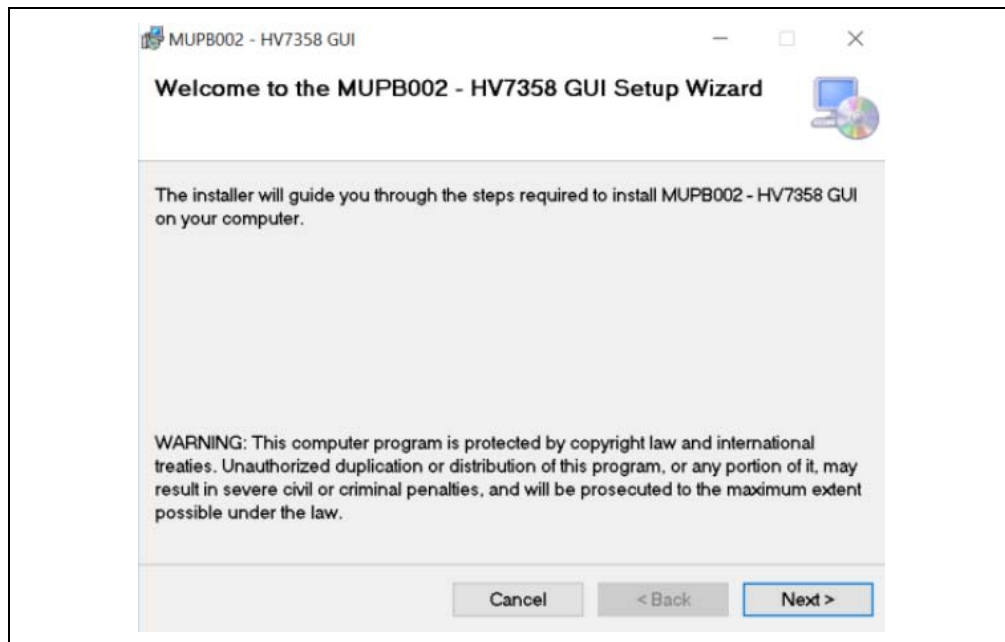


FIGURE 2-10: HV7358 Setup Wizard Opening Window.

3. The License Agreement will appear, as in [Figure 2-11](#). Read and if you agree, select **I agree**, then **Next** to continue. If you do not agree, the installation will stop.

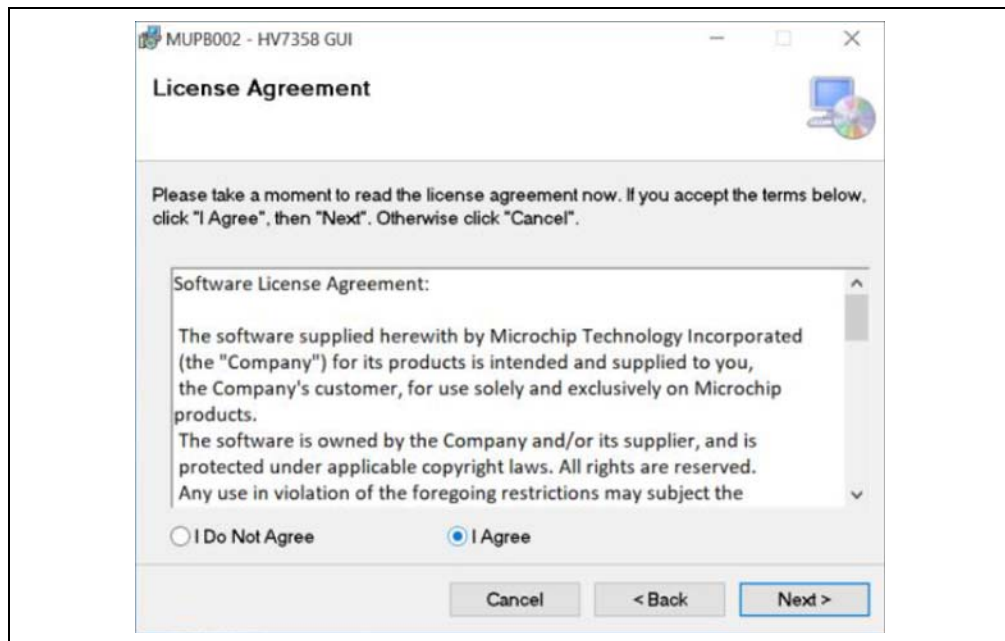


FIGURE 2-11: License Agreement.

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- The next window, shown in [Figure 2-12](#), sets the Select Installation Folder. The default folder is shown. A different folder may also be specified.

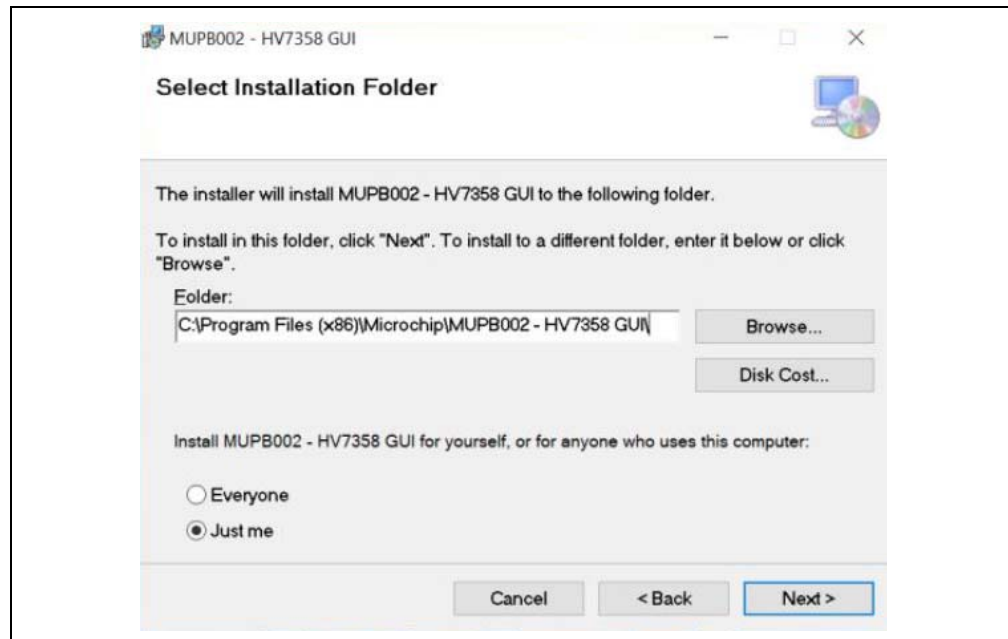


FIGURE 2-12: *Installation Folder.*

- The next window, shown in [Figure 2-13](#), confirms that you are ready to install the HV7358 GUI. If so, click **Next**; otherwise, you can go back and make changes or **Cancel**.

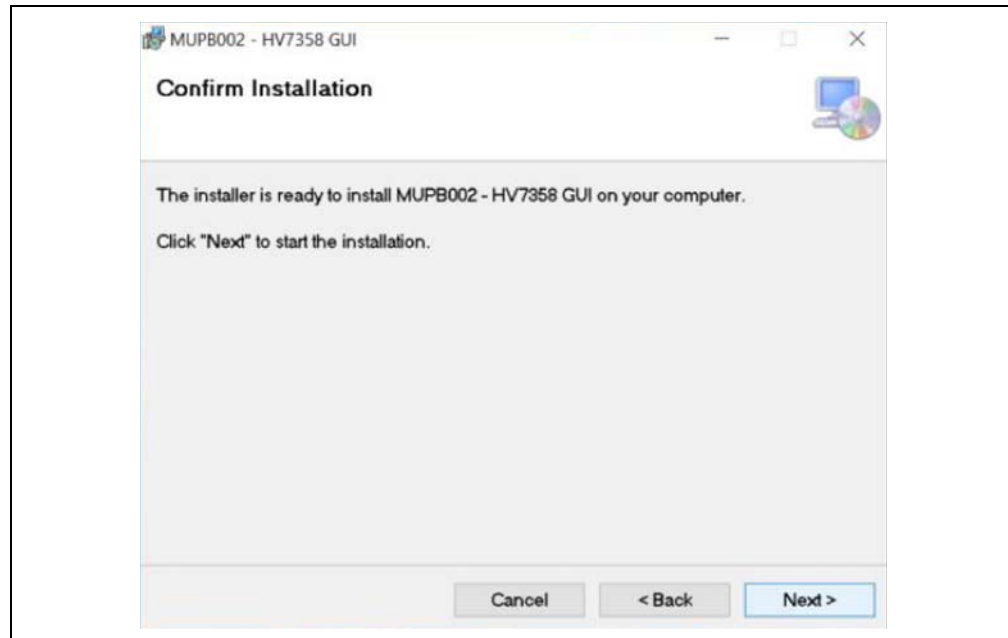


FIGURE 2-13: *Installation Confirmation.*

HV7358DB1 Software Installation

6. The following window, shown in [Figure 2-14](#), will be visible during the actual GUI installation.

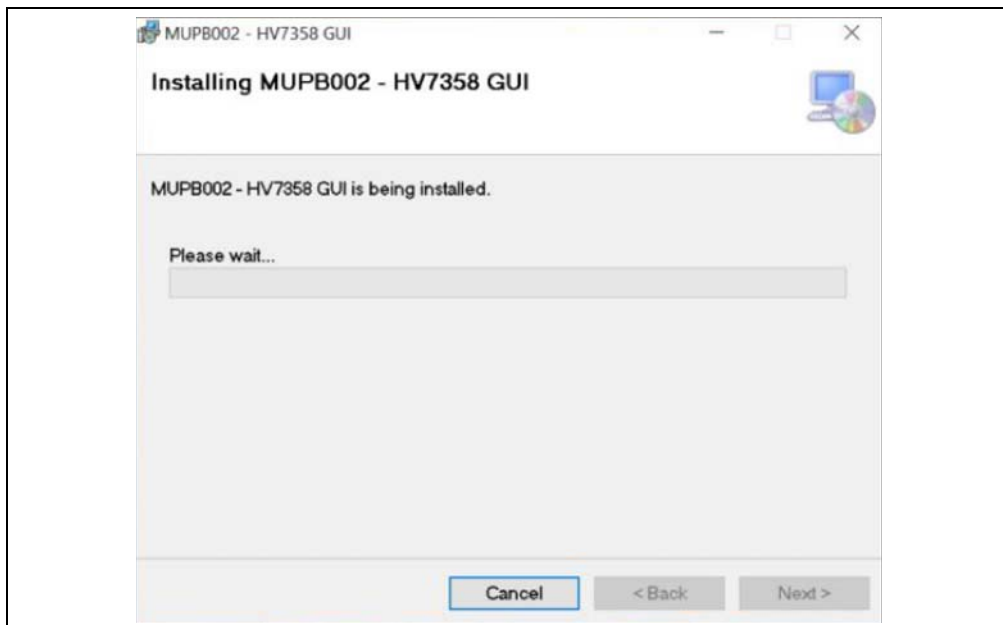


FIGURE 2-14: *Installation Window.*

Once installation is complete, the following window will appear, as shown in [Figure 2-15](#). Click on **Close** when the installation is complete. The GUI window will disappear.

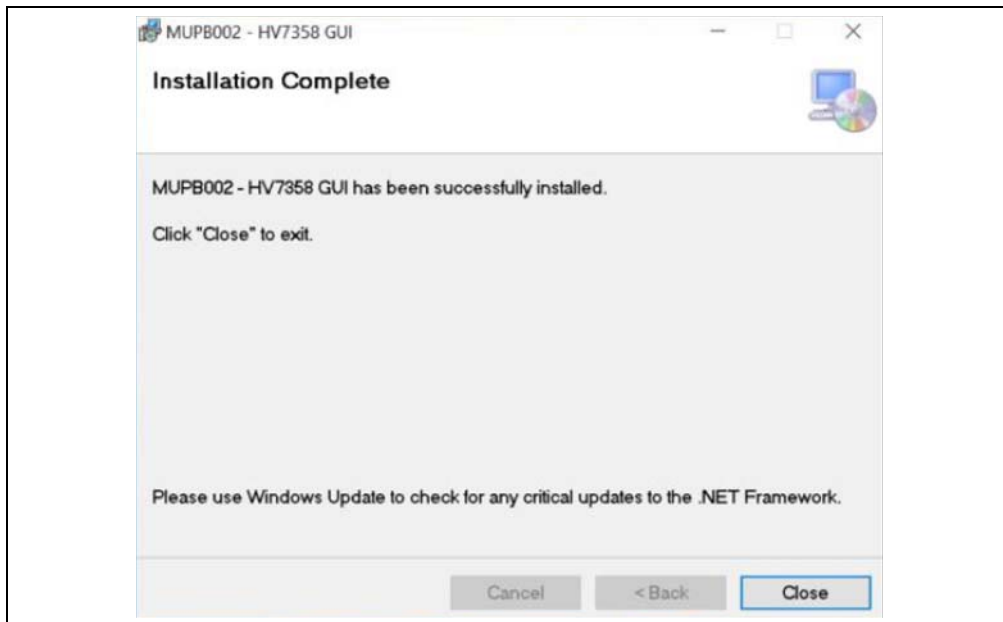


FIGURE 2-15: *Installation Complete Window.*

The icon below in [Figure 2-16](#) will be left on your desktop. Double click to open the HV7358 GUI. The GUI Installation is complete.

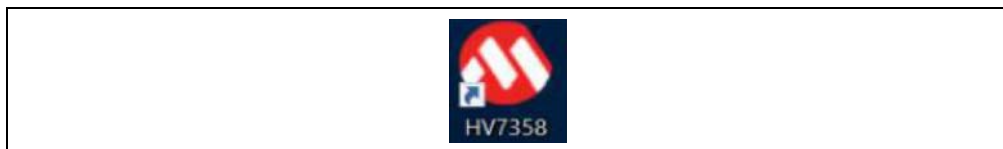


FIGURE 2-16: *HV7358 GUI Icon.*

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NOTES:

Chapter 3. HV7358DB1 GUI Operation

3.1 GETTING STARTED

The HV7358DB1 is a 16-channel, 3-level, $\pm 80V$, 1.6A ultrasound beamformer evaluation board. To operate, it requires the use of the MUPB002 board (ADM00900), the PC GUI software and multiple voltage rails for the full functional demonstration.

Note: To update the latest software driver and demonstration program, please go to the www.microchip.com website.

3.2 SETUP PROCEDURE

To operate the HV7358DB1, the following steps must be completed:

1. Connect J1 and J2 of the MPUB002 board to J5 and J12 of the HV7358DB1.
2. Connect a USB cable from the lower male Micro-B connector (J7) on the MPUB002 board to any USB connector on your PC.
3. Install jumpers, J6, J14, J15, J16 and JP1 (JP1 requires two jumpers), as per [Table 3-1](#).

TABLE 3-1: JUMPER FUNCTION

| Power Jumper | Powered Bank | Selection (2.5V/3.3V) |
|--------------|--------------|-----------------------|
| J6 | Bank1 | +2.5V |
| J14 | Bank0 | +2.5V |
| J15 | Auxiliary | +3.3V |
| J16 | Bank3 | +2.5V |
| JP1 | GND | 0V |

4. Jumpers, J19 through J35, connect a 330 pF||2.5K load to each respective TX output. Without the jumper, the TX output will be open. If the load is wanted, add the jumpers.

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3.3 HV7358DB1 POWER SUPPLY REQUIREMENTS

Connect all power supplies to the HV7358DB1 power supply connector (J10). The voltage and current requirements can be found in [Table 3-2](#) below. Leave the power supplies turned off.

TABLE 3-2: J10 POWER SUPPLY CONNECTION INFORMATION

| Terminal | Rail Name | Voltage | Average Current Limit |
|----------|-----------------|-----------|-----------------------|
| J10-1 | V _{CC} | +5V | 50 mA |
| J10-2 | V _{DD} | +5V | 180 mA |
| J10-3 | V _{GN} | -5V | 30 mA |
| J10-4 | V _{PP} | 0 to +80V | 5 mA |
| J10-5 | GND | 0V | — |
| J10-6 | V _{NN} | 0 to -80V | 5 mA |

The power-up and down sequencing is shown in [Table 3-3](#) below.

TABLE 3-3: POWER-UP/DOWN SEQUENCE

| Step # | Power-up | Step # | Power-Down |
|--------|--------------------------------------|--------|---------------------------------------|
| 1 | V _{CC} , V _{DD} On | 1 | EN = 0 |
| 2 | V _{GN} On | 2 | V _{PP} , V _{NN} Off |
| 3 | V _{PP} , V _{NN} On | 3 | V _{GN} Off |
| 4 | EN = 1 | 4 | V _{CC} , V _{DD} Off |

3.4 MUPB002 AND GUI/USB PROGRAMMING

Open and run the GUI by double clicking the HV7358DB1 icon. The GUI will open showing the following screen:

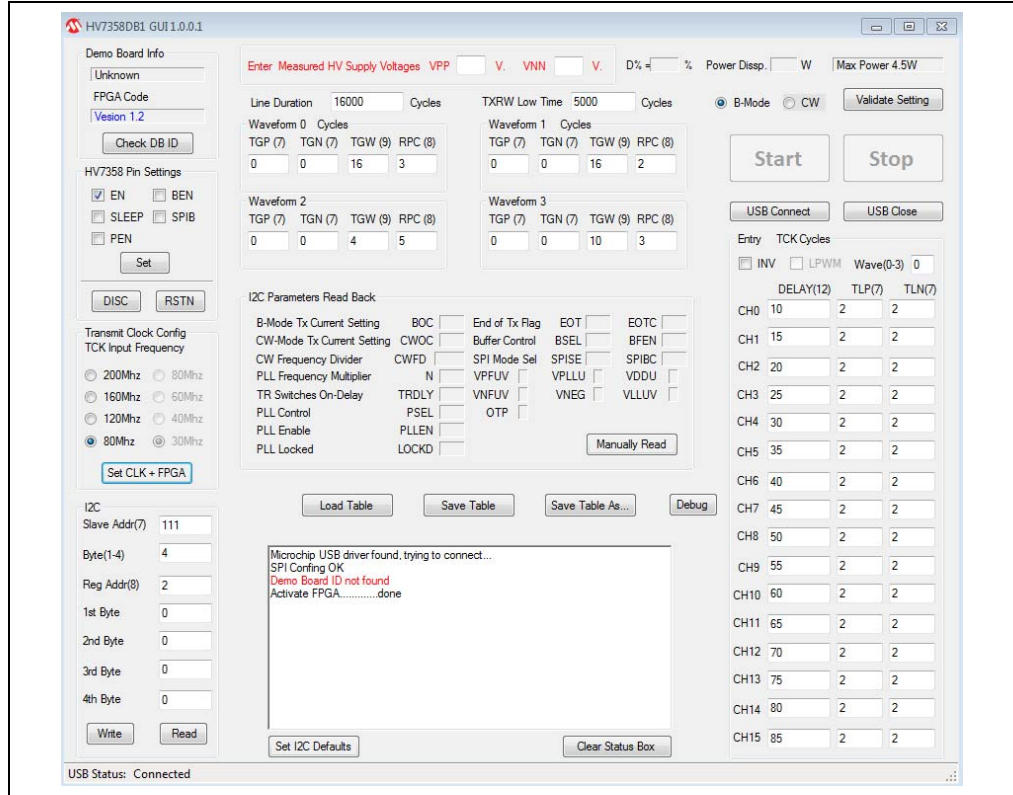


FIGURE 3-1: Full GUI Screen.

At the bottom left hand corner, there should be the “USB Status: Connected” note, as shown in Figure 3-2 below.

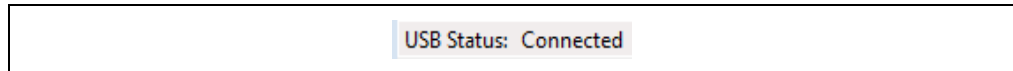


FIGURE 3-2: USB Status Note.

When the MUPB002 board is connected to the PC, or when the GUI is started, the USB should connect automatically. If it does not, there is a **USB Connect** button at the upper right corner of the GUI. If it is required to disconnect the USB, there is also a **USB Close** button. See Figure 3-3 below.



FIGURE 3-3: USB Connect and Close Buttons.

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In the upper left corner there is a “Demo Board Info” box, as shown in [Figure 3-4](#) below. Click on the **Check DB ID** button. An HV7358DB1 revision number and an FPGA code version number should be shown.

If the USB status is “Connected” and the “Demo Board Info” is shown per above, then the GUI has successfully connected to the MUPB002 board.

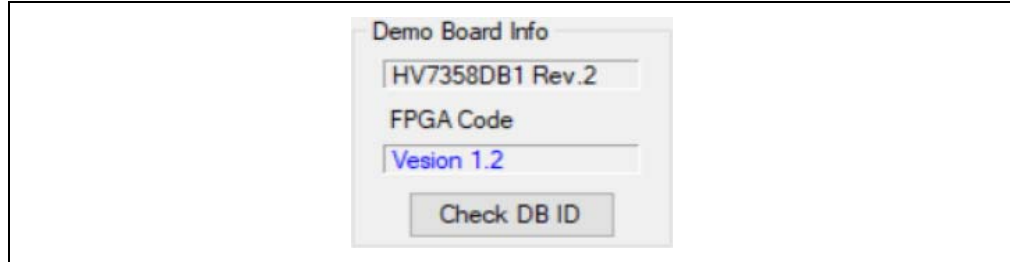


FIGURE 3-4: “Demo Board Info” Box.

3.4.1 HV7358 Pin Settings Box

The “HV7358 Pin Settings” box is shown in [Figure 3-5](#).

3.4.1.1 EN (ENABLE) PIN

The HV7358 Enable pin sets all TX outputs to High-Z.

TABLE 3-4: ENABLE SIGNAL

| EN | TX Outputs |
|----|------------|
| 0 | High-Z |
| 1 | Active |

3.4.1.2 BEN (BUFFER ENABLE) PIN

BFEN is an input logic pin that can disable the LVDS pins used to broadcast or daisy-chain multiple HV7358 chips. This ability can be used to reduce power dissipation. The BEN pin function can be overwritten with the BSEL and BFEN I²C signals. BSEL determines if BEN or BFEN actually controls the LVDS outputs.

TABLE 3-5: BUFFER ENABLE LOGIC

| BEN | BFEN | BSEL | LVDS Output Control Signal | LVDS Output |
|-----|------|------|----------------------------|-------------|
| 0 | 0 | 0 | BEN | Disabled |
| 1 | 0 | 0 | BEN | Enabled |
| 0 | 1 | 0 | BEN | Disabled |
| 1 | 1 | 0 | BEN | Enabled |
| 0 | 0 | 1 | BFEN | Disabled |
| 1 | 0 | 1 | BFEN | Disabled |
| 0 | 1 | 1 | BFEN | Enabled |
| 1 | 1 | 1 | BFEN | Enabled |

3.4.1.3 SLEEP (SLEEP MODE ENABLE) PIN

If the SLEEP pin is enabled, then the device is in power-saving mode. All the internal registers' data will be preserved and the internal clocks will freeze. The I²C interface is still active.

TABLE 3-6: SLEEP LOGIC

| SLEEP | HV7358 State |
|-------|-----------------|
| 0 | Enabled/Active |
| 1 | Sleep/Low Power |

3.4.1.4 SPIB (SPI FAST PROGRAMMING INTERFACE) PIN

This pin switches between the SPI Broadcast mode and the Daisy-Chain mode.

TABLE 3-7: SPIB LOGIC

| SPIB | Mode |
|------|---------------|
| 0 | Daisy-Chain |
| 1 | SPI Broadcast |

3.4.1.5 PEN (PLL ENABLE) PIN

PEN is an input logic pin that can enable or disable the internal PLL. The PEN pin function can be changed by the PLEN and PSEL I²C signals. PSEL determines if the PEN or PLEN bit in the I²C register actually controls the PLL.

TABLE 3-8: PEN LOGIC

| PEN | PLEN | PSEL | PLL Control Signal | Internal PLL |
|-----|------|------|--------------------|--------------|
| 0 | 0 | 0 | PEN | Disabled |
| 1 | 0 | 0 | PEN | Enabled |
| 0 | 1 | 0 | PEN | Disabled |
| 1 | 1 | 0 | PEN | Enabled |
| 0 | 0 | 1 | PLEN | Disabled |
| 1 | 0 | 1 | PLEN | Disabled |
| 0 | 1 | 1 | PLEN | Enabled |
| 1 | 1 | 1 | PLEN | Enabled |

3.4.1.6 SET BUTTON

Sends the selected data to the HV7358 data input pins.

Select the signals appropriate for your application and press the **SET** button.

3.4.1.7 DISC BUTTON

The **DISC** button will send a pulse to the HV7358 that activates the internal V_{PP} and V_{NN} switches that discharge their respective supply rails.

These switches have a 5 mA capability and are meant to discharge the bypass caps only. The supplies need to be turned off before activating the discharge switches.

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3.4.1.8 RSTN BUTTON

The **RSTN** button will send a pulse to the RESET pin on the HV7358. This will reset all HV7358 internal SPI and I²C registers to their default value.

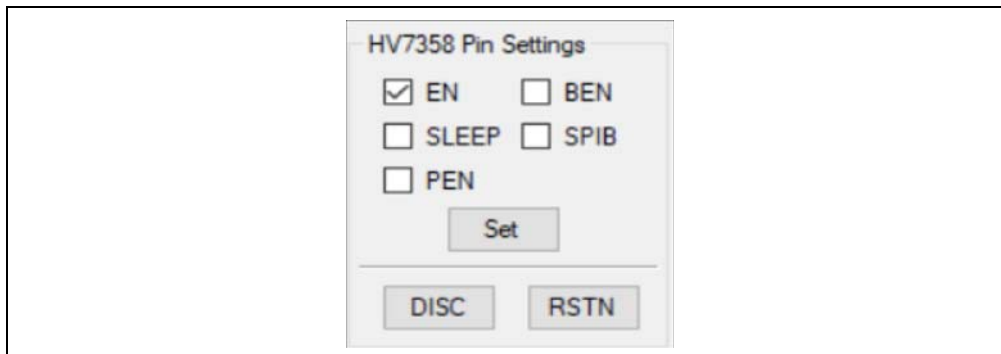


FIGURE 3-5: “HV7358 Pin Settings” Box.

3.4.2 V_{PP}/V_{NN} Values

The actual V_{PP} and V_{NN} values must be entered in the box as shown in Figure 3-6. The box is at the top center of the GUI page. An example of the window is shown below. V_{PP} = 55V and V_{NN} = -55V were entered in Figure 3-6. These values will be used to calculate the power dissipation.

Enter the V_{PP} and V_{NN} values.

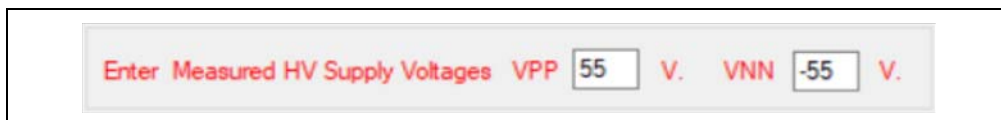


FIGURE 3-6: V_{PP} and V_{NN} Voltage Window.

3.4.3 Mode and Power Calculation

Click either the B mode or the CW mode button.

Click the **Validate Setting** button. The GUI will calculate the duty cycle (D%) and the power dissipation. It will also confirm that the power is within the limit of the HV7358. If the power is acceptable, the box will read “Power Within Limit”; otherwise, it will read “Power Outside Limit” and the **Start** button will be disabled.

For CW mode, 100% will be used for the duty cycle.



FIGURE 3-7: Mode and Power Dissipation Window.

3.4.4 Transmit Clock Frequency Configuration Window

The “Transmit Clock Frequency” box is shown below in [Figure 3-8](#).

F_{TCK} is the external frequency. The internal clock frequency is F_C . F_C is a function of F_{TCK} , PEN and mode setting.

The frequency choice is a function of the PEN variable. When PEN = 1, it turns the PLL on. The frequency selections for both PEN choices are shown below.

If the PLL mode is off (PEN = 0), then the external frequency choices are 80 MHz, 120 MHz, 160 MHz or 200 MHz. They are shown on the left side of [Figure 3-8](#).

If the PLL mode is on (PEN = 1), the external frequency choices are 30 MHz, 40 MHz, 60 MHz or 80 MHz. They are shown on the right side of [Figure 3-8](#). When in PLL mode, the frequency selections are on the left of [Figure 3-8](#).

In B mode with PEN = 0, the PLL is disabled and the internal clock frequency will be:

EQUATION 3-1: B MODE, NO PLL

$$F_C = F_{TCK}$$

If PEN = 1, the PLL circuitry is enabled; then, the I^2C parameter, “N”, will be part of the equation:

EQUATION 3-2: B MODE WITH PLL

$$F_C = F_{TCK} * N$$

In CW-Mode, the $TX_{(x)}$ output frequency will be:

EQUATION 3-3: CW MODE

$$F_{CW} = F_{TCK} / (2 * CWFD)$$

In CW mode, the PLL function cannot be used. Therefore, PEN and the PLL are disabled.

Choose the frequency by clicking on the appropriate box, then click on the **Set CLK + FPGA** button.

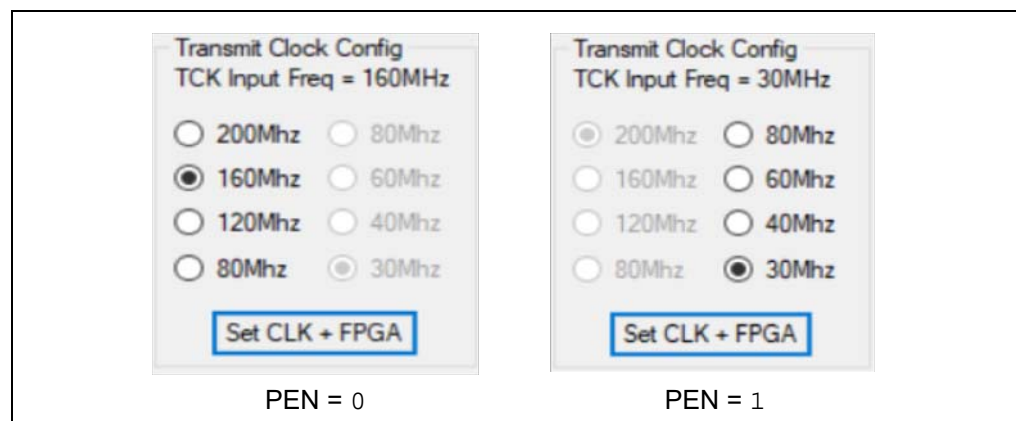
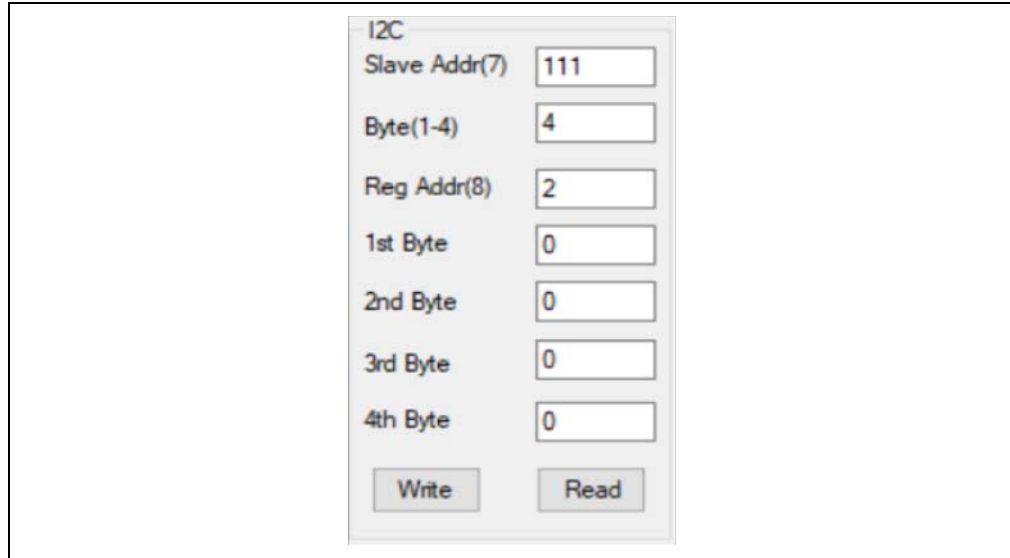


FIGURE 3-8: Transmit Clock Frequency Window.

3.4.5 I²C Box

The “I²C Read/Write” box is shown in [Figure 3-9](#).

This box can read the current I²C settings or write new ones. The default settings can be used for most applications. The HV7358DB1 is the slave and the HV7358 GUI is the master. The slave address ('111' by default) can be changed by adding jumpers on J28, J30 and J31. Clicking the **Read** button shows the current settings. Making a change to any of the values and clicking **Write** changes the current settings.



The screenshot shows a GUI window titled "I2C". It contains the following fields and buttons:

- Slave Addr(7): 111
- Byte(1-4): 4
- Reg Addr(8): 2
- 1st Byte: 0
- 2nd Byte: 0
- 3rd Byte: 0
- 4th Byte: 0
- Buttons: Write, Read

FIGURE 3-9: “I²C Read/Write” Box.

3.4.6 Line Duration Cycles and TXRW Low Time

The “Line Duration” and “TXRW Low Time” entry box is shown in [Figure 3-10](#).

Line Duration (LD) is the time it takes for one complete transmit pulse to be completed. It includes time for the actual TX waveform and the receive part. This is sometimes referred to as the “pulse repetition frequency”. The following limit must be observed: $(TGW * RPC) \gg LDR$

Line Duration cycles can be calculated from the following [Equation 3-4](#).

Choose the LD time or frequency. Calculate LD cycles using [Equation 3-4](#) and enter them into the Line Duration Cycles box shown in [Figure 3-10](#).

EQUATION 3-4:

$$LD \text{ Cycles} = (LD \text{ Time}) \times F_{TCK}$$

Where:
LD = Line Duration

HV7358DB1 GUI Operation

The “TXRW Low Time” is the programmable time allowed for the SPI or I²C bus to complete all required read/write commands after the pulse is completed. It is actually part of the LD time calculated above. It can be calculated using [Equation 3-5](#).

EQUATION 3-5:

$$TXRW \text{ Cycles} = (TXRW \text{ Low Time}) \times F_{TCK}$$

Choose the required “TXRW Low Time” and use [Equation 3-5](#) to determine the “TXRW Low Time Cycles”. Enter the “Line Duration Cycles” in the box and enter the “TXRW Low Time Cycles” in the box, as shown in [Figure 3-10](#).



The screenshot shows two input fields. The first is labeled "Line Duration" and contains the value "16000" followed by the unit "Cycles". The second is labeled "TXRW Low Time" and contains the value "5000" followed by the unit "Cycles".

FIGURE 3-10: “Line Duration” and “TXRW Low Time”.

3.4.7 Waveform Definition

The “Waveform Definition” box is shown in [Figure 3-11](#).

The HV7358 can store four different waveforms in the beamformer. They are numbered: Waveform 0 through Waveform 3.

TGP: Stands for Time Global Positive. **TGN:** Stands for Time Global Negative. These signals are disabled in the GUI. They could be used to set the delay time on a per TX_x basis.

TGW: Sets the maximum TX Global Pulse Width (P_W). It does this by setting the number of F_C time periods that the pulse remains high. The actual TGW is a 9-bit binary word. The GUI accepts a number between 0 and 511 and makes the conversion. TGW can be calculated from the following equation:

EQUATION 3-6:

$$TGW P_W \times F_{TCK}$$

P_W is the default maximum pulse width for any of the TX pulses, either positive or negative.

RPC: Sets the number of pulses in the waveform before returning to GND. If RPC = 1, a single positive pulse will be defined. If RPC = 2, one positive and one negative pulse will be done. RPC = 3 will be a positive, a negative and another positive pulse, etc.

The beamformer can hold up to four different waveforms. The parameters defined in this box are “global”. A global waveform is the same for each TX(0) through TX(15), but they can be different for each Waveform 0 through 3.



The screenshot shows a grid of four waveform definition boxes. Each box has a title "Waveform X Cycles" and four input fields labeled "TGP (7)", "TGN (7)", "TGW (9)", and "RPC (8)".

| Waveform | TGP (7) | TGN (7) | TGW (9) | RPC (8) |
|------------|---------|---------|---------|---------|
| Waveform 0 | 0 | 0 | 16 | 3 |
| Waveform 1 | 0 | 0 | 16 | 2 |
| Waveform 2 | 0 | 0 | 4 | 5 |
| Waveform 3 | 0 | 0 | 10 | 3 |

FIGURE 3-11: “Waveform Definition” Box.

Knowing the maximum pulse width, calculate TGW. Enter into the TGW box for each waveform. Enter into the RPC box for each waveform. See [Figure 3-11](#).

3.4.8 I²C Parameters Read-Back Window

The I²C parameters that are programmed into the GUI can be seen in the I2C Parameters Read Back window shown in [Figure 3-12](#). They can also be changed to meet specific application requirements.

The I2C Parameters Read Back window is located at the low middle of the GUI screen. All the parameters are read back from the HV7358 I²C registers.

3.4.8.1 BOC[1:0] BITS

The BOC bits are the I²C control for B mode TX output peak current limit setting. This is a global signal that applies to every TX channel.

TABLE 3-9: TX CURRENT LIMIT SETTING

| BOC[1:0] (Binary) | BOC (GUI) | TX Current Limit |
|-------------------|-----------|------------------|
| 00 | 0 | ±1.6A |
| 01 | 1 | ±900mA |
| 10 | 2 | ±600mA |
| 11 | 3 | ±300mA |

3.4.8.2 CWOC BIT

CWOC is the I²C control bit that determines the CW output R_{ON} selection.

TABLE 3-10: CWOC R_{ON}

| CWOC | R _{ON} |
|------|-----------------|
| 0 | 30Ω |
| 1 | 45Ω |

3.4.8.3 CWFD[7:0] BITS

These bits set the CW frequency divisor I²C register. A complete explanation can be found in [Section 3.4.4 “Transmit Clock Frequency Configuration Window”](#).

3.4.8.4 N[2:0] BITS

These bits set the PLL frequency multiplier number in the I²C register. The bits are used in determining the F_{TCK} frequency when in PLL mode. See [Section 3.4.4 “Transmit Clock Frequency Configuration Window”](#).

TABLE 3-11: FREQUENCY MULTIPLIER

| N[2:0] in GUI | N[2:0] in HV7358 |
|---------------|------------------|
| 1 | 1 |
| 2 | 2 |
| 3 | 3 |
| 4 | 4 |
| 5 | 5 |
| 6 | 6 |
| 7 | 8 |

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3.4.8.5 TRDLY[4:0] BITS

The TRDLY bits set the I²C T/R Switch On-Time Delay Selection Control register. The TRDLY are a 5-bit binary word. The GUI accepts 0 to 31 in decimal. The actual delay time is calculated from the equation:

EQUATION 3-7:

$$T_{TRDLY} = K/F_C$$

K is determined by [Table 3-12](#).

TABLE 3-12: TRDLY

| D4 | D3 | D2 | D1 | D0 | Decimal | K |
|----|----|----|----|----|---------|-----|
| 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 0 | 1 | 1 | 8 |
| 0 | 0 | 0 | 1 | 0 | 2 | 12 |
| 0 | 0 | 0 | 1 | 1 | 3 | 16 |
| 0 | 0 | 1 | 0 | 0 | 4 | 20 |
| 0 | 0 | 1 | 0 | 1 | 5 | 24 |
| 0 | 0 | 1 | 1 | 0 | 6 | 36 |
| 0 | 0 | 1 | 1 | 1 | 7 | 40 |
| 0 | 1 | 0 | 0 | 0 | 8 | 48 |
| 0 | 1 | 0 | 0 | 1 | 9 | 60 |
| 0 | 1 | 0 | 1 | 0 | 10 | 64 |
| 0 | 1 | 0 | 1 | 1 | 11 | 72 |
| 0 | 1 | 1 | 0 | 0 | 12 | 80 |
| 0 | 1 | 1 | 0 | 1 | 13 | 96 |
| 0 | 1 | 1 | 1 | 0 | 14 | 100 |
| 0 | 1 | 1 | 1 | 1 | 15 | 120 |
| 1 | 0 | 0 | 0 | 0 | 16 | 128 |
| 1 | 0 | 0 | 0 | 1 | 17 | 144 |
| 1 | 0 | 0 | 1 | 0 | 18 | 160 |
| 1 | 0 | 0 | 1 | 1 | 19 | 192 |
| 1 | 0 | 1 | 0 | 0 | 20 | 200 |
| 1 | 0 | 1 | 0 | 1 | 21 | 240 |
| 1 | 0 | 1 | 1 | 0 | 22 | 288 |

3.4.8.6 PSEL BIT

PSEL is the I²C bit that determines if PLEN or PEN controls the PLL enable.

TABLE 3-13: PSEL EFFECT

| PSEL | Controlling Signal |
|------|--------------------|
| 0 | PEN |
| 1 | PLEN |

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3.4.8.7 PLEN BIT

PLEN is the I²C bit that determines if the PLL is used when PSEL = 1.

TABLE 3-14: PLEN

| PLEN | PLL |
|------|-----|
| 0 | Off |
| 1 | On |

3.4.8.8 LOCKD BIT

LOCKD is the I²C bit that determines if the PLL is used when PSEL = 1.

TABLE 3-15: LOCKD

| LOCKD | PLL Locked? |
|-------|-------------|
| 0 | No |
| 1 | Yes |

3.4.8.9 EOT BIT

EOT is a read-only I²C bit that signals that the transmit signals are complete. EOT is a global signal looking at all 16 channels.

TABLE 3-16: EOT

| EOT | TX Complete? |
|-----|--------------|
| 0 | No |
| 1 | Yes |

3.4.8.10 BSEL BIT

BSEL is the I²C bit that determines if BFEN or BEN controls the output buffer enable.

TABLE 3-17: BSEL

| BSEL | Buffer Enable Signal |
|------|----------------------|
| 0 | BEN |
| 1 | BFEN |

3.4.8.11 SPISEL BIT

SPISEL determines which signal controls the broadcast enable.

TABLE 3-18: SPISEL

| SPISEL | Control Signal |
|--------|----------------|
| 0 | SPIB |
| 1 | SPIBC |

3.4.8.12 V(x)UV BITS

These five bits are output flags. They can be read, but not written. They signal an undervoltage on their respective power supply. V(x)UV can stand for: VNFUV, VPFUV, VPLLUV, VDDUV or VLLUV.

3.4.8.13 OTP BIT

OTP is an I²C bit that signals an overtemperature condition inside the HV7358 part. The flag is reset by the I²C reading of the ADDR = 01h register. If the overtemperature event continues, the flag will be retrigged at the next EN rising edge. See [Table 3-19](#).

3.4.8.14 BFEN BIT

BFEN is the I²C bit that determines the output buffer enable when BSEL = 1.

TABLE 3-19: BFEN FOR BSEL = 1

| OTP | Temperature |
|-----|-----------------|
| 0 | In Range |
| 1 | Overtemperature |

3.4.8.15 EOTC BIT

Determines when the RTZ+ and TRSW delay starts. If EOTC = 0, the period starts immediately after all channels are finished. If EOTC = 1, the period starts at the first F_C clock rising edge after ETI becomes high and after all channels finish the TX_{CH} period.

3.4.8.16 SPIBC BIT

Enables the SPI Broadcast mode when SPISEL = 1.

TABLE 3-20: SPIBC FOR SPISEL = 1

| SPIBC | |
|-------|----------|
| 0 | Disabled |
| 1 | Enabled |

3.4.8.17 Manually Read BUTTON

The **Manually Read** button will read and display the current values of the I²C registers.

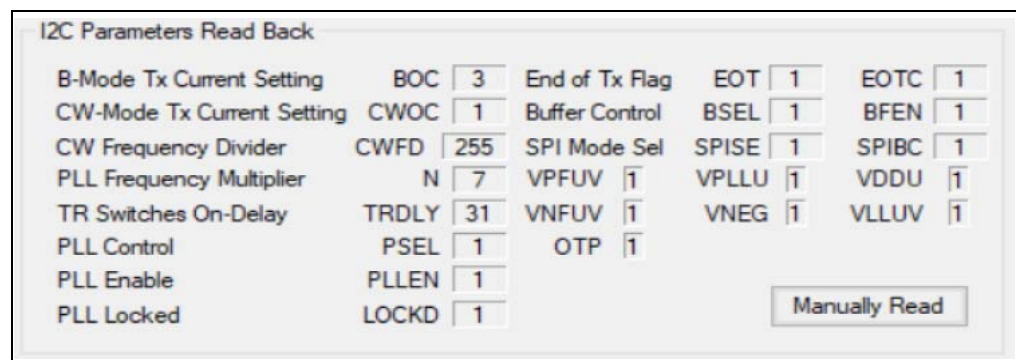


FIGURE 3-12: I²C Parameter Read Back Window.

3.4.9 Loading and Saving Table

The table function buttons are shown in [Figure 3-13](#) below.

A table is a file that stores all the data from the HV7358 GUI. It will save the “HV7358 Pin Settings”, “Transmit Clock Frequency”, “Line Duration”, “TRSW Low Time”, “Waveform Definition” and “TCK Cycles” data.

When the GUI is closed, the data are automatically saved in the default file:

C:\Users\Public\Documents\hv7358db1_GUI.json

The **Save Table** button will save all the settings to the default file. The **Save Table As** button will ask for a unique filename to save to. The **Load Table** will ask for the filename to be loaded.

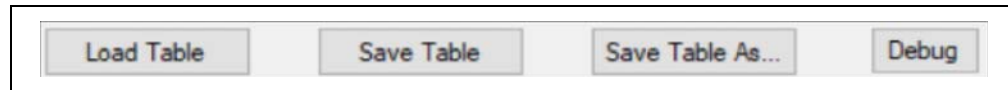


FIGURE 3-13: Table Function Buttons.

3.4.10 Invert and Individual Delay and Pulse-Width Control

This GUI window is shown in [Figure 3-14](#).

INV: Will invert every waveform. By default, the first pulse is positive. With INV checked, the first pulse will be negative. This is a global control bit. It will be the same for each TX channel and each waveform.

Delay: Each channel can have its own unique delay. The starting point is TGW, which sets the longest delay. For details, see [Section 3.4.7 “Waveform Definition”](#). TGW is the maximum delay time and is common to all channels. The total delay can be decreased, on a per channel basis, with the Delay bit. Delay is a 12-bit word. The GUI will accept anything from 0 to 4095.

The delay for each channel will be:

EQUATION 3-8:

$$TIMEDELAY_X = (TGW - DELAY_X) \times (1/F_{TCK})$$

This allows a unique time delay for each channel.

TLP and TLN: Each channel and polarity can have its own unique pulse width. The starting point is P_W , which sets the longest pulse width. For details, see [Section 3.4.7 “Waveform Definition”](#). P_W is the maximum delay time and is common to all channels. The total delay can be decreased, on a per channel, per polarity basis, with the TLPx and TLNx bits.

The pulse for each channel will be:

EQUATION 3-9:

$$POSITIVE PULSE WIDTH_X = (P_W - TLP_x) \times (1/F_{TCK})$$

EQUATION 3-10:

$$NEGATIVE PULSE WIDTH_X = (P_W - TLN_x) \times (1/F_{TCK})$$

This allows a unique pulse width for each polarity of each channel.

The screenshot displays a configuration window for the HV7358DB1. At the top, there is a section for 'Entry TCK Cycles' with three checkboxes: 'INV' (unchecked), 'LPWM' (unchecked), and 'Wave(0-3)' (set to '0'). Below this is a table with three columns: 'DELAY(12)', 'TLP(7)', and 'TLN(7)'. The rows represent channels from CH0 to CH15. Each channel has a numerical value in the 'DELAY' column and '2' in both the 'TLP' and 'TLN' columns.

| | DELAY(12) | TLP(7) | TLN(7) |
|------|-----------|--------|--------|
| CH0 | 10 | 2 | 2 |
| CH1 | 15 | 2 | 2 |
| CH2 | 20 | 2 | 2 |
| CH3 | 25 | 2 | 2 |
| CH4 | 30 | 2 | 2 |
| CH5 | 35 | 2 | 2 |
| CH6 | 40 | 2 | 2 |
| CH7 | 45 | 2 | 2 |
| CH8 | 50 | 2 | 2 |
| CH9 | 55 | 2 | 2 |
| CH10 | 60 | 2 | 2 |
| CH11 | 65 | 2 | 2 |
| CH12 | 70 | 2 | 2 |
| CH13 | 75 | 2 | 2 |
| CH14 | 80 | 2 | 2 |
| CH15 | 85 | 2 | 2 |

FIGURE 3-14: Invert and Individual Delay and Individual Pulse-Width Control.

3.5 RUNNING THE HV7358DB1

1. Connect the scope probes to the appropriate signals.
2. Turn on the power supplies, observing the power-up sequence in [Table 3-3](#).
3. Click on the **Start** button. The HV7358DB1 is now running.

3.6 STOPPING THE HV7358DB1

1. Click on the **Stop** button.
2. Power down the power supplies, observing the power-down sequence in [Table 3-3](#).
3. Complete.

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3.7 SAMPLE WAVEFORM

A sample of the waveform generation is shown in [Figure 3-15](#).

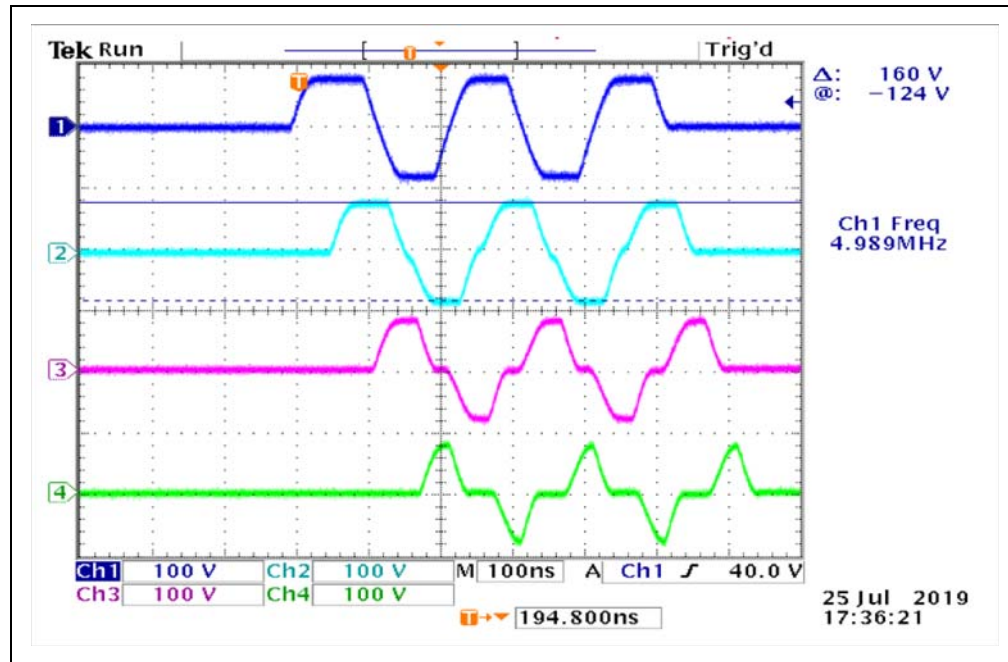


FIGURE 3-15: Sample Waveform from Multiple Channels of the HV7358.

Chapter 4. MUPB002 FPGA Configuration

4.1 INTRODUCTION

The MUPB002 board connects to and controls the HV7358DB1. It connects to the host PC and interfaces with the GUI. The MUPB002 is preprogrammed and ready for immediate use. However, if changes in the code are required, the directions below will allow changes to the configuration.

4.2 HARDWARE AND SOFTWARE REQUIRED

4.2.1 Hardware Required

- MUPB002 Board
- Type A Male to Type Micro-B Male USB Cable
- Xilinx® Platform Cable USB II

4.2.2 Software Required

- “Xilinx ISE Design Suite 14.7” must be installed to the host PC.
- FPGA configuration file, `hv7358_top_main.bit`, available from the Microchip website.
- Flash memory configuration file, `HV7358_BVLDS_TRIG.mcs`, available from the Microchip website.

4.3 SETUP PROCEDURE

This procedure explains how to reconfigure the Flash memory (U15) on MUPB002. After the Flash memory is reconfigured, the latest configuration is automatically used when the MUPB002 powers up.

Note: The Flash memory has been configured at the factory. This chapter is ONLY required when the default program needs to be changed.

1. Connect a USB cable (M-to-M, Type A to Type Micro-B) between the PC and the Micro-B USB female (J7) connector of MUPB002. This connection powers up the MUPB002 board. LED4 will light up, showing the MUPB002 is being powered through the USB cable.
2. Connect the Xilinx Platform Cable USB II hardware between the PC and J4 connector of MUPB002. The light of the platform cable turns on in green.

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4.4 SOFTWARE EXECUTION

1. Start the iMPACT tool of Xilinx by clicking on the iMPACT icon. See [Figure 4-1](#).

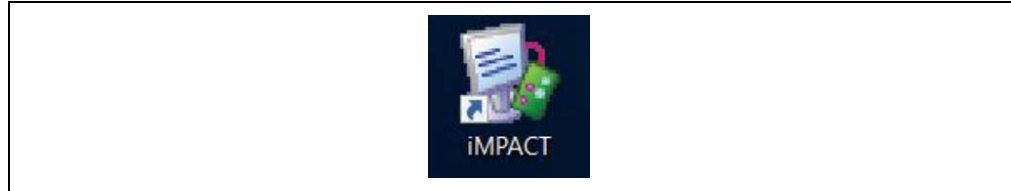


FIGURE 4-1: iMPACT Icon.

2. The window in [Figure 4-2](#) will appear.
3. Left click on “Boundary Scan” as shown in [Figure 4-2](#).
4. Right click on top of the “Right click to Add Device or Initialize JTAG chain” statement.

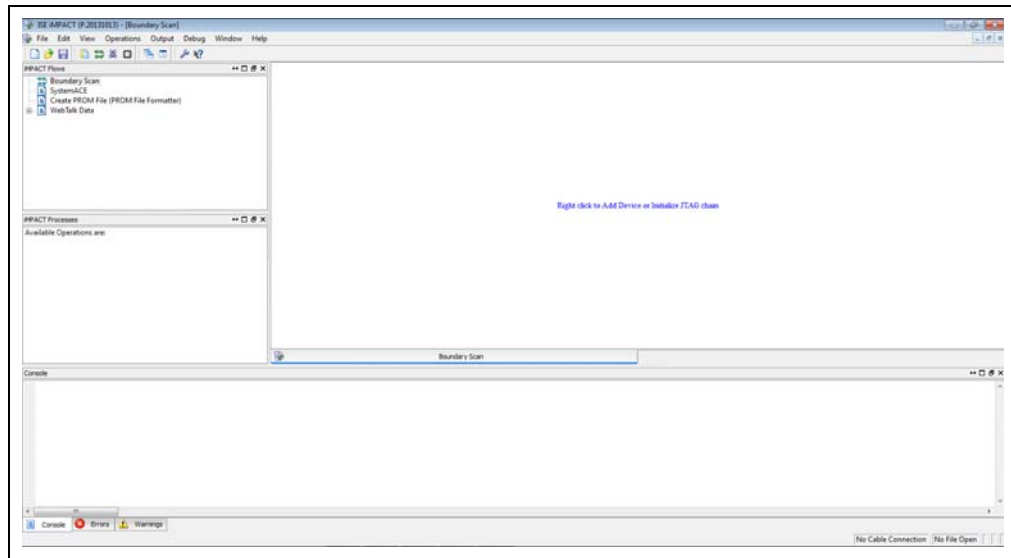


FIGURE 4-2: iMPACT Window.

5. Choose “Add Xilinx Device...” from the menu and click.

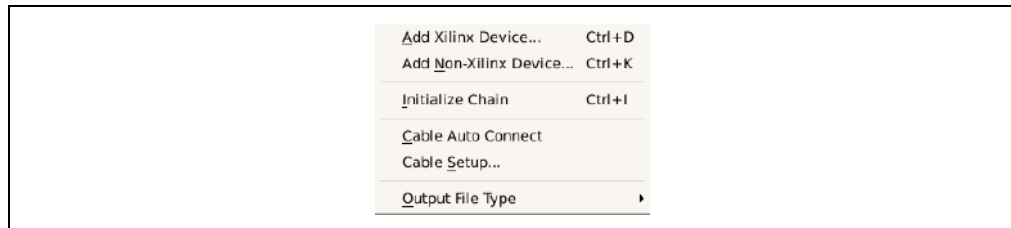


FIGURE 4-3: Xilinx Setup Window.

MUPB002 FPGA Configuration

The window in Figure 4-4 will appear. The actual files are a function of what is on your PC. They will not match Figure 4-4.

6. Browse in your PC to the file, hv7358_top_main.bit. Then click on the **Open** button.

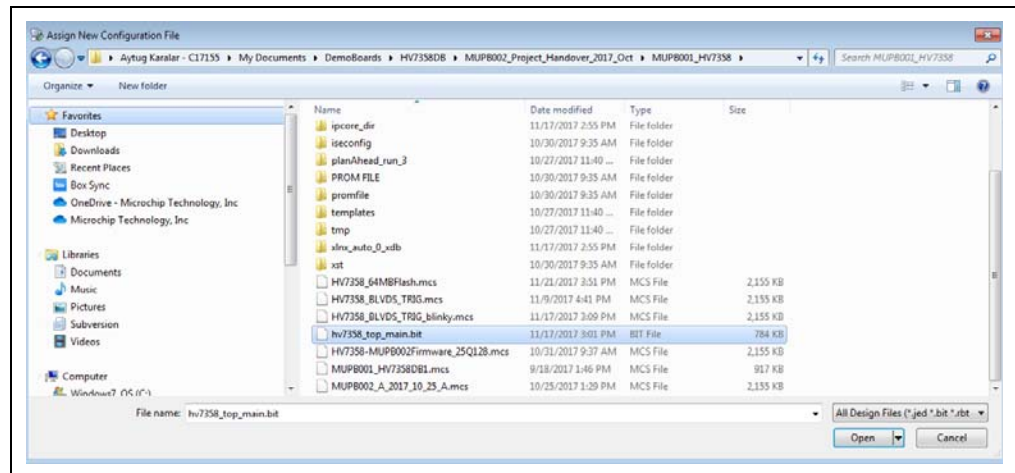


FIGURE 4-4: Assign New FPGA Configuration File Selection.

The window in Figure 4-5 will appear. Only the upper right corner of the window is shown for clarity. It shows an external block diagram of the FPGA (xc6slx25). Now we will choose the Flash memory that we want to configure.

7. Right click on the “SPI/BPI?” statement on top of the FPGA symbol.

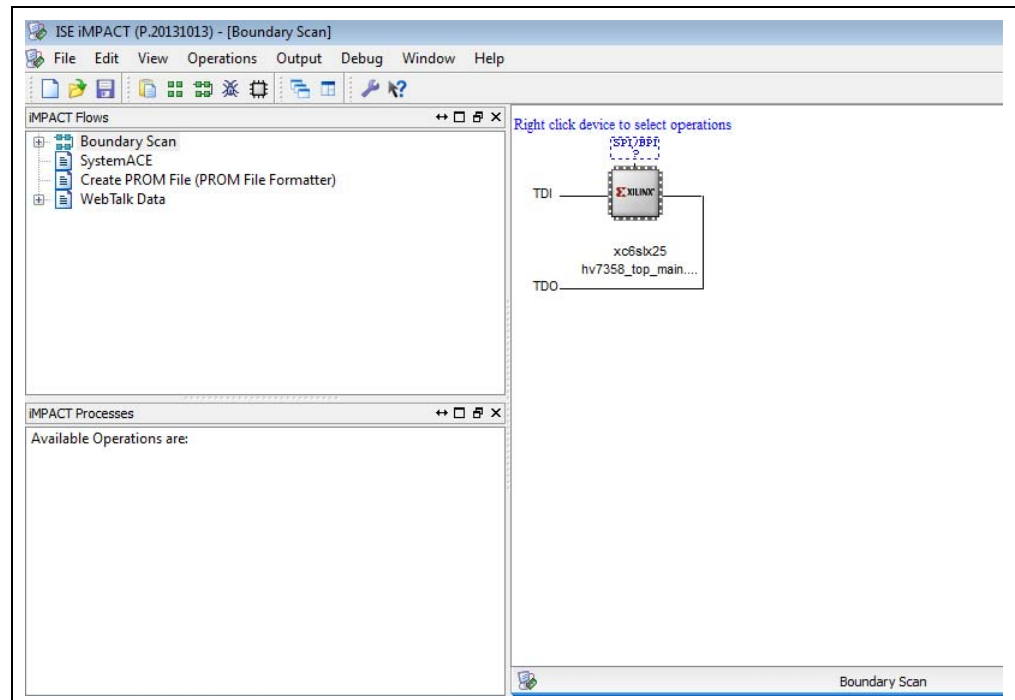


FIGURE 4-5: SPI/BPI Window.

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The small box with “Add SPI/BPI Flash” will appear (see [Figure 4-6](#)).

8. Click on the “Add SPI/BPI Flash...” box.

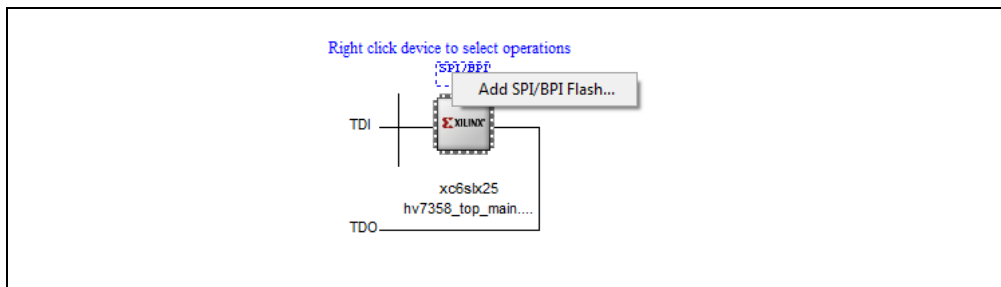


FIGURE 4-6: “Add SPI/BPI Flash...” Box.

The box in [Figure 4-7](#) will appear.

9. Browse to the file named, HV7358_BLVDS_TRIG.mcs.
10. Click on the **Open** button.

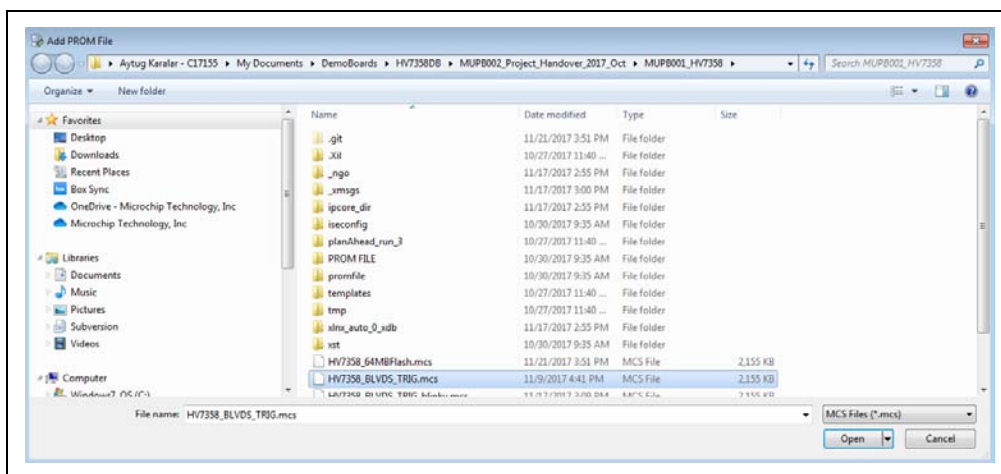


FIGURE 4-7: SPI/BPI File Choice.

The window in [Figure 4-8](#) will appear.

11. Select “S25FL128S” for the 128 MB Flash memory (U15) installed on the MUPB002 board.
12. Click the **OK** button.

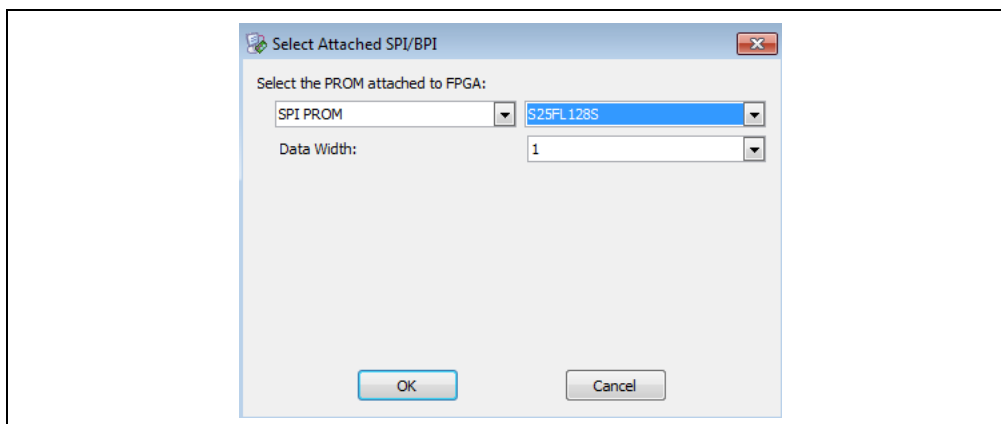


FIGURE 4-8: Select Attached SPI/BPI Window.

MUPB002 FPGA Configuration

Figure 4-9 shows the upper left part of the next window.

13. There is a **FLASH** button in the upper right. Click on it.

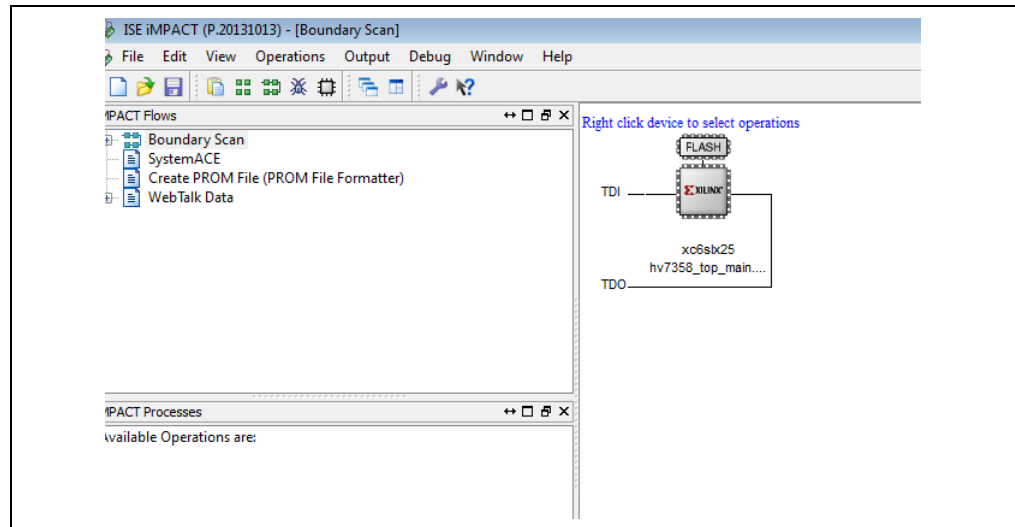


FIGURE 4-9: *FLASH Button.*

The **FLASH** button will turn green as shown in Figure 4-10.

14. Click on the green **FLASH** button.

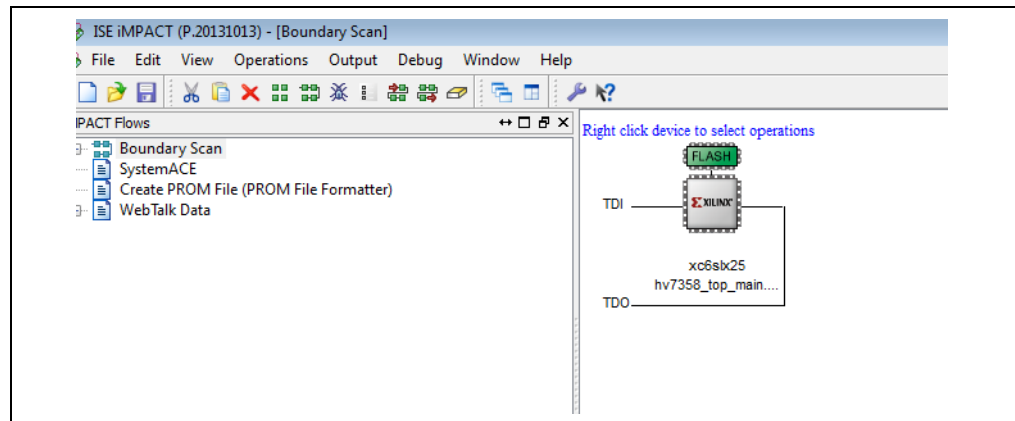


FIGURE 4-10: *Green FLASH Button.*

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The Device Programming Properties window, shown in [Figure 4-11](#), will appear.
15. Click the **OK** button.

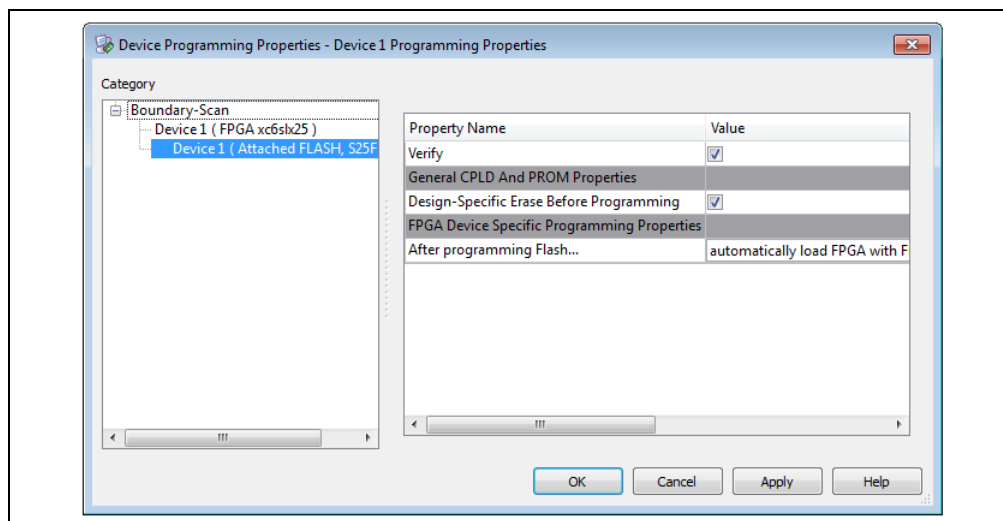


FIGURE 4-11: Device Programming Properties Window.

The FPGA will be programmed. This may take over a minute.
When completed, the window in [Figure 4-12](#) will appear.

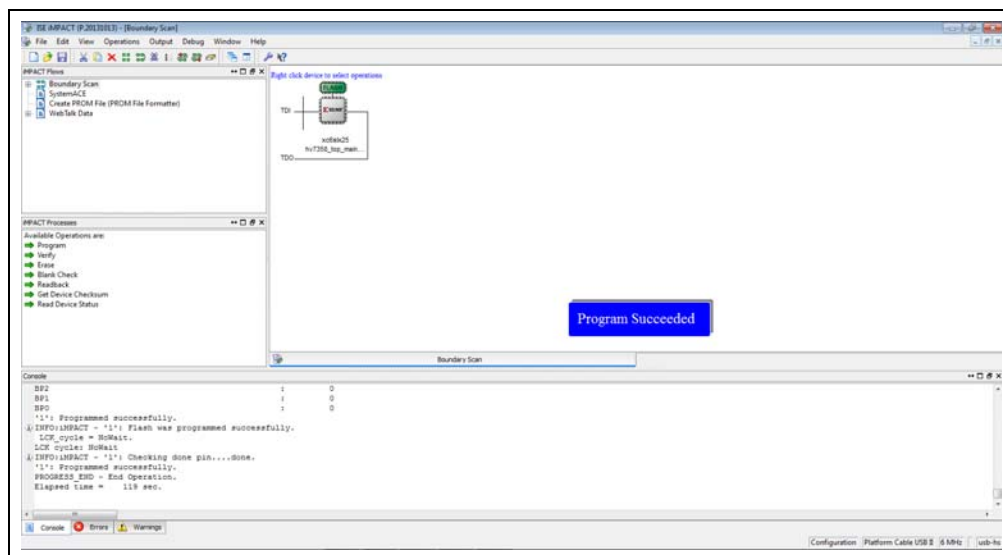


FIGURE 4-12: Complete Window.

4.5 CONCLUSION

A procedure to program the MUPB002 FPGA for use with the HV7358DB1 has been presented. This procedure with different file names can be used to program the MUPB002 for different Microchip ultrasound transmitters.

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NOTES:

Chapter 5. PCB Design and Layout Techniques

5.1 INTRODUCTION

The PCB layout techniques are a very important part of the ultrasound system design. The HV7358DB1 generates high-voltage, high-current, high-frequency and high-speed pulses. Proper PCB layout is required to optimize the waveforms.

5.1.1 High-Speed Trace, Grounding and Heatsinking PCB Design Techniques

A solid GND plane must be created. It should be a solid copper layer, on Layer 2, directly under HV7358.

To optimize heatsinking of the HV7358, use as many vias from V_{SUB} , RGND and GND to the GND plane as possible. These signals carry large currents. Their PCB traces should be on the top layer; they should be as short as possible and have as many vias as possible. Maximize the number of vias on all the power supply traces.

High-speed (200 MHz) PCB trace design practices should be used as a starting point. The TX outputs are high-voltage and high-speed traces. V_{PP} and V_{NN} are high-voltage and high-current traces. Additional trace spacing may be required for the high-voltage traces. Also, any parasitic coupling from the HV7358 TX outputs to digital input signals may cause error signals on the logic input pins. Adequate spacing and possible isolation are required. Additional width is required for the high-current traces.

5.1.2 Bypass Caps

The V_{LL} , V_{DD} , V_{GP} , V_{GN} , $V_{PP}/1$ and $V_{NN}/1$ power supply pins, and the CPF0/1, CNF0/1, CPOS and CNEG internal gate driver floating supply rails all require bypass capacitors. All can draw fast transient currents of up to 2.8 Amperes each. X7R or X5R-type capacitors, 1.0 to 2.2 μ F are recommended. They must be located as close to the HV7358 pins as possible. PCB trace width should be capable of handling these transients.

5.1.3 PCB Layout Techniques for TCKP/TCKN

The clock can be driven with a pair of LVDS connections or a single-ended clock.

For LVDS implementations, an 100 Ω differential termination resistor must be connected as close as possible to the LVDS input pair.

LVDS clock traces on the PCB should be designed as two 50 Ω transmission lines with respect to the GND plane. The differential traces should be as close as possible after they leave the LVDS buffer IC.

With a single-ended clock, a 33 Ω series termination resistor is required for each buffer output. These resistors should be as close to the clock buffer output pin as possible. The clock trace on the PCB should be designed as a 50 Ω transmission line with respect to the GND plane.

5.1.4 Decoupling Capacitors

The PCB layout decoupling capacitor's placement rule is simple: place the capacitor as close as possible to the pin being decoupled. The actual placement of the capacitor may generate EMI/RFI. The placement determines the return current path. The return path is from the GND side of the bypass cap, through the PCB trace, through any vias, through the GND plane and back to the GND pin on the HV7358. This path also needs to be as short as possible. There are also high current spikes from the VPP and VNN supplies to the HV7358 TX outputs. Use the same design rules with TX output traces and vias.

5.1.5 Return Current Design in PCB Layout

Many EMI problems associated with the high-speed circuits are due to improper design of the return current path. PCB designers put considerable effort into carefully designing traces with the proper length, proper transmission line impedance, etc., but neglect the return current path that completes the current loop. These EMI problems can usually be avoided with proper design of the return current path.

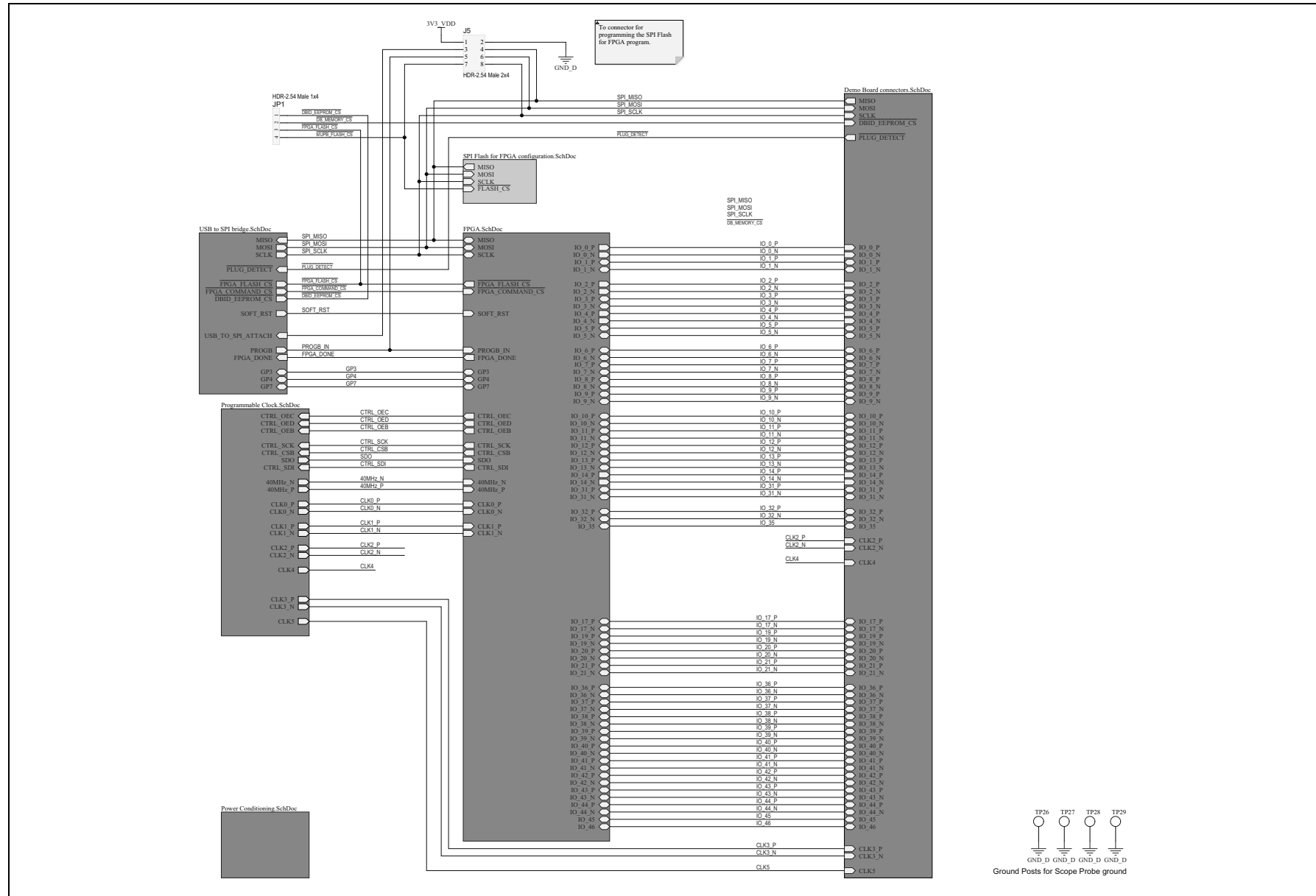
Appendix A. HV7835DB1 and MUPB002 Schematics and Layouts

A.1 INTRODUCTION

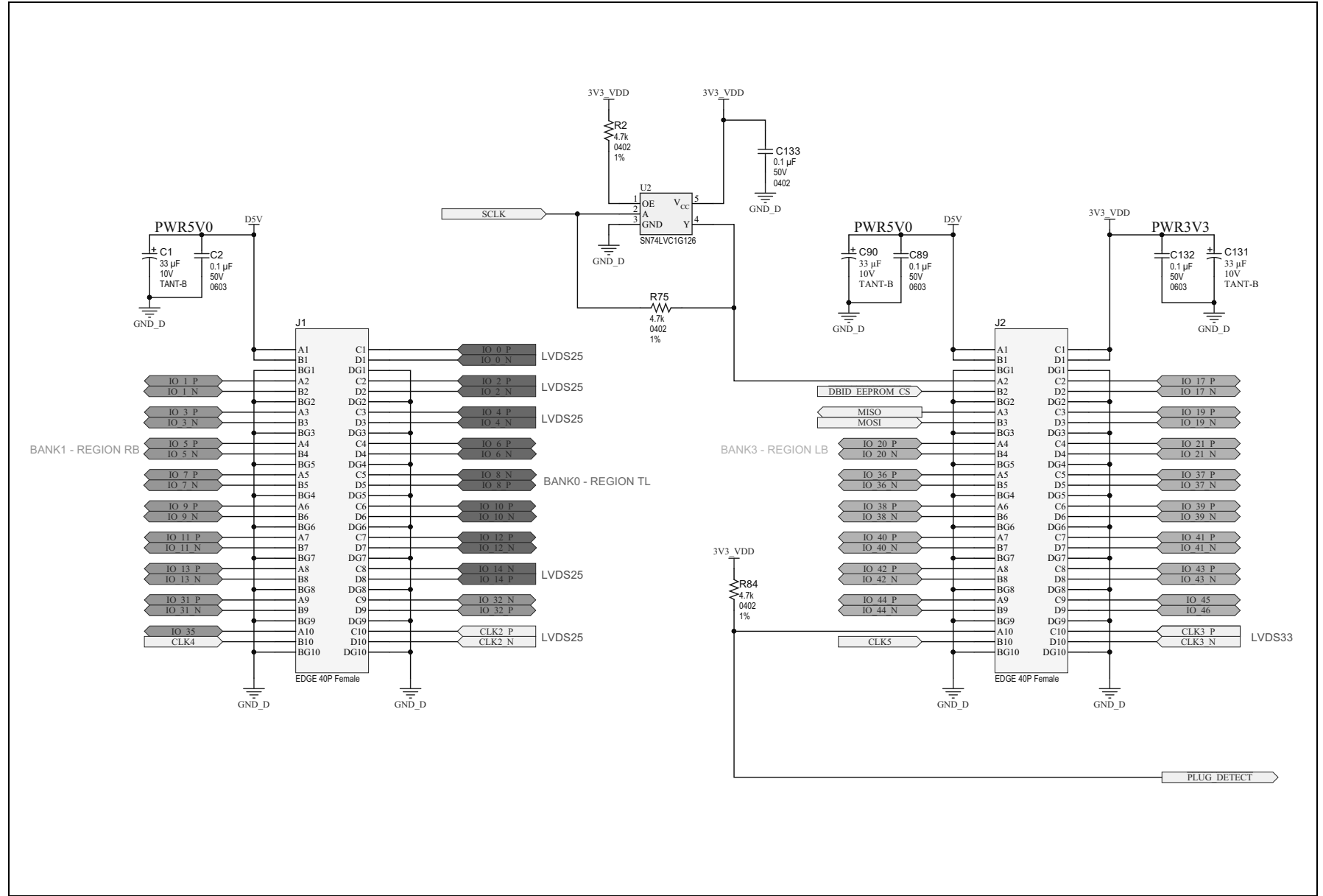
This appendix contains the following schematics and layouts for the HV7358DB1 and MUPB002:

- [HV7358DB1 – Schematic](#)
- [MUPB002 Schematic – Top Block Diagram](#)
- [MUPB002 Schematic – Demo Board Connectors](#)
- [MUPB002 Schematic – FPGA](#)
- [MUPB002 Schematic – SPI Flash for FPGA Configuration](#)
- [MUPB002 Schematic – Programmable Clock](#)
- [MUPB002 Schematic – FPGA Decoupling Capacitors](#)
- [HV7358DB1 – Top Silk](#)
- [HV7358DB1 – Top Copper and Silk](#)
- [HV7358DB1 – Top Copper](#)
- [HV7358DB1 – Bottom Copper](#)
- [HV7358DB1 – Bottom Copper and Silk](#)
- [HV7358DB1 – Bottom Silk](#)
- [MUPB002 – Top Silk](#)
- [MUPB002 – Top Copper and Silk](#)
- [MUPB002 – Top Copper](#)
- [MUPB002 – Bottom Copper](#)
- [MUPB002 – Bottom Copper and Silk](#)
- [MUPB002 – Bottom Silk](#)

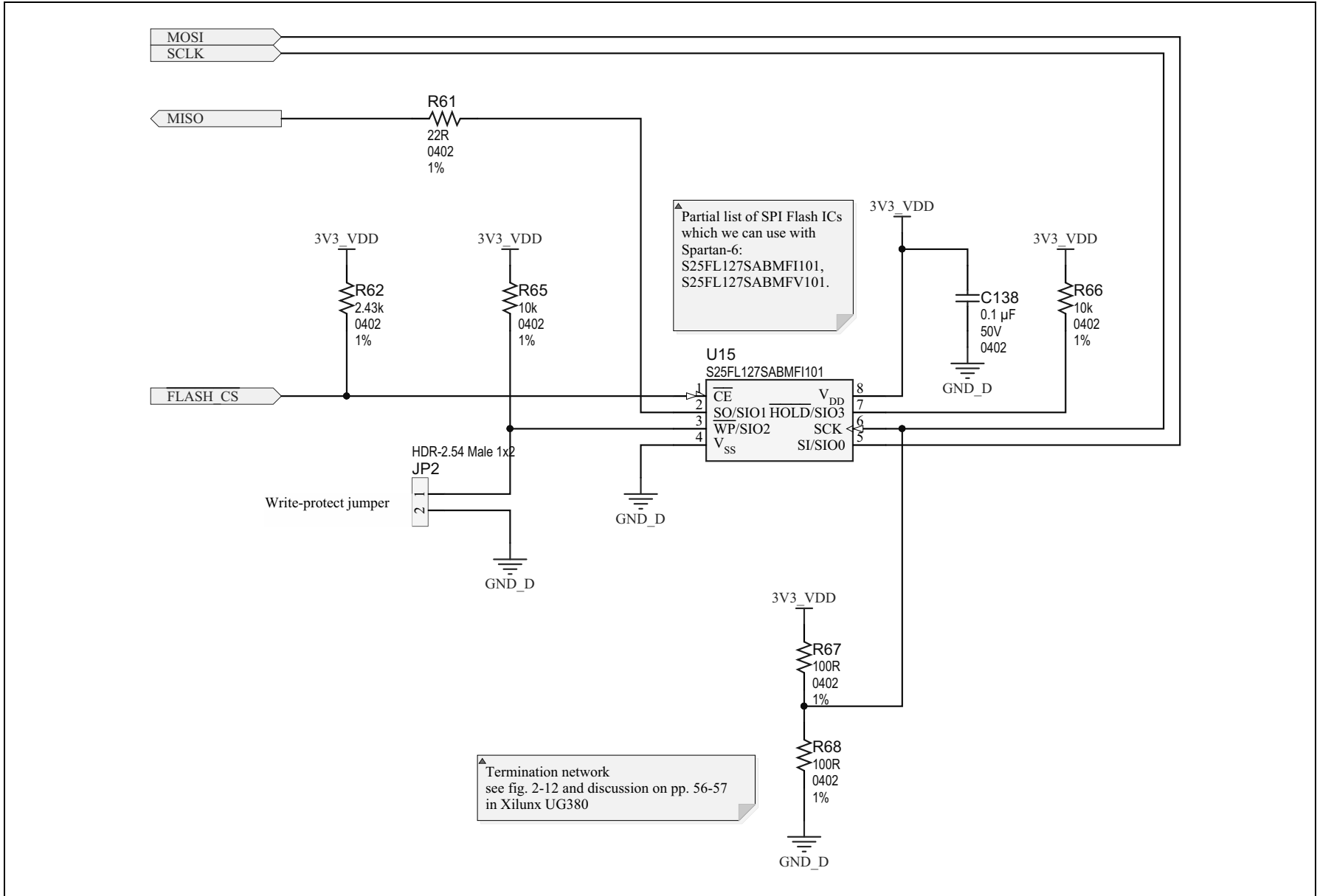
A.3 MUPB002 SCHEMATIC – TOP BLOCK DIAGRAM



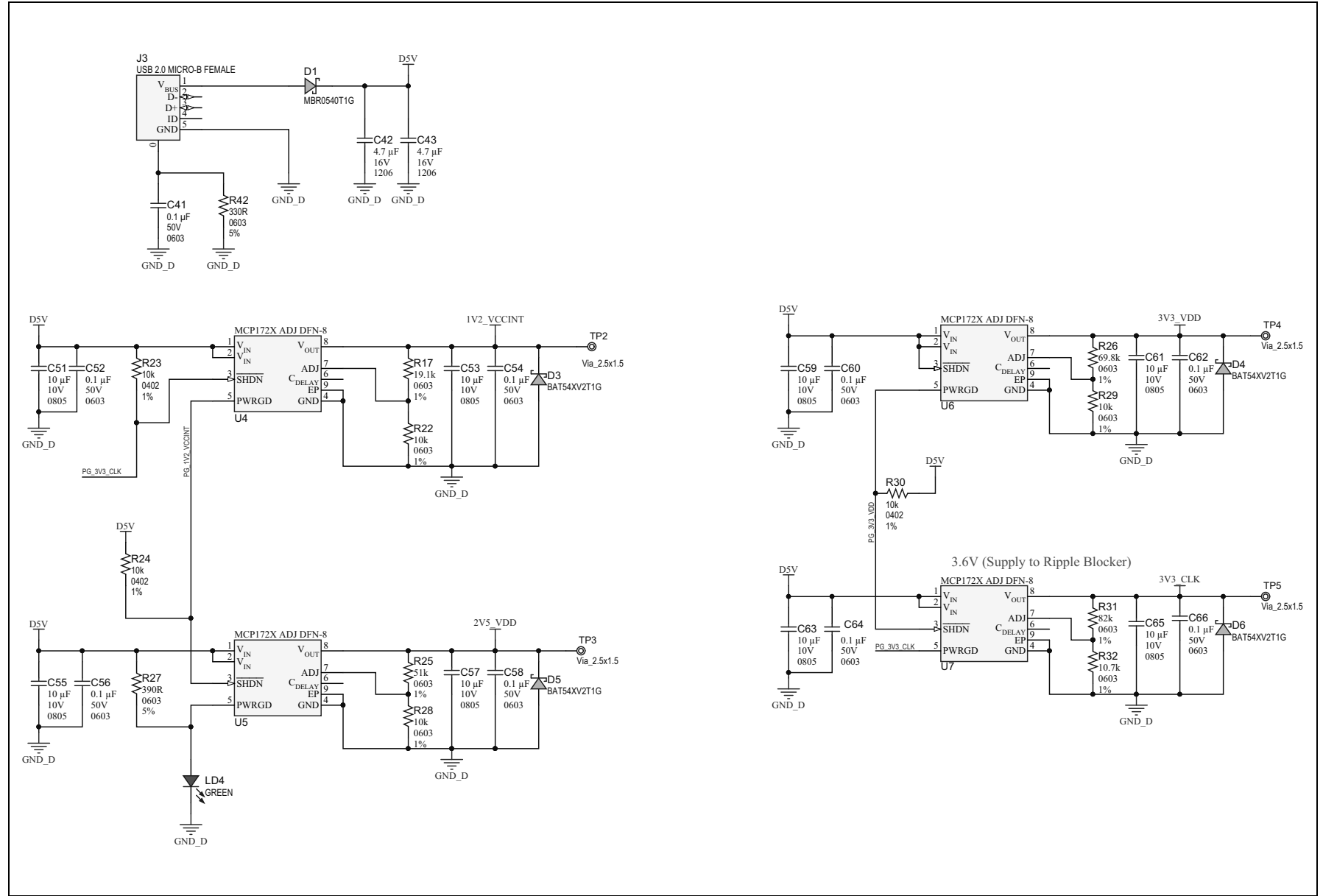
A.4 MUPB002 SCHEMATIC – DEMO BOARD CONNECTORS



A.6 MUPB002 SCHEMATIC – SPI FLASH FOR FPGA CONFIGURATION

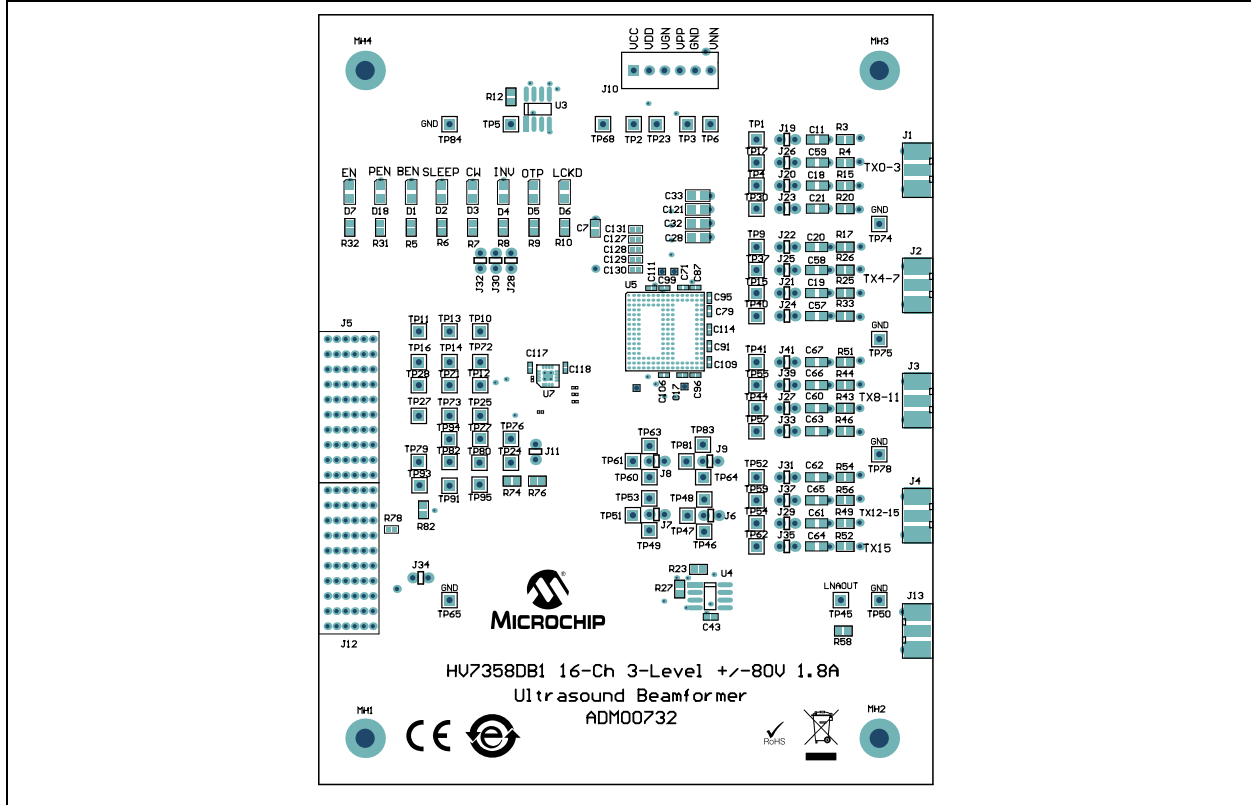


A.8 MUPB002 SCHEMATIC – FPGA DECOUPLING CAPACITORS

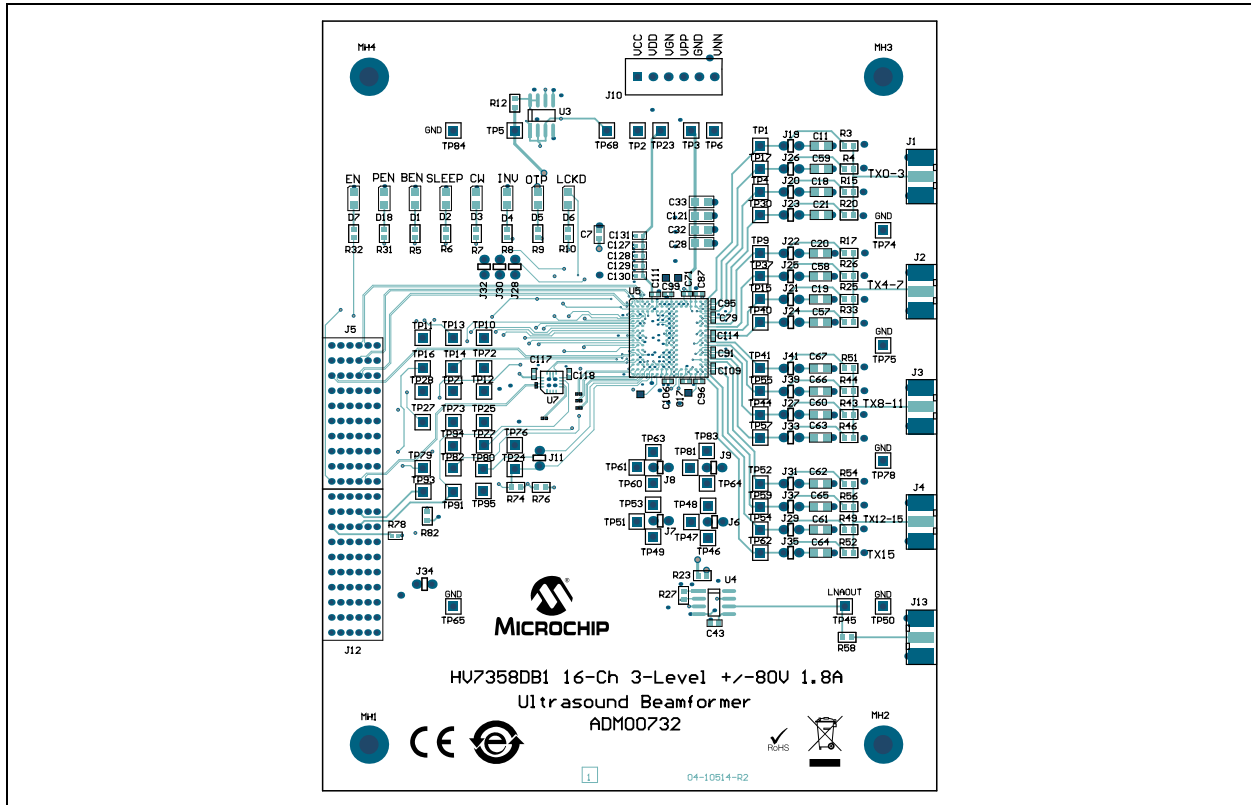


HV7358DB1 and MUPB002 Schematics and Layouts

A.9 HV7358DB1 – TOP SILK

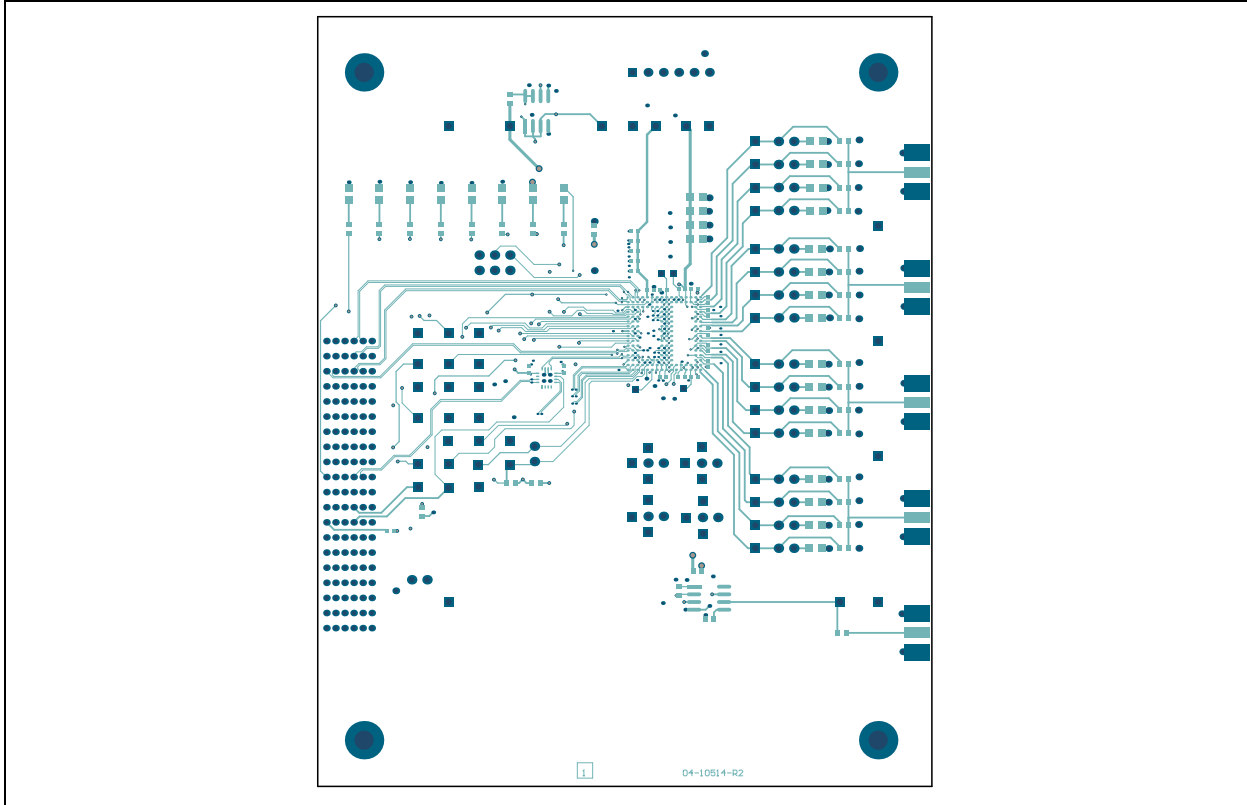


A.10 HV7358DB1 – TOP COPPER AND SILK

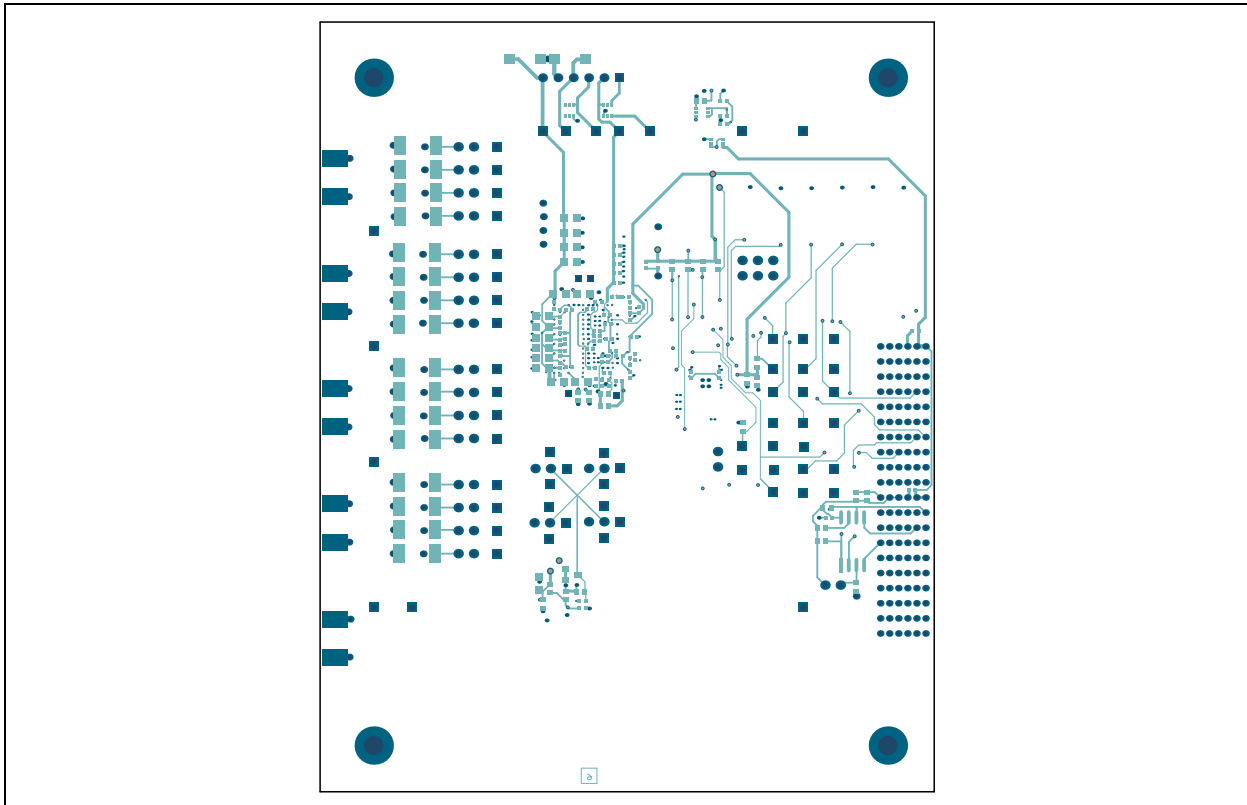


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A.11 HV7358DB1 – TOP COPPER

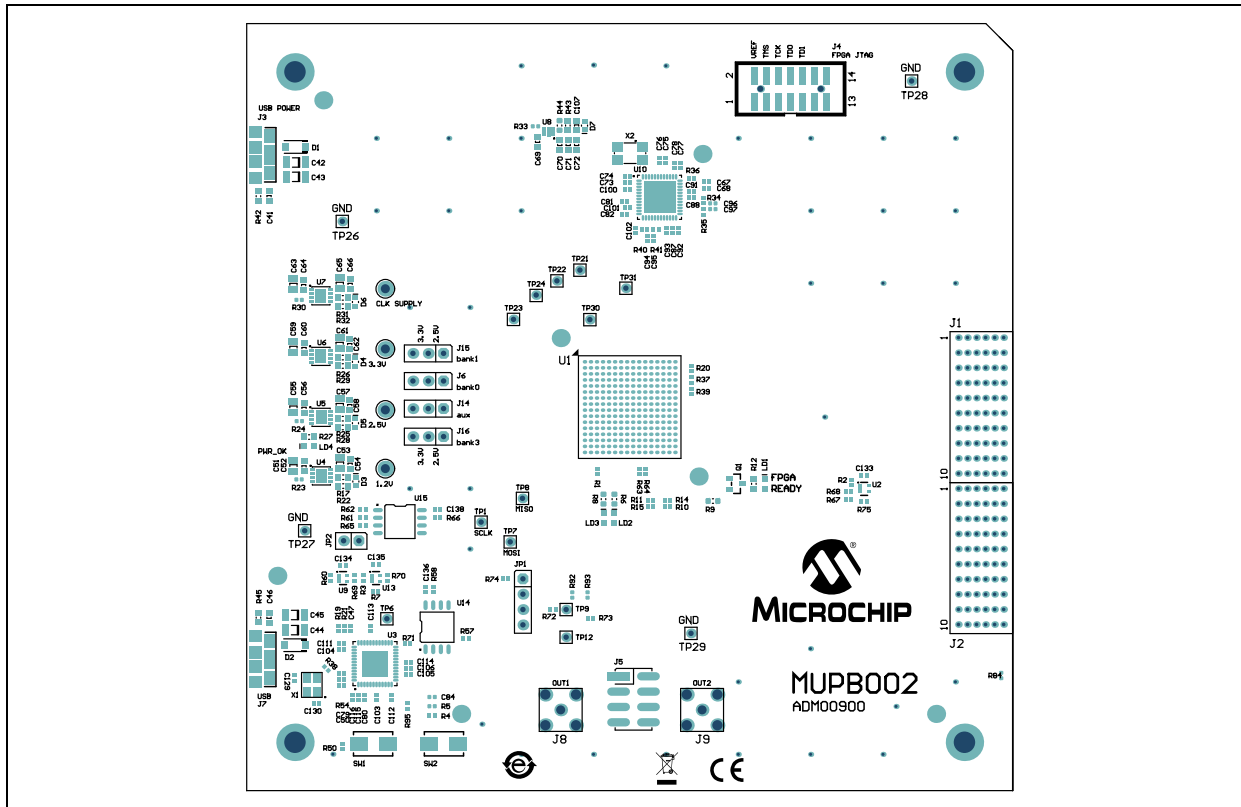


A.12 HV7358DB1 – BOTTOM COPPER

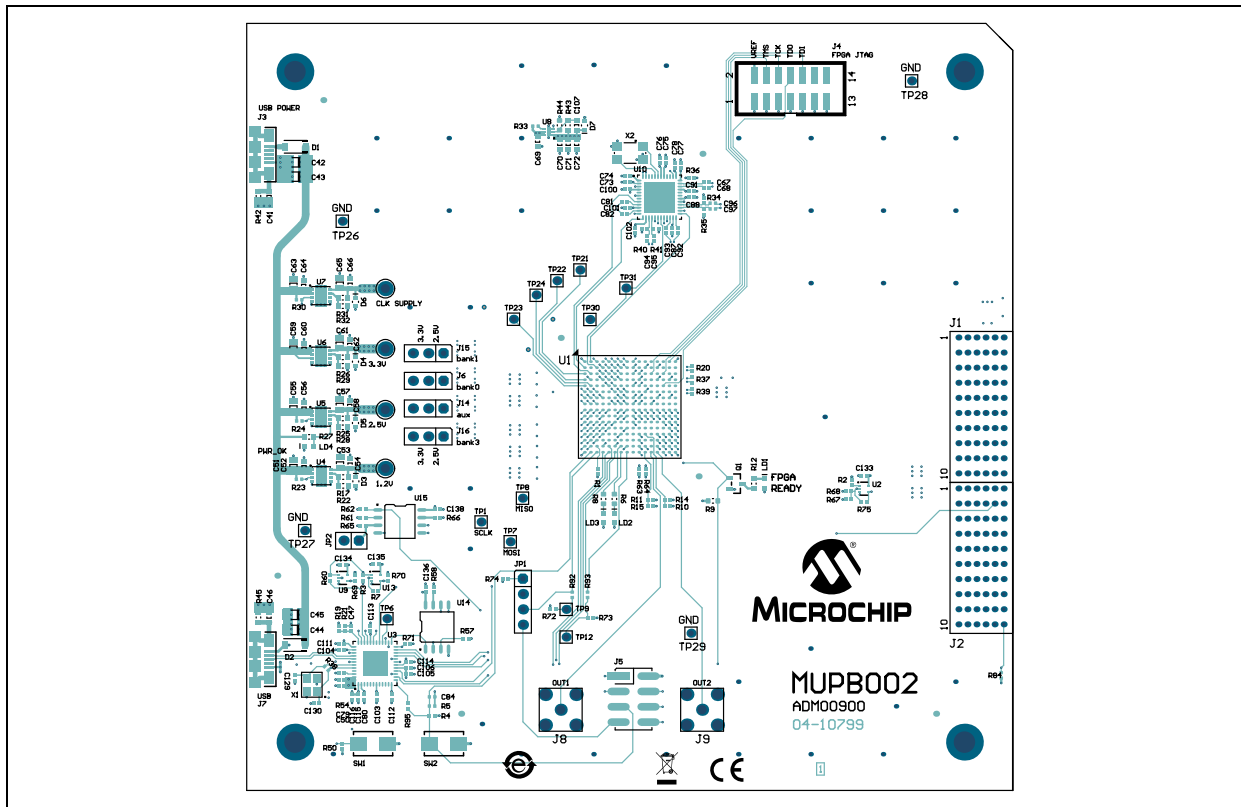


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A.15 MUPB002 – TOP SILK

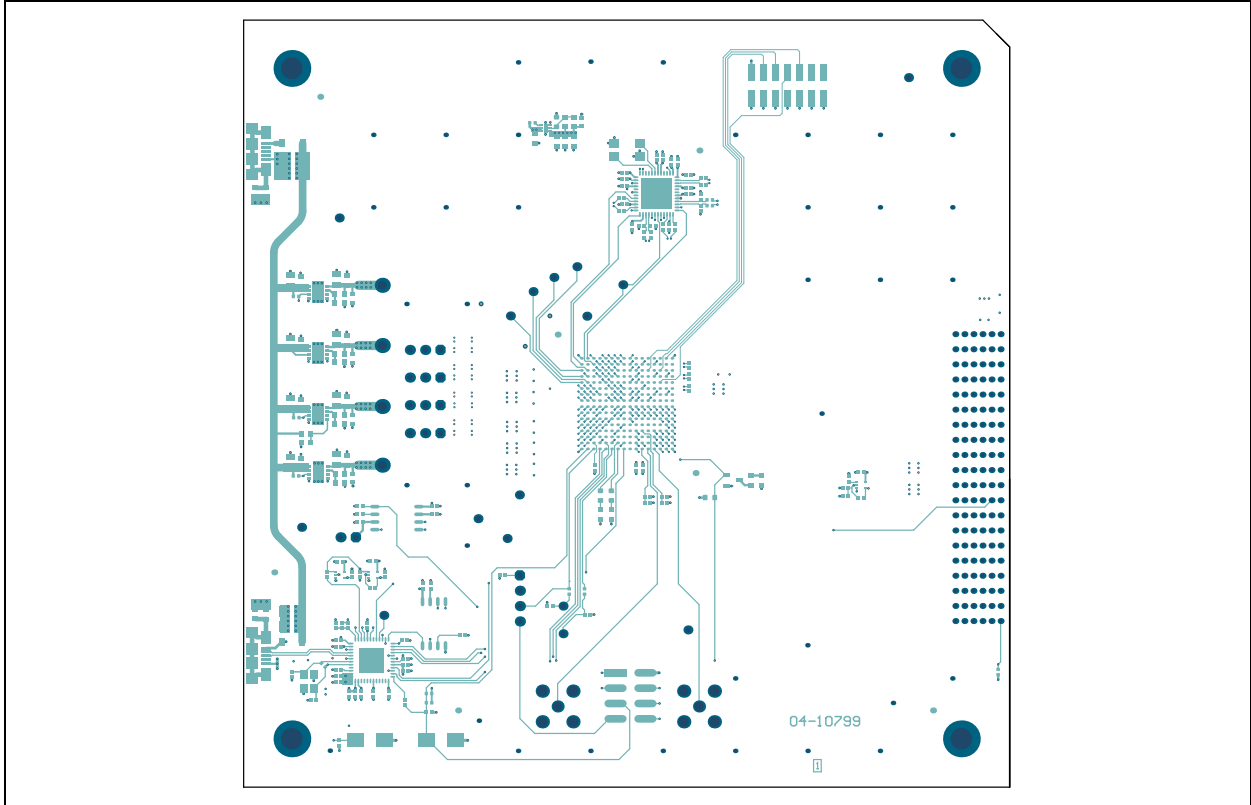


A.16 MUPB002 – TOP COPPER AND SILK

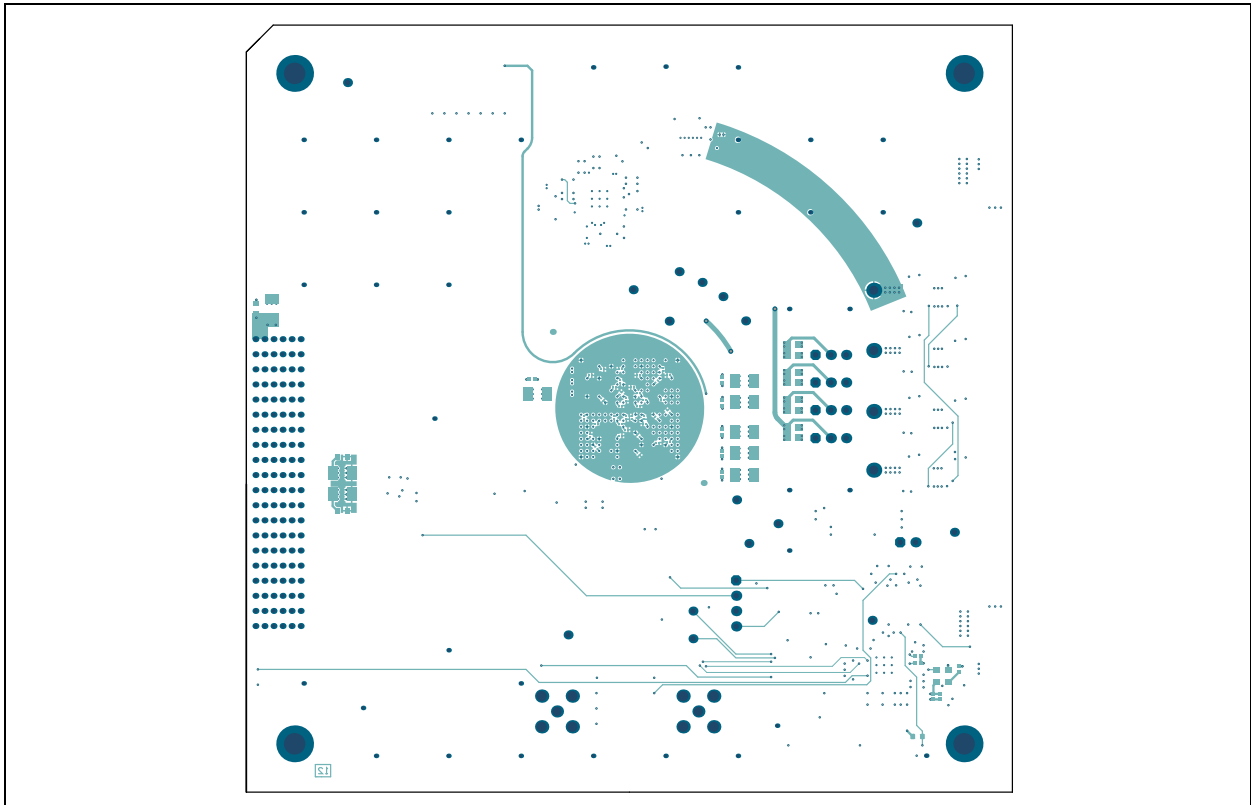


HV7358DB1 and MUPB002 Schematics and Layouts

A.17 MUPB002 – TOP COPPER

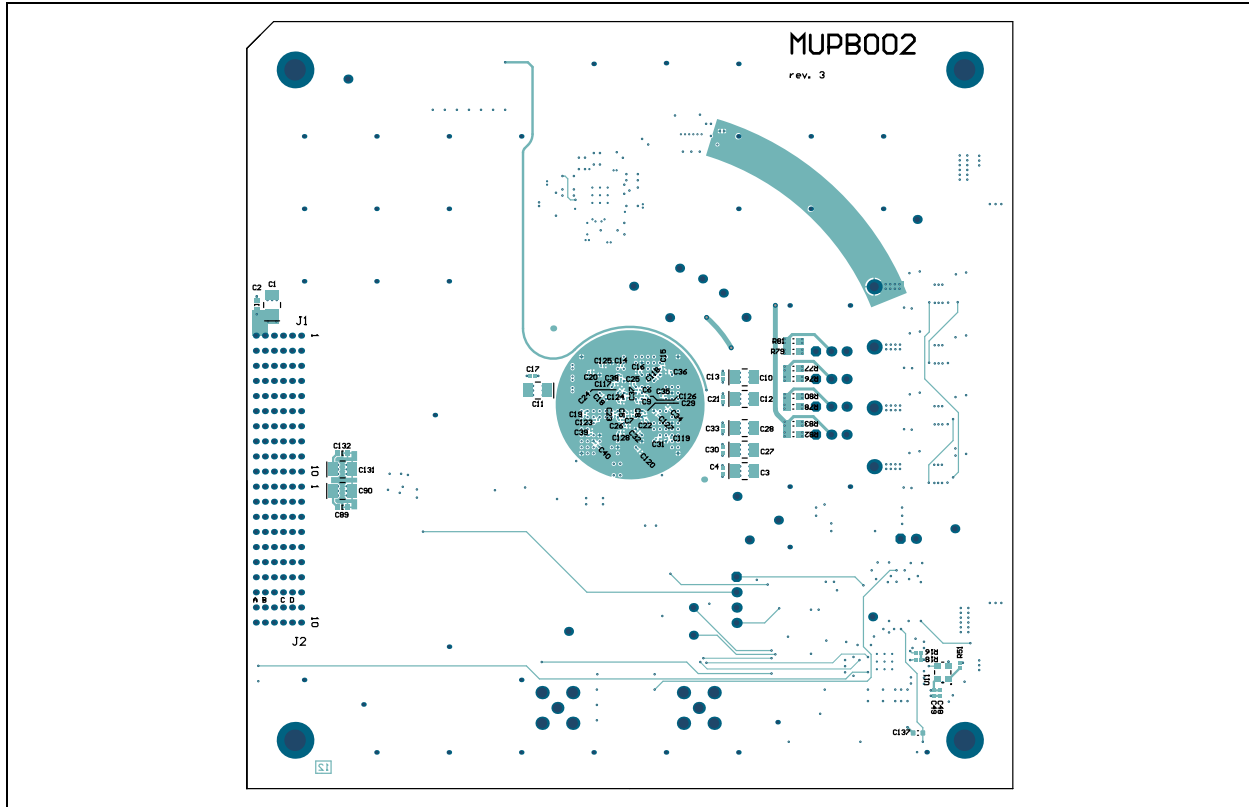


A.18 MUPB002 – BOTTOM COPPER

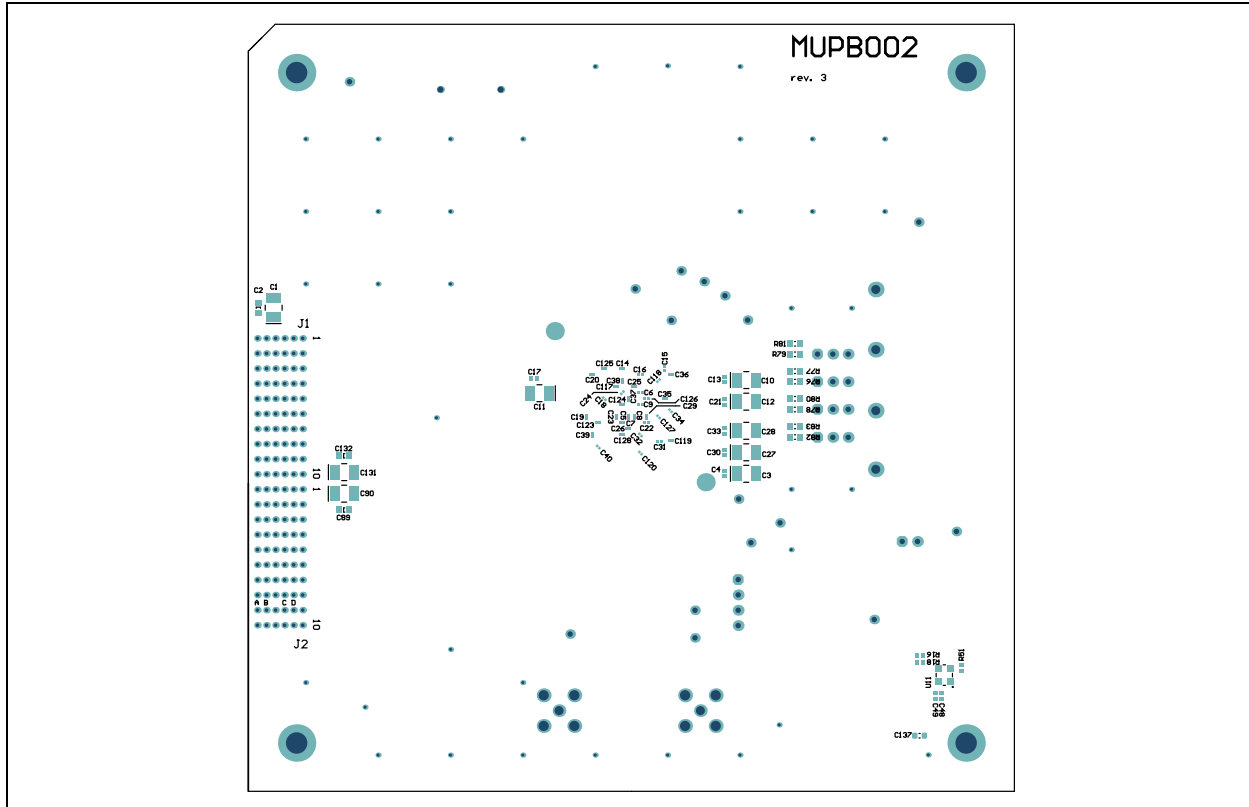


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A.19 MUPB002 – BOTTOM COPPER AND SILK



A.20 MUPB002 – BOTTOM SILK



Appendix B. Bill of Materials (BOM)

TABLE B-1: HV7358DB1 BILL OF MATERIALS (BOM)⁽¹⁾

| Qty. | Reference | Description | Manufacturer | Part Number |
|------|--|--|--------------------------|----------------------|
| 16 | C11, C18-21, C57-67 | Capacitor, Ceramic, 330 pF, 250V, U2J, 0805 | Murata Electronics® | GCM21A7U2E331JX01D |
| 3 | C112, C116, C119 | Capacitor, Ceramic, 0.1 µF, 10V, 10%, X7R, 0402 | TDK Corporation | C1005X7R1A104K050BB |
| 18 | C3-6, C10, C12-14, C22, C25-28, C32-33, C98, C120-121 | Capacitor, Ceramic, 1 µF, 100V, 10%, X7S, 0805 | TDK Corporation | CGA4J3X7S2A105K125AB |
| 1 | C36 | Capacitor, Ceramic, 10 µF, 16V, X5R, 0805 | Yageo Corporation | CC0805KKX5R6BB106 |
| 4 | C41, C42, C117, C118 | Capacitor, Ceramic, 10000 pF, 50V, ±10%, X7R, 0402 | TDK Corporation | CGA2B3X7R1H103K050BB |
| 1 | C43 | Capacitor, Ceramic, 2.0 pF, 50V, 0603 | Panasonic® - ECG | CGJ3E2C0G1H020C080AA |
| 1 | C51 | Capacitor, Ceramic, 1000 pF, 16V, X7R, 0603 | AVX Corporation | 0603YC102KAT2A |
| 5 | C7, C15, C23, C24, C29 | Capacitor, Ceramic, .22 µF, 16V, X7R, 10%, 0603 | TDK Corporation | C1608X7R1C224K |
| 18 | C75-78, C80-81, C90, C92, C93, C100-106, C108, C110 | Capacitor, Ceramic, 1 µF, 16V, X5R, 0402 | TDK Corporation | CGB2A1X5R1C105M033BC |
| 8 | C8, C30-31, C46, C74, C99, C111, C113 | Capacitor, Ceramic, 1 µF, 10V, X7S, 0402 | TDK Corporation | C1005X7S1A105K050BC |
| 36 | C9, C16-17, C68-72, C79, C82-89, C91, C94-97, C107, C109, C114-115, C122-131 | Capacitor, Ceramic, 2.2 µF, 10V, X5R, 0402 | TDK Corporation | C1005X5R1A225K050BC |
| 3 | D1, D5, D18 | LED, Thin, 635NM, Red, DIFF | Lumex® Inc. | SML-LXT0805IW-TR |
| 2 | D13, D14 | Diode, Schottky, 100V, 1A | Diodes Incorporated® | B1100-13F |
| 3 | D2, D6, D7 | LED, Thin, 565NM, Green, DIFF | Lumex Inc. | SML-LXT0805GW-TR |
| 2 | D3, D4 | LED, Thin, 585NM, Yellow, DIFF | Lumex Inc. | SML-LXT0805YW-TR |
| 4 | D8, D10, D11, D17 | Diode, Schottky, Dual, 30V | Diodes Incorporated | BAT54DW-7 |
| 1 | D9 | Diode, Switch, SS, Dual, 70V | Fairchild Semiconductor® | BAV99WT1G |
| 5 | J1, J2, J3, J4, J13 | SMA, Jack End Launch PCB | Johnson | 142-0711-821 |

Note 1: The components listed in this Bill of Materials are representative of the PCB assembly. The released BOM used in manufacturing uses all RoHS-compliant components.

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TABLE B-1: HV7358DB1 BILL OF MATERIALS (BOM)⁽¹⁾ (CONTINUED)

| Qty. | Reference | Description | Manufacturer | Part Number |
|------|---|---|----------------------------|-------------------------|
| 1 | J10 | Connector, Header, Vertical, .100, 6POS | TE Connectivity, Ltd. | 3-641213-6 |
| 2 | J5, J12 | Connector, Header, 40POS, R/A, HM-ZD | TE Connectivity, Ltd. | 6469169-1 |
| 25 | J6-9, J11, J19-35, J37, J39, J41 | Connector, Header, Vertical, .100, 2POS, | Molex® | 22-28-4023 |
| 7 | J6, 11, 15, 19-22 | Shunt, Econ, PHBR, 5AU, Black | TE Connectivity, Ltd. | 382811-8 |
| 4 | MH1-4 | Screw Machine Phillips, 4-40X1/4 | B&F | PMS 440 0025 PH |
| 4 | MH1, MH2, MH3, MH4 | Standoff, HEX, 4-40 THR, .250"L | Keystone Electronics Corp. | 1891 |
| 3 | R12, R35, R36 | Resistor, SMD, 0.0Ω, Jumper | Panasonic - ECG | ERJ-3GEY0R00V |
| 16 | R13-14,16,19,22,45,47-48,50,53,55,57,60,62-64 | Resistor, 2.55 kΩ, 1W, 1%, 2512 | Panasonic - ECG | ERJ-1TNF2551U |
| 2 | R24, R29 | Resistor, 499Ω, 1/10W, 1%, 0603 | Panasonic - ECG | ERJ-3EKF4990V |
| 1 | R27 | Resistor, 249Ω, 1/10W, 1%, 0603 | Panasonic - ECG | ERJ-3EKF2490V |
| 3 | R28, R18, R21 | Resistor, 1.00 kΩ, 1/16W, 1%, 0603 | Panasonic - ECG | ERJ-3EKF1001V |
| 6 | R3, R17, R23, R51, R54, R58 | Resistor, 49.9Ω, 1/16W, 1%, 0603 | Panasonic - ECG | ERJ-3EKF49R9V |
| 13 | R30, R69-77, R80-81, R83 | Resistor, 1.27 kΩ, ±1%, 1/10W, 0603 | Panasonic - ECG | ERJ-3EKF1271V |
| 7 | R34, R65, R66, R67, R68, R79, R82 | Resistor, 100Ω, 1/10W, 1%, 0402 | Panasonic - ECG | ERJ-2RKF1000X |
| 12 | R4, R15, R20, R25, R26, R33, R43, R44, R46, R49, R52, R56 | Not installed | NA | NA |
| 8 | R5, R6, R7, R8, R9, R10, R31, R32 | Resistor, 200Ω, 1/10W, 1%, 0603 | Panasonic - ECG | ERJ-3GEYJ201V |
| 1 | R78 | Resistor, SMD, 22.1Ω, 1%, 1/10W, 0402 | Panasonic - ECG | ERJ-2RKF22R1X |
| 6 | TP50, 65, 74, 75, 78, 84 | Connector, PC, Pin, Circular, 0.030 Diameter | Mill-Max Mfg. Corporation | 3132-0-00-15-00-00-08-0 |
| 1 | U3 | IC, Reg, LDO, 2.5V, 1.5A, 8-Lead SOIC | Microchip Technology Inc. | MCP1727-2502E/SN |
| 1 | U4 | IC, Op Amp, VFB, 510 MHz, 8-Lead SOIC | ADI | AD8099ARDZ |
| 1 | U5 | 16-Channel, ±80V, 1.8A, Ultrasound Beamformer | Microchip Technology Inc. | HV7358TFBGA |
| 1 | U6 | IC, Flash, 128 Mbit, 108 MHz, 8-Lead SOIC | Micron Technology Inc. | N25Q128A13ESE40F |
| 1 | U7 | IC, 2.5V, 2:1, LVDS, Mux in 3x3, 16-Lead QFN | Microchip Technology Inc. | SY58611UMG |

Note 1: The components listed in this Bill of Materials are representative of the PCB assembly. The released BOM used in manufacturing uses all RoHS-compliant components.

Bill of Materials (BOM)

TABLE B-2: MUPB002 BILL OF MATERIALS (BOM)⁽¹⁾

| Qty. | Reference | Description | Manufacturer | Part Number |
|------|---|---|--|---------------------|
| 8 | C1, C10, C11, C12, C27, C28, C90, C131 | Capacitor, Tantalum, 33 μ F, 10V, 10%, 1.4 Ohm, SMD, B | KEMET | T494B336K010AT |
| 2 | C129, C130 | Capacitor, Ceramic, 18 pF, 50V, 5%, C0G, SMD, 0402 | Murata Electronics | GRM1555C1H180JA01D |
| 14 | C2, C41, C46, C52, C54, C56, C58, C60, C62, C64, C66, C89, C132, C137 | Capacitor, Ceramic, 0.1 μ F, 50V, 20%, X7R, SMD, 0603 | TDK Corporation | C1608X7R1H104M |
| 1 | C3 | Capacitor, Tantalum, 100 μ F, 6.3V, 10%, 0.4 Ohm, SMD, B | AVX Corporation | TPSB107K006R0400 |
| 6 | C4, C13, C17, C21, C30, C33 | Capacitor, Ceramic, 0.047 μ F, 16V, 10%, X7R, SMD, 0402 | Taiyo Yuden Co., Ltd. | EMK105B7473KV-F |
| 2 | C42, C43 | Capacitor, Ceramic, 4.7 μ F, 16V, 10%, X7R, SMD, 1206 | KEMET | C1206C475K4RACTU |
| 0 | C44, C45 | Capacitor, Ceramic, 4.7 μ F, 16V, 10%, X7R, SMD, 1206, NOT POPULATED | KEMET | C1206C475K4RACTU |
| 13 | C47, C73, C74, C75, C76, C77, C78, C87, C88, C91, C100, C101, C102 | Capacitor, Ceramic, 10000 pF, 25V, 20%, X7R, SMD, 0402 | TDK Corporation | C1005X7R1E103M |
| 0 | C48 | Capacitor, Ceramic, 0.1 μ F, 50V, 10%, X7R, SMD, 0402, NOT POPULATED | TDK Corporation | C1005X7R1H104K050BB |
| 0 | C49 | Capacitor, Ceramic, 4.7 μ F, 6.3V, 20%, X5R, SMD, 0402, NOT POPULATED | Murata Electronics | GRM155R60J475ME47D |
| 36 | C5, C6, C7, C8, C9, C14, C15, C16, C18, C19, C20, C22, C23, C24, C25, C26, C29, C31, C32, C34, C35, C36, C37, C38, C39, C40, C117, C118, C119, C120, C123, C124, C125, C126, C127, C128 | Capacitor, Ceramic, 1000 pF, 25V, 5%, C0G, SMD, 0201 | Digi-Key [®] Electronics | 587-5297-1-ND |
| 3 | C50, C105, C115 | Capacitor, Ceramic, 4.7 μ F, 6.3V, 20%, X5R, SMD, 0402 | Murata Electronics | GRM155R60J475ME47D |
| 8 | C51, C53, C55, C57, C59, C61, C63, C65 | Capacitor, Ceramic, 10 μ F, 10V, 10%, X7R, SMD, 0805 | Samsung Electro-Mechanics America, Inc | CL21B106KPQNFNE |
| 24 | C67, C68, C79, C80, C81, C82, C84, C92, C93, C94, C95, C103, C104, C106, C111, C112, C113, C114, C116, C133, C134, C135, C136, C138 | Capacitor, Ceramic, 0.1 μ F, 50V, 10%, X7R, SMD, 0402 | TDK Corporation | C1005X7R1H104K050BB |
| 2 | C69, C70 | Capacitor, Ceramic, 4.7 μ F, 16V, 10%, X5R, SMD, 0603 | TDK Corporation | C1608X5R1C475K080AC |

Note 1: The components listed in this Bill of Materials are representative of the PCB assembly. The released BOM used in manufacturing uses all RoHS-compliant components.

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TABLE B-2: MUPB002 BILL OF MATERIALS (BOM)⁽¹⁾ (CONTINUED)

| Qty. | Reference | Description | Manufacturer | Part Number |
|------|-------------------------|--|--|--------------------|
| 2 | C71, C107 | Capacitor, Ceramic, 10000 pF, 50V, 10%, X7R, SMD, 0603 | AVX Corporation | 06035C103KAT2A |
| 1 | C72 | Capacitor, Ceramic, 4700 pF, 50V, 10%, X7R, SMD, 0603 | KEMET | C0603C472K5RACTU |
| 2 | D1, D2 | Diode, Schottky, MBR0540T1G, 510 mV, 500 mA, 40V, SMD, SOD-123 | ON [®] Semiconductor | MBR0540T1G |
| 5 | D3, D4, D5, D6, D7 | Diode, Schottky, BAT54XV2T1G, 30V, 200 mA, 40V, SOD-523 | ON Semiconductor | BAT54XV2T1G |
| 2 | J1, J2 | Connector, Edge, HMZd, 2.5 mm, 40P, Female, TH, R/A | Tyco Electronics (TE Connectivity Ltd.) | 1469028-1 |
| 2 | J3, J7 | Connector, USB 2.0, Micro-B, Female, SMD, R/A | FCI | 10118192-0001LF |
| 1 | J4 | Connector, Header, 2 mm, Male, 2x7, Milli-Grid, Gold, Shroud, SMD, Vertical | Molex, LLC | 878321420 |
| 0 | J5 | Connector, Header-2.54, Male, 2x4, Gold, 5.84 MH, SMT, Vertical, NOT POPULATED | Sullins Connector Solutions | GBC04DABN-M30 |
| 4 | J6, J14, J15, J16 | Connector, Header-2.54, Male, 1x3, Tin, 6.75 MH, TH, Vertical | Molex | 90120-0123 |
| 0 | J8, J9 | Connector, RF, Coaxial, SMA, Female, 2P, TH, Vertical, NOT POPULATED | TE Connectivity Ltd. | 5-1814832-1 |
| 1 | JP1 | Connector, Header-2.54, Male, 1x4, Tin, 5.84 MH, TH, Vertical | FCI | 68002-404HLF |
| 1 | JP2 | Connector, Header-2.54 Male, 1x2, Gold, 5.84 MH, TH, Vertical | FCI | 77311-118-02LF |
| 4 | LD1, LD2, LD3, LD4 | Diode, LED, Green, 2.2V, 25 mA, 15 mcd, Clear, SMD, 0603 | Kingbright Electronic Co., Ltd. | APT1608SGC |
| 1 | Q1 | Transformer, FET, N-CH, BSS123, 100V, 170 mA, 300 mW, 3-Lead SOT-23 | Diodes Incorporated | BSS123-7-F |
| 5 | R1, R2, R4, R60, R84 | Resistor, TKF, 4.7k, 1%, 1/10W, 0402 | KOA Speer Electronic, Inc. | RK73H1ETTP4701F |
| 0 | R10, R15 | Resistor, TKF, 22R, 1%, 1/20W, SMD, 0402, NOT POPULATED | Panasonic Electronic Components | ERJ-2RKF22R0X |
| 5 | R11, R14, R61, R63, R64 | Resistor, TKF, 22R, 1%, 1/20W, SMD, 0402 | Panasonic Electronic Components | ERJ-2RKF22R0X |
| 5 | R16, R18, R92, R93, R95 | Resistor, TKF, 1k, 1%, 1/10W, SMD, 0402 | Panasonic - ECG | ERJ-2RKF1001X |
| 1 | R17 | Resistor, TKF, 19.1k, 1%, 1/10W, SMD, 0603 | Panasonic - ECG | ERJ-3EKF1912V |
| 5 | R20, R37, R39, R67, R68 | Resistor, TKF, 100R, 1%, 1/16W, SMD, 0402 | Yageo Corporation | RC0402FR-07100RL |
| 3 | R22, R28, R29 | Resistor, TF, 10k, 1%, 1/8W, SMD, 0603 | Vishay Beyschlag | MCT06030C1002FP500 |

Note 1: The components listed in this Bill of Materials are representative of the PCB assembly. The released BOM used in manufacturing uses all RoHS-compliant components.

Bill of Materials (BOM)

TABLE B-2: MUPB002 BILL OF MATERIALS (BOM)⁽¹⁾ (CONTINUED)

| Qty. | Reference | Description | Manufacturer | Part Number |
|------|---|--|---------------------------------|--------------------|
| 9 | R23, R24, R30, R33, R65, R66, R72, R73, R74 | Resistor, TKF, 10k, 1%, 1/10W, SMD, 0402 | Panasonic - ECG | ERJ-2RKF1002X |
| 1 | R25 | Resistor, TKF, 51k, 1%, 1/10W, SMD, 0603 | Panasonic - ECG | ERJ-3EKF5102V |
| 1 | R26 | Resistor, TKF, 69.8k, 1%, 1/10W, SMD, 0603 | Panasonic - ECG | ERJ-3EKF6982V |
| 1 | R27 | Resistor, TKF, 390R, 5%, 1/10W, SMD, 0603 | Panasonic - ECG | ERJ-3GEYJ391V |
| 5 | R3, R19, R21, R36, R50 | Resistor, TKF, 100k, 1%, 1/10W, SMD, 0402 | Panasonic - ECG | ERJ-2RKF1003X |
| 1 | R31 | Resistor, TKF, 82k, 1%, 1/10W, SMD, 0603 | Panasonic Electronic Components | ERJ-3EKF8202V |
| 1 | R32 | Resistor, TKF, 10.7k, 1%, 1/10W, SMD, 0603 | Panasonic - ECG | ERJ-3EKF1072V |
| 0 | R34, R35, R40, R41 | Resistor, TKF, 0R, 1/16W, SMD, 0402, NOT POPULATED | Yageo Corporation | RC0402JR-070RL |
| 0 | R38 | Resistor, TKF, 3.3M, 1%, 1/16W, SMD, 0402, NOT POPULATED | Yageo Corporation | RC0402FR-073M3L |
| 0 | R5, R7, R51, R75 | Resistor, TKF, 4.7k, 1%, 1/10W, 0402, NOT POPULATED | KOA Speer Electronic, Inc. | RK73H1ETTP4701F |
| 1 | R43 | Resistor, TKF, 100k, 1%, 1/10W, SMD, 0603 | Panasonic - ECG | ERJ-3EKF1003V |
| 1 | R44 | Resistor, TKF, 78.7k, 1%, 1/10W, SMD, 0603 | Panasonic Electronic Components | ERJ-3EKF7872V |
| 1 | R54 | Resistor, TKF, 12k, 1%, 1/16W, SMD, 0402 | ROHM Semiconductor | MCR01MZPF1202 |
| 0 | R57, R58, R69, R70, R71 | Resistor, TKF, 10k, 1%, 1/10W, SMD, 0402, NOT POPULATED | Panasonic - ECG | ERJ-2RKF1002X |
| 6 | R6, R8, R9, R12, R42, R45 | Resistor, MF, 330R, 5%, 1/16W, SMD, 0603 | Panasonic Electronic Components | ERA-V33J331V |
| 1 | R62 | Resistor, TKF, 2.43k, 1%, 1/16W, SMD, 0402 | Yageo Corporation | RC0402FR-072K43L |
| 0 | R76, R77, R78, R79, R80, R81, R82, R83 | NOT POPULATED | Panasonic - ECG | ERJ-3GSY0R00V |
| 2 | SW1, SW2 | Switch, TACT, SPST, 24V, 50 mA, FSM2JMTR, SMD | TE Connectivity Alcoswitch | FSM2JMTR |
| 0 | TP1, TP6, TP7, TP8, TP9, TP12, TP21, TP22, TP23, TP24, TP30, TP31 | Connector, TP, Loop, Silver, 3.4x5, SMD, NOT POPULATED | Component Corporation | TP-107-2 |
| 0 | TP26, TP27, TP28, TP29 | NOT POPULATED | | |
| 1 | U1 | IC, FPGA, XC6SLX25-2FTG256C, 186 I/O, 1.2V, BGA-256 | Xilinx Inc. | XC6SLX25-2FTG256C |
| 1 | U10 | Microchip Clock Generation, Quad, 156.25 MHz, SM803004UMY, 48-Lead QFN | Microchip Technology Inc. | SM803004UMY |

Note 1: The components listed in this Bill of Materials are representative of the PCB assembly. The released BOM used in manufacturing uses all RoHS-compliant components.

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TABLE B-2: MUPB002 BILL OF MATERIALS (BOM)⁽¹⁾ (CONTINUED)

| Qty. | Reference | Description | Manufacturer | Part Number |
|------|----------------|--|-----------------------------------|-----------------------------|
| 0 | U11 | Microchip Clock Oscillator, Single, 24 MHz, DSC6003CI2A-024.0000, SMD, 4-Lead DFN, NOT POPULATED | Microchip Technology Inc. | DSC6003CI2A-024.0000 |
| 0 | U14 | Microchip Memory Serial Flash, 16M, 104 MHz, SST26VF016B-104I/SM, 8-Lead SOIJ, NOT POPULATED | Microchip Technology Inc. | SST26VF016B-104I/SM |
| 1 | U15 | Flash – NOR Memory IC, 128 Mb (16Mx8), SPI – Quad, I/O, 108 MHz, 8-Lead SOIC | Cypress Semiconductor Corporation | S25FL127SABMFV101 |
| 3 | U2, U9, U13 | IC, Bus, BUFF, TRI-ST, N-INV, Single, SN74LVC1G126, SOT-553 | Texas Instruments | SN74LVC1G126DRLR |
| 1 | U3 | Microchip Interface, USB, Hub/Flash, USB4604-1080HN, 48-Lead SQFN | Microchip Technology Inc. | USB4604-1080HN |
| 4 | U4, U5, U6, U7 | Microchip Analog, LDO, 0.8V-5V, MCP1727T-ADJE/MF, 8-Lead DFN | Microchip Technology Inc. | MCP1727T-ADJE/MF |
| 1 | U8 | Microchip Analog, LDO, ADJ, MIC94325YMT-TR, 6-Lead TDFN | Microchip Technology Inc. | MIC94325YMT-TR |
| 1 | X1 | Crystal, 24 MHz, 18 pF, SMD, ABM8G | Abracon Corporation (LLC) | ABM8G-24.000MHZ-18-D2 Y-T |
| 1 | X2 | Crystal, 40 MHz, 12 pF, SMD, L5W3.2H0.9 | TXC Corporation | 7B-40.000MAAE-T |
| 2 | C96, C97 | Resistor, TKF, 0, 1%, 1/10W, SMD, 0402 | Panasonic Electronic Components | ERJ-2GE0R00X |

Note 1: The components listed in this Bill of Materials are representative of the PCB assembly. The released BOM used in manufacturing uses all RoHS-compliant components.

Appendix C. HV7358DB1 Waveforms

C.1 MIC2800 EVALUATION BOARD TEST WAVEFORM EXAMPLES

Appendix C shows sample waveforms created with the MUPB002 and HV7358DB1 combination.

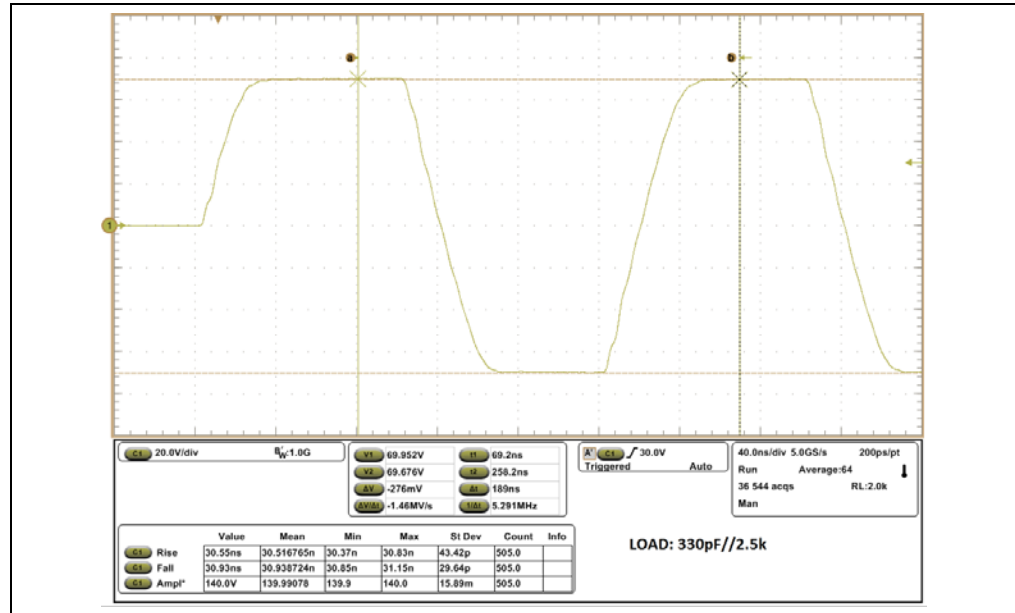


FIGURE C-1: 5 MHz $V_{PP}/V_{NF} = \pm 80V$ Load: 330 pF//2.5K.

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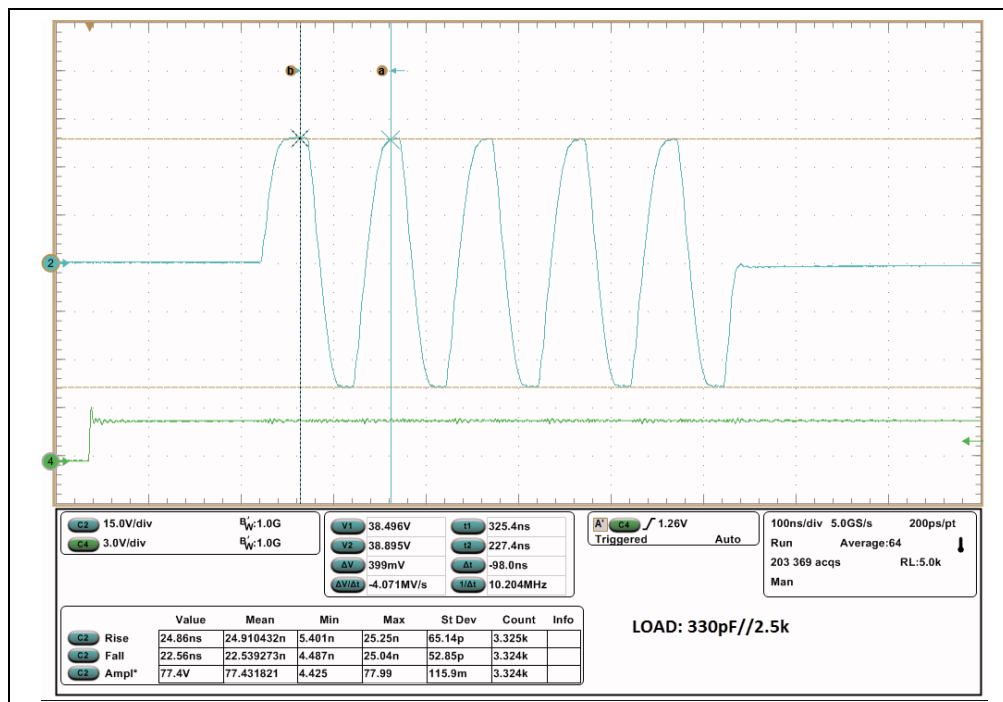


FIGURE C-2: 10 MHz $V_{PP}/V_{NN} = \pm 70V$ Load: 330 pF//2.5K.

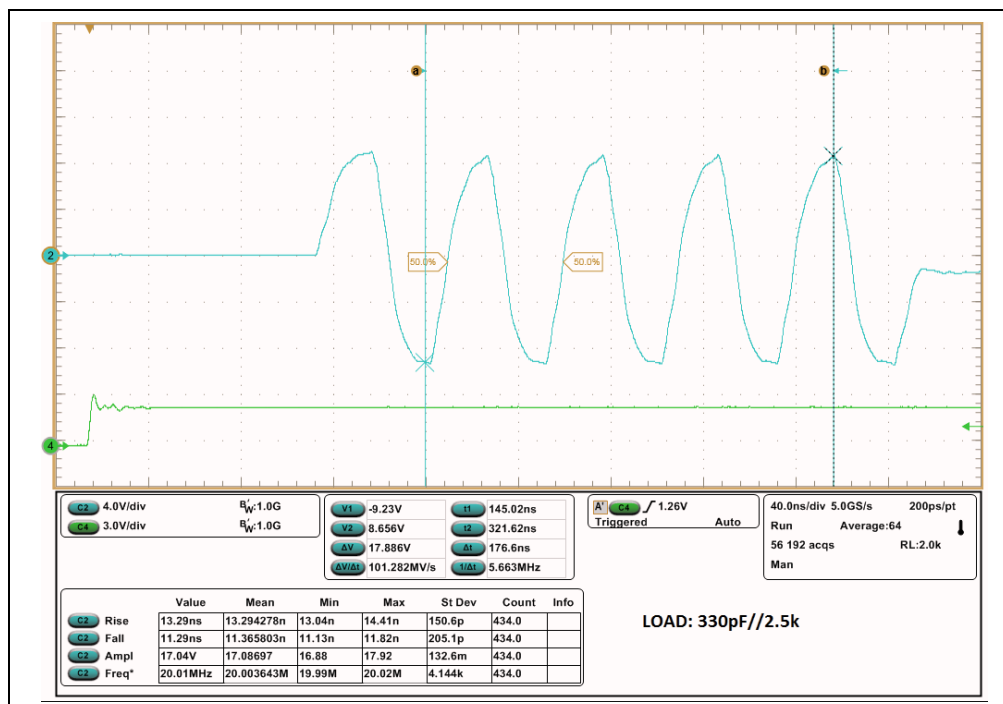


FIGURE C-3: TX Output 20 MHz 4-Cycle 17.8 $V_{(p-p)}$ 330 pF//2.5K Load.

HV7358DB1 Waveforms

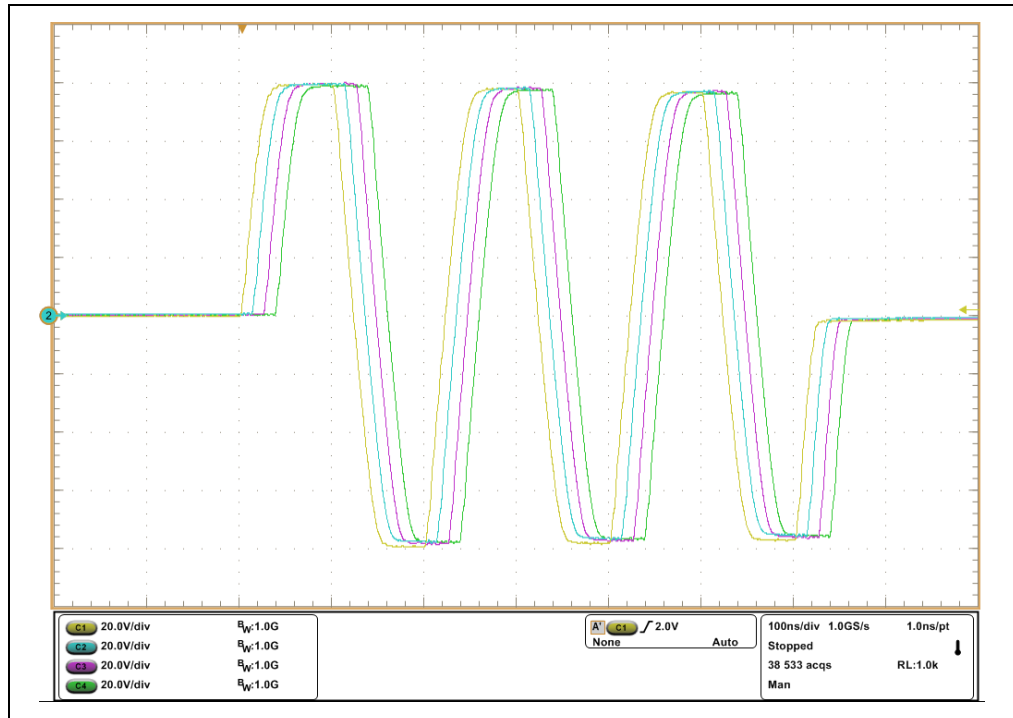


FIGURE C-4: Ch8-11 $V_{PP}/V_{NN} = \pm 80V$, 5 MHz with 330 pF/2.5K, All Channels On.

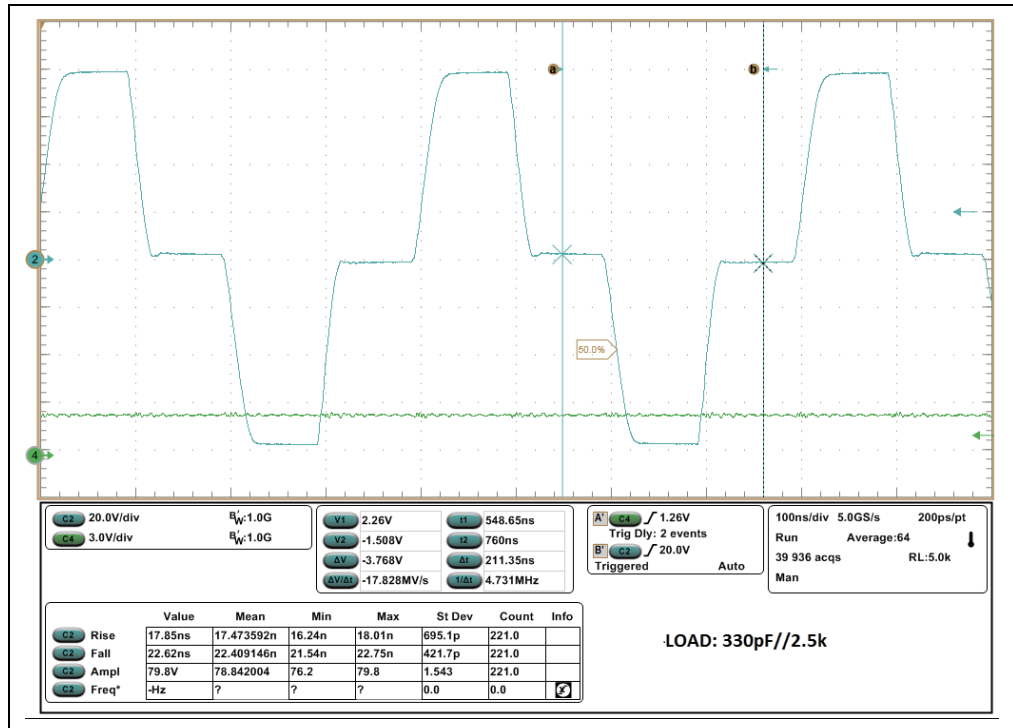


FIGURE C-5: Rise Fall Time of $\pm 80V$, 5 MHz RTZ, 330 pF/2.5K Load.

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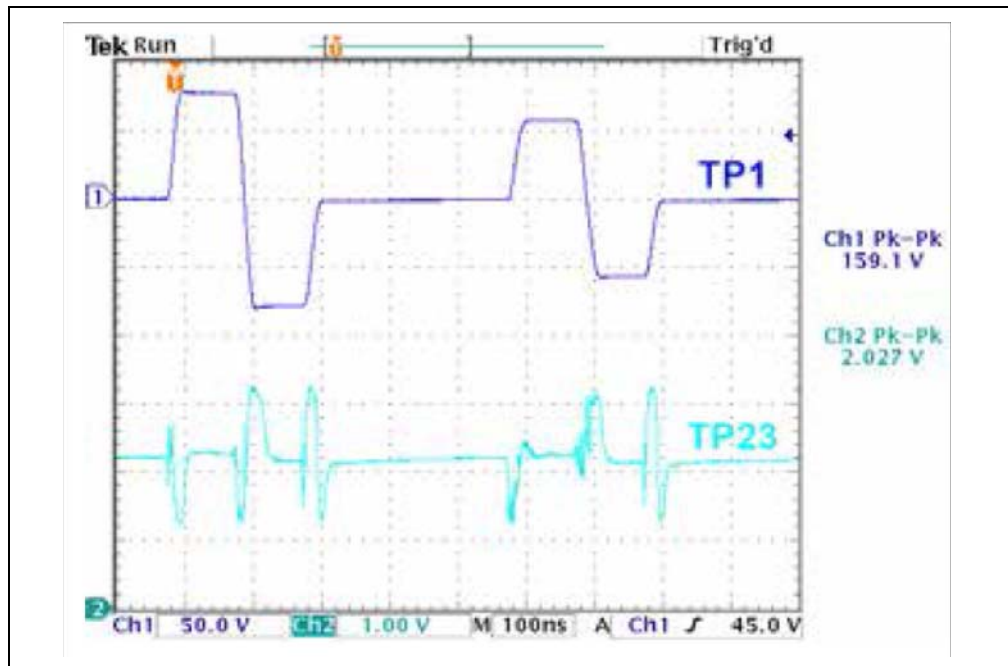


FIGURE C-6: TX and RX B Mode, 5 MHz, 1-Cycle with 330 pF/2.5k Load.

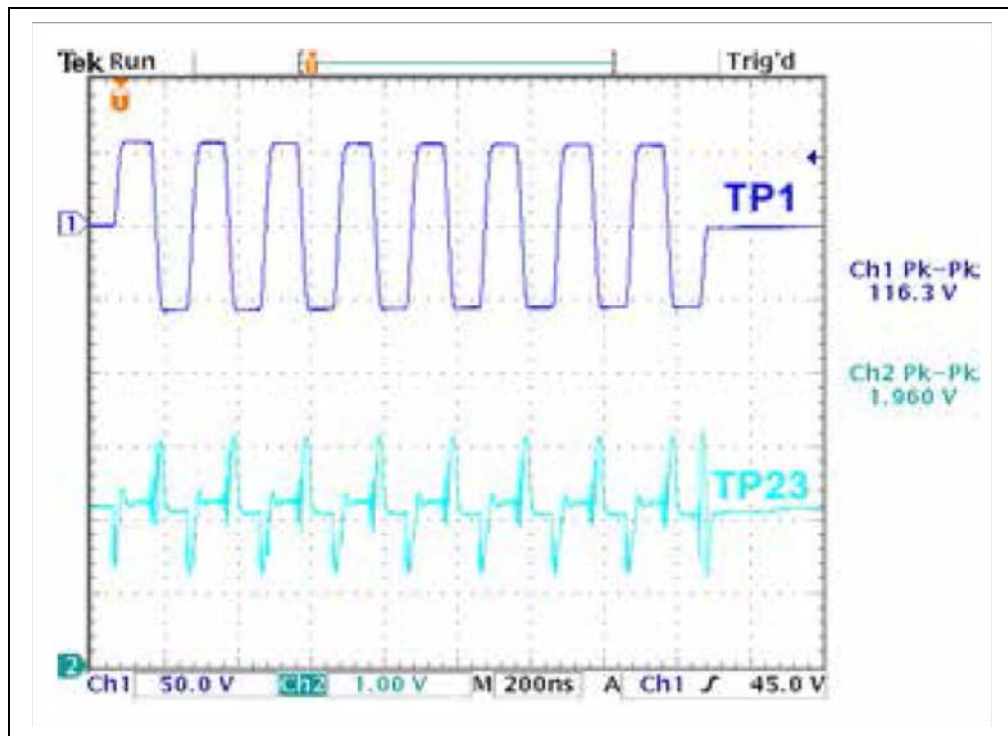


FIGURE C-7: TX and RX in P_w Mode, 5 MHz, 8-Cycle, 330 pF/2.5K Load.

HV7358DB1 Waveforms

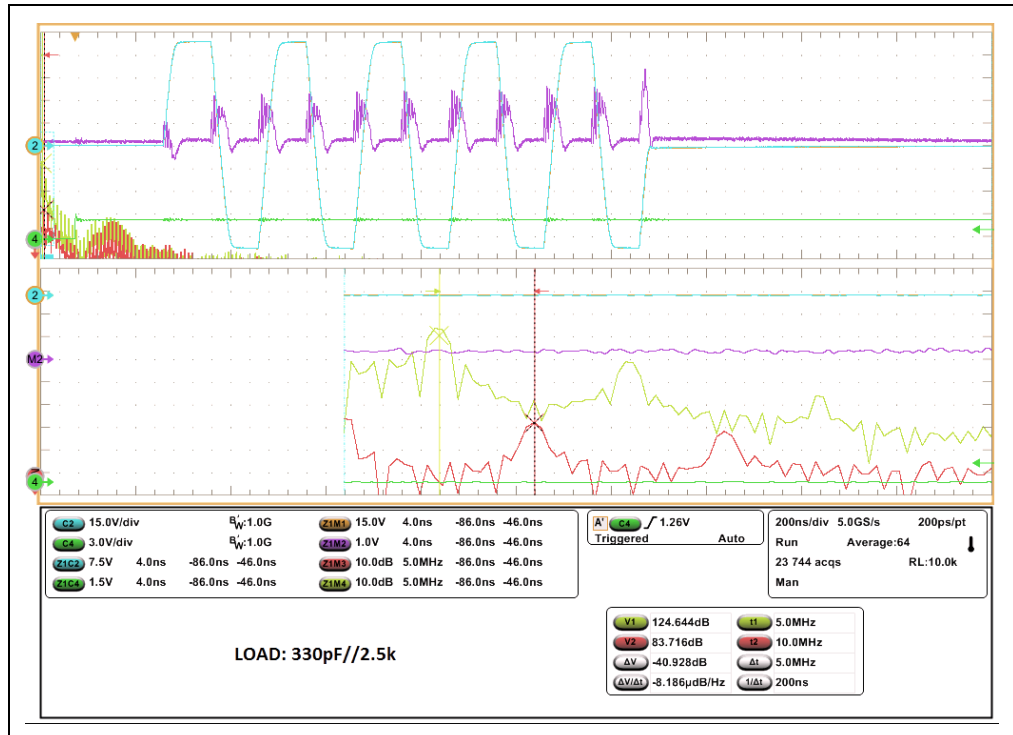


FIGURE C-8: 4-Cycle Canceling, 5 MHz, 4-Cycle Canceling, 5 MHz.

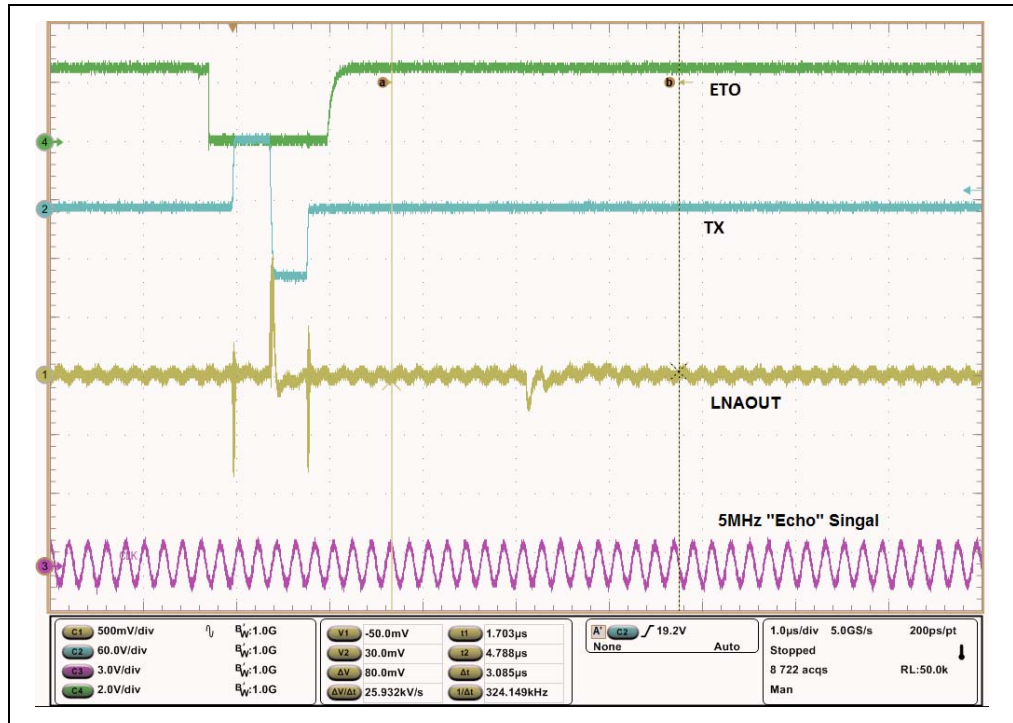


FIGURE C-9: LNAOut RX0 Signal After TX, 1-Cycle, $\pm 80V$.

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NOTES:

Appendix D. HV7358 GUI Parameter and Default

D.1 HV7358 GUI PARAMETER LIMITS AND DEFAULT PAGE-1

| HV7358DB1 GUI Parameter Limits and Initial Default Values | | | | | | |
|---|-----------------------------------|---------|---------|--------------|---------|--|
| GUI SYM | Parameter | Unit | Min | Ini. Default | Max | Note-1 |
| H/W System Variables | | | | | | |
| VLL | Logic voltage at VLL pin | V | 2.375 | 2.5 | 3.625 | fixed by H/W |
| VDD | Digital voltage at VDD & AVDD pin | V | 4.75 | 5 | 5.25 | fixed by H/W |
| VGN | LV bias voltage at VGN pin | V | -5.25 | -5 | -4.75 | fixed by H/W |
| VPF | Pos gate-drive voltage at CPF pin | V | 4.5 | 5.1 | 5.2 | fixed by H/W |
| VNF | Neg gate-drive voltage at CNF pin | V | -5.2 | -5.2 | -4.5 | fixed by H/W |
| User Entered Variables | | | | | | |
| VPP | HV Positive in CW-Mode | V | 0 | 5 | 7 | User must enter a measured value |
| | HV Positive in B-Mode | | 8 | 70 | 81 | User must enter a measured value |
| VNN | HV Negative in CW-Mode | V | -7 | -5 | 0 | User must enter a measured value |
| | HV Negative in B-Mode | | -81 | -70 | -8 | User must enter a measured value |
| Calculated Variables | | | | | | |
| B-Mode | B-Mode Display | Binary | 0 | NOT(CW) | 1 | Opposite to CW bit (pin) |
| fTCK | Tx Clock Pin Freq. PEN=1 | MHz | 30 | 40 | 80 | GUI Select: 30, 40, 65, 80MHz if PEN=1. From SM803004 |
| | Tx Clock Pin Freq. PEN=0 | | 30 | 80 | 200 | GUI Select: 80, 120, 160, 200MHz if PEN=0. From SM803004 |
| fc | IC Internal Clock Freq. | MHz | 160 | Calculated | 240 | fc=fTCK if PEN=0, fc=N*fTCK if PEN=LCKD=1. See MathCAD Limitation Calculation. |
| fVCO | PLL VCO freq. | MHz | 160 | Calculated | 240 | No Display |
| fRF | Ultrasound Frequency in B-mode | MHz | 1 | Calculated | 20 | Display on GUI When CW=0 |
| | Ultrasound Frequency in CW-mode | | 1 | Calculated | 20 | Display on GUI When CW=1 |
| LDR | Line Duration | fC Cyc. | 5.0E+04 | Calculated | 1.6E+05 | Note: Limited by D%, See MathCAD Limitation Calculation |
| D% Max | Tx B-mode pulses burst-duty-cycle | % | 0 | 20 | 100 | CW=1 See MathCAD Limitation Calculation |
| | Tx CW-duty-cycle | | 0 | 5 | 8 | CW=0 See MathCAD Limitation Calculation |
| t(TXRW) | TX or R/W mode control signal | us | 50 | Calculated | 500 | GUI calculated commend to FPGA. See MathCAD Limitation Calculation |
| Auto Stop | Tx auto stop time | sec | NA | 60 | 300 | Demo Tx waveform auto off feature for safety |
| SPI, Read back from I2C | | | | | | |
| TGP(0) | Globe-off-time P | fC Cyc. | 0 | 0 | 127 | 7-bit (as example of selcted in this table) |
| TGN(0) | Globe-off-time N | fC Cyc. | 0 | 0 | 127 | 7-bit (as example of selcted in this table) |
| TGW(0) | Globe Pulse Width | fC Cyc. | 2 | 16 | 511 | 9-bit (as example of selcted in this table) |
| RPC(0) | Rep. Pulses # | fC Cyc. | 0 | 3 | 32 | 8-bit (as example of selcted in this table) |
| TGP(1) | Globe-off-time P | fC Cyc. | 0 | 0 | 127 | 7-bit |
| TGN(1) | Globe-off-time N | fC Cyc. | 0 | 0 | 127 | 7-bit |
| TGW(1) | Globe Pulse Width | fC Cyc. | 2 | 16 | 511 | 9-bit |
| RPC(1) | Rep. Pulses # | fC Cyc. | 0 | 2 | 32 | 8-bit |
| TGP(2) | Globe-off-time P | fC Cyc. | 0 | 0 | 127 | 7-bit |
| TGN(2) | Globe-off-time N | fC Cyc. | 0 | 0 | 127 | 7-bit |
| TGW(2) | Globe Pulse Width | fC Cyc. | 2 | 4 | 511 | 9-bit |
| RPC(2) | Rep. Pulses # | fC Cyc. | 0 | 5 | 32 | 8-bit |
| TGP(3) | Globe-off-time P | fC Cyc. | 0 | 0 | 127 | 7-bit |
| TGN(3) | Globe-off-time N | fC Cyc. | 0 | 0 | 127 | 7-bit |
| TGW(3) | Globe Pulse Width | fC Cyc. | 2 | 10 | 511 | 9-bit |
| RPC(3) | Rep. Pulses # | fC Cyc. | 0 | 3 | 32 | 8-bit |
| DLY(0) | Beamform dely Ch-0 | fC Cyc. | 0 | 10 | 4095 | 12-bit |
| DLY(1) | Beamform dely Ch-1 | fC Cyc. | 0 | 15 | 4095 | 12-bit |
| DLY(2) | Beamform dely Ch-2 | fC Cyc. | 0 | 20 | 4095 | 12-bit |
| DLY(3) | Beamform dely Ch-3 | fC Cyc. | 0 | 25 | 4095 | 12-bit |
| DLY(4) | Beamform dely Ch-4 | fC Cyc. | 0 | 30 | 4095 | 12-bit |
| DLY(5) | Beamform dely Ch-5 | fC Cyc. | 0 | 35 | 4095 | 12-bit |
| DLY(6) | Beamform dely Ch-6 | fC Cyc. | 0 | 40 | 4095 | 12-bit |
| DLY(7) | Beamform dely Ch-7 | fC Cyc. | 0 | 45 | 4095 | 12-bit |
| DLY(8) | Beamform dely Ch-8 | fC Cyc. | 0 | 50 | 4095 | 12-bit |
| DLY(9) | Beamform dely Ch-9 | fC Cyc. | 0 | 55 | 4095 | 12-bit |
| DLY(10) | Beamform dely Ch-10 | fC Cyc. | 0 | 60 | 4095 | 12-bit |
| DLY(11) | Beamform dely Ch-11 | fC Cyc. | 0 | 65 | 4095 | 12-bit |
| DLY(12) | Beamform dely Ch-12 | fC Cyc. | 0 | 70 | 4095 | 12-bit |
| DLY(13) | Beamform dely Ch-13 | fC Cyc. | 0 | 75 | 4095 | 12-bit |
| DLY(14) | Beamform dely Ch-14 | fC Cyc. | 0 | 80 | 4095 | 12-bit |
| DLY(15) | Beamform dely Ch-15 | fC Cyc. | 0 | 85 | 4095 | 12-bit |
| TLP(0) | Local PWM P-OFF-Time Ch-0 | fC Cyc. | 0 | 2 | 127 | 7-bit |
| TLP(1) | Local PWM P-OFF-Time Ch-1 | fC Cyc. | 0 | 2 | 127 | 7-bit |

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D.2 HV7358DB1 GUI PARAMETER INITIAL VALUE AND LIMITS PAGE-2

HV7358DB1 GUI Parameter Limits and Initial Default Values

| GUI SYM | Parameter | Unit | Min | Ini. Default | Max | Note-1 |
|--------------------------------|-----------------------------------|---------|---------|--------------|---------|--|
| H/W System Variables | | | | | | |
| VLL | Logic voltage at VLL pin | V | 2.375 | 2.5 | 3.625 | fixed by H/W |
| VDD | Digital voltage at VDD & AVDD pin | V | 4.75 | 5 | 5.25 | fixed by H/W |
| VGN | LV bias voltage at VGN pin | V | -5.25 | -5 | -4.75 | fixed by H/W |
| VPF | Pos gate-drive voltage at CPF pin | V | 4.5 | 5.1 | 5.2 | fixed by H/W |
| VNF | Neg gate-drive voltage at CNF pin | V | -5.2 | -5.2 | -4.5 | fixed by H/W |
| User Entered Variables | | | | | | |
| VPP | HV Positive in CW-Mode | V | 0 | 5 | 7 | User must enter a measured value |
| | HV Positive in B-Mode | | 8 | 70 | 81 | User must enter a measured value |
| VNN | HV Negative in CW-Mode | V | -7 | -5 | 0 | User must enter a measured value |
| | HV Negative in B-Mode | | -81 | -70 | -8 | User must enter a measured value |
| Calculated Variables | | | | | | |
| B-Mode | B-Mode Display | Binary | 0 | NOT(CW) | 1 | Opposite to CW bit (pin) |
| fTCK | Tx Clock Pin Freq. PEN=1 | MHz | 30 | 40 | 80 | GUI Select: 30, 40, 65, 80MHz if PEN=1. From SM803004 |
| | Tx Clock Pin Freq. PEN=0 | | 30 | 80 | 200 | GUI Select: 80, 120, 160, 200MHz if PEN=0. From SM803004 |
| fC | IC Internal Clock Freq. | MHz | 160 | Calculated | 240 | fC=fTCK if PEN=0, fC=N*fTCK if PEN=LCKD=1. See MathCAD Limitation Calculation. |
| fVCO | PLL VCO freq. | MHz | 160 | Calculated | 240 | No Display |
| fRF | Ultrasound Frequency in B-mode | MHz | 1 | Calculated | 20 | Display on GUI When CW=0 |
| | Ultrasound Frequency in CW-mode | | 1 | Calculated | 20 | Display on GUI When CW=1 |
| LDR | Line Duration | fC Cyc. | 5.0E+04 | Calculated | 1.6E+05 | Note: Limited by D%, See MathCAD Limitation Calculation |
| D% Max | Tx B-mode pulses burst-duty-cycle | % | 0 | 20 | 100 | CW=1 See MathCAD Limitation Calculation |
| | Tx CW-duty-cycle | | 0 | 5 | 8 | CW=0 See MathCAD Limitation Calculation |
| t(TXRW) | TX or R/W mode control signal | us | 50 | Calculated | 500 | GUI calculated comment to FPGA. See MathCAD Limitation Calculation |
| Auto Stop | Tx auto stop time | sec | NA | 60 | 300 | Demo Tx waveform auto off feature for safety |
| SPI, Read back from I2C | | | | | | |
| TGP(0) | Globe-off-time P | fC Cyc. | 0 | 0 | 127 | 7-bit (as example of selected in this table) |
| TGN(0) | Globe-off-time N | fC Cyc. | 0 | 0 | 127 | 7-bit (as example of selected in this table) |
| TGW(0) | Globe Pulse Width | fC Cyc. | 2 | 16 | 511 | 9-bit (as example of selected in this table) |
| RPC(0) | Rep. Pulses # | fC Cyc. | 0 | 3 | 32 | 8-bit (as example of selected in this table) |
| TGP(1) | Globe-off-time P | fC Cyc. | 0 | 0 | 127 | 7-bit |
| TGN(1) | Globe-off-time N | fC Cyc. | 0 | 0 | 127 | 7-bit |
| TGW(1) | Globe Pulse Width | fC Cyc. | 2 | 16 | 511 | 9-bit |
| RPC(1) | Rep. Pulses # | fC Cyc. | 0 | 2 | 32 | 8-bit |
| TGP(2) | Globe-off-time P | fC Cyc. | 0 | 0 | 127 | 7-bit |
| TGN(2) | Globe-off-time N | fC Cyc. | 0 | 0 | 127 | 7-bit |
| TGW(2) | Globe Pulse Width | fC Cyc. | 2 | 4 | 511 | 9-bit |
| RPC(2) | Rep. Pulses # | fC Cyc. | 0 | 5 | 32 | 8-bit |
| TGP(3) | Globe-off-time P | fC Cyc. | 0 | 0 | 127 | 7-bit |
| TGN(3) | Globe-off-time N | fC Cyc. | 0 | 0 | 127 | 7-bit |
| TGW(3) | Globe Pulse Width | fC Cyc. | 2 | 10 | 511 | 9-bit |
| RPC(3) | Rep. Pulses # | fC Cyc. | 0 | 3 | 32 | 8-bit |
| DLY(0) | Beamform dely Ch-0 | fC Cyc. | 0 | 10 | 4095 | 12-bit |
| DLY(1) | Beamform dely Ch-1 | fC Cyc. | 0 | 15 | 4095 | 12-bit |
| DLY(2) | Beamform dely Ch-2 | fC Cyc. | 0 | 20 | 4095 | 12-bit |
| DLY(3) | Beamform dely Ch-3 | fC Cyc. | 0 | 25 | 4095 | 12-bit |
| DLY(4) | Beamform dely Ch-4 | fC Cyc. | 0 | 30 | 4095 | 12-bit |
| DLY(5) | Beamform dely Ch-5 | fC Cyc. | 0 | 35 | 4095 | 12-bit |
| DLY(6) | Beamform dely Ch-6 | fC Cyc. | 0 | 40 | 4095 | 12-bit |
| DLY(7) | Beamform dely Ch-7 | fC Cyc. | 0 | 45 | 4095 | 12-bit |
| DLY(8) | Beamform dely Ch-8 | fC Cyc. | 0 | 50 | 4095 | 12-bit |
| DLY(9) | Beamform dely Ch-9 | fC Cyc. | 0 | 55 | 4095 | 12-bit |
| DLY(10) | Beamform dely Ch-10 | fC Cyc. | 0 | 60 | 4095 | 12-bit |
| DLY(11) | Beamform dely Ch-11 | fC Cyc. | 0 | 65 | 4095 | 12-bit |
| DLY(12) | Beamform dely Ch-12 | fC Cyc. | 0 | 70 | 4095 | 12-bit |
| DLY(13) | Beamform dely Ch-13 | fC Cyc. | 0 | 75 | 4095 | 12-bit |
| DLY(14) | Beamform dely Ch-14 | fC Cyc. | 0 | 80 | 4095 | 12-bit |
| DLY(15) | Beamform dely Ch-15 | fC Cyc. | 0 | 85 | 4095 | 12-bit |
| TLP(0) | Local PWM P-OFF-Time Ch-0 | fC Cyc. | 0 | 2 | 127 | 7-bit |
| TLP(1) | Local PWM P-OFF-Time Ch-1 | fC Cyc. | 0 | 2 | 127 | 7-bit |

HV7358 GUI Parameter and Default

D.3 HV7358DB1 GUI PARAMETER INITIAL VALUE AND LIMITS PAGE-3

| | | | | | | |
|-----------|------------------------------------|----------|------|------------|--------|--|
| LPWM | Local / Global PWM Off-Time Sel. | Binary | 0 | 0 | 1 | GUI selecting number |
| INV | Inverting Function Pin Control | Binary | 0 | 0 | 1 | GUI selecting number |
| LCKD | LCKD-Read Only Pin | Binary | 0 | 7 | 1 | Open-Drain Output |
| RSTN | Active Low, Reset pin | One-Shot | 0 | 1 | 1 | GUI Button One-Shot-Low |
| DISC | Active High, VPP/VNN Discharge pin | One-Shot | 0 | 1 | 1 | GUI Button One-Shot-High |
| TXRW | TX or R/W mode control pin | us | 50 | Calculated | 500 | Accordinging FPGA control see t(TXRW) calculated |
| LDR | Line Duration | fc Cyc. | 4000 | 16000 | 160000 | GUI user input |
| TXRW_HI | TXRW High Time | fc Cyc. | 2000 | 12000 | 20000 | GUI JSON initial Only |
| TXRW2TRIG | TXRW High to TRIG High | fc Cyc. | 6 | 8 | 12 | GUI JSON initial Only |
| TRIG_HI | TRIG HIGH time | fc Cyc. | 6 | 8 | 12 | GUI JSON initial Only |
| DCC | Duty Cycle Correction | fc Cyc. | 6 | 8 | 12 | GUI JSON initial Only |
| TBSPiW | Time Between SPI Writ | fc Cyc. | 10 | 50 | 55 | GUI JSON initial Only |
| ETIAT | ETI Assertion time | fc Cyc. | 0 | 0 | 5 | GUI JSON initial Only |
| RSTN_LO | RSTN Low time | fc Cyc. | 20 | 50 | 70 | GUI JSON initial Only |
| I2CSTUP | I2C Setup time | fc Cyc. | 10 | 20 | 40 | GUI JSON initial Only |
| I2C_HDUP | I2C Hold time | fc Cyc. | 10 | 20 | 40 | GUI JSON initial Only |



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