MAX2079

Low-Power, High-Performance, Fully Integrated Octal Ultrasound Receiver (Octal LNA, VGA, AAF, ADC, and CWD Beamformer)

General Description

The MAX2079 fully integrated octal ultrasound receiver is optimized for high channel count, high-performance portable and cart-based ultrasound systems. The easy-to-use integrated receiver allows the user to achieve high-end 2D and Doppler imaging capability using substantially less space and power. The highly compact low-noise amplifier (LNA), variable-gain amplifier (VGA), anti-alias filter (AAF), analog-to-digital converter (ADC), and digital highpass filter (HPF) achieve an ultra-low 2.8dB noise figure at $R_S = R_{IN} = 200\Omega$ with a very low 120mW per channel power dissipation at 50Msps. The full receive channel has been optimized for second-harmonic imaging with an exceptional 76dBFS SNR over a 2MHz bandwidth, and -70dBc second-harmonic distortion at f_{RF} = 5MHz over the full receiver gain range. Near-carrier dynamic range has also been optimized for exceptional pulsed and color-flow Doppler performance under high-clutter conditions. The bipolar front-end and CMOS ADC achieve an exceptional near-carrier SNR of 137dBFS/Hz at 1kHz from a 5MHz tone for excellent low-velocity Doppler sensitivity.

The device also includes an octal CWD beamformer for a full Doppler solution. Separate mixers for each channel are available for optimal CWD sensitivity.

The MAX2079 octal ultrasound front-end is available in a small, 10mm x 10mm, CTBGA package and is specified over the 0°C to +70°C temperature range.

Applications

Medical Ultrasound Imaging

Sonar

Benefits and Features

- **Minimizes PCB Area and Design Cost**
  - **8 Full Channels of LNA, VGA, AAF, 12-Bit ADC, Digital HPF and CWD Mixer Beamformer in a Small, 10mm x 10mm CTBGA Package**
- **Improves System Sensitivity**
  - **Ultra-Low Full-Channel Noise Figure of 2.8dB at $R_S = R_{IN} = 200\Omega$**
- **Improves System Dynamic Range**
  - **76dBFS Image Path SNR Over 2MHz Bandwidth at f_{RF} = 5MHz**
  - **137dBFS/Hz Image Path SNR at 1kHz Offset from f_{RF} = 5MHz**
- **Consumes Less Power**
  - **Ultra-Low Power of Only 120mW per Full Channel in Imaging Mode at 50Msps**
- **Selectable Active Input Impedance Matching of 50Ω, 100Ω, 200Ω, and 1kΩ**
- **Programmable VGA Output Clamp**
- **Integrated Selectable 3-Pole 9MHz, 10MHz, 15MHz, and 18MHz Butterworth Anti-Alias Filter**
- **Programmable, Digital Highpass, 2-Pole Filter**
- **Serial LVDS Digital Outputs**
- **Fast Recovery Low-Power Modes (< 2µs)**
- **Separate Channel I/Q CWD Mixers for Improved Dynamic Range and Sensitivity**

Ordering Information appears at end of data sheet.

For related parts and recommended products to use with this part, refer to www.maximintegrated.com/MAX2079.related.

ABSOLUTE MAXIMUM RATINGS

V_{CC3}, V_{CC5} to GND....................-0.3V to +5.5V
AVDD, OVDD to GND....................-0.3V to +2.1V
V_{CC5} - V_{CC3} .... > -0.3V
V_{REF}, LO+/-, GC+/- to GND....................-0.3V to (V_{CC3} + 0.3V)
CI+/-, CQ+/- to GND....................-0.3V to +13V
ZF_, IN_, AG to GND....................-0.3V to (V_{CC5} + 0.3V)
INC_....................±20mA DC
IN_ to AG....................-0.6V to +0.6V
REFIO, CLKIN+/-, LOON to GND.......... -0.3V to the lower of (V_{AVDD} + 0.3V) and +2.1V
OUT+/-, SDIO, SCLK, $\overline{CS}$, CLKOUT+/-, FRAME+/-, SHDN, CWD to GND.... -0.3V to the lower of (V_{OVDD} + 0.3V) and +2.1V
CI+/-, CQ+/-, V_{CC5}, V_{CC3}, AVDD/OVDD, V_{REF} analog and digital control signals must be applied in this order.
Input Differential Voltage....................2.0V_{P-P} differential
Continuous Power Dissipation (T_A = +70°C)
144-Bump CTBGA (derate 33.3mW/°C above +70°C)....3200mW
Operating Case Temperature Range (Note 1)....0°C to +70°C
Junction Temperature....................+150°C
Storage Temperature Range....................-40°C to +150°C
Soldering Temperature (reflow)....................+260°C

Note 1: T_C is the temperature on the bump of the package. T_A is the ambient temperature of the device and PCB.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS (Note 2)

Junction-to-Ambient Thermal Resistance (θ_{JA})....................25°C/W
Junction-to-Case Thermal Resistance (θ_{JC})....................7.7°C/W

Note 2: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

OCTAL ULTRASOUND FRONT-END SPECIFICATIONS
DC ELECTRICAL CHARACTERISTICS—VGA MODE (CWD BEAMFORMER OFF)

(V_{REF} = 2.5V, V_{CC3} = 3.13V to 3.47V, V_{CC5} = 4.5V to 5.25V, V_{AVDD} = V_{OVDD} = 1.7V to 1.9V, T_A = 0°C to +70°C, V_{GND} = 0V, SHDN = 0, CWD = 0, LOON = 0, f_{RF} = 5MHz, 50mV_{P-P}, ADC f_{CLK} = 50Msps, digital HPF set to 60/64, two poles, 15/16 digital gain, V_{GC+} - V_{GC-} = -3V (minimum gain), high LNA gain. Typical values are at V_{REF} = 2.5V, V_{CC3} = 3.3V, V_{CC5} = 4.75V, V_{AVDD} = V_{OVDD} = 1.8V, V_{GC+} - V_{GC-} = 0V, T_A = +25°C, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
3.3V Supply Voltage	V_{CC3}	V_{CC3} pins	3.13	3.3	3.47	V
5V Supply Voltage	V_{CC5}	V_{CC5} pins	4.5	4.75	5.25	V
1.8V Supply Voltage	$V_{CC1.8}$	AVDD and OVDD pins	1.7	1.8	1.9	V
External Reference Voltage Range	V_{REF}	(Note 4)	2.475		2.525	V
External Reference Current		Total current into the V_{REF} pin		5		µA
3V Supply Current per Channel	I_{CC3}	Total I divided by 8, V_{GC+} - V_{GC-} = 0.4V		9.5	16	mA
5V Supply Current per Channel	I_{CC5}	Total I divided by 8		6.4	9	mA
1.8V Supply Current per Channel	$I_{CC1.8}$	Total I divided by 8, AVDD + OVDD		32	37.9	mA
		Total I divided by 8, AVDD		20	22.8	mA
		Total I divided by 8, OVDD		12	15.1	mA
DC Power per Channel	P_NM	V_{GC+} - V_{GC-} = -0.4V		120		mW
Differential Analog Control Voltage Range	VGAIN_RANG	V_{GC+} - V_{GC-}		±3		V

DC ELECTRICAL CHARACTERISTICS—VGA MODE (CWD BEAMFORMER OFF) (continued)

(V_{REF} = 2.5V, V_{CC3} = 3.13V to 3.47V, V_{CC5} = 4.5V to 5.25V, V_{AVDD} = V_{OVDD} = 1.7V to 1.9V, T_A = 0°C to +70°C, V_{GND} = 0V, SHDN = 0, CWD = 0, LOON = 0, f_{RF} = 5MHz, 50mV$_{P-P}$, ADC f_{CLK} = 50Msps, digital HPF set to 60/64, two poles, 15/16 digital gain, V_{GC+} - V_{GC-} = -3V (minimum gain), high LNA gain. Typical values are at V_{REF} = 2.5V, V_{CC3} = 3.3V, V_{CC5} = 4.75V, V_{AVDD} = V_{OVDD} = 1.8V, V_{GC+} - V_{GC-} = 0V, T_A = +25°C, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
5V Supply Nap Current	I_NP_5V_TOT	SHDN = 1, nap mode (all 8 channels)		30		mA
3V Supply Nap Current	I_NP_3V_TOT	SHDN = 1, nap mode (all 8 channels)		0.035		mA
1.8V Supply Nap Current		SHDN = 1, nap mode (all 8 channels)		40		mA
5V Supply Power-Down Current	I_PD_5V_TOT	SHDN = 1, power-down mode (all 8 channels)		1		µA
3V Supply Power-Down Current	I_PD_3V_TOT	SHDN = 1, power-down mode (all 8 channels)		1		µA
1.8V Supply Power-Down Current		SHDN = 1, power-down mode (all 8 channels)		0.38		mA
Common-Mode Voltage for Differential Analog Control	VGAIN_COMM	(V_{GC+} - V_{GC-})/2		1.65 ±5%		V
Source/Sink Current for Gain Control Pins	I_ACONTROL	Per pin		±1.6		µA

AC ELECTRICAL CHARACTERISTICS—VGA MODE (CWD BEAMFORMER OFF)

(V_{REF} = 2.5V, V_{CC3} = 3.13V to 3.47V, V_{CC5} = 4.5V to 5.25V, V_{AVDD} = V_{OVDD} = 1.7V to 1.9V, T_A = 0°C to +70°C, V_{GND} = 0V, SHDN = 0, CWD = 0, LOON = 0, f_{RF} = 5MHz, 50mV$_{P-P}$, ADC f_{CLK} = 50Msps, digital HPF set to 60/64, two poles, 15/16 digital gain, V_{GC+} - V_{GC-} = -3V (minimum gain), high LNA gain. Typical values are at V_{REF} = 2.5V, V_{CC3} = 3.3V, V_{CC5} = 4.75V, V_{AVDD} = V_{OVDD} = 1.8V, V_{GC+} - V_{GC-} = 0V, T_A = +25°C, unless otherwise noted.) (Note 3)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
ADC Bits			12		Bits
Minimum ADC Sample Rate			25		Msps
Maximum ADC Sample Rate		50			Msps
Mode-Select Response Time (Note 5)	CWD stepped from 0 to 1, DC stable within 10%		1		µs
	CWD stepped from 1 to 0, DC stable within 10%		1		
Input Impedance	50Ω mode, f_{RF} = 2MHz		50		Ω
	100Ω mode, f_{RF} = 2MHz		100		
	200Ω mode, f_{RF} = 2MHz		200		
	1kΩ mode, f_{RF} = 2MHz		1000		
Noise Figure (High LNA Gain)	R_S = R_{IN} = 50Ω, V_{GC+} - V_{GC-} = +3V		4.8		dB
	R_S = R_{IN} = 100Ω, V_{GC+} - V_{GC-} = +3V		3.8		
	R_S = R_{IN} = 200Ω, V_{GC+} - V_{GC-} = +3V		2.8		
	R_S = R_{IN} = 1000Ω, V_{GC+} - V_{GC-} = +3V		2.5		
Noise Figure (Low LNA Gain)	R_S = R_{IN} = 200Ω, V_{GC+} - V_{GC-} = +3V		3.8		dB

AC ELECTRICAL CHARACTERISTICS—VGA MODE (CWD BEAMFORMER OFF) (continued)

(V_{REF} = 2.5V, V_{CC3} = 3.13V to 3.47V, V_{CC5} = 4.5V to 5.25V, V_{AVDD} = V_{OVDD} = 1.7V to 1.9V, T_A = 0°C to +70°C, V_{GND} = 0V, SHDN = 0, CWD = 0, LOON = 0, f_{RF} = 5MHz, 50mV$_{P-P}$, ADC f_{CLK} = 50Msps, digital HPF set to 60/64, two poles, 15/16 digital gain, V_{GC+} - V_{GC-} = -3V (minimum gain), high LNA gain. Typical values are at V_{REF} = 2.5V, V_{CC3} = 3.3V, V_{CC5} = 4.75V, V_{AVDD} = V_{OVDD} = 1.8V, V_{GC+} - V_{GC-} = 0V, T_A = +25°C, unless otherwise noted.) (Note 3)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
8-Channel Correlated Noise Power	No input signal, ratio of 8-channel noise power to single-channel noise power		9.0		dB
	5MHz signal applied to all 8 channels, V_{GC+} - V_{GC-} = 0V, f_{RF} = 5MHz at -3dBFS, ratio of 8-channel noise power to single-channel noise power		8.5		
LNA Gain (Low LNA Gain)			12.5		dB
LNA Gain (High LNA Gain)			18.5		dB
Maximum Gain (High LNA Gain)	V_{GC+} - V_{GC-} = +3V (max gain), LNA input to ADC Input		44.7		dB
Minimum Gain (High LNA Gain)	V_{GC+} - V_{GC-} = -3V (min gain), LNA input to ADC Input		5.9		dB
Maximum Gain (Low LNA Gain)	V_{GC+} - V_{GC-} = +3V (max gain), LNA input to ADC Input		40.4		dB
Minimum Gain (Low LNA Gain)	V_{GC+} - V_{GC-} = = -3V (min gain), LNA input to ADC input		1.4		dB
Gain Range			38.8		dB
AA Filter 3dB Corner Frequency	9MHz setting		9		MHz
	10MHz setting		10		
	15MHz setting		15		
	18MHz setting		18		
AA Filter 3dB Corner Frequency Accuracy			±10		%
Digital Highpass Filter 3dB Corner Frequency	2 poles, coefficients R1 = R2 = 63/64, f_{CLK} = 50Msps		0.185		MHz
	2 poles, coefficients R1 = R2 = 54/64, f_{CLK} = 50Msps		1.736		
Clamp Level	Clamp on (V$_{P-P}$ on AAF Output/ADC Input, digital HPF bypassed)		92		%FS
Device-to-Device Gain Matching	T_A = +25°C, V_{GC+} - V_{GC-} = -3V to +3V (Note 6)	-1.6	±0.5	+1.6	dB
Input Gain Compression	LNA = high gain, V_{GC+} - V_{GC-} = -3V (VGA = min gain), gain ratio with 330mV$_{P-P}$/50mV$_{P-P}$ input tones		0.7		dB
	LNA = low gain, V_{GC+} - V_{GC-} = -3V (VGA = min gain), gain ratio with 600mV$_{P-P}$/50mV$_{P-P}$ input tones		0.9		
VGA Gain Response Time	Gain step up (V_{IN} = 5mV$_{P-P}$, V_{GC+} - V_{GC-} changed from -3V to +3V, settling time is measured within 1dB final value)		0.8		µs
	Gain step down (V_{IN} = 5mV$_{P-P}$, V_{GC+} - V_{GC-} changed from -3V to +3V, settling time is measured within 1dB final value)		1.8		
VGA Output Offset Under Pulsed Overload	Over drive is ±10mA in clamping diodes, V_{GC+} - V_{GC-} = 1.0V (gain = 30dB), 16 pulses at 5MHz, repetition rate 20kHz; offset is measured at output when RF duty cycle is off		< 3.3		%FS
Signal-to-Noise Over ADC Nyquist Band (25MHz)	$V_{OUT\_}$ = -1dBFS, V_{IN} = 200mV$_{P-P}$, f_{RF} = 5MHz at -1dBFS, anti-alias filter = 9MHz, 50Msps sample rate		67		dBFS

AC ELECTRICAL CHARACTERISTICS—VGA MODE (CWD BEAMFORMER OFF) (continued)

(V_{REF} = 2.5V, V_{CC3} = 3.13V to 3.47V, V_{CC5} = 4.5V to 5.25V, V_{AVDD} = V_{OVDD} = 1.7V to 1.9V, T_A = 0°C to +70°C, V_{GND} = 0V, SHDN = 0, CWD = 0, LOON = 0, f_{RF} = 5MHz, 50mV_{P-P}, ADC f_{CLK} = 50Msps, digital HPF set to 60/64, two poles, 15/16 digital gain, V_{GC+} - V_{GC-} = -3V (minimum gain), high LNA gain. Typical values are at V_{REF} = 2.5V, V_{CC3} = 3.3V, V_{CC5} = 4.75V, V_{AVDD} = V_{OVDD} = 1.8V, V_{GC+} - V_{GC-} = 0V, T_A = +25°C, unless otherwise noted.) (Note 3)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Signal-to-Noise Over 2MHz Bandwidth	$V_{OUT\_}$ = -1dBFS, V_{IN} = 200mV_{P-P}, f_{RF} = 5MHz at -1dBFS, anti-alias filter = 9MHz, 50Msps sample rate		76		dBFS
Near-Carrier Signal-to-Noise Ratio	V_{GC+} - V_{GC-} = 0V (gain = 22dB), f_{RF} = 5.3MHz at -0.5dBFS, measured at 1kHz from f_{RF}, 50Msps sample rate		-137		dBFS/Hz
Second Harmonic (HD2)	V_{IN} = 50mV_{P-P}, f_{RF} = 2MHz, ADC out = -3dBFS		-71		dBc
	V_{IN} = 50mV_{P-P}, f_{RF} = 5MHz, ADC out = -3dBFS		-70		
IM3 Distortion	V_{IN} = 50mV_{P-P}, f_{RF1} = 5MHz, f_{RF2} = 5.01MHz ADC out = -3dBFS (Note 7)		-54		dBc
Nap Mode Power-Up Response Time	V_{GC+}-V_{GC-} = 0.6V (gain = 28dB), f_{RF} = 5MHz, ADC out = -3dBFS, settled with in 1dB from transition on SHDN pin (includes ADC)		2		µs
Nap Mode Power-Down Response Time	To reach DC current target ±10%, on V_{CC5}, V_{CC3}, AVDD, OVDD from transition on SHDN pin		4		µs
Sleep Mode Power-Up Response Time	V_{GC+} - V_{GC-} = 0.6V (gain = 28dB), f_{RF} = 5MHz, $V_{OUT\_}$ = -1dBFS, settled within 1dB from transition on SHDN		2		ms
Sleep Mode Power-Down Response Time	V_{GC+} - V_{GC-} = 0.6V (gain = 28dB), f_{RF} = 5MHz, DC power reaches 1mW/channel, from transition on SHDN (includes ADC)		4		ms
Adjacent-Channel Crosstalk	$V_{OUT\_}$ = -3dBFS, f_{RF} = 5MHz, V_{GC+} - V_{GC-} = 0.6V (gain = 28dB)		-60		dBc
Alternate-Channel Crosstalk	$V_{OUT\_}$ = -3dBFS, f_{RF} = 5MHz, V_{GC+} - V_{GC-} = 0.6V (gain = 28dB)		-80		dBc
Phase Matching Between Channels	V_{GC+}-V_{GC-} = 0.6V (gain = 28dB), f_{RF} = 5MHz, $V_{OUT\_}$ = -3dBFS		±1.2		Degrees

DC ELECTRICAL CHARACTERISTICS—CWD MODE (VGA, AAF, AND ADC OFF)

(V_{REF} = 2.5V, V_{CC3} = 3.13V to 3.47V, V_{CC5} = 4.5V to 5.25V, V_{AVDD} = V_{OVDD} = 1.7V to 1.9V, T_A = 0°C to +70°C, V_{GND} = 0V, SHDN = 0, CWD = 1, LOON = 1, R_{IN} = 200Ω, high LNA gain, CI+, CI-, CQ+, CQ- pulled up to +11V through four separate 0.1% 120Ω resistors. No RF signals applied. Typical values are at V_{REF} = 2.5V, V_{CC3} = 3.3V, V_{CC5} = 4.75V, V_{AVDD} = V_{OVDD} = 1.8V, T_A = +25°C, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Mixer LVDS LO Input Common-Mode Voltage	V_LVDS_CM	Pins LO+ and LO-		1.25 ± 0.2		V
LVDS LO Differential Input Voltage	V_LVDS_DM	Common-mode input voltage = 1.25V (Note 8)	200	700		mV_{P-P}
LVDS LO Input Common-Mode Current	I_LVDS_CM	Input bias current, common-mode input voltage = 1.25V (Note 8)		160		µA

DC ELECTRICAL CHARACTERISTICS—CWD MODE (VGA, AAF, AND ADC OFF) (continued)

(V_{REF} = 2.5V, V_{CC3} = 3.13V to 3.47V, V_{CC5} = 4.5V to 5.25V, V_{AVDD} = V_{OVDD} = 1.7V to 1.9V, T_A = 0°C to +70°C, V_{GND} = 0V, SHDN = 0, CWD = 1, LOON = 1, R_{IN} = 200Ω, high LNA gain, CI+, CI-, CQ+, CQ- pulled up to +11V through four separate 0.1% 120Ω resistors. No RF signals applied. Typical values are at V_{REF} = 2.5V, V_{CC3} = 3.3V, V_{CC5} = 4.75V, V_{AVDD} = V_{OVDD} = 1.8V, T_A = +25°C, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LVDS LO Differential Input Resistance	R_LVDS_DM	(Note 9)		8		kΩ
FULL-POWER MODE						
5V Supply Current per Channel	I_C_5V_F	Total I divided by 8		31.6	41	mA
3.3V Supply Current per Channel	I_C_3_3V_F	Total I divided by 8		1.8	3	mA
1.8V Supply Current per Channel	I_C_1_8V_F	Total I divided by 8, AVDD + OVDD		6.3		mA
11V Supply Current per Channel	I_C_11V_F	Total I divided by 8		11.7	16.2	mA
External Reference Current		Total current into V_{REF} pin		70		µA
On-Chip Power Dissipation (All 8 Channels)	PDIS_FP_TOT_F	(Note 11)		2.1		W
On-Chip Power Dissipation per Channel	PDIS_FP_F	(Note 11)		260		mW
5V Power-Down Current		SHDN = 1, power-down mode (all 8 channels)		1		µA
3V Power-Down Current		SHDN = 1, power-down mode (all 8 channels)		1		µA
1.8V Supply Power-Down Current		SHDN = 1, power-down mode (all 8 channels)		0.38		mA
LOW-POWER MODE						
5V Supply Current per Channel	I_C_5V_L	Total I divided by 8		27	35	mA
3.3V Supply Current per Channel	I_C_3_3V_L	Total I divided by 8		1.8	3	mA
1.8V Supply Current per Channel	I_C_1_8V_L	Total I divided by 8, AVDD + OVDD		6.3		mA
11V Supply current per channel	I_C_11V_L	Total I divided by 8		7		mA
On-Chip Power Dissipation (All 8 Channels)	PDIS_FP_TOT_L	(Note 11)		1.6		W
On-Chip Power Dissipation per Channel	PDIS_FP_L	(Note 11)		200		mW

AC ELECTRICAL CHARACTERISTICS—CWD MODE (VGA, AAF, AND ADC OFF)

(V_{REF} = 2.5V, V_{CC3} = 3.13V to 3.47V, V_{CC5} = 4.5V to 5.25V, V_{AVDD} = V_{OVDD} = 1.7V to 1.9V, T_A = 0°C to +70°C, V_{GND} = 0V, SHDN = 0, CWD = 1, SHDN = 0, LOON = 1, R_{IN} = 200Ω, f_{RF} = 5MHz, Source resistance R_S = 200Ω, CI+, CI-, CQ+, CQ- pulled up to +11V through four separate 0.1% 120Ω resistors). The rise/fall time of the LVDS clock driving LO+/LO- is required to be 0.5ns, reference noise less than 10nV/√Hz from 1kHz to 20MHz (Note 10). Typical values are at V_{CC3} = 3.3V, V_{CC5} = 4.75V, V_{AVDD} = V_{OVDD} = 1.8V, T_A = +25°C, unless otherwise noted.) (Note 3)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CW DOPPER MIXER					
Mixer RF Frequency Range		0.9		7.6	MHz
LO Frequency Range		8.0		60	MHz
Mixer Output Frequency Range		DC		100	kHz
FULL-POWER MODE					
Noise Figure	No carrier		4.8		dB
SNR at 100mV_{P-P} Input	100mV_{P-P} on input, f_{RF} = f_{LO}/8 = 1.25MHz, measured at 1kHz offset		146		dBc/Hz
SNR at 200mV_{P-P} Input	200mV_{P-P} on input, f_{RF} = f_{LO}/8 = 1.25MHz, measured at 1kHz offset		151		dBc/Hz
IM3 Distortion	V_{IN} = 100mV_{P-P}, f_{RF1} = 5MHz, f_{RF2} = 5.01MHz, f_{LO} = 8 x 5MHz (Note 7)		-57		dBc
Mixer Output-Voltage Compliance	Valid voltage range (AC + DC) on summed mixer output pins (Note12)	4.5		12	V
Channel-to-Channel Phase Matching	Measured under zero beat conditions. V_{IN} = 100mV_{P-P}, f_{RF} = 5MHz, f_{LO}/8 = 5MHz	-1	±0.5	+1	Degrees
Channel-to-Channel Gain Matching	Measured under zero beat conditions V_{IN} = 100mV_{P-P}, f_{RF} = 5MHz, f_{LO}/8 = 5MHz	-1	±0.5	+1	dB
Transconductance	f_{LO}/8 = 1.25MHz (Note 13)	19	23	26.5	mS
LOW-POWER MODE					
Noise Figure	No carrier		4.8		dB
SNR at 100mV_{P-P} Input	100mV_{P-P} on input, f_{RF} = f_{LO}/8 = 1.25MHz, measured at 1kHz offset		146		dBc/Hz
SNR at 200mV_{P-P} Input	200mV_{P-P} on input, f_{RF} = f_{LO}/8 = 1.25MHz, measured at 1kHz offset		150		dBc/Hz
IM3 Distortion	V_{IN} = 100mV_{P-P}, f_{RF1} = 5MHz, f_{RF2} = 5.01MHz, f_{LO} = 8 x 5MHz (Note 7)		-44		dBc
Mixer Output-Voltage Compliance	Valid voltage range (AC + DC) on summed mixer output pins (Note 12)	4.5		12	V
Transconductance	f_{LO}/8 = 1.25MHz (Note 13)	18	22	25.5	mS

ELECTRICAL CHARACTERISTICS—CLOCK AND TIMING

(V_{REF} = 2.5V, V_{CC3} = 3.13V to 3.47V, V_{CC5} = 4.5V to 5.25V, V_{AVDD} = V_{OVDD} = 1.7V to 1.9V, T_A = 0°C to +70°C, V_{GND} = 0V, SHDN = 0, CWD = 0, LOON = 0. f_{RF} = 5MHz, 50mV_{P-P}, ADC f_{CLK} = 50Msps, digital HPF set to 60/64, two poles, 15/16 digital gain, V_{GC+} - V_{GC-} = -3V (minimum gain), high LNA gain. Typical values are at V_{REF} = 2.5V, V_{CC3} = 3.3V, V_{CC5} = 4.75V, V_{AVDD} = V_{OVDD} = 1.8V, V_{GC+} - V_{GC-} = 0V, T_A = +25°C, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CLOCK INPUTS (CLKIN+, CLKIN-), DIFFERENTIAL MODE						
Differential Clock Input Voltage				0.4 to 2.0		V_{P-P}
Common-Mode Voltage	V_{CLKCM}	Self-biased		1.2		V
		DC-coupled clock signal		1.0 to 1.4		
Input Resistance	R_{CLK}	Differential, default setting		10		kΩ
		Differential, programmable internal termination selected		0.1		
		Common mode to GND		9		
Input Capacitance	C_{CLK}	Capacitance to GND, each input		3		pF
CLOCK INPUTS (CLKIN+, CLKIN-), SINGLE-ENDED MODE (CLKIN- < 0.1V)						
Single-Ended Mode-Selection Threshold (CLKIN-)					0.1	V
Single-Ended Clock Input High Threshold (CLKIN+)			1.5			V
Single-Ended Clock Input Low Threshold (CLKIN+)					0.3	V
Input Leakage (CLKIN+)		V_{IH} = 1.8V			+5	µA
		V_{IL} = 0V	-5			
Input Leakage (CLKIN-)		V_{IL} = 0V	-150		-50	µA
Input Capacitance (CLKIN+)				3		pF
DIGITAL INPUTS (CWD, LOON, SHDN, SCLK, SDIO, $\overline{CS}$)						
Input High Threshold	V_{IH}		1.5			V
Input Low Threshold	V_{IL}				0.3	V
Input Leakage	I_{IH}	V_{IH} = 1.8V			+5	µA
	I_{IL}	V_{IL} = 0V	-5			
Input Capacitance	C_{DIN}			3		pF
DIGITAL OUTPUTS (SDIO)						
Output Voltage Low	V_{OL}	I_{SINK} = 200µA			0.2	V
Output Voltage High	V_{OH}	I_{SOURCE} = 200µA	OVDD - 0.2			V
LVDS DIGITAL OUTPUTS (OUT_+/-, CLKOUT+/-, FRAME+/-) (I = 3.5mA, VCM = 1.2V)						
Differential Output Voltage	$\lvert V_{OD} \rvert$	R_{LOAD} = 100Ω	225	300	490	mV
Output Offset Voltage	V_{OS}		1.125	1.200	1.375	V

ELECTRICAL CHARACTERISTICS—CLOCK AND TIMING (continued)

(V_{REF} = 2.5V, V_{CC3} = 3.13V to 3.47V, V_{CC5} = 4.5V to 5.25V, V_{AVDD} = V_{OVDD} = 1.7V to 1.9V, T_A = 0°C to +70°C, V_{GND} = 0V, SHDN = 0, CWD = 0, LOON = 0. f_{RF} = 5MHz, 50mV$_{P-P}$, ADC f_{CLK} = 50Msps, digital HPF set to 60/64, two poles, 15/16 digital gain, V_{GC+} - V_{GC-} = -3V (minimum gain), high LNA gain. Typical values are at V_{REF} = 2.5V, V_{CC3} = 3.3V, V_{CC5} = 4.75V, V_{AVDD} = V_{OVDD} = 1.8V, V_{GC+} - V_{GC-} = 0V, T_A = +25°C, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SERIAL-PORT INTERFACE TIMING						
SCLK Period	t_{SCLK}		50			ns
SCLK-to-$\overline{CS}$ Setup Time	t_{CSS}		10			ns
SCLK-to-$\overline{CS}$ Hold Time	t_{CSH}		10			ns
SDIO-to-SCLK Setup Time	t_{SDS}	Serial-data write	10			ns
SDIO-to-SCLK Hold Time	t_{SDH}	Serial-data write	0			ns
SCLK-to-SDIO Output Data Delay	t_{SDD}	Serial-data read			10	ns
LVDS DIGITAL OUTPUT TIMING CHARACTERISTICS						
Data Valid to CLKOUT_ Rise/Fall	t_{OD}		(t_{SAMPLE}/ 24) - 0.10	(t_{SAMPLE}/ 24) + 0.05	(t_{SAMPLE}/ 24) + 0.20	ns
CLKOUT_ Output-Width High	t_{CH}			t_{SAMPLE}/ 12		ns
CLKOUT_ Output-Width Low	t_{CL}			t_{SAMPLE}/ 12		ns
FRAME_ Rise to CLKOUT_ Rise	t_{DF}		(t_{SAMPLE}/ 24) - 0.10	(t_{SAMPLE}/ 24) + 0.05	(t_{SAMPLE}/ 24) + 0.20	ns
Sample CLKIN_ Rise to FRAME_ Rise	t_{SF}		(t_{SAMPLE}/ 2) + 1.6	(t_{SAMPLE}/ 24) + 2.3	(t_{SAMPLE}/ 2) + 3.3	ns
CWD LO TIMING						
LOON Setup Time	t_{SU}	Setup time from LOON high to LVDS LO clock low-to-high transition	5			ns

ELECTRICAL CHARACTERISTICS—CLOCK AND TIMING (continued)

(V_{REF} = 2.5V, V_{CC3} = 3.13V to 3.47V, V_{CC5} = 4.5V to 5.25V, V_{AVDD} = V_{OVDD} = 1.7V to 1.9V, T_A = 0°C to +70°C, V_{GND} = 0V, SHDN = 0, CWD = 0, LOON = 0. f_{RF} = 5MHz, 50mV$_{P-P}$, ADC f_{CLK} = 50Msps, digital HPF set to 60/64, two poles, 15/16 digital gain, V_{GC+} - V_{GC-} = -3V (minimum gain), high LNA gain. Typical values are at V_{REF} = 2.5V, V_{CC3} = 3.3V, V_{CC5} = 4.75V, V_{AVDD} = V_{OVDD} = 1.8V, V_{GC+} - V_{GC-} = 0V, T_A = +25°C, unless otherwise noted.) (Note 3)

Note 3: Minimum and maximum limits at T_A = +25°C and +70°C are guaranteed by production test. Specifications for T_A < +25°C are guaranteed by design and/or characterization.

Note 4: Noise performance of the device is dependent on the noise contribution from V_{REF}. Use a low-noise supply for V_{REF}.

Note 5: This response time does not include the CW output highpass filter. When switching to VGA mode, the CW outputs stop drawing current and the output voltage goes to the rail. If a highpass filter is used, the recovery time can be excessive and a switching network is recommended.

Note 6: Specifications are guaranteed by design and characterization.

Note 7: See Figure 22 in the *Ultrasound-Specific IMD3 Specification* section.

Note 8: The LVDS CWD LO inputs are DC-coupled. See the *CWD Beamformer Programming and Clocking* section for details of LO startup synchronization.

Note 9: An external 100Ω resistor terminates the LVDS differential signal path (LO+, LO-).

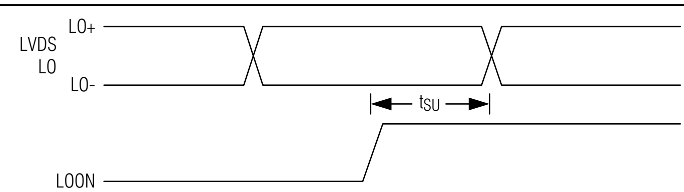
Note 10: The reference input noise is given for 8 channels, knowing that the reference-noise contributions are correlated in all 8 channels. If more channels are used, the reference noise must be reduced to get the best noise performance.

Note 11: Total on-chip power dissipation is calculated as $P_{DISS} = V_{CC5} \times I_{CC5} + V_{CC3} \times I_{CC3} + V_{AVDD} \times I_{AVDD} + V_{OVDD} \times I_{OVDD} + V_{REF} \times I_{REF} + [11V - (I_{11V}/4) \times 120] \times I_{11V}$. Additional power is dissipated through the off-chip 120Ω load resistors.

Note 12: Mixer output-voltage compliance is the range of acceptable voltages allowed on the CW mixer outputs.

Note 13: Transconductance is defined as the differential output current at baseband for each individual (I or Q) mixer output, divided by the single-ended RF input voltage directly on a single LNA input pin (INj). This can be calculated as $g_{mI} = (I_{CI+} - I_{CI-})/V_{INj}$ and $g_{mQ} = (I_{CQ+} - I_{CQ-})/V_{INj}$; or equivalently as $g_{mI} = (V_{CI+} - V_{CI-})/(R_L \times V_{INj})$ and $g_{mQ} = (I_{CQ+} - I_{CQ-})/(R_L \times V_{INj})$ (where j = 1, 2, …8 is a specific channel number, INj is a single LNA input pin, and R_L is the load resistance on each individual mixer output pin).

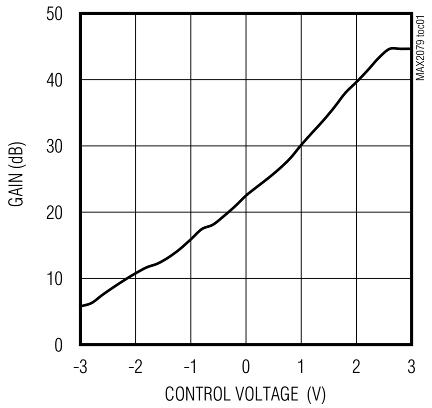
CWD LOON (LO On/Off) Timing Detail



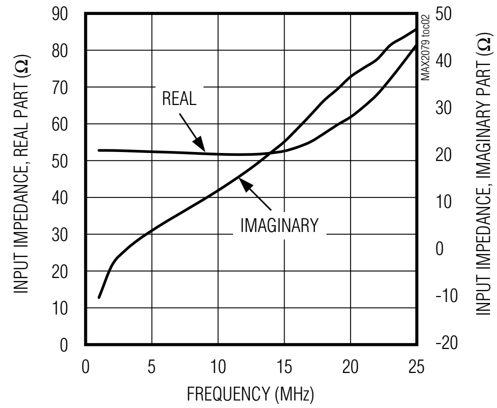
Typical Operating Characteristics

(Typical values are at V_{REF} = 2.5V, V_{CC3} = 3.3V, V_{CC5} = 4.75V, V_{AVDD} = V_{OVDD} = 1.8V, V_{GC+} - V_{GC-} = 0V, T_A = +25°C, unless otherwise noted.) (Note 3)

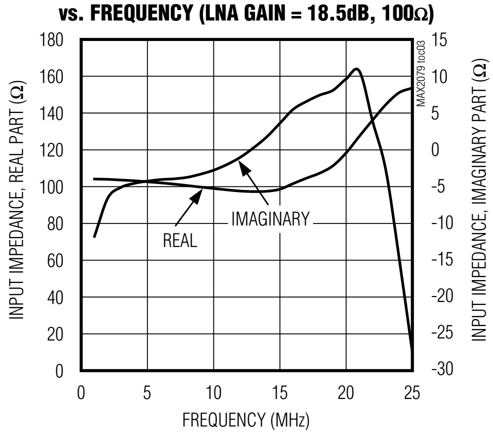
GAIN vs. DIFFERENTIAL ANALOG CONTROL VOLTAGE



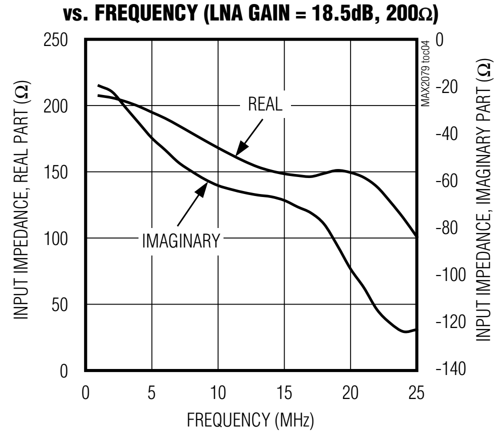
COMPLEX INPUT IMPEDANCE MAGNITUDE vs. FREQUENCY (LNA GAIN = 18.5dB, 50Ω)



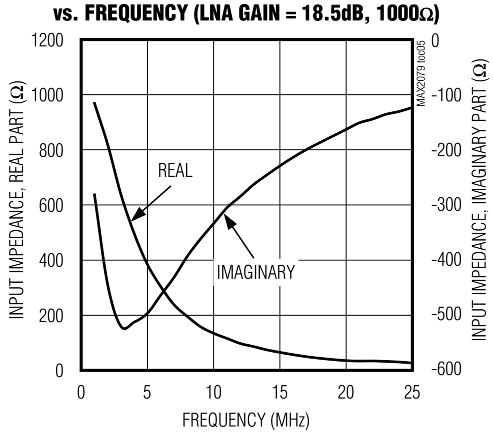
COMPLEX INPUT IMPEDANCE MAGNITUDE vs. FREQUENCY (LNA GAIN = 18.5dB, 100Ω)



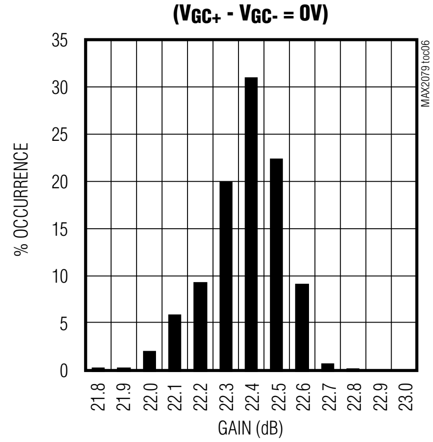
COMPLEX INPUT IMPEDANCE MAGNITUDE vs. FREQUENCY (LNA GAIN = 18.5dB, 200Ω)



COMPLEX INPUT IMPEDANCE MAGNITUDE vs. FREQUENCY (LNA GAIN = 18.5dB, 1000Ω)



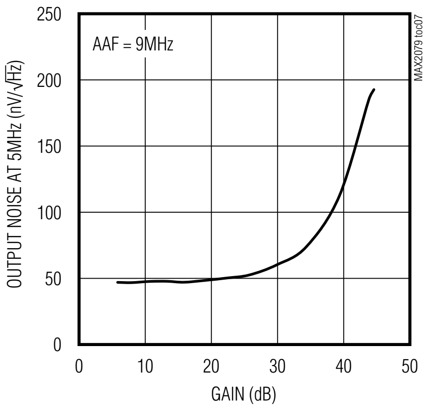
GAIN DISTRIBUTION (V_{GC+} - V_{GC-} = 0V)



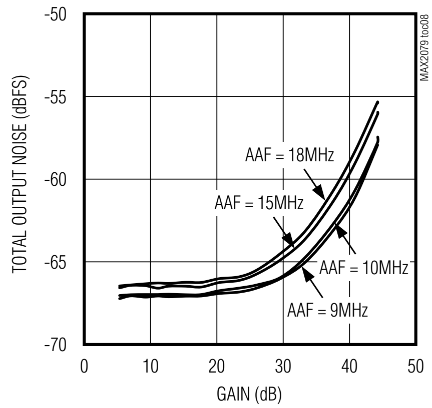
Typical Operating Characteristics (continued)

(Typical values are at V_{REF} = 2.5V, V_{CC3} = 3.3V, V_{CC5} = 4.75V, V_{AVDD} = V_{OVDD} = 1.8V, V_{GC+} - V_{GC-} = 0V, T_A = +25°C, unless otherwise noted.) (Note 3)

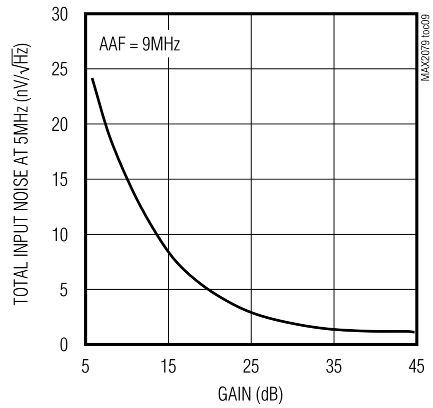
TOTAL OUTPUT NOISE (AFE + ADC) vs. GAIN



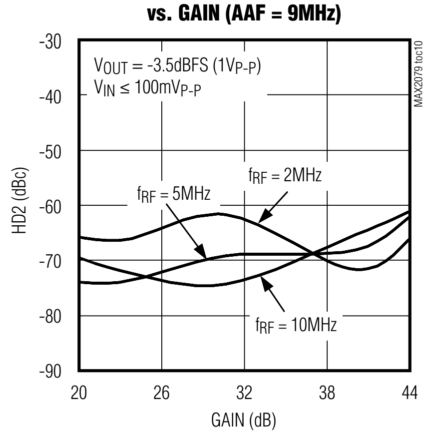
TOTAL OUTPUT NOISE vs. GAIN



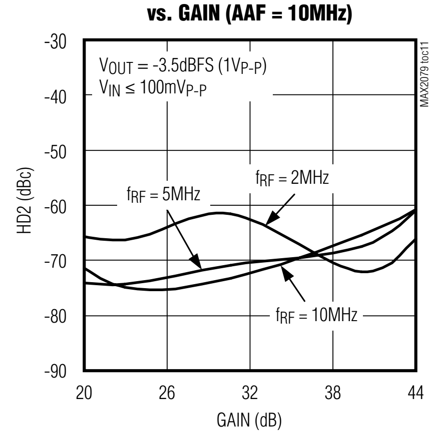
TOTAL INPUT NOISE (AFE + ADC) vs. GAIN



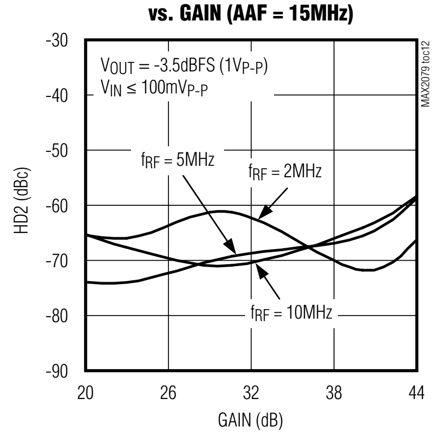
SECOND-HARMONIC DISTORTION vs. GAIN (AAF = 9MHz)



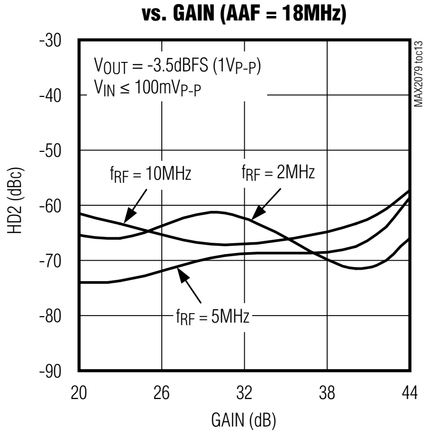
SECOND-HARMONIC DISTORTION vs. GAIN (AAF = 10MHz)



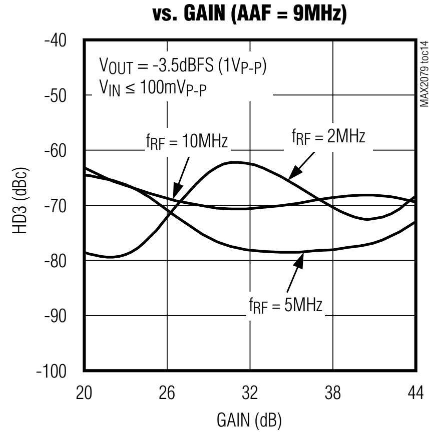
SECOND-HARMONIC DISTORTION vs. GAIN (AAF = 15MHz)



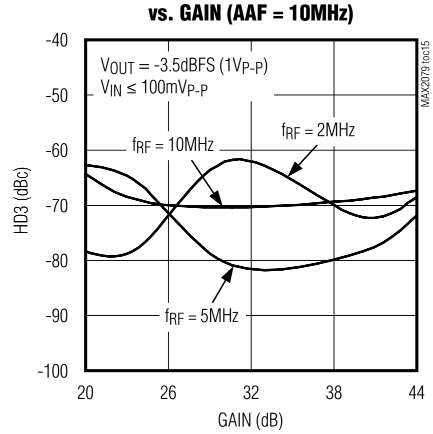
SECOND-HARMONIC DISTORTION vs. GAIN (AAF = 18MHz)



THIRD-HARMONIC DISTORTION vs. GAIN (AAF = 9MHz)



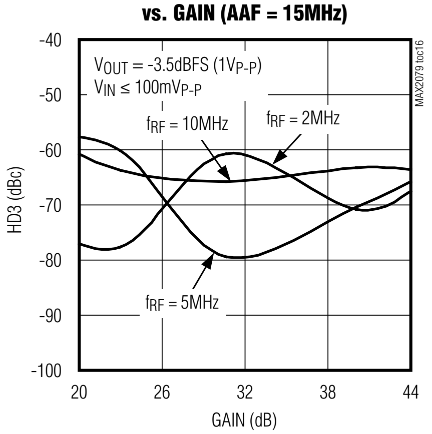
THIRD-HARMONIC DISTORTION vs. GAIN (AAF = 10MHz)



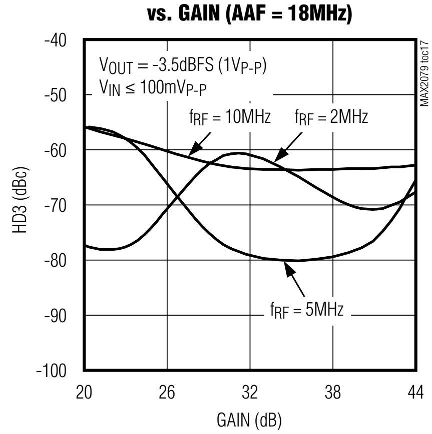
Typical Operating Characteristics (continued)

(Typical values are at V_{REF} = 2.5V, V_{CC3} = 3.3V, V_{CC5} = 4.75V, V_{AVDD} = V_{OVDD} = 1.8V, V_{GC+} - V_{GC-} = 0V, T_A = +25°C, unless otherwise noted.) (Note 3)

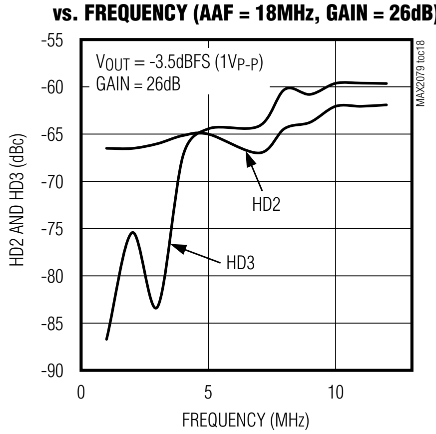
THIRD-HARMONIC DISTORTION vs. GAIN (AAF = 15MHz)



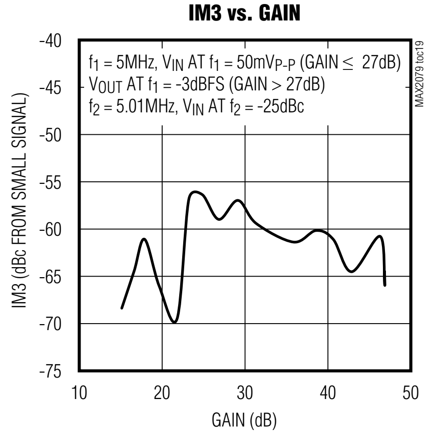
THIRD-HARMONIC DISTORTION vs. GAIN (AAF = 18MHz)



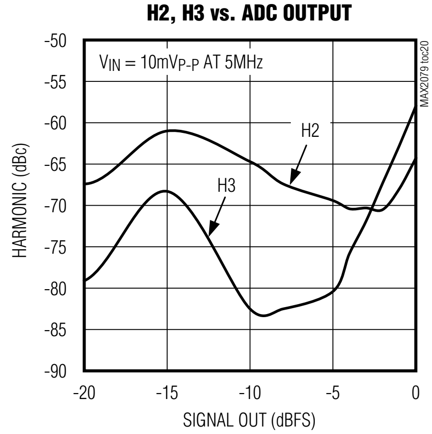
SECOND- AND THIRD-HARMONIC DISTORTION vs. FREQUENCY (AAF = 18MHz, GAIN = 26dB)



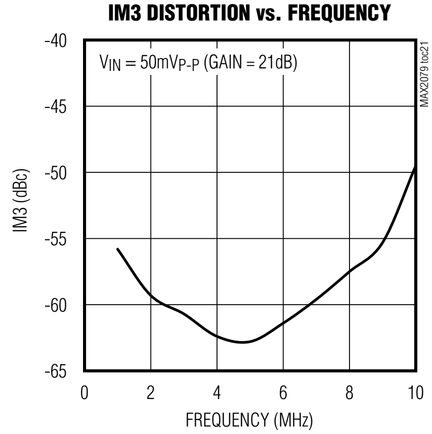
IM3 vs. GAIN



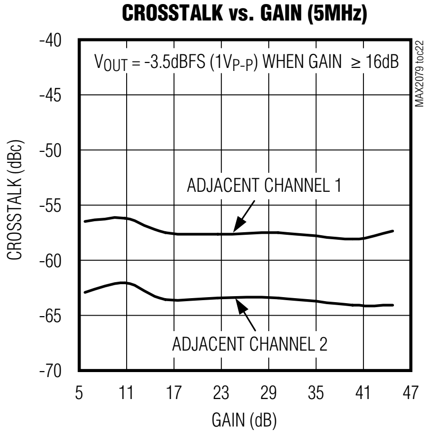
H2, H3 vs. ADC OUTPUT



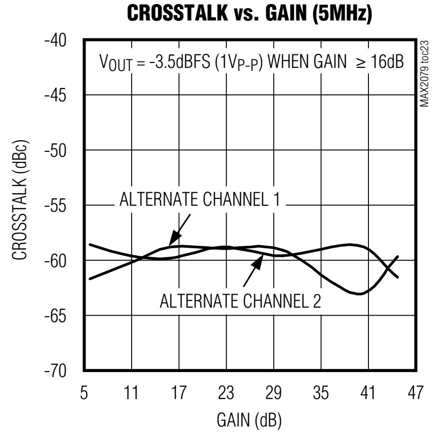
IM3 DISTORTION vs. FREQUENCY



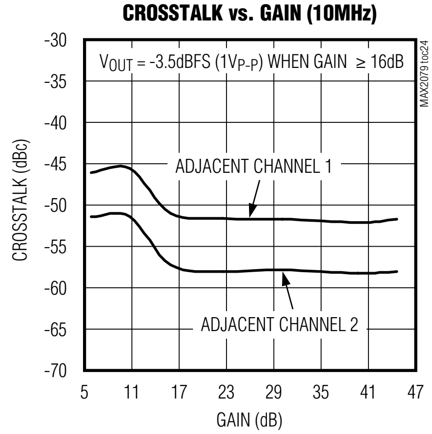
ADJACENT CHANNEL-TO-CHANNEL CROSSTALK vs. GAIN (5MHz)



ALTERNATE CHANNEL-TO-CHANNEL CROSSTALK vs. GAIN (5MHz)



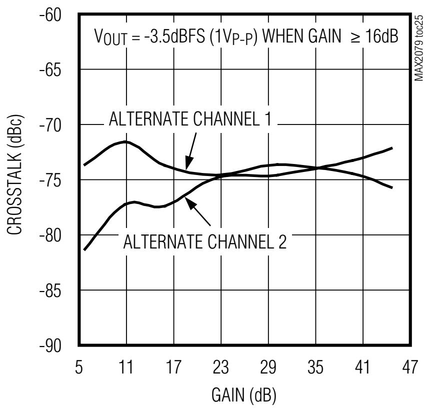
ADJACENT CHANNEL-TO-CHANNEL CROSSTALK vs. GAIN (10MHz)



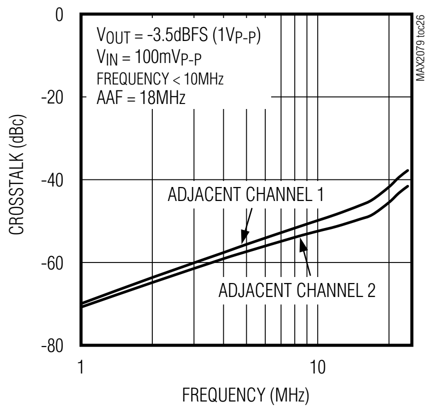
Typical Operating Characteristics (continued)

(Typical values are at V_{REF} = 2.5V, V_{CC3} = 3.3V, V_{CC5} = 4.75V, V_{AVDD} = V_{OVDD} = 1.8V, V_{GC+} - V_{GC-} = 0V, T_A = +25°C, unless otherwise noted.) (Note 3)

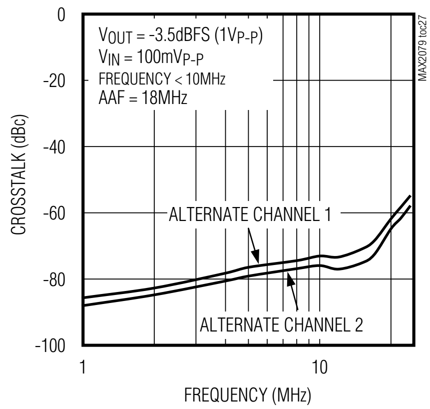
ALTERNATE CHANNEL-TO-CHANNEL CROSSTALK vs. GAIN (10MHz)



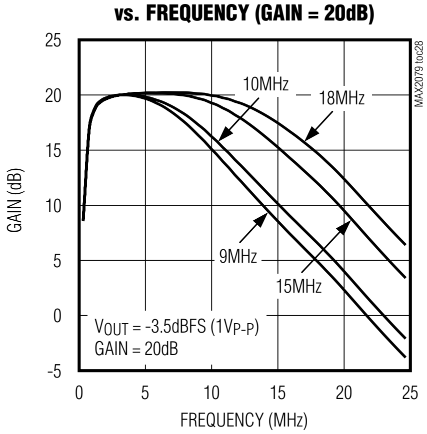
ADJACENT CHANNEL-TO-CHANNEL CROSSTALK vs. FREQUENCY



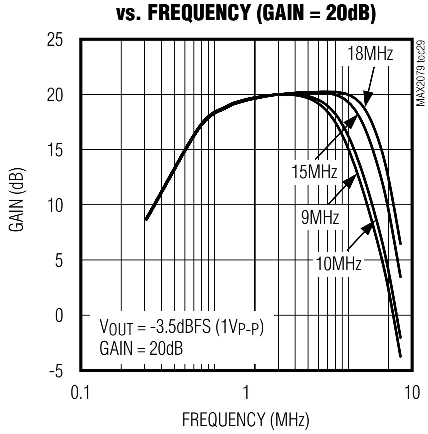
ALTERNATE CHANNEL-TO-CHANNEL CROSSTALK vs. FREQUENCY



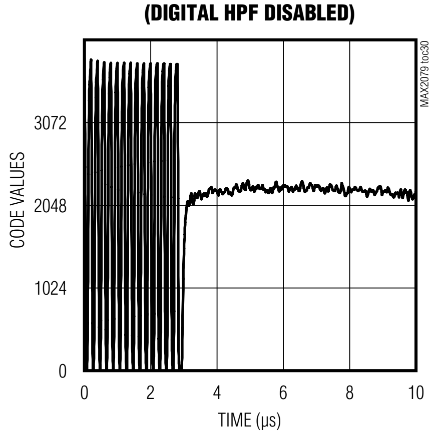
LARGE-SIGNAL BANDWIDTH vs. FREQUENCY (GAIN = 20dB)



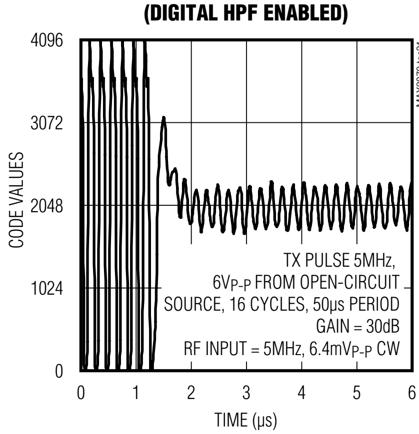
LARGE-SIGNAL BANDWIDTH vs. FREQUENCY (GAIN = 20dB)



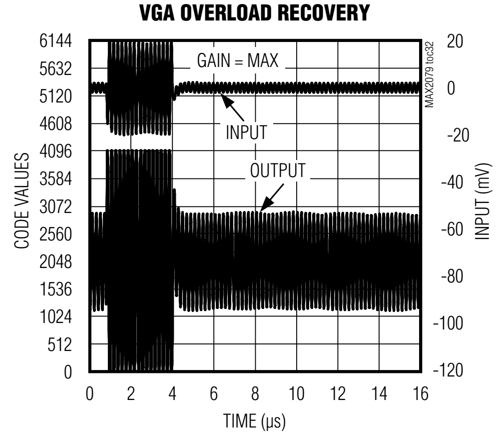
LNA OVERLOAD RECOVERY (DIGITAL HPF DISABLED)



LNA OVERLOAD RECOVERY (DIGITAL HPF ENABLED)

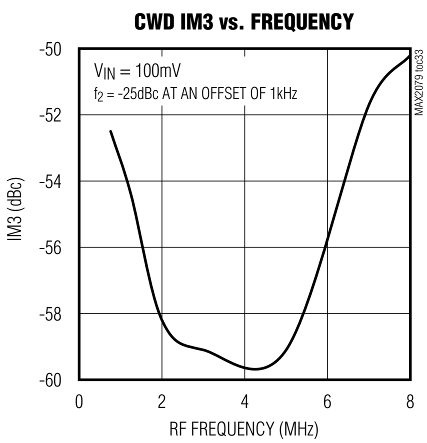


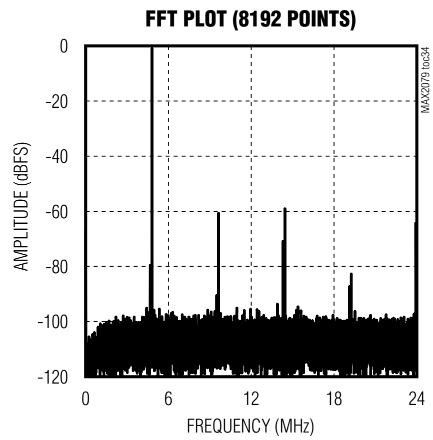
VGA OVERLOAD RECOVERY

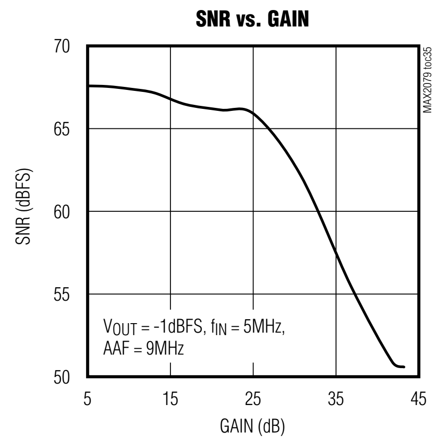


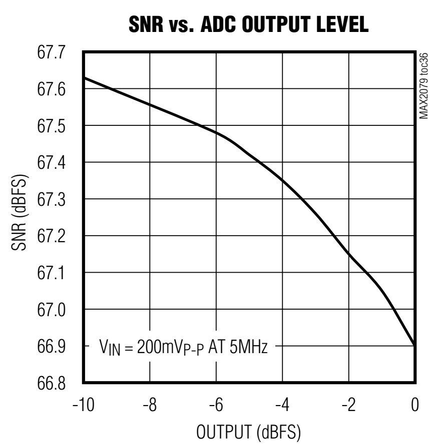
Typical Operating Characteristics (continued)

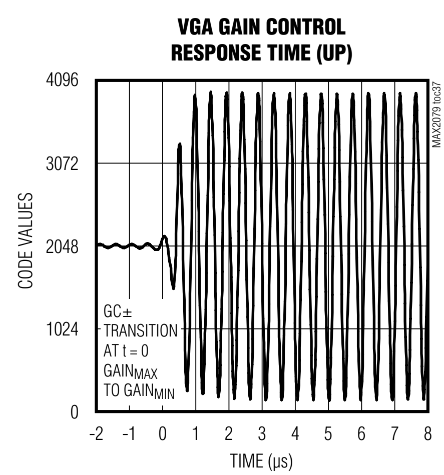
(Typical values are at V_{REF} = 2.5V, V_{CC3} = 3.3V, V_{CC5} = 4.75V, V_{AVDD} = V_{OVDD} = 1.8V, V_{GC+} - V_{GC-} = 0V, T_A = +25°C, unless otherwise noted.) (Note 3)







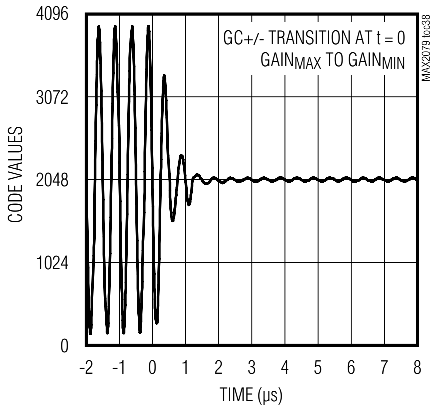




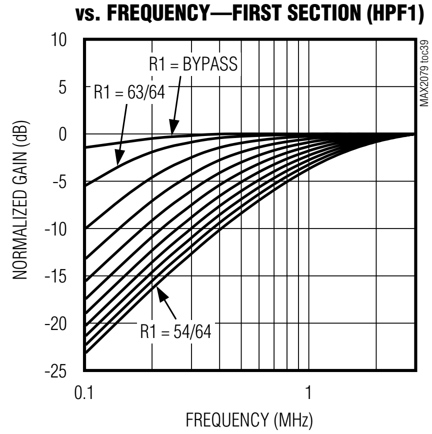
Typical Operating Characteristics (continued)

(Typical values are at V_{REF} = 2.5V, V_{CC3} = 3.3V, V_{CC5} = 4.75V, V_{AVDD} = V_{OVDD} = 1.8V, V_{GC+} - V_{GC-} = 0V, T_A = +25°C, unless otherwise noted.) (Note 3)

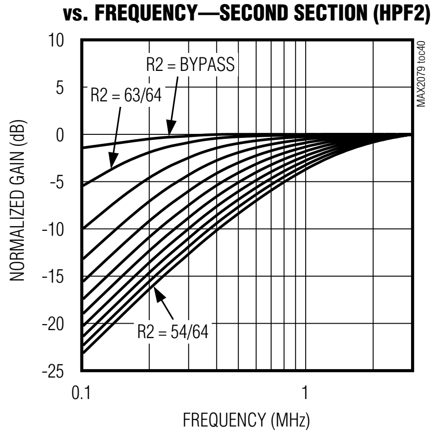
VGA GAIN CONTROL RESPONSE TIME (DOWN)



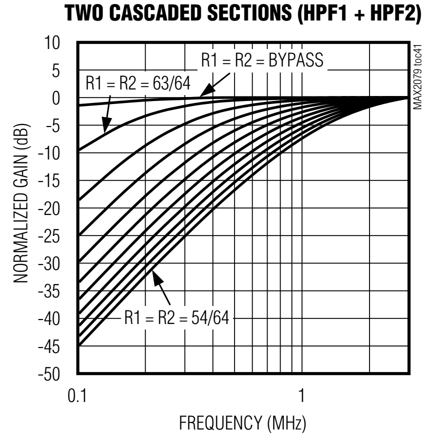
DIGITAL HIGHPASS FILTER NORMALIZED MAGNITUDE RESPONSES vs. FREQUENCY—FIRST SECTION (HPF1)



DIGITAL HIGHPASS FILTER NORMALIZED MAGNITUDE RESPONSES vs. FREQUENCY—SECOND SECTION (HPF2)



DIGITAL HIGHPASS FILTER NORMALIZED MAGNITUDE RESPONSES vs. FREQUENCY—TWO CASCADED SECTIONS (HPF1 + HPF2)



Bump Configuration

TOP VIEW

	1	2	3	4	5	6	7	8	9	10	11	12	
A	IN1	ZF1	V_{CC3}	CI+	CQ+	LO+	AVDD	N.C.	REFIO	CWD	GND	OVDD	A
B	ZF2	INC1	V_{CC5}	CI-	CQ-	LO-	LOON	AVDD	I.C.	SHDN	OUT1+	OUT1-	B
C	INC2	IN2	GND	GND	GND	GND	GND	GND	GND	GND	OUT2+	OUT2-	C
D	IN3	ZF3	GND	GND	GND	GND	GND	GND	GND	GND	OUT3+	OUT3-	D
E	ZF4	INC3	GND	GND	GND	GND	GND	GND	GND	GND	OUT4+	OUT4-	E
F	INC4	IN4	AG	GND	GND	GND	GND	GND	GND	OVDD	CLKOUT+	CLKOUT-	F
G	IN5	ZF5	AG	GND	GND	GND	GND	GND	GND	OVDD	FRAME+	FRAME-	G
H	ZF6	INC5	GND	GND	GND	GND	GND	GND	GND	GND	OUT5+	OUT5-	H
J	INC6	IN6	GND	GND	GND	GND	GND	GND	GND	GND	OUT6+	OUT6-	J
K	IN7	ZF7	GND	GND	GND	GND	GND	GND	GND	GND	OUT7+	OUT7-	K
L	ZF8	INC7	V_{CC5}	V_{REF}	GC-	V_{CC3}	AVDD	CLKIN+	GND	SDIO	OUT8+	OUT8-	L
M	IN8	INC8	V_{CC5}	V_{CC5}	GC+	V_{CC3}	AVDD	CLKIN-	GND	SCLK	$\overline{CS}$	OVDD	M
	1	2	3	4	5	6	7	8	9	10	11	12	

Bump Description

BUMP	NAME	FUNCTION
A1	IN1	Channel 1 Input. Connect to a 4.7nF coupling capacitor.
A2	ZF1	Channel 1 Active Impedance Matching Line. AC-couple to IN1 with a 2.2nF capacitor.
A3, L6, M6	V_{CC3}	3.3V Power-Supply Voltage. Bypass to GND with a 0.1µF capacitor as close as possible to the part.
A4	CI+	8-Channel CW Positive In-Phase Output. Connect to 11V with a 120Ω external resistor.
A5	CQ+	8-Channel CW Positive Quadrature Output. Connect to 11V with a 120Ω external resistor.
A6	LO+	Positive CW Local Oscillator Input. This clock is then divided in the beamformer.
A7, B8, L7, M7	AVDD	1.8V Analog ADC Power-Supply Voltage. Connect AVDD to a 1.7V to 1.9V power supply. Bypass AVDD to GND with a 0.1µF capacitor as close as possible to the device.
A8	N.C.	No Connection. Internally not connected.
A9	REFIO	I/O Reference (for Internal Calibration)
A10	CWD	VGA/CW Mode Select. Set CWD low to enable the VGAs and disable the CW mixers. Set CWD high to enable the CW mixers and disable the VGAs.
A11, C3–C10, D3–D10, E3–E10, F4–F9, G4–G9, H3–H10, J3–J10, K3–K10, L9, M9	GND	Ground
A12, F10, G10, M12	OVDD	1.8V Digital ADC Power-Supply Voltage. Bypass OVDD to GND with a 0.1µF capacitor as close as possible to the device.
B1	ZF2	Channel 2 Active Impedance Matching Line. AC-couple to IN2 with a 2.2nF capacitor.
B2	INC1	Channel 1 Clamp Input. Connect to the source side of the coupling capacitor.
B3, L3, M3, M4	V_{CC5}	4.75V Power-Supply Voltage. Bypass to GND with a 0.1µF capacitor as close as possible to the device.
B4	CI-	8-Channel CW Negative In-Phase Output. Connect to 11V with a 120Ω external resistor.
B5	CQ-	8-Channel CW Negative Quadrature Output. Connect to 11V with a 120Ω external resistor.
B6	LO-	Negative CW Local Oscillator Input
B7	LOON	LO On Control Input. Turns LO on starting on the next rising or falling edge of LO.
B9	I.C.	Internally Connected. Leave unconnected.
B10	SHDN	Power-Down (Nap or Sleep Mode Programmable through Serial Interface)
B11	OUT1+	Channel 1 Positive LVDS Output
B12	OUT1-	Channel 1 Negative LVDS Output
C1	INC2	Channel 2 Clamp Input. Connect to the source side of the coupling capacitor.
C2	IN2	Channel 2 Input. Connect to a 4.7nF coupling capacitor.

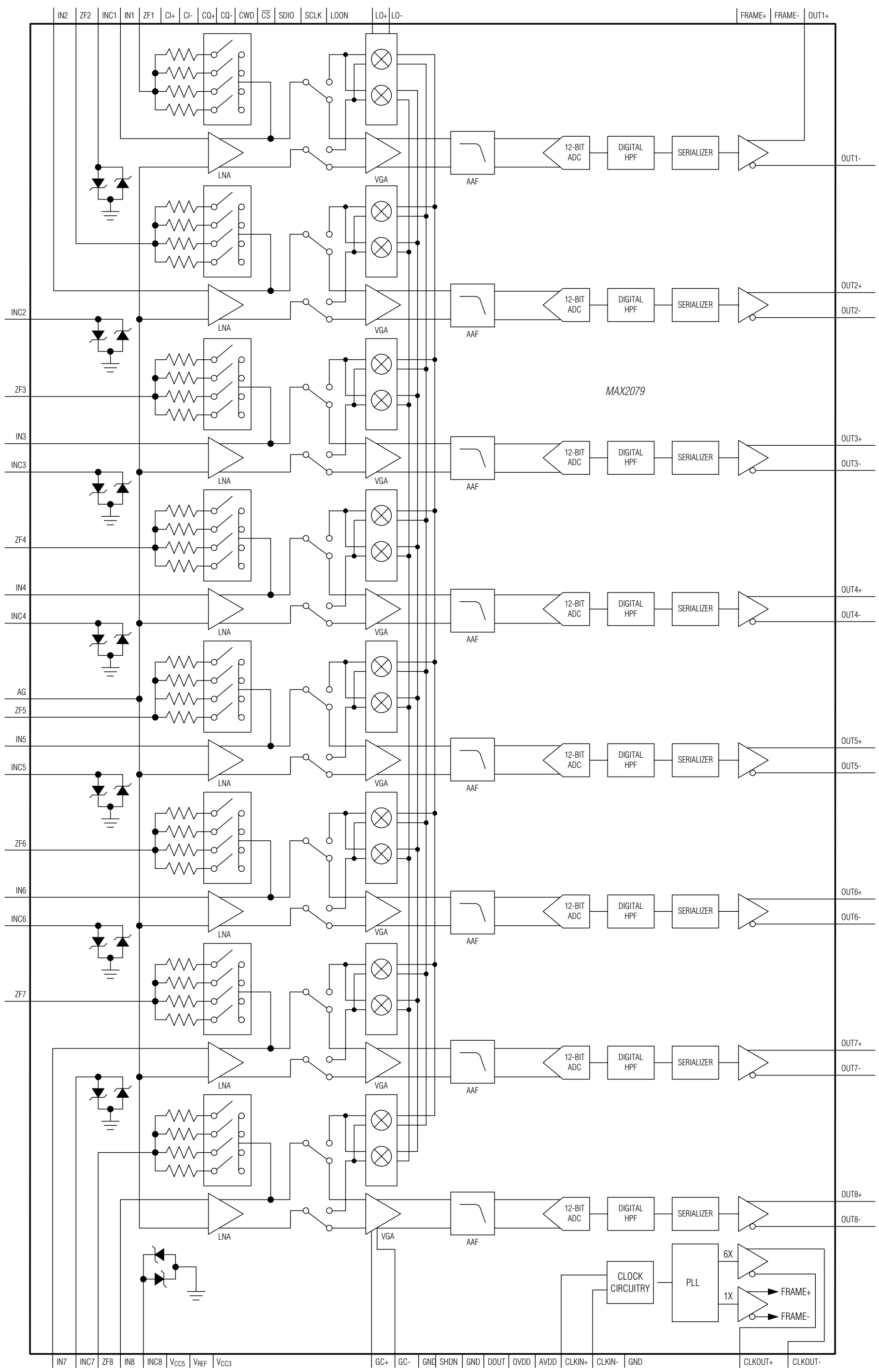
Bump Description (continued)

BUMP	NAME	FUNCTION
C11	OUT2+	Channel 2 Positive LVDS Output
C12	OUT2-	Channel 2 Negative LVDS Output
D1	IN3	Channel 3 Input. Connect to a 4.7nF coupling capacitor.
D2	ZF3	Channel 3 Active Impedance Matching Line. AC-couple to IN3 with a 2.2nF capacitor.
D11	OUT3+	Channel 3 Positive LVDS Output
D12	OUT3-	Channel 3 Negative LVDS Output
E1	ZF4	Channel 4 Active Impedance Matching Line. AC-couple to IN4 with a 2.2nF capacitor.
E2	INC3	Channel 3 Clamp Input. Connect to the source side of the coupling capacitor.
E11	OUT4+	Channel 4 Positive LVDS Output
E12	OUT4-	Channel 4 Negative LVDS Output
F1	INC4	Channel 4 Clamp Input. Connect to the source side of the coupling capacitor.
F2	IN4	Channel 4 Input. Connect to a 4.7nF coupling capacitor.
F11	CLKOUT+	Positive LVDS Serial-Clock Output
F12	CLKOUT-	Negative LVDS Serial-Clock Output
G1	IN5	Channel 5 Input. Connect to a 4.7nF coupling capacitor.
G2	ZF5	Channel 5 Active Impedance Matching Line. AC-couple to IN5 with a 2.2nF capacitor.
G3, F3	AG	Analog Ground for LNA Inputs. Connect to a 47nF AC-coupling capacitor to ground.
G11	FRAME+	Positive Frame-Alignment LVDS Output
G12	FRAME-	Negative Frame-Alignment LVDS Output
H1	ZF6	Channel 6 Active Impedance Matching Line. AC-couple to IN6 with a 2.2nF capacitor.
H2	INC5	Channel 5 Clamp Input. Connect to the source side of the coupling capacitor.
H11	OUT5+	Channel 5 Positive LVDS Output
H12	OUT5-	Channel 5 Negative LVDS Output
J1	INC6	Channel 6 Clamp Input. Connect to the source side of the coupling capacitor.
J2	IN6	Channel 6 Input. Connect to a 4.7nF coupling capacitor.
J11	OUT6+	Channel 6 Positive LVDS Output
J12	OUT6-	Channel 6 Negative LVDS Output
K1	IN7	Channel 7 Input. Connect to a 4.7nF coupling capacitor.
K2	ZF7	Channel 7 Active Impedance Matching Line. AC-couple to IN7 with a 2.2nF capacitor.
K11	OUT7+	Channel 7 Positive LVDS Output
K12	OUT7-	Channel 7 Negative LVDS Output
L1	ZF8	Channel 8 Active Impedance Matching Line. AC-couple to IN8 with a 2.2nF capacitor.
L2	INC7	Channel 7 Clamp Input. Connect to the source side of the coupling capacitor.
L4	V_{REF}	Voltage Reference
L5	GC-	Negative Gain Control Voltage. Set V_{GC+} - V_{GC-} = +3V for maximum gain. Set V_{GC+} - V_{GC-} = -3V for minimum gain.

Bump Description (continued)

BUMP	NAME	FUNCTION
L8	CLKIN+	Positive Differential ADC Clock Input
L10	SDIO	Serial-Data Input
L11	OUT8+	Channel 8 Positive LVDS Output
L12	OUT8-	Channel 8 Negative LVDS Output
M1	IN8	Channel 8 Input. Connect to a 4.7nF coupling capacitor.
M2	INC8	Channel 8 Clamp Input. Connect to the source side of the coupling capacitor.
M5	GC+	Positive Gain Control Voltage. Set V_{GC+} - V_{GC-} = +3V for maximum gain. Set V_{GC+} - V_{GC-} = -3V for minimum gain.
M8	CLKIN-	Negative Differential ADC Clock Input. Connect to 0V for a single-ended clock.
M10	SCLK	Serial-Clock Input
M11	$\overline{CS}$	Chip Select

Functional Diagram



Detailed Description

Modes of Operation

The device requires programming before it can be used. The operating modes are controlled by 17 8-bit registers (00h to 10h). Table 3 shows the functions of these programming registers.

Low-Noise Amplifier (LNA)

Each of the device's LNAs is optimized for excellent dynamic range and linearity performance characteristics, making it ideal for ultrasound imaging applications. When the LNA is placed in low-gain mode, the input resistance (R_{IN}), being a function of the gain A ($R_{IN} = R_F/(1 + A)$), increases by a factor of approximately 2. Consequently, the switches that control the feedback resistance (R_{FB}) have to be changed. For instance, the 100Ω mode in high gain becomes the 200Ω mode in low gain (see Table 30).

Variable-Gain Amplifier (VGA)

The device's VGAs are optimized for high linearity, high dynamic range, and low output-noise performance, all of which are critical parameters for ultrasound imaging applications. Each VGA path includes circuitry for adjusting analog gain, as well as an output buffer with differential output ports that drive the AAF and ADC. The VGA gain can be adjusted through the differential gain-control input (GC+ and GC-). Set the differential gain control input voltage at -3V for minimum gain and +3V for maximum gain. The differential analog control common-mode voltage is 1.65V (typ).

Overload Recovery

The device is also optimized for quick overload recovery for operation under the large input-signal conditions that are typically found in ultrasound input-buffer imaging applications. See the *Typical Operating Characteristics* for an illustration of the rapid recovery time from a transmit-related overload.

Dynamic offsets or DC offsets in the device can be removed by enabling the digital HPF function contained within the ADC. The unique structure of the digital HPF allows for the removal of up to ±117mV of dynamic or static DC offset, without reducing the dynamic range of the ADC.

Octal Continuous-Wave (CW) Mixer

The device CW mixers are designed using an active double-balanced topology. The mixers achieve high dynamic range and high-linearity performance, with exceptionally low thermal and jitter noise, ideal for ultrasound CWD signal reception.

The octal array exhibits quadrature and in-phase differential current outputs (CQ+, CQ-, CI+, CI-) to produce the total CWD beamformed signal. The maximum differential current output is typically $3mA_{P-P}$ and the mixer output-compliance voltage ranges from 4.5V to 12V.

Each mixer can be programmed to 1 of 16 phases; therefore, 4 bits are required for each channel for programming.

Each CW channel can be programmed to an off state by setting bit CW_SHDN_CHn to 1. The power-down mode (SHDN) line overrides this soft shutdown.

After the serial shift registers have been programmed, the $\overline{CS}$ signal, when going high, loads the phase information in the form of 5 bits per channel into the I/Q phase divider/selectors. This presets the dividers, selecting the appropriate mixer phasing. See Table 40 for mixer phase configurations.

CW Mixer Output Summation

The outputs from the octal-channel mixer array are summed internally to produce the total CWD summed beamformed signal. The octal array produces eight differential quadrature (Q) outputs and eight differential in-phase (I) outputs. All quadrature and in-phase outputs are summed into single I and Q differential current outputs (CQ+, CQ-, CI+, CI-).

CWD beamforming is achieved using a single 8 x LO high-frequency master clock that is divided down to the CWD frequency using internal dividers. The beamformer provides λ/16 resolution with an 8 x LO clock using both edges of the clock, assuming a 50% duty cycle. An easily available low-phase-noise 200MHz master clock can therefore be used to generate the necessary CWD frequencies with adequate resolution.

LO Phase Select

The LO phase dividers can be programmed through the shift registers to allow for 16 quadrature phases for a complete CW beamforming solution.

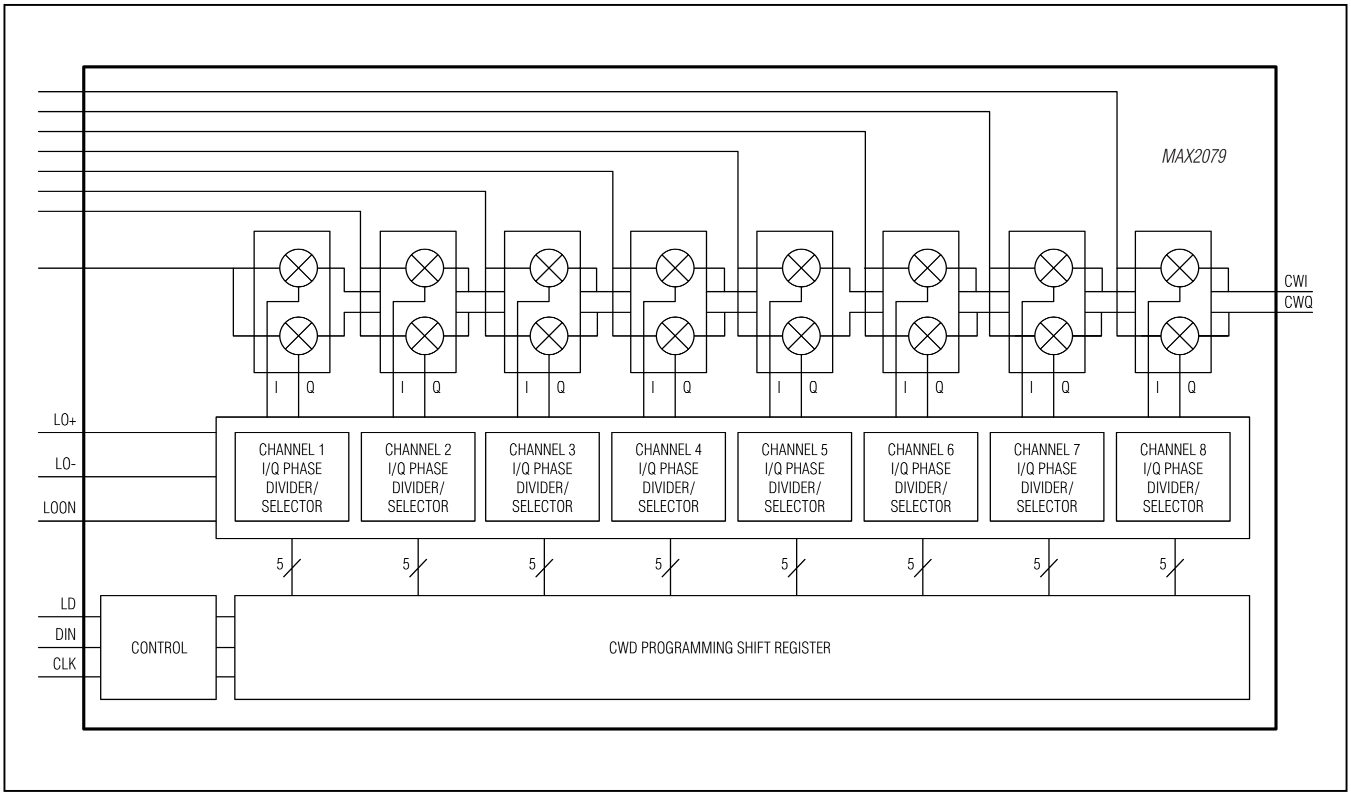


Figure 1. CWD Analog Front-End Beamformer Simplified Block Diagram

VGA and CW Mixer Operation

During normal operation, the device is configured so that either the VGA path is enabled while the mixer array is powered down (VGA mode), or the quadrature mixer array is enabled while the VGA path is powered down (CW mode). For VGA mode, set CWD to a logic-high, and for CW mode, set CWD to a logic-low.

External Voltage Reference

Connect an external, low-noise, +2.5V reference to the V_{REF} pin. Bypass V_{REF} to ground with a 0.1μF capacitor as close as possible to the device. The device noise performance is dependent on the external noise at V_{REF}.

ADC Clock Input

The input clock interface provides for flexibility in the requirements of the clock driver. The device accepts a fully differential clock or single-ended logic-level clock. The device is specified for an input sampling 25MHz to 50MHz frequency range. By default, the internal phase-locked loop (PLL) is configured to accept input clock frequencies from 39MHz to 50MHz. The PLL is programmed through the PLL Sampling Rate register (00h, Table 4). Table 5 details the complete range of PLL sampling frequency settings.

For differential clock operation, connect a differential clock to the CLKIN+ and CLKIN- inputs. The input

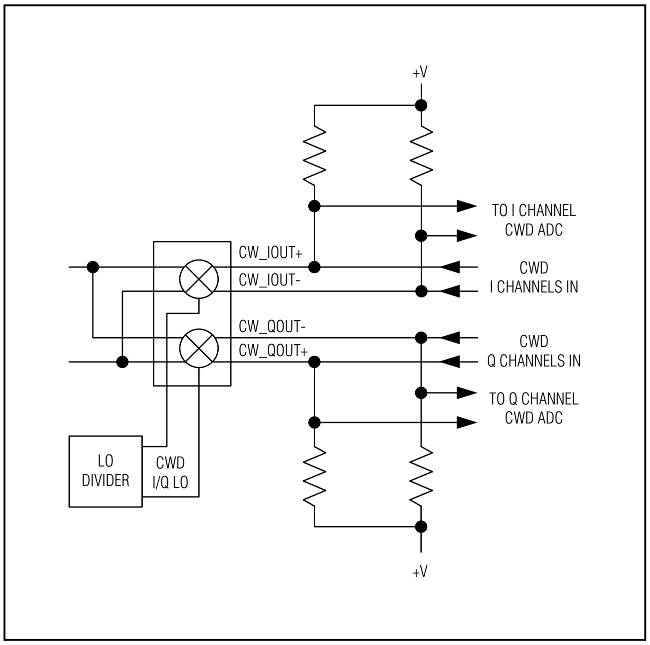


Figure 2. CWD Output Beamforming Example

common mode is established internally to allow for AC-coupling. The self-biased input common-mode voltage defaults to 1.2V. The differential clock signal can also be DC-coupled if the externally established common-mode voltage is constrained to the specified clock input common-mode range of 1V to 1.4V. A differential input termination of 100Ω can be switched in by programming the CLKIN Control register (04h[4], Table 19).

For single-ended operation, connect CLKIN- to GND and drive the CLKIN+ input with a logic-level signal. When the CLKIN- input is grounded (or pulled below the threshold of the clock-mode detection comparator), the differential-to-single-ended conversion stage is disabled and the logic-level inverter path is activated. The input common-mode self-bias is disconnected from CLKIN+, and provides a weak pullup bias to AVDD for CLKIN- during single-ended clock operation.

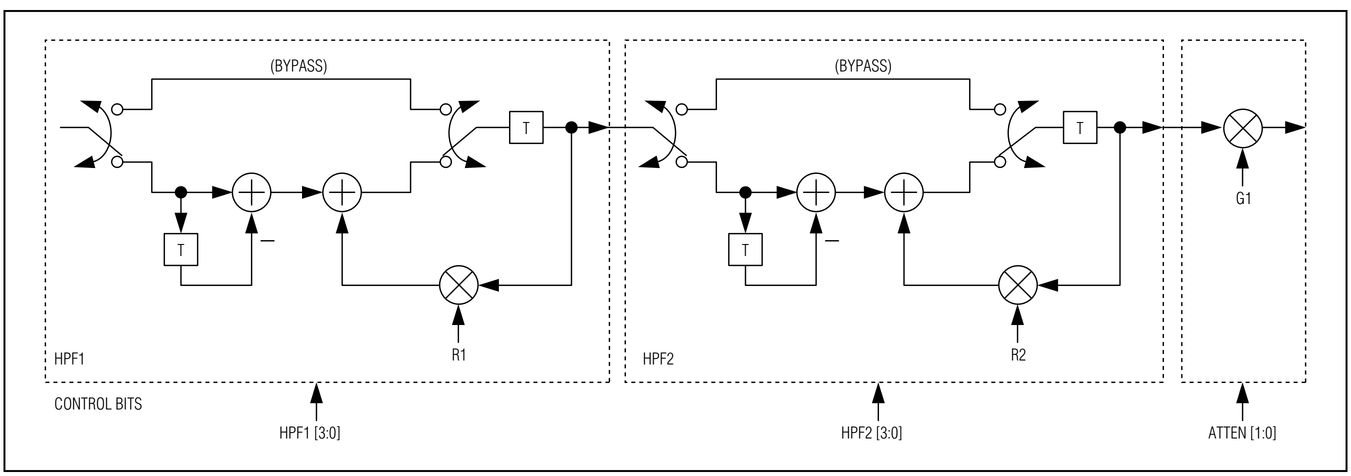


Figure 3. Digital Highpass Filter

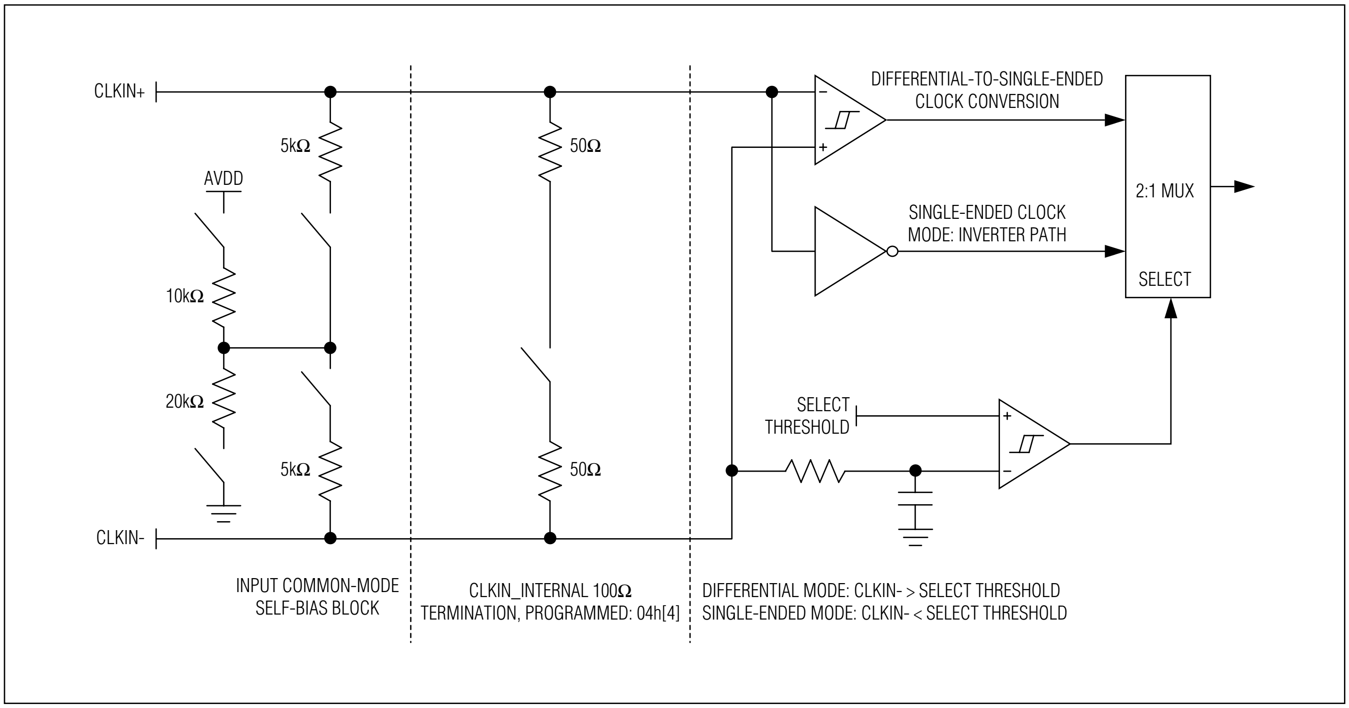


Figure 4. Simplified Clock Input Schematic

Power-Down and Low-Power Mode

The device can also be powered down with the SHDN pin. Set SHDN to +1.8V to place the device in power-down mode. In power-down mode, the device draws a total supply current less than 1µA from the 5V and 3.3V supplies, and less than 0.4mA from the 1.8V supplies. Set SHDN to logic-low for normal operation.

A low-power mode is available to lower the required power for CWD operation. When selected, the complex mixers operate at lower quiescent currents. Note that operation in this mode slightly reduces the dynamic performance of the device. Table 6 shows the logic function of the standard operating modes.

In addition to power-down mode, the device can be placed into a reduced-power Standby or Nap mode, which allows for rapid power-up in VGA mode. Nap mode is accessable by setting the SHDN pin to +1.8V, with the ADC_NAP_SHDN1 and AFE_NAP_SHDN1 registers set to 1 (see Table 6). Nap mode is not meant to be used in conjunction with CWD mode; valid CWD power states are normal CWD low-power and power-down modes. Although no device damage occurs, programming the device for Nap mode and setting the SHDN pin high can create invalid signal outputs in CWD mode.

Programmable, Digital Highpass 2-Pole Filter

Digital Highpass Filter Characteristics

This digital HPF is implemented as the cascade of two identical first-order highpass IIR filter sections. Each section implements the difference equation:

$$y[n] = R \times y[n-1] + x[n] - x[n-1]$$

Where x[n] is the input and y[n] is the output. The highpass 3dB corner frequency is established by the filter coefficient (R). Each section can be independently programmed to one of 10 possible values or placed into bypass mode. The available filter coefficient values and corresponding cutoff frequency are given in Table 1.

Table 1. Digital Filter Cutoff-Frequency Setting

FILTER COEFFICIENT (R)		3dB CUTOFF FREQUENCY ($f_S/2$)	3dB CUTOFF FREQUENCY MHz (f_S = 50Msps)
ONE-FILTER SECTIONS			
54/64	0.843750	0.046294	1.157
55/64	0.859375	0.041943	1.049
56/64	0.875000	0.037535	0.938
57/64	0.890625	0.033069	0.827
58/64	0.906250	0.028544	0.714
59/64	0.921875	0.023956	0.599
60/64	0.937500	0.019303	0.483
61/64	0.953125	0.014584	0.365
62/64	0.968750	0.009796	0.245
63/64	0.984375	0.004935	0.123
TWO-FILTER SECTIONS			
54/64	0.843750	0.069441	1.736
55/64	0.859375	0.062915	1.573
56/64	0.875000	0.056303	1.408
57/64	0.890625	0.049604	1.240
58/64	0.906250	0.042816	1.070
59/64	0.921875	0.035934	0.898
60/64	0.937500	0.028955	0.724
61/64	0.953125	0.021876	0.547
62/64	0.968750	0.014694	0.367
63/64	0.984375	0.007403	0.185

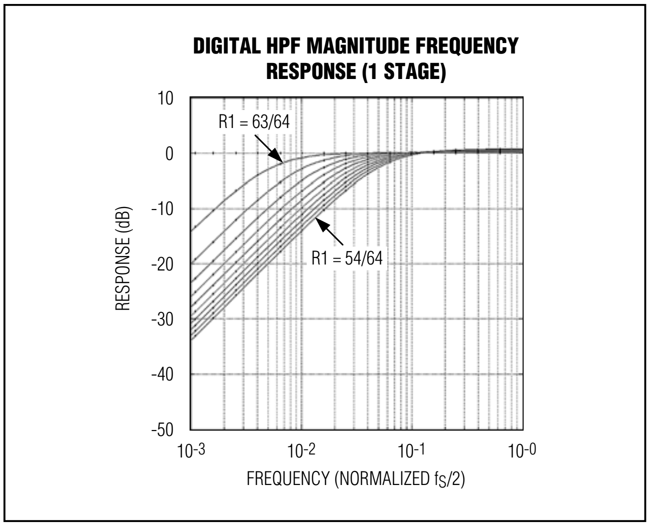


Figure 5. Digital HPF Magnitude Frequency Response (1 Stage)

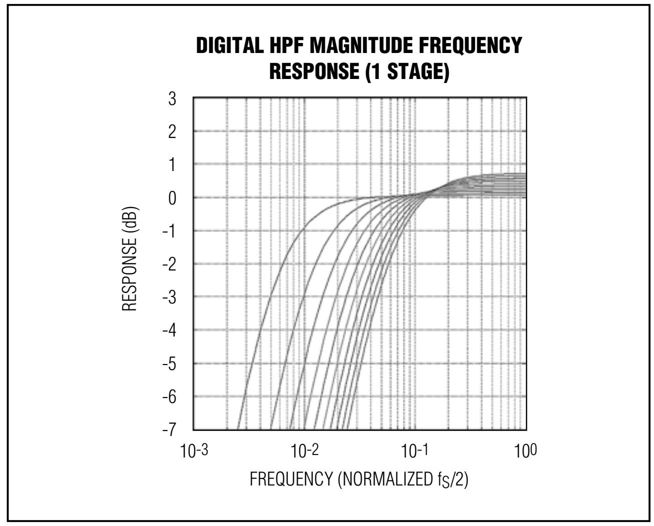


Figure 6. Digital HPF Magnitude Frequency Response (1 Stage)

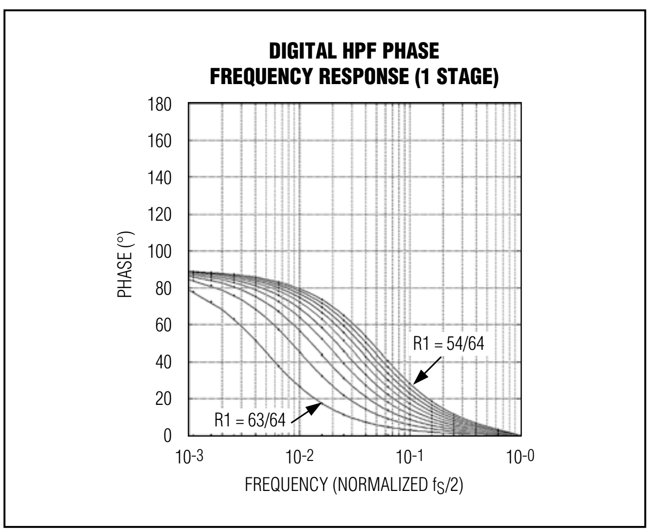


Figure 7. Digital HPF Phase Frequency Response (1 Stage)

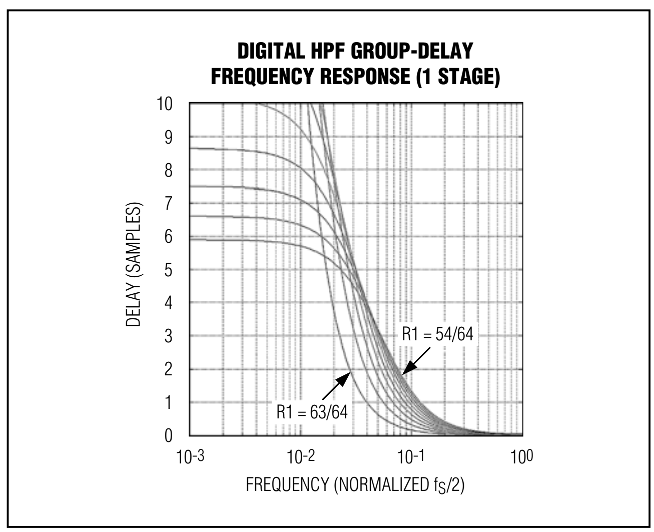


Figure 7a. Digital HPF Group-Delay Frequency Response (1 Stage)

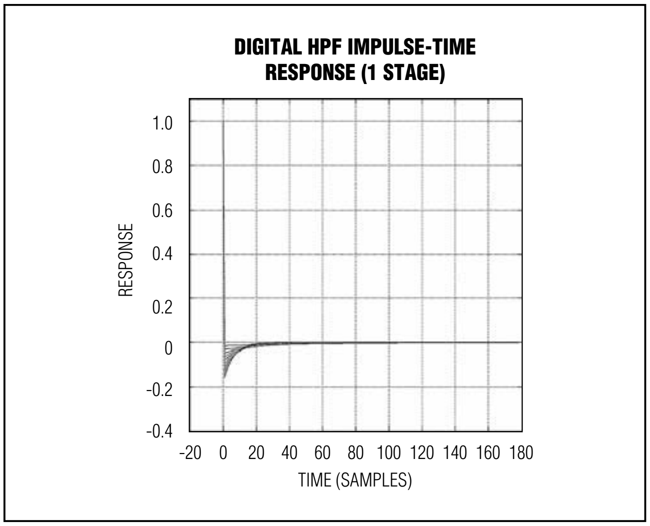


Figure 8. Digital HPF Impulse-Time Response (1 Stage)

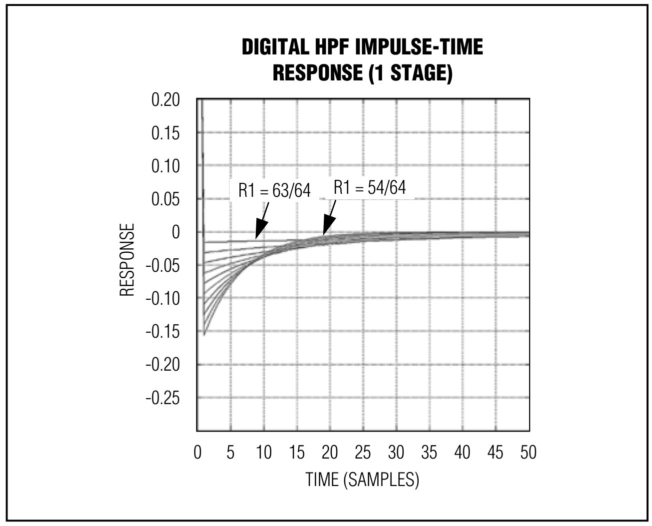


Figure 9. Digital HPF Impulse-Time Response (1 Stage)

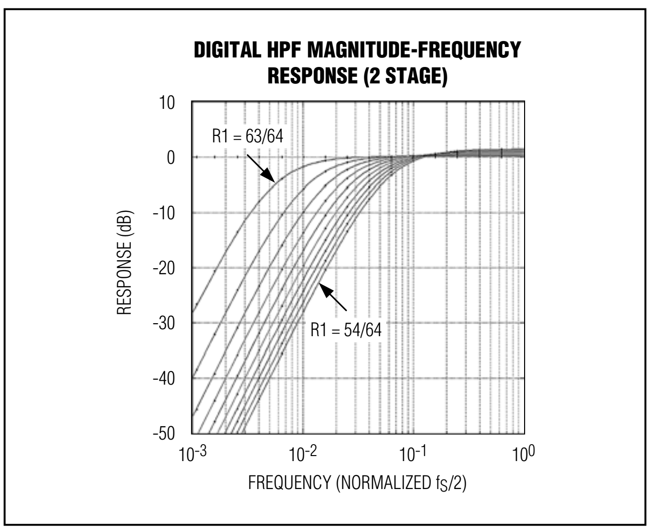


Figure 10. Digital HPF Magnitude-Frequency Response (2 Stage)

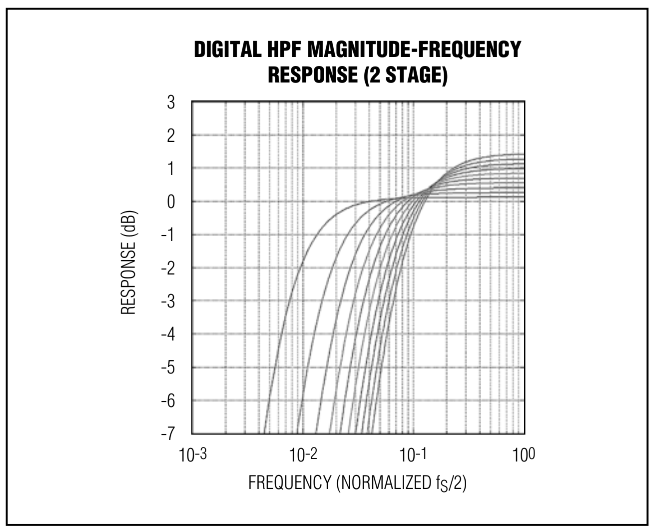


Figure 11. Digital HPF Magnitude-Frequency Response (2 Stage)

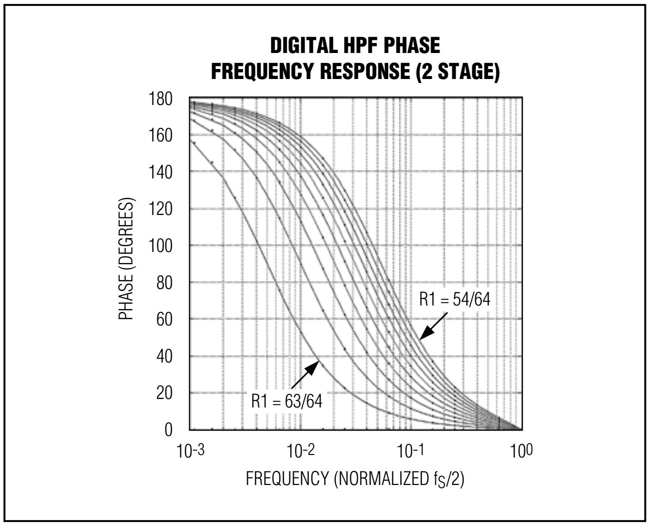


Figure 12. Digital HPF Phase Frequency Response (2 Stage)

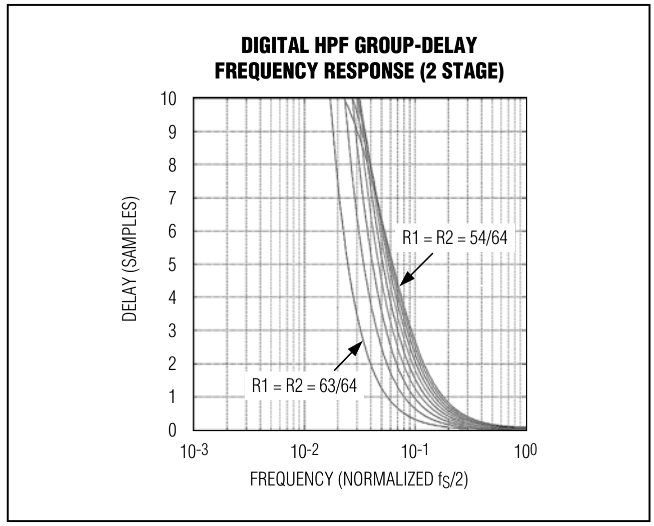


Figure 13. Digital HPF Group-Delay Frequency Response (2 Stage)

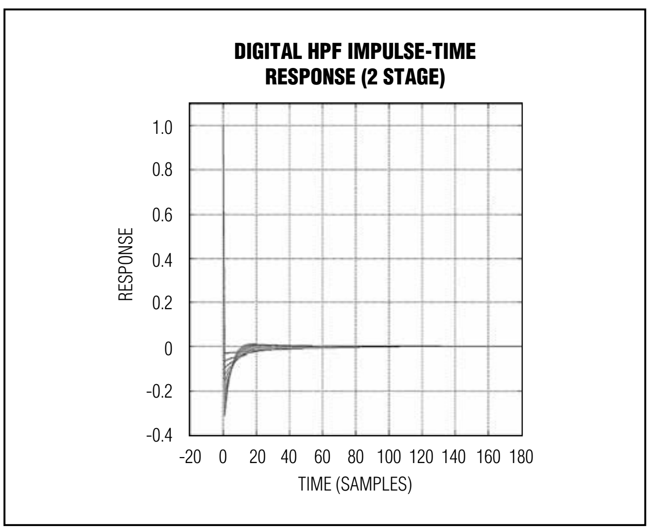


Figure 14. Digital HPF Impulse-Time Response (2 Stage)

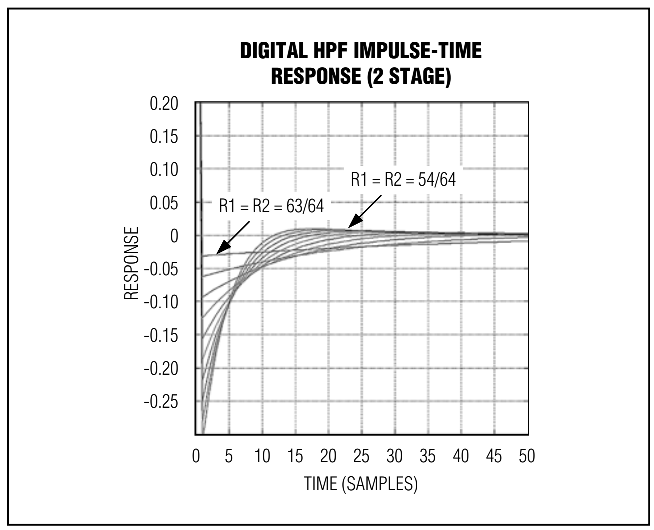


Figure 15. Digital HPF Impulse-Time Response (2 Stage)

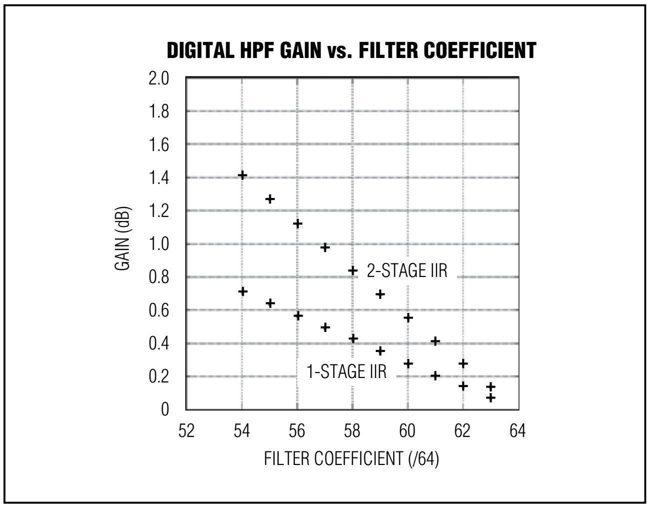


Figure 16. Digital HPF Gain vs. Filter Coefficient

The digital HPF provides a small-signal gain that depends on the filter coefficient. This effectively reduces slightly the full-scale input range of the ADC. A plot of filter gain vs. filter coefficient is shown in Figure 16. A coarse digital multiplier is incorporated at the output of the filter to provide partial compensation of the digital filter gain.

Table 2 provides the recommended gain-compensation settings for different filter cutoff-frequency settings.

Table 2. Gain-Compensation Settings for Different Filter Cutoff-Frequency Settings

R	FILTER MODE	POLES	f_{3dB} (f_S/2)	GAIN	GAIN (dB)	GAIN COMP (dB)	OVERALL GAIN (dB)
N/A	Bypass	N/A	N/A	1	0	0	0
63/64	Filter	1	0.004935	1	0.0681	0	0.0681
62/64	Filter	1	0.009796	1	0.1368	0	0.1368
61/64	Filter	1	0.014584	1	0.206	0	0.206
60/64	Filter	1	0.019303	1	0.2758	0	0.2758
59/64	Filter	1	0.023956	1	0.3461	0	0.3461
58/64	Filter	1	0.028544	15/16	0.417	-0.5606	-0.1436
57/64	Filter	1	0.033069	15/16	0.4885	-0.5606	-0.0721
56/64	Filter	1	0.037535	15/16	0.5606	-0.5606	0
55/64	Filter	1	0.041943	15/16	0.6333	-0.5606	0.0727
54/64	Filter	1	0.046294	15/16	0.7066	-0.5606	0.146
63/64	Filter	2	0.007403	1	0.1362	0	0.1362
62/64	Filter	2	0.014694	1	0.2736	0	0.2736
61/64	Filter	2	0.021876	15/16	0.412	-0.5606	-0.1486
60/64*	Filter	2	0.028955	15/16	0.5515	-0.5606	-0.0091
59/64	Filter	2	0.035934	15/16	0.6922	-0.5606	0.1316
58/64	Filter	2	0.042816	15/16	0.834	-0.5606	0.2734
57/64	Filter	2	0.049604	7/8	0.977	-1.1598	-0.1828
56/64	Filter	2	0.056303	7/8	1.1211	-1.1598	-0.0387
55/64	Filter	2	0.062915	7/8	1.2665	-1.1598	0.1067
54/64	Filter	2	0.069441	7/8	1.4131	-1.1598	0.2533

**Parts are factory trimmed with this setting. Programming can be changed.*

System Timing Requirements

Figure 17 shows the relationship between the analog inputs, input clock, frame-alignment output, serial-clock output, and serial-data outputs. The differential ADC input signal is sampled on the rising edge of the applied clock signal (CLKIN+, CLKIN-), and the resulting data appears at the digital outputs 10.5 clock cycles later. Figure 18 provides a detailed, two-conversion timing diagram of the relationship between inputs and outputs.

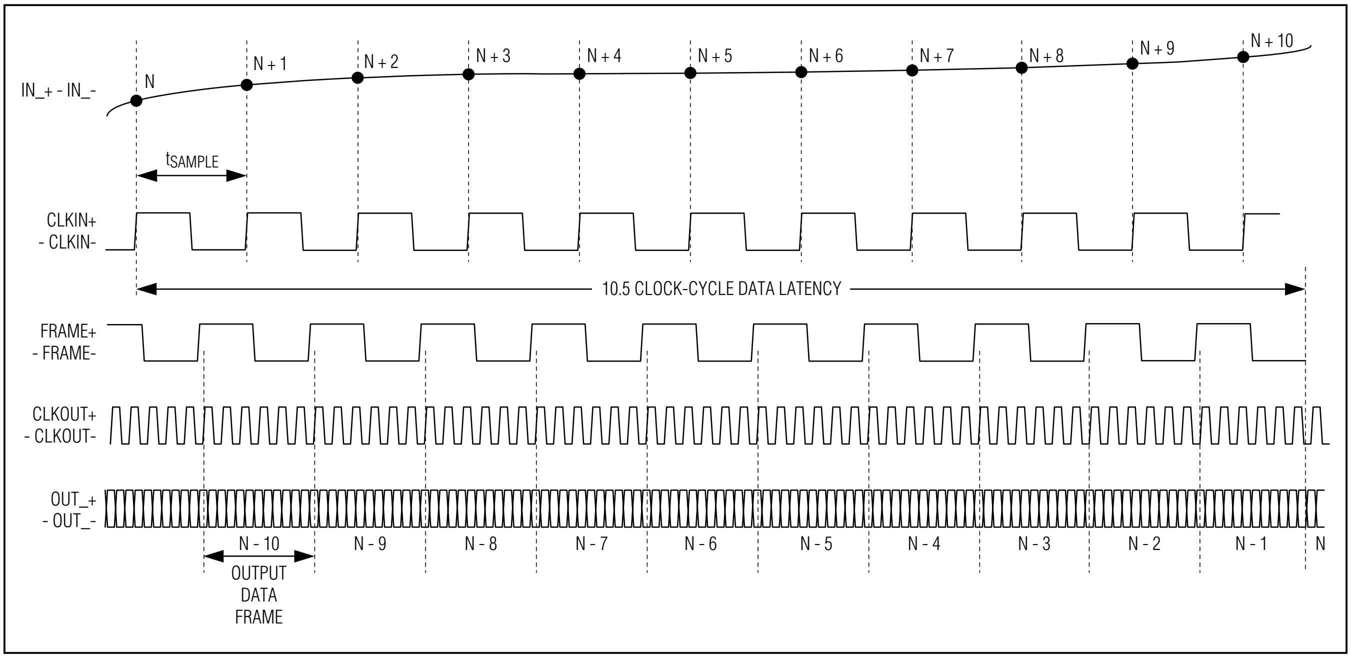


Figure 17. ADC Timing (Overall)

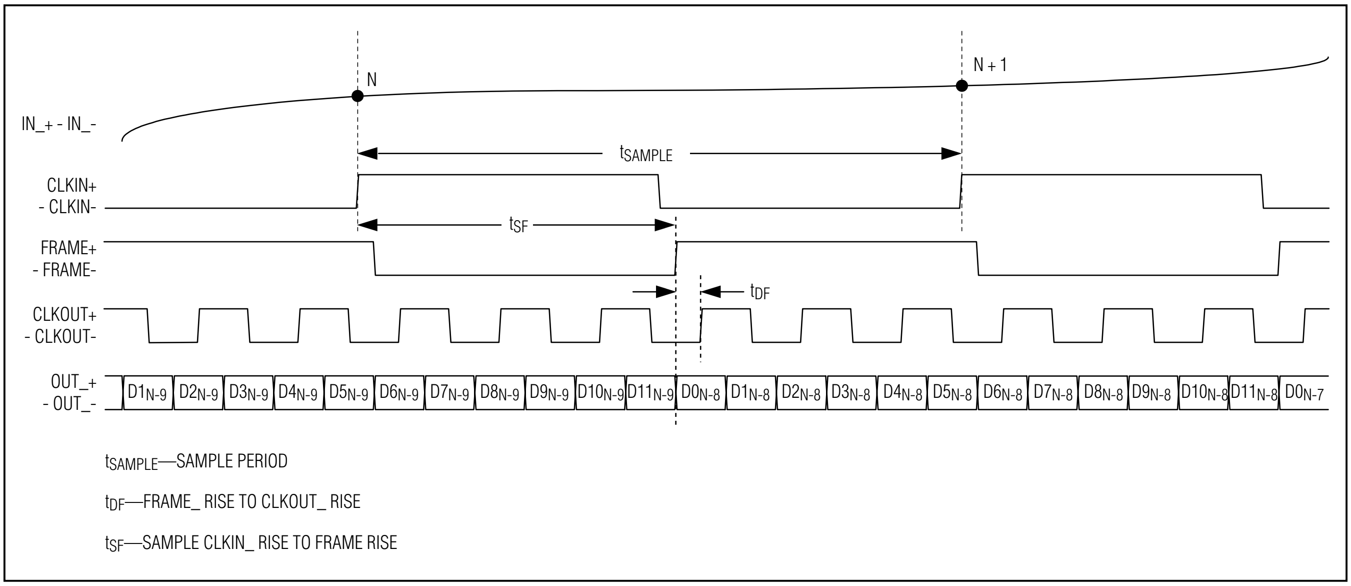


Figure 18. ADC Timing (Detail)

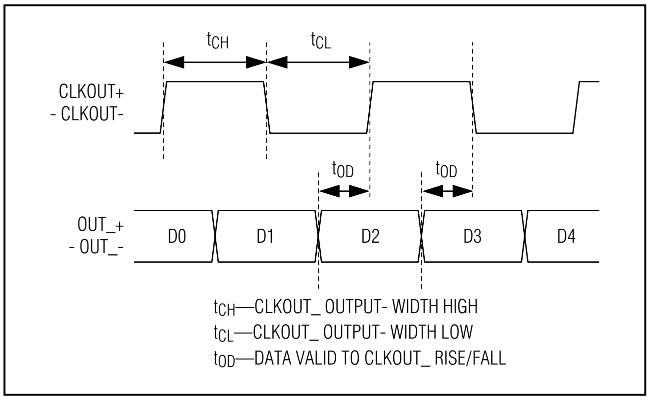


Figure 19. Serial Output Detailed Timing Diagram

Clock Output (CLKOUT+, CLKOUT-)

The ADC provides a differential clock output that consists of CLKOUT+ and CLKOUT-. As shown in Figure 19, the serial-output data is clocked out of the device on both edges of the clock output. The frequency of the output clock is six times (6x) the frequency of the input clock. The Output Data Format and Test Pattern/Digital HPF Select register (01h) allows the phase of the clock output to be adjusted relative to the output data frame (Table 7, Figure 21).

Frame-Alignment Output (FRAME+, FRAME-)

The ADC provides a differential frame-alignment signal that consists of FRAME+ and FRAME-. As shown in Figure 18, the rising edge of the frame-alignment signal corresponds to the first bit (D0) of the 12-bit serial-data stream. The frequency of the frame-alignment signal is identical to the frequency of the input clock; however, the duty cycle varies depending on the input clock frequency.

Serial-Output Data (OUT_+, OUT_-)

The ADC provides conversion results through individual differential outputs consisting of OUT_+ and OUT_-. The results are valid 10.5 input clock cycles after a sample is taken. As shown in Figure 19, the output data is clocked out on both edges of the output clock, LSB (D0) first (by default). Figure 18 displays the detailed serial-output timing diagram.

Differential LVDS Digital Outputs

The ADC features programmable, fully differential LVDS digital outputs. By default, the 12-bit data output is transmitted LSB first, in offset binary format. The Output Data Format and Test Pattern/Digital HPF Select register (01h, Table 7) allows customization of the output bit order and data format. The output bit order can be reconfigured to transmit MSB first, and the output data format can be changed to two's complement. Table 8 contains full output data configuration details.

The LVDS outputs feature flexible programming options. First, the output common-mode voltage can be programmed from 0.6V to 1.2V (default) in 200mV steps (Table 15). Use the LVDS Output Driver Level register (02h, Table 11) to adjust the output common-mode voltage.

The LVDS output driver current is also fully programmable through the LVDS Output Driver Management register (03h, Table 16). By default, the output driver current is set to 3.5mA. The output driver current can be adjusted from 0.5mA to 7.5mA in 0.5mA steps (Table 17).

The LVDS output drivers also feature optional internal terminations that can be enabled and adjusted by the LVDS Output Driver Management register (03h, Table 16). By default, the internal output driver termination is disabled. See Table 18 for all possible configurations.

Output Driver Level Tests

The LVDS outputs (data, clock, and frame) can be configured to static logic-level test states through the LVDS Output Driver Level register (02h, Table 11). The complete list of settings for the static logic-level test states can be found in Tables 12, 13, and 14.

Data Output Test Patterns

The LVDS data outputs can be configured to output several different, recognizable test patterns. Test patterns are enabled and selected using the Output Data Format and Test Pattern/Digital HPF Select register (01h, Table 7). A complete list of test pattern options are listed in Table 9, and custom test pattern details can be found in the Custom Test Pattern registers (07h, 08h, 09h) section (including Tables 24, 27, and 28).

Power Management

The SHDN input is used to toggle between two power-management states. Power state 0 corresponds to SHDN = 0, while power state 1 corresponds to SHDN = 1. The PLL Sampling Rate and Power Management register (00h) and the Channel Power Management registers (05h and 06h) fully define each power-management state. By default, SHDN = 1 shuts down the device, and SHDN = 0 returns the ADCs to full-power operation. Use of the SHDN input is not required for power management.

For either state of SHDN, complete power-management flexibility is provided, including individual ADC channel power-management control, as well as the option of which reduced power-mode to utilize in each power state. The reduced-power modes available are sleep mode and nap mode. The device cannot enter either of these states unless no ADC channels are active in the current power state (Table 6).

In nap mode, the reference, duty-cycle equalizer, and clock-multiplier PLL circuits remain active for rapid wake-up time. In nap mode, the externally applied clock signal must remain active for the duty-cycle equalizer and PLL to remain locked. Typical wake-up time from nap mode is 2µs.

In sleep mode, all circuits are turned off except for the bandgap voltage-generation circuit. All registers retain previously programmed values during sleep mode. Typical wake-up time from sleep mode is 2ms (typ).

Power-On and Reset

The user-programmable register default settings and other factory-programmed settings are stored in a non-volatile memory. Upon device power-up, these values are loaded into the control registers. The operation occurs after the application of a valid supply voltage to AVDD and OVDD, and the presence of an input clock signal. The user-programmed register values are retained as long as the AVDD and OVDD voltages are applied.

A reset condition overwrites all user-programmed registers with the factory-default values. The reset condition occurs on power-up and can be initiated while powered with a software write command (write 5Ah) through the serial-port interface to the Special Function register (10h). The reset time is proportional to the ADC clock period and requires 415µs at 50Msps.

Power-Down and Low-Power (Nap) Mode and Channel Selection

The SHDN pin is a toggle switch between any two power-management states. In most cases, the SHDN = 0 state is on, and the SHDN = 1 state is off. However, complete flexibility is provided, allowing the user to toggle between active and nap, active and sleep, etc. Nap mode is defined as a reduced-power state with rapid wake-up time on the order of 2µs. Sleep mode is a very-low-power mode (~1mW) with a much longer wake-up time on the order of 2ms. The serial port and programmable registers remain active during nap and sleep modes.

CHn_ON_SHDN0 n = [1:8]

1 Channel n is on when the SHDN pin is low.
0 Channel n is off when the SHDN pin is low.

CHn_ON_SHDN1 n = [1:8]

1 Channel n is on when the SHDN pin is high.
0 Channel n is off when the SHDN pin is high.

ADC_NAP_SHDN0

1 ADC in nap mode when all channels are off, or the CWD pin is high and the SHDN pin is low.
0 ADC in sleep mode when all channels are off, or the CWD pin is high and the SHDN pin is low.

ADC_NAP_SHDN1

1 ADC in nap mode when all channels are off, or the CWD pin is high and the SHDN pin is high.
0 ADC in sleep mode when all channels are off, or the CWD pin is high and the SHDN pin is high.

AFE_NAP_SHDN0

1 AFE in nap mode when all channels are off and the SHDN pin is low.
0 AFE in sleep mode when all channels are off and the SHDN pin is low.

AFE_NAP_SHDN1

1 AFE in nap mode when all channels are off and the SHDN pin is high.
0 AFE in sleep mode when all channels are off and the SHDN pin is high.

3-Wire Serial Peripheral Interface (SPI)

The ADC operates as a slave device that sends and receives data through a 3-wire SPI interface. A master device must initiate all data transfers to and from the device. The device uses an active-low SPI chip-select input ($\overline{CS}$) to enable communication with timing controlled through the externally generated SPI clock input (SCLK). All data is sent and received through the bidirectional SPI data line (SDIO). The device has 16 user-programmable control registers and one special-function register, which are accessed and programmed through this interface.

SPI Communication Format

Figure 20 shows an ADC SPI communication cycle. All SPI communication cycles are made up of 2 bytes of data on SDIO and require 16 clock cycles on SCLK to be completed. To initiate an SPI read or write communication cycle, $\overline{CS}$ must first transition from a logic-high to a logic-low state. While $\overline{CS}$ remains low, serial data is clocked in from SDIO on rising edges of SCLK, and clocked out (for a read) on the falling edges of SCLK. When $\overline{CS}$ is high, the device does not respond to SCLK transitions, and no data is read from or written to SDIO. $\overline{CS}$ must transition back to logic-high after each read/write cycle is completed.

The first byte transmitted on SDIO is always provided by the master. The ADC (slave device) clocks in the data from SDIO on each rising edge of SCLK. The first bit received selects whether the communication cycle is a read or a write. Logic 1 selects a read cycle, while logic 0 selects a write cycle. The next 7 bits (MSB first) are the register address for the read or write cycle. The address can indicate any of the 16 user-programmable control registers (00h to 0Fh), or the special-function register (10h, write only). Attempting to read/write with any other address has no effect (Table 3).

The second byte on SDIO is sent to the ADC in the case of a write, or received from the ADC in the case of a read. For a write command, the device continues to clock in the data on SDIO on each rising edge of SCLK. In the case of a read command, the device writes data to SDIO on each falling edge of SCLK. The data byte is transmitted and received MSB first in both cases. The detailed SPI timing requirements are shown in Figure 20.

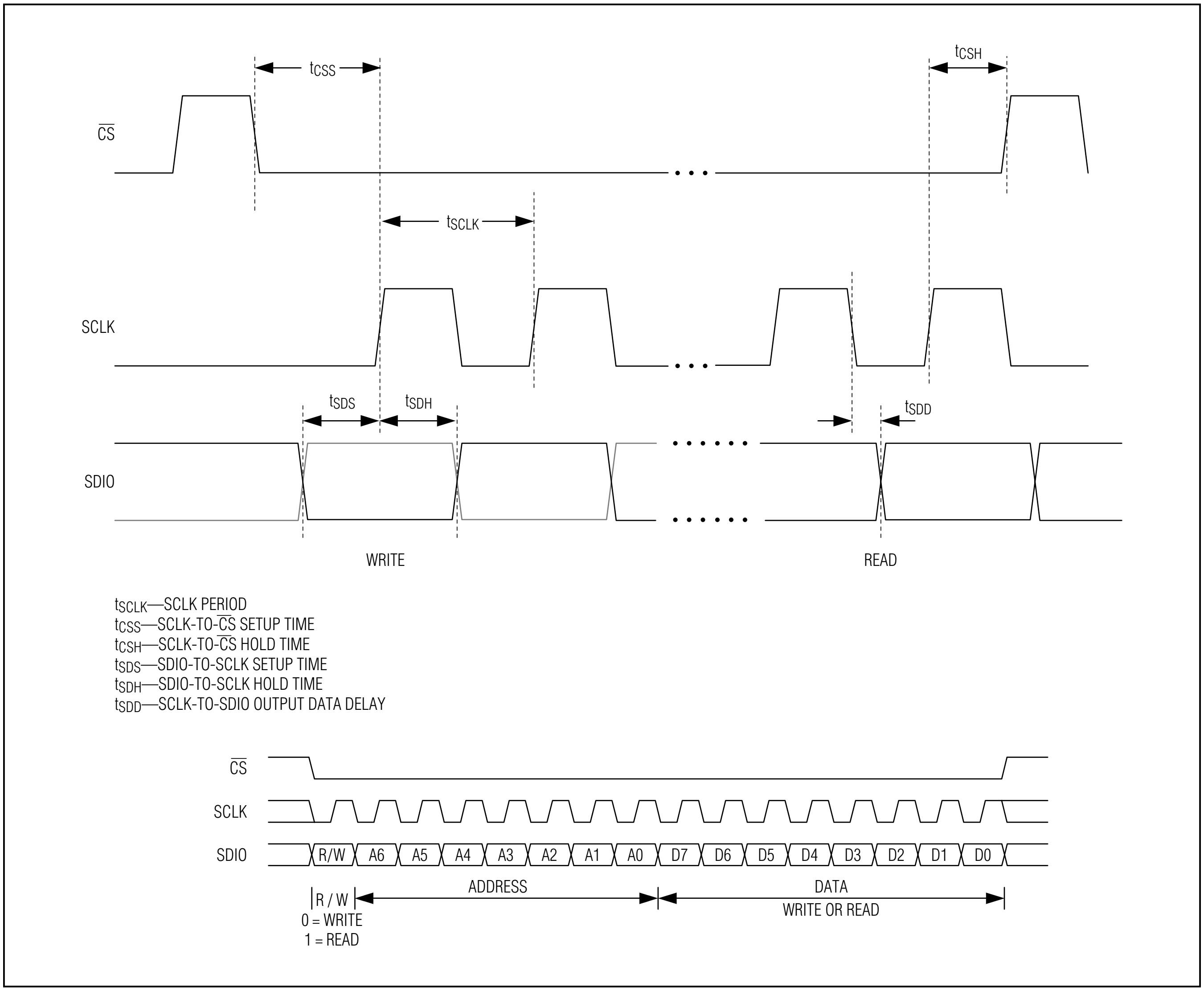


Figure 20. SPI Timing Diagram

Table 3. User-Programmable ADC Control Registers

ADDRESS	READ/WRITE	POR STATE	FUNCTION
00h	R/W	0001-0001	PLL Sampling Rate and Power Management
01h	R/W	0000-0000	Output Data Format and Test Pattern/Digital HPF Select
02h	R/W	0000-0000	LVDS Output Driver Level
03h	R/W	0000-0000	LVDS Output Driver Management
04h	R/W	0000-0000	ADC CLKIN Control
05h	R/W	1111-1111	Channel Power Management: SHDN0
06h	R/W	0000-0000	Channel Power Management: SHDN1
07h	R/W	0100-0100	Digital HPF 1 and 2 -3dB Cutoff/Custom Test Patterns 1
08h	R/W	0101-0110	Digital HPF 1 and Attentuation/Custom Test Patterns 2
09h	R/W	0101-1010	Custom Test Patterns 2 and 1 (4msbs)
0Ah	R/W	0101-1100	AFE Settings
0Bh	R/W	0000-0000	CW Beamformer 1
0Ch	R/W	0000-0000	CW Beamformer 2
0Dh	R/W	0000-0000	CW Beamformer 3
0Eh	R/W	0000-0000	CW Beamformer 4
0Fh	R/W	0000-0000	CW Beamformer 5
10h	R/W	N/A	Special Function

Table 4. PLL Sampling Rate and Power Management (00h)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
—	PLL[2:0]			AFE_NAP_SHDN1	AFE_NAP_SHDN0	ADC_NAP_SHDN1	ADC_NAP_SHDN0

Table 5. PLL Frequency-Control Settings (00h[6:4])

CLOCK MULTIPLIER SETTING			MINIMUM SAMPLING FREQUENCY (MHz)	MAXIMUM SAMPLING FREQUENCY (MHz)
PLL[2]	PLL[1]	PLL[0]		
0	0	0	Not used	
0	0	1	39	50
0	1	0	28.5	39
0	1	1	25	28.8
1	X	X	Not used	

X = Don't care.

Table 6. Power-Management Programming

PINS		REGISTERS						DESCRIPTION
SHDN	CWD	CHn_ON_SHDN0 n = [1:8]	CHn_ON_SHDN1 n = [1:8]	ADC_NAP_SHDN0	ADC_NAP_SHDN1	AFE_NAP_SHDN0	AFE_NAP_SHDN1	
DEFAULT REGISTER MODES								
0	0	11111111	00000000	0	1	0	1	8 channels active (VGA mode)
0	1	11111111	00000000	0	1	0	1	CW Doppler mode (ADC in nap mode)
1	0	11111111	00000000	0	1	0	1	Nap mode (ADC and AFE)
1	1	11111111	00000000	0	1	0	1	CW Doppler mode (ADC in nap mode)
PROGRAMMED REGISTER MODES								
0	0	1XXXXXXX X1XXXXXX XX1XXXXX XXX1XXXX XXXX1XXX XXXXX1XX XXXXXX1X XXXXXXX1	XXXXXXXX	X	X	X	X	1 or more channels active (VGA mode)
0	0	00000000	XXXXXXXX	0	X	0	X	Sleep mode (ADC and AFE)
0	0	00000000	XXXXXXXX	0	X	1	X	ADC sleep/AFE nap
0	0	00000000	XXXXXXXX	1	X	0	X	ADC nap/AFE sleep
0	0	00000000	XXXXXXXX	1	X	1	X	Nap mode (ADC and AFE)
0	1	XXXXXXXX	XXXXXXXX	0	X	X	X	CW Doppler mode (ADC in sleep mode)
0	1	XXXXXXXX	XXXXXXXX	1	X	X	X	CW Doppler mode (ADC in nap mode)
1	0	XXXXXXXX	1XXXXXXX X1XXXXXX XX1XXXXX XXX1XXXX XXXX1XXX XXXXX1XX XXXXXX1X XXXXXXX1	X	X	X	X	1 or more channels active (VGA mode)
1	0	XXXXXXXX	00000000	X	0	X	0	Sleep mode (ADC and AFE)
1	0	XXXXXXXX	00000000	X	0	X	1	ADC sleep/AFE nap
1	0	XXXXXXXX	00000000	X	1	X	0	ADC nap/AFE sleep
1	0	XXXXXXXX	00000000	X	1	X	1	Nap mode (ADC and AFE)
1	1	XXXXXXXX	XXXXXXXX	X	0	X	X	CW Doppler mode (ADC in sleep mode)
1	1	XXXXXXXX	XXXXXXXX	X	1	X	X	CW Doppler mode (ADC in nap mode)

X = Don't care.

Table 7. Output Data Format and Test Pattern/Digital HPF Select (01h)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TEST_PATTERN[2:0]			TEST_DATA	CLKOUT_PHASE[1:0]		DATA_FORMAT	BIT_ORDER

Table 8. LVDS Output Data Format Programming

DATA_FORMAT	BIT_ORDER	LVDS OUTPUT DATA FORMAT
0	0	Binary, LSB first (default)
0	1	Binary, MSB first
1	0	Two's complement, LSB first
1	1	Two's complement, MSB first

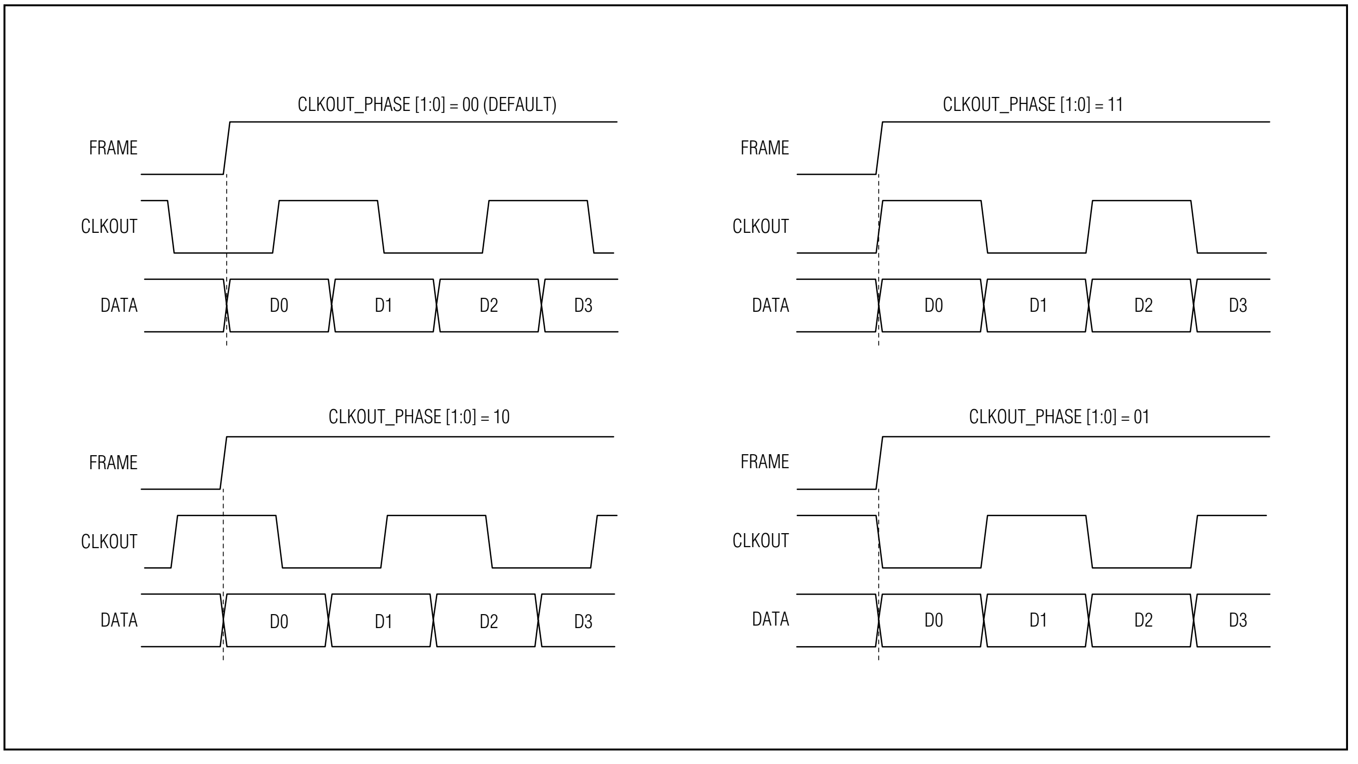


Figure 21. Output Clock Phase

Table 9. Test Pattern Programming and Digital Highpass Filter Selection

TEST_DATA	TEST_PATTERN[2:0]			TEST PATTERN FORMAT
0	X	X	X	Disabled, normal operation with digital HPF selected (default)
1	0	0	0	Data skew (010101010101), repeats every frame
1	0	0	1	Data sync (111111000000), repeats every frame
1	0	1	0	Custom test pattern, repeats every 2 frames
1	0	1	1	Ramping pattern from 0 to 4095 (repeats)
1	1	0	0	Pseudorandom data pattern, short sequence (2^9)
1	1	0	1	Pseudorandom data pattern, long sequence (2^{23})
1	1	1	0	Not used
1	1	1	1	Not used

X = Don't care.

Custom Test Pattern

When custom test pattern is selected (TEST_PATTERN[2:0] = 010), the output alternates between BITS_CUSTOM1[11:0] and BITS_CUSTOM2[11:0]. If a single repeating word is desired, program BITS_CUSTOM2[11:0] to the same value as BITS_CUSTOM1[11:0].

Table 10. Pseudorandom Data Test Pattern

(When custom test pattern is selected (TEST_PATTERN[2:0] = 100) the output is a short (2^9) PN sequence. A long (2^{23}) sequence output is provided when TEST_PATTERN[2:0] = 101.)

SEQUENCE	INITIAL VALUE	FIRST 3 SAMPLES
Short (2^9)	0x0df	0xdf9, 0x353, 0x301
Long (2^{23})	0x29b80a	0x591, 0xfd7, 0x0a3

Table 11. LVDS Output Driver Level (02h)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
LVDS_CM[1:0]		TEST_FRAME_LEVEL[1:0]		TEST_CLKOUT_LEVEL[1:0]		TEST_DATA_LEVEL[1:0]	

Table 12. Test Data (OUT_) Level Programming

TEST_DATA_LEVEL[1:0]		DATA (OUT_) OUTPUT
X	0	Normal data output
0	1	Output low (static)
1	1	Output high (static)

X = Don't care.

Table 13. Test CLKOUT_ Level Programming

TEST_CLKOUT_LEVEL[1:0]		CLKOUT_ OUTPUT
X	0	Normal CLKOUT_ output
0	1	Output low (static)
1	1	Output high (static)

X = Don't care.

Table 14. Test FRAME Level Programming

TEST_FRAME_LEVEL[1:0]		FRAME OUTPUT
X	0	Normal FRAME output
0	1	Output low (static)
1	1	Output high (static)

X = Don't care.

Table 15. LVDS Output Common-Mode Voltage Adjustment

LVDS_CM[1:0]		LVDS OUTPUT COMMON-MODE VOLTAGE (V)
0	0	1.2 (default)
0	1	1.0
1	0	0.8
1	1	0.6

Table 16. LVDS Output Driver Management (03h)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
—	LVDS_TERM[2:0]			LVDS_IADJ[3:0]			

Table 17. LVDS Output Drive Current Configuration

(Selectable LVDS drive current fully selectable from 0.5mA to 7.5mA in 0.5mA increments (3.5mA default). Supports ANSI-644 and IEEE 1596.3.)

LVDS_IADJ[3:0]				LVDS CURRENT (mA)
0	0	0	0	3.5mA, 350mV at 100Ω (default)
0	0	0	1	0.5
0	0	1	0	1.0
0	0	1	1	1.5
0	1	0	0	2.0
0	1	0	1	2.5
0	1	1	0	3.0
0	1	1	1	3.5
1	0	0	0	4.0
1	0	0	1	4.5
1	0	1	0	5.0
1	0	1	1	5.5
1	1	0	0	6.0
1	1	0	1	6.5
1	1	1	0	7.0
1	1	1	1	7.5

Table 18. LVDS Output Driver Internal Termination Configuration

LVDS_TERM[2:0]			LVDS INTERNAL TERMINATION (Ω)
0	0	0	—
0	0	1	800
0	1	0	400
0	1	1	267
1	0	0	200
1	0	1	160
1	1	0	133
1	1	1	100

Table 19. CLKIN Termination Control (04h)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
—	—	—	CLKIN_TERM	—	—	—	0

Bit 0

Always program this bit to 0.

Clock Input Termination

CLKIN_TERM = 0: 100Ω not selected.

CLKIN_TERM = 1: Switches in 100Ω across differential clock inputs.

Table 20. Channel Power Management: SHDN0 (05h)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CH8_SHDN0	CH7_SHDN0	CH6_SHDN0	CH5_SHDN0	CH4_SHDN0	CH3_SHDN0	CH2_SHDN0	CH1_SHDN0

Table 21. Channel Power Management: SHDN1 (06h)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CH8_SHDN1	CH7_SHDN1	CH6_SHDN1	CH5_SHDN1	CH4_SHDN1	CH3_SHDN1	CH2_SHDN1	CH1_SHDN1

Table 22. Digital Highpass Filter Control Coefficients (07h; If TEST_DATA 01[4] = 0)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
HPF2[3:0]				HPF1[3:0]			

Table 23. Digital Highpass Filter Configuration

HPF1[3:0], HPF2[3:0]				R1/R2	FILTER MODE
0	0	0	0	N/A	Bypass
0	0	0	1	63/64	Filter; f_{3dB} = 0.004935, f_S/2
0	0	1	0	62/64	Filter; f_{3dB} = 0.009796, f_S/2
0	0	1	1	61/64	Filter; f_{3dB} = 0.014584, f_S/2
0	1	0	0	60/64	Filter; f_{3dB} = 0.019303, f_S/2
0	1	0	1	59/64	Filter; f_{3dB} = 0.023956, f_S/2
0	1	1	0	58/64	Filter; f_{3dB} = 0.028544, f_S/2
0	1	1	1	57/64	Filter; f_{3dB} = 0.033069, f_S/2
1	0	0	0	56/64	Filter; f_{3dB} = 0.037535, f_S/2
1	0	0	1	55/64	Filter; f_{3dB} = 0.041943, f_S/2
1	0	1	0	54/64	Filter; f_{3dB} = 0.046294, f_S/2
1	0	1	1	N/A	Bypass
1	1	0	0	N/A	Bypass
1	1	0	1	N/A	Bypass
1	1	1	0	N/A	Bypass
1	1	1	1	N/A	Bypass

Table 24. Custom Test Pattern 1 (07h; If TEST_DATA 01[4] = 1)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
BITS_CUSTOM1[7:0]							

Table 25. Digital Highpass Filter Attenuation (08h; If TEST_DATA 01[4] = 0)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
—	—	—	—	—	—	ATTEN[1:0]	

Table 26. Digital Highpass Filter Attenuation

ATTEN[1:0]		GAIN	GAIN (dB)
0	0	1	0
0	1	1	0
1	0	15/16	-0.58
1	1	7/8	-1.16

Table 27. Custom Test Pattern 2 (08h; If TEST_DATA 01[4] = 1)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
BITS_CUSTOM2[7:0]							

Table 28. Custom Test Pattern 3 (09h)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
BITS_CUSTOM2[11:8]				BITS_CUSTOM1[11:8]			

Table 29. AFE Settings (0Ah)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
AFE_RIN[0:2]			AFE_LNA_GAIN	AFE_BW[0:1]		CWD_POWER_MODE	AFE_OCLAMP

Table 30. AFE Input Impedance and LNA Gain Control

AFE_LNA_GAIN	AFE_RIN[0:2]			INPUT RESISTANCE (Ω)	LNA GAIN (dB)
0	0	0	0	100	12.5
0	1	0	0	200	12.5
0	0	1	0	400	12.5
0	1	1	0	2000	12.5
0	X	X	1	External R	12.5
1	0	0	0	50	18.5
1	1	0	0	100	18.5
1	0	1	0	200	18.5
1	1	1	0	1000	18.5
1	X	X	1	External R	18.5

X = Don't care.

Table 31. AFE Filter Bandwidth Control

AFE_BW[0:1]		BANDWIDTH (MHz)
0	0	9
0	1	10
1	0	15
1	1	18

Table 32. CWD Power Mode

CWD_POWER_MODE	CWD POWER MODE
0	Full power (default, nominal)
1	Low power

Table 33. VGA Output Clamp Control

AFE_OCLAMP	VGA OUTPUT CLAMP
0	No clamp (default, nominal)
1	Clamp active

Table 34. CW Beamformer 1 (0Bh)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CW_PHASE_CH2[1:3]			CW_SHDN_CH1	CW_PHASE_CH1[0:3]			

Table 35. CW Beamformer 2 (0Ch)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CW_PHASE_CH4[3]	CW_SHDN_CH3	CW_PHASE_CH3[0:3]				CW_SHDN_CH2	CW_PHASE_CH2[0]

Table 36. CW Beamformer 3 (0Dh)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CW_PHASE_CH5[0:3]				CW_SHDN_CH4	CW_PHASE_CH4[0:2]		

Table 37. CW Beamformer 4 (0Eh)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CW_PHASE_CH7[2:3]		CW_SHDN_CH6	CW_PHASE_CH6[0:3]				CW_SHDN_CH5

Table 38. CW Beamformer 5 (0Fh)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CW_SHDN_CH8	CW_PHASE_CH8[0:3]				CW_SHDN_CH7	CW_PHASE_CH7[0:1]	

CW Doppler Mode Control

CW_SHDN_CHn is set to 0 in normal operation (default). Set it to 1 for power-down channel n when in CW Doppler mode.

Note: The transfer data to AFE procedure described in the *AFE Programming and Data Transfer* section should be performed twice when setting any CW_SHDN_CHn bits from 0 to 1 to enable a CW Doppler channel(s). This procedure only applies to the CW_SHDN_CHn bits; all other bits are transferred to the AFE in a single operation.

Table 39. Degree Change by Each Phase Bit

PH[0]	PH[1]	PH[2]	PH[3]	PHASE
-22.5	-180	-90	-45	Degrees

Table 40. Phase Rotation

CW_PHASE_CHn[0:3]				PHASE (Degrees)
-22.5	-180	-90	-45	
0	0	0	0	0
1	0	0	0	337.5
0	1	0	0	180
1	1	0	0	157.5
0	0	1	0	270
1	0	1	0	247.5
0	1	1	0	90
1	1	1	0	67.5
0	0	0	1	315
1	0	0	1	292.5
0	1	0	1	135
1	1	0	1	112.5
0	0	1	1	225
1	0	1	1	202.5
0	1	1	1	45
1	1	1	1	22.5

Table 41. Special Function Register (10h)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
STATUS7	STATUS6	STATUS5	STATUS4	STATUS3	STATUS2	STATUS1	STATUS0

Table 42. Status Byte (Reads from 10h)

STATUS BIT NO.	READ VALUE	DESCRIPTION
7	0	Reserved
6	0	1 = AFE load in progress; 0 = load complete
5	0 or 1	1 = ROM read in progress
4	0 or 1	1 = ROM read completed, and register data is valid (checksum ok)
3	0	Reserved
2	1	Reserved
1	0 or 1	Reserved
0	0 or 1	1 = Duty-cycle equalizer DLL is locked

Table 43. SPI Commands (Writes to 10h)

(All commands are issued by writing SPI address 10h.)

COMMAND	WRITE DATA	DESCRIPTION
Soft reset	5Ah	Initiates software reset
Transfer data to AFE	AEh	Initiates transfer of data in ADC registers 0Ah to 0Fh to AFE

Soft Reset

Software reset allows the user to reset the part through writes to the serial port. A soft reset can be performed by writing the reset code 5Ah to address 10h. Upon initiation of soft reset, the fuse memory is read and loaded into the SPI registers. See the *3-Wire Serial Peripheral Interface (SPI)* section for further detail. The reset is self-clearing, subsequent serial-port write(s) are not needed to clear the reset condition.

AFE Programming and Data Transfer

The internal analog front-end (AFE) and ADC are programmed through a common serial-port interface. There are 48 user-programmable bits in the ADC that store AFE control information. These bits are written to registers 0Ah to 0Fh in the ADC, and transferred to the AFE shift registers when AEh is written to register 10h. The user must provide at least 50 clock cycles on SCLK after this control word is written to complete the data transfer to the AFE. To verify that the data has been transferred to the AFE, poll address 10h until bit 6 is 0. As a final step, write 00h to address 10h. Changes in registers 0Ah to 0Fh do not take effect in the AFE until this transfer is complete.

CWD Beamformer Programming and Clocking

Programming of the CWD beamformer occurs in the following sequence:

1) During normal CWD mode, the mixer clock (LO+, LO-) is on. LOON is high.
2) Shut off the mixer clock (LO+, LO-) or pull LOON low to start the programming sequence.
3) Write the phase and channel shutdown information into the proper control registers.
4) Transfer the phase information from the control registers to the AFE (see above) and wait for the write to complete. Turn on the mixer clock and set LOON to high to start beamforming (the AFE shift registers can also be written with the mixer clock running and LOON set low). If turning on the mixer clock source, the clock must turn on such that it starts at the beginning of a mixer clock cycle. A narrow glitch on the mixer clock is not acceptable and could cause metastability in the I/Q phase dividers. If using the LOON control to turn on the mixer clock, the LOON signal must be synchronous to the LO clock, and it must meet the minimum setup time specification.

5) To program new CWD phase information, turn off the mixer clock and/or set LOON low and repeat steps 1–5.
6) For switching between VGA and CWD modes without reprogramming the SPI registers (fast-mode switching): When changing from CWD mode to VGA mode, nothing needs to be done to maintain the AFE programming settings. When switching from VGA mode to CWD mode, the user must provide a $\overline{CS}$ pulse after the CWD pin goes high to initialize the CWD beamformer phase registers. This pulse must occur 100ns or more after the rising edge of the CWD pin, and must be at least 80ns in width.

Applications Information

Ultrasound-Specific IMD3 Specification

Unlike typical communications applications, the two input tones are not equal in magnitude for the ultrasound-specific IMD3 two-tone specification. In this measurement, f_1 represents reflections from tissue and f_2 represents reflections from blood. The latter reflections are typically 25dB lower in magnitude. IM3 performance for the device is measured with the smaller tone at -25dBc in order to more accurately resolve the small IM3 products over the thermal noise floor. The IMD3 product of interest (f_1 - (f_2 - f_1)) presents itself as an undesired Doppler error signal in ultrasound applications (see Figure 22).

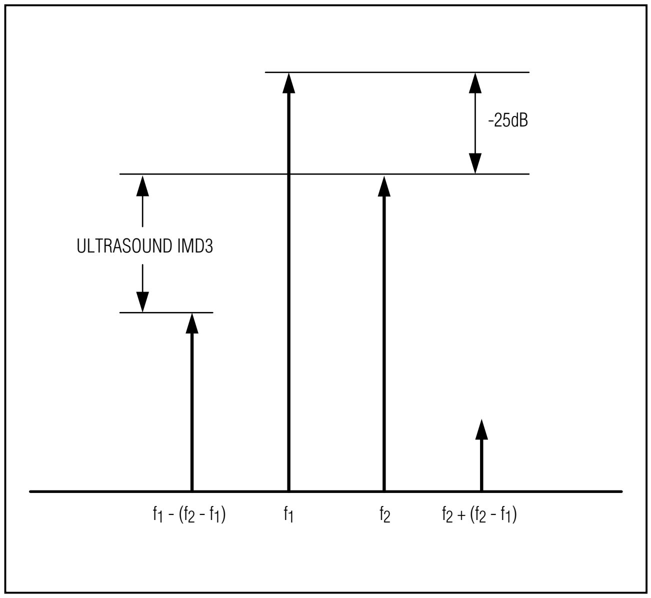
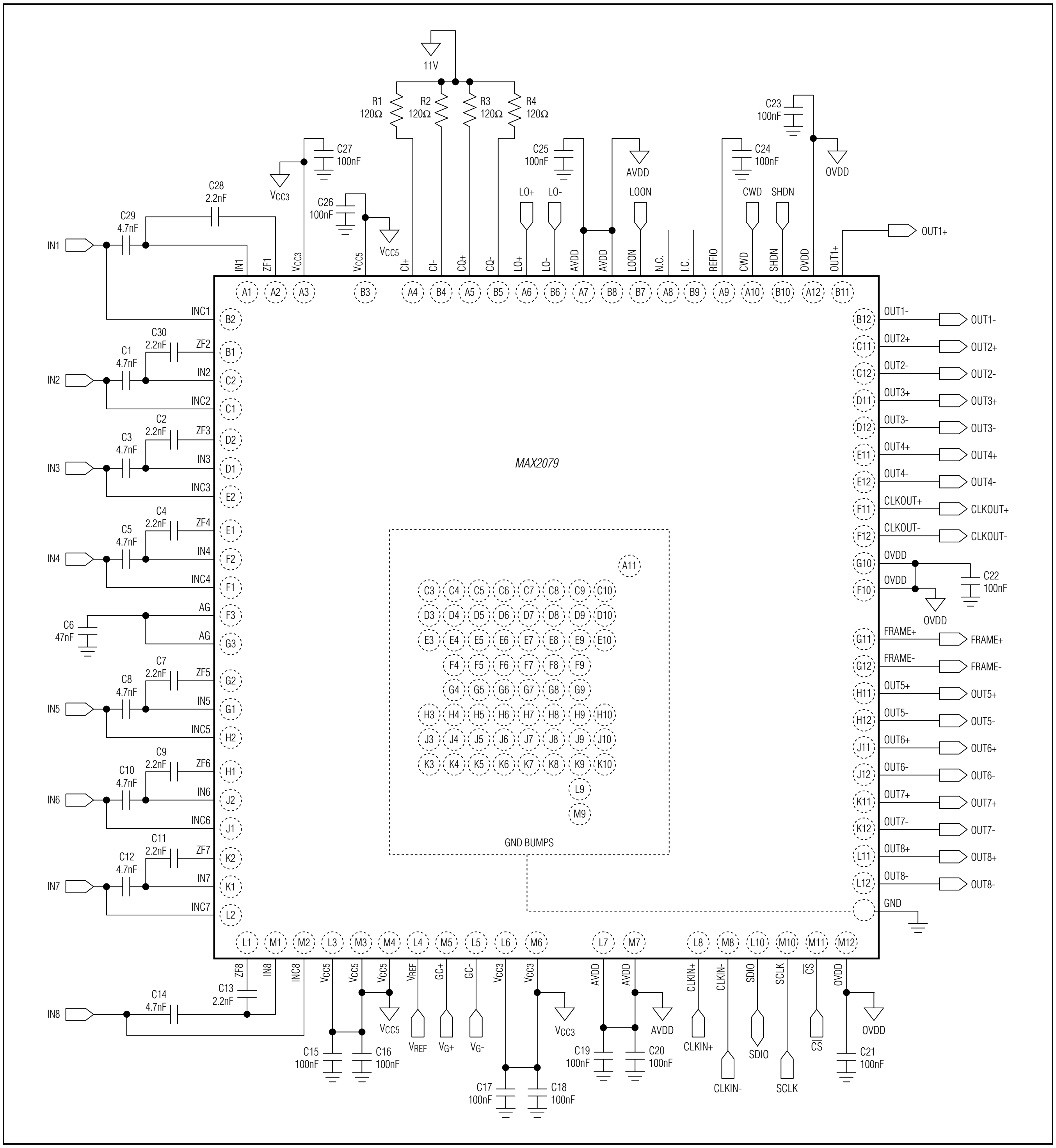


Figure 22. Ultrasound-Specific IMD3

Typical Application Circuit



Chip Information

PROCESS: BiCMOS/CMOS

Ordering Information

PART	TEMP RANGE	BUMP-PACKAGE
MAX2079CXE+	0°C to +70°C	144 CTBGA
MAX2079CXE+T	0°C to +70°C	144 CTBGA

+Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape and reel.

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
144 CTBGA	X14400M+1	21-0492	90-0347

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	8/11	Initial release	—
1	10/12	Fix errors and update *Typical Operating Characteristics*	

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- Поставка сложных, дефицитных, либо снятых с производства позиций;
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- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.

Как с нами связаться

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