

### FEATURES

- 44 V supply maximum rating**
- $V_{SS}$  to  $V_{DD}$  analog signal range**
- Single- or dual-supply specifications**
- Wide supply ranges (10.8 V to 16.5 V)**
- Microprocessor compatible (100 ns  $\overline{WR}$  pulse)**
- Extended plastic temperature range ( $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ )**
- Low leakage (20 pA typical)**
- Low power dissipation (28 mW maximum)**
- Available in PDIP, CERDIP, SOIC, and PLCC packages**
- Superior alternative to DG526 and DG527**

### APPLICATIONS

- Data acquisition systems**
- Communication systems**
- Automatic test equipment**
- Microprocessor controlled systems**

### GENERAL DESCRIPTION

The ADG526A and ADG527A are CMOS monolithic analog multiplexers with 16 single channels and dual 8 channels, respectively. On-chip latches facilitate microprocessor interfacing.

The ADG526A switches one of 16 inputs to a common output, depending on the state of four binary addresses and an enable input. The ADG527A switches one of eight differential inputs to a common differential output, depending on the state of three binary addresses and an enable input. Both devices have TTL and 5 V CMOS logic-compatible digital inputs.

The ADG526A and ADG527A are designed on an enhanced LC<sup>2</sup>MOS process that gives an increased signal capability of  $V_{SS}$  to  $V_{DD}$  and enables operation over a wide range of supply voltages. The devices can comfortably operate anywhere in the 10.8 V to 16.5 V single- or dual-supply range. These multiplexers also feature high switching speeds and low  $R_{ON}$ .

### FUNCTIONAL BLOCK DIAGRAMS

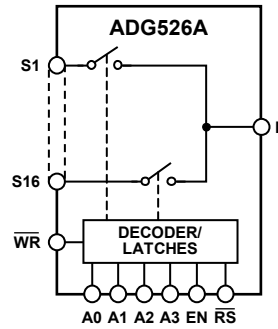


Figure 1. ADG526A

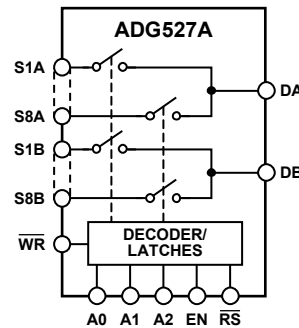


Figure 2. ADG527A

### PRODUCT HIGHLIGHTS

1. Single- or Dual-Supply Specifications with a Wide Tolerance. The devices are specified in the 10.8 V to 16.5 V range for both single and dual supplies.
2. Easily Interfaced. The ADG526A and ADG527A can be easily interfaced with microprocessors. The  $\overline{WR}$  signal latches the state of the address control lines and the enable line. The  $\overline{RS}$  signal clears both the address and enable data in the latches, resulting in no output (all switches off).  $\overline{RS}$  can be tied to the microprocessor reset pin.
3. Extended Signal Range. The enhanced LC<sup>2</sup>MOS processing results in a high breakdown and an increased analog signal range from  $V_{SS}$  to  $V_{DD}$ .
4. Break-Before-Make Switching. Switches are guaranteed break-before-make so that input signals are protected against momentary shorting.
5. Low Leakage. Leakage currents in the range of 20 pA make these multiplexers suitable for high precision circuits.

#### Rev. C

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective owners.

## TABLE OF CONTENTS

|                                |   |  |    |
|--------------------------------|---|--|----|
| Features .....                 | 1 | ESD Caution.....                                   | 7  |
| Applications.....              | 1 | Pin Configurations and Function Descriptions ..... | 8  |
| General Description .....      | 1 | Typical Performance Characteristics .....          | 11 |
| Functional Block Diagrams..... | 1 | Terminology .....                                  | 12 |
| Product Highlights .....       | 1 | Timing.....  | 13 |
| Revision History .....         | 2 | Test Circuits.....                                 | 14 |
| Specifications.....            | 3 | Outline Dimensions .....                           | 17 |
| Dual Supply .....              | 3 | Ordering Guide .....                               | 19 |
| Single Supply .....            | 5 |  |    |
| Absolute Maximum Ratings.....  | 7 |  |    |

## REVISION HISTORY

### 6/08—Rev. B to Rev. C.

|  |           |
|--|-----------|
| Updated Format .....                         | Universal |
| ADG526A LCCC Package Removed .....           | Universal |
| Changes to Features.....                     | 1         |
| Added Applications Section.....              | 1         |
| Changes to Absolute Maximum Ratings .....    | 7         |
| Added Table 4, Renumbered Sequentially ..... | 8         |
| Added Table 5.....                           | 9         |
| Changes to Figure 7 and Figure 8.....        | 11        |
| Updated Outline Dimensions .....             | 17        |
| Changes to Ordering Guide .....              | 19        |

### 2/02—Rev. A to Rev. B.

|  |   |
|--|---|
| Edits to Specifications Table, Dual Supply .....   | 2 |
| Edits to Specifications Table, Single Supply ..... | 3 |
| Edits to Ordering Guide .....                      | 4 |
| Removal of one Pin Configuration and Diagram ..... | 6 |

# SPECIFICATIONS

## DUAL SUPPLY

$V_{DD} = 10.8\text{ V to }16.5\text{ V}$ ,  $V_{SS} = -10.8\text{ V to }-16.5\text{ V}$ , unless otherwise noted.

Table 1.

| Parameter   | ADG526A/ADG527A |                |           |                | ADG526A   |                 | Unit              | Comments  |
|---|-----------------|----------------|-----------|----------------|-----------|-----------------|-------------------|---|
|   | K Version       |                | B Version |                | T Version |                 |                   |   |
|   | 25°C            | -40°C to +85°C | 25°C      | -40°C to +85°C | 25°C      | -55°C to +125°C |                   |   |
| <b>ANALOG SWITCH</b>  |                 |                |           |                |           |                 |                   |   |
| Analog Signal Range   | $V_{SS}$        | $V_{SS}$       | $V_{SS}$  | $V_{SS}$       | $V_{SS}$  | $V_{SS}$        | V min             |   |
|   | $V_{DD}$        | $V_{DD}$       | $V_{DD}$  | $V_{DD}$       | $V_{DD}$  | $V_{DD}$        | V max             |   |
| $R_{ON}$  | 280             |                | 280       |                | 280       |                 | $\Omega$ typ      | $-10\text{ V} \leq V_s \leq +10\text{ V}$ , $I_{DS} = 1\text{ mA}$ ;<br>see Figure 15 |
|   | 450             | 600            | 450       | 600            | 450       | 600             | $\Omega$ max      |   |
|   | 300             | 400            | 300       | 400            |           |                 | $\Omega$ max      | $V_{DD} = +15\text{ V} (\pm 10\%)$ ,<br>$V_{SS} = -15\text{ V} (\pm 10\%)$            |
|   |                 |                |           |                | 300       | 400             | $\Omega$ max      | $V_{DD} = +15\text{ V} (\pm 5\%)$ ,<br>$V_{SS} = -15\text{ V} (\pm 5\%)$              |
| $R_{ON}$ Drift  | 0.6             |                | 0.6       |                | 0.6       |                 | %/°C typ          | $-10\text{ V} \leq V_s \leq +10\text{ V}$ , $I_{DS} = 1\text{ mA}$                    |
| $R_{ON}$ Match  | 5               |                | 5         |                | 5         |                 | % typ             | $-10\text{ V} \leq V_s \leq +10\text{ V}$ , $I_{DS} = 1\text{ mA}$                    |
| $I_s$ (Off), Off Input Leakage                              | 0.02            |                | 0.02      |                | 0.02      |                 | nA typ            | $V_1 = \pm 10\text{ V}$ , $V_2 = \mp 10\text{ V}$ ;<br>see Figure 16                  |
|   | 1               | 50             | 1         | 50             | 1         | 50              | nA max            |   |
| $I_D$ (Off), Off Output Leakage                             | 0.04            |                | 0.04      |                | 0.04      |                 | nA typ            | $V_1 = \pm 10\text{ V}$ , $V_2 = \mp 10\text{ V}$ ;<br>see Figure 17                  |
| ADG526A   | 1               | 200            | 1         | 200            | 1         | 200             | nA max            |   |
| ADG527A   | 1               | 100            | 1         | 100            |           |                 | nA max            |   |
| $I_D$ (On), On Channel Leakage                              | 0.04            |                | 0.04      |                | 0.04      |                 | nA typ            | $V_1 = \pm 10\text{ V}$ , $V_2 = \mp 10\text{ V}$ ;<br>see Figure 18                  |
| ADG526A   | 1               | 200            | 1         | 200            | 1         | 200             | nA max            |   |
| ADG527A   | 1               | 100            | 1         | 100            |           |                 | nA max            |   |
| $I_{DIFF}$ , Differential Off Output Leakage (ADG527A Only) | 25              |                | 25        |                |           |                 | nA max            | $V_1 = \pm 10\text{ V}$ , $V_2 = \mp 10\text{ V}$ ;<br>see Figure 19                  |
| <b>DIGITAL CONTROL</b>                                      |                 |                |           |                |           |                 |                   |   |
| $V_{INH}$ , Input High Voltage                              | 2.4             |                | 2.4       |                | 2.4       |                 | V min             |   |
| $V_{INL}$ , Input Low Voltage                               | 0.8             |                | 0.8       |                | 0.8       |                 | V max             |   |
| $I_{INL}$ or $I_{INH}$                                      | 1               |                | 1         |                | 1         |                 | $\mu\text{A}$ max | $V_{IN} = 0$ to $V_{DD}$  |
| $C_{IN}$ , Digital Input Capacitance                        | 8               |                | 8         |                | 8         |                 | pF max            |   |
| <b>DYNAMIC CHARACTERISTICS<sup>1</sup></b>                  |                 |                |           |                |           |                 |                   |   |
| $t_{TRANSITION}$  | 200             |                | 200       |                | 200       |                 | ns typ            | $V_1 = \pm 10\text{ V}$ , $V_2 = \mp 10\text{ V}$ ;<br>see Figure 20                  |
|   | 300             | 400            | 300       | 400            | 300       | 400             | ns max            |   |
| $t_{OPEN}$  | 50              |                | 50        |                | 50        |                 | ns typ            | See Figure 21   |
|   | 25              | 10             | 25        | 10             | 25        | 10              | ns min            |   |
| $t_{ON}$ (EN, $\overline{WR}$ )                             | 200             |                | 200       |                | 200       |                 | ns typ            | See Figure 22 and Figure 23   |
|   | 300             | 400            | 300       | 400            | 300       | 400             | ns max            |   |
| $t_{OFF}$ (EN, $\overline{RS}$ )                            | 200             |                | 200       |                | 200       |                 | ns typ            | See Figure 22 and Figure 24   |
|   | 300             | 400            | 300       | 400            | 300       | 400             | ns max            |   |
| $t_W$ , Write Pulse Width                                   | 100             | 120            | 100       | 120            | 100       | 130             | ns min            | See Figure 13   |
| $t_S$ , Address Enable Setup Time                           | 100             |                | 100       |                | 100       |                 | ns min            | See Figure 13   |
| $t_H$ , Address Enable Hold Time                            | 10              |                | 10        |                | 10        |                 | ns min            | See Figure 13   |
| $t_{RS}$ , Reset Pulse Width                                | 100             |                | 100       |                | 100       |                 | ns min            | See Figure 14   |

# ADG526A/ADG527A

| Parameter                    | ADG526A/ADG527A |                |           |                | ADG526A   |                 | Unit              | Comments  |
|------------------------------|-----------------|----------------|-----------|----------------|-----------|-----------------|-------------------|---|
|                              | K Version       |                | B Version |                | T Version |                 |                   |   |
|                              | 25°C            | -40°C to +85°C | 25°C      | -40°C to +85°C | 25°C      | -55°C to +125°C |                   |   |
| Off Isolation                | 68              |                | 68        |                | 68        |                 | dB typ            | $V_{EN} = 0.8\text{ V}$ , $R_L = 1\text{ k}\Omega$ , $C_L = 15\text{ pF}$ , $V_S = 7\text{ V rms}$ , $f = 100\text{ kHz}$ |
| $C_S$ (Off)                  | 50              |                | 50        |                | 50        |                 | dB min            | $V_S = 7\text{ V rms}$ , $f = 100\text{ kHz}$   |
| $C_D$ (Off)                  | 5               |                | 5         |                | 5         |                 | pF typ            | $V_{EN} = 0.8\text{ V}$   |
| ADG526A                      | 44              |                | 44        |                | 44        |                 | pF typ            | $V_{EN} = 0.8\text{ V}$   |
| ADG527A                      | 22              |                | 22        |                |           |                 | pF typ            |   |
| $Q_{INj}$ , Charge Injection | 4               |                | 4         |                | 4         |                 | pC typ            | $R_S = 0\ \Omega$ , $V_S = 0\text{ V}$ ;<br>see Figure 25   |
| <b>POWER SUPPLY</b>          |                 |                |           |                |           |                 |                   |   |
| $I_{DD}$                     | 0.6             |                | 0.6       |                | 0.6       |                 | mA typ            | $V_{IN} = V_{INL}$ or $V_{INH}$   |
|                              |                 | 1.5            |           | 1.5            |           | 1.5             | mA max            |   |
| $I_{SS}$                     | 20              |                | 20        |                | 20        |                 | $\mu\text{A typ}$ | $V_{IN} = V_{INL}$ or $V_{INH}$   |
|                              |                 | 0.2            |           | 0.2            |           | 0.2             | mA max            |   |
| Power Dissipation            | 10              |                | 10        |                | 10        |                 | mW typ            |   |
|                              |                 | 28             |           | 28             |           | 28              | mW max            |   |

<sup>1</sup> Sample tested at 25°C to ensure compliance.

## SINGLE SUPPLY

$V_{DD} = 10.8\text{ V to }16.5\text{ V}$ ,  $V_{SS} = \text{GND to }0\text{ V}$ , unless otherwise noted.

**Table 2.**

| Parameter   | ADG526A/ADG527A |                |           |                | ADG526A   |                 | Unit              | Comments  |
|---|-----------------|----------------|-----------|----------------|-----------|-----------------|-------------------|---|
|   | K Version       |                | B Version |                | T Version |                 |                   |   |
|   | 25°C            | -40°C to +85°C | 25°C      | -40°C to +85°C | 25°C      | -55°C to +125°C |                   |   |
| <b>ANALOG SWITCH</b>  |                 |                |           |                |           |                 |                   |   |
| Analog Signal Range   | $V_{SS}$        | $V_{SS}$       | $V_{SS}$  | $V_{SS}$       | $V_{SS}$  | $V_{SS}$        | V min             |   |
|   | $V_{DD}$        | $V_{DD}$       | $V_{DD}$  | $V_{DD}$       | $V_{DD}$  | $V_{DD}$        | V max             |   |
| $R_{ON}$  | 500             |                | 500       |                | 500       |                 | $\Omega$ typ      | $0\text{ V} \leq V_S \leq 10\text{ V}$ , $I_{DS} = 0.5\text{ mA}$ ; see Figure 15 |
| $R_{ON}$ Drift  | 700             | 1000           | 700       | 1000           | 700       | 1000            | $\Omega$ max      |   |
|   | 0.6             |                | 0.6       |                | 0.6       |                 | %/°C typ          | $0\text{ V} \leq V_S \leq 10\text{ V}$ , $I_{DS} = 0.5\text{ mA}$                 |
| $R_{ON}$ Match  | 5               |                | 5         |                | 5         |                 | % typ             | $0\text{ V} \leq V_S \leq 10\text{ V}$ , $I_{DS} = 0.5\text{ mA}$                 |
| $I_S$ (Off), Off Input Leakage                              | 0.02            |                | 0.02      |                | 0.02      |                 | nA typ            | $V_1 = 10\text{ V}/0\text{ V}$ , $V_2 = 0\text{ V}/10\text{ V}$ ; see Figure 16   |
| $I_D$ (Off), Off Output Leakage                             | 1               | 50             | 1         | 50             | 1         | 50              | nA max            |   |
|   | 0.04            |                | 0.04      |                | 0.04      |                 | nA typ            | $V_1 = 10\text{ V}/0\text{ V}$ , $V_2 = 0\text{ V}/10\text{ V}$ ; see Figure 17   |
| ADG526A   | 1               | 200            | 1         | 200            | 1         | 200             | nA max            |   |
| ADG527A   | 1               | 100            | 1         | 100            |           |                 | nA max            |   |
| $I_D$ (On), On Channel Leakage                              | 0.04            |                | 0.04      |                | 0.04      |                 | nA typ            | $V_1 = 10\text{ V}/0\text{ V}$ , $V_2 = 0\text{ V}/10\text{ V}$ ; see Figure 18   |
| ADG526A   | 1               | 200            | 1         | 200            | 1         | 200             | nA max            |   |
| ADG527A   | 1               | 100            | 1         | 100            |           |                 | nA max            |   |
| $I_{DIFF}$ , Differential Off Output Leakage (ADG527A Only) |                 | 25             |           | 25             |           |                 | nA max            | $V_1 = 10\text{ V}/0\text{ V}$ , $V_2 = 0\text{ V}/10\text{ V}$ ; see Figure 19   |
| <b>DIGITAL CONTROL</b>                                      |                 |                |           |                |           |                 |                   |   |
| $V_{INH}$ , Input High Voltage                              |                 | 2.4            |           | 2.4            |           | 2.4             | V min             |   |
| $V_{INL}$ , Input Low Voltage                               |                 | 0.8            |           | 0.8            |           | 0.8             | V max             |   |
| $I_{INL}$ or $I_{INH}$                                      |                 | 1              |           | 1              |           | 1               | $\mu\text{A}$ max | $V_{IN} = 0\text{ to }V_{DD}$   |
| $C_{IN}$ , Digital Input Capacitance                        | 8               |                | 8         |                | 8         |                 | pF max            |   |
| <b>DYNAMIC CHARACTERISTICS<sup>1</sup></b>                  |                 |                |           |                |           |                 |                   |   |
| $t_{TRANSITION}$  | 300             |                | 300       |                | 300       |                 | ns typ            | $V_1 = 10\text{ V}/0\text{ V}$ , $V_2 = 0\text{ V}/10\text{ V}$ ; see Figure 20   |
| $t_{OPEN}$  | 450             | 600            | 450       | 600            | 450       | 600             | ns max            |   |
|   | 50              |                | 50        |                | 50        |                 | ns typ            | See Figure 21   |
|   | 25              | 10             | 25        | 10             | 25        | 10              | ns min            |   |
| $t_{ON}$ (EN, $\overline{WR}$ )                             | 250             |                | 250       |                | 250       |                 | ns typ            | See Figure 22 and Figure 23   |
| $t_{OFF}$ (EN, $\overline{RS}$ )                            | 450             | 600            | 450       | 600            | 450       | 600             | ns max            |   |
|   | 250             |                | 250       |                | 250       |                 | ns typ            | See Figure 22 and Figure 24   |
| $t_W$ Write Pulse Width                                     | 450             | 600            | 450       | 600            | 450       | 600             | ns max            |   |
|   | 100             | 120            | 100       | 120            | 100       | 130             | ns min            | See Figure 13   |
| $t_S$ Address Enable Setup Time                             |                 | 100            |           | 100            |           | 100             | ns min            | See Figure 13   |
| $t_H$ Address Enable Hold Time                              |                 | 10             |           | 10             |           | 10              | ns min            | See Figure 13   |
| $t_{RS}$ Reset Pulse Width                                  |                 | 100            |           | 100            |           | 100             | ns min            | See Figure 14   |
| Off Isolation   | 68              |                | 68        |                | 68        |                 | dB typ            | $V_{EN} = 0.8\text{ V}$ , $R_L = 1\text{ k}\Omega$ , $C_L = 15\text{ pF}$         |
|   | 50              |                | 50        |                | 50        |                 | dB min            | $V_S = 3.5\text{ V rms}$ , $f = 100\text{ kHz}$                                   |

# ADG526A/ADG527A

| Parameter                    | ADG526A/ADG527A |                |           |                | ADG526A   |                 | Unit   | Comments   |
|------------------------------|-----------------|----------------|-----------|----------------|-----------|-----------------|--------|--|
|                              | K Version       |                | B Version |                | T Version |                 |        |  |
|                              | 25°C            | -40°C to +85°C | 25°C      | -40°C to +85°C | 25°C      | -55°C to +125°C |        |  |
| $C_S$ (Off)                  | 5               |                | 5         |                | 5         |                 | pF typ | $V_{EN} = 0.8\text{ V}$                                |
| $C_D$ (Off)                  | 44              |                | 44        |                | 44        |                 | pF typ | $V_{EN} = 0.8\text{ V}$                                |
| ADG526A                      | 22              |                | 22        |                |           |                 | pF typ |  |
| ADG527A                      | 4               |                | 4         |                | 4         |                 | pC typ | $R_S = 0\ \Omega$ , $V_S = 0\text{ V}$ ; see Figure 25 |
| $Q_{INj}$ , Charge Injection |                 |                |           |                |           |                 |        |  |
| POWER SUPPLY                 |                 |                |           |                |           |                 |        |  |
| $I_{DD}$                     | 0.6             |                | 0.6       |                | 0.6       |                 | mA typ | $V_{IN} = V_{INL}$ or $V_{INH}$                        |
|                              |                 | 1.5            |           | 1.5            |           | 1.5             | mA max |  |
| Power Dissipation            | 11              |                | 11        |                | 11        |                 | mW typ |  |
|                              |                 | 25             |           | 25             |           | 25              | mW max |  |

<sup>1</sup> Sample tested at 25°C to ensure compliance.

## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ , unless otherwise noted.

**Table 3.**

| Parameter  | Rating   |
|--|--|
| $V_{DD}$ to $V_{SS}$   | 44 V   |
| $V_{DD}$ to GND  | 25 V   |
| $V_{SS}$ to GND  | -25 V  |
| Analog Inputs <sup>1</sup>                                     |  |
| Voltage at Sx or Dx Pins                                       | $V_{SS} - 2\text{ V}$ to $V_{DD} + 2\text{ V}$<br>or 20 mA, whichever occurs first |
| Continuous Current, Sx or Dx Pins                              | 20 mA  |
| Pulsed Current, Sx or Dx Pins<br>1 ms Duration, 10% Duty Cycle | 40 mA  |
| Digital Inputs <sup>1</sup>                                    |  |
| Voltage at A, EN, $\overline{WR}$ , $\overline{RS}$            | $V_{SS} - 4\text{ V}$ to $V_{DD} + 4\text{ V}$<br>or 20 mA, whichever occurs first |
| Power Dissipation (Any Package)                                |  |
| Up to $75^\circ\text{C}$                                       | 470 mW   |
| Derates Above $75^\circ\text{C}$                               | 6 mW/ $^\circ\text{C}$   |
| Operating Temperature Range                                    |  |
| Commercial (K Version)   | $-40^\circ\text{C}$ to $+85^\circ\text{C}$   |
| Industrial (B Version)   | $-40^\circ\text{C}$ to $+85^\circ\text{C}$   |
| Storage Temperature Range                                      | $-65^\circ\text{C}$ to $+150^\circ\text{C}$  |
| Lead Temperature (Soldering, 10 sec)                           | $300^\circ\text{C}$  |

<sup>1</sup> Overvoltage at A, EN,  $\overline{WR}$ ,  $\overline{RS}$ , Sx, or Dx pins are clamped by diodes. Limit current to the maximum rating in Table 3.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# ADG526A/ADG527A

## PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

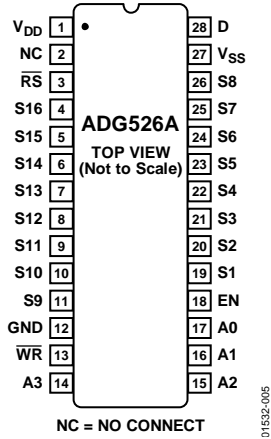


Figure 3. ADG526A PDIP, SOIC, and CERDIP Pin Configuration



Figure 4. ADG526A PLCC Pin Configuration

Table 4. ADG526A Pin Function Descriptions

| Pin No. | Mnemonic        | Description   |
|---------|-----------------|---|
| 1       | V <sub>DD</sub> | Most Positive Power Supply Potential.   |
| 2       | NC              | No Connect.   |
| 3       | $\overline{RS}$ | Reset. The $\overline{RS}$ signal clears both the address and enable data in the latches resulting in no output (all switches off). |
| 4       | S16             | Source Terminal. This pin can be an input or output.  |
| 5       | S15             | Source Terminal. This pin can be an input or output.  |
| 6       | S14             | Source Terminal. This pin can be an input or output.  |
| 7       | S13             | Source Terminal. This pin can be an input or output.  |
| 8       | S12             | Source Terminal. This pin can be an input or output.  |
| 9       | S11             | Source Terminal. This pin can be an input or output.  |
| 10      | S10             | Source Terminal. This pin can be an input or output.  |
| 11      | S9              | Source Terminal. This pin can be an input or output.  |
| 12      | GND             | Ground (0 V) Reference.   |
| 13      | $\overline{WR}$ | Write. The $\overline{WR}$ signal latches the state of the address control lines and the enable line.                               |
| 14      | A3              | Logic Control Inputs. Selects which source terminal is connected to the drain (D).  |
| 15      | A2              | Logic Control Inputs. Selects which source terminal is connected to the drain (D).  |
| 16      | A1              | Logic Control Inputs. Selects which source terminal is connected to the drain (D).  |
| 17      | A0              | Logic control inputs. Selects which source terminal is connected to the drain (D).  |
| 18      | EN              | Enable. Active high logic control input.  |
| 19      | S1              | Source Terminal. This pin can be an input or output.  |
| 20      | S2              | Source Terminal. This pin can be an input or output.  |
| 21      | S3              | Source Terminal. This pin can be an input or output.  |
| 22      | S4              | Source Terminal. This pin can be an input or output.  |
| 23      | S5              | Source Terminal. This pin can be an input or output.  |
| 24      | S6              | Source Terminal. This pin can be an input or output.  |
| 25      | S7              | Source Terminal. This pin can be an input or output.  |
| 26      | S8              | Source Terminal. This pin can be an input or output.  |
| 27      | V <sub>SS</sub> | Most Negative Power Supply Potential.   |
| 28      | D               | Drain Terminal. This pin can be an input or output.   |





Figure 5. ADG527A PDIP, SOIC Pin Configuration

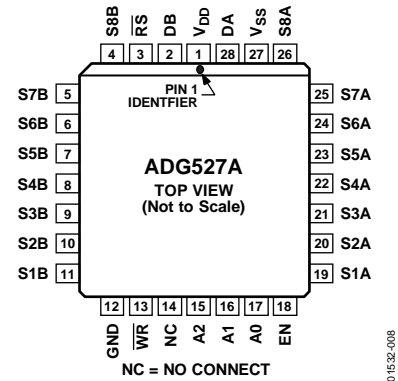


Figure 6. ADG527A PLCC Pin Configuration

**Table 5. ADG527A Pin Function Descriptions**

| Pin No. | Mnemonic        | Description   |
|---------|-----------------|---|
| 1       | V <sub>DD</sub> | Most Positive Power Supply Potential.   |
| 2       | DB              | Drain Terminal. This pin can be an input or output.   |
| 3       | $\overline{RS}$ | Reset. The $\overline{RS}$ signal clears both the address and enable data in the latches resulting in no output (all switches off). |
| 4       | S8B             | Source Terminal. This pin can be an input or output.  |
| 5       | S7B             | Source Terminal. This pin can be an input or output.  |
| 6       | S6B             | Source Terminal. This pin can be an input or output.  |
| 7       | S5B             | Source Terminal. This pin can be an input or output.  |
| 8       | S4B             | Source Terminal. This pin can be an input or output.  |
| 9       | S3B             | Source Terminal. This pin can be an input or output.  |
| 10      | S2B             | Source Terminal. This pin can be an input or output.  |
| 11      | S1B             | Source Terminal. This pin can be an input or output.  |
| 12      | GND             | Ground (0 V) Reference.   |
| 13      | $\overline{WR}$ | Write. The $\overline{WR}$ signal latches the state of the address control lines and the enable line.                               |
| 14      | NC              | No Connect.   |
| 15      | A2              | Logic Control Inputs. Selects which source terminal is connected to the drain (D).  |
| 16      | A1              | Logic Control Inputs. Selects which source terminal is connected to the drain (D).  |
| 17      | A0              | Logic Control Inputs. Selects which source terminal is connected to the drain (D).  |
| 18      | EN              | Enable. Active high logic control input.  |
| 19      | S1A             | Source Terminal. This pin can be an input or output.  |
| 20      | S2A             | Source Terminal. This pin can be an input or output.  |
| 21      | S3A             | Source Terminal. This pin can be an input or output.  |
| 22      | S4A             | Source Terminal. This pin can be an input or output.  |
| 23      | S5A             | Source Terminal. This pin can be an input or output.  |
| 24      | S6A             | Source Terminal. This pin can be an input or output.  |
| 25      | S7A             | Source Terminal. This pin can be an input or output.  |
| 26      | S8A             | Source Terminal. This pin can be an input or output.  |
| 27      | V <sub>SS</sub> | Most Negative Power Supply Potential.   |
| 28      | DA              | Drain Terminal. This pin can be an input or output.   |

# ADG526A/ADG527A

Table 6. ADG526A Truth Table<sup>1</sup>

| A3 | A2 | A1 | A0 | EN | $\overline{WR}$       | $\overline{RS}$ | ON SWITCH                                 |
|----|----|----|----|----|-----------------------|-----------------|---|
| X  | X  | X  | X  | X  | $\overline{\text{f}}$ | 1               | Retains previous switch condition         |
| X  | X  | X  | X  | X  | X                     | 0               | None (address and enable latches cleared) |
| X  | X  | X  | X  | 0  | 0                     | 1               | None                                      |
| 0  | 0  | 0  | 0  | 1  | 0                     | 1               | 1   |
| 0  | 0  | 0  | 1  | 1  | 0                     | 1               | 2   |
| 0  | 0  | 1  | 0  | 1  | 0                     | 1               | 3   |
| 0  | 0  | 1  | 1  | 1  | 0                     | 1               | 4   |
| 0  | 1  | 0  | 0  | 1  | 0                     | 1               | 5   |
| 0  | 1  | 0  | 1  | 1  | 0                     | 1               | 6   |
| 0  | 1  | 1  | 0  | 1  | 0                     | 1               | 7   |
| 0  | 1  | 1  | 1  | 1  | 0                     | 1               | 8   |
| 1  | 0  | 0  | 0  | 1  | 0                     | 1               | 9   |
| 1  | 0  | 0  | 1  | 1  | 0                     | 1               | 10  |
| 1  | 0  | 1  | 0  | 1  | 0                     | 1               | 11  |
| 1  | 0  | 1  | 1  | 1  | 0                     | 1               | 12  |
| 1  | 1  | 0  | 0  | 1  | 0                     | 1               | 13  |
| 1  | 1  | 0  | 1  | 1  | 0                     | 1               | 14  |
| 1  | 1  | 1  | 0  | 1  | 0                     | 1               | 15  |
| 1  | 1  | 1  | 1  | 1  | 0                     | 1               | 16  |

<sup>1</sup> X = don't care.

Table 7. ADG527A Truth Table<sup>1</sup>

| A2 | A1 | A0 | EN | $\overline{WR}$       | $\overline{RS}$ | ON SWITCH PAIR                            |
|----|----|----|----|-----------------------|-----------------|---|
| X  | X  | X  | X  | $\overline{\text{f}}$ | 1               | Retains previous switch condition         |
| X  | X  | X  | X  | X                     | 0               | None (address and enable latches cleared) |
| X  | X  | X  | 0  | 0                     | 1               | None                                      |
| 0  | 0  | 0  | 1  | 0                     | 1               | 1   |
| 0  | 0  | 1  | 1  | 0                     | 1               | 2   |
| 0  | 1  | 0  | 1  | 0                     | 1               | 3   |
| 0  | 1  | 1  | 1  | 0                     | 1               | 4   |
| 1  | 0  | 0  | 1  | 0                     | 1               | 5   |
| 1  | 0  | 1  | 1  | 0                     | 1               | 6   |
| 1  | 1  | 0  | 1  | 0                     | 1               | 7   |
| 1  | 1  | 1  | 1  | 0                     | 1               | 8   |

<sup>1</sup> X = don't care.

# TYPICAL PERFORMANCE CHARACTERISTICS

The multiplexers are guaranteed functional with reduced single or dual supplies down to 4.5 V.

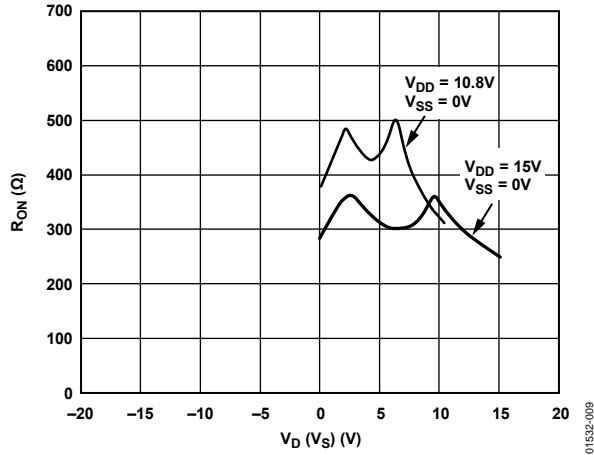


Figure 7.  $R_{ON}$  as a Function of  $V_D$  ( $V_S$ ): Single-Supply Voltage,  $T_A = 25^\circ\text{C}$

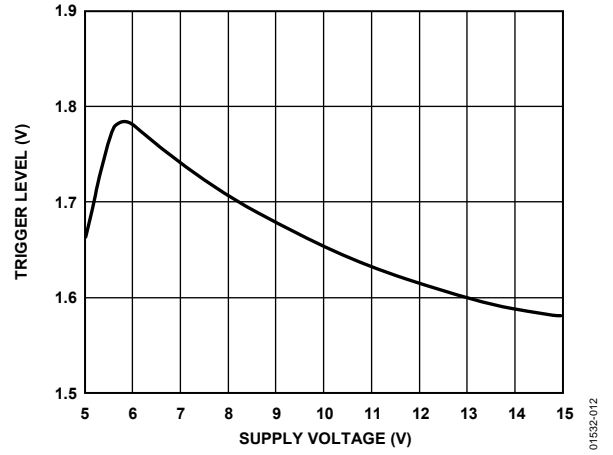


Figure 10. Trigger Levels vs. Power Supply Voltage, Dual or Single Supply,  $T_A = 25^\circ\text{C}$

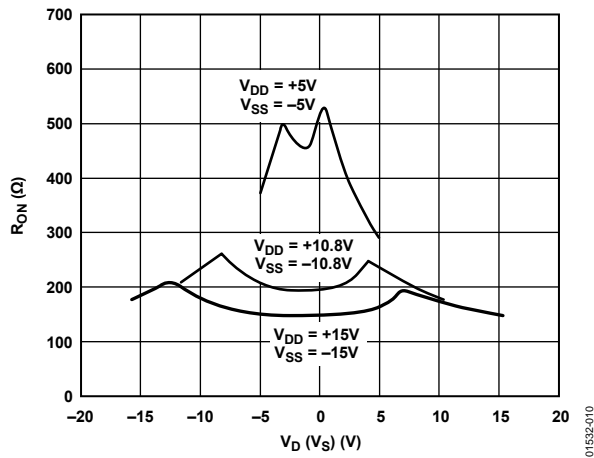


Figure 8.  $R_{ON}$  as a Function of  $V_D$  ( $V_S$ ): Dual-Supply Voltage,  $T_A = 25^\circ\text{C}$

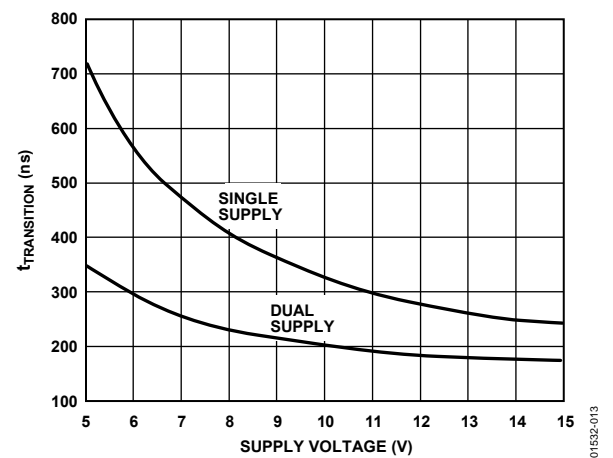


Figure 11.  $t_{TRANSITION}$  vs. Supply Voltage: Dual and Single Supplies,  $T_A = 25^\circ\text{C}$   
(Note: For  $V_{DD}$  and  $V_{SS} < 10\text{ V}$ ;  $V_1 = V_{DD}/V_{SS}$ ,  $V_2 = V_{SS}/V_{DD}$ ; See Figure 20)

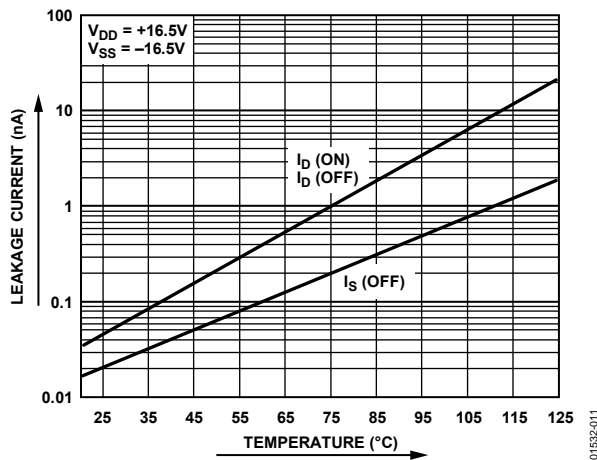


Figure 9. Leakage Current as a Function of Temperature (Leakage Currents Reduce as the Supply Voltages Reduce)

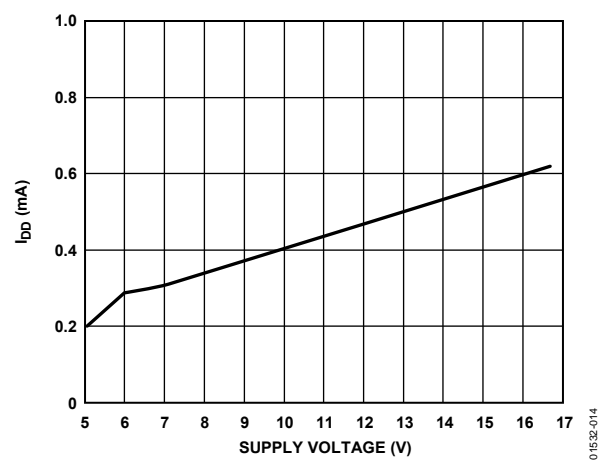


Figure 12.  $I_{DD}$  vs. Supply Voltage: Dual or Single Supply,  $T_A = 25^\circ\text{C}$

## TERMINOLOGY

**R<sub>ON</sub>**

Ohmic resistance between Terminal D and Terminal S.

**R<sub>ON</sub> Match**

Difference between the R<sub>ON</sub> of any two channels.

**R<sub>ON</sub> Drift**

Change in R<sub>ON</sub> vs. temperature.

**I<sub>S</sub> (Off)**

Source terminal leakage current when the switch is off.

**I<sub>D</sub> (Off)**

Drain terminal leakage current when the switch is off.

**I<sub>D</sub> (On)**

Leakage current that flows from the closed switch into the body.

**V<sub>S</sub> (V<sub>D</sub>)**

Analog voltage on Terminal S or Terminal D.

**C<sub>S</sub> (Off)**

Channel input capacitance for off condition.

**C<sub>D</sub> (Off)**

Channel output capacitance for off condition.

**C<sub>IN</sub>**

Digital input capacitance.

**t<sub>ON</sub> (EN)**

Delay time between the 50% and 90% points of the digital input and switch on condition.

**t<sub>OFF</sub> (EN)**

Delay time between the 50% and 10% points of the digital input and switch off condition.

**t<sub>TRANSITION</sub>**

Delay time between the 50% and 90% points of the digital inputs and switch on condition when switching from one address state to another.

**t<sub>OPEN</sub>**

Off time measured between 50% points of both switches when switching from one address state to another.

**V<sub>INL</sub>**

Maximum input voltage for Logic 0.

**V<sub>INH</sub>**

Minimum input voltage for Logic 1.

**I<sub>INL</sub> (I<sub>INH</sub>)**

Input current of the digital input.

**V<sub>DD</sub>**

Most positive voltage supply.

**V<sub>SS</sub>**

Most negative voltage supply.

**I<sub>DD</sub>**

Positive supply current.

**I<sub>SS</sub>**

Negative supply current.

**TIMING**

Figure 13 shows the timing sequence for latching the switch address and enable inputs. The latches are level sensitive; therefore, while  $\overline{WR}$  is held low, the latches are transparent and the switches respond to the address and enable inputs. This input data is latched on the rising edge of  $\overline{WR}$ .

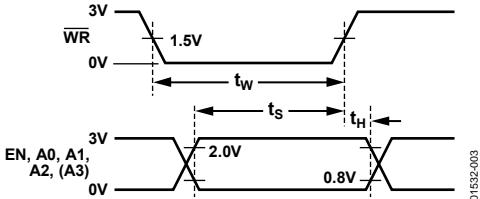


Figure 13. Timing Sequence

01552-003

Figure 14 shows the reset pulse width,  $t_{RS}$ , and reset turn-off time,  $t_{OFF}(\overline{RS})$ .

Note that all digital input signal rise and fall times are measured from 10% to 90% of 3 V,  $t_R = t_F = 20$  ns.

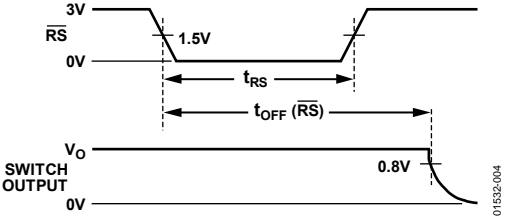


Figure 14. Reset Pulse

01552-004

## TEST CIRCUITS



Figure 15.  $R_{ON}$

01532-015

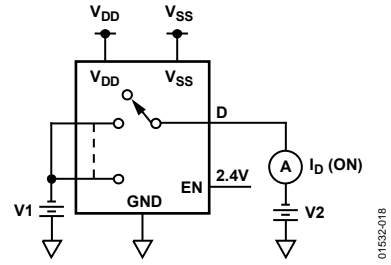


Figure 18.  $I_D$  (On)

01532-018

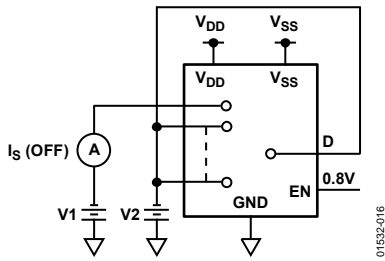


Figure 16.  $I_S$  (Off)

01532-016

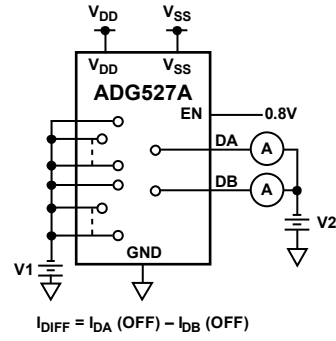


Figure 19.  $I_{DIFF}$

01532-019

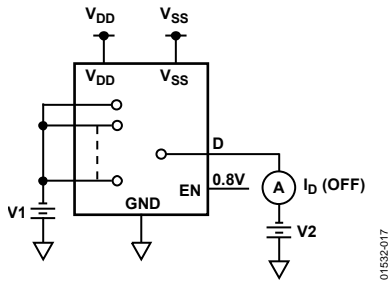


Figure 17.  $I_D$  (Off)

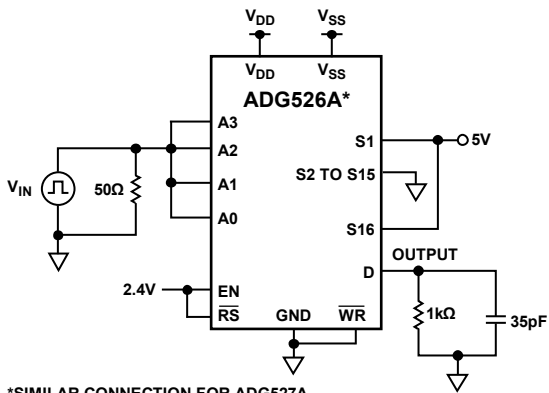
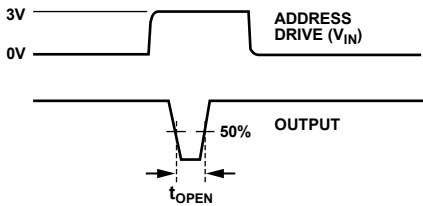
01532-017



\*SIMILAR CONNECTION FOR ADG527A.

Figure 20. Switching Time of Multiplexer,  $t_{TRANSITION}$

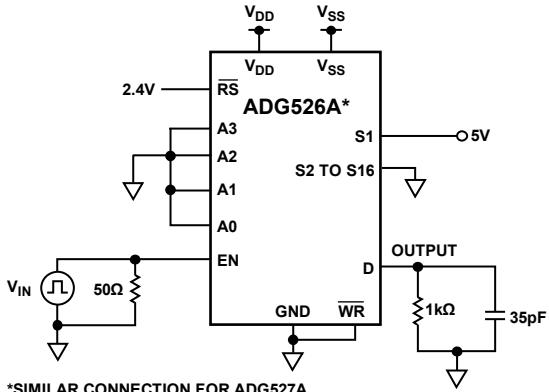
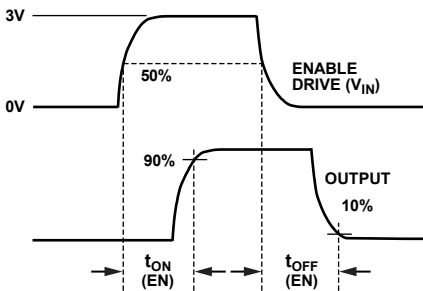
01532-020



\*SIMILAR CONNECTION FOR ADG527A.

Figure 21. Break-Before-Make Delay,  $t_{OPEN}$

01532-021



\*SIMILAR CONNECTION FOR ADG527A.

Figure 22. Enable Delay,  $t_{ON} (EN)$   $t_{OFF} (EN)$

01532-022

# ADG526A/ADG527A

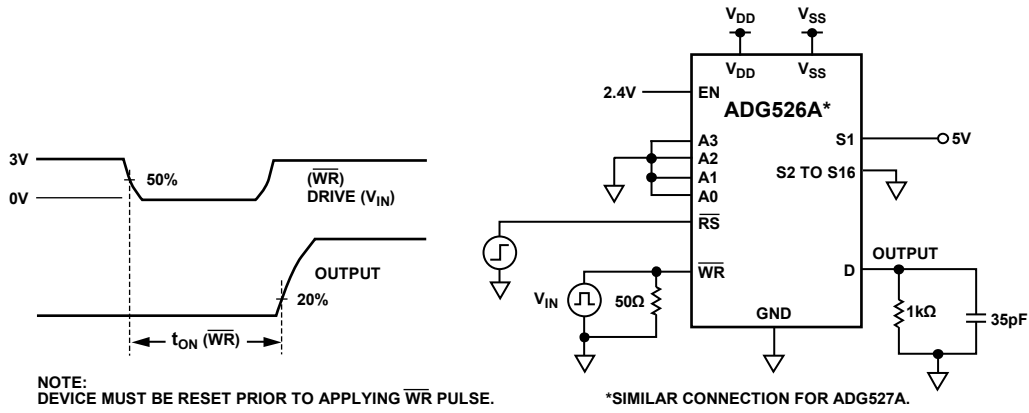


Figure 23. Write Turn-On Time,  $t_{ON}(\overline{WR})$

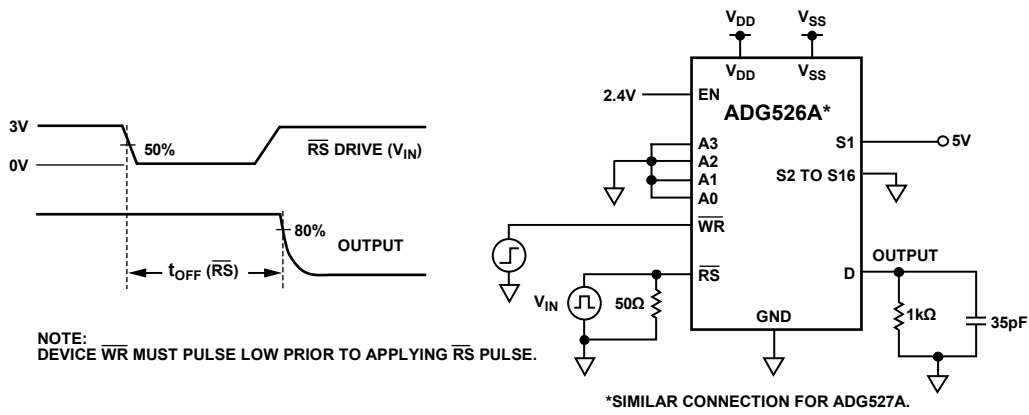


Figure 24. Reset Turn-Off,  $t_{OFF}(\overline{RS})$

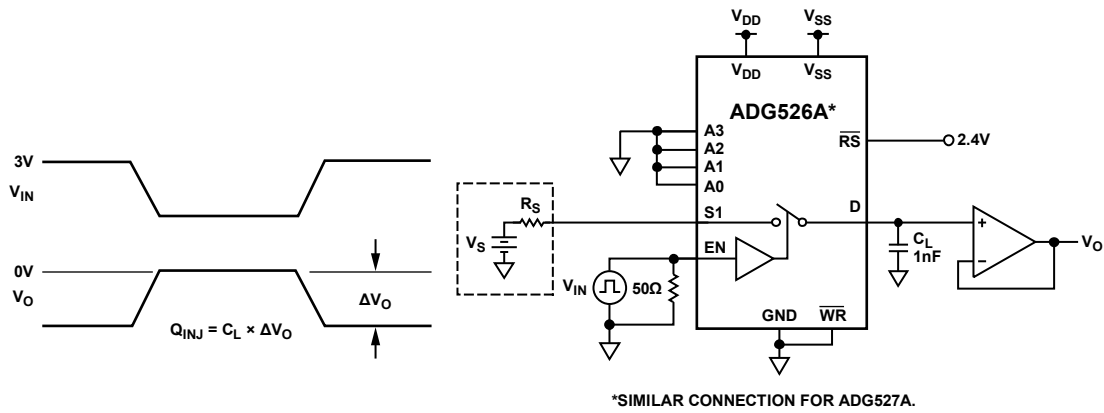
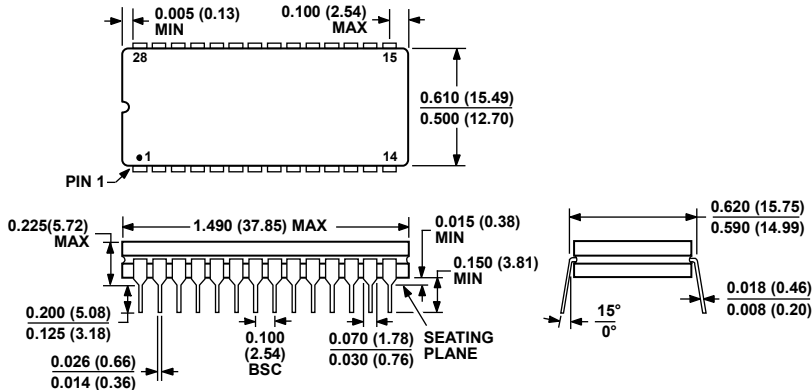


Figure 25. Charge Injection



OUTLINE DIMENSIONS

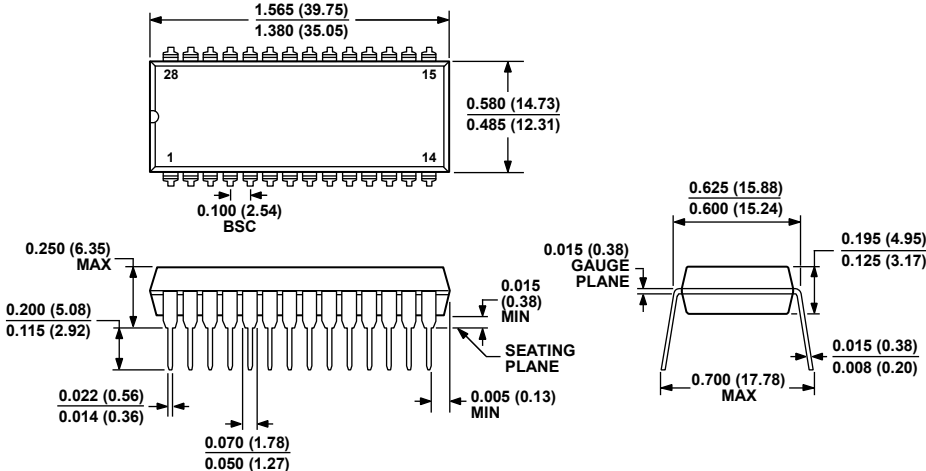


CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

030106-A

Figure 26. 28-Lead Ceramic Dual In-Line Package [CERDIP] (Q-28)

Dimensions shown in inches and (millimeters)



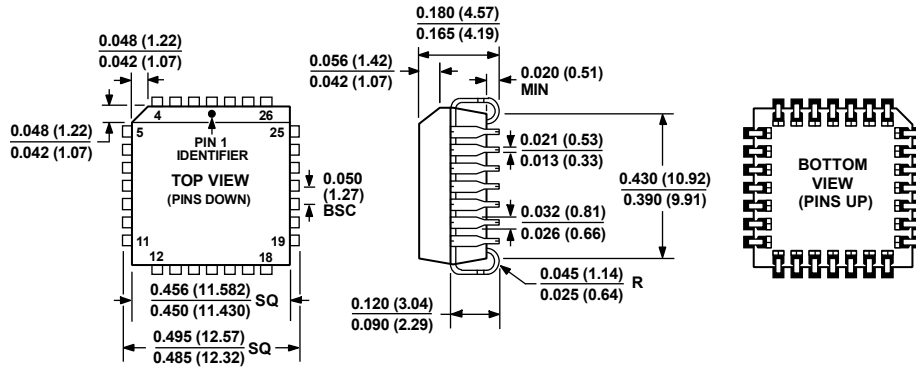
COMPLIANT TO JEDEC STANDARDS MS-011  
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN. CORNER LEADS MAY BE CONFIGURED AS WHOLE LEADS.

071006-A

Figure 27. 28-Lead Plastic Dual In-Line Package [PDIP] (N-28)

Dimensions shown in inches and (millimeters)

# ADG526A/ADG527A



COMPLIANT TO JEDEC STANDARDS MO-047-AB  
 CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS  
 (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR  
 REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 28. 28-Lead Plastic Leaded Chip Carrier [PLCC]  
 (P-28A)

Dimensions shown in inches and (millimeters)

0425018-A



COMPLIANT TO JEDEC STANDARDS MS-013-AE  
 CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS  
 (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR  
 REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 29. 28-Lead Standard Small Outline Package [SOIC] Wide Body  
 (RW-28)

Dimensions shown in millimeters and (inches)

060706-A

**ORDERING GUIDE**

| Model                        | Temperature Range | Package Description | Package Option |
|------------------------------|-------------------|---------------------|----------------|
| ADG526AKN                    | -40°C to +85°C    | 28-Lead PDIP        | N-28           |
| ADG526AKNZ <sup>1</sup>      | -40°C to +85°C    | 28-Lead PDIP        | N-28           |
| ADG526AKR                    | -40°C to +85°C    | 28-Lead SOIC        | RW-28          |
| ADG526AKR-REEL               | -40°C to +85°C    | 28-Lead SOIC        | RW-28          |
| ADG526AKRZ <sup>1</sup>      | -40°C to +85°C    | 28-Lead SOIC        | RW-28          |
| ADG526AKRZ-REEL <sup>1</sup> | -40°C to +85°C    | 28-Lead SOIC        | RW-28          |
| ADG526AKP                    | -40°C to +85°C    | 28-Lead PLCC        | P-28A          |
| ADG526AKP-REEL               | -40°C to +85°C    | 28-Lead PLCC        | P-28A          |
| ADG526AKPZ <sup>1</sup>      | -40°C to +85°C    | 28-Lead PLCC        | P-28A          |
| ADG526AKPZ-REEL <sup>1</sup> | -40°C to +85°C    | 28-Lead PLCC        | P-28A          |
| ADG526ATQ                    | -55°C to +125°C   | 28-Lead CERDIP      | Q-28           |
| ADG526ABQ                    | -40°C to +85°C    | 28-Lead CERDIP      | Q-28           |
| ADG526ATCHIPS                |                   |                     | DIE            |
| ADG527AKN                    | -40°C to +85°C    | 28-Lead PDIP        | N-28           |
| ADG527AKNZ <sup>1</sup>      | -40°C to +85°C    | 28-Lead PDIP        | N-28           |
| ADG527AKR                    | -40°C to +85°C    | 28-Lead SOIC        | RW-28          |
| ADG527AKR-REEL               | -40°C to +85°C    | 28-Lead SOIC        | RW-28          |
| ADG527AKRZ <sup>1</sup>      | -40°C to +85°C    | 28-Lead SOIC        | RW-28          |
| ADG527AKP                    | -40°C to +85°C    | 28-Lead PLCC        | P-28A          |
| ADG527AKPZ <sup>1</sup>      | -40°C to +85°C    | 28-Lead PLCC        | P-28A          |

<sup>1</sup> Z = RoHS Compliant Part, # denotes RoHS complaint product, may be top or bottom marked.

**NOTES**



Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов;
- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



#### Как с нами связаться

**Телефон:** 8 (812) 309 58 32 (многоканальный)

**Факс:** 8 (812) 320-02-42

**Электронная почта:** [org@eplast1.ru](mailto:org@eplast1.ru)

**Адрес:** 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.