

## Product Summary

$V_{(BR)DSS}$	$R_{DS(ON)}$ max	$I_D$ $T_A = +25^\circ C$
60V	69m $\Omega$ @ $V_{GS} = 10V$	4.3A
	100m $\Omega$ @ $V_{GS} = 4.5V$	3.5A

## Description

This new generation MOSFET has been designed to minimize the on-state resistance ( $R_{DS(on)}$ ) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.


## Applications

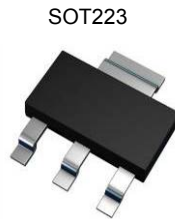
- Motor control
- Transformer driving switch
- DC-DC Converters
- Power management functions
- Uninterrupted power supply

## Features

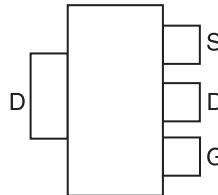
- 100% Unclamped Inductive Switch (UIS) test in production
- Fast switching speed
- Low on-resistance
- **Lead-Free Finish; RoHS compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **Qualified to AEC-Q101 Standards for High Reliability**

## Mechanical Data

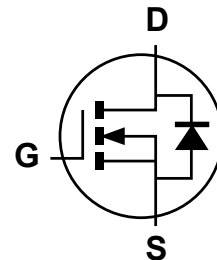
- Case: SOT223
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0 (Note 1)
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals Connections: See diagram below
- Terminals: Finish - Matte Tin annealed over Copper lead frame. Solderable per MIL-STD-202, Method 208 
- Weight: 0.112 grams (approximate)



Top View



Pin Out - Top View



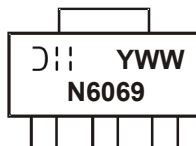
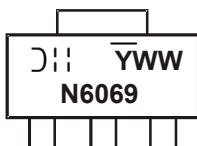
Equivalent Circuit


## Ordering Information (Note 4)

Part Number	Qualification	Case	Packaging
DMN6069SE-13	Standard	SOT223	2,500 / Tape & Reel

- Notes:
1. EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant. All applicable RoHS exemptions applied.
  2. See [http://www.diodes.com/quality/lead\\_free.html](http://www.diodes.com/quality/lead_free.html) for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
  3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
  4. For packaging details, go to our website at <http://www.diodes.com/products/packages.html>.

## Marking Information



 = Manufacturer's Marking  
 N6069 = Marking Code  
 YWW = Date Code Marking for SAT (Shanghai Assembly/ Test site)  
 YWW = Date Code Marking for CAT (Chengdu Assembly/ Test site)  
 Y or Y = Year (ex: 3 = 2013)  
 WW = Week (01 - 53)

**Maximum Ratings** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Units
Drain-Source Voltage	V <sub>DSS</sub>	60	V
Gate-Source Voltage	V <sub>GSS</sub>	±20	V
Continuous Drain Current (Note 6) V <sub>GS</sub> = 10V	T <sub>A</sub> = +25°C	I <sub>D</sub> = 4.3	A
	T <sub>A</sub> = +70°C	I <sub>D</sub> = 3.3	A
Pulsed Drain Current (10µs pulse, duty cycle = 1%)	T <sub>C</sub> = +25°C	I <sub>D</sub> = 10	A
	T <sub>C</sub> = +70°C	I <sub>D</sub> = 8	A
Maximum Body Diode Continuous Current	I <sub>S</sub>	3.2	A

**Thermal Characteristics** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Units
Total Power Dissipation (Note 5)	P <sub>D</sub>	T <sub>A</sub> = +25°C	2.2
		T <sub>A</sub> = +70°C	1.4
Thermal Resistance, Junction to Ambient (Note 5)	R <sub>θJA</sub>	58	°C/W
Total Power Dissipation (Note 5)	P <sub>D</sub>	11	W
Thermal Resistance, Junction to Case (Note 5)	R <sub>θJC</sub>	8.9	°C/W
Operating and Storage Temperature Range	T <sub>J</sub> , T <sub>STG</sub>	-55 to +150	°C

**Electrical Characteristics** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
<b>OFF CHARACTERISTICS (Note 7)</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	60	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250µA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	—	—	1	µA	V <sub>DS</sub> = 60V, V <sub>GS</sub> = 0V
Gate-Source Leakage	I <sub>GSS</sub>	—	—	±100	nA	V <sub>GS</sub> = ±20V, V <sub>DS</sub> = 0V
<b>ON CHARACTERISTICS (Note 7)</b>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	1	—	3	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250µA
Static Drain-Source On-Resistance	R <sub>DS(on)</sub>	—	47	69	mΩ	V <sub>GS</sub> = 10V, I <sub>D</sub> = 3A
		—	54	100		V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 2.4A
Diode Forward Voltage	V <sub>SD</sub>	—	0.8	1.1	V	V <sub>GS</sub> = 0V, I <sub>S</sub> = 2.5A
<b>DYNAMIC CHARACTERISTICS (Note 8)</b>						
Input Capacitance	C <sub>iss</sub>	—	825	—	pF	V <sub>DS</sub> = 30V, V <sub>GS</sub> = 0V f = 1MHz
Output Capacitance	C <sub>oss</sub>	—	40	—		
Reverse Transfer Capacitance	C <sub>rss</sub>	—	29	—		
Gate Resistance	R <sub>G</sub>	—	2.3	—	Ω	V <sub>DS</sub> = 0V, V <sub>GS</sub> = 0V, f = 1.0MHz
Total Gate Charge (V <sub>GS</sub> = 4.5V)	Q <sub>g</sub>	—	7.2	—	nC	V <sub>DS</sub> = 30V, I <sub>D</sub> = 12A
Total Gate Charge (V <sub>GS</sub> = 10V)	Q <sub>g</sub>	—	16	—		
Gate-Source Charge	Q <sub>gs</sub>	—	3.2	—		
Gate-Drain Charge	Q <sub>gd</sub>	—	2.8	—		
Turn-On Delay Time	t <sub>D(on)</sub>	—	3.8	—	nS	V <sub>DD</sub> = 30V, V <sub>GS</sub> = 10V, R <sub>G</sub> = 6Ω, I <sub>D</sub> = 12A
Turn-On Rise Time	t <sub>r</sub>	—	6.7	—		
Turn-Off Delay Time	t <sub>D(off)</sub>	—	16	—		
Turn-Off Fall Time	t <sub>f</sub>	—	5.3	—		

- Notes:
- Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.
  - Device mounted on FR-4 substrate PC board, 2oz copper, with thermal vias to bottom layer 1inch square copper plate
  - Short duration pulse test used to minimize self-heating effect.
  - Guaranteed by design. Not subject to product testing.

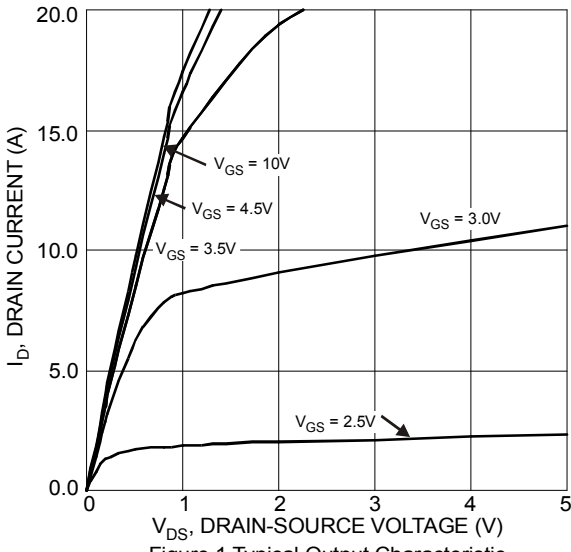


Figure 1 Typical Output Characteristic

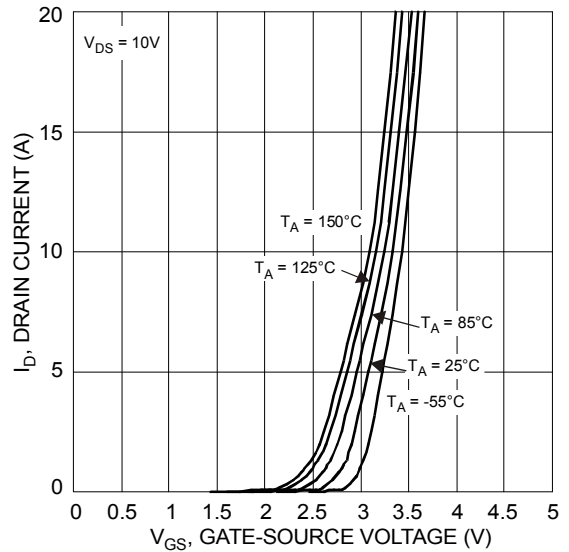


Figure 2 Typical Transfer Characteristics

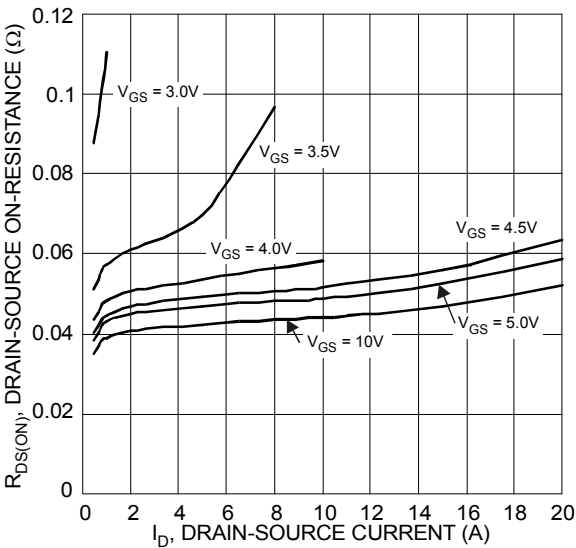


Figure 3 Typical On-Resistance vs. Drain Current and Gate Voltage

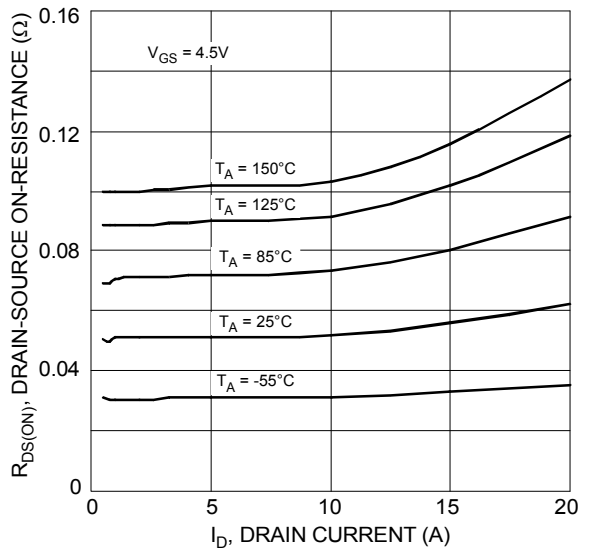


Figure 4 Typical On-Resistance vs. Drain Current and Temperature

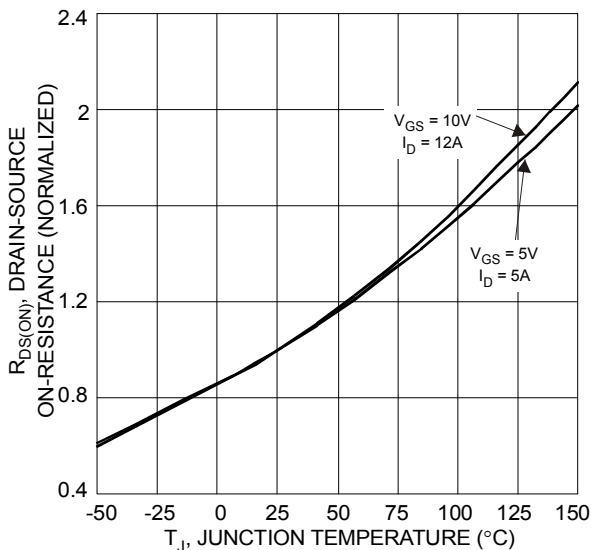


Figure 5 On-Resistance Variation with Temperature

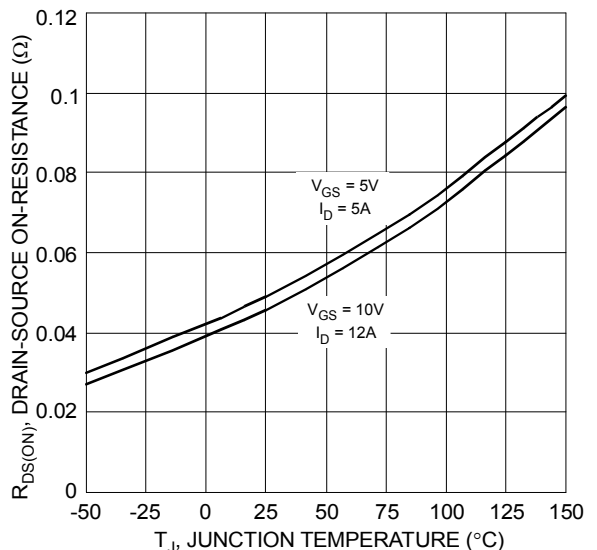


Figure 6 On-Resistance Variation with Temperature

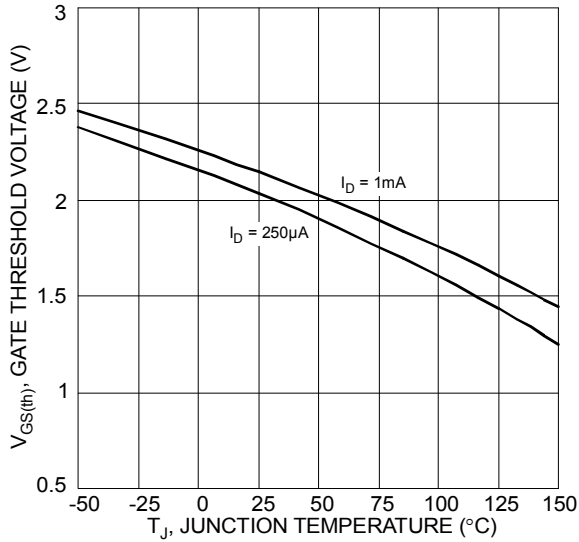


Figure 7 Gate Threshold Variation vs. Ambient Temperature

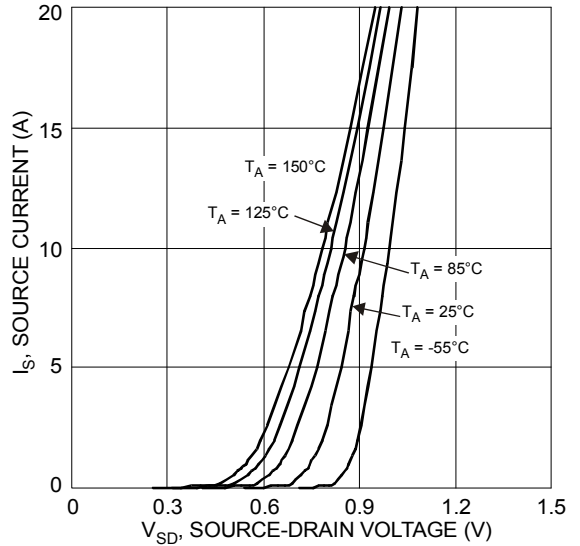


Figure 8 Diode Forward Voltage vs. Current

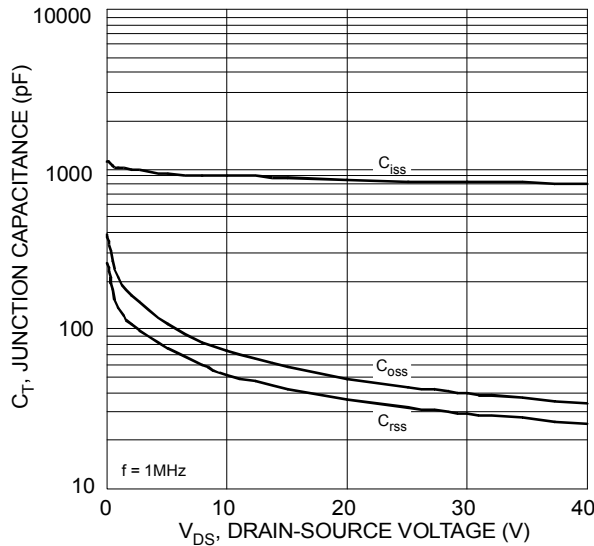


Figure 9 Typical Junction Capacitance

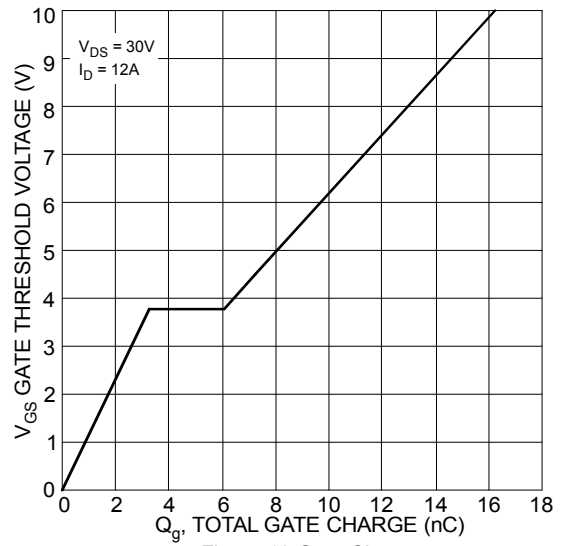


Figure 10 Gate Charge

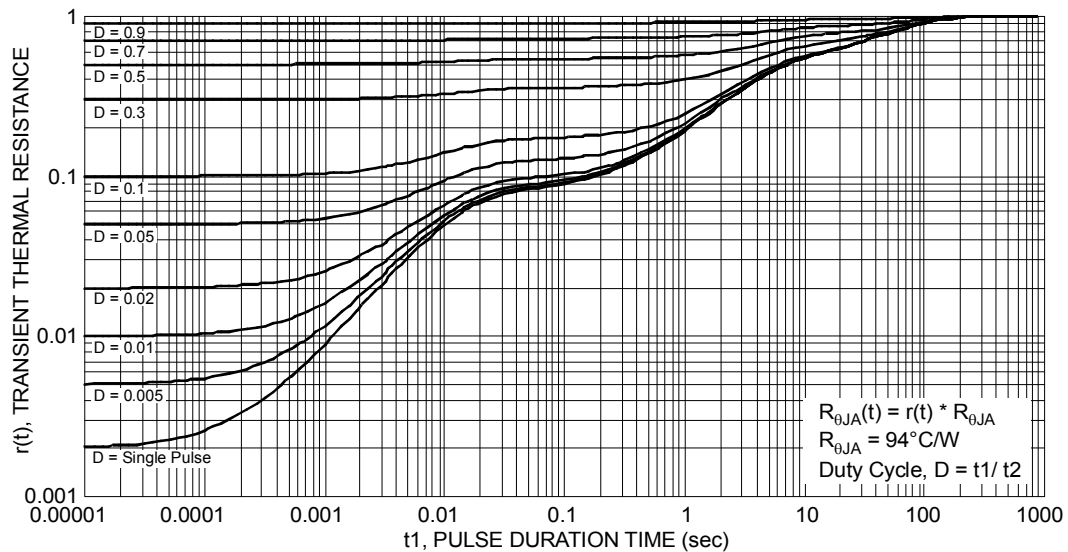
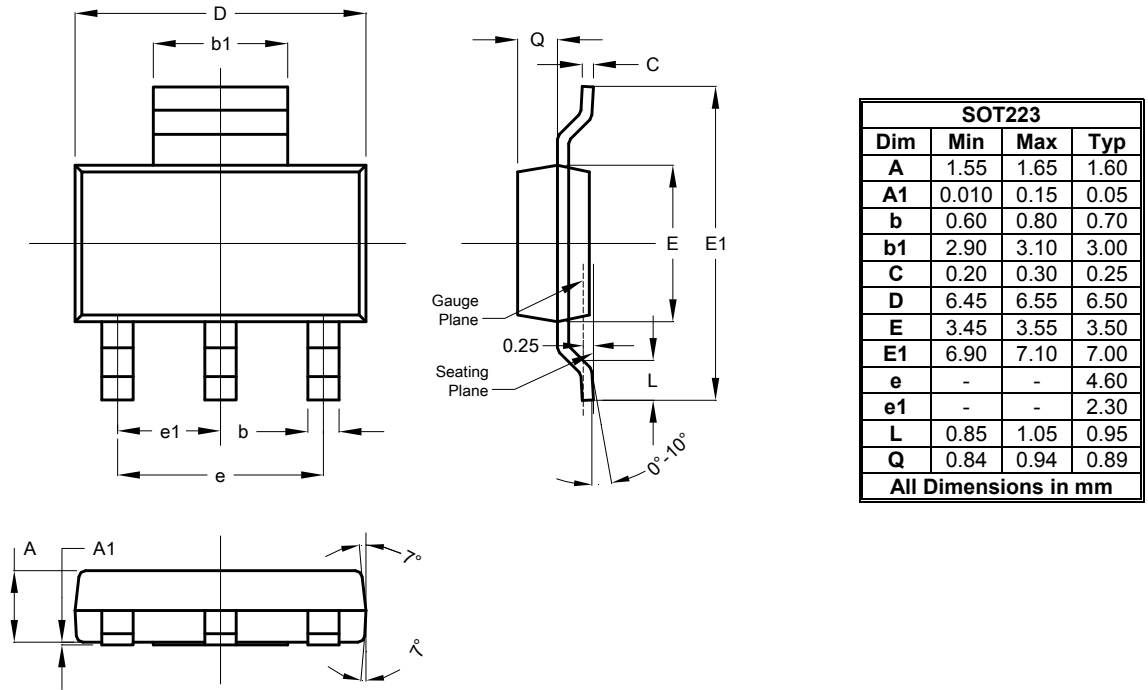


Figure 11 Transient Thermal Resistance

$R_{\theta JA}(t) = r(t) * R_{\theta JA}$   
 $R_{\theta JA} = 94^{\circ}\text{C/W}$   
 Duty Cycle,  $D = t1 / t2$

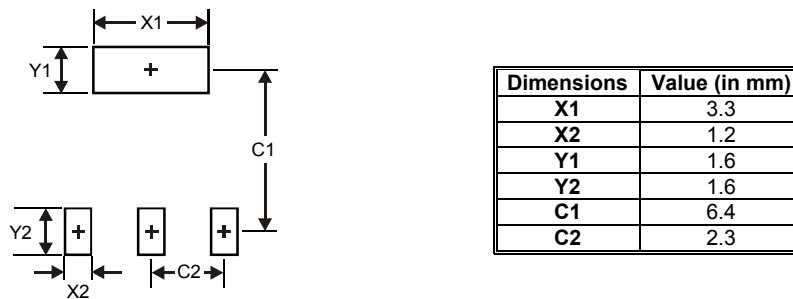
**Package Outline Dimensions**

Please see AP02002 at <http://www.diodes.com/datasheets/ap02002.pdf> for latest version.



**Suggested Pad Layout**

Please see AP02001 at <http://www.diodes.com/datasheets/ap02001.pdf> for the latest version.



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#### Как с нами связаться

**Телефон:** 8 (812) 309 58 32 (многоканальный)

**Факс:** 8 (812) 320-02-42

**Электронная почта:** [org@eplast1.ru](mailto:org@eplast1.ru)

**Адрес:** 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.