

DMP21D0UT

20V P-CHANNEL ENHANCEMENT MODE MOSFET

Product Summary

$V_{(BR)DSS}$	$R_{DS(on) Max}$	$I_D Max$ @ $T_A = 25^\circ C$ (Note 4)
-20V	495m Ω @ $V_{GS} = -4.5V$	-0.59A
	690m Ω @ $V_{GS} = -2.5V$	-0.50A
	960m Ω @ $V_{GS} = -1.8V$	-0.42A

Description and Applications

This MOSFET has been designed to minimize the on-state resistance ($R_{DS(on)}$) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

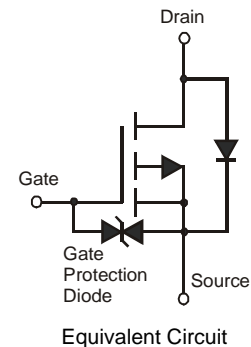
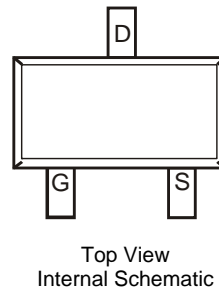
- Portable electronics

Features and Benefits

- Footprint of just 3mm² – less than half the size of SOT23
- 0.8mm profile – ideal for low profile applications
- Low Gate Threshold Voltage
- Fast Switching Speed
- **ESD Protected Gate 3kV**
- **Totally Lead-Free & Fully RoHS compliant (Note 1)**
- **Halogen and Antimony Free. "Green" Device (Note 2)**
- **Qualified to AEC-Q101 Standards for High Reliability**

Mechanical Data

- Case: SOT523
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Matte Tin Finish ; Solderable per MIL-STD-202, Method 208
- Weight: 0.002 grams (approximate)

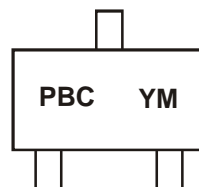


Ordering Information (Note 3)

Part Number	Marking	Reel size (inches)	Tape width (mm)	Quantity per reel
DMP21D0UT-7	PBC	7	8	3,000

- Notes:
1. EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant. No purposely added lead. Halogen and Antimony free.
 2. Diodes Inc's "Green" policy can be found on our website at <http://www.diodes.com>.
 3. For packaging details, go to our website at <http://www.diodes.com>.

Marking Information



PBC = Product Type Marking Code
 YM = Date Code Marking
 Y = Year (ex: Y = 2011)
 M = Month (ex: 9 = September)

Date Code Key

Year	2011	2012	2013	2014	2015	2016	2017
Code	Y	Z	A	B	C	D	E

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

Maximum Ratings @T_A = 25°C unless otherwise specified

Characteristic			Symbol	Value	Unit
Drain-Source Voltage			V _{DSS}	-20	V
Gate-Source Voltage			V _{GSS}	±8	V
Continuous Drain Current	Steady State	T _A = 25°C (Note 4)	I _D	-0.59	A
		T _A = 85°C (Note 4)		-0.42	
		T _A = 25°C (Note 5)		-0.65	
Pulsed Drain Current (Note 6)			I _{DM}	-5.0	A

Thermal Characteristics @T_A = 25°C unless otherwise specified

Characteristic			Symbol	Value	Unit
Power Dissipation (Note 4)			P _D	0.24	W
Power Dissipation (Note 5)			P _D	0.33	W
Thermal Resistance, Junction to Ambient (Note 4)			R _{θJA}	525	°C/W
Thermal Resistance, Junction to Ambient (Note 5)			R _{θJA}	383	°C/W
Operating and Storage Temperature Range			T _J , T _{STG}	-55 to +150	°C

- Notes:
- Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout
 - Device mounted on 25mm X 25mm FR-4 PCB with high coverage of 2oz copper
 - Device mounted on minimum recommended pad layout test board, 10μs pulse duty cycle = 1%.

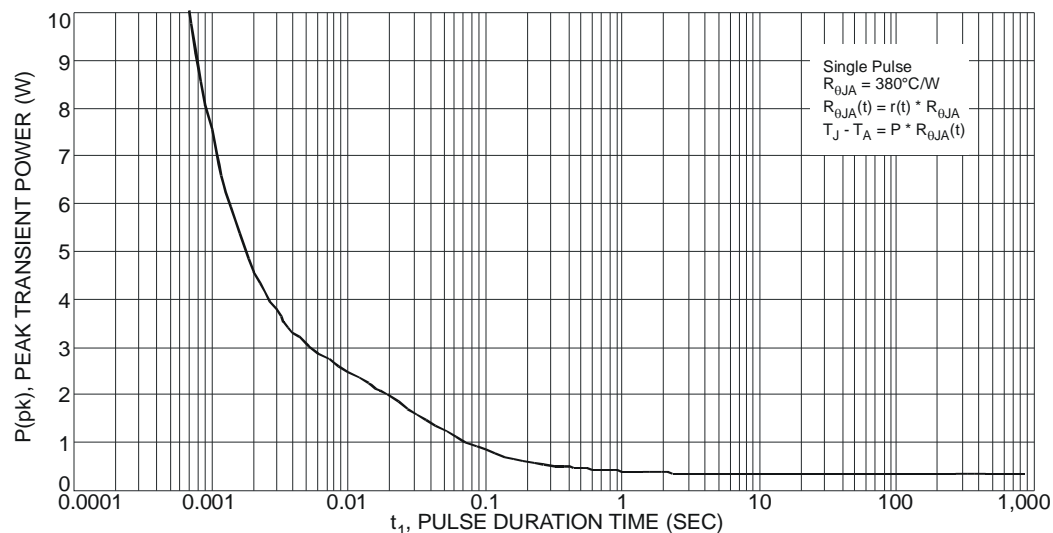


Fig. 1 Single Pulse Maximum Power Dissipation

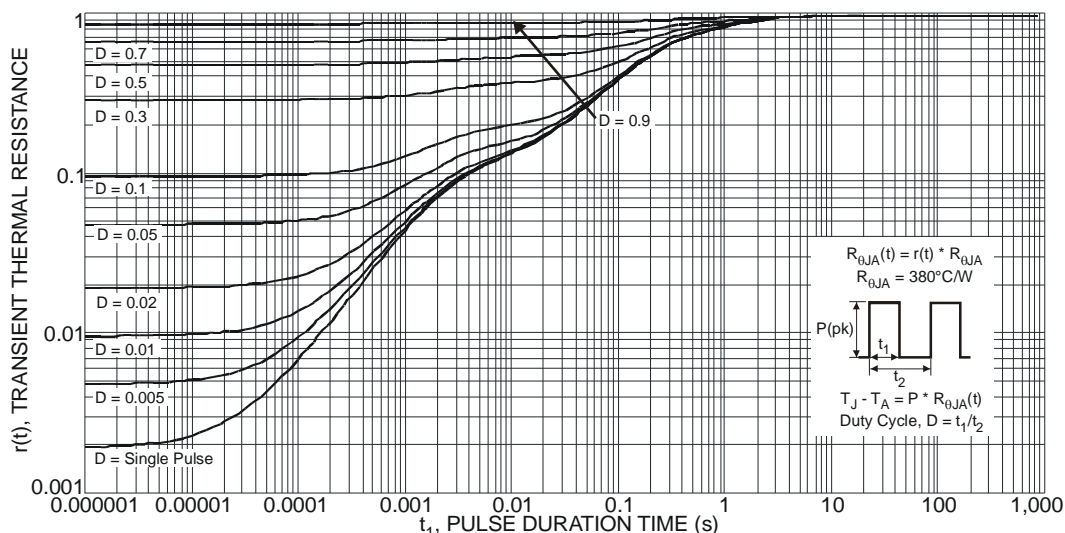
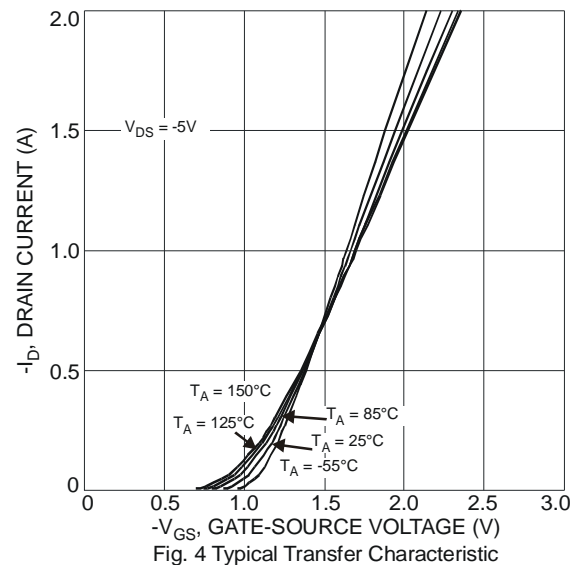
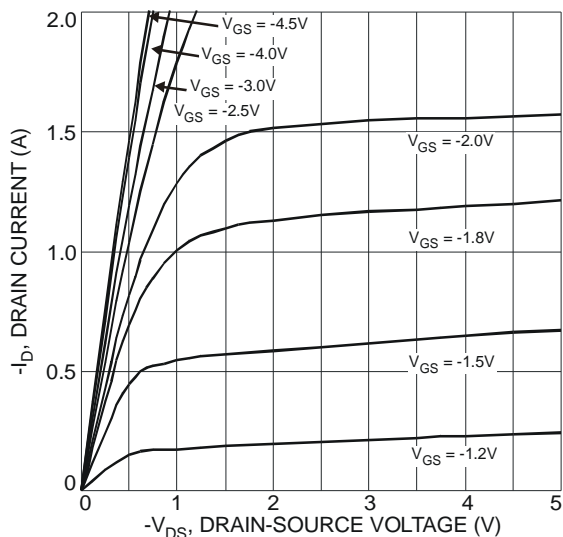


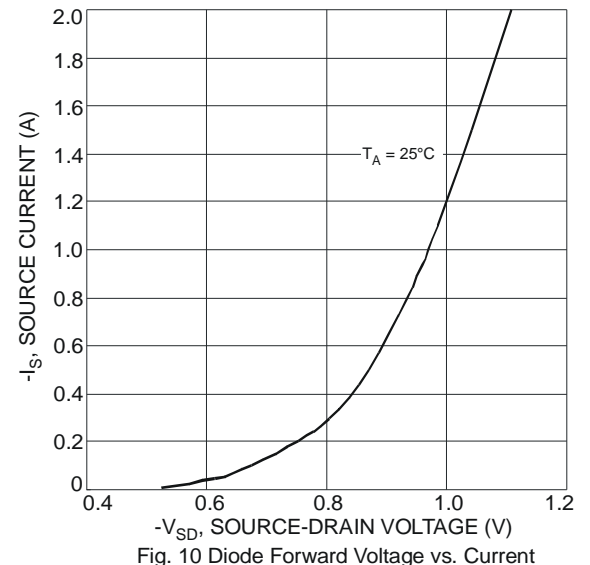
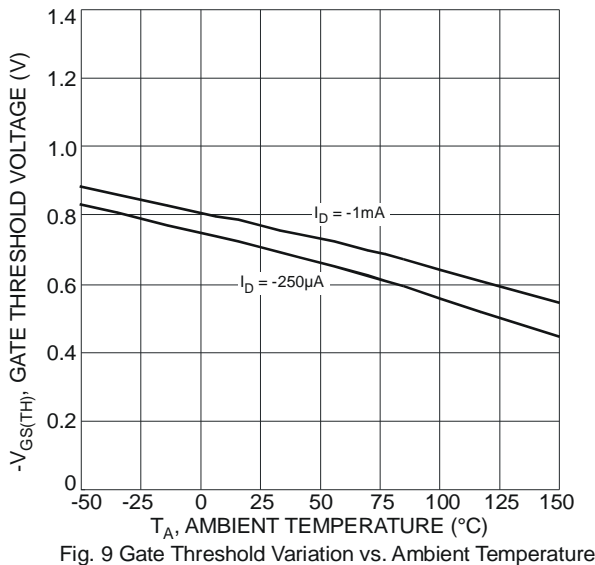
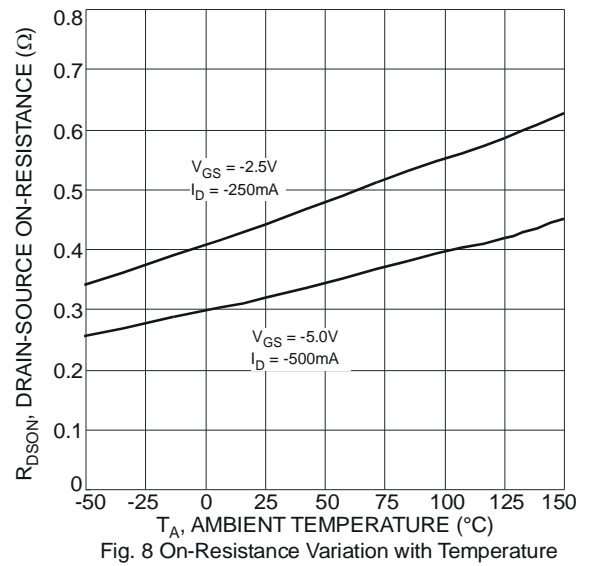
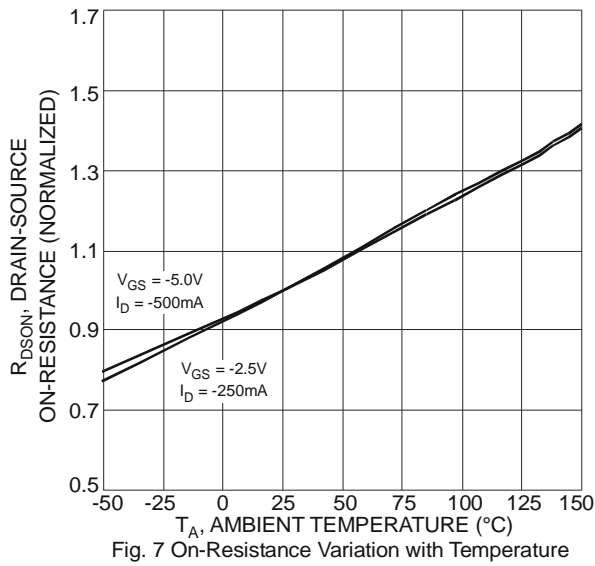
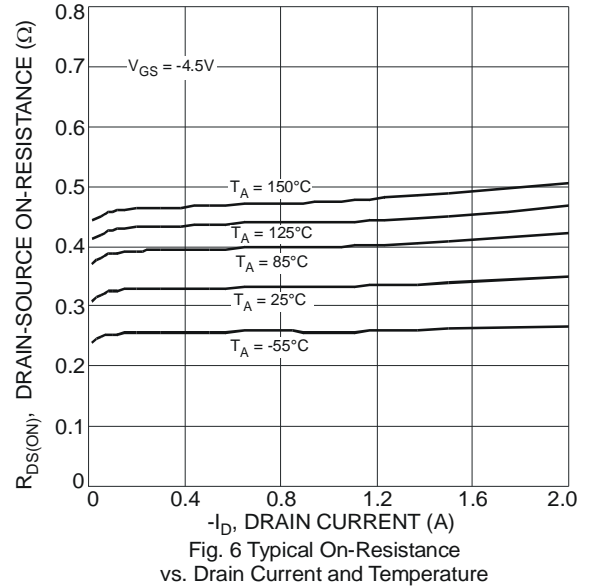
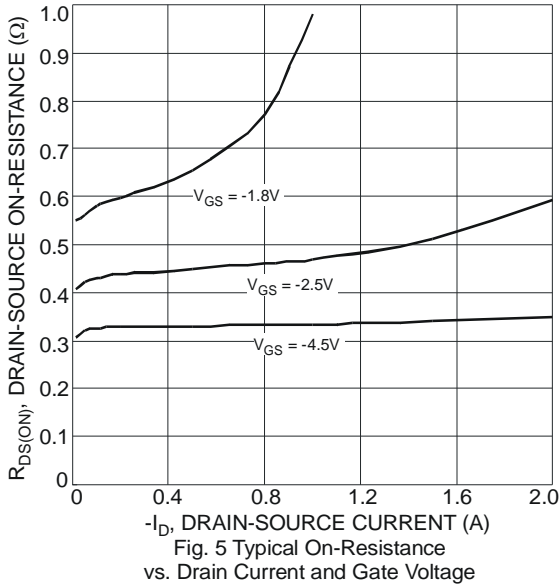
Fig. 2 Transient Thermal Response

Electrical Characteristics @ $T_A = 25^\circ\text{C}$ unless otherwise specified

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV_{DSS}	-20	-	-	V	$V_{GS} = 0V, I_D = -250\mu A$
Zero Gate Voltage Drain Current $T_J = 25^\circ\text{C}$	I_{DSS}	-	-	-1	μA	$V_{DS} = -20V, V_{GS} = 0V$
Gate-Source Leakage	I_{GSS}	-	-	± 10	μA	$V_{GS} = \pm 8V, V_{DS} = 0V$
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	$V_{GS(th)}$	-	-0.7	-	V	$V_{DS} = V_{GS}, I_D = -250\mu A$
Static Drain-Source On-Resistance	$R_{DS(on)}$	-	-	495	m Ω	$V_{GS} = -4.5V, I_D = -400mA$
				690		$V_{GS} = -2.5V, I_D = -300mA$
				960		$V_{GS} = -1.8V, I_D = -100mA$
Forward Transfer Admittance	$ Y_{fs} $	50	-	-	mS	$V_{DS} = -3V, I_D = -300mA$
Diode Forward Voltage	V_{SD}	-	-	-1.2	V	$V_{GS} = 0V, I_S = -300mA$
DYNAMIC CHARACTERISTICS						
Input Capacitance	C_{iss}	-	76.5	-	pF	$V_{DS} = -10V, V_{GS} = 0V,$ $f = 1.0MHz$
Output Capacitance	C_{oss}	-	13.7	-	pF	
Reverse Transfer Capacitance	C_{rss}	-	10.7	-	pF	
Gate Resistance	R_g	-	195	-	Ω	$V_{DS} = 0V, V_{GS} = 0V, f = 1MHz$
Total Gate Charge	Q_g	-	1.5	-	nC	$V_{GS} = -8V, V_{DS} = -15V, I_D = -1A$
Total Gate Charge	Q_g	-	1.0	-	nC	$V_{GS} = -4.5V, V_{DS} = -15V,$ $I_D = -1A$
Gate-Source Charge	Q_{gs}	-	0.2	-	nC	
Gate-Drain Charge	Q_{gd}	-	0.3	-	nC	
Turn-On Delay Time	$t_{D(on)}$	-	7.1	-	ns	$V_{DS} = -10V, -I_D = 1A$ $V_{GS} = -4.5V, R_G = 6\Omega$
Turn-On Rise Time	t_r	-	8.0	-	ns	
Turn-Off Delay Time	$t_{D(off)}$	-	31.7	-	ns	
Turn-Off Fall Time	t_f	-	18.5	-	ns	

Notes: 7. Short duration pulse test used to minimize self-heating effect.





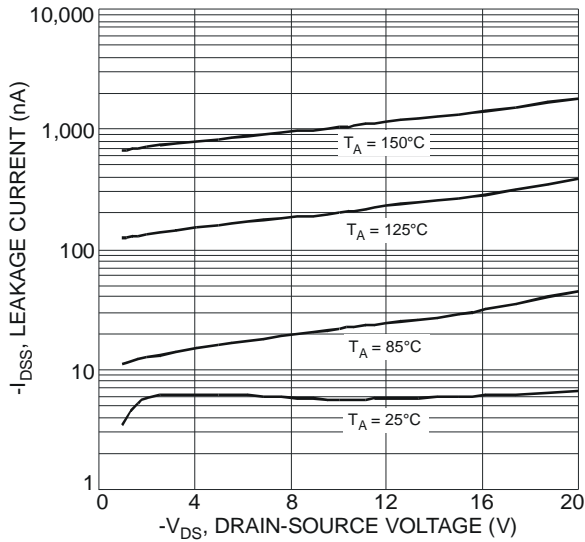


Fig. 11 Typical Leakage Current vs. Drain-Source Voltage

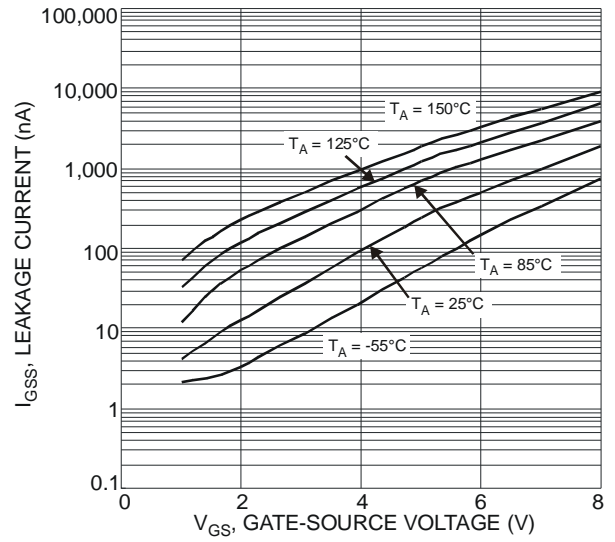


Fig. 12 Leakage Current vs. Gate-Source Voltage

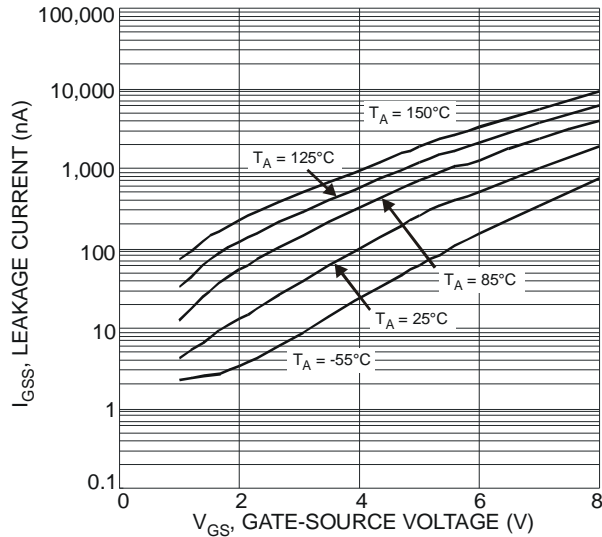


Fig. 13 Leakage Current vs. Gate-Source Voltage

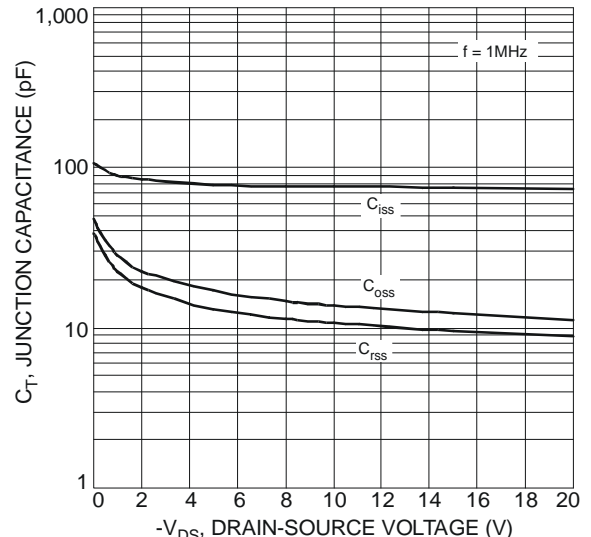


Fig. 14 Typical Junction Capacitance

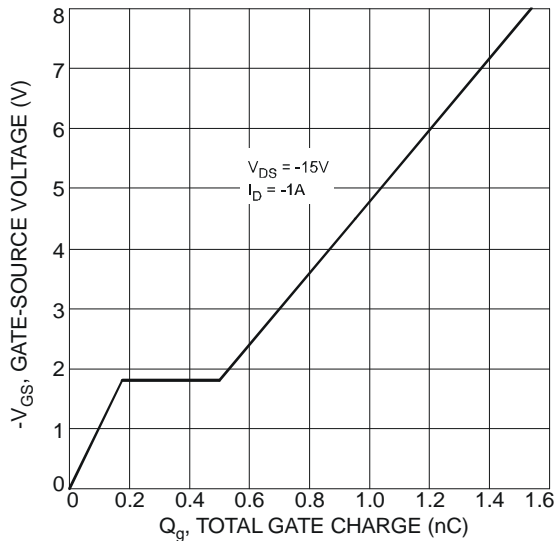
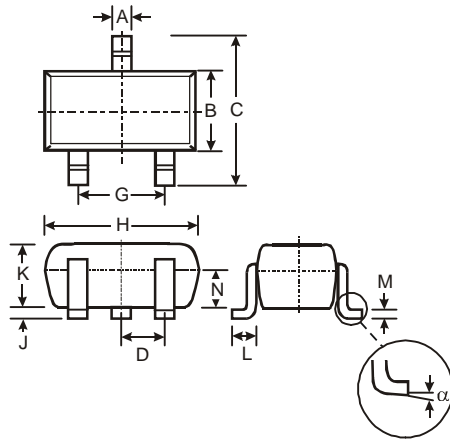


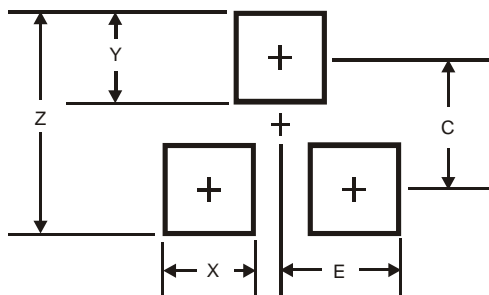
Fig. 15 Gate-Charge Characteristics

Package Outline Dimensions



SOT523			
Dim	Min	Max	Typ
A	0.15	0.30	0.22
B	0.75	0.85	0.80
C	1.45	1.75	1.60
D	—	—	0.50
G	0.90	1.10	1.00
H	1.50	1.70	1.60
J	0.00	0.10	0.05
K	0.60	0.80	0.75
L	0.10	0.30	0.22
M	0.10	0.20	0.12
N	0.45	0.65	0.50
α	0°	8°	—
All Dimensions in mm			

Suggested Pad Layout



Dimensions	Value (in mm)
Z	1.8
X	0.4
Y	0.51
C	1.3
E	0.7

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Как с нами связаться

Телефон: 8 (812) 309 58 32 (многоканальный)

Факс: 8 (812) 320-02-42

Электронная почта: org@eplast1.ru

Адрес: 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.