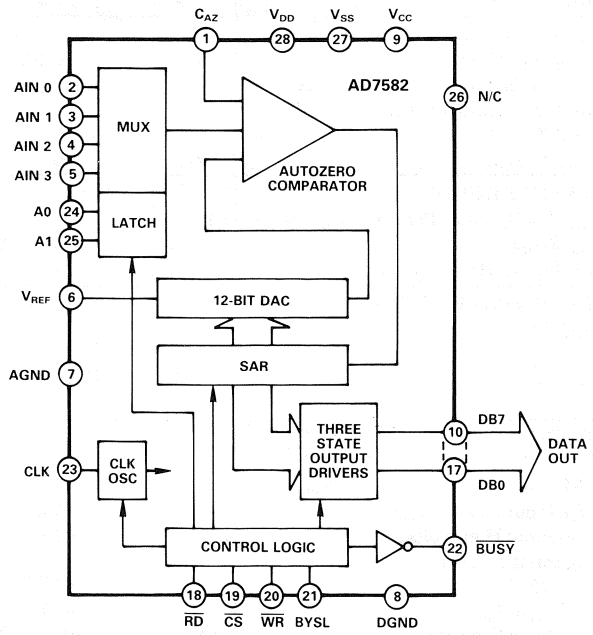
CMOS 12-Bit Successive Approximation ADC

AD7582

FEATURES

12-Bit Successive Approximation ADC
Four High Impedance Input Channels
Analog Input Voltage Range of 0 to +5V with Positive Reference of +5V
Conversion Time of 100μs per Channel
No Missed Codes Over Full Temperature Range
Low Total Unadjusted Error ±1LSB max
Autozero Cycle for Low Offset Voltage
Monolithic Construction

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7582 is a medium speed, 4-channel 12-bit CMOS A/D converter which uses the successive approximation technique to provide a conversion time of 100μs per channel. An auto-zero cycle occurs at the start of each conversion resulting in very low system offset voltages, typically less than 100μV. The device is designed for easy microprocessor interface using standard control signals; $\overline{CS}$ (decoded device address), $\overline{RD}$ ($\overline{READ}$) and $\overline{WR}$ ($\overline{WRITE}$). The 4-channel input multiplexer is controlled via address inputs A0 and A1.

Conversion results are available in two bytes, 8LSB's and 4MSB's, over an 8-bit three state output bus. Either byte can be read first. Two converter busy flags are available to facilitate polling of the converter's status.

The analog input voltage range is 0V to +5V when using a reference voltage of +5V. The four analog inputs are all high impedance inputs with tight channel-to-channel matching–typically 0.1LSBs.

PRODUCT HIGHLIGHTS

1. The AD7582 is a complete 4 channel 12-bit A/D converter in either a 28-pin DIP or 28-terminal surface mount package requiring only a few passive components and a voltage reference.
2. Autozero cycle realizes very low offset voltages, typically 100μV.
3. The four channel input multiplexer (user addressable) features high input impedance and excellent channel-to-channel matching.
4. Standard microprocessor control signals to allow easy interfacing to most popular 8- and 16-bit microprocessors.

REV. B

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AD7582—SPECIFICATIONS (V_{DD} = +15V, V_{CC} = +5V, V_{SS} = −5V, V_{REF} = +5.0V f_{CLK} = 140kHz external, all specifications T_{MIN} to T_{MAX} unless otherwise noted)

Parameter	K Version[1]	B Version[1]	T Version[1]	Units	Conditions/Comments
ACCURACY					
Resolution	12	12	12	Bits	
Total Unadjusted Error[2]	±1	±1	±1	LSB max	All channels, AIN0–AIN3
Differential Nonlinearity	±1	±1	±1	LSB max	No missing codes guaranteed
Full Scale Error (Gain Error)[3]	±1/4	±1/4	±1/4	LSB max	All channels, AIN0–AIN3 Full Scale TC is typically 5ppm/°C
Offset Error[3]	±1/4	±1/4	±1/4	LSB max	All channels, AIN0–AIN3 Offset Error TC is typically 5ppm/°C
Channel to Channel Mismatch[3]	±1/4	±1/4	±1/4	LSB max	
ANALOG INPUTS					
Analog Input Range	0 to +5	0 to +5	0 to +5	V	V_{REF} = +5.0V
C_{AIN}, On Channel Input Capacitance	8	8	8	pF typ	
I_{AIN}, Input Leakage Current					AIN0–AIN3; 0 to +5V
+25°C	10	10	10	nA max	
T_{min} to T_{max}	100	100	100	nA max	
REFERENCE INPUT					
V_{REF} (For Specified Performance)	+5	+5	+5	V	±5%
V_{REF} Range	+4 to +6	+4 to +6	+4 to +6	V	Degraded transfer accuracy
V_{REF} Input Reference Current	1.0	1.0	1.0	mA max	V_{REF} = +5.0V
POWER SUPPLY REJECTION					
V_{DD} Only	±1/8	±1/8	±1/8	LSB typ	V_{DD} = +14.25V to +15.75V V_{SS} = −5V
V_{SS} Only	±1/8	±1/8	±1/8	LSB typ	V_{SS} = −4.75V to −5.25V V_{DD} = +15V
LOGIC INPUTS					
$\overline{RD}$ (Pin 18), $\overline{CS}$ (Pin 19), $\overline{WR}$ (Pin 20)					
BYSL (Pin 21), A0 (Pin 24), A1 (Pin 25)					
V_{IL} Input Low Voltage	+0.8	+0.8	+0.8	V max	V_{CC} = +5V ±5%
V_{IH} Input High Voltage	+2.4	+2.4	+2.4	V min	
I_{IN} Input Current					
+25°C	±1	±1	±1	μA max	V_{IN} = 0 to V_{CC}
T_{min} to T_{max}	+10	+10	+10	μA max	
C_{IN} Input Capacitance[3]	10	10	10	pF max	
CLK (Pin 23)					
V_{IL}, Input Low Voltage	+0.8	+0.8	+0.8	V max	V_{CC} = +5V ±5%
V_{IH}, Input High Voltage	+3.0	+3.0	+3.0	V min	
I_{IL}, Input Low Current	±10	±10	±10	μA max	
I_{IH}, Input High Current	+1.5	+1.5	+1.5	mA max	
LOGIC OUTPUTS					
DB0–DB7 (Pins 10–17), $\overline{BUSY}$ (Pin 22)[4]					
V_{OL}, Output Low Voltage	+0.4	+0.4	+0.4	V max	V_{CC} = +5V ±5%, I_{SINK} = 1.6mA[4]
V_{OH}, Output High Voltage	+4.0	+4.0	+4.0	V min	V_{CC} = +5V ±5%, I_{SOURCE} = 200μA
Floating State Leakage Current					
(Pins 10–17)	±1	±1	±1	μA max	V_{OUT} = 0V to V_{CC}
Floating State Output Capacitance	15	15	15	pF max	
CONVERSION TIME[5]					
With External Clock	100	100	100	μs min	f_{CLK} = 140kHz
With Internal Clock, T_A = +25°C	50/100	50/100	50/100	μs min/max	Using recommended clock components as shown in Figure 6.
POWER REQUIREMENTS[6]					
V_{DD}	+15	+15	+15	V NOM	±5% for specified performance
V_{SS}	−5	−5	−5	V NOM	±5% for specified performance
V_{CC}	+5	+5	+5	V NOM	±5% for specified performance
I_{DD}	7.5	7.5	7.5	mA max	Typically 4mA with V_{DD} = +15V
I_{SS}	7.5	7.5	7.5	mA max	Typically 3mA with V_{SS} = −5V
I_{CC}	100	100	100	μA typ	V_{IN} = V_{IL} or V_{IH}
	1.0	1.0	1.0	mA max	
Power Dissipation	75	75	75	mW typ	$\overline{WR}$ = $\overline{RD}$ = $\overline{CS}$ = $\overline{BUSY}$ = Logic HIGH

NOTES
[1]Temperature Range as follows: K, B Versions; −40°C to +85°C
T Version; −55°C to +125°C
[2]Includes Full Scale Error, Offset Error and Relative Accuracy.
[3]Guaranteed by Design, not Production tested.
[4]I_{SINK} for $\overline{BUSY}$ (pin 22) is 1.0 milliamp.
[5]Conversion Time includes autozero cycle time.
[6]Power supply current is measured when AD7582 is inactive i.e., $\overline{WR}$ = $\overline{RD}$ = $\overline{CS}$ = $\overline{BUSY}$ = Logic HIGH.
Specifications subject to change without notice.

TIMING SPECIFICATIONS[1] (V_{DD} = +15V, V_{CC} = +5V, V_{SS} = −5V, V_{REF} = +5V)

Parameter	Limit at +25°C (All Grades)	Limit at T_{min}, T_{max} (K & B Grades)	Limit at T_{min}, T_{max} (T Grade)	Units	Conditions/Comments
t_1	0	0	0	ns min	$\overline{CS}$ to $\overline{WR}$ Setup Time
t_2 (INT)[2]	200	240	280	ns min	$\overline{WR}$ Pulse Width (Internal Clock Operation)
t_2 (EXT)[2]	10	10	10	μs min	$\overline{WR}$ Pulse Width (External Clock Operation)
t_3	0	0	0	ns min	$\overline{CS}$ to $\overline{WR}$ Hold Time
t_4	130	160	200	ns typ	
	200	250	300	ns max	$\overline{WR}$ to $\overline{BUSY}$ Propagation Delay
t_5	0	0	0	ns min	A0, A1 Valid to $\overline{WR}$ Setup Time
t_6	20	20	20	ns min	A0, A1 Valid to $\overline{WR}$ Hold Time
t_7	0	0	0	ns min	$\overline{BUSY}$ to $\overline{CS}$ Setup Time
t_8	0	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Setup Time
t_9	200	240	280	ns min	$\overline{RD}$ Pulse Width
t_{10}	0	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Hold Time
t_{11}	50	50	50	ns min	BYSL to $\overline{RD}$ Setup Time
t_{12}	0	0	0	ns min	BYSL to $\overline{RD}$ Hold Time
t_{13}[3]	150	180	200	ns typ	
	200	240	280	ns max	$\overline{RD}$ to Valid Data (Bus Access Time)
t_{14}[4]	20	20	20	ns min	$\overline{RD}$ to Three State Output
	130	150	150	ns max	(Bus Relinquish Time)

NOTES
[1]Timing Specifications are guaranteed by Design, not Production tested. All input control signals are specified with $t_r = t_f$ = 20ns (10% to 90% of +5V) and timed from a voltage level of +1.6V. Data is timed from V_{IH}, V_{IL} or V_{OH}, V_{OL}.
[2]When using an external clock source the $\overline{WR}$ pulse width must be extended to provide the minimum auto-zero cycle time of 10μs. See "External Clock Operation".
[3]t_{13} is measured with the load circuits of Figure 3 and defined as the time required for an output to cross 0.8V or 2.4V.
[4]t_{14} is defined as the time required for the data lines to change 0.5V when loaded with the circuits of Figure 4.
Specifications subject to change without notice.

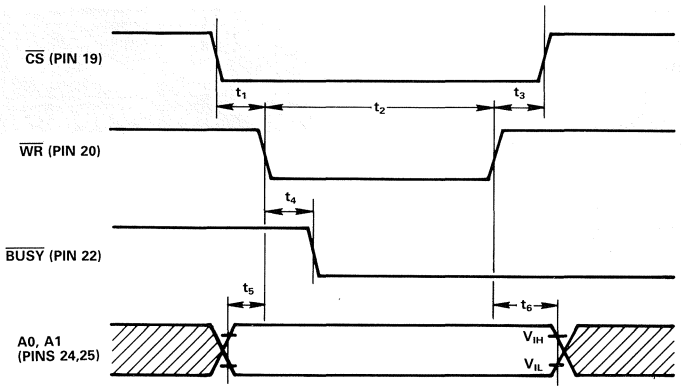


Figure 1. Start Cycle Timing

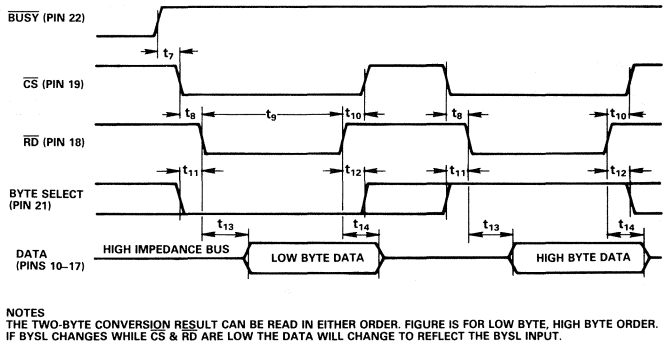
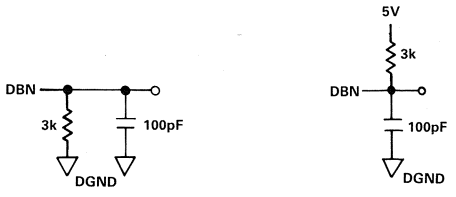
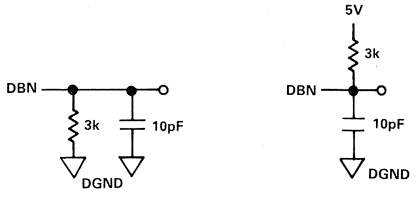


Figure 2. Read Cycle Timing



a. High-Z to V_{OH} *b. High-Z to V_{OL}*

Figure 3. Load Circuits for Access Time Test (t_{13})



a. V_{OH} to High-Z *b. V_{OL} to High-Z*

Figure 4. Load Circuits for Output Float Delay Test (t_{14})

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise stated)

V_{DD} to DGND . . . . . −0.3V, +17V
V_{SS} to DGND . . . . . +0.3V, −7V
AGND to DGND . . . . . −0.3V, V_{REF} +0.3V
V_{CC} to DGND . . . . . −0.3V, V_{DD} +0.3V
V_{REF} to AGND . . . . . −0.3V, V_{DD} +0.3V
AIN (0-3) to AGND . . . . . −0.3V, V_{DD} +0.3V
Digital Input Voltage to DGND
(Pins 18-21, 23-25) . . . . . −0.3V, V_{DD} +0.3V
Digital Output Voltage to DGND
(Pins 10-17, 22) . . . . . −0.3V, V_{DD} +0.3V
Operating Temperature Range
Commercial (K Version) . . . . . −40°C to +85°C
Industrial (B Version) . . . . . −40°C to +85°C
Extended (T Version) . . . . . −55°C to +125°C
Storage Temperature . . . . . −65°C to +150°C
Junction Temperature . . . . . +150°C
DIP Package, Power Dissipation 875mW
θ_{JA} Thermal Impedance . . . . . 75°C/W
Lead Temperature, Soldering (10sec) . . . . . +260°C
Cerdip Package, Power Dissipation 1000mW
θ_{JA} Thermal Impedance . . . . . 51°C/W
Lead Temperature, Soldering (10sec) . . . . . +300°C
PLCC Package, Power Dissipation 500mW
θ_{JA} Thermal Impedance . . . . . 80°C/W
Lead Temperature, Soldering
Vapor Phase (60sec) . . . . . +215°C
Infrared (15sec) . . . . . +210°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model[1]	Temperature Range	Total Unadjusted Error T_{MIN} –T_{MAX}	Package Option[2]
AD7582KN	−40°C to +85°C	±1LSB	N-28
AD7582BQ	−40°C to +85°C	±1LSB	Q-28
AD7582TQ	−55°C to +125°C	±1LSB	Q-28
AD7582KP	−40°C to +85°C	±1LSB	P-28A

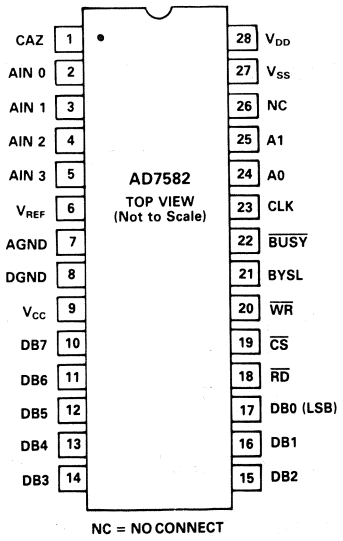
NOTES
[1]To order MIL-STD-883, Class B processed parts, add /883B to part number. Contact your local sales office for military data sheet.
[2]N = Plastic DIP; Q = Cerdip, P = Plastic Leaded Chip Carrier.

CAUTION

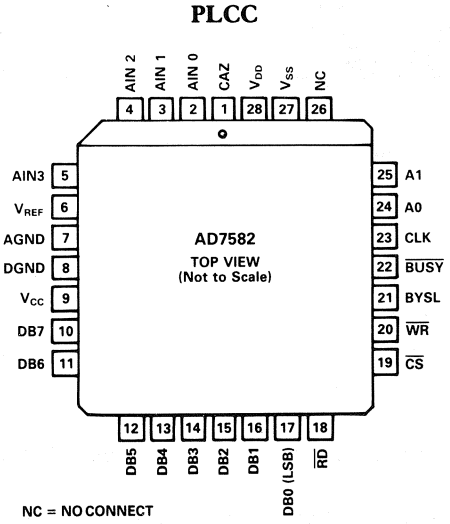
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V, which readily accumulate on the human body and on test equipment, can discharge without detection. Although these devices feature proprietary ESD protection circuitry, permanent damage may still occur on these devices if they are subjected to high energy electrostatic discharges. Therefore, proper precautions are recommended to avoid any performance degradation or loss of functionality.

PIN CONFIGURATIONS

DIP



PLCC



PIN FUNCTION DESCRIPTION

PIN	MNEMONIC	DESCRIPTION
1	CAZ	Autozero Capacitor Input. Connect other side of capacitor to AGND.
2	AIN 0	Analog Input, channel 0
3	AIN 1	Analog Input, channel 1
4	AIN 2	Analog Input, channel 2
5	AIN 3	Analog Input, channel 3
6	V_{REF}	Voltage reference input. The AD7582 is specified with $V_{REF} = +5.0V$.
7	AGND	Analog Ground
8	DGND	Digital Ground
9	V_{CC}	Logic Supply. For $V_{CC} = +5V$ digital inputs and outputs are TTL compatible.
10-17		Three state data outputs. They become active when $\overline{CS}$ & $\overline{RD}$ are brought low. Individual pin function is dependent upon the Byte Select (BYSL) input.

DATA BUS OUTPUT, $\overline{CS}$ & $\overline{RD}$ = LOW

	BYSL = HIGH	BYSL = LOW
Pin 10	BUSY[1]	DB7
Pin 11	LOW[2]	DB6
Pin 12	LOW[2]	DB5
Pin 13	LOW[2]	DB4
Pin 14	DB11 (MSB)	DB3
Pin 15	DB10	DB2
Pin 16	DB9	DB1
Pin 17	DB8	DB0 (LSB)

[1]BUSY (Pin 10) is a converter status flag and is HIGH during a conversion.
[2]Pins 11-13 output a logic LOW when BYSL is HIGH.
DB11–DB0 are the 12-bit conversion results, DB11 is the MSB.

18	$\overline{RD}$	READ input. This active LOW signal, in combination with $\overline{CS}$, is used to enable the output data three-state drivers.
19	$\overline{CS}$	CHIP SELECT Input. Decoded device address, active LOW. Used in combination with either $\overline{RD}$ or $\overline{WR}$ for control.
20	$\overline{WR}$	WRITE Input. This active LOW signal, in combination with $\overline{CS}$, is used to start a new conversion on a selected channel. When the AD7582 internal clock is used, the minimum $\overline{WR}$ pulse width is t2 (INT). When an external clock source is used, the minimum $\overline{WR}$ pulse width must be extended to include the autozero cycle time. For external clock operation, the minimum $\overline{WR}$ pulse width is t2 (EXT).
21	BYSL	BYTE SELECT. This control input determines whether the high or low byte of data is placed on the output data bus during a data READ operation ($\overline{CS}$ & $\overline{RD}$ LOW). See description of pins 10-17.
22	$\overline{BUSY}$	$\overline{BUSY}$ indicates converter status. $\overline{BUSY}$ is LOW during conversion, otherwise $\overline{BUSY}$ is held at a logic HIGH.
23	CLK	CLOCK Input for internal/external clock operation. Internal : Connect R_{CLK} and C_{CLK1}/C_{CLK2} timing components. See Figure 6 and Figure 7. External : Connect external 74HC compatible clock source as shown in Figure 8.
24	AO	Address Input AO. See pin 25 description.
25	A1	Address Input A1. Address inputs AO and A1 select the input channel to be converted. The address input latch is transparent when $\overline{CS}$ & $\overline{WR}$ are LOW. The address inputs are latched by $\overline{WR}$ returning HIGH.

A1	A0	CHANNEL SELECTED
0	0	AIN 0
0	1	AIN 1
1	0	AIN 2
1	1	AIN 3

26	N/C	No connect pin.
27	V_{SS}	Negative supply, −5V.
28	V_{DD}	Positive supply, +15V.

Operating Information

OPERATIONAL DIAGRAM

An operational diagram for the AD7582 is shown in Figure 5. The only passive components required are the autozero capacitor C_{AZ} and timing components R_{CLK}, C_{CLK1} & C_{CLK2} for the internal clock oscillator. If the AD7582 is to be used with an external clock source, then only C_{AZ} is required. Individual pin functions are described in detail on the previous page.

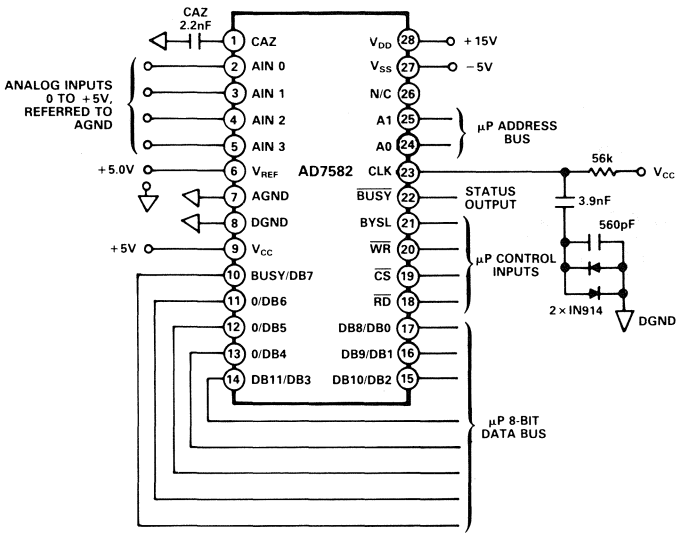


Figure 5. AD7582 Operational Diagram

INTERNAL CLOCK OPERATION

The clock circuitry for internal clock operation is shown in Figure 6 and the AD7582 operating waveforms are shown in Figure 7.

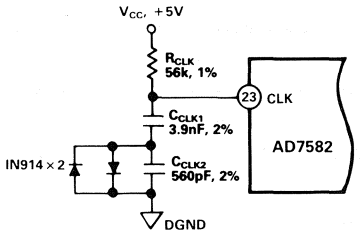
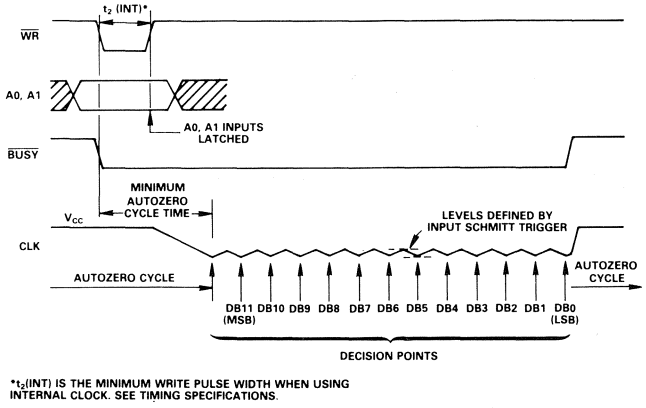


Figure 6. Circuitry Required for Internal Clock Operation



*t_2(INT) IS THE MINIMUM WRITE PULSE WIDTH WHEN USING INTERNAL CLOCK. SEE TIMING SPECIFICATIONS.

Figure 7. Operating Waveforms – Internal Clock

Between conversions ($\overline{BUSY}$ = HIGH) the AD7582 is in the autozero cycle. When $\overline{WR}$ goes LOW (with $\overline{CS}$ LOW) to start a new conversion, the input multiplexer is switched to the selected channel N, via address inputs A0, A1. The autozero capacitor C_{AZ} now charges to AIN N–V_{OS} where V_{OS} is the input offset voltage of the autozero comparator.

A minimum time of 10μs is required for this autozero cycle. In applications using the internal clock oscillator, it is not necessary for $\overline{WR}$ to remain LOW for this period of time since it is automatically provided by the AD7582. This is achieved by switching a constant current load across the clock capacitors, C_{CLK1} and C_{CLK2}, causing the voltage at the CLK input pin to slowly decay from V_{CC}. This occurs after $\overline{WR}$ returns HIGH; $\overline{WR}$ returning HIGH also latches the multiplexer address inputs A0, A1 (see Figure 7). The Schmitt trigger circuit monitoring the voltage on the CLK input ends the autozero cycle when its LOW input trigger level is reached. At this point, the constant current load across the clock capacitors is removed allowing them to charge towards V_{CC} via R_{CLK}. When the voltage at the CLK input reaches the HIGH trigger level, the constant current load is replaced across C_{CLK1} and C_{CLK2}. The MSB decision is made when the LOW trigger level is reached. This cycle repeats itself 12 times to provide 12 clock pulses for the conversion cycle. The circuit arrangement of Figure 6 provides the relatively slow autozero cycle time at the beginning of a conversion while allowing the clock oscillator to speed up once the autozero cycle is complete.

EXTERNAL CLOCK OPERATION

For external clock operation R_{CLK}, C_{CLK1} and C_{CLK2} are discarded and the CLK input is driven from a 74HC compatible clock source. The mark/space ratio of the external clock can vary from 40/60 to 60/40. The AD7582 $\overline{WR}$ pulse width must now be extended to provide the minimum autozero cycle time of 10μs since this is no longer provided automatically by the AD7582. Referring to the operating waveforms of Figure 9, the minimum $\overline{WR}$ pulse width when using an external clock source is t_2 (EXT). Multiplexer address inputs A0 and A1, in addition to the $\overline{CS}$ input must now remain valid for the external $\overline{WR}$ pulse width. One approach to stretching the available μP signals is shown in the general 8-bit μP interface circuit of Figure 20. It is not necessary to synchronize the external clock source with the extended $\overline{WR}$ pulse width, the MSB decision being made on the second falling edge of the clock input after the $\overline{WR}$ input returns HIGH.

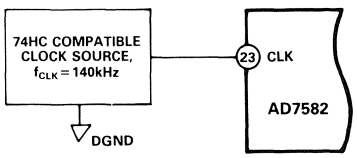


Figure 8. External Clock Operation

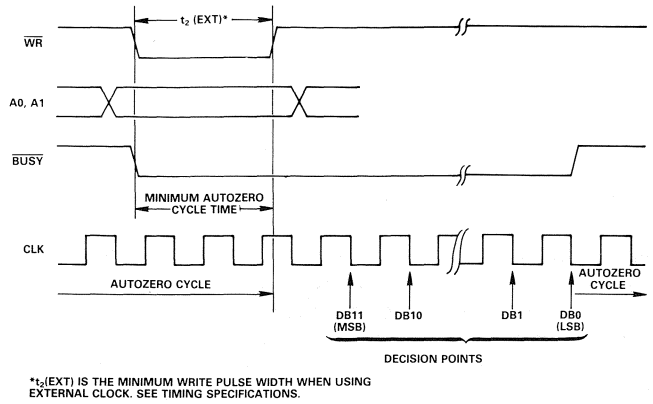


Figure 9. Operating Waveforms – External Clock

READING DATA

The 12-bit conversion data plus a converter status flag are available over an 8-bit wide data bus. Data is transferred from the AD7582 in right-justified format (i.e., the LSB is the most right-hand bit in a 16-bit word). Two READ operations are required, the Byte Select (BYSL) input determining which byte–8 least significant bits or 4 most significant bits plus status flag–is to be read first.

Since the AD7582 uses the successive approximation register (SAR) to hold conversion results (refer to Functional Diagram), it is necessary to wait until a conversion is finished before reading valid 12-bit data. Executing a READ instruction (HIGH or LOW byte) to the AD7582 while a conversion is in progress will place the existing contents of the SAR onto the data bus. Three different approaches can ensure valid 12-bit data is available for reading.

1. Insert a software delay greater than the ADC conversion time between the conversion start instruction and the data read instructions.
2. At user-defined intervals after a conversion start instruction, poll the internal converter status flag, BUSY. This signal is available on pin 10 during a HIGH byte READ instruction and is the most left-hand bit in a 16-bit right-justified word. The status bit can be shifted into a microprocessor's accumulator-carry position for testing (BUSY is HIGH during conversion).
3. Use the externally available $\overline{\text{BUSY}}$ (pin 22) signal as an interrupt to the microprocessor. This signal is LOW during a conversion and returns HIGH at conversion end.

Executing a WRITE instruction while conversion is in progress will restart the conversion.

COMPONENT SELECTION

1. Autozero Capacitor, C_{AZ}
   The autozero capacitor must be a low leakage, low dielectric absorption type such as polystyrene, polypropylene or teflon. To minimize noise connect the outside foil of C_{AZ} to AGND (pin 7), the analog system ground. C_{AZ} should be 2,200pF.
2. Clock Oscillator Components, R_{CLK}, C_{CLK1} and C_{CLK2}
   Clock pulses are generated by the action of series connected capacitors, C_{CLK1} and C_{CLK2} charging through an external resistor R_{CLK} and discharging through an internal switch. Nominal conversion time versus temperature for the recommended R_{CLK} and C_{CLK1}/C_{CLK2} combination is shown in Figure 10. Due to process variations, the actual operating frequency for this R_{CLK} and C_{CLK1}/C_{CLK2} combination can vary from device to device by up to 20%. For this reason, Analog Devices recommends using an external clock in the following situations:
   a. Applications requiring a conversion time which is within 20% of 100μs, the maximum conversion time for specified accuracy (a 140kHz clock frequency gives a 100μs conversion time).
   b. Applications which cannot accommodate conversion time differences which may occur due to unit clock frequency variations or temperature variations.

   It is possible to replace the fixed R_{CLK} resistor with a 50k potentiometer in series with a fixed 22kΩ resistor to allow individual adjustment of internal clock frequency. Reducing the value of R_{CLK} from 56k to 47k decreases the conversion time by typically 12μs.

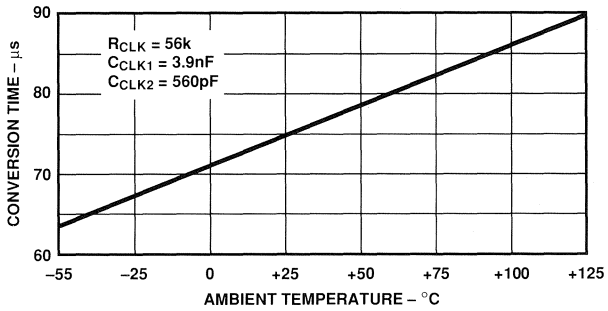


Figure 10. Typical Conversion Time vs. Temperature Using Internal Clock

APPLYING THE AD7582

The high input impedance of the analog channels, AIN0–AIN3, allows simple analog interfacing. Zero to +5V signal sources can be connected directly to the analog input channels without additional buffering for source impedances up to 5kΩ (see Figure 11). The input/output transfer characteristic and transition points for this input signal range are shown in Figure 12 and Table I respectively. The designed transition points on the AD7582 transfer characteristic occur on integer multiples of 1LSB. The output code is Natural Binary with 1LSB = (F.S.) (1/4096) = (5/4096)V = 1.22mV.

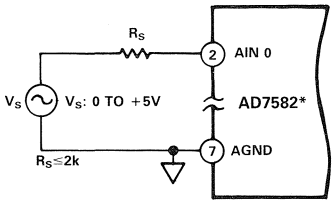


Figure 11. Unipolar 0 to +5V Operation

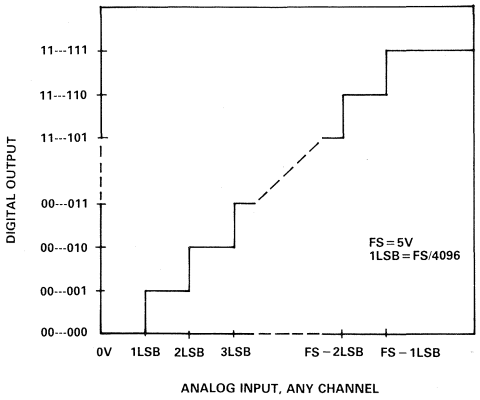


Figure 12. Ideal Input/Output Transfer Characteristic for Unipolar Circuit of Figure 11

Table I. Transition Points for Unipolar 0 to +5V Operation

Analog Input, Volts	Digital Output
0.00122	000 001
0.00244	000 010
2.49878	011 111
2.50000	100 000
2.50122	100 001
4.99756	111 110
4.99878	111 111

Signal ranges other than 0 to +5V are easily accommodated by using resistor divider networks to produce 0 to +5V signal ranges at the AD7582 input pins. Figure 13 shows a divider network on channel 0 to allow an AIN 0 signal range of 0 to +10V. The input resistors must be selected to match within 0.01% and should be the same type and from the same manufacturer so that their temperature coefficients match. Note that since the source impedance has not been included in the resistor divider ratio, it must now be as low as possible. For Figure 13 with a source impedance of 0.5Ω the maximum error across the network is approximately 0.5LSB. The LSB size is (F.S.)(1/4096) = (10/4096)V = 2.44mV.

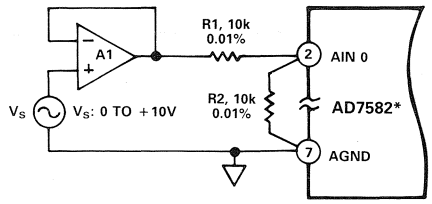


Figure 13. Unipolar 0 to +10V Operation

Bipolar signal ranges of −5V to +5V are accommodated by referencing the resistor divider network to V_{REF} as shown in Figure 14 for channel 0. With the resistor values shown, the signal source must be capable of sinking 0.5mA. The input/output transfer characteristic and transition points for this ±5V signal range are shown in Figure 15 and Table II respectively. The output code is Offset Binary with an LSB size of (F.S.)(1/4096) = (10/4096)V = 2.44mV.

With an analog input (V_S) of −1.22mV, the input offset voltage of A1 should be adjusted until the ADC output flickers between 0111 1111 1111 and 1000 0000 0000. Alternatively the −1/2LSB signal offset can be included in the signal conditioning electronics.

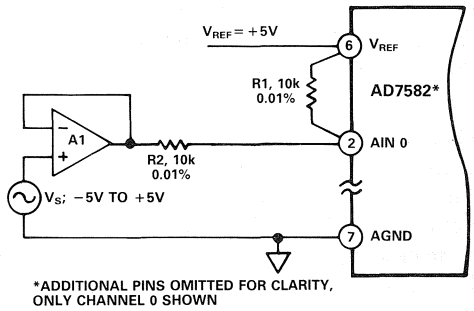


Figure 14. Bipolar −5V to +5V Operation

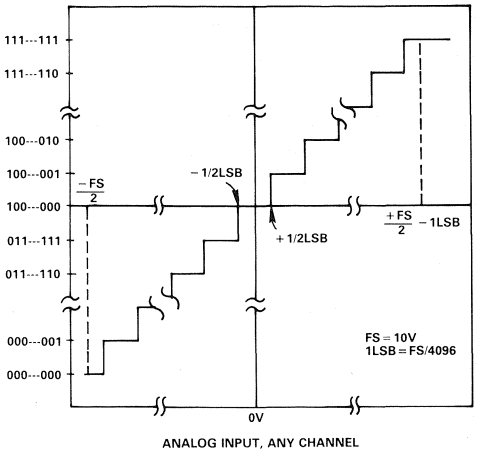


Figure 15. Ideal Input/Output Transfer Characteristic for Bipolar Circuit of Figure 14

Table II. Transition Points for Bipolar −5V to +5V Operation

Analog Input, Volts	Digital Output
−4.99878	000 001
−4.99634	000 010
−0.00122	100 000
+0.00122	100 001
+4.99389	111 110
+4.99634	111 111

Applications

Power Supply Decoupling: All power supplies to the AD7582 should be bypassed with either 10μF tantulum or electrolytic capacitors. To ensure good high frequency performance, each capacitor should be bypassed with an 0.01μF disc ceramic capacitor. All capacitors should be placed as close as possible to the AD7582.

Reference Circuit: Figure 16 shows how to configure an AD584LH to produce a reference voltage of 5.00V. R2 provides a typical adjustment range of ±75mV. The AD584LH will contribute less than 1LSB of gain error over the commercial temperature range.

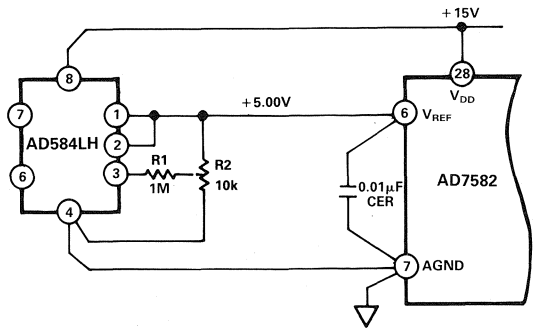


Figure 16. AD584LH as Reference Generator

Transient currents flow at the V_{REF} input during a conversion. To avoid dynamic errors place a 0.01μF disc ceramic from the V_{REF} pin to AGND.

Proper Layout: Layout for a printed circuit board should ensure that digital and analog signal lines are separated as much as possible. In particular, care should be taken not to run any digital track alongside an analog signal track or close to the autozero capacitor. The analog inputs, the reference input and the autozero input should be screened by AGND.

A single point analog ground separate from the logic system ground should be established at pin 7 (AGND) or as close as possible to the AD7582. This single point analog ground should be connected to the digital system ground, to which pin 8 (DGND) is connected, at one point only and as close to the AD7582 as possible. The autozero capacitor, bypass capacitors for the reference input and the analog supplies, AIN commons and any input signal screening should be returned to the analog ground point. Low impedance analog and digital power supply common returns are essential to low noise operation of the ADC and the foil width for these tracks should be as wide as possible.

Noise: Input signal leads to AIN 0-3 and signal return leads from AGND (pin 7) should be kept as short as possible to minimize input noise coupling. In applications where this is not possible, a shielded cable between source and ADC is recommended. Also since any potential difference in grounds between the signal source and ADC appears as an error voltage in series with the input signal, attention should be paid to reducing the ground circuit impedances as much as possible.

In applications where the AD7582 data outputs are connected to a continuously busy (and noisy) microprocessor bus it is possible to get LSB errors in conversion results. These errors are due to feedthrough from the microprocessor bus to the autozero comparator. The problem exists only for ceramic package versions of the AD7582.

Stopping bus activity during a conversion eliminates this problem. Alternatively the AD7582 can be isolated from the microprocessor bus by means of three-state buffers.

Microprocessor Interfacing

MICROPROCESSOR INTERFACING

When the AD7582 is used with its own internal clock oscillator, microprocessor interfacing is straightforward and requires at most a few external gates (see Figures 17 through 19, 21 and 22). When the AD7582 is used with an external clock source, additional circuitry is required to extend the μP control signals (see Figure 20).

MC6800, MC6809 and 6502 MICROPROCESSORS

A typical interface to the AD7582 with any of the above microprocessors is shown in Figure 17. The decoder can be enabled high using VMA in 6800 systems or enabled low by NOR'ing ϕ_0 and ϕ_2 in 6502 systems or by NOR'ing E and Q in 6809 systems. Address lines A0, A1, and A2 of the 6800 have been tied to A0, A1 and BYSL respectively of the AD7582. Assuming the AD7582 is assigned a memory block starting at address 8000H, the input multiplexer is addressed as follows:

8000H	Channel 0
8001H	Channel 1
8002H	Channel 2
8003H	Channel 3

A write instruction to one of these addresses will start a conversion of the selected channel. To read the conversion results, it is necessary only to bring control inputs $\overline{CS}$ and $\overline{RD}$ low. The BYSL input (tied to A2 of the μP) determines whether the data high or low byte is placed onto the 8-bit data bus. A read instruction to any one of the previous channel addresses will result in the low byte of data being transferred to the μP (BYSL = Low). Similarly a read instruction to any address having A2 HIGH and within the assigned memory block, e.g., 8004H, transfers the high byte of data to the μP. The converter status flag BUSY can be polled at intervals to check whether the present conversion has finished and valid 12-bit data is available. This is accomplished by the following instructions on the 6800:

```
LDA  A   $8004     Load Flag from AD7582
ASL  A             Shift Flag into Carry
BCC      FETCH     Branch to Data Fetch
                   Subroutine if BUSY is LOW
```

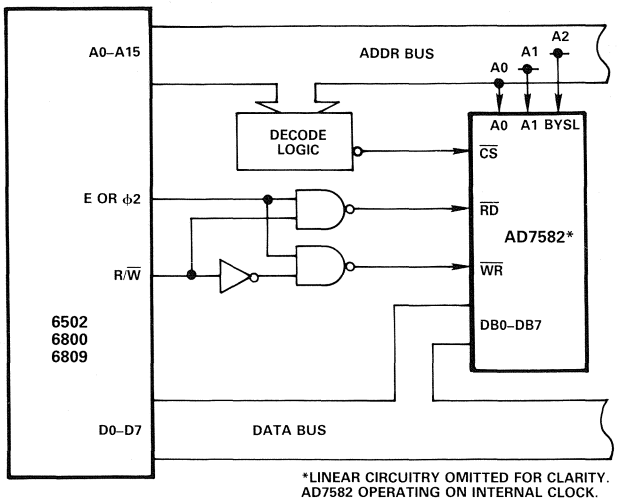


Figure 17. AD7582 – MC6800, 6809, 6502 Interface

8085A, Z80 MICROPROCESSORS

A typical interface to either of these microprocessors is shown in Figure 18. Not shown in the figure is the 8-bit latch required to demultiplex the 8085A common address/data bus. This interface uses slightly different low-level address decoding than the previous interface. Address lines A0, A1 & A2 of the µP have been tied to BYSL, A0 & A1 respectively of the AD7582. This allows the 16-bit data move instructions on both the 8085A and the Z80 to be used when reading conversion results. Assuming the AD7582 is again assigned a memory block starting at address 8000H the input multiplexer is now addressed as follows:

8000H	Channel 0
8002H	Channel 1
8004H	Channel 2
8006H	Channel 3

A write instruction to one of these addresses will start a conversion of the selected channel. The 12-bit conversion results can be read (low byte first then high byte) by a single read instruction;

On the 8085A

LHLD 8000

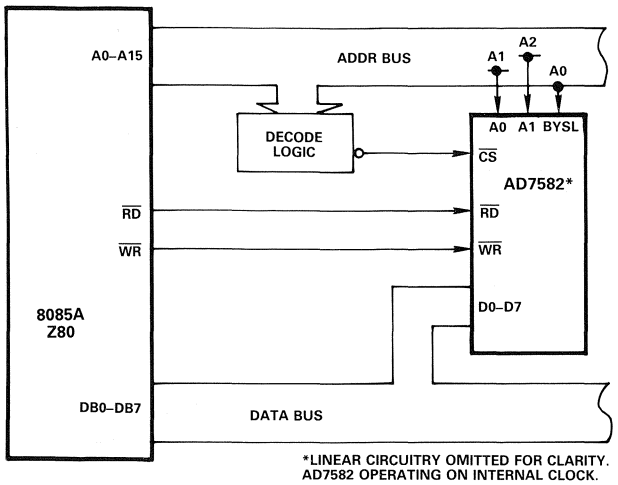


Figure 18. AD7582 – 8085A, Z80 Interface

moves the conversion results into register pair HL

On the Z80

LD BC, (8000)

moves the conversion results into register pair BC

MC68000, MC68008 MICROPROCESSOR

Figure 19 shows an AD7582–MC68000/MC68008 interface.

Address lines A1, A2 and A3 of the µP are connected to BYSL, A0 & A1 inputs respectively of the AD7582.

With the simple decoding logic shown in Figure 19, the AD7582 is decoded in a memory block from C000H to FFFFH. The input multiplexer is now addressed as follows:

C000H	Channel 0
C004H	Channel 1
C008H	Channel 2
C00CH	Channel 3

A write instruction to one of these addresses will start a conversion of the selected channel, i.e.,

MOVE. W D0 $C004

starts a conversion of channel 1. When the conversion is complete, the µP acquires the result by reading from the AD7582, i.e,

MOVEP. W $000 (A2), D0

This instruction places the conversion data in the D0 register of the µP. Address register A2 should contain an odd-order address for the AD7582, e.g., $C003.

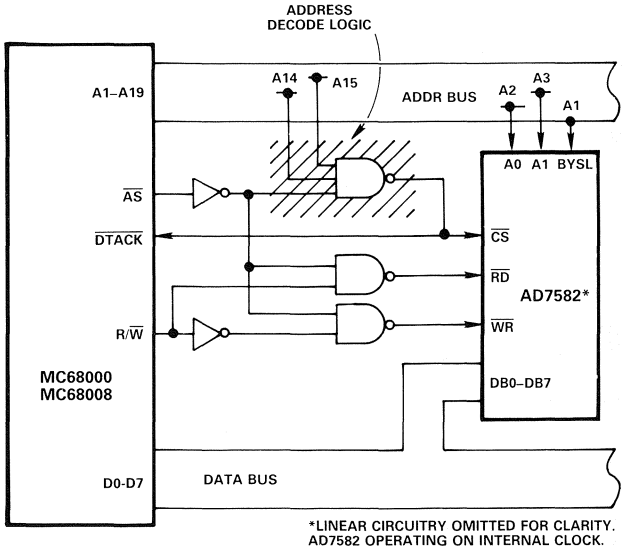


Figure 19. AD7582 – MC68000/MC68008 Interface

MICROPROCESSOR INTERFACE TO AD7582 WITH EXTERNAL CLOCK

Figure 20 shows the additional circuitry generally required to interface an 8-bit µP to the AD7582 operating from an external clock source. During a write operation, the 74121 monostable (one-shot) is triggered to latch the data (A0, A1 and $\overline{CS}$) in the 7477, a 4-bit bistable latch. The monostable timing components (not shown in Figure 20) should be chosen to provide an output pulse width corresponding to t_2 (EXT), the minimum autozero cycle time. To avoid any possibility of spurious triggering, the monostable should be enabled by a valid memory address signal. During a data read cycle, the 7477 latch is transparent and data is read normally. Note that the µP write and read cycle times are unaffected by the interface circuitry.

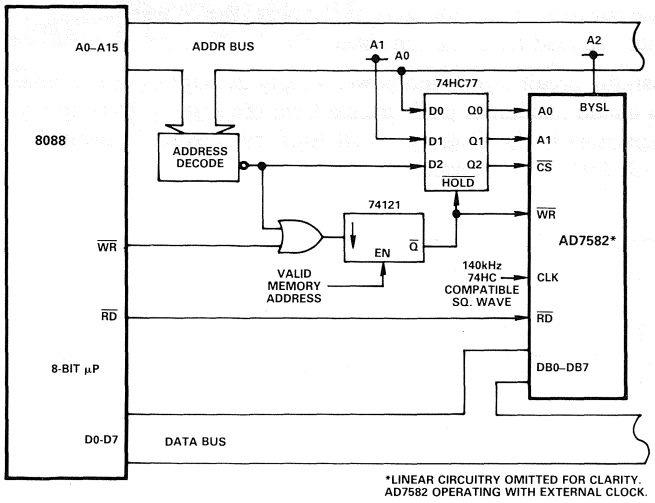


Figure 20. Interface to AD7582 Using External Clock

8088, 8086 MICROPROCESSORS

Figure 21 shows an AD7582–8088 interface.

Address lines A0, A1 and A2 are connected to BYSL, A0 and A1 inputs respectively of the AD7582. With the simple decoding shown in Figure 21 the AD7582 is decoded in a memory block from 4000H to 7FFFH. The input multiplexer is now addressed as follows:

4000H	Channel 0
4002H	Channel 1
4004H	Channel 2
4006H	Channel 3

A write instruction to one of these addresses will start a conversion of the selected channel, i.e,

MOV 4004, AX

starts a conversion of channel 2. When the conversion is finished the 8088 acquires the result by reading from the AD7582, i.e.,

MOV AX, 4000

places the conversion data in the accumulator.

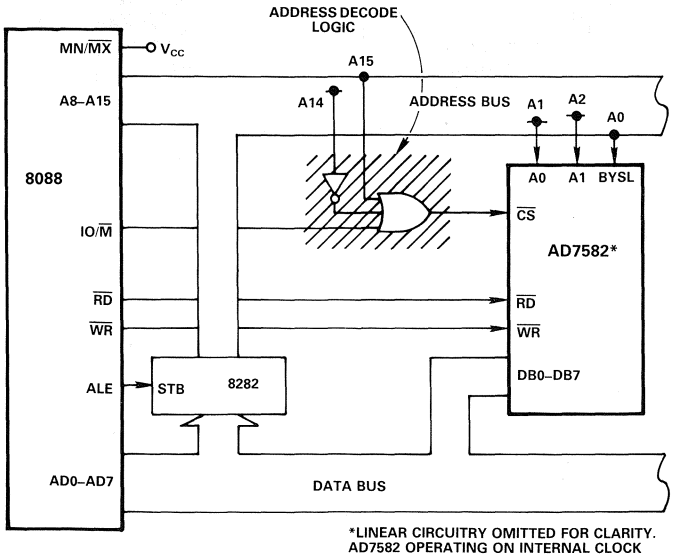


Figure 21. AD7582 – 8088 Interface

Figure 22 shows an AD7582–8086 interface. Address lines A1, A2 and A3 are connected to BYSL, A0 and A1 inputs respectively of the AD7582. The AD7582 is again decoded in a memory block from 4000H to 7FFFH. The input multiplexer is now addressed as follows:

4000H	Channel 0
4004H	Channel 1
4008H	Channel 2
400CH	Channel 3

A write instruction to one of these addresses will start a conversion of the selected channel, i.e,

MOV 4008, AX

starts a conversion of channel 2. When the conversion is finished, the 8086 acquires the result by reading from the AD7582 in two read cycles, i.e.,

MOV AL, 4000
MOV AH, 4002

places the conversion data in the accumulator.

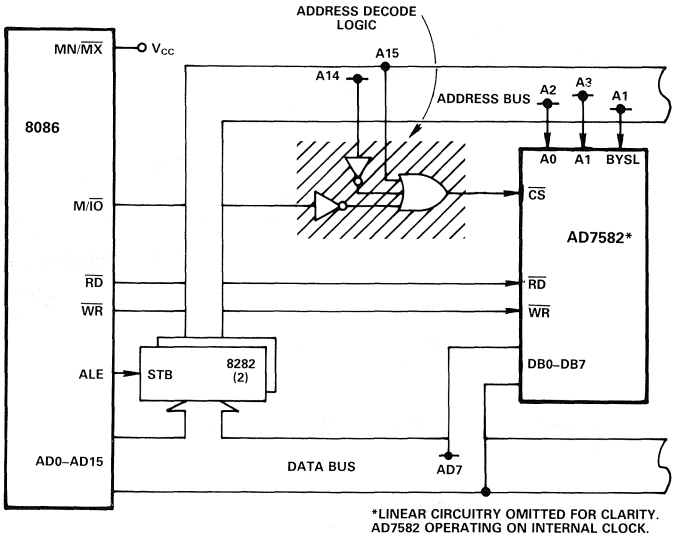


Figure 22. AD7582 – 8086 Interface

AD7582-AD585 SAMPLE-HOLD INTERFACE

Figure 23 shows an AD585 Sample-Hold Amplifier driving A_{IN1} of the AD7582. At a sampling frequency of 8kHz the maximum input signal frequency is 4kHz. The AD7582 is configured for bipolar operation to allow an input signal swing of ±5V. No clock components are shown for the AD7582 but the conversion time of the AD7582 should be adjusted for 100 microseconds. With an external hold capacitor of 100pF, the acquisition time for the sample-hold amplifier is 10 microseconds. The circuit operates from 0°C to +70°C.

To take a sample of the input, a WRITE instruction is executed to the AD7582 control inputs. The converter busy flag, $\overline{BUSY}$, is driven low indicating that a conversion is in progress. The falling edge of this $\overline{BUSY}$ signal places the sample-hold amplifier into the HOLD mode "freezing" the input signal to the AD7582. After 100 microseconds the conversion is finished and the $\overline{BUSY}$ signal is brought high. This allows a time of 25 microseconds for the AD585 to come out of the hold mode and acquire the input signal in time for the next sample. Between the end of one conversion and the start of the next, the conversion results must be read from the converter.

Careful circuit layout and power supply decoupling are necessary to obtain maximum performance from the system. Decoupling capacitors in the diagram are all 10μF electroytics in parallel with 0.01μF disc ceramics.

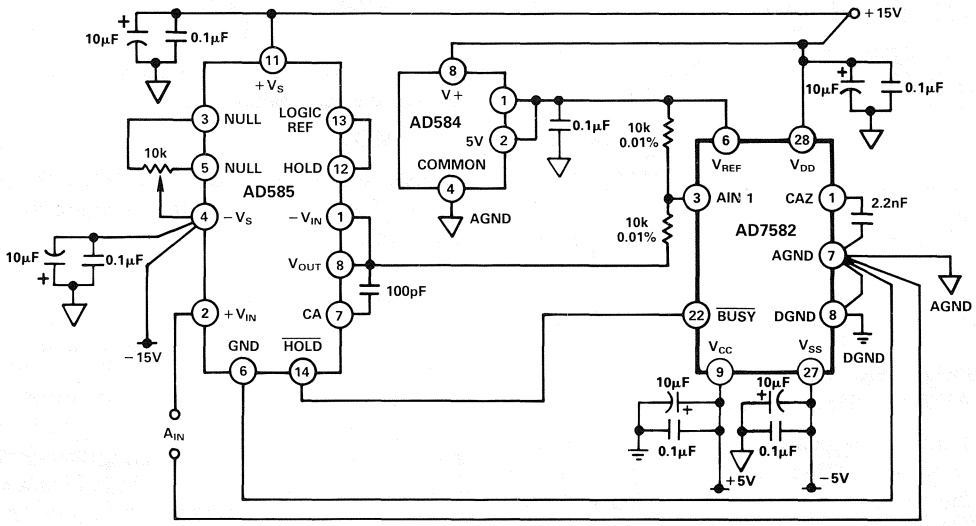
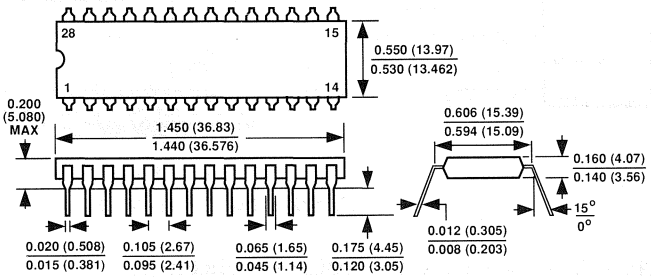


Figure 23. AD7582-AD585 Interface

MECHANICAL INFORMATION

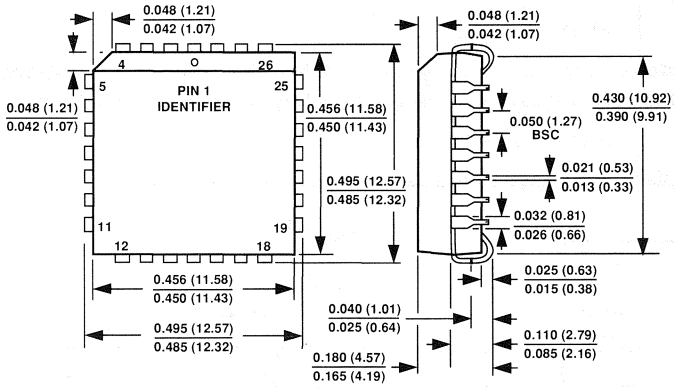
Dimensions shown in inches and (mm).

28-Pin Plastic DIP (N-28)

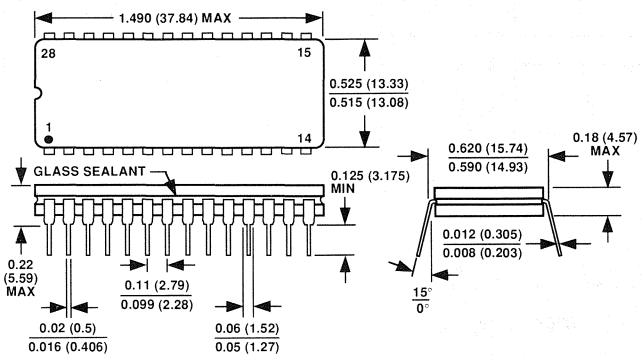


LEADS ARE SOLDER DIPPED OR TIN-PLATED ALLOY 42 OR COPPER.

28-Pin PLCC (P-28A)



28-Pin Cerdip (Q-28)



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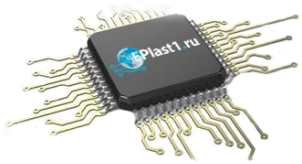

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