

# THC63LVD827

## LOW POWER / SMALL PACKAGE / 24Bit COLOR LVDS TRANSMITTER

### General Description

The THC63LVD827 transmitter is designed to support pixel data transmission between Host and Flat Panel Display and Dual Link transmission between Host and Flat Panel Display up to 1080p/1920x1440 resolutions.

The THC63LVD827 converts 27bits (RGB 8 bits + Hsync, Vsync, DE) of CMOS/TTL data into LVDS (Low Voltage Differential Signaling) data stream. The transmitter can be programmed for rising edge or falling edge clocks through a dedicated pin.

For dual LVDS out, LVDS clock frequency of 87MHz, 51bits of RGB data are transmitted at an effective rate of 609Mbps per LVDS channel.

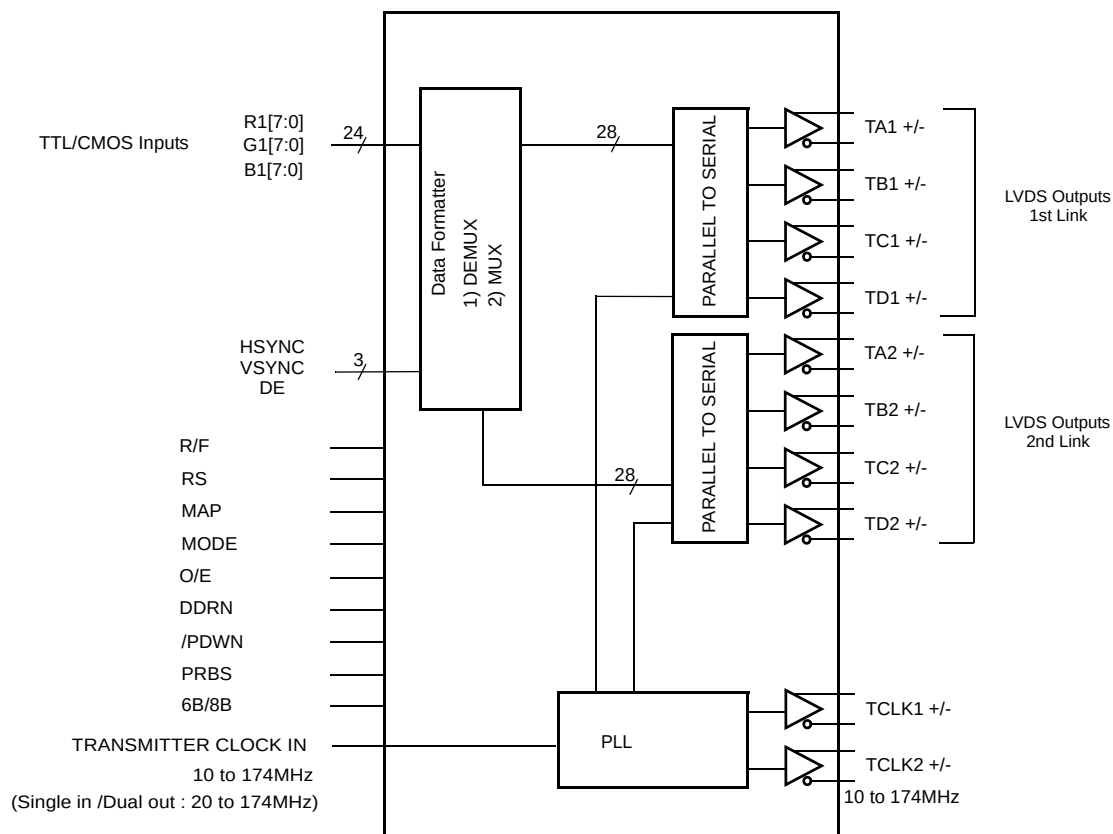
For single LVDS out, LVDS clock frequency of 174MHz, 27bits of RGB data are transmitted at an effective rate of 1218Mbps per LVDS channel.

21bits (RGB 6 bits + Hsync, Vsync, DE) mode is also selectable for 6bit color transmission with lower power.

### Features

- Low power 1.8V CMOS design
- 7mm x 7mm/72pin/0.65mm pitch/TFBGA package applicable to non-HDI PCB.
- Wide dot clock range, 10-174MHz, suited for  
TV Signal: up to 1080p(74.25MHz dual)  
PC Signal: up to 1920x1440(86MHz dual)
- Supports 1.8V single power supply
- 1.8V/2.5V/3.3V TTL/CMOS inputs are supported by setting IOVCC=1.8V/2.5V/3.3V
- LVDS swing reducible by RS-pin to reduce both EMI and power consumption
- PLL requires No external components
- Flexible Input/Output mode
  1. Single in / Dual LVDS out
  2. Single in / Single LVDS out
  3. Double edge Single in / Dual LVDS out
- 2 LVDS data mapping to simplify PCB layout
- Power down mode
- Input clock triggering edge selectable by R/F pin
- 6bit / 8bit modes selectable by 6B/8B pin

### Block Diagram



## Pin Out (top view)

### TOP VIEW

|   | 1    | 2    | 3           | 4          | 5           | 6    | 7          | 8     | 9          |   |
|---|------|------|-------------|------------|-------------|------|------------|-------|------------|---|
| A | TA1+ | TB1+ | TC1+        | TCLK1<br>+ | TD1+        | TA2+ | TB2+       | TC2+  | TCLK2<br>+ | A |
| B | TA1- | TB1- | TC1-        | TCLK1<br>- | TD1-        | TA2- | TB2-       | TC2-  | TCLK2<br>- | B |
| C | PRBS | N/C  | Reserved1   | GND        | LVDS<br>VCC | GND  | PLL<br>VCC | TD2-  | TD2+       | C |
| D | R11  | R10  | LVDS<br>VCC |            |             |      | GND        | /PDWN | O/E        | D |
| E | R13  | R12  | GND         |            |             |      | MODE       | MAP   | DDRN       | E |
| F | R15  | R14  | GND         |            |             |      | 6B/8B      | RS    | CLKIN      | F |
| G | R17  | R16  | VCC         | GND        | VCC         | GND  | IOVCC      | R/F   | DE         | G |
| H | G10  | G12  | G14         | G16        | B10         | B12  | B14        | B16   | VSYNC      | H |
| J | G11  | G13  | G15         | G17        | B11         | B13  | B15        | B17   | HSYNC      | J |
|   | 1    | 2    | 3           | 4          | 5           | 6    | 7          | 8     | 9          |   |

## Pin Description

| Pin Name          | Pin #                               | Type     | Description                                                                                                                                                                                                   |      |                                     |   |                                   |   |                               |
|-------------------|-------------------------------------|----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|-------------------------------------|---|-----------------------------------|---|-------------------------------|
| TA1+, TA1-        | A1,B1                               | LVDS OUT | The 1st Link.<br>The 1st pixel output data when Dual out.<br>Output data when Single out.                                                                                                                     |      |                                     |   |                                   |   |                               |
| TB1+, TB1-        | A2,B2                               |          |                                                                                                                                                                                                               |      |                                     |   |                                   |   |                               |
| TC1+, TC1-        | A3,B3                               |          |                                                                                                                                                                                                               |      |                                     |   |                                   |   |                               |
| TD1+, TD1-        | A5,B5                               |          |                                                                                                                                                                                                               |      |                                     |   |                                   |   |                               |
| TCLK1+, TCLK1-    | A4,B4                               | LVDS OUT | LVDS Clock Out for 1st Link.                                                                                                                                                                                  |      |                                     |   |                                   |   |                               |
| TA2+, TA2-        | A6,B6                               | LVDS OUT | The 2nd Link.<br>The 2nd pixel output data when Dual out.                                                                                                                                                     |      |                                     |   |                                   |   |                               |
| TB2+, TB2-        | A7,B7                               |          |                                                                                                                                                                                                               |      |                                     |   |                                   |   |                               |
| TC2+, TC2-        | A8,B8                               |          |                                                                                                                                                                                                               |      |                                     |   |                                   |   |                               |
| TD2+, TD2-        | C9,C8                               |          |                                                                                                                                                                                                               |      |                                     |   |                                   |   |                               |
| TCLK2+, TCLK2-    | A9,B9                               | LVDS OUT | LVDS Clock Out for 2nd Link.                                                                                                                                                                                  |      |                                     |   |                                   |   |                               |
| R17 ~ R10         | G1,G2,F1,F2<br>E1,E2,D1,D2          | IN       | Pixel Data Inputs.                                                                                                                                                                                            |      |                                     |   |                                   |   |                               |
| G17 ~ G10         | J4,H4,J3,H3<br>J2,H2,J1,H1          |          |                                                                                                                                                                                                               |      |                                     |   |                                   |   |                               |
| B17 ~ B10         | J8,H8,J7,H7<br>J6,H6,J5,H5          |          |                                                                                                                                                                                                               |      |                                     |   |                                   |   |                               |
| DE                | G9                                  | IN       | Data Enable Input.                                                                                                                                                                                            |      |                                     |   |                                   |   |                               |
| VSYNC             | H9                                  | IN       | Vsync Input.                                                                                                                                                                                                  |      |                                     |   |                                   |   |                               |
| HSYNC             | J9                                  | IN       | Hsync Input.                                                                                                                                                                                                  |      |                                     |   |                                   |   |                               |
| CLKIN             | F9                                  | IN       | Clock Input.                                                                                                                                                                                                  |      |                                     |   |                                   |   |                               |
| R/F               | G8                                  | IN       | Input Clock Triggering Edge Select.<br>H: Rising edge, L: Falling edge                                                                                                                                        |      |                                     |   |                                   |   |                               |
| RS                | F8                                  | IN       | LVDS swing mode select. <table><tr><td>RS</td><td>LVDS Swing (VOD, see Fig4 and Fig5)</td></tr><tr><td>H</td><td>350mV</td></tr><tr><td>L</td><td>200mV</td></tr></table>                                     | RS   | LVDS Swing (VOD, see Fig4 and Fig5) | H | 350mV                             | L | 200mV                         |
| RS                | LVDS Swing (VOD, see Fig4 and Fig5) |          |                                                                                                                                                                                                               |      |                                     |   |                                   |   |                               |
| H                 | 350mV                               |          |                                                                                                                                                                                                               |      |                                     |   |                                   |   |                               |
| L                 | 200mV                               |          |                                                                                                                                                                                                               |      |                                     |   |                                   |   |                               |
| MAP               | E8                                  | IN       | LVDS mapping table select. See Fig9 and Fig10. <table><tr><td>MAP</td><td>Mapping Mode</td></tr><tr><td>H</td><td>Mapping MODE1</td></tr><tr><td>L</td><td>Mapping MODE2</td></tr></table>                    | MAP  | Mapping Mode                        | H | Mapping MODE1                     | L | Mapping MODE2                 |
| MAP               | Mapping Mode                        |          |                                                                                                                                                                                                               |      |                                     |   |                                   |   |                               |
| H                 | Mapping MODE1                       |          |                                                                                                                                                                                                               |      |                                     |   |                                   |   |                               |
| L                 | Mapping MODE2                       |          |                                                                                                                                                                                                               |      |                                     |   |                                   |   |                               |
| MODE              | E7                                  | IN       | Pixel data mode. See Fig7 and Fig8. <table><tr><td>MODE</td><td>Modes</td></tr><tr><td>H</td><td>Single out (Single-in/Single-out)</td></tr><tr><td>L</td><td>Dual out (Single-in/Dual-out)</td></tr></table> | MODE | Modes                               | H | Single out (Single-in/Single-out) | L | Dual out (Single-in/Dual-out) |
| MODE              | Modes                               |          |                                                                                                                                                                                                               |      |                                     |   |                                   |   |                               |
| H                 | Single out (Single-in/Single-out)   |          |                                                                                                                                                                                                               |      |                                     |   |                                   |   |                               |
| L                 | Dual out (Single-in/Dual-out)       |          |                                                                                                                                                                                                               |      |                                     |   |                                   |   |                               |
| O/E               | D9                                  | IN       | Output enable.<br>H: Output enable,<br>L: Output disable (all outputs are Hi-Z).                                                                                                                              |      |                                     |   |                                   |   |                               |
| /PDWN             | D8                                  | IN       | H: Normal operation,<br>L: Power down (all outputs are Hi-Z and all circuits are stand-by mode with minimum current (ITCCS)).                                                                                 |      |                                     |   |                                   |   |                               |
| PRBS <sup>a</sup> | C1                                  | IN       | Must be tied to GND.                                                                                                                                                                                          |      |                                     |   |                                   |   |                               |

## Pin Description (Continued)

| Pin Name  | Pin #                    | Type   | Description                                                                                                                                                        |
|-----------|--------------------------|--------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Reserved1 | C3                       | IN     | Must be tied to GND.                                                                                                                                               |
| 6B/8B     | F7                       | IN     | 6bit / 8bit mode select.<br>H: 6bit mode (21bit mode),<br>L: 8bit mode (27bit mode).                                                                               |
| DDRN      | E9                       | IN     | DDR function is active when MODE = L (Dual-out mode).<br>H: DDR (Double Edge input) function disable (Fig4).<br>L: DDR (Double Edge input) function enable (Fig5). |
| N/C       | C2                       |        | Must be Open.                                                                                                                                                      |
| VCC       | G3,G5                    | Power  | Power Supply Pins for digital circuitry.                                                                                                                           |
| IOVCC     | G7                       | Power  | Power Supply Pin for IO inputs circuitry.                                                                                                                          |
| LVDSVCC   | C5,D3                    | Power  | Power Supply Pins for LVDS Outputs.                                                                                                                                |
| PLLVC     | C7                       | Power  | Power Supply Pin for PLL circuitry.                                                                                                                                |
| GND       | F3,G4,G6,C4,<br>E3,C6,D7 | Ground | Ground Pins.                                                                                                                                                       |

- a: Setting the PRBS pin high enables the internal test pattern generator. It generates Pseudo-Random Bit Sequence of  $2^{23}-1$ . The generated PRBS is fed into input data latches, encoded and serialized into LVDS OUT. This function is normally to be used for analyzing the signal integrity of the transmission channel including PCB traces, connectors, and cables.

## Absolute Maximum Ratings

|                                       |                          |
|---------------------------------------|--------------------------|
| Supply Voltage (IOVCC)                | -0.3V ~ +4.0V            |
| Supply Voltage (VCC, PLLVCC, LVDSVCC) | -0.3V ~ +2.1V            |
| CMOS/TTL Input Voltage                | -0.3V ~ (IOVCC+ 0.3V)    |
| LVDS Transmitter Output Voltage       | -0.3V ~ (LVDSVCC + 0.3V) |
| Output Current                        | -50mA ~ 50mA             |
| Junction Temperature                  | +125°C                   |
| Storage Temperature Range             | -55°C ~ +125°C           |
| Reflow Peak Temperature / Time        | +260°C / 10sec.          |
| Maximum Power Dissipation @+25°C      | 1.3W                     |

## Recommended Operating Conditions

| Parameter                               |                      |                               |             | Min  | Typ             | Max  | Units |
|-----------------------------------------|----------------------|-------------------------------|-------------|------|-----------------|------|-------|
| Supply Voltage (IOVCC)                  |                      |                               |             | 1.62 | 1.8 / 2.5 / 3.3 | 3.6  | V     |
| Supply Voltage (PLLVCC / LVDSVCC / VCC) |                      |                               |             | 1.62 | 1.8             | 1.98 | V     |
| Operating Ambient Temperature (Ta)      |                      |                               |             | -40  |                 | 85   | °C    |
| Clock Frequency                         | MODE=L<br>Dual-out   | Single Edge Input<br>(DDRN=H) | Input       | 20   |                 | 174  | MHz   |
|                                         |                      |                               | LVDS Output | 10   |                 | 87   | MHz   |
|                                         |                      | Double Edge Input<br>(DDRN=L) | Input       | 10   |                 | 174  | MHz   |
|                                         |                      |                               | LVDS Output | 10   |                 | 174  | MHz   |
|                                         | MODE=H<br>Single-out |                               | Input       | 10   |                 | 174  | MHz   |
|                                         |                      |                               | LVDS Output | 10   |                 | 174  | MHz   |

## Electrical Characteristics

### CMOS/TTL (Pin type “IN”) DC Specifications

Over recommended operating supply and temperature ranges unless otherwise specified.

| Symbol     | Parameter                     | Conditions             | Min.         | Typ. | Max.         | Units   |
|------------|-------------------------------|------------------------|--------------|------|--------------|---------|
| $V_{IH18}$ | High Level Data Input Voltage | $IOVCC=1.62V\sim1.98V$ | 0.65 $IOVCC$ |      | $IOVCC+0.3$  | V       |
| $V_{IL18}$ | Low Level Data Input Voltage  |                        | -0.3         |      | 0.35 $IOVCC$ | V       |
| $V_{IH25}$ | High Level Data Input Voltage | $IOVCC=2.3V\sim2.7V$   | 1.7          |      | $IOVCC+0.3$  | V       |
| $V_{IL25}$ | Low Level Data Input Voltage  |                        | -0.3         |      | 0.7          | V       |
| $V_{IH33}$ | High Level Data Input Voltage | $IOVCC=3.0V\sim3.6V$   | 2.0          |      | $IOVCC+0.3$  | V       |
| $V_{IL33}$ | Low Level Data Input Voltage  |                        | -0.3         |      | 0.8          | V       |
| $I_{INC}$  | Input Current                 | $V_{IN}=GND\sim IOVCC$ | -10          |      | 10           | $\mu A$ |

### LVDS Transmitter (Pin type “LVDS OUT”) DC Specifications

Over recommended operating supply and temperature ranges unless otherwise specified.

| Symbol       | Parameter                                         | Conditions                              |                         | Min.  | Typ. | Max.  | Units   |
|--------------|---------------------------------------------------|-----------------------------------------|-------------------------|-------|------|-------|---------|
| VOD          | Differential Output Voltage                       | $RL=100\Omega$                          | Normal swing<br>$RS=H$  | 250   | 350  | 450   | mV      |
|              |                                                   |                                         | Reduced swing<br>$RS=L$ | 140   | 200  | 300   | mV      |
| $\Delta VOD$ | Change in VOD between complementary output states | $RL=100\Omega$                          |                         |       |      | 35    | mV      |
| VOC          | Common Mode Voltage                               |                                         |                         | 1.125 | 1.25 | 1.375 | V       |
| $\Delta VOC$ | Change in VOC between complementary output states |                                         |                         |       |      | 35    | mV      |
| $I_{OS}$     | Output Short Circuit Current                      | $V_{OUT}=GND, RL=100\Omega$             |                         |       |      | 100   | mA      |
| $I_{OZ}$     | Output TRI-State current                          | $/PDWN=L,$<br>$V_{OUT}=GND\sim LVDSVCC$ |                         | -20   |      | 20    | $\mu A$ |

## Electrical Characteristics (Continued)

### Supply Current

Over recommended operating supply and temperature ranges unless otherwise specified.

| Symbol            | Parameter                                      | Conditions                                  |                                                  |               | Typ. <sup>(a)</sup> | Max. <sup>(b)</sup> | Units |
|-------------------|------------------------------------------------|---------------------------------------------|--------------------------------------------------|---------------|---------------------|---------------------|-------|
| I <sub>TCCW</sub> | Transmitter<br>Supply<br>Current               | RL=100Ω<br>CL=5pF<br><br>RS = H<br>(RS = L) | MODE=H<br>Single-out                             | CLKIN=37MHz   | 24<br>(18)          | 33<br>(26)          | mA    |
|                   |                                                |                                             |                                                  | CLKIN=65MHz   | 29<br>(23)          | 43<br>(37)          | mA    |
|                   |                                                |                                             |                                                  | CLKIN=72MHz   | 30<br>(24)          | 46<br>(40)          | mA    |
|                   |                                                |                                             | MODE=L<br>Dual-out                               | CLKIN=89MHz   | 48<br>(36)          | 65<br>(53)          | mA    |
|                   |                                                |                                             |                                                  | CLKIN=119MHz  | 53<br>(41)          | 75<br>(63)          | mA    |
|                   |                                                |                                             |                                                  | CLKIN=139MHz  | 56<br>(44)          | 82<br>(70)          | mA    |
|                   |                                                |                                             | DDRN=H<br>DDR Input Off                          | CLKIN=154MHz  | 58<br>(46)          | 88<br>(76)          | mA    |
|                   |                                                |                                             |                                                  |               |                     |                     |       |
|                   |                                                |                                             | MODE=L<br>Dual-out<br><br>DDRN=L<br>DDR Input On | CLKIN=44.5MHz | 47<br>(35)          | 64<br>(52)          | mA    |
|                   |                                                |                                             |                                                  | CLKIN=59.5MHz | 51<br>(39)          | 74<br>(62)          | mA    |
|                   |                                                |                                             |                                                  | CLKIN=69MHz   | 54<br>(42)          | 80<br>(68)          | mA    |
|                   |                                                |                                             |                                                  | CLKIN=77MHz   | 56<br>(44)          | 85<br>(73)          | mA    |
| I <sub>TCCS</sub> | Transmitter<br>Power Down<br>Supply<br>Current | /PDWN = L, All Inputs = Fixed L or H        |                                                  |               | 1                   | 50                  | uA    |

(a) All Typ. values are at Vcc=1.8V, Ta=25°C . The 256 Grayscale Test Pattern inputs test for a typical display pattern.

(b) All Max. values are at Vcc=1.98V, Ta=85°C . Worst Case Test Pattern produces maximum switching frequency for all the LVDS outputs (Fig.1).

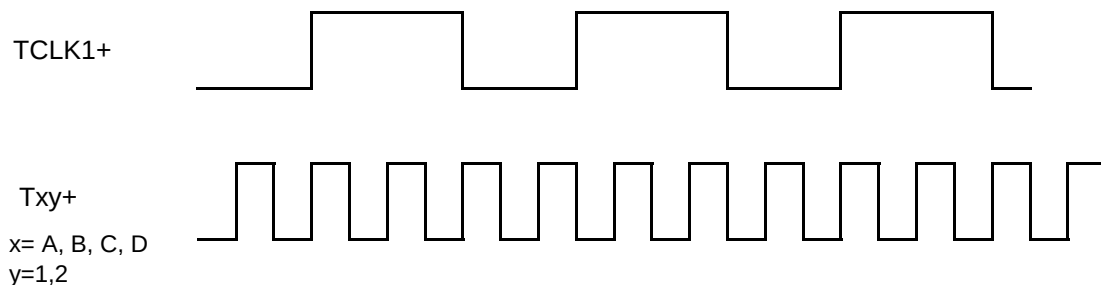


Fig1. Test Pattern  
(LVDS Output Full Toggle Pattern)

## Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

| Symbol             | Parameter                                               |                                    | Min.                         | Typ.                      | Max.                         | Units |
|--------------------|---------------------------------------------------------|------------------------------------|------------------------------|---------------------------|------------------------------|-------|
| t <sub>TCIP</sub>  | CLK IN Period(Fig4,5)                                   |                                    | 5.75                         |                           | 100                          | ns    |
| t <sub>TCH</sub>   | CLK IN High Time(Fig4,5)                                |                                    | 0.35t <sub>TCIP</sub>        | 0.5t <sub>TCIP</sub>      | 0.65t <sub>TCIP</sub>        | ns    |
| t <sub>TCL</sub>   | CLK IN Low Time(Fig4,5)                                 |                                    | 0.35t <sub>TCIP</sub>        | 0.5t <sub>TCIP</sub>      | 0.65t <sub>TCIP</sub>        | ns    |
| t <sub>TS</sub>    | TTL Data Setup to CLK IN(Fig4,5)                        |                                    | 0.8                          |                           |                              | ns    |
| t <sub>TH</sub>    | TTL Data Hold from CKL IN(Fig4,5)                       |                                    | 0.8                          |                           |                              | ns    |
| t <sub>TCD</sub>   | CLK IN to TCLK+/- Delay (Fig4,5)                        | MODE=L,DDR=H                       | 9t <sub>TCIP</sub> +3.1      |                           | 9t <sub>TCIP</sub> +8.0      | ns    |
|                    |                                                         | Others                             | 5t <sub>TCIP</sub> +3.1      |                           | 5t <sub>TCIP</sub> +8.0      | ns    |
| t <sub>TCOP</sub>  | CLK OUT Period(Fig6)                                    |                                    | 5.75                         |                           | 100                          | ns    |
| t <sub>LVT</sub>   | LVDS Transition Time(Fig2)                              |                                    |                              | 0.6                       | 1.5                          | ns    |
| t <sub>TOP1</sub>  | Output Data Position0 (Fig6)                            | t <sub>TCOP</sub> =<br>5.75ns~15ns | -0.15                        | 0.0                       | +0.15                        | ns    |
| t <sub>TOP0</sub>  | Output Data Position1 (Fig6)                            |                                    | $\frac{t_{TCOP}}{7} - 0.15$  | $\frac{t_{TCOP}}{7}$      | $\frac{t_{TCOP}}{7} + 0.15$  | ns    |
| t <sub>TOP6</sub>  | Output Data Position2 (Fig6)                            |                                    | $2\frac{t_{TCOP}}{7} - 0.15$ | $2\frac{t_{TCOP}}{7}$     | $2\frac{t_{TCOP}}{7} + 0.15$ | ns    |
| t <sub>TOP5</sub>  | Output Data Position3 (Fig6)                            |                                    | $3\frac{t_{TCOP}}{7} - 0.15$ | $3\frac{t_{TCOP}}{7}$     | $3\frac{t_{TCOP}}{7} + 0.15$ | ns    |
| t <sub>TOP4</sub>  | Output Data Position4 (Fig6)                            |                                    | $4\frac{t_{TCOP}}{7} - 0.15$ | $4\frac{t_{TCOP}}{7}$     | $4\frac{t_{TCOP}}{7} + 0.15$ | ns    |
| t <sub>TOP3</sub>  | Output Data Position5 (Fig6)                            |                                    | $5\frac{t_{TCOP}}{7} - 0.15$ | $5\frac{t_{TCOP}}{7}$     | $5\frac{t_{TCOP}}{7} + 0.15$ | ns    |
| t <sub>TOP2</sub>  | Output Data Position6 (Fig6)                            |                                    | $6\frac{t_{TCOP}}{7} - 0.15$ | $6\frac{t_{TCOP}}{7}$     | $6\frac{t_{TCOP}}{7} + 0.15$ | ns    |
| t <sub>TPLL</sub>  | Phase Lock Time(Fig3)                                   |                                    |                              |                           | 10.0                         | ms    |
| t <sub>DEINT</sub> | DE input period (Fig3-1)<br>Dual out mode only (MODE=L) |                                    | 4t <sub>TCIP</sub>           | tTCIP*(2n) <sup>(a)</sup> |                              | ns    |
| t <sub>DEH</sub>   | DE High time (Fig3-1)<br>Dual-out mode only (MODE=L)    |                                    | 2t <sub>TCIP</sub>           | tTCIP*(2m) <sup>(a)</sup> |                              | ns    |
| t <sub>DEL</sub>   | DE Low time(Fig3-1)<br>Dual-out mode only (MODE=L)      |                                    | 2t <sub>TCIP</sub>           |                           |                              | ns    |

(a) Refer to Fig3-1 for details.



## AC Timing Diagrams

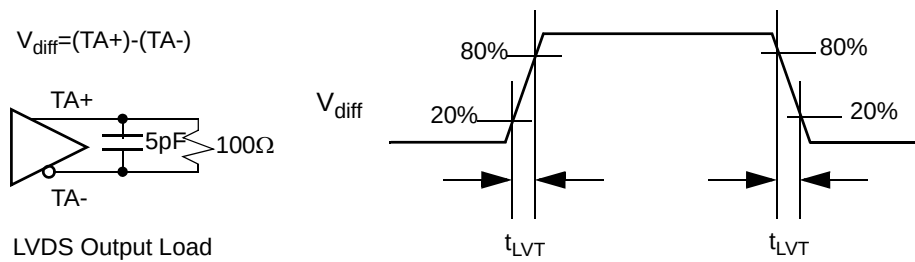


Fig2. LVDS Output Load and Transition Time

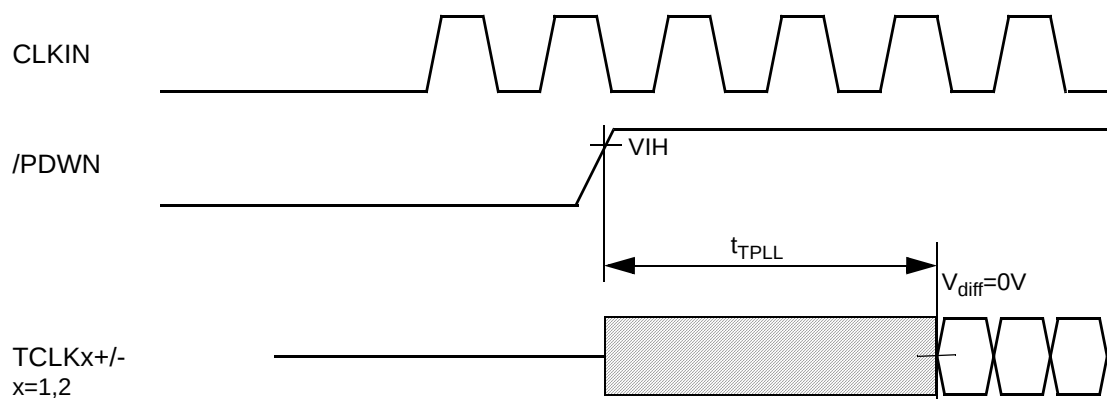
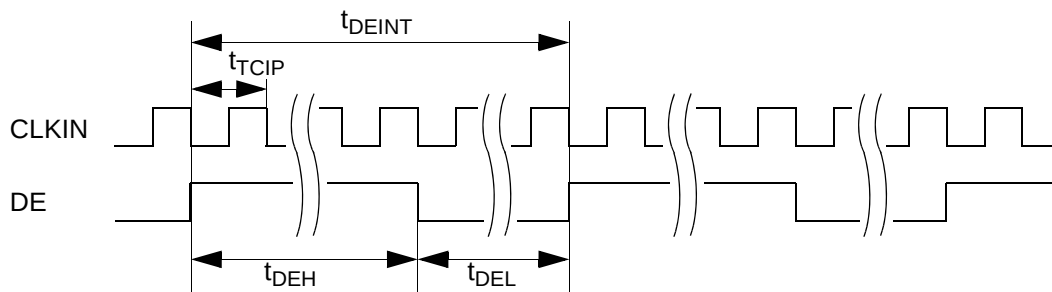


Fig3. PLL Lock Time



Note: In dual-out mode (MODE=L), the period between rising edges of DE ( $t_{DEINT}$ ), high time of DE ( $t_{DEH}$ ) should always satisfy following equations.

$$t_{DEH} = t_{TCIP} * (2m)$$

$$t_{DEINT} = t_{TCIP} * (2n)$$

$m, n = \text{integer}$

Fig3-1. Dual OUT mode DE input timing

## AC Timing Diagrams (Continued)

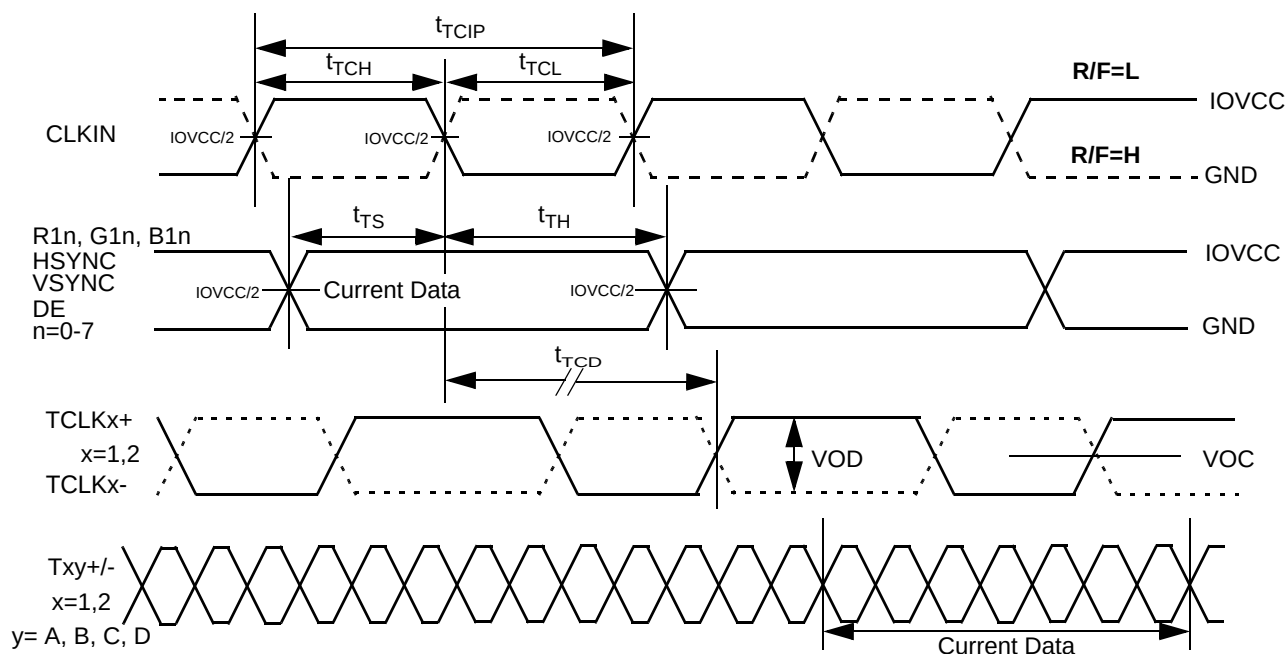


Fig4. CLKIN Period, High/Low Time, Setup/Hold Timing for Single Edge Input Mode  
MODE=H or MODE=L,DDR=H

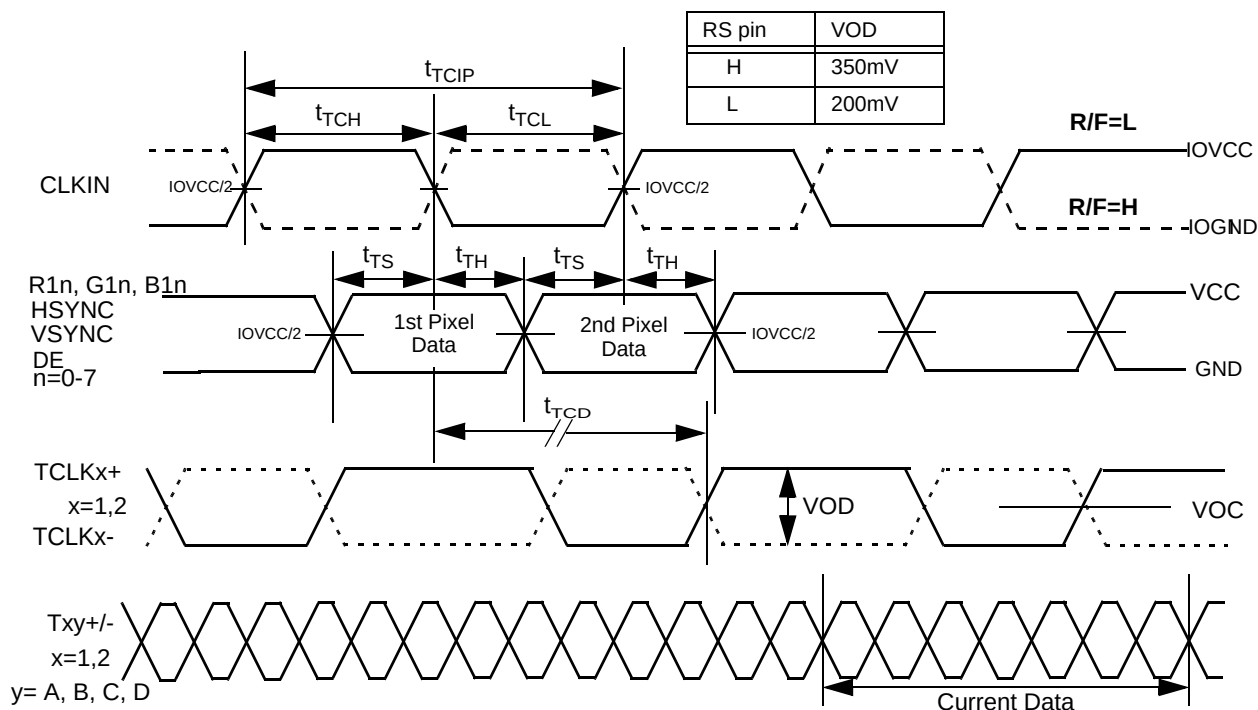


Fig5. CLKIN Period, High/Low Time, Setup/Hold Timing for Double Edge Input Mode (DDR)  
MODE=L,DDR=L

## AC Timing Diagrams (Continued)

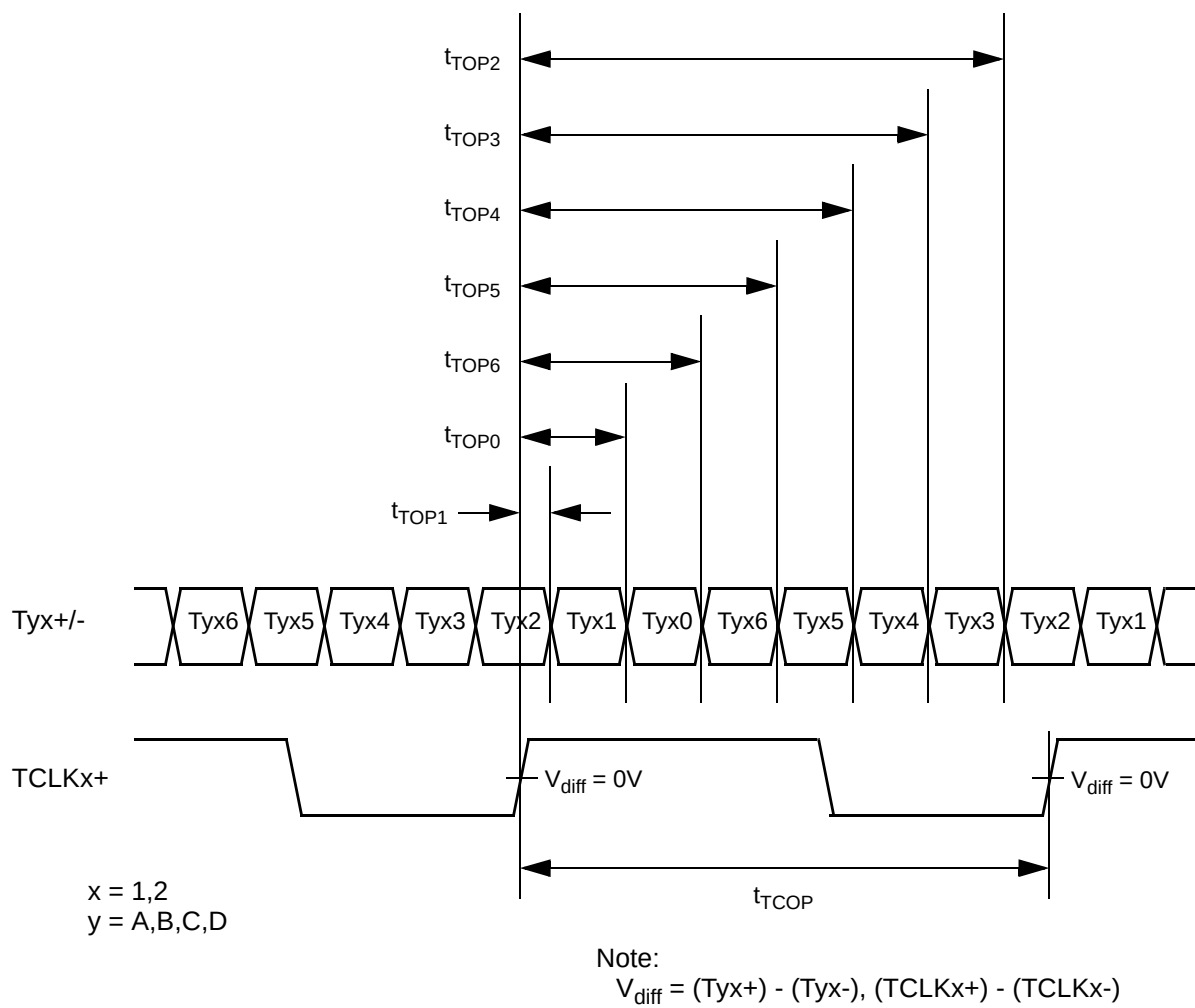


Fig6. LVDS Output Data Position

## Single-In / Dual-Out Mode (MODE = L)

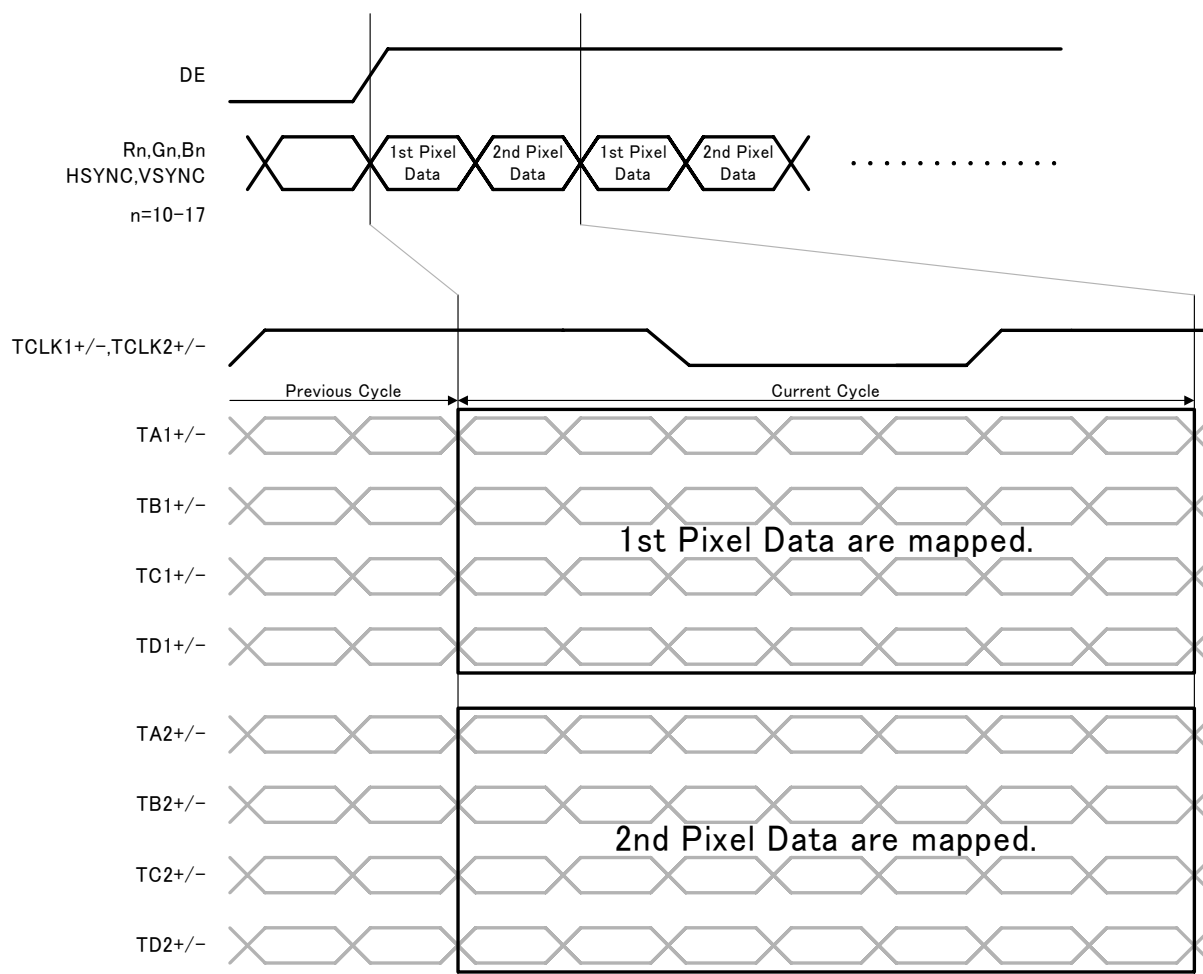


Fig7. Single-In / Dual-Out Mode (MODE=L)

## Single-In / Single-Out Mode (MODE=H)

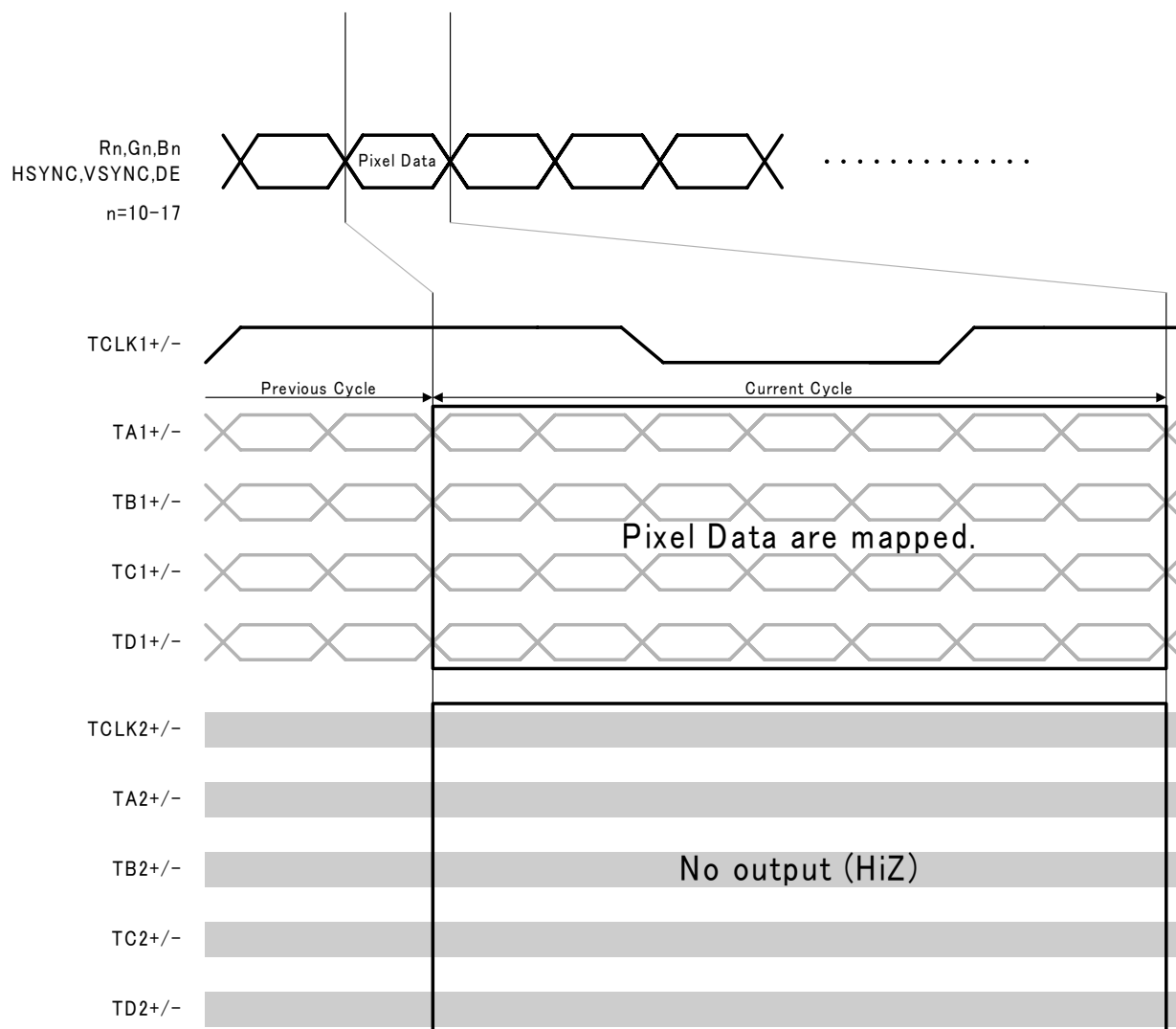
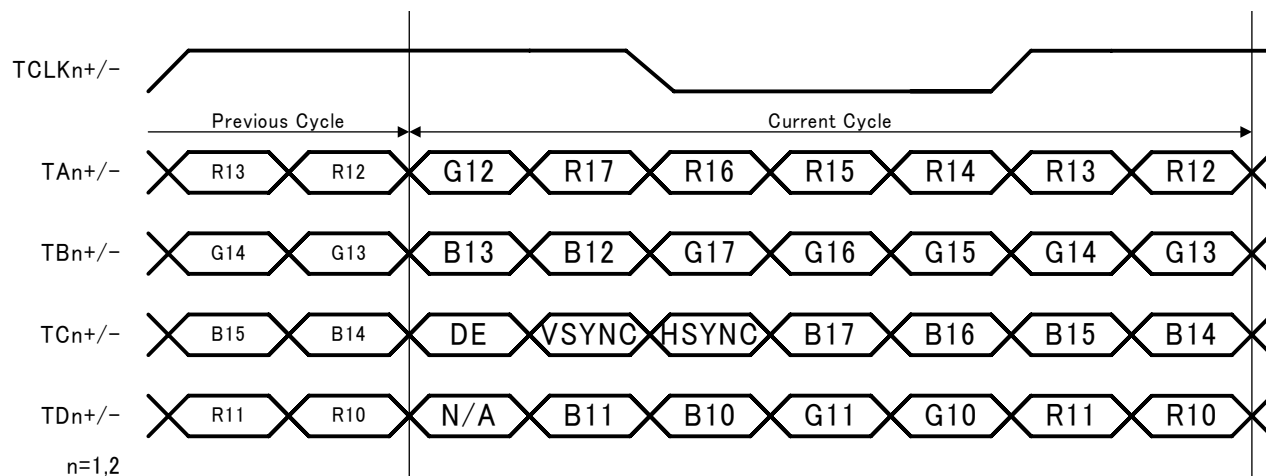
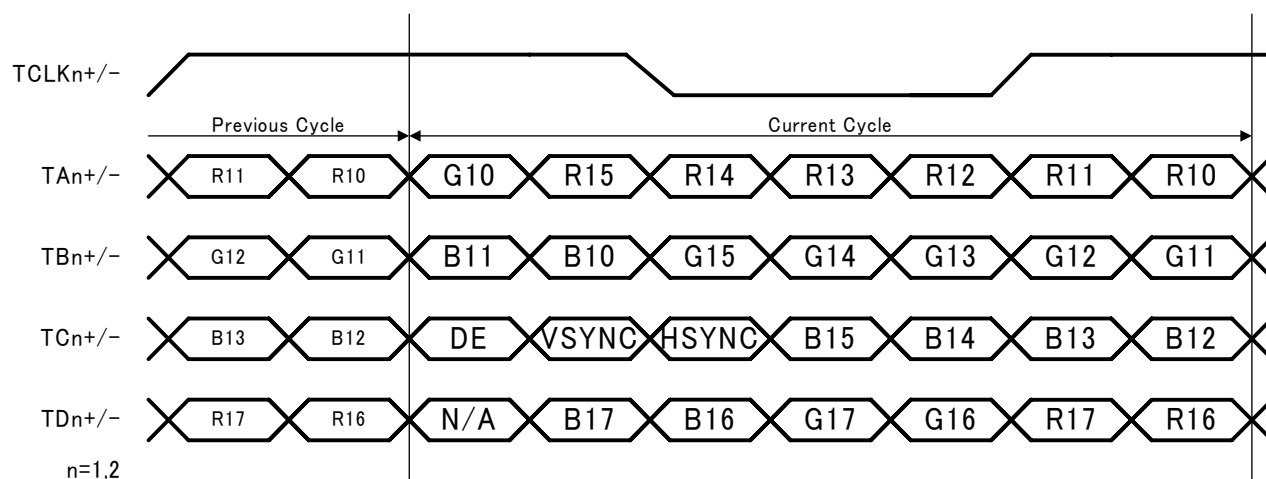


Fig8. Single-In / Single-Out Mode (MODE=H)

## LVDS Data Mapping for 8 bit mode (6B/8B=L)



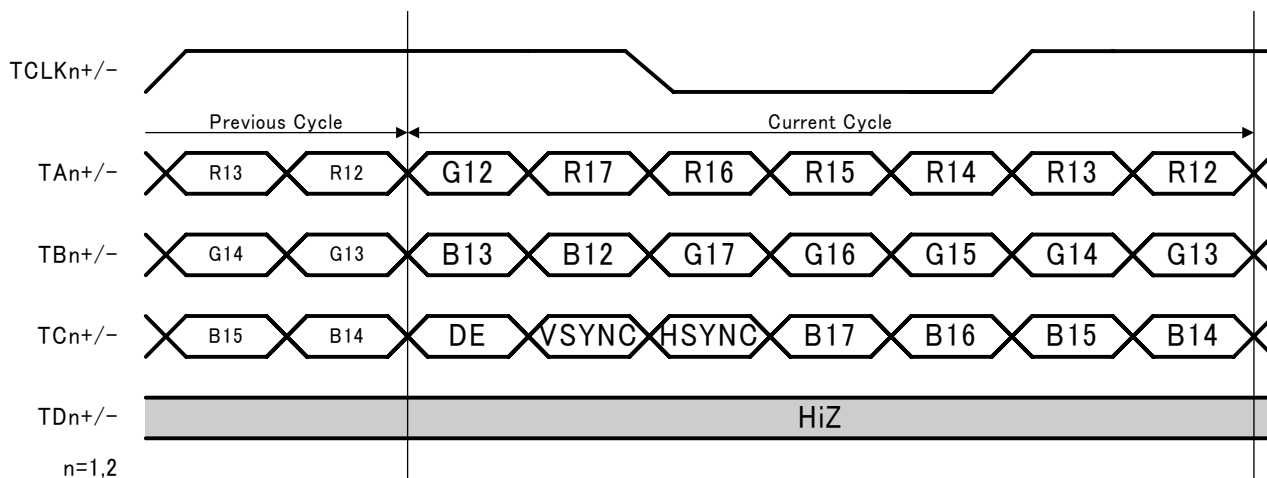
(a) LVDS Data Mapping when MAP = H (Mapping Mode 1)



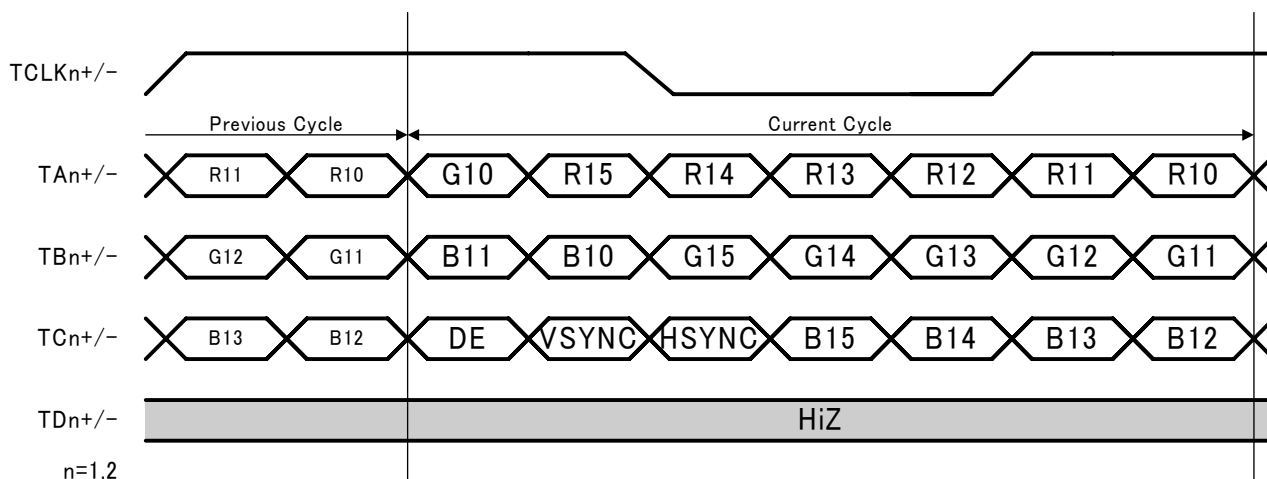
(b) LVDS Data Mapping when MAP = L (Mapping Mode 2)

Fig9. LVDS Data Mapping for 8 bit mode (6B/8B=L)

## LVDS Data Mapping for 6 bit mode (6B/8B=H)



(a) LVDS Data Mapping when MAP = H (Mapping Mode 1)



(b) LVDS Data Mapping when MAP = L (Mapping Mode 2)

Fig10. LVDS Data Mapping for 6 bit mode (6B/8B=H)

Note: Input pins which are not used in 6 bit mode (R10-11, G10-11, B10-11 on Mapping Mode 1, R16-17, G16-17, B16-17 on Mapping Mode 2) can be H, L, or Open.

## Note

### 1)Cable Connection and Disconnection

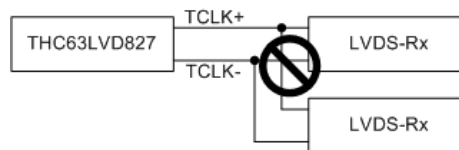
Don't connect and disconnect the LVDS cable, when the power is supplied to the system.

### 2)GND Connection

Connect the each GND of the PCB which THC63LVD827 and LVDS-Rx on it. It is better for EMI reduction to place GND cable as close to LVDS cable as possible.

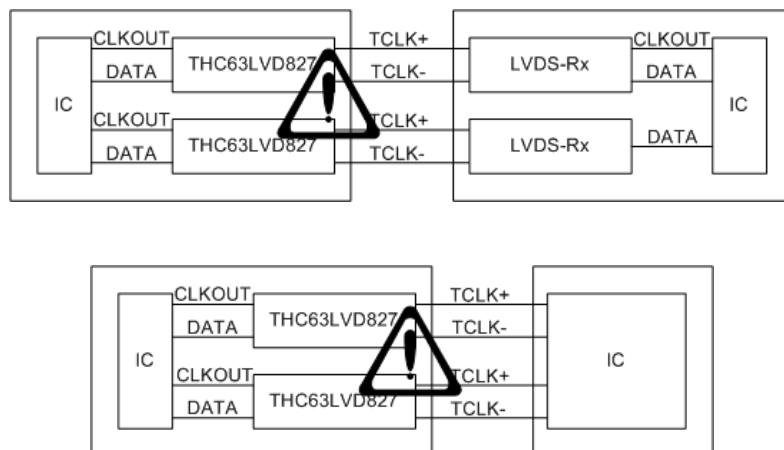
### 3)Multi Drop Connection

Multi drop connection is not recommended.



### 4)Asynchronous use

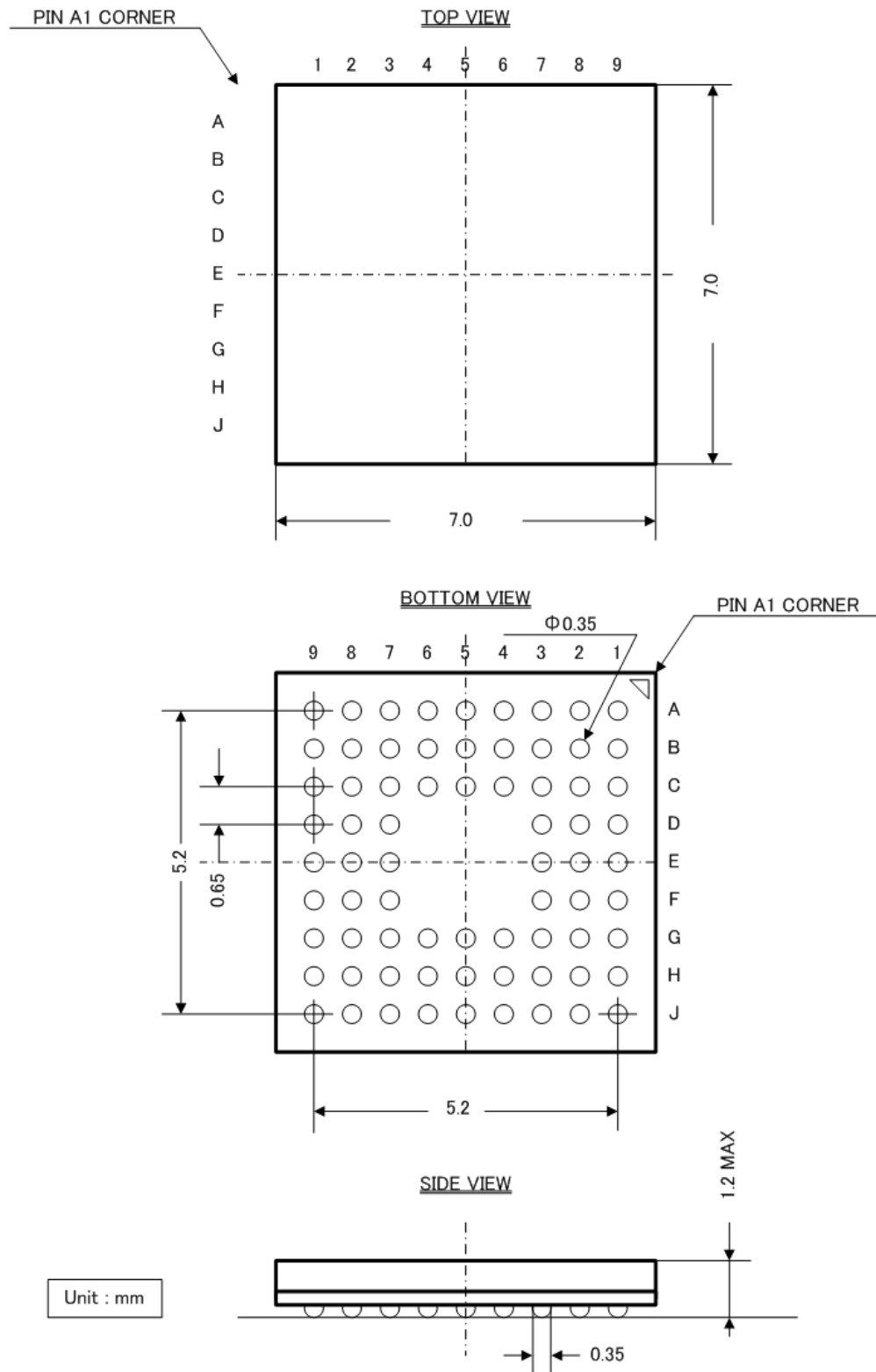
Asynchronous use such as following systems are not recommended.





## Package

TFBGA



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#### Как с нами связаться

**Телефон:** 8 (812) 309 58 32 (многоканальный)

**Факс:** 8 (812) 320-02-42

**Электронная почта:** [org@eplast1.ru](mailto:org@eplast1.ru)

**Адрес:** 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.