

TOSHIBA Field Effect Transistor Silicon N Channel MOS Type (U-MOS III)

## SSM3K15AFU

### Load Switching Applications

- 2.5 V drive
- Low ON-resistance:  $R_{DS(ON)} = 3.6 \Omega$  (max) (@ $V_{GS} = 4$  V)  
 $R_{DS(ON)} = 6.0 \Omega$  (max) (@ $V_{GS} = 2.5$  V)

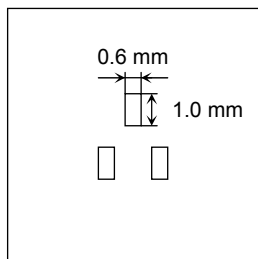
### Absolute Maximum Ratings ( $T_a = 25^\circ\text{C}$ )

Characteristics	Symbol	Rating	Unit
Drain-Source voltage	$V_{DSS}$	30	V
Gate-Source voltage	$V_{GSS}$	$\pm 20$	V
Drain current	DC	$I_D$	mA
	Pulse	$I_{DP}$	
Power dissipation	$P_D$ (Note 1)	150	mW
Channel temperature	$T_{ch}$	150	$^\circ\text{C}$
Storage temperature range	$T_{stg}$	-55 to 150	$^\circ\text{C}$

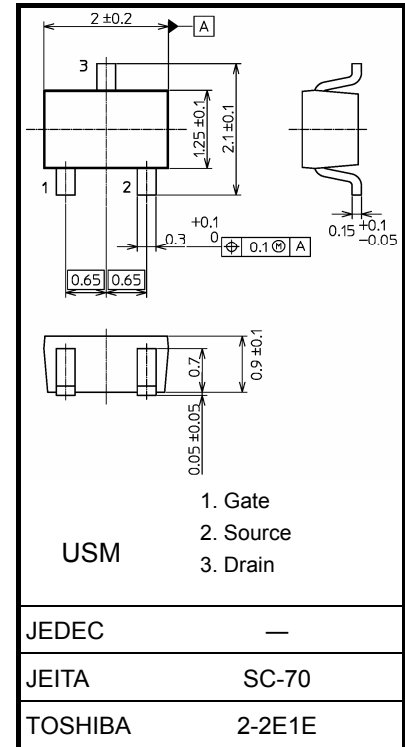
Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Mounted on FR4 board (25.4 mm  $\times$  25.4 mm  $\times$  1.6mm , Cu Pad : 0.6mm<sup>2</sup>  $\times$  3)

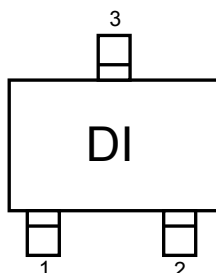


Unit: mm

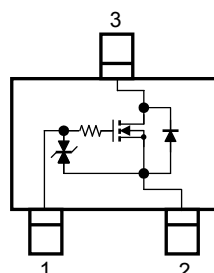


Weight: 6.0 mg (typ.)

### Marking



### Equivalent Circuit (top view)



Start of commercial production  
2012-08

## Electrical characteristics (Ta = 25°C)

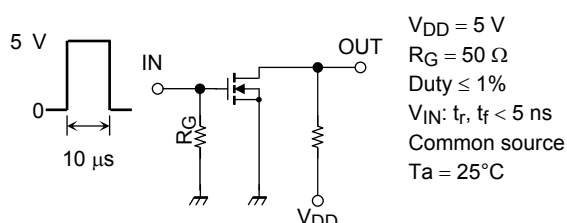
Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Drain-Source breakdown voltage	$V_{(BR)DSS}$	$I_D = 0.1 \text{ mA}$ , $V_{GS} = 0 \text{ V}$	30	—	—	V
	$V_{(BR)DSX}$	$I_D = 0.1 \text{ mA}$ , $V_{GS} = -10 \text{ V}$ (Note 3)	16	—	—	
Drain cut-off current	$I_{DSS}$	$V_{DS} = 30 \text{ V}$ , $V_{GS} = 0 \text{ V}$	—	—	1	$\mu\text{A}$
Gate leakage current	$I_{GSS}$	$V_{GS} = \pm 16 \text{ V}$ , $V_{DS} = 0 \text{ V}$	—	—	$\pm 1$	$\mu\text{A}$
Gate threshold voltage	$V_{th}$	$V_{DS} = 3 \text{ V}$ , $I_D = 0.1 \text{ mA}$	0.8	—	1.5	V
Forward transfer admittance	$ Y_{fs} $	$V_{DS} = 3 \text{ V}$ , $I_D = 10 \text{ mA}$ (Note 2)	35	—	—	mS
Drain-Source ON-resistance	$R_{DS(ON)}$	$I_D = 10 \text{ mA}$ , $V_{GS} = 4 \text{ V}$ (Note 2)	—	2.3	3.6	$\Omega$
		$I_D = 10 \text{ mA}$ , $V_{GS} = 2.5 \text{ V}$ (Note 2)	—	3.5	6.0	
Input capacitance	$C_{iss}$	$V_{DS} = 3 \text{ V}$ , $V_{GS} = 0 \text{ V}$ , $f = 1 \text{ MHz}$	—	13.5	—	pF
Output capacitance	$C_{oss}$		—	8.0	—	
Reverse transfer capacitance	$C_{rss}$		—	6.5	—	
Switching time	Turn-on time	$V_{DD} = 5 \text{ V}$ , $I_D = 10 \text{ mA}$ $V_{GS} = 0 \text{ to } 5 \text{ V}$ , $R_G = 50 \Omega$	—	5.5	—	ns
	Turn-off time		—	35	—	
Drain-source forward voltage	$V_{DSF}$	$I_D = -100 \text{ mA}$ , $V_{GS} = 0 \text{ V}$ (Note 2)	—	-0.85	-1.2	V

Note 2: Pulse test

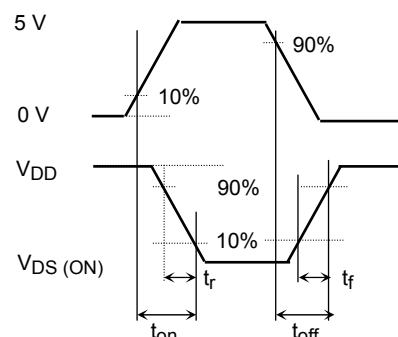
Note 3: If a reverse bias is applied between gate and source, this device enters  $V_{(BR)DSX}$  mode. Note that the drain-source breakdown voltage is lowered in this mode

## Switching Time Test Circuit

### (a) Test circuit



### (b) $V_{IN}$



### (c) $V_{OUT}$

## Precaution

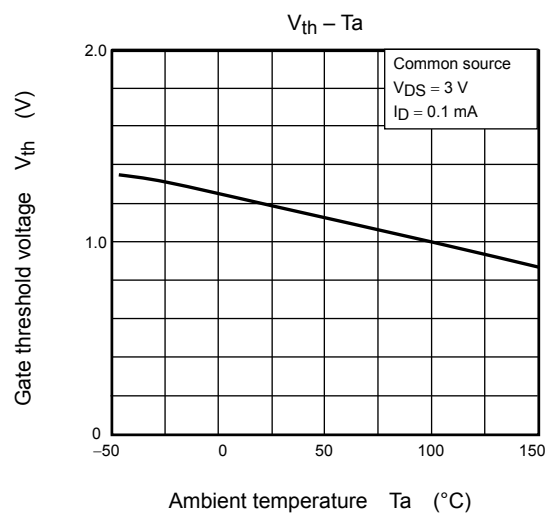
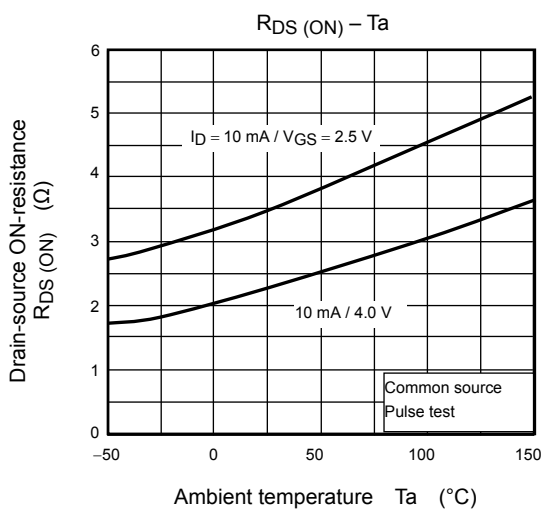
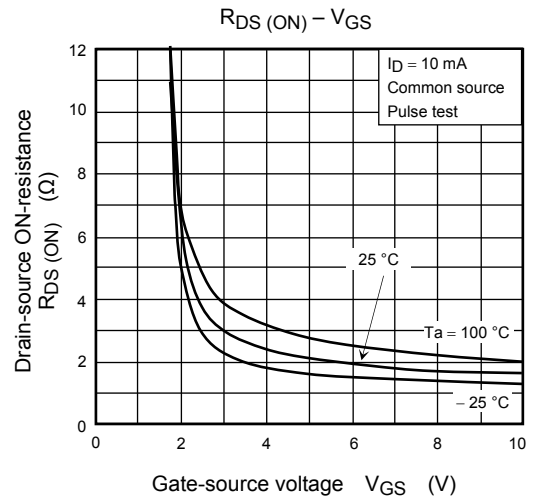
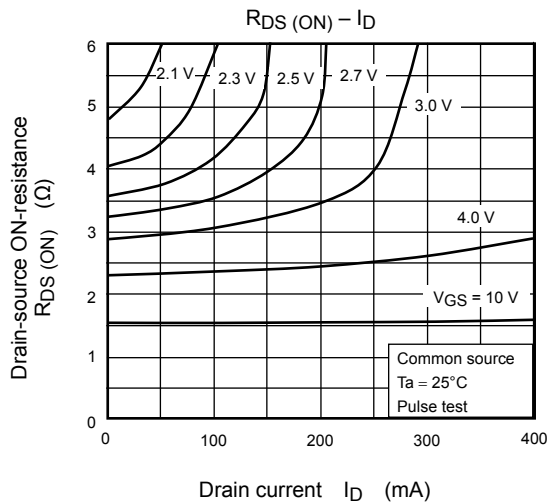
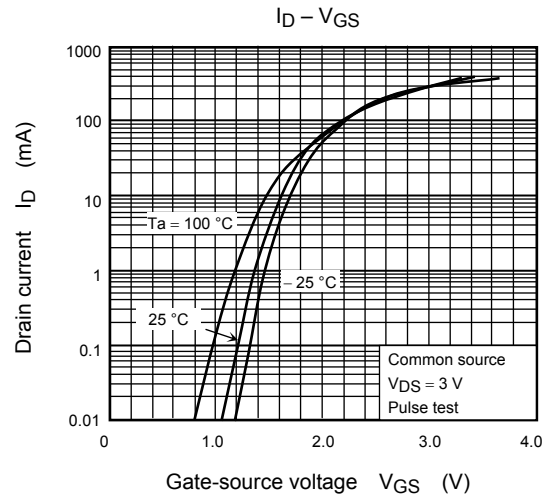
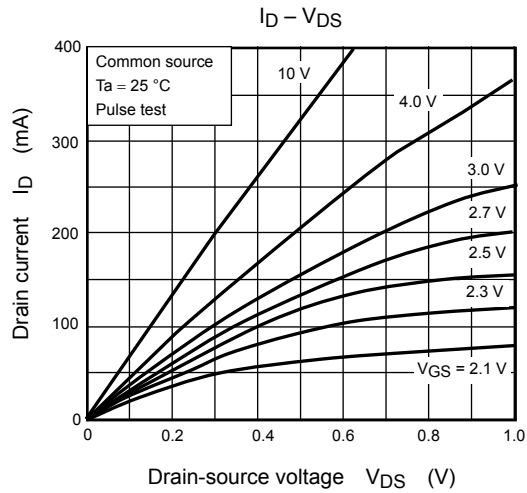
$V_{th}$  can be expressed as voltage between gate and source when low operating current value is  $I_D = 0.1 \text{ mA}$  for this product. For normal switching operation,  $V_{GS(on)}$  requires higher voltage than  $V_{th}$  and  $V_{GS(off)}$  requires lower voltage than  $V_{th}$ . (Relationship can be established as follows:  $V_{GS(off)} < V_{th} < V_{GS(on)}$ ) Please take this into consideration for using the device.

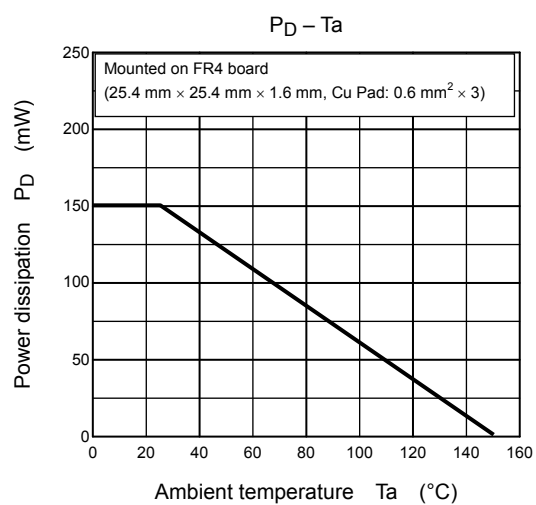
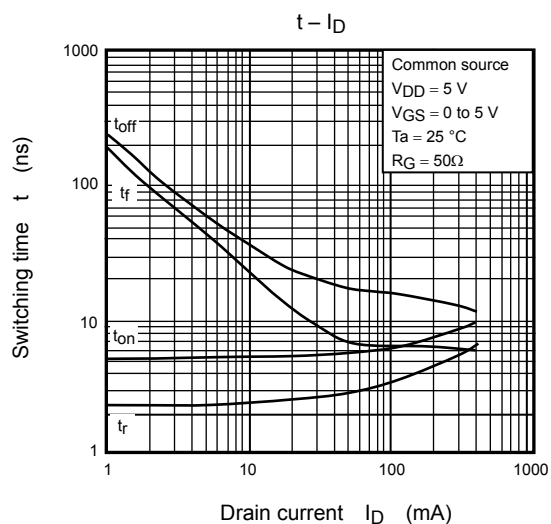
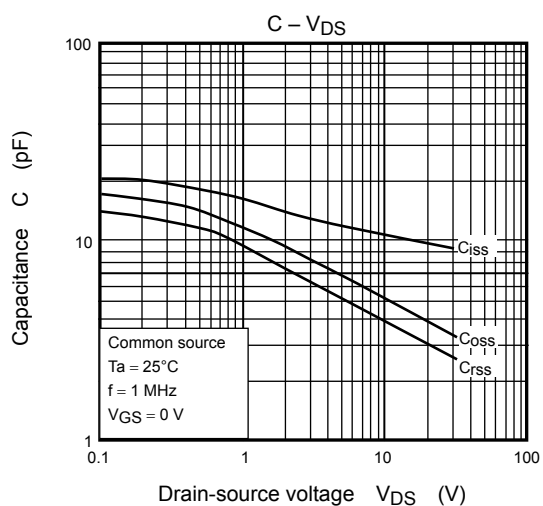
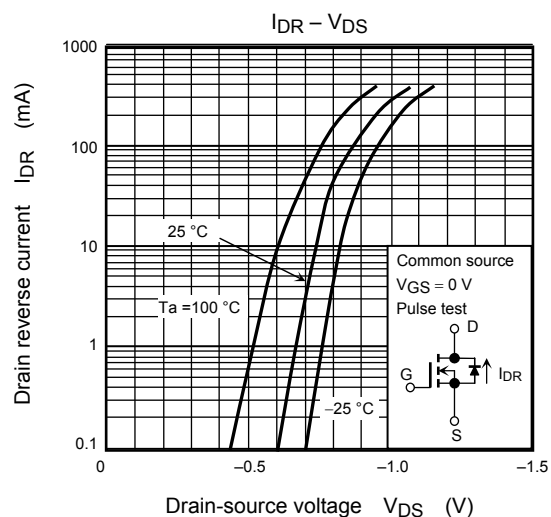
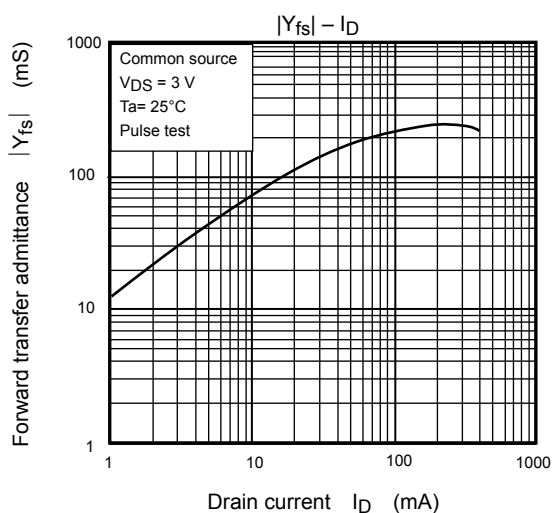
Do not use this device under avalanche mode. It may cause the device to break down.

## Handling Precaution

When handling individual devices (which are not yet mounting on a circuit board), be sure that the environment is protected against electrostatic electricity. Operators should wear anti-static clothing, and containers and other objects that come into direct contact with devices should be made of anti-static materials.

Thermal resistance  $R_{th(ch-a)}$  and power dissipation  $P_D$  vary depending on board material, board area, board thickness and pad area. When using this device, please take heat dissipation into consideration





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