# CY25561

# Spread Spectrum Clock Generator

## Features

- 50 to 166 MHz Operating Frequency Range
- Wide Range of Spread Selections:9
- Accepts Clock and Crystal Inputs
- Low Power Dissipation
  - 70 mW–Typ at 66 MHz
- Frequency Spread Disable Function
- Center Spread Modulation
- Low Cycle-to-cycle Jitter
- 8-pin SOIC Package

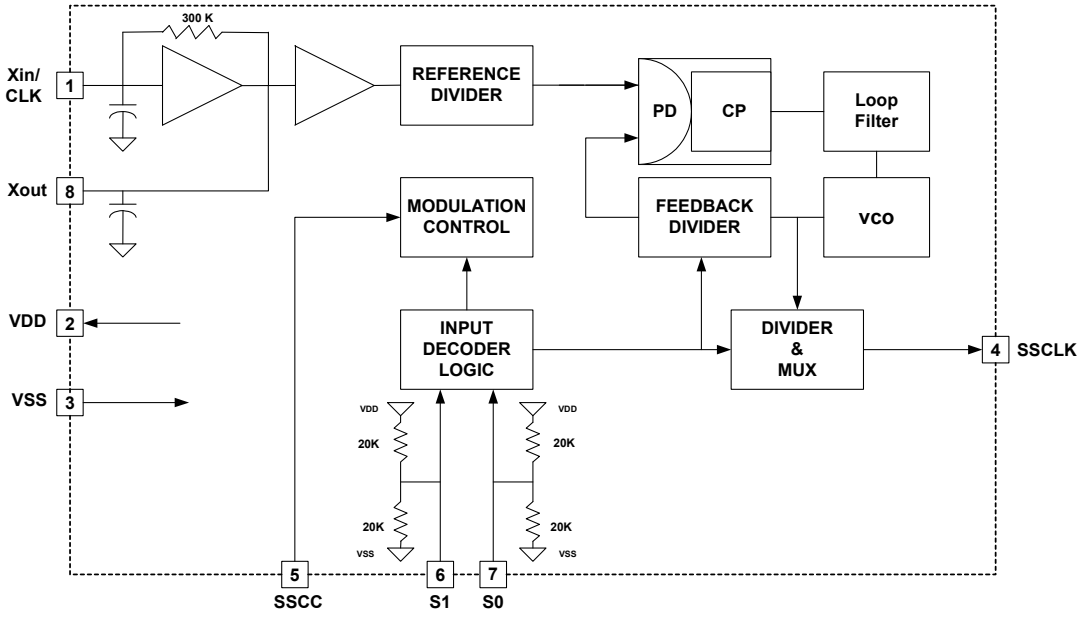
## Applications

- Desktop, notebook, and tablet PCs
- VGA controllers
- LCD panels and monitors
- Workstations and servers

## Benefits

- Peak EMI reduction by 8 to16 dB
- Fast time to market
- Cost reduction

## Logic Block Diagram



## Pinout

**Figure 1. Pin Configuration**

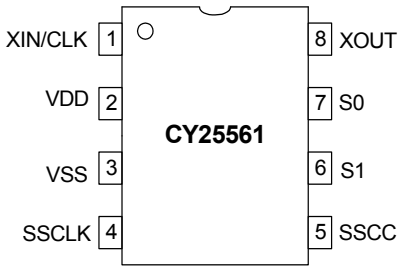



**Table 1. Pin Description**

| Pin | Name | Type | Description |
|---|---|---|---|
| 1 | Xin/CLK | I | Clock or crystal connection input. Refer to Table 2 for input frequency range selection. |
| 2 | VDD | P | Positive power supply |
| 3 | GND | P | Power supply ground |
| 4 | SSCLK | O | Modulated clock output |
| 5 | SSCC | I | Spread spectrum clock control (enable/disable) function. SSCG function is enabled when input is high and disabled when input is low. This pin is pulled high internally. |
| 6 | S1 | I | Tri-level logic input control pin used to select frequency and bandwidth. Frequency/Bandwidth selection and tri-level logic programming. See Figure 2. Pin 6 has internal resistor divider network to $V_{DD}$ and $V_{SS}$. Refer to Logic Block Diagram on page 1. |
| 7 | S0 | I | Tri-level logic input control pin used to select frequency and bandwidth. Frequency/Bandwidth selection and tri-level logic programming. See Figure 2. Pin 7 has internal resistor divider network to $V_{DD}$ and $V_{SS}$. Refer to Logic Block Diagram on page 1. |
| 8 | Xout | O | Oscillator output pin connected to crystal. Leave this pin unconnected If an external clock drives Xin/CLK. |

## General Description

CY25561 is a spread spectrum clock generator (SSCG) IC used to reduce electromagnetic Interference (EMI) found in today's high speed digital electronic systems.

CY25561 uses a Cypress proprietary Phase Locked Loop (PLL) and Spread Spectrum Clock (SSC) technology to synthesize and frequency modulate the input frequency of the reference clock. By doing this, the measured EMI at the fundamental and harmonic frequencies of clock (SSCLK) is reduced.

This reduction in radiated energy can significantly reduce the cost of complying with regulatory requirements and time to market without degrading the system performance.

CY25561 is a very simple and versatile device to use. The frequency and spread percentage range is selected by programming S0 and S1 digital inputs. These inputs use three logic states including high (H), low (L), and middle (M) logic levels to select one of the nine available spread percentage ranges. Refer to Table 2 for programming details.

CY25561 is intended for use with applications with a reference frequency in the range of 50 to 166 MHz.

A wide range of digitally selectable spread percentages is made possible by using tri-level (high, low, and middle) logic at the S0 and S1 digital control inputs.

The output spread (frequency modulation) is symmetrically centered on the input frequency.

Spread spectrum clock control (SSCC) function enables or disables the frequency spread and is provided for easy comparison of system performance during EMI testing.

CY25561 is available in an eight-pin SOIC package with a 0°C to 70°C operating temperature range.

**Note**: Refer to the CY25560 data sheet for operation at frequencies from 25 to100 MHz.

**Table 2. Frequency and Spread Percentage Selection (Center Spread)**

**50–100 MHz (Low Range)**

| Input Frequency (MHz) | S1=M S0=M (%) | S1=M S0=0 (%) | S1=1 S0=0 (%) | S1=0 S0=0 (%) | S1=0 S0=M (%) |
|---|---|---|---|---|---|
| 50 - 60 | 4.3 | 3.9 | 3.3 | 2.9 | 2.7 |
| 60 - 70 | 4.0 | 3.6 | 3.1 | 2.6 | 2.5 |
| 70 - 80 | 3.8 | 3.4 | 2.9 | 2.5 | 2.4 |
| 80 - 100 | 3.5 | 3.1 | 2.7 | 2.2 | 2.1 |

Select the Frequency and Center Spread % desired and then set S1, S0 as indicated.

**100–166 MHz (High Range)**

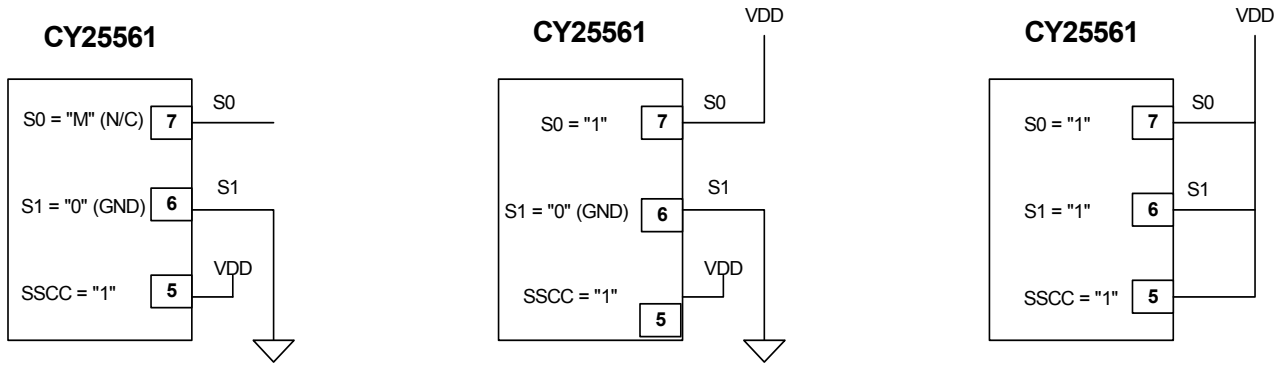
| Input Frequency (MHz) | S1=1 S0=M (%) | S1=0 S0=1 (%) | S1=1 S0=1 (%) | S1=M S0=1 (%) |
|---|---|---|---|---|
| 100 - 120 | 3.0 | 2.4 | 1.5 | 1.3 |
| 120 -130 | 2.7 | 2.1 | 1.4 | 1.1 |
| 130 - 140 | 2.6 | 2.0 | 1.3 | 1.1 |
| 140 - 150 | 2.6 | 2.0 | 1.3 | 1.1 |
| 150 - 166 | 2.5 | 1.8 | 1.2 | 1.0 |

Select the Frequency and Center Spread % desired and then set S1, S0 as indicated.

## Tri-level Logic

With binary logic, four states can be programmed with two control lines, whereas tri-level logic can program nine logic states using two control lines. Tri-level logic in CY25561 is implemented by defining a third logic state in addition to the standard logic “1” and “0”. Pins 6 and 7 of CY25561 recognize a logic state by the voltage applied to the respective pin. These states are defined as “0” (low), “M” (middle), and “1” (one). Each of these states has a defined voltage range that is interpreted by CY25561 as a “0,” “M,” or “1” logic state. Refer to Table 3 for voltage ranges for each logic state. CY25561 has two equal value resistors connected internally to pin 6 and pin 7 that produce the default “M” state. Pins 6 and/or 7 can be tied directly to ground or $V_{DD}$ to program a logic “0” or “1” state, respectively. Refer to Figure 2 for examples.

**Figure 2. Tri-level Logic Examples**



## SSCG Theory of Operation

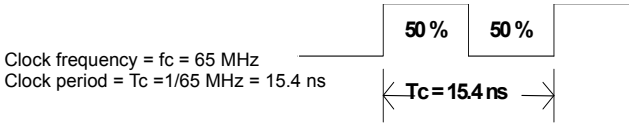
CY25561 is a PLL-type clock generator using a proprietary Cypress design. By precisely controlling the bandwidth of the output clock, CY25561 becomes a low-EMI clock generator. The theory and detailed operation of CY25561 is discussed in the following sections.

## EMI

All digital clocks generate unwanted energy in their harmonics. Conventional digital clocks are square waves with a duty cycle that is very close to 50 percent. Because of this 50/50 duty cycle, digital clocks generate most of their harmonic energy in odd harmonics, that is; third, fifth, seventh, etc. The amount of energy contained in the fundamental and odd harmonics can be reduced by increasing the bandwidth of the fundamental clock frequency. Conventional digital clocks have a very high Q factor; all the energy at that frequency is concentrated in a very narrow bandwidth, and consequently, higher energy peaks. Regulatory agencies test electronic equipment by the amount of peak energy radiated from the equipment. By reducing the peak energy at the fundamental and harmonic frequencies, the equipment under test is able to satisfy agency requirements for EMI. Conventional methods of reducing EMI use shielding, filtering, multilayer PCBs, etc. CY25561 uses the approach of reducing the peak energy in the clock by increasing the clock bandwidth, and lowering the Q.

## SSCG

SSCG uses a patented technology of modulating the clock over a very narrow bandwidth and controlled rate of change, both peak and cycle-to-cycle. CY25561 takes a narrow band digital reference clock in the range of 50 to166 MHz and produces a clock that sweeps between a controlled start and stop frequency and precise rate of change. To understand what happens to a clock when SSCG is applied, consider a 65 MHz clock with a 50 percent duty cycle, as shown in the following figure:




If this clock is applied to the Xin/CLK pin of CY25561, the output clock at pin 4 (SSCLK) sweeps back and forth between two frequencies. These two frequencies, F1 and F2, are used to calculate total amount of spread or bandwidth applied to the reference clock at pin 1. As the clock is making the transition from F1 to F2, the amount of time and sweep waveform play a very important role in the amount of EMI reduction realized from an SSCG clock.

The modulation domain analyzer is used to visualize the sweep waveform and sweep period. Figure 4 shows the modulation profile of a 65 MHz SSCG clock. Notice that the actual sweep waveform is not a simple sine or sawtooth waveform. Figure 4 also shows a scan of the same SSCG clock using a spectrum analyzer. In this scan, you can see a 6.48 dB reduction in the peak RF energy when using the SSCG clock.



[+] Feedback

## Modulation Rate

Spectrum spread clock generators use frequency modulation (FM) to distribute energy over a specific band of frequencies. The maximum frequency of the clock (Fmax) and minimum frequency of the clock (Fmin) determine this band of frequencies. The time required to transition from Fmin to Fmax and back to Fmin is the period of the modulation rate, Tmod. Modulation rates of SSCG clocks are most commonly referred to in terms of frequency or Fmod = 1/Tmod.

The input clock frequency, Fin, and the internal divider count, Cdiv, determine the modulation rate. In some SSCG clock generators, the selected range determines the internal divider count. In other SSCG clocks, the internal divider count is fixed over the operating range of the part. CY25561 has a fixed divider count, as shown in Figure 3.

**Figure 3. SSCG Clock, Part Number, Fin = 65 MHz**

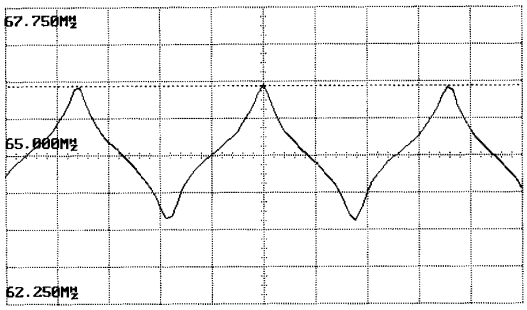
| **Device** | **Cdiv** |
|---|---|
| CY25561 | 2332 (All Ranges) |

Example:

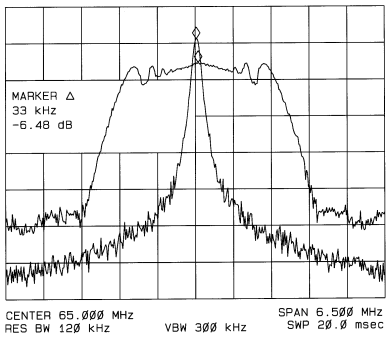
Device = CY25561
Fin = 65 MHz
Range = S1 = 1, S0 = 0

Then;

Modulation Rate = Fmod = 65 MHz/2332 = 27.9 kHz.




**Modulation Profile**



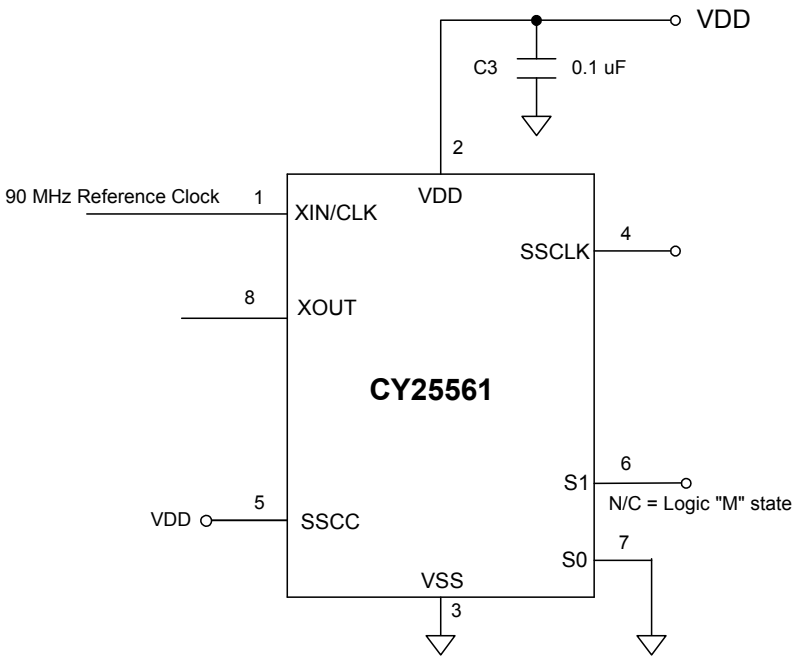

**Spectrum Analyzer**



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## Part Number Application Schematic

**Figure 4. Application Schematic**




The schematic in Figure 4 above demonstrates how CY25561 is configured in a typical application. This application is using a 90 MHz reference clock connected to pin 1. Because an external reference clock is used, pin 8 (XOUT) is left unconnected.

Figure 4 shows that pin 6 has no connection, which programs the logic “M” state, due to the internal resistor divider network of CY25561. Programming a logic “0” state is as simple as connecting to logic ground, as shown on pin 7.

With this configuration, CY25561 produces an SSCG clock that is at a center frequency of 90 MHz. Referring to Table 3, range “M, 0” at 90 MHz generates a modulation profile that has a 3.1percent peak-to-peak spread.

## Absolute Maximum Ratings[1, 2]

Supply voltage ($V_{DD}$) .....–0.5V to +6.0V
DC input voltage ..... –0.5V to $V_{DD}$ + 0.5V
Junction temperature..... –40°C to +140°C
Operating temperature ..... 0°C to 70°C
Storage temperature..... –65°C to +150°C
Static discharge voltage (ESD)..... 2,000V min

**Table 3. DC Electrical Characteristics** $V_{DD}$ = 3.3V, $T_A$ = 25°C and $C_L$ (pin 4) = 15 pF, unless otherwise noted

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Power supply range | ±10% | 2.97 | 3.3 | 3.63 | V |
| $V_{INH}$ | Input high voltage | S0 and S1 only. | $0.85V_{DD}$ | $V_{DD}$ | $V_{DD}$ | V |
| $V_{INM}$ | Input middle voltage | S0 and S1 only. | $0.40V_{DD}$ | $0.50V_{DD}$ | $0.60V_{DD}$ | V |
| $V_{INL}$ | Input low voltage | S0 and S1 only. | 0.0 | 0.0 | $0.15V_{DD}$ | V |
| $V_{OH1}$ | Output high voltage | $I_{OH}$ = 6 ma | 2.4 | | | V |
| $V_{OH2}$ | Output high voltage | $I_{OH}$ = 20 ma | 2.0 | | | V |
| $V_{OL1}$ | Output low voltage | $I_{OH}$ = 6 ma | | | 0.4 | V |
| $V_{OL2}$ | Output low voltage | $I_{OH}$ = 20 ma | | | 1.2 | V |
| $C_{in1}$ | Input capacitance | Xin/CLK (pin 1) | 3 | 4 | 5 | pF |
| $C_{in2}$ | Input capacitance | Xout (pin 8) | 6 | 8 | 10 | pF |
| $C_{in2}$ | Input capacitance | S0, S1, SSCC (pins 7, 6, 5) | 3 | 4 | 5 | pF |
| $I_{DD1}$ | Power supply current | Fin = 65 MHz, CL = 0 | | 23 | 30 | mA |
| $I_{DD2}$ | Power supply current | Fin = 166 MHz, CL = 0 | | 48 | 60 | mA |

**Table 4. Electrical Timing Characteristics** $V_{DD}$ = 3.3V, $T_A$ = 25°C and $C_L$ = 15 pF, unless otherwise noted

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{CLKFR}$ | Input clock frequency range | $V_{DD}$ = 3.3V | 50 | | 166 | MHz |
| $t_{RISE}$ | Clock rise time (pin 4) | SSCLK1 @ 0.4–2.4V | 1.1 | 1.4 | 1.7 | ns |
| $t_{FALL}$ | Clock fall time (pin 4) | SSCLK1 @ 0.4–2.4V | 1.1 | 1.4 | 1.7 | ns |
| $D_{TYin}$ | Input clock duty cycle | XIN/CLK (pin 1) | 30 | 50 | 70 | % |
| $D_{TYout}$ | Output clock duty cycle | SSCLK1 (pin 4) | 45 | 50 | 55 | % |
| $C_{CJ1}$ | Cycle-to-Cycle jitter | 50 – 100 MHz, (S1 = M, S0 = M) | – | 150 | 225 | ps |
| $C_{CJ2}$ | Cycle-to-Cycle jitter | 100 – 166 MHz, (S1 = 1, S0 = M) | – | 200 | 300 | ps |

## Ordering Information

| Part Number | Package Type | Product Flow |
|---|---|---|
| CY25561SXC | 8-pin SOIC, Pb-free | Commercial, 0° to 70°C |
| CY25561SXCT | 8-pin SOIC – tape and reel, Pb-free | Commercial, 0° to 70°C |

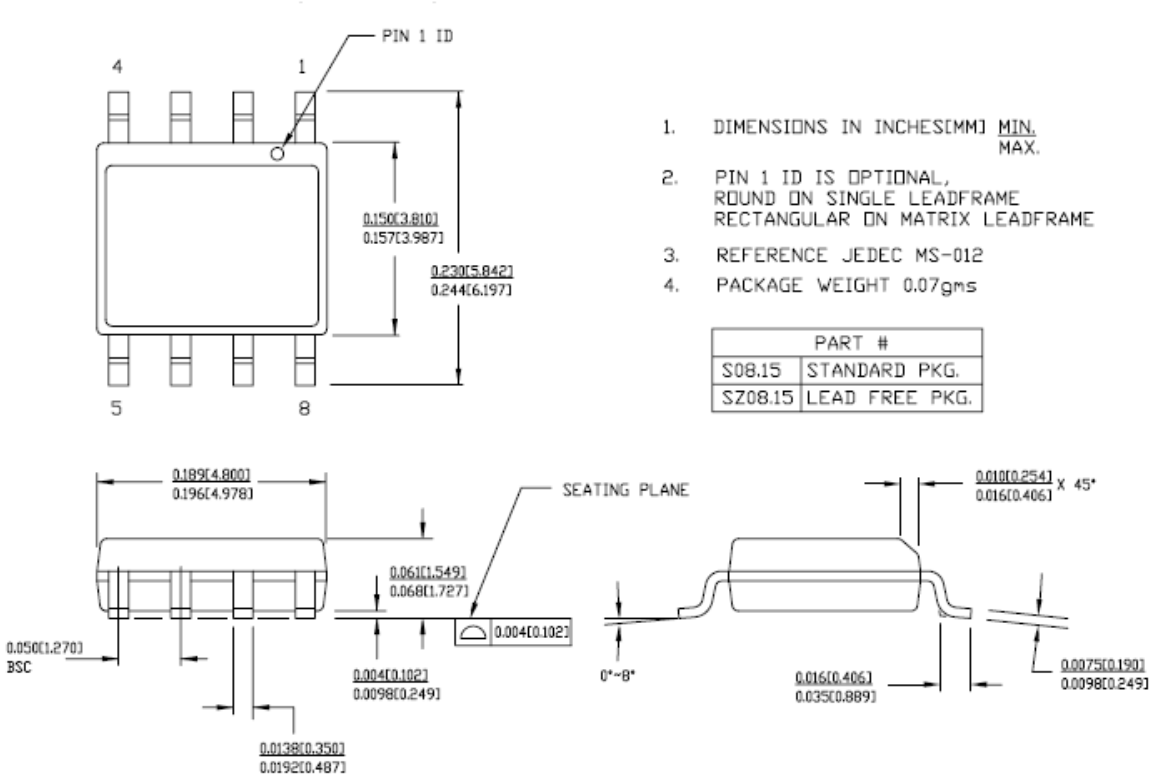
**Notes**
1. Operation at any absolute maximum rating is not implied.
2. Single power supply: The voltage on any input or I/O pin cannot exceed the power pine during power-up.



[+] Feedback

## Package Drawing and Dimensions

**Figure 5. 8 Lead (150 Mil) SOIC-SO8**




51-85066 *C



[+] Feedback

## Document History Page

| Document Title: CY25561 Spread Spectrum Clock Generator<br>Document Number: 38-07242 | | | | |
|---|---|---|---|---|
| **Rev.** | **ECN No.** | **Submission Date** | **Orig. of Change** | **Description of Change** |
| ** | 115369 | 07/05/02 | OXC | New Data Sheet |
| *A | 119443 | 10/17/02 | RGL | Corrected the values in the Absolute Maximum Ratings to match the device. |
| *B | 122694 | 12/27/02 | RBI | Added power up requirements to maximum rating information. |
| *C | 2567245 | 09/16/08 | PYG/KVM/ AESA | Replaced CY25561SC w/ CY25561SXC, CY255651SCT w/ CY25561SXCT.<br>Package changed from S8 to SZ8.<br>Updated template. |

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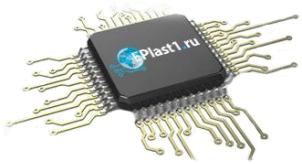
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