



# PSMN015-100B

N-channel TrenchMOS SiliconMAX standard level FET

Rev. 06 — 17 December 2009

Product data sheet

## 1. Product profile

### 1.1 General description

SiliconMAX standard level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product is designed and qualified for use in computing, communications, consumer and industrial applications only.

### 1.2 Features and benefits

- Low conduction losses due to low on-state resistance
- Rated for avalanche ruggedness

### 1.3 Applications

- DC-to-DC convertors
- Switched-mode power supplies

### 1.4 Quick reference data

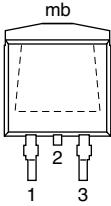
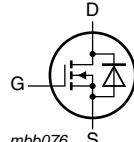
Table 1. Quick reference

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25^\circ\text{C}; T_j \leq 175^\circ\text{C}$	-	-	100	V
$I_D$	drain current	$T_{mb} = 25^\circ\text{C}; V_{GS} = 10\text{ V}$ ; see <a href="#">Figure 1</a> and <a href="#">3</a>	-	-	75	A
$P_{tot}$	total power dissipation	$T_{mb} = 25^\circ\text{C}$ ; see <a href="#">Figure 2</a>	-	-	300	W
<b>Dynamic characteristics</b>						
$Q_{GD}$	gate-drain charge	$V_{GS} = 10\text{ V}; I_D = 75\text{ A};$ $V_{DS} = 80\text{ V}; T_j = 25^\circ\text{C}$ ; see <a href="#">Figure 11</a>	-	35	-	nC
<b>Static characteristics</b>						
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 25\text{ A};$ $T_j = 25^\circ\text{C}$ ; see <a href="#">Figure 9</a> and <a href="#">10</a>	-	12	15	mΩ

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## 2. Pinning information

**Table 2. Pinning information**

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		
2	D	drain	[1]	
3	S	source		
mb	D	mounting base; connected to drain		
				<b>SOT404 (D2PAK)</b>

[1] It is not possible to make a connection to pin 2.

## 3. Ordering information

**Table 3. Ordering information**

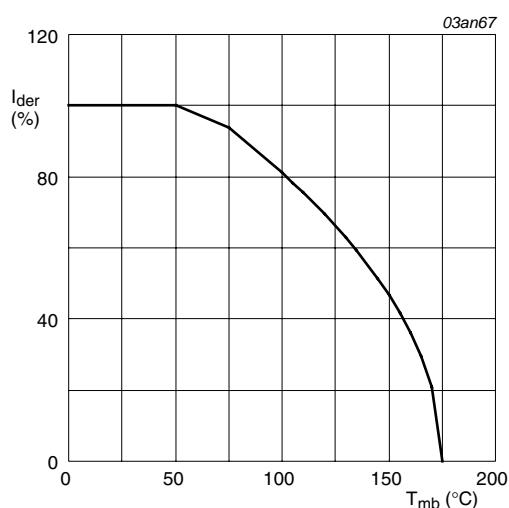
Type number	Package		Version
	Name	Description	
PSMN015-100B	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404

## 4. Limiting values

**Table 4. Limiting values**

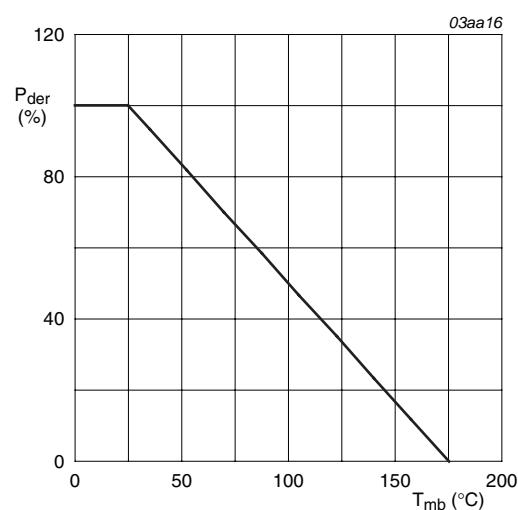
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25^\circ\text{C}; T_j \leq 175^\circ\text{C}$	-	100	V
$V_{DGR}$	drain-gate voltage	$T_j \leq 175^\circ\text{C}; T_j \geq 25^\circ\text{C}; R_{GS} = 20\text{ k}\Omega$	-	100	V
$V_{GS}$	gate-source voltage		-20	20	V
$I_D$	drain current	$V_{GS} = 10\text{ V}; T_{mb} = 100^\circ\text{C}$ ; see <a href="#">Figure 1</a>	-	60.8	A
		$V_{GS} = 10\text{ V}; T_{mb} = 25^\circ\text{C}$ ; see <a href="#">Figure 1</a> and <a href="#">3</a>	-	75	A
$I_{DM}$	peak drain current	$t_p \leq 10\text{ }\mu\text{s}$ ; pulsed; $T_{mb} = 25^\circ\text{C}$ ; see <a href="#">Figure 3</a>	-	240	A
$P_{tot}$	total power dissipation	$T_{mb} = 25^\circ\text{C}$ ; see <a href="#">Figure 2</a>	-	300	W
$T_{stg}$	storage temperature		-55	175	°C
$T_j$	junction temperature		-55	175	°C
<b>Source-drain diode</b>					
$I_S$	source current	$T_{mb} = 25^\circ\text{C}$	-	75	A
$I_{SM}$	peak source current	$t_p \leq 10\text{ }\mu\text{s}$ ; pulsed; $T_{mb} = 25^\circ\text{C}$	-	240	A
<b>Avalanche ruggedness</b>					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}; T_{j(\text{init})} = 25^\circ\text{C}; I_D = 36\text{ A}; V_{sup} \leq 50\text{ V}$ ; unclamped; $t_p = 0.11\text{ ms}$ ; $R_{GS} = 50\text{ }\Omega$	-	320	mJ



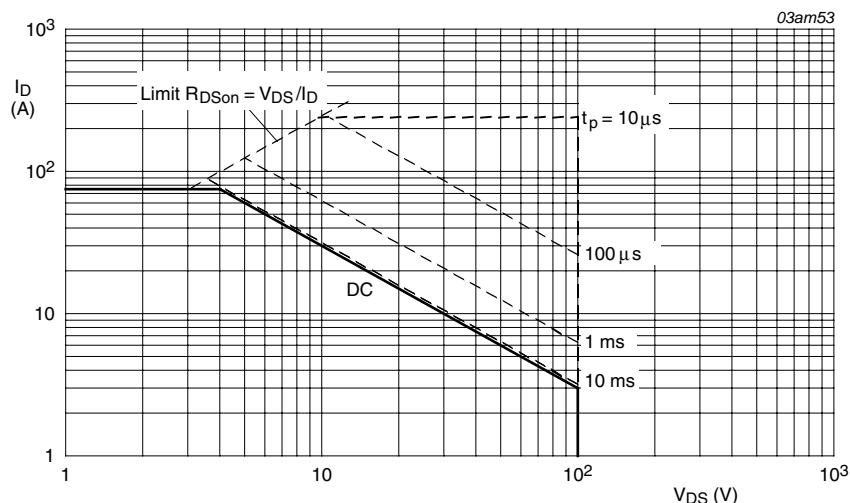
$$I_{der} = \frac{I_D}{I_{D(25^\circ C)}} \times 100\%$$

**Fig 1. Normalized continuous drain current as a function of mounting base temperature**



$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ C)}} \times 100\%$$

**Fig 2. Normalized total power dissipation as a function of mounting base temperature**



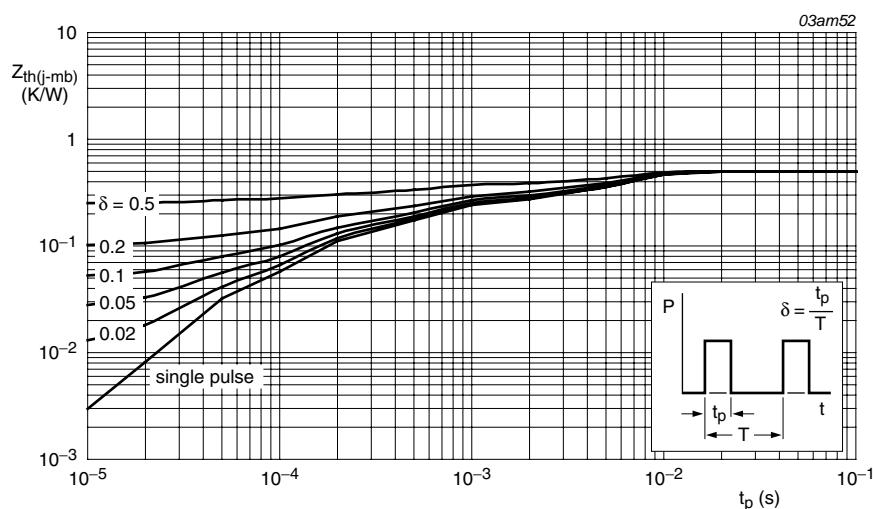
T<sub>mb</sub> = 25°C; I<sub>DM</sub> is single pulse; V<sub>GS</sub> = 10V

**Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage**

## 5. Thermal characteristics

**Table 5. Thermal characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j\text{-}mb)}$	thermal resistance from junction to mounting base	see <a href="#">Figure 4</a>	-	-	0.5	K/W
$R_{th(j\text{-}a)}$	thermal resistance from junction to ambient	mounted on a printed-circuit board; minimum footprint; vertical in still air	-	50	-	K/W

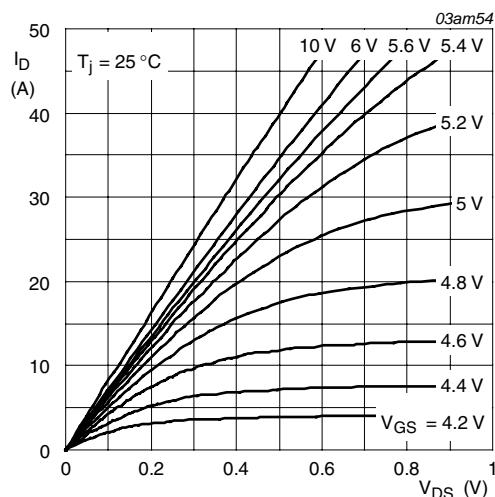


**Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration**

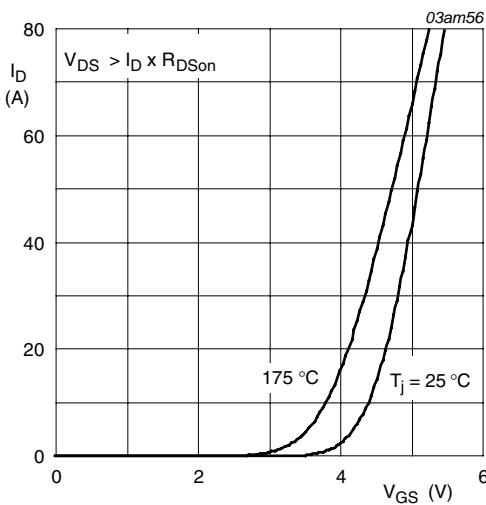
## 6. Characteristics

**Table 6. Characteristics**

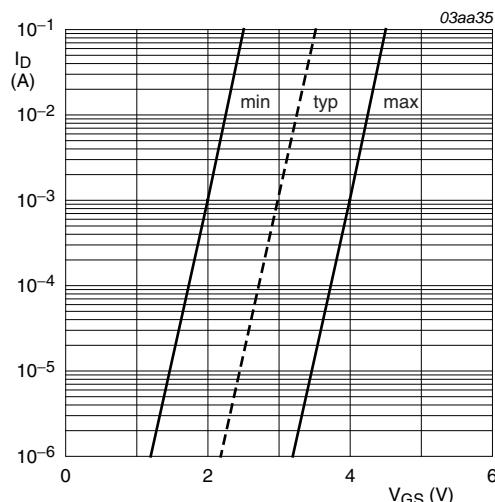
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55^\circ C$	89	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25^\circ C$	100	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 mA; V_{DS} = V_{GS}; T_j = 175^\circ C;$ see <a href="#">Figure 8</a>	1	-	-	V
		$I_D = 1 mA; V_{DS} = V_{GS}; T_j = -55^\circ C;$ see <a href="#">Figure 8</a>	-	-	4.4	V
		$I_D = 1 mA; V_{DS} = V_{GS}; T_j = 25^\circ C;$ see <a href="#">Figure 8</a>	2	3	4	V
$I_{DSS}$	drain leakage current	$V_{DS} = 100 V; V_{GS} = 0 V; T_j = 25^\circ C$	-	0.05	10	$\mu A$
		$V_{DS} = 100 V; V_{GS} = 0 V; T_j = 175^\circ C$	-	-	500	$\mu A$
$I_{GSS}$	gate leakage current	$V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25^\circ C$	-	2	100	nA
		$V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25^\circ C$	-	2	100	nA
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 10 V; I_D = 25 A; T_j = 175^\circ C;$ see <a href="#">Figure 9</a> and <a href="#">10</a>	-	32.4	40.5	$m\Omega$
		$V_{GS} = 10 V; I_D = 25 A; T_j = 25^\circ C;$ see <a href="#">Figure 9</a> and <a href="#">10</a>	-	12	15	$m\Omega$
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$I_D = 75 A; V_{DS} = 80 V; V_{GS} = 10 V;$	-	90	-	nC
$Q_{GS}$	gate-source charge	$T_j = 25^\circ C;$ see <a href="#">Figure 11</a>	-	20	-	nC
$Q_{GD}$	gate-drain charge		-	35	-	nC
$C_{iss}$	input capacitance	$V_{DS} = 25 V; V_{GS} = 0 V; f = 1 MHz;$	-	4900	-	pF
$C_{oss}$	output capacitance	$T_j = 25^\circ C;$ see <a href="#">Figure 12</a>	-	390	-	pF
$C_{rss}$	reverse transfer capacitance		-	220	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 50 V; R_L = 1.8 \Omega; V_{GS} = 10 V;$	-	25	-	ns
$t_r$	rise time	$R_{G(ext)} = 5.6 \Omega; T_j = 25^\circ C$	-	65	-	ns
$t_{d(off)}$	turn-off delay time		-	95	-	ns
$t_f$	fall time		-	50	-	ns
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = 25 A; V_{GS} = 0 V; T_j = 25^\circ C;$ see <a href="#">Figure 13</a>	-	0.8	1.1	V
$t_{rr}$	reverse recovery time	$I_S = 20 A; dI_S/dt = -100 A/\mu s; V_{GS} = 0 V;$	-	80	-	ns
$Q_r$	recovered charge	$V_{DS} = 25 V; T_j = 25^\circ C$	-	115	-	nC


 $T_j = 25^\circ C$ 

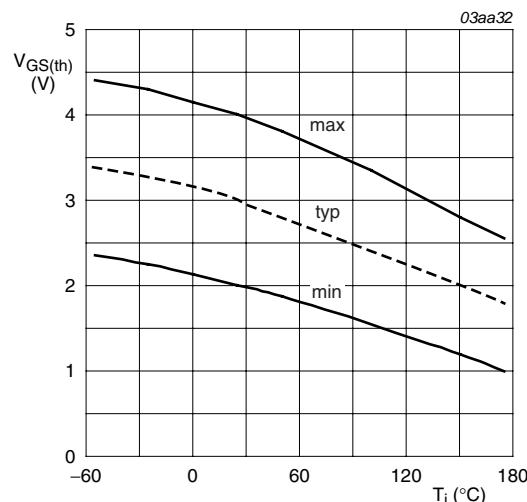
**Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values**


 $T_j = 25^\circ C \text{ and } 175^\circ C; V_{DS} > I_D \times R_{DSon}$ 

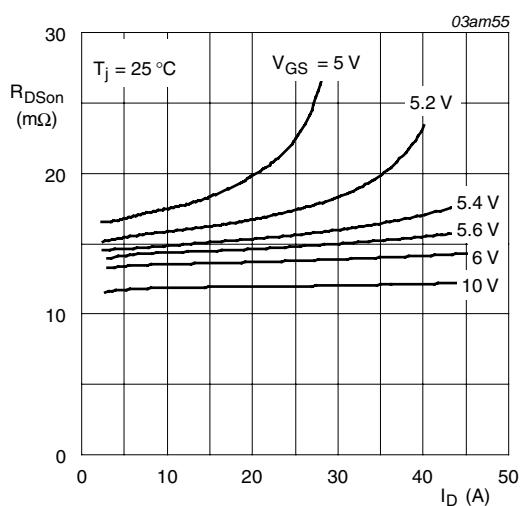
**Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values**


 $T_j = 25^\circ C; V_{DS} = 5V$ 

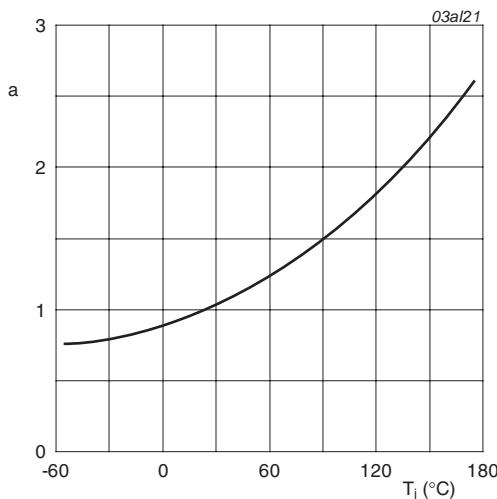
**Fig 7. Sub-threshold drain current as a function of gate-source voltage**


 $I_D = 1mA; V_{DS} = V_{GS}$ 

**Fig 8. Gate-source threshold voltage as a function of junction temperature**

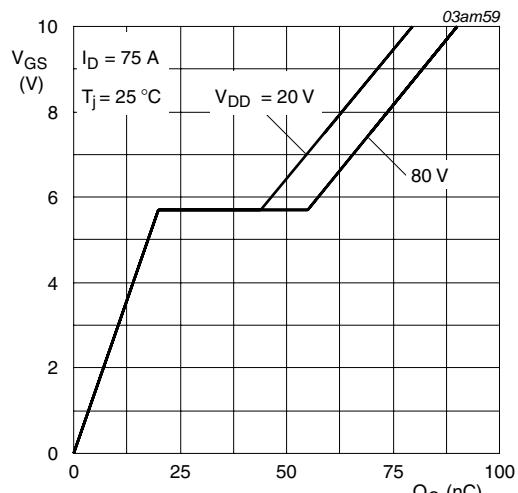

 $T_j = 25^\circ C$ 

**Fig 9.** Drain-source on-state resistance as a function of drain current; typical values

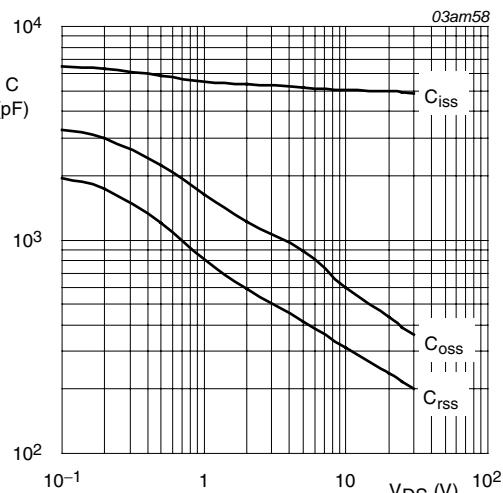


$$a = \frac{R_{DSon}}{R_{DSon}(25^\circ C)}$$

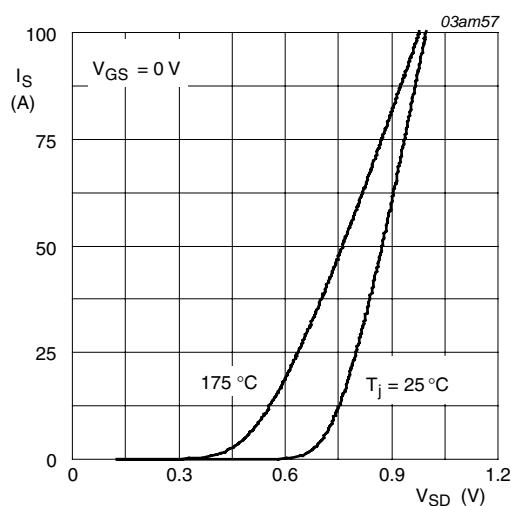
**Fig 10.** Normalized drain-source on-state resistance factor as a function of junction temperature


 $I_D = 75 A; T_j = 25^\circ C$ 

**Fig 11.** Gate-source voltage as a function of gate charge; typical values



**Fig 12.** Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$T_j = 25^\circ\text{C}$  and  $175^\circ\text{C}$ ;  $V_{GS} = 0\text{V}$

Fig 13. Source current as a function of source-drain voltage; typical values

## 7. Package outline

Plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)

SOT404

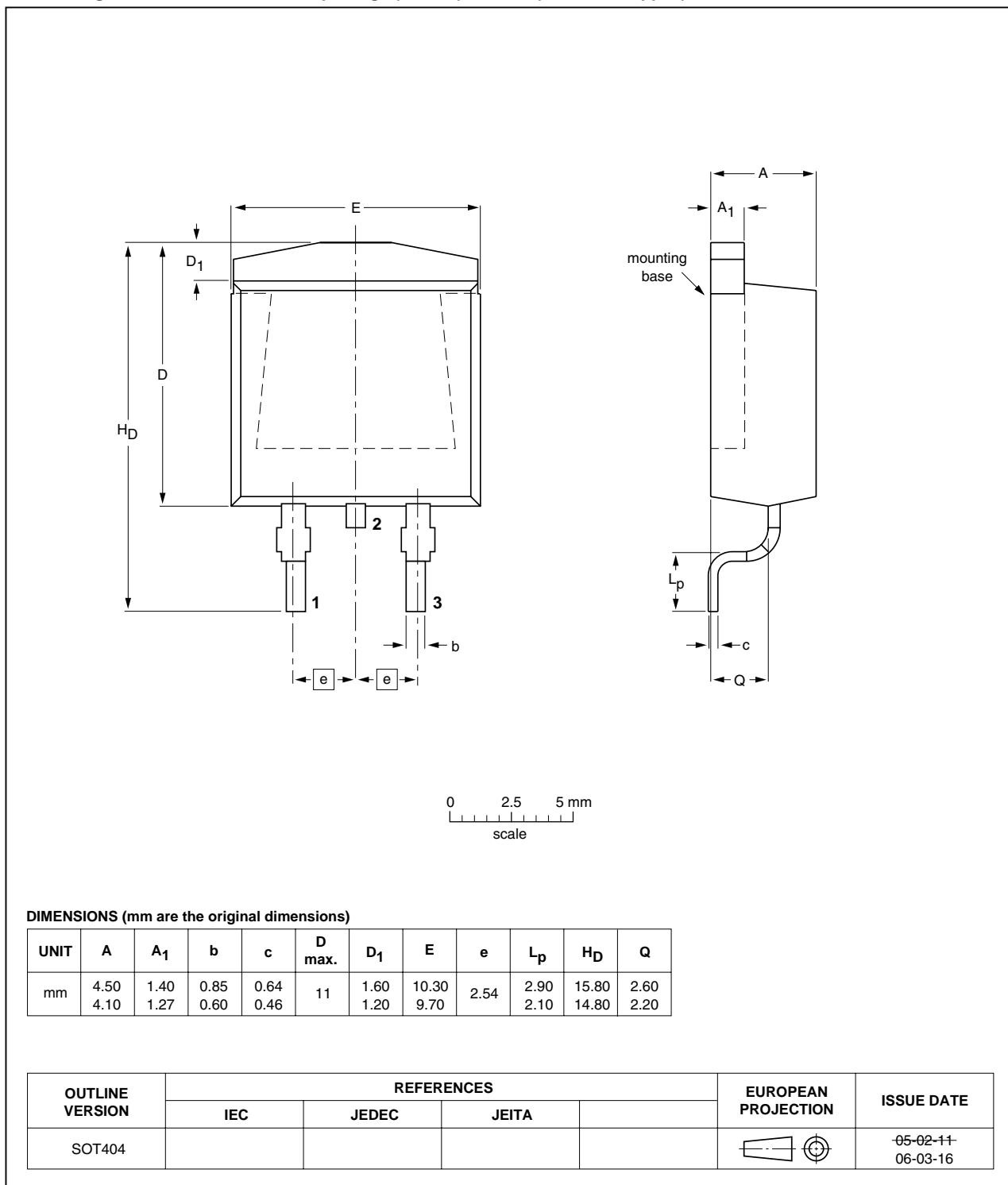


Fig 14. Package outline SOT404 (D2PAK)

## 8. Revision history

**Table 7. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes
PSMN015-100B_6	20091217	Product data sheet	-	PSMN015_100P_100B-05
Modifications:	<ul style="list-style-type: none"><li>The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li><li>Legal texts have been adapted to the new company name where appropriate.</li><li>Type number PSMN015-100B separated from data sheet PSMN015_100P_100B-05.</li></ul>			
PSMN015_100P_100B-05 (9397 750 12543)	20040114	Product data	-	-

## 9. Legal information

### 9.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".

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## 11. Contents

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<b>1</b>	<b>Product profile</b> .....	<b>1</b>
1.1	General description .....	1
1.2	Features and benefits.....	1
1.3	Applications .....	1
1.4	Quick reference data .....	1
<b>2</b>	<b>Pinning information</b> .....	<b>2</b>
<b>3</b>	<b>Ordering information</b> .....	<b>2</b>
<b>4</b>	<b>Limiting values</b> .....	<b>2</b>
<b>5</b>	<b>Thermal characteristics</b> .....	<b>4</b>
<b>6</b>	<b>Characteristics</b> .....	<b>5</b>
<b>7</b>	<b>Package outline</b> .....	<b>9</b>
<b>8</b>	<b>Revision history</b> .....	<b>10</b>
<b>9</b>	<b>Legal information</b> .....	<b>11</b>
9.1	Data sheet status .....	11
9.2	Definitions.....	11
9.3	Disclaimers.....	11
9.4	Trademarks.....	11
<b>10</b>	<b>Contact information</b> .....	<b>11</b>



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