

# DATA SHEET

## **BF510 to 513**

N-channel silicon field-effect  
transistors

Product specification

December 1997



N-channel silicon field-effect transistors

BF510 to 513

DESCRIPTION

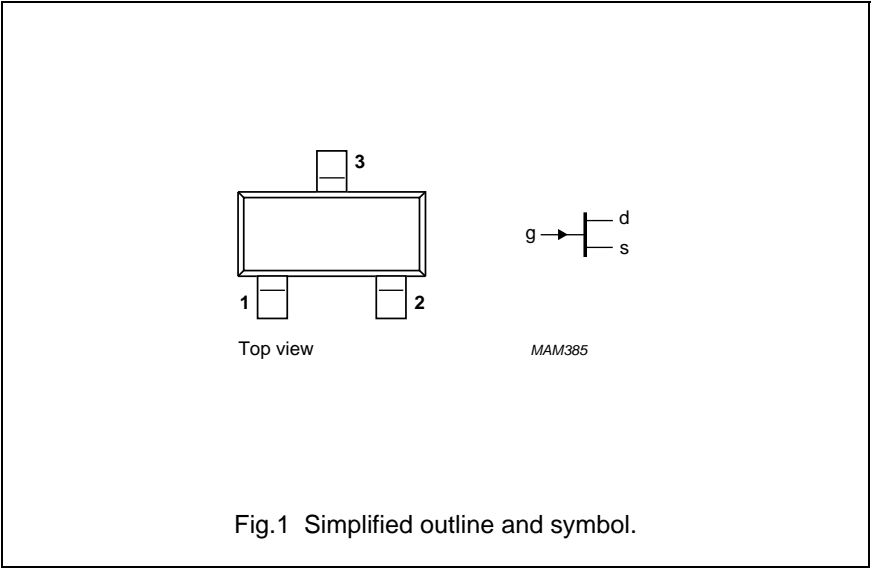
Asymmetrical N-channel planar epitaxial junction field-effect transistors in the miniature plastic envelope intended for applications up to the v.h.f. range in hybrid thick and thin-film circuits. Special features are the low feedback capacitance and the low noise figure. These features make the product very suitable for applications such as the r.f. stages in f.m. portables (BF510), car radios (BF511) and mains radios (BF512) or the mixer stage (BF513).

PINNING - SOT23

- 1 = gate
- 2 = drain
- 3 = source

MARKING CODE

- BF510 = S6p
- BF511 = S7p
- BF512 = S8p
- BF513 = S9p



QUICK REFERENCE DATA

Drain-source voltage	$V_{DS}$	max.	20				V
Drain current (DC or average)	$I_D$	max.	30				mA
Total power dissipation up to $T_{amb} = 40\text{ }^{\circ}\text{C}$	$P_{tot}$	max.	250				mW
			<b>BF510</b>	<b>511</b>	<b>512</b>	<b>513</b>	
Drain current	$I_{DSS}$	$>$	0.7	2.5	6	10	mA
$V_{DS} = 10\text{ V}; V_{GS} = 0$	$I_{DSS}$	$<$	3.0	7.0	12	18	mA
Transfer admittance (common source) $V_{DS} = 10\text{ V}; V_{GS} = 0; f = 1\text{ kHz}$	$ y_{fs} $	$>$	2.5	4	6	7	mS
Feedback capacitance $V_{DS} = 10\text{ V}; V_{GS} = 0$	$C_{rs}$	typ.	0.3	0.3	—	—	pF
$V_{DS} = 10\text{ V}; I_D = 5\text{ mA}$	$C_{rs}$	typ.	—	—	0.3	0.3	pF
Noise figure at optimum source admittance $G_S = 1\text{ mS}; -B_S = 3\text{ mS}; f = 100\text{ MHz}$	F	typ.	1.5	1.5	—	—	dB
$V_{DS} = 10\text{ V}; I_D = 5\text{ mA}$	F	typ.	—	—	1.5	1.5	dB

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**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Drain-source voltage	$V_{DS}$	max.	20 V
Drain-gate voltage (open source)	$V_{DGO}$	max.	20 V
Drain current (DC or average)	$I_D$	max.	30 mA
Gate current	$\pm I_G$	max.	10 mA
Total power dissipation up to $T_{amb} = 40\text{ }^{\circ}\text{C}$ (note 1)	$P_{tot}$	max.	250 mW
Storage temperature range	$T_{stg}$	–65 to + 150	$^{\circ}\text{C}$
Junction temperature	$T_j$	max.	150 $^{\circ}\text{C}$

**THERMAL RESISTANCE**

From junction to ambient (note 1)	$R_{th\ j-a}$	=	430 K/W
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**Note**

1. Mounted on a ceramic substrate of 8 mm × 10 mm × 0.7 mm.

**STATIC CHARACTERISTICS** $T_{amb} = 25\text{ }^{\circ}\text{C}$ 

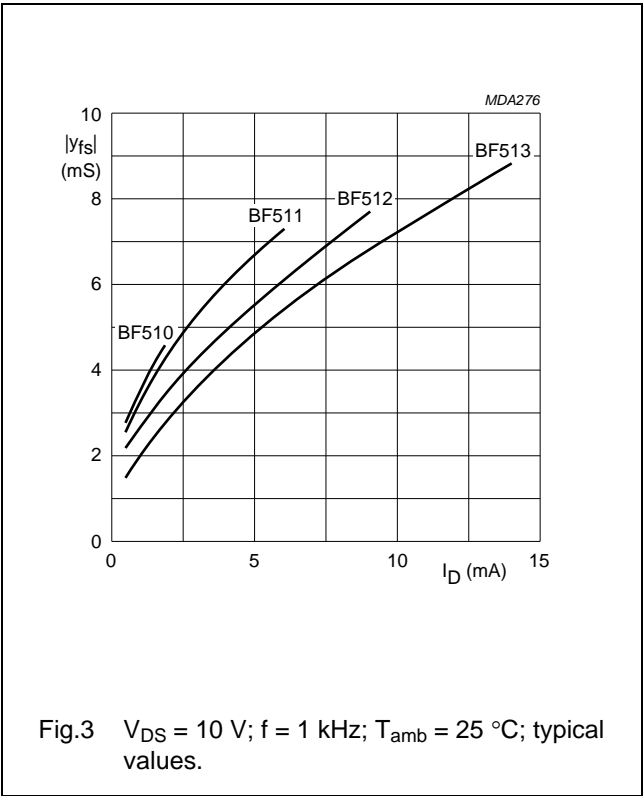
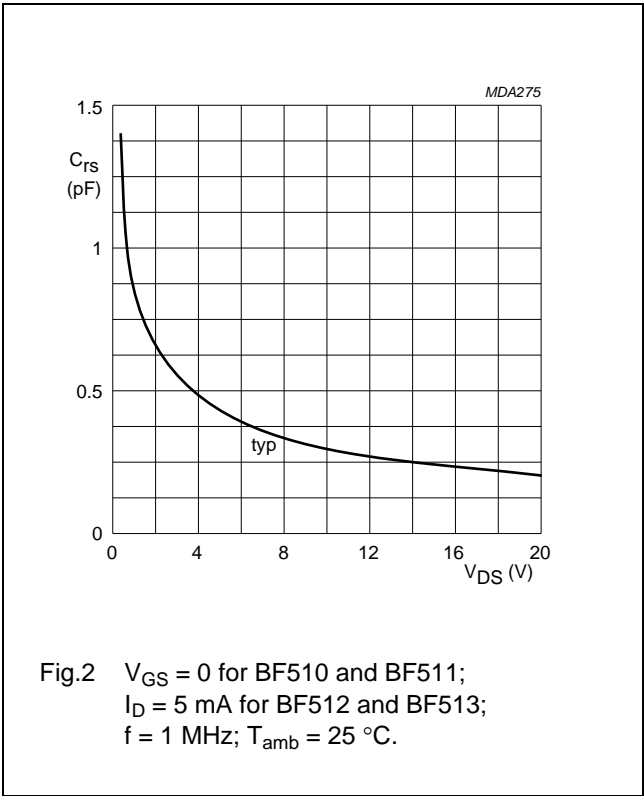
			BF510	511	512	513
Gate cut-off current						
– $V_{GS} = 0.2\text{ V}$ ; $V_{DS} = 0$	$-I_{GSS}$	<	10	10	10	10 nA
Gate-drain breakdown voltage						
$I_S = 0$ ; $-I_D = 10\text{ }\mu\text{A}$	$-V_{(BR)GDO}$	>	20	20	20	20 V
Drain current						
$V_{DS} = 10\text{ V}$ ; $V_{GS} = 0$	$I_{DSS}$	>	0.7	2.5	6	10 mA
		<	3.0	7.0	12	18 mA
Gate-source cut-off voltage						
$I_D = 10\text{ }\mu\text{A}$ ; $V_{DS} = 10\text{ V}$	$-V_{(P)GS}$	typ.	0.8	1.5	2.2	3 V

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DYNAMIC CHARACTERISTICS

<b>Measuring conditions (common source):</b>			$V_{DS} = 10\text{ V}; V_{GS} = 0; T_{amb} = 25\text{ }^{\circ}\text{C}$ for BF510 and BF511			
			$V_{DS} = 10\text{ V}; I_D = 5\text{ mA}; T_{amb} = 25\text{ }^{\circ}\text{C}$ for BF512 and BF513			
<b>y-parameters (common source)</b>			BF510	511	512	513
Input capacitance at $f = 1\text{ MHz}$	$C_{is}$	<	5	5	5	5 pF
Input conductance at $f = 100\text{ MHz}$	$g_{is}$	typ.	100	90	60	50 $\mu\text{S}$
Feedback capacitance at $f = 1\text{ MHz}$	$C_{rs}$	typ.	0.4	0.4	0.4	0.4 pF
		<	0.5	0.5	0.5	0.5 pF
Transfer admittance at $f = 1\text{ kHz}$	$ y_{fs} $	>	2.5	4.0	4.0	3.5 mS
$V_{GS} = 0$ instead of $I_D = 5\text{ mA}$	$ y_{fs} $	>	—	—	6.0	7.0 mS
Transfer admittance at $f = 100\text{ MHz}$	$ y_{fs} $	typ.	3.5	5.5	5.0	5.0 mS
Output capacitance at $f = 1\text{ MHz}$	$C_{os}$	<	3	3	3	3 pF
Output conductance at $f = 1\text{ MHz}$	$g_{os}$	<	60	80	100	120 $\mu\text{S}$
Output conductance at $f = 100\text{ MHz}$	$g_{os}$	typ.	35	55	70	90 $\mu\text{S}$
<b>Noise figure</b> at optimum source admittance						
$G_S = 1\text{ mS}; -B_S = 3\text{ mS};$						
$f = 100\text{ MHz}$	F	typ.	1.5	1.5	1.5	1.5 dB



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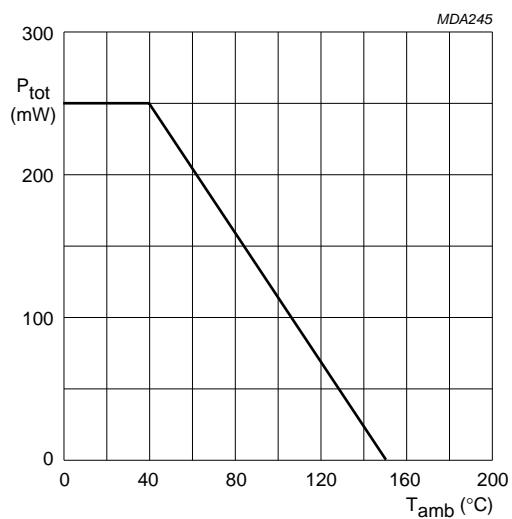


Fig.4 Power derating curve.

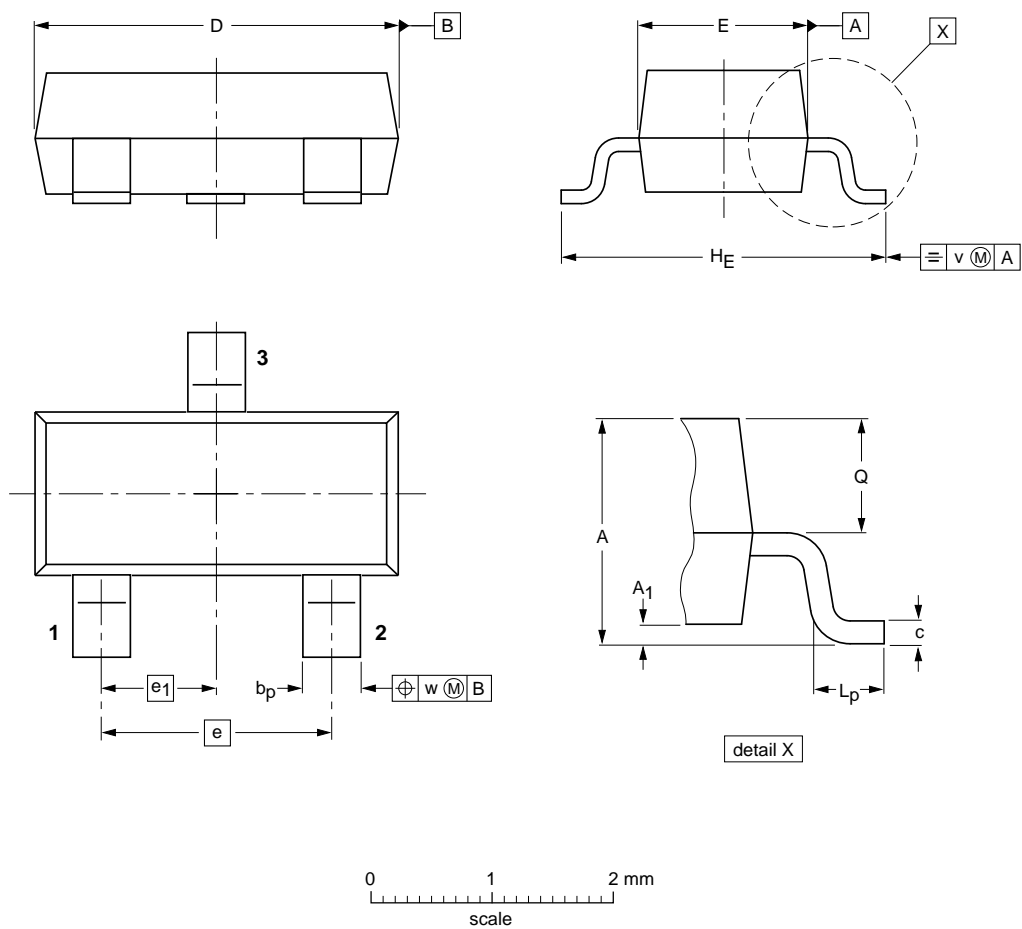
N-channel silicon field-effect transistors

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PACKAGE OUTLINE

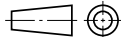
Plastic surface-mounted package; 3 leads

SOT23



DIMENSIONS (mm are the original dimensions)

UNIT	A	A <sub>1</sub> max.	b <sub>p</sub>	c	D	E	e	e <sub>1</sub>	H <sub>E</sub>	L <sub>p</sub>	Q	v	w
mm	1.1 0.9	0.1	0.48 0.38	0.15 0.09	3.0 2.8	1.4 1.2	1.9	0.95	2.5 2.1	0.45 0.15	0.55 0.45	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT23		TO-236AB				<del>04-11-04</del> 06-03-16

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## DATA SHEET STATUS

DOCUMENT STATUS <sup>(1)</sup>	PRODUCT STATUS <sup>(2)</sup>	DEFINITION
Objective data sheet	Development	This document contains data from the objective specification for product development.
Preliminary data sheet	Qualification	This document contains data from the preliminary specification.
Product data sheet	Production	This document contains the product specification.

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**Телефон:** 8 (812) 309 58 32 (многоканальный)

**Факс:** 8 (812) 320-02-42

**Электронная почта:** [org@eplast1.ru](mailto:org@eplast1.ru)

**Адрес:** 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.