

DESCRIPTION

The 3825 group is the 8-bit microcomputer based on the 740 family core technology.

The 3825 group has the LCD drive control circuit, an 8-channel A-D converter, and a Serial I/O as additional functions.

The various microcomputers in the 3825 group include variations of internal memory size and packaging. For details, refer to the section on part numbering.

For details on availability of microcomputers in the 3825 group, refer the section on group expansion.

FEATURES

- Basic machine-language instructions 71
- The minimum instruction execution time 0.5 μ s
(at 8MHz oscillation frequency)
- Memory size
 - ROM 4 K to 60 K bytes
 - RAM 192 to 2048 bytes
- Programmable input/output ports 43
- Software pull-up/pull-down resistors (Ports P0–P8)
- Interrupts 17 sources, 16 vectors
(includes key input interrupt)
- Timers 8-bit $\times$ 3, 16-bit $\times$ 2
- Serial I/O 8-bit $\times$ 1 (UART or Clock-synchronized)
- A-D converter 8-bit $\times$ 8 channels

• LCD drive control circuit

- Bias 1/2, 1/3
- Duty 1/2, 1/3, 1/4
- Common output 4
- Segment output 40

• 2 Clock generating circuits

- Clock (XIN-XOUT) Internal feedback resistor
- Sub-clock (XCIN-XCOUT) Without internal feedback resistor
(connect to external ceramic resonator or quartz-crystal oscillator)

• Power source voltage

- In high-speed mode 4.0 to 5.5 V
- In middle-speed mode 2.5 to 5.5 V
(Low power source version: 2.2 V to 5.5 V)
- (Extended operating temperature version: 3.0 V to 5.5 V)
- In low-speed mode 2.5 to 5.5 V
(Low power source version: 2.2 V to 5.5 V)
- (Extended operating temperature version: 3.0 V to 5.5 V)

• Power dissipation

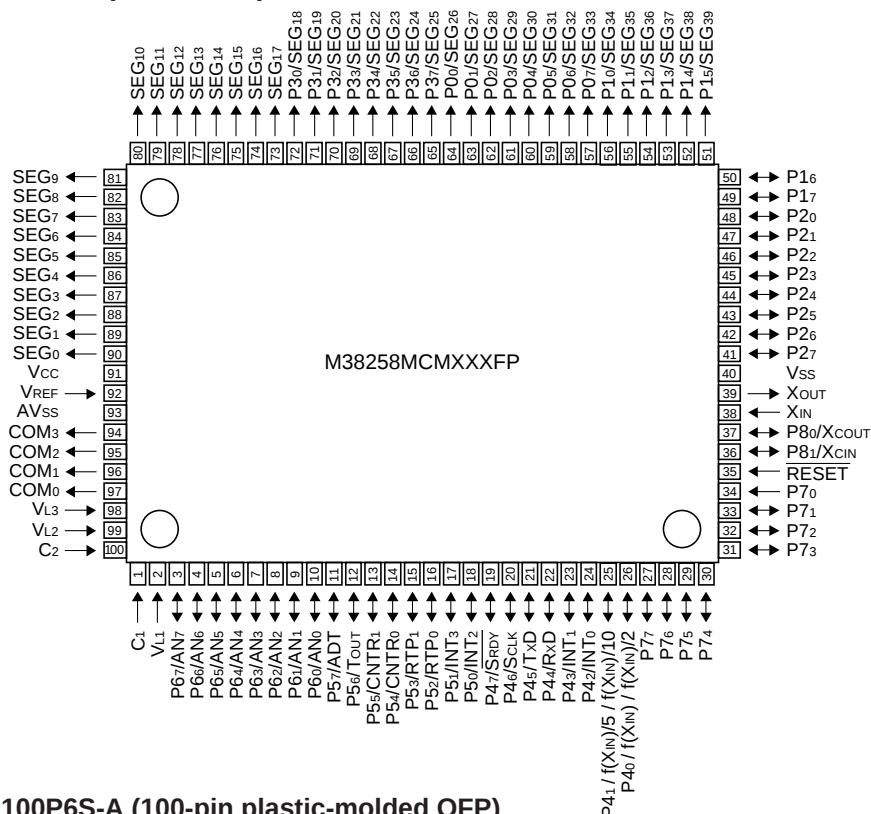
- In high-speed mode 32 mW
(at 8 MHz oscillation frequency, at 5 V power source voltage)
- In low-speed mode 45 μ W
(at 32 kHz oscillation frequency, at 3 V power source voltage)

- Operating temperature range – 20 to 85°C
(Extended operating temperature version: –40 to 85°C)

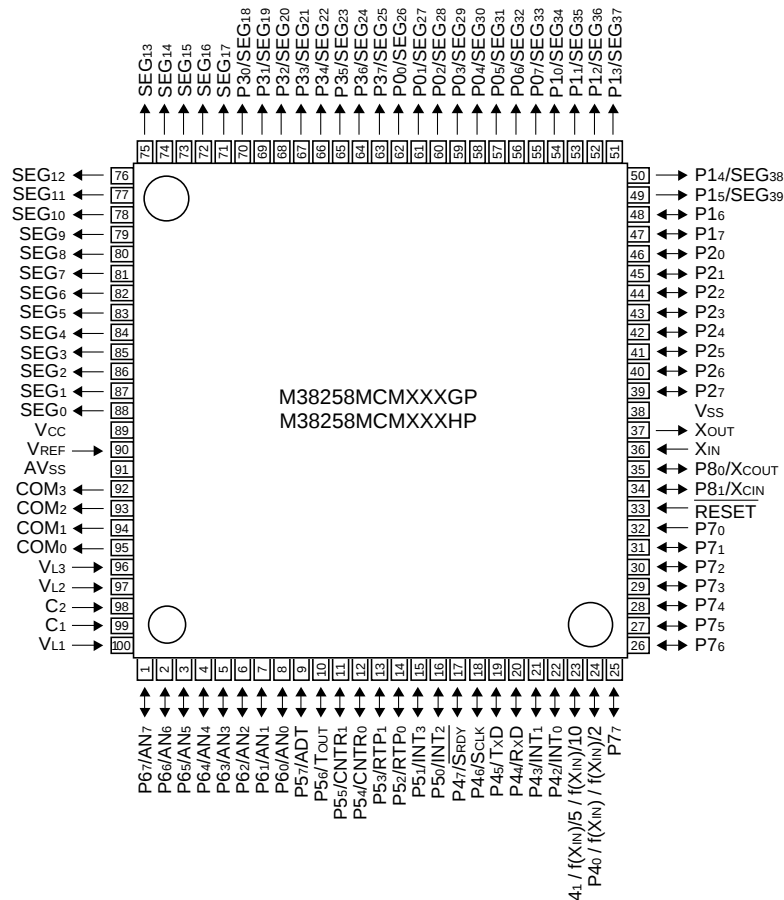
APPLICATIONS

Camera, household appliances, consumer electronics, etc.

PIN CONFIGURATION (TOP VIEW)



PIN CONFIGURATION (TOP VIEW)



Package type : GP 100P6Q-A (100-pin plastic-molded LQFP)

Package type : HP 100PFB-A (100-pin plastic-molded TQFP)

Fig. 2 Pin configuration of M38258MCMXXXGP, M38258MCMXXXHP

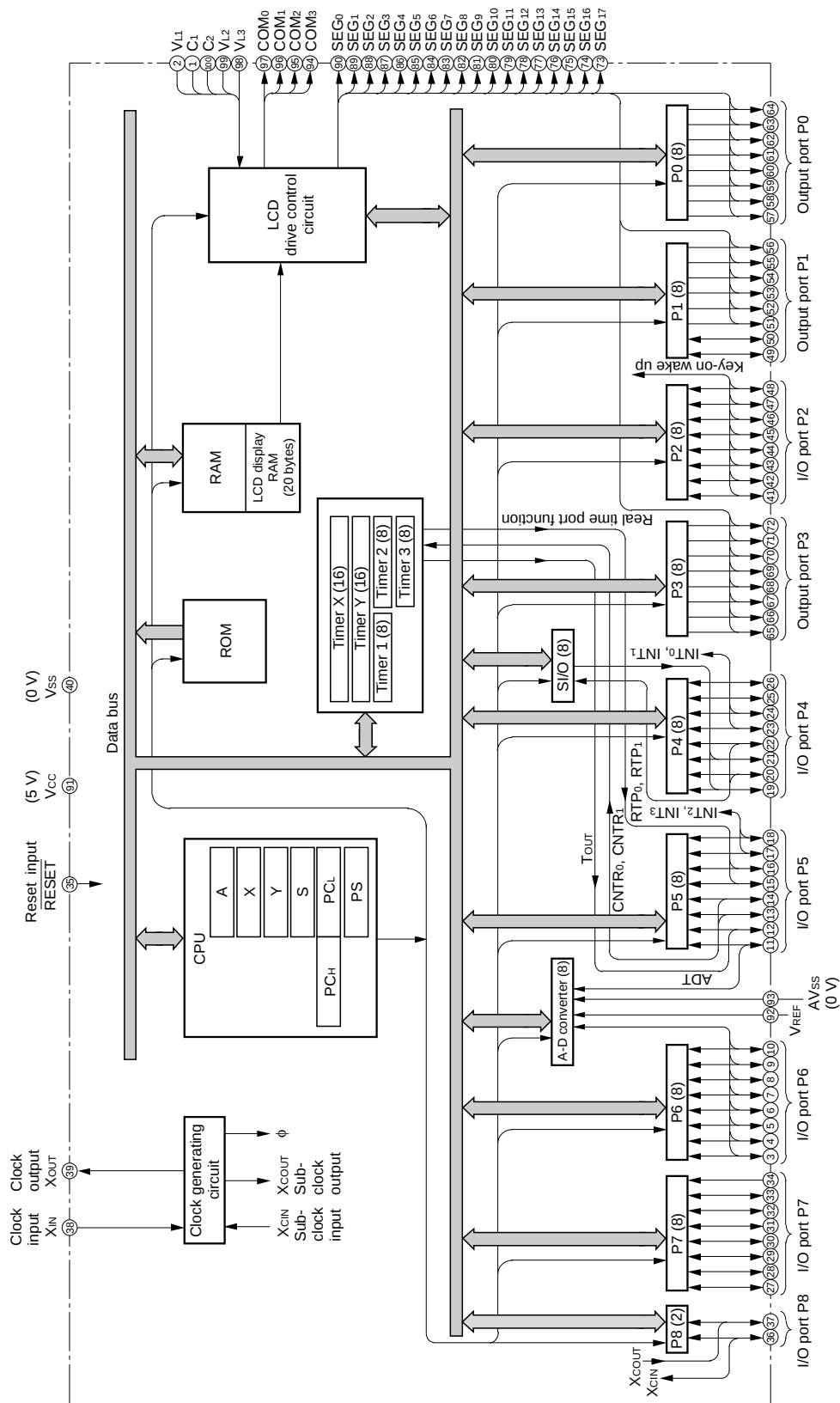


Fig. 3 Functional block diagram.

PIN DESCRIPTION

Table 1. Pin description (1)

Pin	Name	Function	
			Function except a port function
VCC, VSS	Power source	• Apply voltage of 2.2 V to 5.5 V to VCC, and 0 V to VSS.	
VREF	Analog reference voltage	• Reference voltage input pin for A-D converter.	
AVSS	Analog power source	• GND input pin for A-D converter. • Connect to VSS.	
$\overline{\text{RESET}}$	Reset input	• Reset input pin for active “L”	
XIN	Clock input	• Input and output pins for the main clock generating circuit. • Feedback resistor is built in between XIN pin and XOUT pin. • Connect a ceramic resonator or a quartz-crystal oscillator between the XIN and XOUT pins to set the oscillation frequency. • If an external clock is used, connect the clock source to the XIN pin and leave the XOUT pin open. • This clock is used as the oscillating source of system clock.	
XOUT	Clock output		
VL1 – VL3	LCD power source	• Input $0 \leq \text{VL1} \leq \text{VL2} \leq \text{VL3} \leq \text{VCC}$ voltage • Input 0 – VL3 voltage to LCD	
C1, C2	Charge-pump capacitor pin	• External capacitor pins for a voltage multiplier (3 times) of LCD control.	
COM0 – COM3	Common output	• LCD common output pins • COM2 and COM3 are not used at 1/2 duty ratio. • COM3 is not used at 1/3 duty ratio.	
SEG0 – SEG17	Segment output	• LCD segment output pins	
P00/SEG26 – P07/SEG33	Output port P0	• 8-bit output port • CMOS 3-state output structure • Pull-down control is enabled. • Port output control is enabled.	• LCD segment pins
P10/SEG34 – P15/SEG39	Output port P1	• 6-bit output port • CMOS 3-state output structure • Pull-down control is enabled. • Port output control is enabled.	
P16, P17	I/O port P1	• 2-bit I/O port • CMOS compatible input level • CMOS 3-state output structure • I/O direction register allows each pin to be individually programmed as either input or output. • Pull-up control is enabled.	
P20 – P27	I/O port P2	• 8-bit Input port • CMOS compatible input level • CMOS 3-state output structure • I/O direction register allows each pin to be individually programmed as either input or output. • Pull-up control is enabled.	• Key input (key-on wake up) interrupt input pins
P30/SEG18 – P37/SEG25	Output port P3	• 8-bit output port • CMOS 3-state output structure • Pull-down control is enabled. • Port output control is enabled.	• LCD segment pins

Table 2. Pin description (2)

Pin	Name	Function	Function except a port function
P40/f(X _{IN})/ f(X _{IN})/2, P41/f(X _{IN})/5/ f(X _{IN})/10	I/O port P4	• 8-bit I/O port • CMOS compatible input level • CMOS 3-state output structure • I/O direction register allows each pin to be individually programmed as either input or output. • Pull-up control is enabled.	• Clock output pins
P42/INT ₀ , P43/INT ₁			• Interrupt input pins
P44/RxD, P45/TxD, P46/SCLK, P47/SRDY			• Serial I/O function pins
P50/INT ₂ , P51/INT ₃	I/O port P5	• 8-bit I/O port • CMOS compatible input level • CMOS 3-state output structure • I/O direction register allows each pin to be individually programmed as either input or output. • Pull-up control is enabled.	• Interrupt input pins
P52/RTP ₀ , P53/RTP ₁			• Real time port function pins
P54/CNTR ₀ , P55/CNTR ₁			• Timers X, Y functions pins
P56/TOUT			• Timer 2 output pin
P57/ADT			• A-D trigger input pin
P60/AN ₀ – P67/AN ₇	I/O port P6	• 8-bit I/O port • CMOS compatible input level • CMOS 3-state output structure • I/O direction register allows each pin to be individually programmed as either input or output. • Pull-up control is enabled.	• A-D conversion input pins
P7 ₀	Input port P7	• 1-bit input port • CMOS compatible input level	
P7 ₁ –P7 ₇	I/O port P7	• 7-bit I/O port • CMOS compatible input level • CMOS 3-state output structure • I/O direction register allows each pin to be individually programmed as either input or output. • Pull-up control is enabled.	
P80/XCOUT, P81/XCIN	I/O port P8	• 2-bit I/O port • CMOS compatible input level • CMOS 3-state output structure • I/O direction register allows each pin to be individually programmed as either input or output. • Pull-up control is enabled.	• Sub-clock generating circuit I/O pins (Connect a resonator. External clock cannot be used.)

PART NUMBERING

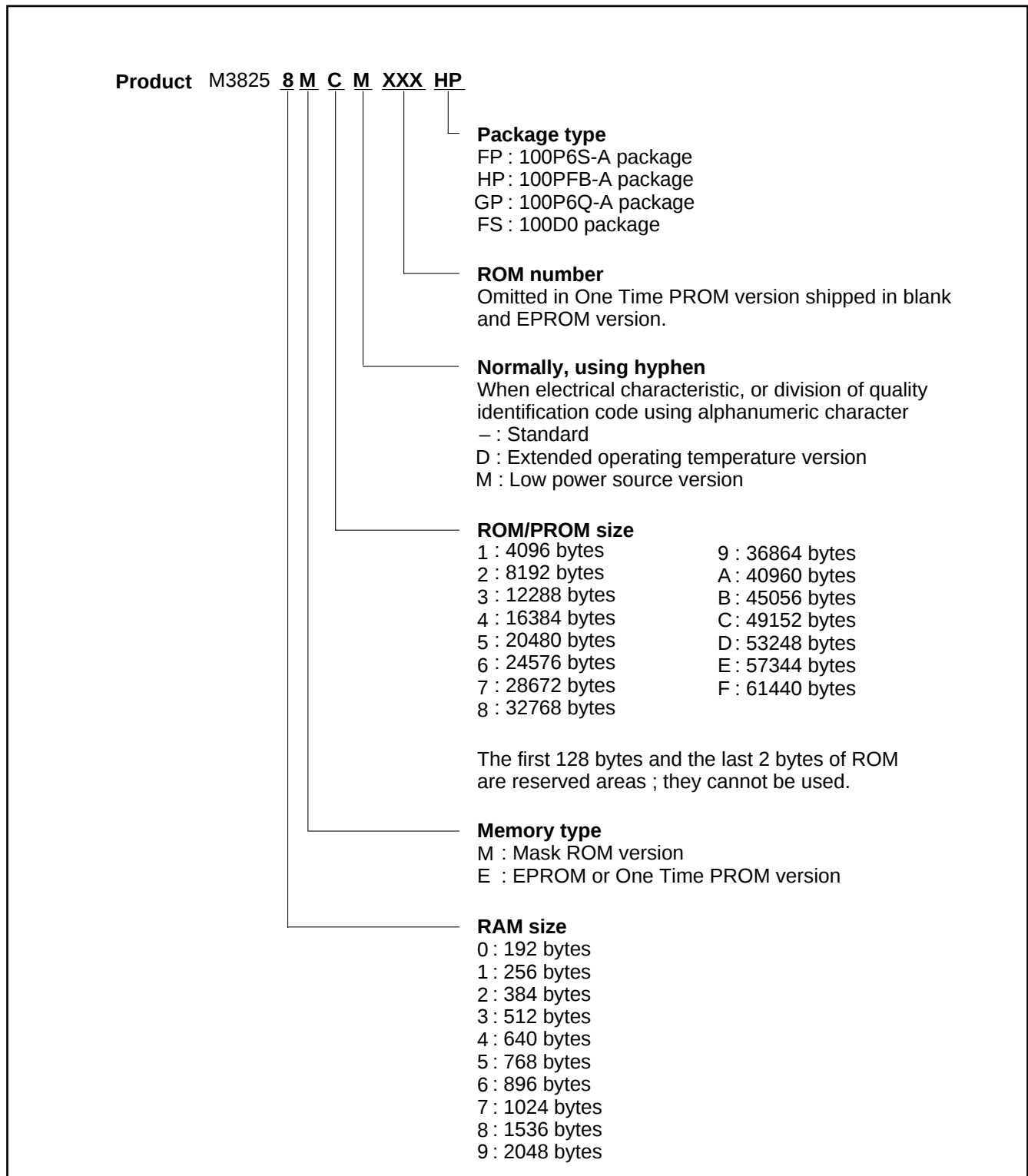


Fig. 4 Part numbering

GROUP EXPANSION

Mitsubishi plans to expand the 3825 group as follows.

Memory Type

Support for mask ROM, One Time PROM, and EPROM versions.

Memory Size

ROM/PROM size 16 K to 60 Kbytes

RAM size 640 to 2048 bytes

Packages

100PFB-A 0.4 mm-pitch plastic molded TQFP

100P6Q-A 0.5 mm-pitch plastic molded LQFP

100P6S-A 0.65 mm-pitch plastic molded QFP

100D0 Ceramic QFN (EPROM version)

Memory Expansion Plan

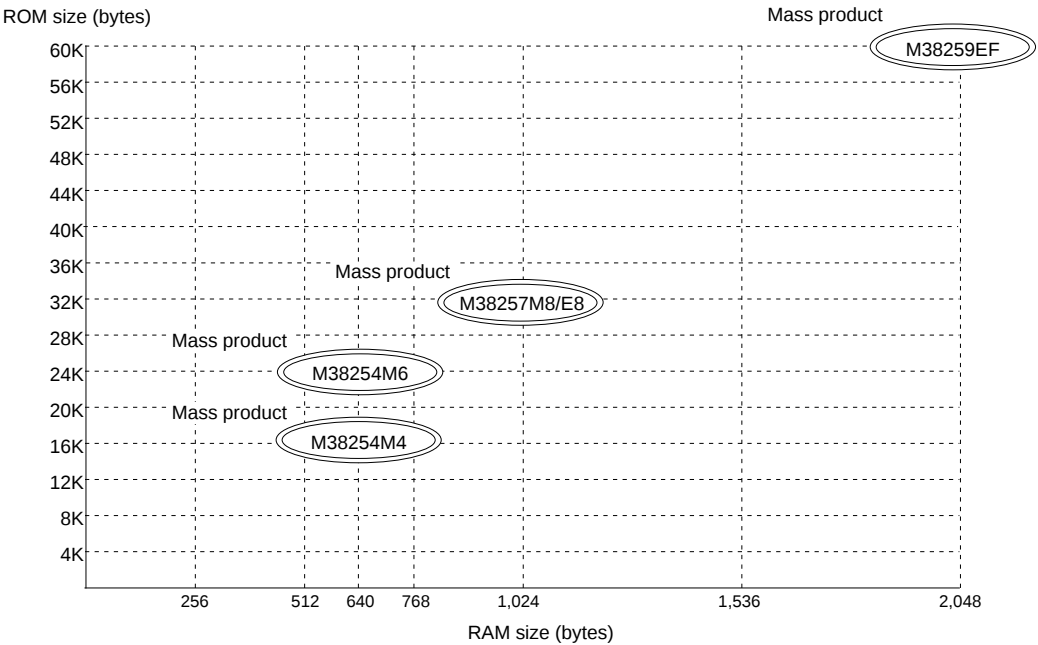


Fig. 5 Memory expansion plan

Currently supported products are listed below.

Table 3. List of supported products

As of June 1999

Product	(P) ROM size (bytes) ROM size for User in ()	RAM size (bytes)	Package	Remarks
M38254M4-XXXFP	16384	640	100P6S-A	Mask ROM version
M38254M4-XXXGP	(16254)		100P6Q-A	Mask ROM version
M38254M6-XXXFP	24576	640	100P6S-A	Mask ROM version
M38254M6-XXXGP	(24446)		100P6Q-A	
M38257M8-XXXFP	32768 (32638)	1024	100P6S-A	Mask ROM version
M38257E8-XXXFP				One Time PROM version
M38257E8FP				One Time PROM version (blank)
M38257M8-XXXGP			100P6Q-A	Mask ROM version
M38257E8-XXXGP				One Time PROM version
M38257E8GP				One Time PROM version (blank)
M38257E8FS			100D0	EPROM version
M38259EF-XXXFP	61440 (61310)	2048	100P6S-A	One Time PROM version
M38259EFP				One Time PROM version (blank)
M38259EF-XXXHP			100PFB-A	One Time PROM version
M38259EFHP				One Time PROM version (blank)
M38259EF-XXXGP			100P6Q-A	One Time PROM version
M38259EFGP				One Time PROM version (blank)
M38259EFS			100D0	EPROM version

GROUP EXPANSION
(EXTENDED OPERATING TEMPERATURE VERSION)

Mitsubishi plans to expand the 3825 group (extended operating temperature version) as follows.

Memory Type

Support for mask ROM and One Time PROM versions.

Memory Size

ROM/PROM 16 K to 60 Kbytes
RAM size 640 to 2048 bytes

Packages

100P6S-A 0.65 mm-pitch plastic molded QFP

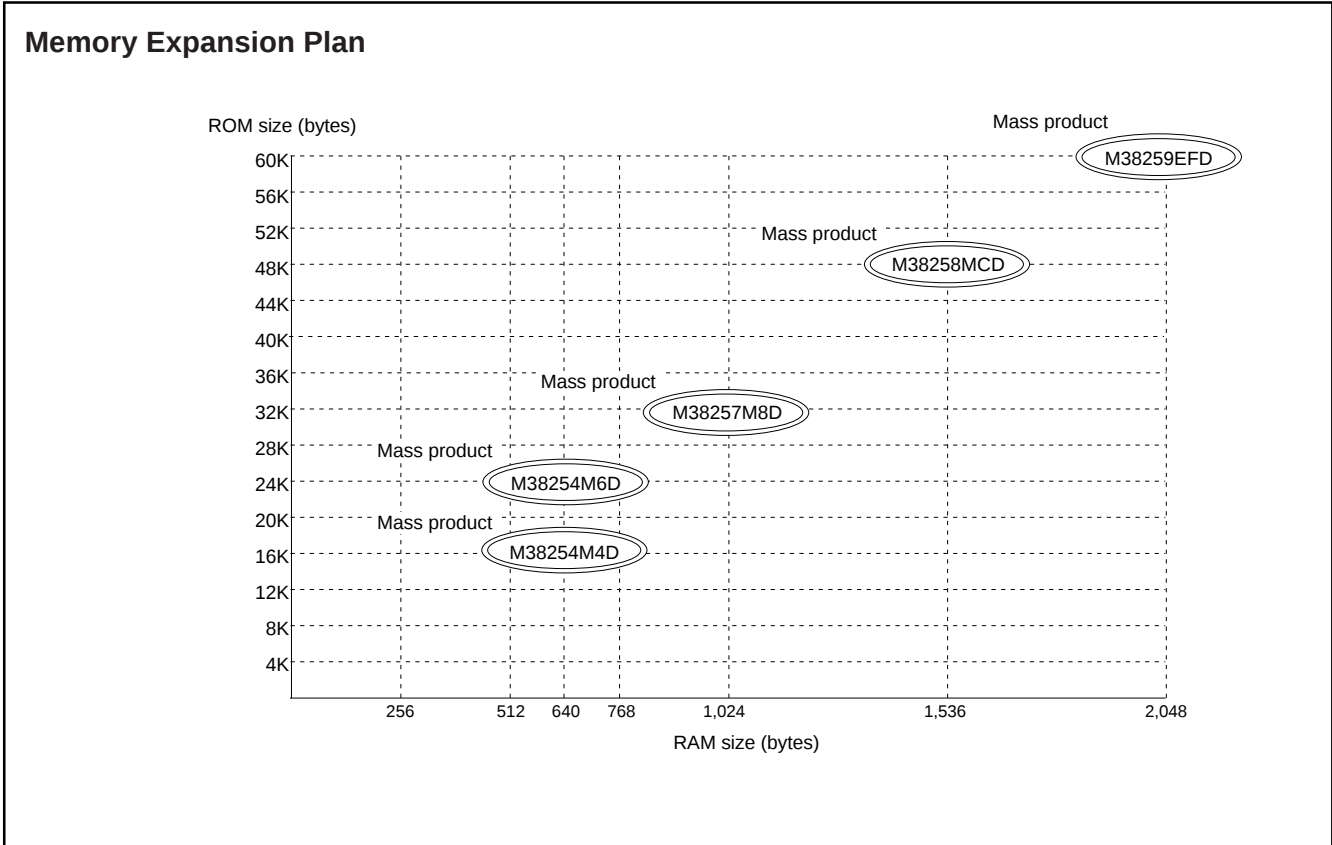


Fig. 6 Memory expansion plan for extended operating temperature version

Currently supported products are listed below.

Table 4. List of supported products for extended operating temperature version As of June 1999

Product	(P) ROM size (bytes) ROM size for User in ()	RAM size (bytes)	Package	Remarks
M38254M4DXXXFP	16384 (16254)	640	100P6S-A	Mask ROM version
M38254M6DXXXFP	24576 (24446)	640		Mask ROM version
M38257M8DXXXFP	32768 (32638)	1024		Mask ROM version
M38258MCDXXXFP	49152 (49022)	1536		Mask ROM version
M38259EFDXXXFP	61440	2048		One Time PROM version
M38259EFD	(61310)			One Time PROM version (blank)

GROUP EXPANSION
(LOW POWER SOURCE VERSION)

Mitsubishi plans to expand the 3825 group (low power source version) as follows.

Memory Type
Support for mask ROM version.

Memory Size
ROM 48 Kbytes
RAM size 1536 bytes

Packages
100PFB-A 0.4 mm-pitch plastic molded TQFP
100P6Q-A 0.5 mm-pitch plastic molded LQFP
100P6S-A 0.65 mm-pitch plastic molded QFP

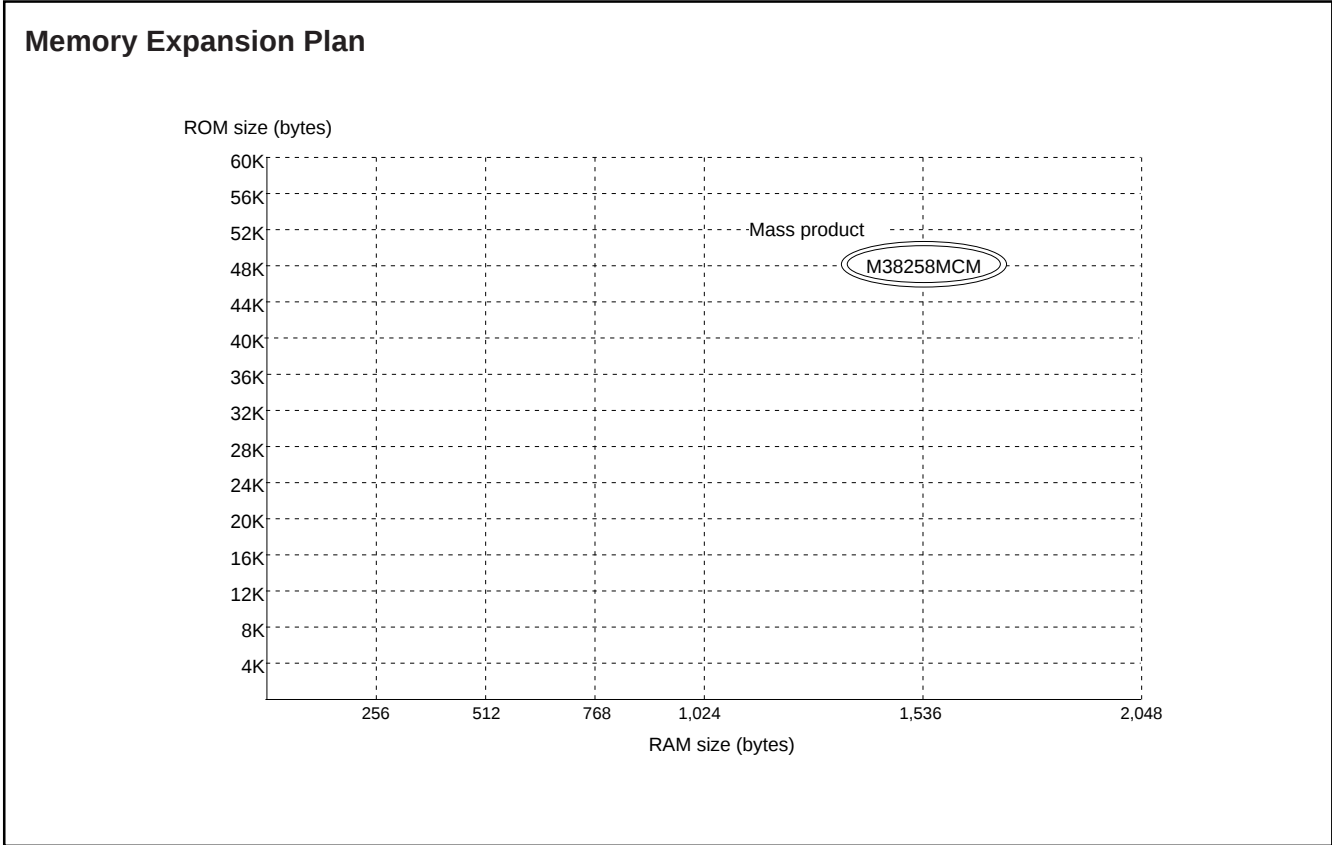


Fig. 7 Memory expansion plan for low power source version

Currently supported products are listed below.

Table 5. List of supported products for low power source version As of June 1999

Product	(P) ROM size (bytes) ROM size for User in ()	RAM size (bytes)	Package	Remarks
M38258MCMXXXFP	49152 (49022)	1536	100P6S-A	Mask ROM version
M38258MCMXXXHP			100PFB-A	
M38258MCMXXXGP			100P6Q-A	

FUNCTIONAL DESCRIPTION
CENTRAL PPROCESSING UNIT (CPU)

The 3825 group uses the standard 740 family instruction set. Refer to the 740 Family Software Manual for details on the instruction set. Machine-resident 740 family instructions are as follows:
The FST and SLW instructions cannot be used.
The STP, WIT, MUL, and DIV instructions can be used.

[CPU Mode Register (CPUM)] 003B16

The CPU mode register is allocated at address 003B16. The CPU mode register contains the stack page selection bit and the internal system clock selection bit.

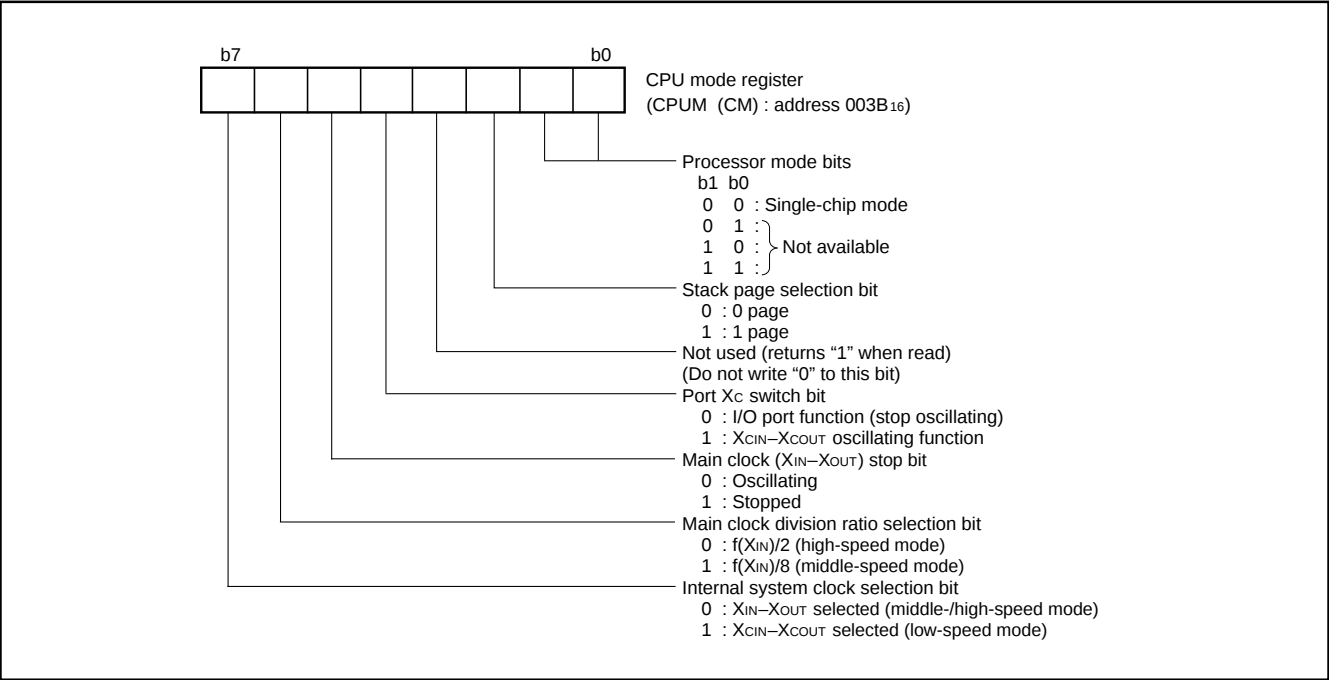


Fig. 8 Structure of CPU mode register

MEMORY

Special Function Register (SFR) Area

The Special Function Register area in the zero page contains control registers such as I/O ports and timers.

RAM

RAM is used for data storage and for stack area of subroutine calls and interrupts.

ROM

The first 128 bytes and the last 2 bytes of ROM are reserved for device testing and the rest is user area for storing programs.

Interrupt Vector Area

The interrupt vector area contains reset and interrupt vectors.

Zero Page

The 256 bytes from addresses 0000₁₆ to 00FF₁₆ are called the zero page area. The internal RAM and the special function registers (SFR) are allocated to this area.

The zero page addressing mode can be used to specify memory and register addresses in the zero page area. Access to this area with only 2 bytes is possible in the zero page addressing mode.

Special Page

The 256 bytes from addresses FF00₁₆ to FFFF₁₆ are called the special page area. The special page addressing mode can be used to specify memory addresses in the special page area. Access to this area with only 2 bytes is possible in the special page addressing mode.

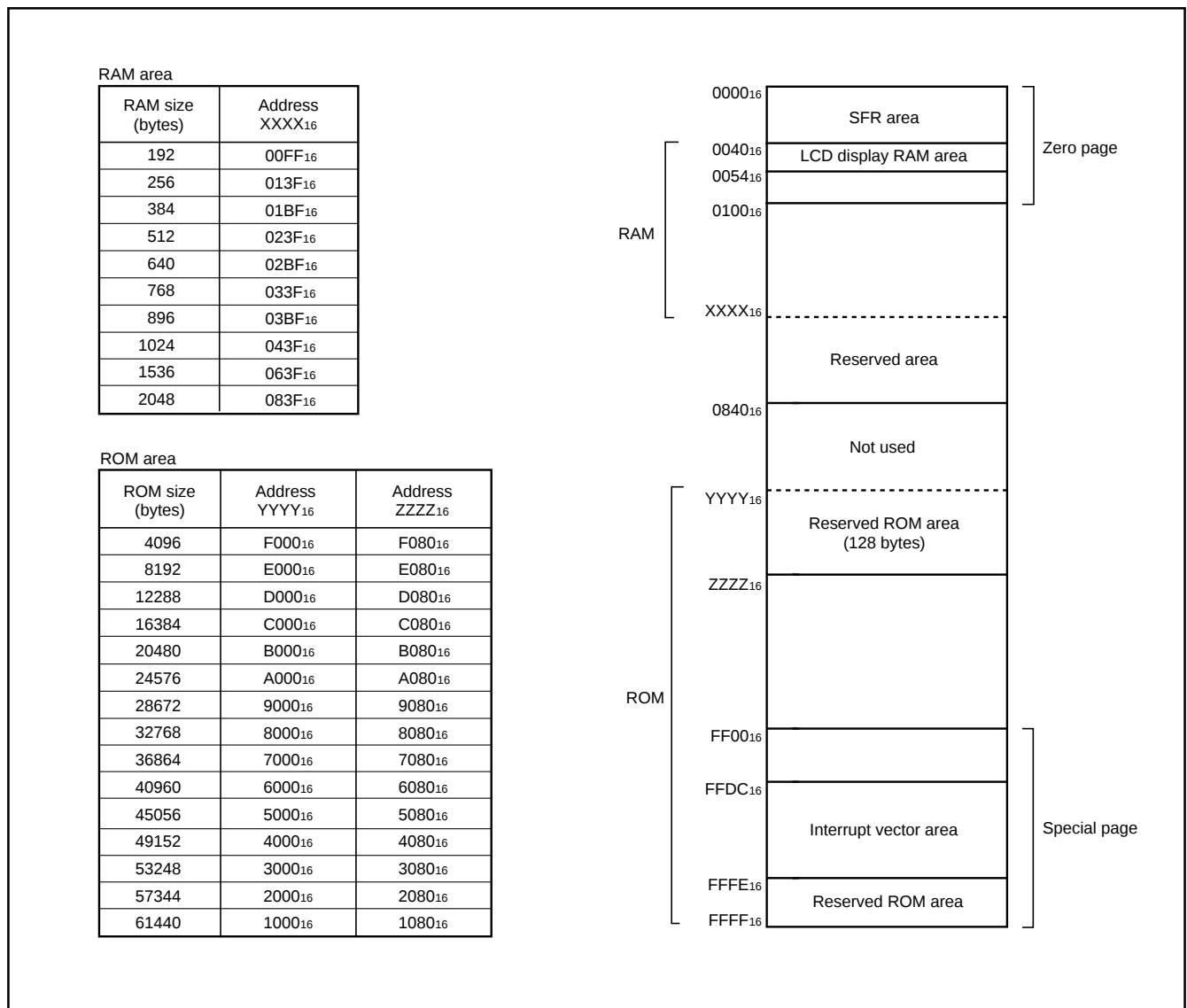


Fig. 9 Memory map diagram

0000 ₁₆	Port P0 (P0)	0020 ₁₆	Timer X (low) (TXL)
0001 ₁₆		0021 ₁₆	Timer X (high) (TXH)
0002 ₁₆	Port P1 (P1)	0022 ₁₆	Timer Y (low) (TYL)
0003 ₁₆	Port P1 output control register (P1C)	0023 ₁₆	Timer Y (high) (TYH)
0004 ₁₆	Port P2 (P2)	0024 ₁₆	Timer 1 (T1)
0005 ₁₆	Port P2 direction register (P2D)	0025 ₁₆	Timer 2 (T2)
0006 ₁₆	Port P3 (P3)	0026 ₁₆	Timer 3 (T3)
0007 ₁₆		0027 ₁₆	Timer X mode register (TXM)
0008 ₁₆	Port P4 (P4)	0028 ₁₆	Timer Y mode register (TYM)
0009 ₁₆	Port P4 direction register (P4D)	0029 ₁₆	Timer 123 mode register (T123M)
000A ₁₆	Port P5 (P5)	002A ₁₆	Clock output control register (TCON)
000B ₁₆	Port P5 direction register (P5D)	002B ₁₆	
000C ₁₆	Port P6 (P6)	002C ₁₆	
000D ₁₆	Port P6 direction register (P6D)	002D ₁₆	
000E ₁₆	Port P7 (P7)	002E ₁₆	
000F ₁₆	Port P7 direction register (P7D)	002F ₁₆	
0010 ₁₆	Port P8 (P8)	0030 ₁₆	
0011 ₁₆	Port P8 direction register (P8D)	0031 ₁₆	
0012 ₁₆		0032 ₁₆	
0013 ₁₆		0033 ₁₆	
0014 ₁₆		0034 ₁₆	A-D control register (ADCON)
0015 ₁₆		0035 ₁₆	A-D conversion register (AD)
0016 ₁₆	PULL register A (PULLA)	0036 ₁₆	
0017 ₁₆	PULL register B (PULLB)	0037 ₁₆	
0018 ₁₆	Transmit/Receive buffer register (TB/RB)	0038 ₁₆	Segment output enable register (SEG)
0019 ₁₆	Serial I/O status register (SIOSTS)	0039 ₁₆	LCD mode register (LM)
001A ₁₆	Serial I/O control register (SIO1CON)	003A ₁₆	Interrupt edge selection register (INTEDGE)
001B ₁₆	UART control register (UARTCON)	003B ₁₆	CPU mode register (CPUM)
001C ₁₆	Baud rate generator (BRG)	003C ₁₆	Interrupt request register 1(IREQ1)
001D ₁₆		003D ₁₆	Interrupt request register 2(IREQ2)
001E ₁₆		003E ₁₆	Interrupt control register 1(ICON1)
001F ₁₆		003F ₁₆	Interrupt control register 2(ICON2)

Fig. 10 Memory map of special function register (SFR)

I/O PORTS

Direction Registers

The 3825 group has 43 programmable I/O pins arranged in seven I/O ports (ports P16, P17, P2, P4–P6, P71–P77, P80 and P81). The I/O ports have direction registers which determine the input/output direction of each individual pin. (Ports P16 and P17 are shared with bits 6 and 7 of the port P1 output control register). Each bit in a direction register corresponds to one pin, and each pin can be set to be input port or output port.

When “0” is written to the bit corresponding to a pin, that pin becomes an input pin. When “1” is written to that bit, that pin becomes an output pin.

If data is read from a pin set to output, the value of the port output latch is read, not the value of the pin itself. Pins set to input are floating. If a pin set to input is written to, only the port output latch is written to and the pin remains floating.

Port P1 Output Control Register

Bit 0 of the port P1 output control register (address 0003₁₆) enables control of the output of ports P10 to P15.

When the bit is set to “1”, the port output function is valid.

In this case, setting of the PULL register A to ports P10 to P15 is invalid.

When resetting, bit 0 of the port P1 output control register is set to “0” (the port output function is invalid.)

Pull-up/Pull-down Control

By setting the PULL register A (address 0016₁₆) or the PULL register B (address 0017₁₆), ports P0 to P8 except P70 can control either pull-down or pull-up (pins that are shared with the segment output pins for LCD are pull-down; all other pins are pull-up) with a program.

However, the contents of PULL register A and PULL register B do not affect ports programmed as the output ports. (except for ports P0 and P3).

Ports P0 and P3 share the port output control function with bit 0 of the PULL register A. When set to “1”, the port output function is invalid (Pull-down is valid).

When set to “0”, the port output function is valid (Pull-down is invalid).

The PULL register A setting is invalid for pins set to segment output with the segment output enable register.

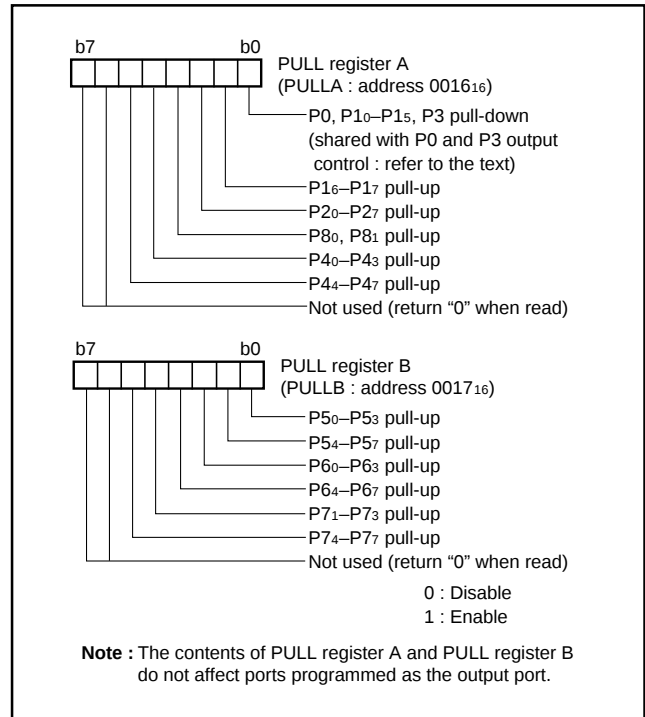


Fig. 11 Structure of PULL register A and PULL register B

Table 6. I/O ports functions

Pin	Name	Input/Output	I/O Format	Non-Port Function	Related SFRs	Diagram No.
P00/SEG26– P07/SEG33	Port P0	Output	CMOS 3-state output	LCD segment output	PULL register A Segment output enable register	(1)
P10/SEG34– P15/SEG39	Port P1	Output	CMOS 3-state output	LCD segment output	PULL register A Segment output enable register Port P1 output control register	(1)
P16 , P17		Input/output, individual bits	CMOS compatible input level CMOS 3-state output		PULL register A	(2)
P20–P27	Port P2	Input/output, individual bits	CMOS compatible input level CMOS 3-state output	Key-on wake up interrupt input	PULL register A Interrupt control register 2	(2)
P30/SEG18– P37/SEG25	Port P3	Output	CMOS 3-state output	LCD segment output	PULL register A Segment output enable register	(1)
P40/f(X _{IN})/ f(X _{IN})/2, P41/f(X _{IN})/5/ f(X _{IN})/10	Port P4	Input/output, individual bits	CMOS compatible input level CMOS 3-state output	Clock output	Clock output control register PULL register A	(2)
P42/INT0, P43/INT1				External interrupt input	PULL register A Interrupt edge selection register	
P44/RxD P54/TxD P46/SCLK P47/SRDY				Serial I/O function I/O	PULL register A Serial I/O control register Serial I/O status register UART control register	(3)
						(4)
P50/INT2, P51/INT3	Port P5	Input/output, individual bits	CMOS compatible input level CMOS 3-state output	External interrupt input	PULL register B Interrupt edge selection register	(2)
P52/RTP0, P53/RTP1				Real time port function output	PULL register B Timer X mode register	(7)
P54/CNTR0				Timer X function I/O	PULL register B Timer X mode register	(8)
P55/CNTR1				Timer Y function input	PULL register B Timer Y mode register	(9)
P56/TOUT				Timer 2 output	PULL register B Timer 123 mode register	(8)
P57/ADT				A-D trigger input	PULL register B A-D control register	(9)
P60/AN0– P67/AN7	Port P6	Input/output, individual bits	CMOS compatible input level CMOS 3-state output	A-D conversion input	PULL register B A-D control register	(10)
P70	Port P7	Input	CMOS compatible input level			(11)
P71–P77		Input/output, individual bits	CMOS compatible input level CMOS 3-state output		PULL register B	(12)
P80/XCOUT	Port P8	Input/output, individual bits	CMOS compatible input level CMOS 3-state output	Sub-clock generating circuit	PULL register A CPU mode register	(13)
P81/XCIN						(14)
COM0–COM3	Common	Output	LCD common output		LCD mode register	(15)
SEG0–SEG17	Segment	Output	LCD segment output			(16)

Note 1: When using double-function ports as functional I/O pins, refer the method to the relevant sections.

2: Make sure that the input level at each pin is either 0 V or V_{CC} during execution of the STP instruction.

When an input level is at an intermediate potential, a current will flow from V_{CC} to V_{SS} through the input-stage gate.

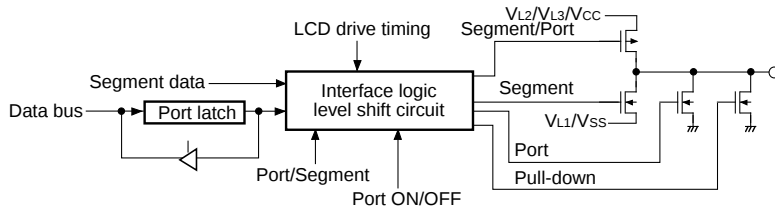
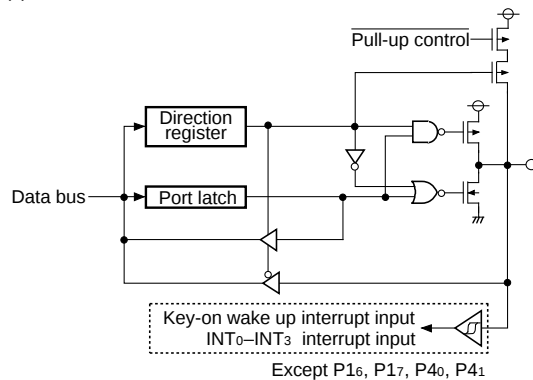
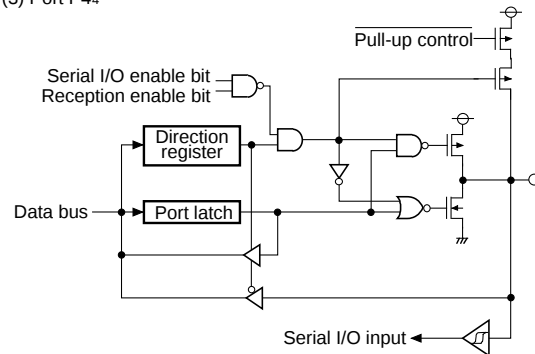
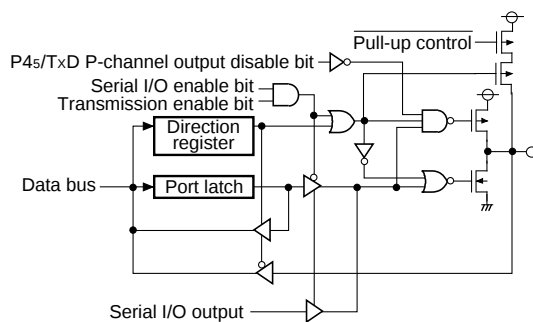
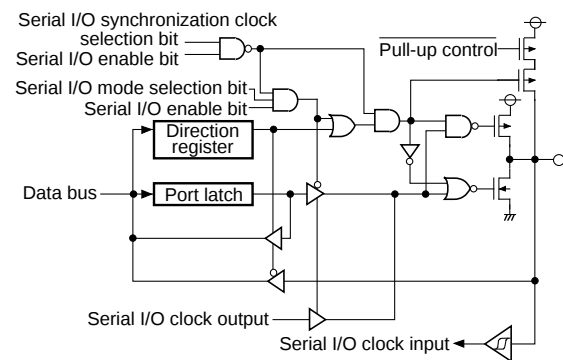
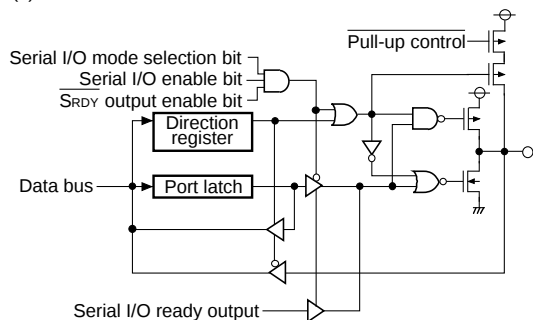
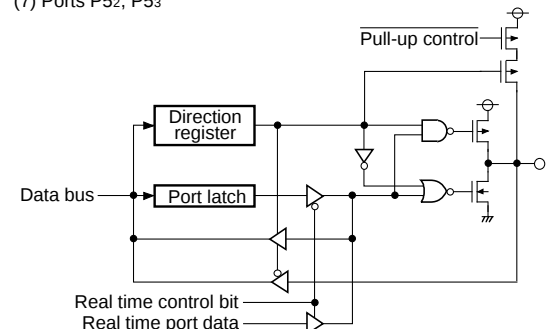
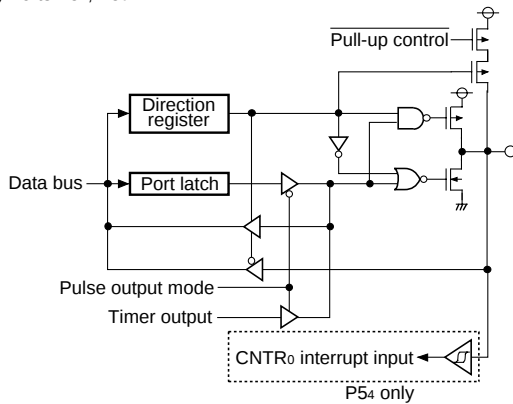
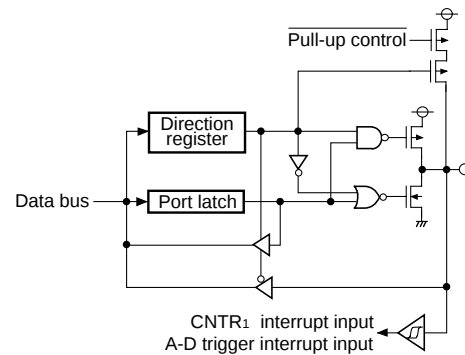
(1) Ports P0, P1₀–P1₅, P3(2) Ports P1₆, P1₇, P2, P4₀–P4₃, P5₀, P5₁(3) Port P4₄(4) Port P4₅(5) Port P4₆(6) Port P4₇(7) Ports P5₂, P5₃

Fig. 12 Port block diagram (1)

(8) Ports P5₄, P5₆(9) Ports P5₅, P5₇

(10) Port P6

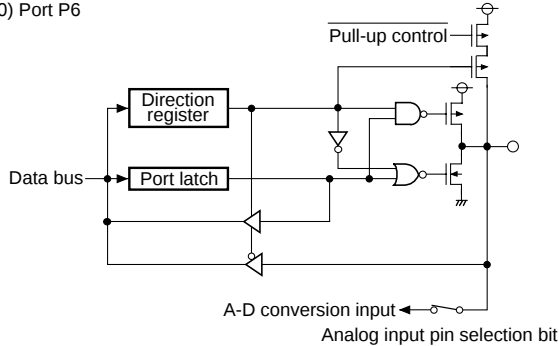
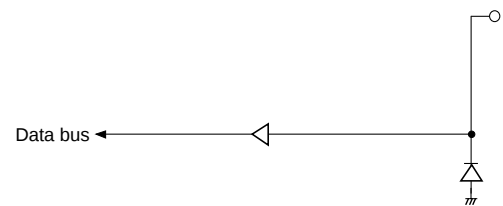
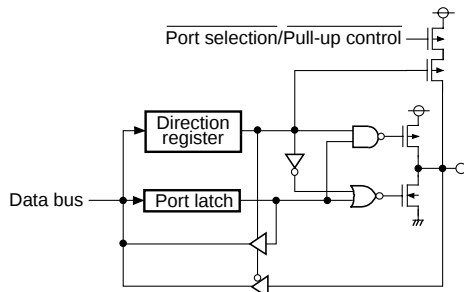
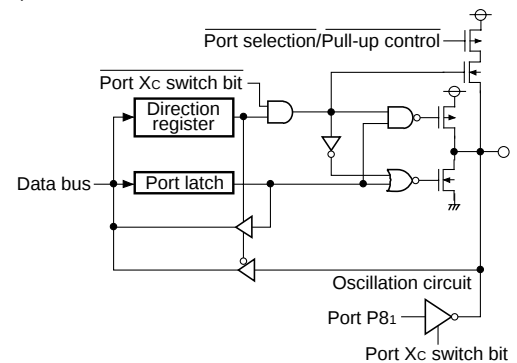
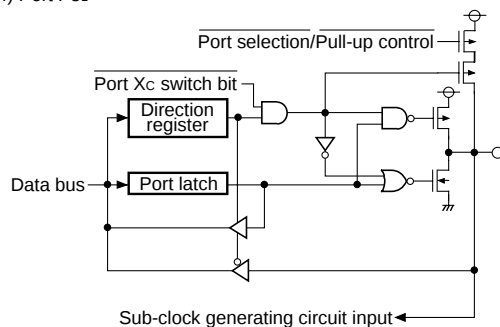
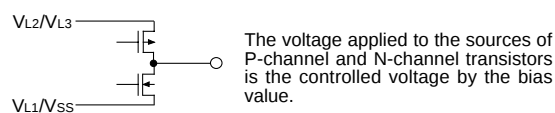
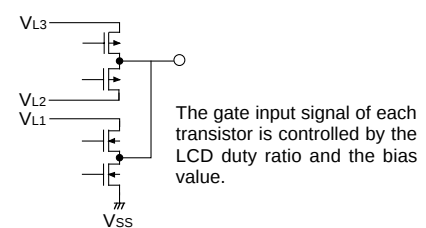
(11) Port P7₀(12) Ports P7₁–P7₇(13) Port P8₀(14) Port P8₁(16) SEG₀–SEG₁₇(15) COM₀–COM₃

Fig. 13 Port block diagram (2)

INTERRUPTS

Interrupts occur by seventeen sources: eight external, eight internal, and one software.

Interrupt Control

Each interrupt is controlled by an interrupt request bit, an interrupt enable bit, and the interrupt disable flag except for the software interrupt set by the BRK instruction. An interrupt occurs if the corresponding interrupt request and enable bits are "1" and the interrupt disable flag is "0".

Interrupt enable bits can be set or cleared by software.

Interrupt request bits can be cleared by software, but cannot be set by software.

The BRK instruction cannot be disabled with any flag or bit. The I flag disables all interrupts except the BRK instruction interrupt.

When several interrupts occur at the same time, the interrupts are received according to priority.

Interrupt Operation

By acceptance of an interrupt, the following operations are automatically performed:

1. The contents of the program counter and the processor status register are automatically pushed onto the stack.
2. The interrupt disable flag is set and the corresponding interrupt request bit is cleared.
3. The interrupt jump destination address is read from the vector table into the program counter.

■Notes

When the active edge of an external interrupt (INT0–INT3, CNTR0, or CNTR1) is changed, the corresponding interrupt request bit may also be set. Therefore, please take following sequence:

- (1) Disable the external interrupt which is selected
- (2) Change the active edge selection (use the timer X mode register for CNTR0, the timer Y mode register for CNTR1)
- (3) Clear the interrupt request bit which is selected to "0"
- (4) Enable the external interrupt which is selected.

Table 7. Interrupt vector addresses and priority

Interrupt Source	Priority	Vector Addresses (Note 1)		Interrupt Request Generating Conditions	Remarks
		High	Low		
Reset (Note 2)	1	FFFD ₁₆	FFFC ₁₆	At reset	Non-maskable
INT0	2	FFFB ₁₆	FFFA ₁₆	At detection of either rising or falling edge of INT0 input	External interrupt (active edge selectable)
INT1	3	FFF9 ₁₆	FFF8 ₁₆	At detection of either rising or falling edge of INT1 input	External interrupt (active edge selectable)
Serial I/O reception	4	FFF7 ₁₆	FFF6 ₁₆	At completion of serial I/O data reception	Valid when serial I/O is selected
Serial I/O transmission	5	FFF5 ₁₆	FFF4 ₁₆	At completion of serial I/O transmit shift or when transmission buffer is empty	Valid when serial I/O is selected
Timer X	6	FFF3 ₁₆	FFF2 ₁₆	At timer X underflow	
Timer Y	7	FFF1 ₁₆	FFF0 ₁₆	At timer Y underflow	
Timer 2	8	FFE _F 1 ₁₆	FFE _E 1 ₁₆	At timer 2 underflow	
Timer 3	9	FFED ₁₆	FFEC ₁₆	At timer 3 underflow	
CNTR0	10	FFE _B 1 ₁₆	FFE _A 1 ₁₆	At detection of either rising or falling edge of CNTR0 input	External interrupt (active edge selectable)
CNTR1	11	FFE ₉ 1 ₁₆	FFE ₈ 1 ₁₆	At detection of either rising or falling edge of CNTR1 input	External interrupt (active edge selectable)
Timer 1	12	FFE ₇ 1 ₁₆	FFE ₆ 1 ₁₆	At timer 1 underflow	
INT2	13	FFE ₅ 1 ₁₆	FFE ₄ 1 ₁₆	At detection of either rising or falling edge of INT2 input	External interrupt (active edge selectable)
INT3	14	FFE ₃ 1 ₁₆	FFE ₂ 1 ₁₆	At detection of either rising or falling edge of INT3 input	External interrupt (active edge selectable)
Key input (Key-on wake up)	15	FFE ₁ 1 ₁₆	FFE ₀ 1 ₁₆	At falling of conjunction of input level for port P2 (at input mode)	External interrupt (valid when an "L" level is applied)
ADT	16	FFD _F 1 ₁₆	FFD _E 1 ₁₆	At falling of ADT input	Valid when ADT interrupt is selected External interrupt (Valid at falling)
A-D conversion				At completion of A-D conversion	Valid when A-D interrupt is selected
BRK instruction	17	FFD _D 1 ₁₆	FFD _C 1 ₁₆	At BRK instruction execution	Non-maskable software interrupt

Notes 1: Vector addresses contain interrupt jump destination addresses.

2: Reset function in the same way as an interrupt with the highest priority.

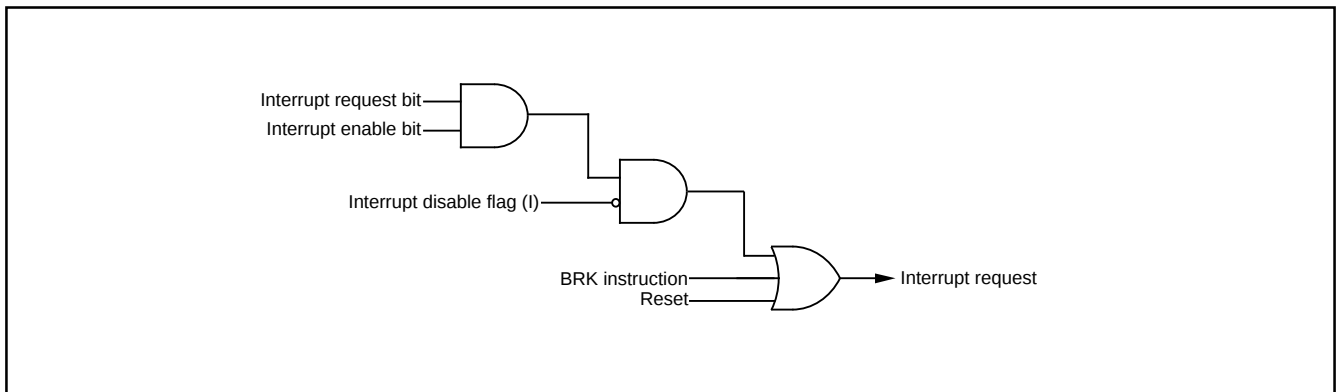


Fig. 14 Interrupt control

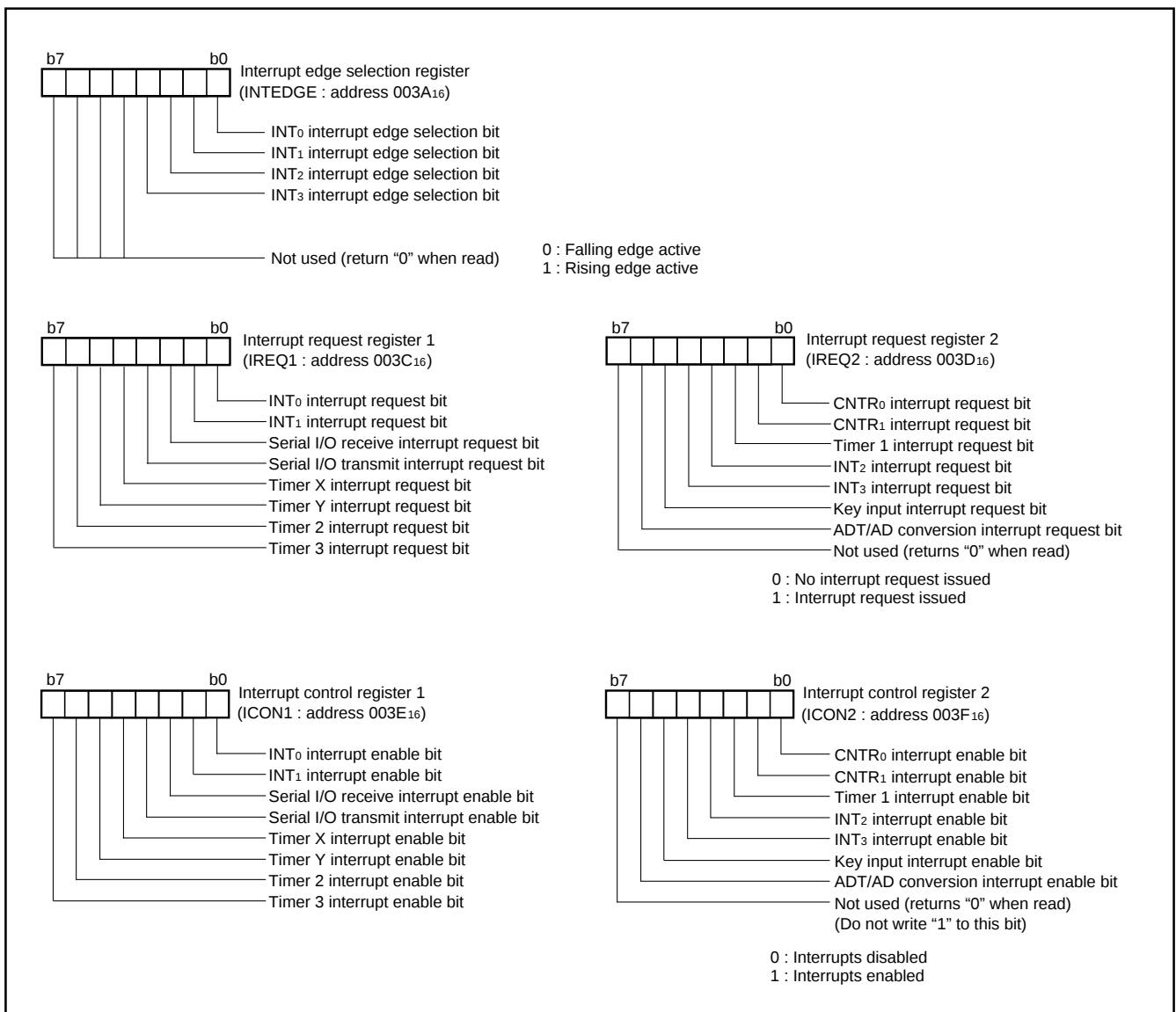


Fig. 15 Structure of interrupt-related registers

Key Input Interrupt (Key-on Wake Up)

A Key-on wake up interrupt request is generated by applying a falling edge to any pin of port P2 that have been set to input mode. In other words, it is generated when AND of input level goes from

"1" to "0". An example of using a key input interrupt is shown in Figure 16, where an interrupt request is generated by pressing one of the keys consisted as an active-low key matrix which inputs to ports P20–P23.

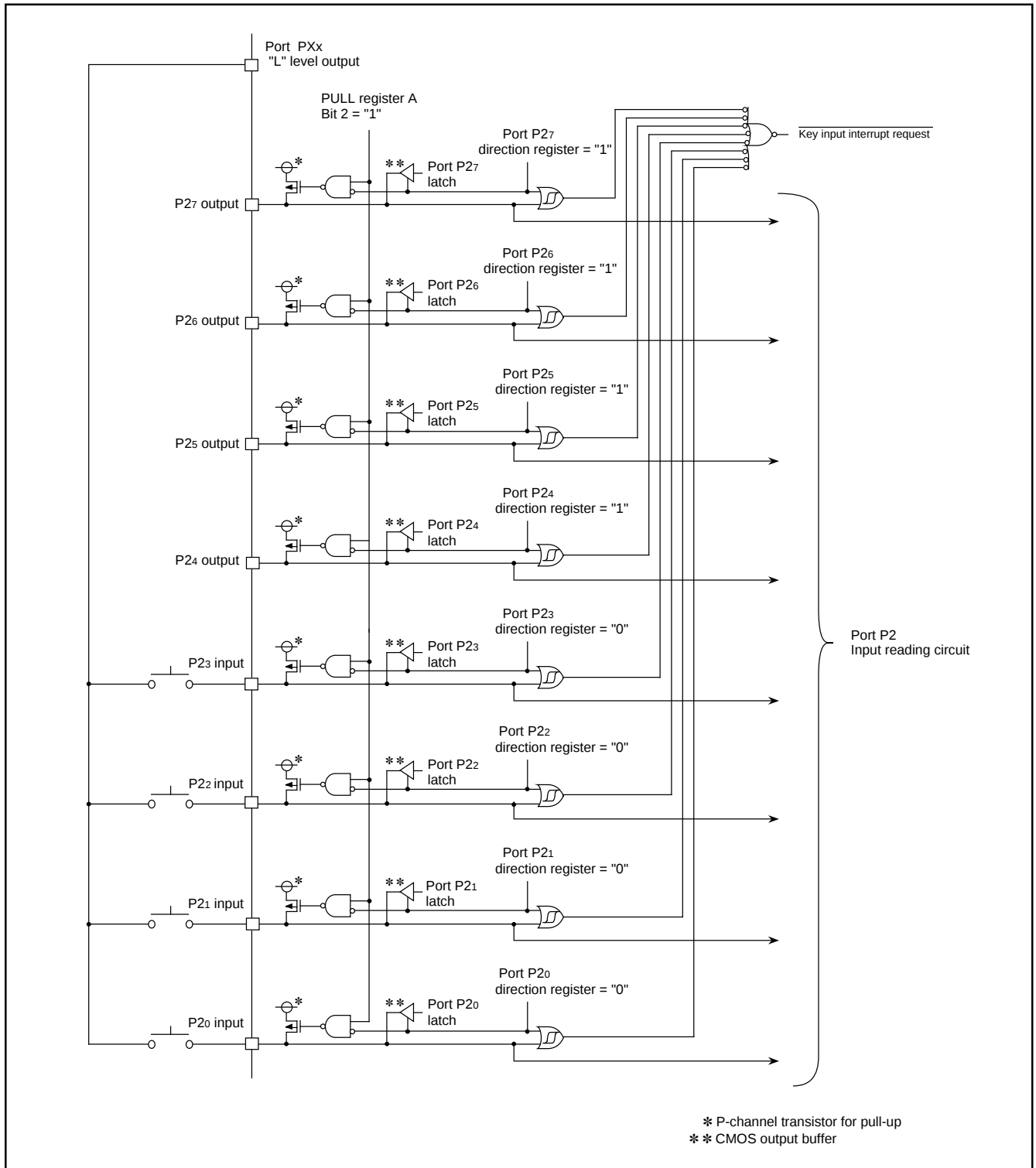


Fig. 16 Connection example when using key input interrupt and port P2 block diagram

TIMERS

The 3825 group has five timers: timer X, timer Y, timer 1, timer 2, and timer 3. Timer X and timer Y are 16-bit timers, and timer 1, timer 2, and timer 3 are 8-bit timers.

All timers are down count timers. When the timer reaches "0016", an underflow occurs at the next count pulse and the corresponding timer latch is reloaded into the timer and the count is continued. When a timer underflows, the interrupt request bit corresponding to that timer is set to "1".

Read and write operation on 16-bit timer must be performed for both high- and low-order bytes. When reading a 16-bit timer, read the high-order byte first. When writing to a 16-bit timer, write the low-order byte first. The 16-bit timer cannot perform the correct operation when reading during the write operation, or when writing during the read operation.

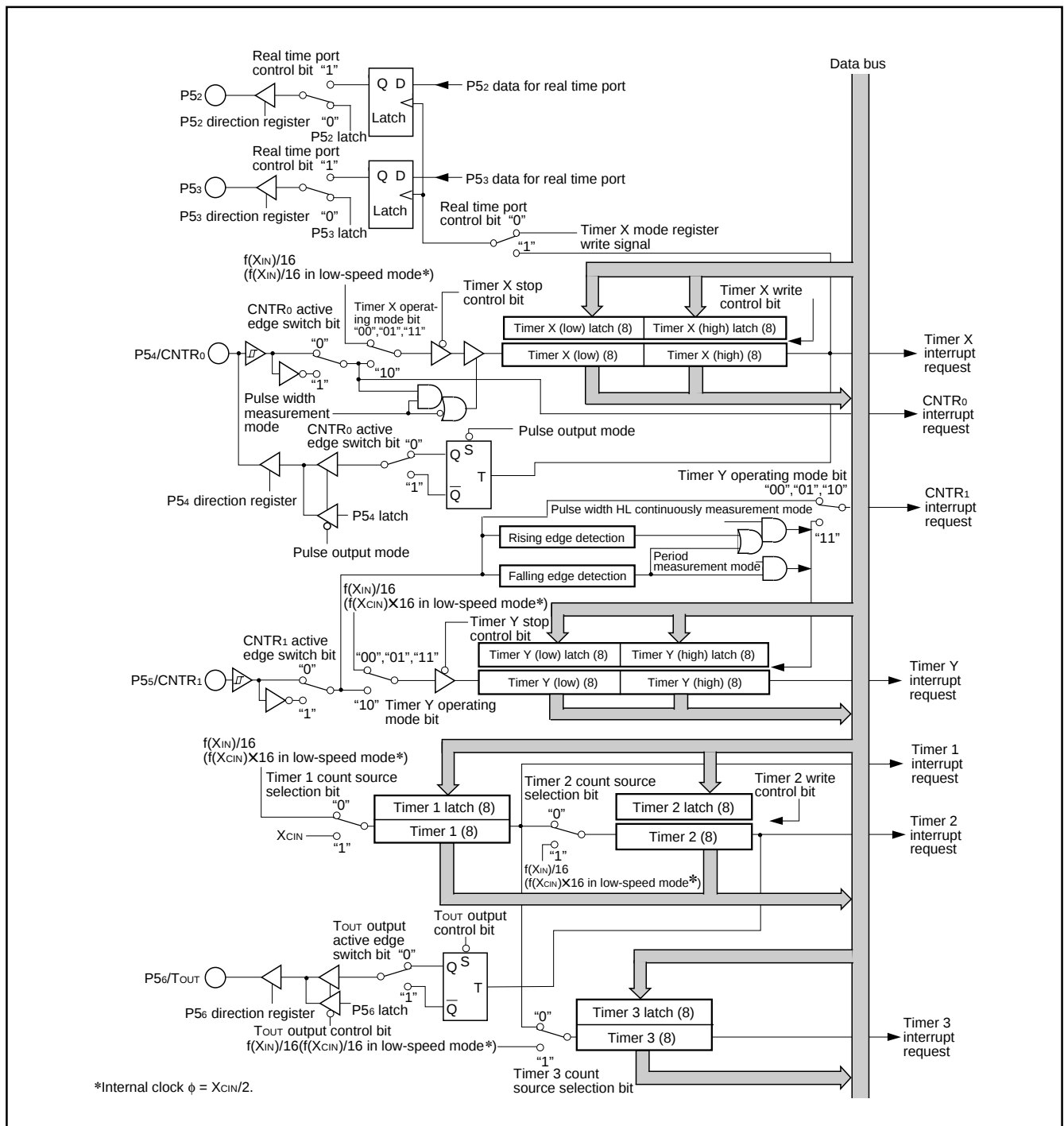


Fig. 17 Timer block diagram

Timer X

Timer X is a 16-bit timer that can be selected in one of four modes and can be controlled the timer X write and the real time port by setting the timer X mode register.

(1) Timer mode

The timer counts $f(X_{IN})/16$ (or $f(X_{CIN})/16$ in low-speed mode).

(2) Pulse output mode

Each time the timer underflows, a signal output from the CNTR0 pin is inverted. Except for this, the operation in pulse output mode is the same as in timer mode. When using a timer in this mode, set the corresponding port P54 direction register to output mode.

(3) Event counter mode

The timer counts signals input through the CNTR0 pin.

Except for this, the operation in event counter mode is the same as in timer mode. When using a timer in this mode, set the corresponding port P54 direction register to input mode.

(4) Pulse width measurement mode

The count source is $f(X_{IN})/16$ (or $f(X_{CIN})/16$ in low-speed mode. If CNTR0 active edge switch bit is "0", the timer counts while the input signal of CNTR0 pin is at "H". If it is "1", the timer counts while the input signal of CNTR0 pin is at "L". When using a timer in this mode, set the corresponding port P54 direction register to input mode.

●Timer X Write Control

If the timer X write control bit is "0", when the value is written in the address of timer X, the value is loaded in the timer X and the latch at the same time.

If the timer X write control bit is "1", when the value is written in the address of timer X, the value is loaded only in the latch. The value in the latch is loaded in timer X after timer X underflows.

If the value is written in latch only, when writing in the timer latch at the timer underflow, the value is set in the timer and the latch at one time. Additionally, unexpected value may be set in the high-order counter when the writing in high-order latch and the underflow of timer X are performed at the same timing.

●Real Time Port Control

While the real time port function is valid, data for the real time port are output from ports P52 and P53 each time the timer X underflows. (However, if the real time port control bit is changed from "0" to "1" after set of the real time port data, data are output independent of the timer X operation.) If the data for the real time port is changed while the real time port function is valid, the changed data are output at the next underflow of timer X.

Before using this function, set the corresponding port direction registers to output mode.

■Note on CNTR0 interrupt active edge selection

CNTR0 interrupt active edge depends on the CNTR0 active edge switch bit.

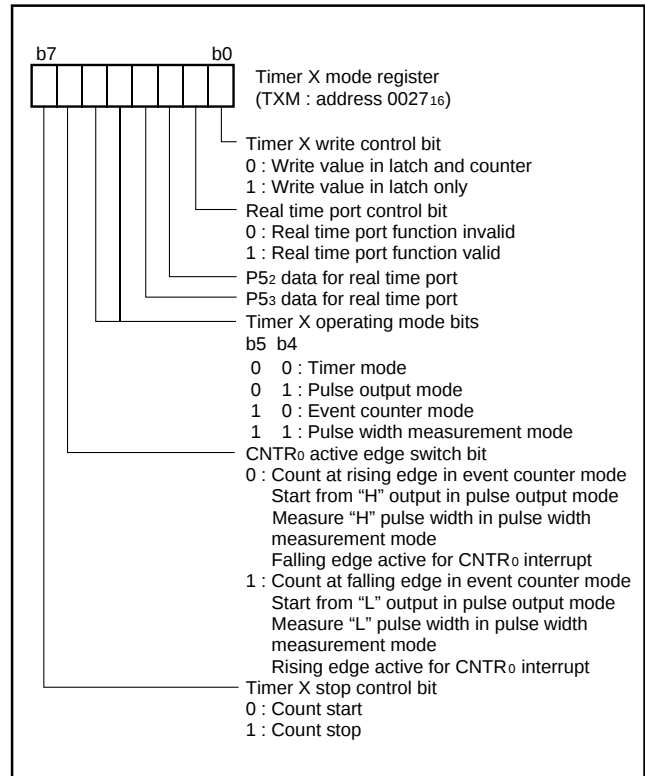


Fig. 18 Structure of timer X mode register

Timer Y

Timer Y is a 16-bit timer that can be selected in one of four modes.

(1) Timer mode

The timer counts $f(X_{IN})/16$ (or $f(X_{CIN})/16$ in low-speed mode).

(2) Period measurement mode

CNTR1 interrupt request is generated at rising/falling edge of CNTR1 pin input signal. Simultaneously, the value in timer Y latch is reloaded in timer Y and timer Y continues counting down/Except for the above-mentioned, the operation in period measurement mode is the same as in timer mode.

The timer value just before the reloading at rising/falling of CNTR1 pin input signal is retained until the timer Y is read once after the reload.

The rising/falling timing of CNTR1 pin input signal is found by CNTR1 interrupt. When using a timer in this mode, set the corresponding port P55 direction register to input mode.

(3) Event counter mode

The timer counts signals input through the CNTR1 pin.

Except for this, the operation in event counter mode is the same as in timer mode. When using a timer in this mode, set the corresponding port P55 direction register to input mode.

(4) Pulse width HL continuously measurement mode

CNTR1 interrupt request is generated at both rising and falling edges of CNTR1 pin input signal. Except for this, the operation in pulse width HL continuously measurement mode is the same as in period measurement mode. When using a timer in this mode, set the corresponding port P55 direction register to input mode.

■Note on CNTR1 interrupt active edge selection

CNTR1 interrupt active edge depends on the CNTR1 active edge switch bit. However, in pulse width HL continuously measurement mode, CNTR1 interrupt request is generated at both rising and falling edges of CNTR1 pin input signal regardless of the setting of CNTR1 active edge switch bit.

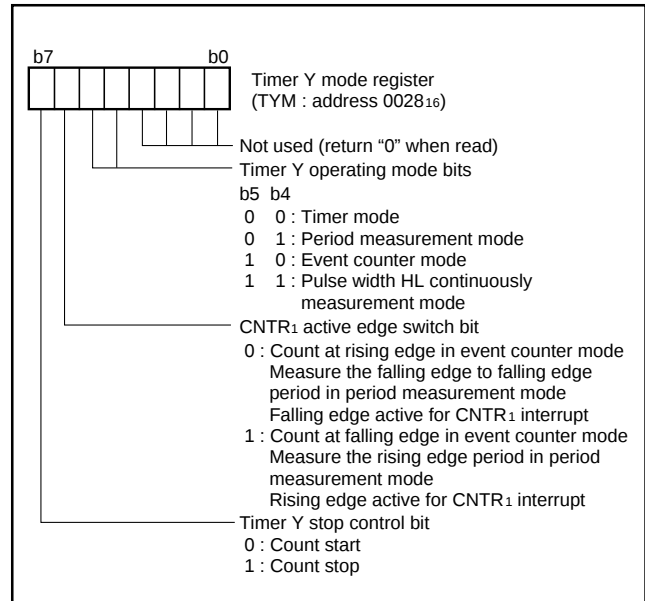


Fig. 19 Structure of timer Y mode register

Timer 1, Timer 2, Timer 3

Timer 1, timer 2, and timer 3 are 8-bit timers. The count source for each timer can be selected by timer 123 mode register. The timer latch value is not affected by a change of the count source. However, because changing the count source may cause an inadvertent count down of the timer, rewrite the value of timer whenever the count source is changed.

●Timer 2 Write Control

If the timer 2 write control bit is "0", when the value is written in the address of timer 2, the value is loaded in the timer 2 and the latch at the same time.

If the timer 2 write control bit is "1", when the value is written in the address of timer 2, the value is loaded only in the latch. The value in the latch is loaded in timer 2 after timer 2 underflows.

●Timer 2 Output Control

When the timer 2 (TOUT) is output enabled, an inversion signal from pin TOUT is output each time timer 2 underflows.

In this case, set the port P56 shared with the TOUT pin to the output mode.

■Note on Timer 1 to Timer 3

When the count source of timers 1 to 3 is changed, the timer counting value may be changed large because a thin pulse is generated in count input of timer. If timer 1 output is selected as the count source of timer 2 or timer 3, when timer 1 is written, the counting value of timer 2 or timer 3 may be changed large because a thin pulse is generated in timer 1 output.

Therefore, set the value of timer in the order of timer 1, timer 2 and timer 3 after the count source selection of timer 1 to 3.

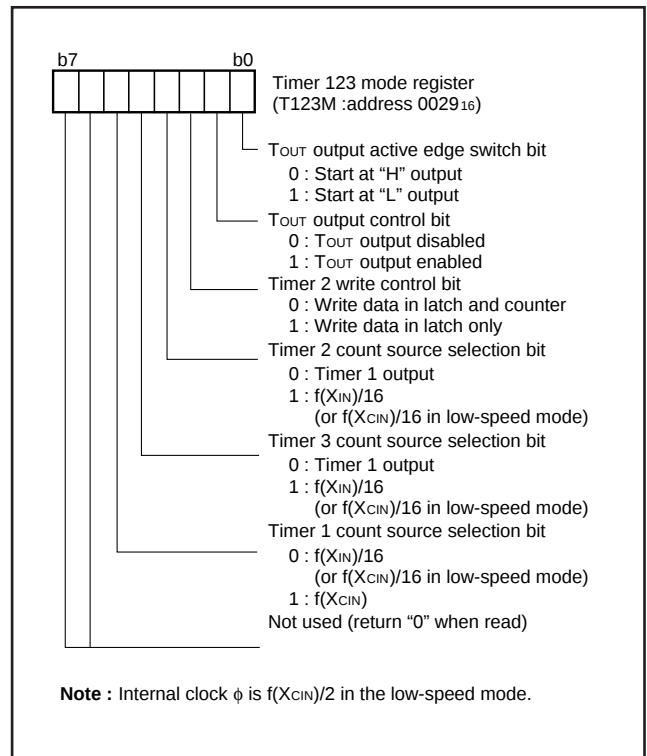


Fig. 20 Structure of timer 123 mode register

SERIAL I/O

Serial I/O can be used as either clock synchronous or asynchronous (UART) serial I/O. A dedicated timer (baud rate generator) is also provided for baud rate generation.

(1) Clock Synchronous Serial I/O Mode

Clock synchronous serial I/O mode can be selected by setting the mode selection bit of the serial I/O control register to "1".

For clock synchronous serial I/O, the transmitter and the receiver must use the same clock. If an internal clock is used, transfer is started by a write signal to the TB/RB (address 0018₁₆).

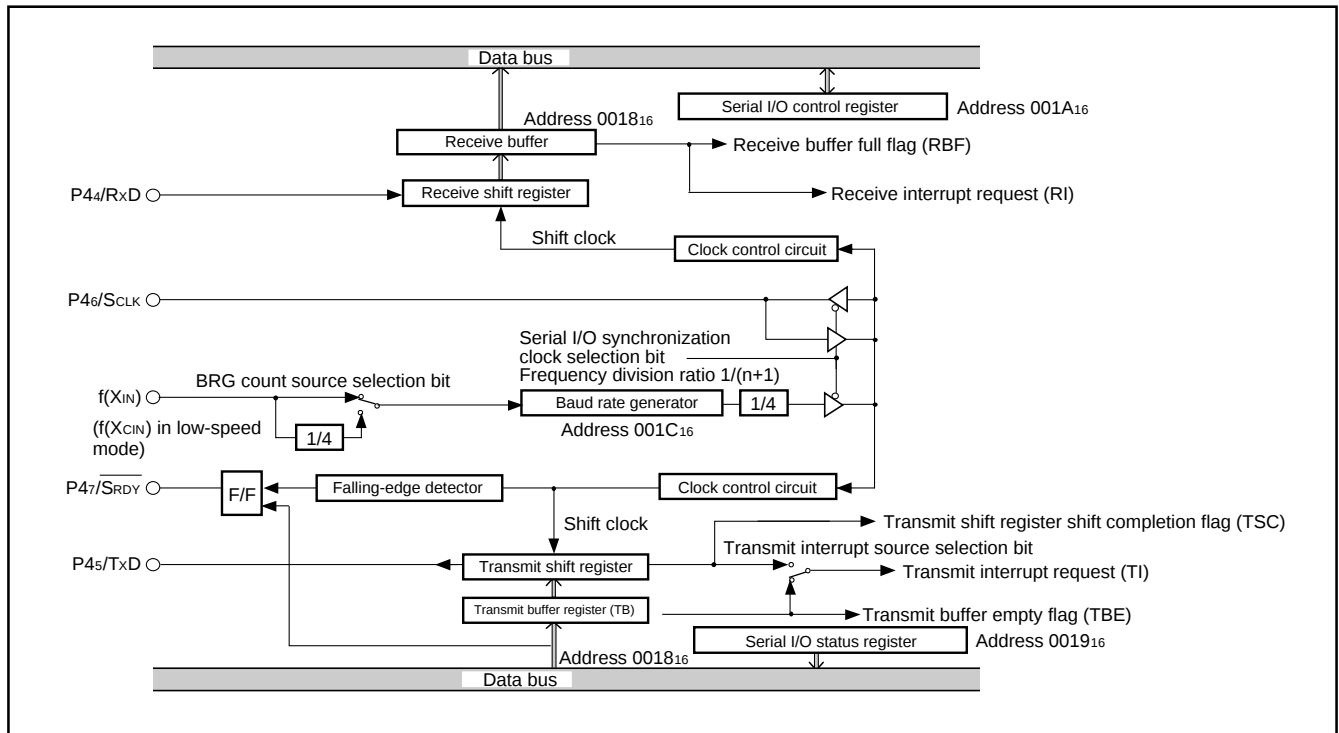


Fig. 21 Block diagram of clock synchronous serial I/O

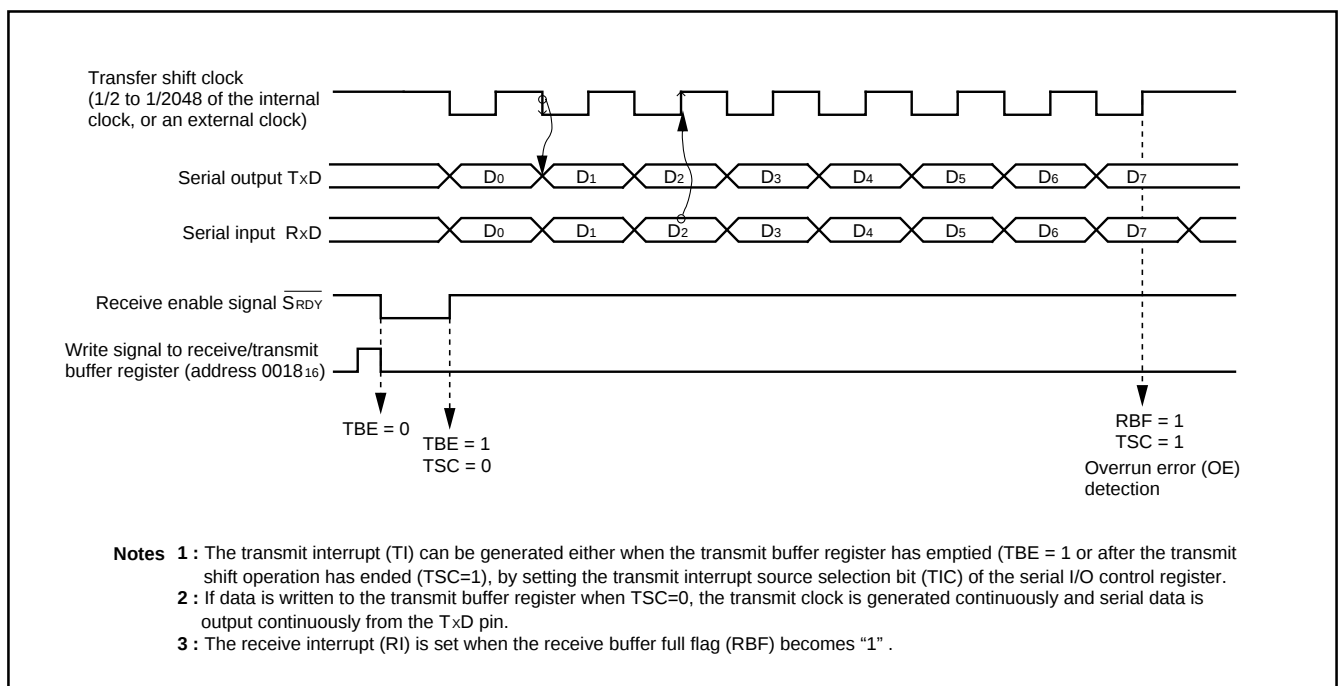


Fig. 22 Operation of clock synchronous serial I/O function

(2) Asynchronous Serial I/O (UART) Mode

Clock asynchronous serial I/O mode (UART) can be selected by clearing the serial I/O mode selection bit of the serial I/O control register to "0".

Eight serial data transfer formats can be selected, and the transfer formats used by a transmitter and receiver must be identical.

The transmit and receive shift registers each have a buffer regis-

ter, but the two buffers have the same address in memory. Since the shift register cannot be written to or read from directly, transmit data is written to the transmit buffer, and receive data is read from the receive buffer.

The transmit buffer can also hold the next data to be transmitted, and the receive buffer register can hold a character while the next character is being received.

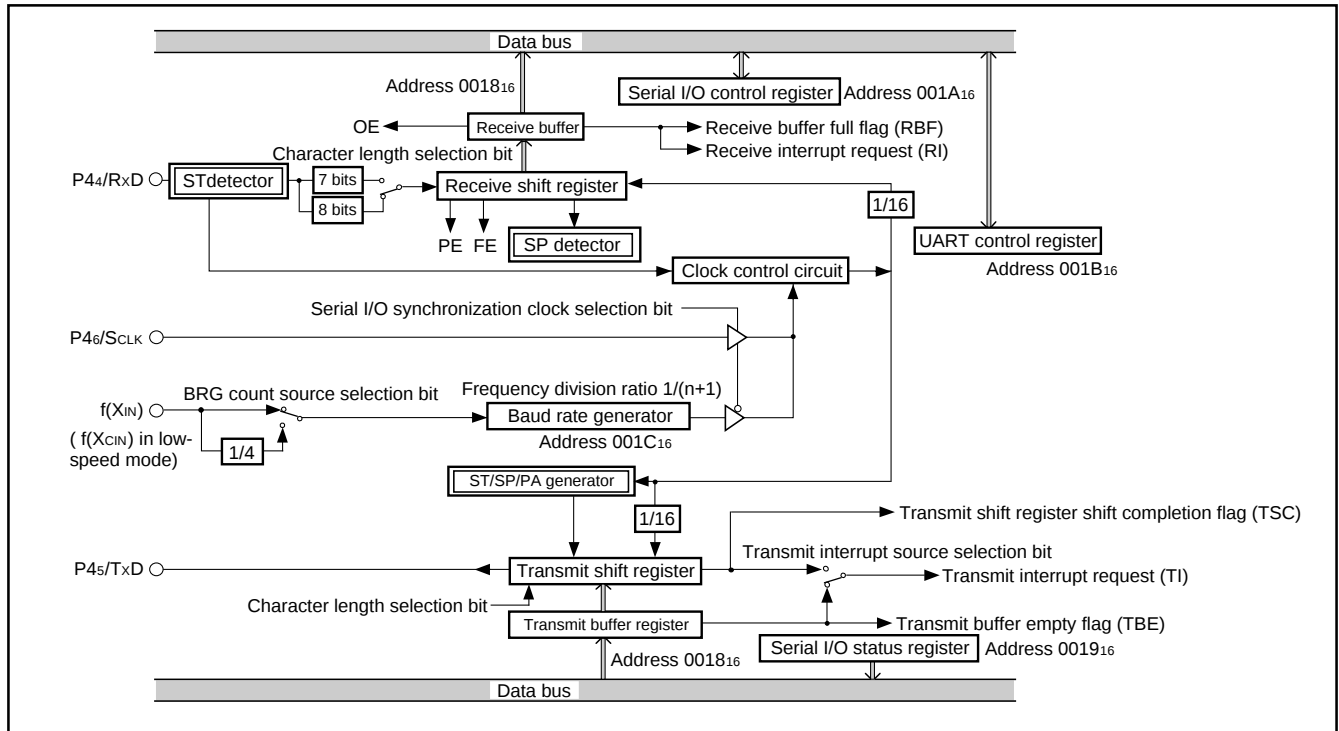


Fig. 23 Block diagram of UART serial I/O

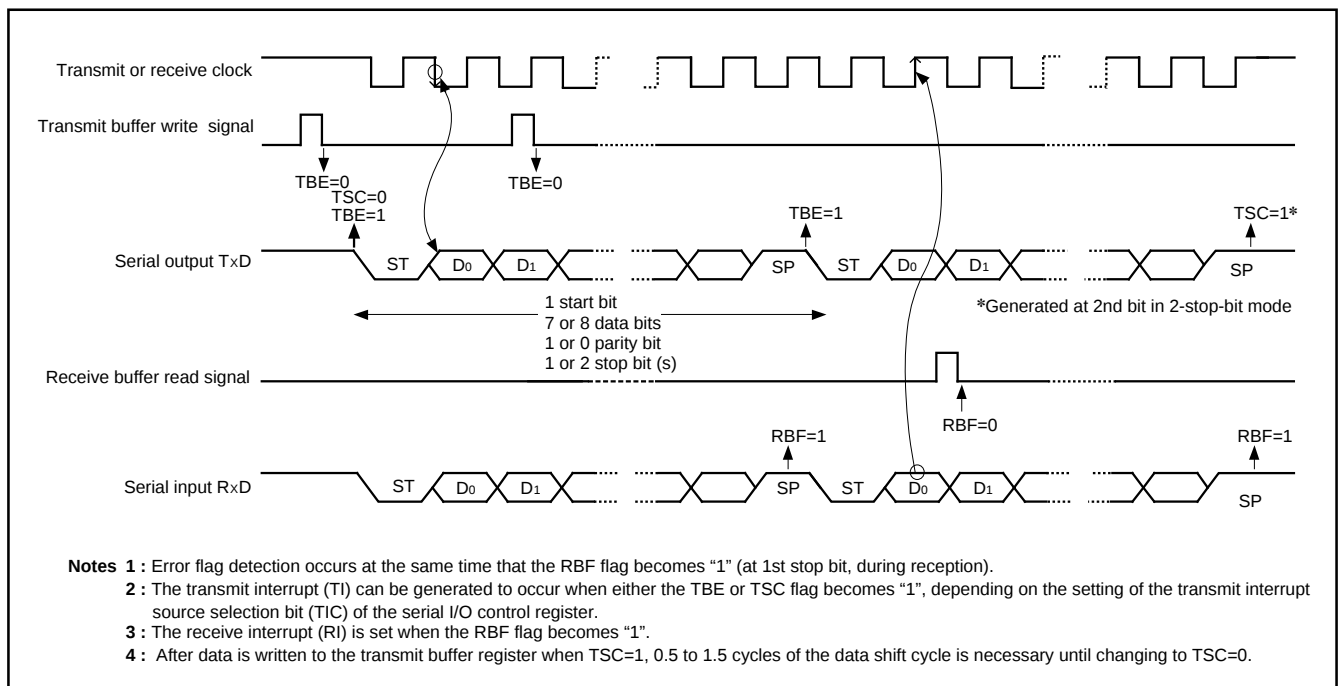


Fig. 24 Operation of UART serial I/O function

[Transmit Buffer/Receive Buffer Register (TB/RB)] 0018₁₆

The transmit buffer register and the receive buffer register are located at the same address. The transmit buffer register is write-only and the receive buffer register is read-only. If a character bit length is 7 bits, the MSB of data stored in the receive buffer register is "0".

[Serial I/O Status Register (SIOSTS)] 0019₁₆

The read-only serial I/O status register consists of seven flags (bits 0 to 6) which indicate the operating status of the serial I/O function and various errors.

Three of the flags (bits 4 to 6) are valid only in UART mode.

The receive buffer full flag (bit 1) is cleared to "0" when the receive buffer is read.

If there is an error, it is detected at the same time that data is transferred from the receive shift register to the receive buffer register, and the receive buffer full flag is set. A write to the serial I/O status register clears all the error flags OE, PE, FE, and SE (bit 3 to bit 6, respectively). Writing "0" to the serial I/O enable bit SIOE (bit 7 of the Serial I/O Control Register) also clears all the status flags, including the error flags.

All bits of the serial I/O status register are initialized to "0" at reset, but if the transmit enable bit (bit 4) of the serial I/O control register has been set to "1", the transmit shift register shift completion flag (bit 2) and the transmit buffer empty flag (bit 0) become "1".

[Serial I/O Control Register (SIOCON)] 001A₁₆

The serial I/O control register contains eight control bits for the serial I/O function.

[UART Control Register (UARTCON)] 001B₁₆

The UART control register consists of four control bits (bits 0 to 3) which are valid when asynchronous serial I/O is selected and set the data format of an data transfer. One bit in this register (bit 4) is always valid and sets the output structure of the P45/TxD pin.

[Baud Rate Generator (BRG)] 001C₁₆

The baud rate generator determines the baud rate for serial transfer.

The baud rate generator divides the frequency of the count source by $1/(n + 1)$, where n is the value written to the baud rate generator.

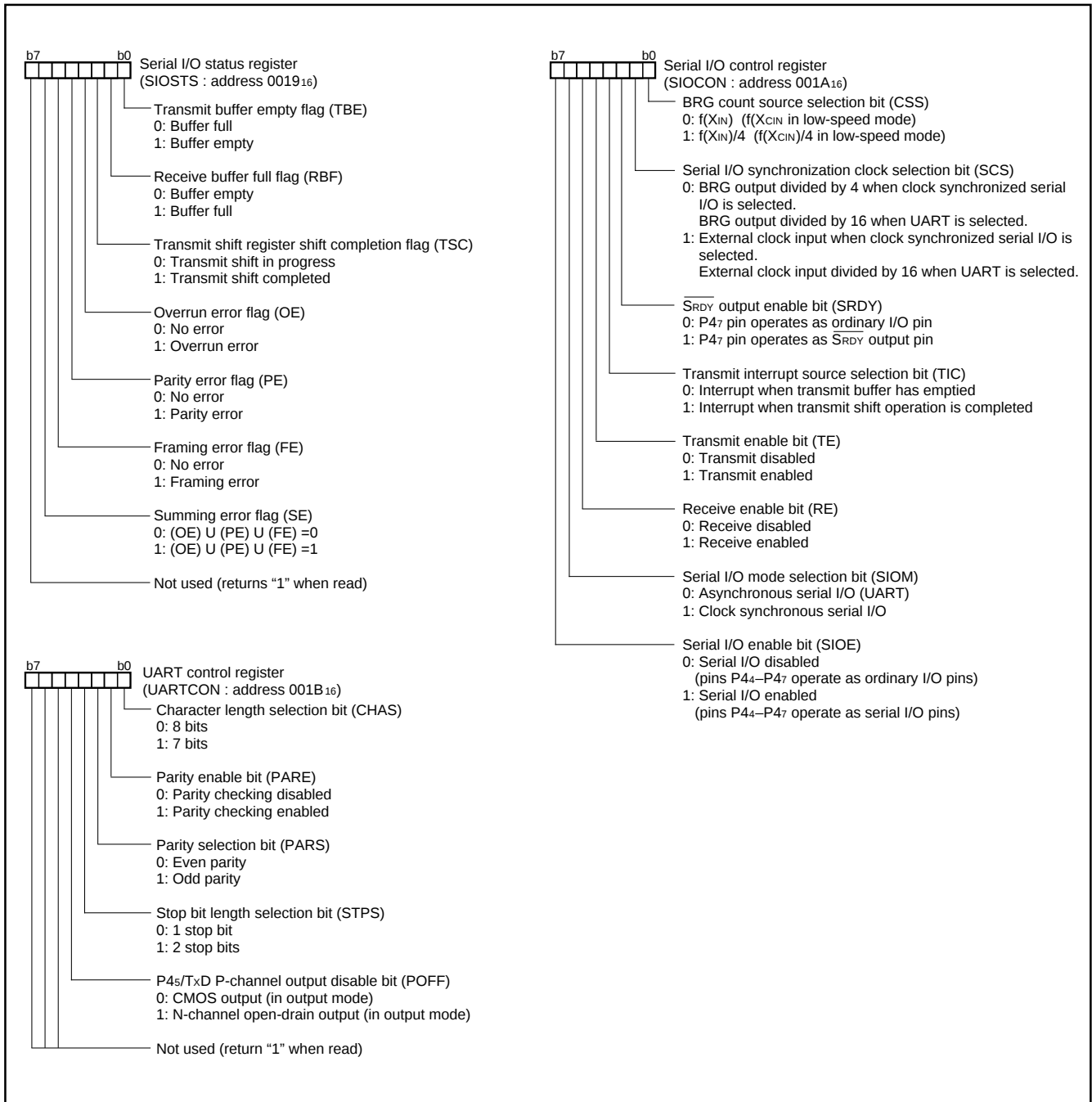


Fig. 25 Structure of serial I/O control registers

A-D CONVERTER

The functional blocks of the A-D converter are described below.

[A-D Conversion Register (AD)] 0035₁₆

The A-D conversion register is a read-only register that contains the result of an A-D conversion. When reading this register during an A-D conversion, the previous conversion result is read.

[A-D Control Register (ADCON)] 0034₁₆

The A-D control register controls the A-D conversion process. Bits 0 to 2 of this register select specific analog input pins. Bit 3 signals the completion of an A-D conversion. The value of this bit remains at "0" during an A-D conversion, then changes to "1" when the A-D conversion is completed. Writing "0" to this bit starts the A-D conversion. Bit 4 controls the transistor which breaks the through current of the resistor ladder. When bit 5, which is the AD external trigger valid bit, is set to "1", this bit enables A-D conversion even by a falling edge of an ADT input. Set ports which share with ADT pins to input when using an A-D external trigger.

Comparison Voltage Generator

The comparison voltage generator divides the voltage between AVSS and VREF by 256, and outputs the divided voltages.

Channel Selector

The channel selector selects one of the input ports P67/AN7–P60/AN0.

Comparator and Control Circuit

The comparator and control circuit compare an analog input voltage with the comparison voltage and store the result in the A-D conversion register. When an A-D conversion is completed, the control circuit sets the AD conversion completion bit and the AD interrupt request bit to "1".

Note that the comparator is constructed linked to a capacitor, so set f(XIN) to at least 500kHz during A-D conversion.

Use the clock divided from the main clock XIN as the internal clock ϕ .

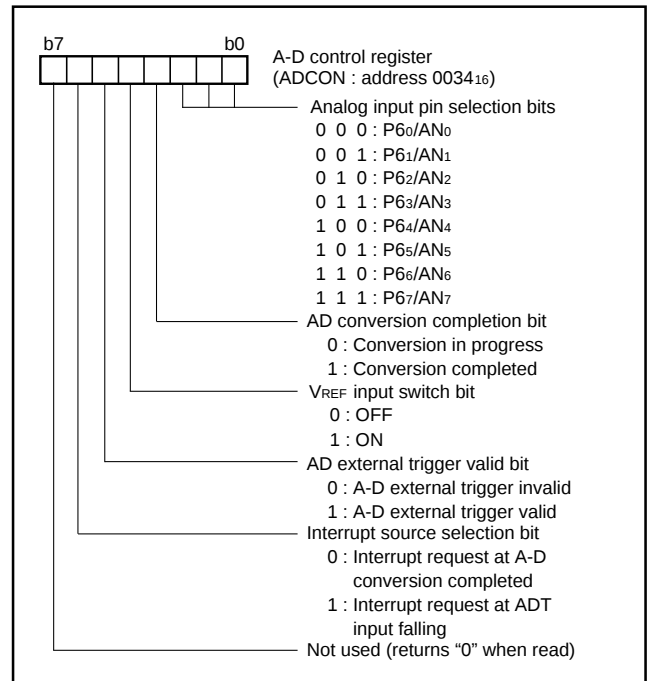


Fig. 26 Structure of A-D control register

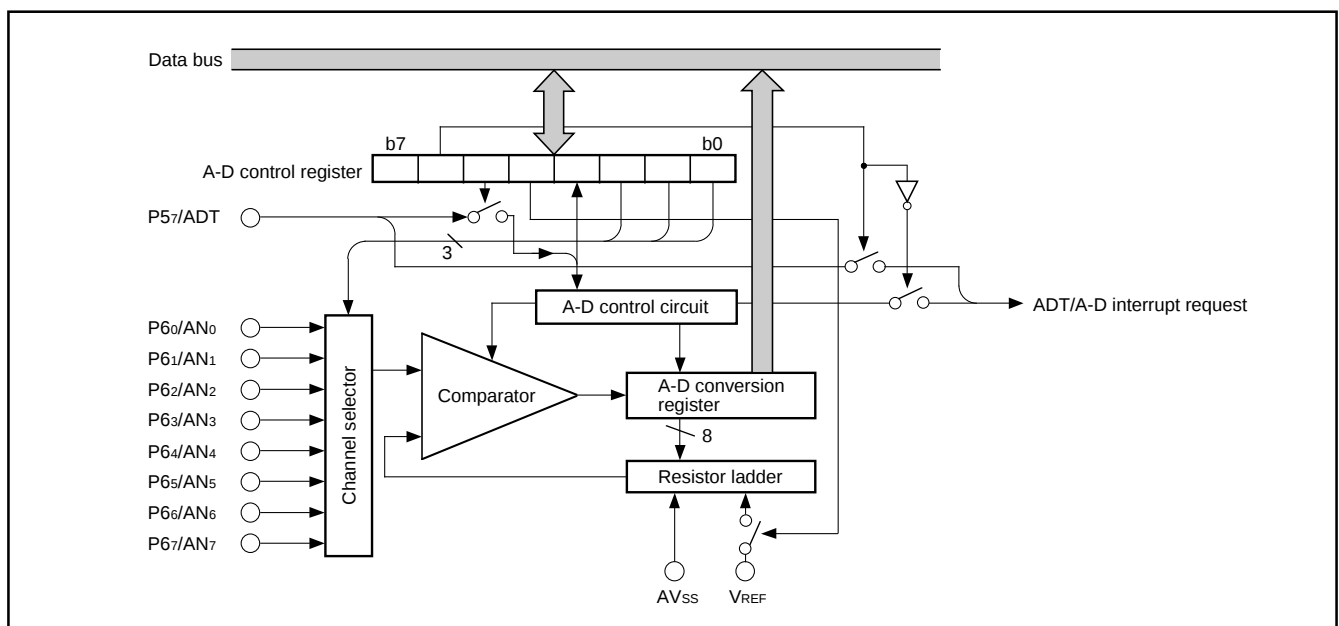


Fig. 27 A-D converter block diagram

LCD DRIVE CONTROL CIRCUIT

The 3825 group has the built-in Liquid Crystal Display (LCD) drive control circuit consisting of the following.

- LCD display RAM
- Segment output enable register
- LCD mode register
- Voltage multiplier
- Selector
- Timing controller
- Common driver
- Segment driver
- Bias control circuit

A maximum of 40 segment output pins and 4 common output pins can be used.

Up to 160 pixels can be controlled for LCD display. When the LCD

enable bit is set to "1" after data is set in the LCD mode register, the segment output enable register and the LCD display RAM, the LCD drive control circuit starts reading the display data automatically, performs the bias control and the duty ratio control, and displays the data on the LCD panel.

Table 8. Maximum number of display pixels at each duty ratio

Duty ratio	Maximum number of display pixel
2	80 dots or 8 segment LCD 10 digits
3	120 dots or 8 segment LCD 15 digits
4	160 dots or 8 segment LCD 20 digits

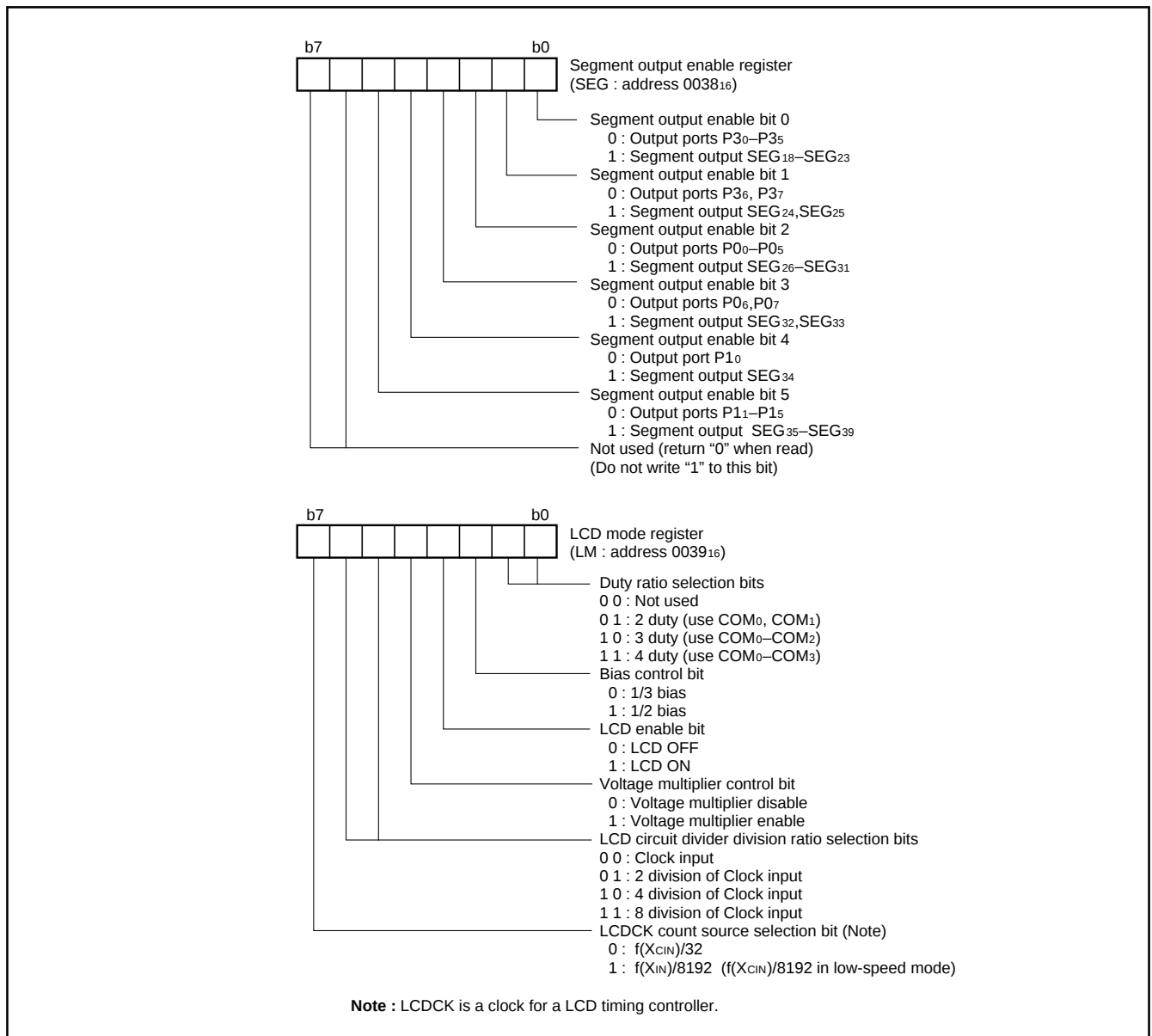


Fig. 28 Structure of segment output enable register and LCD mode register

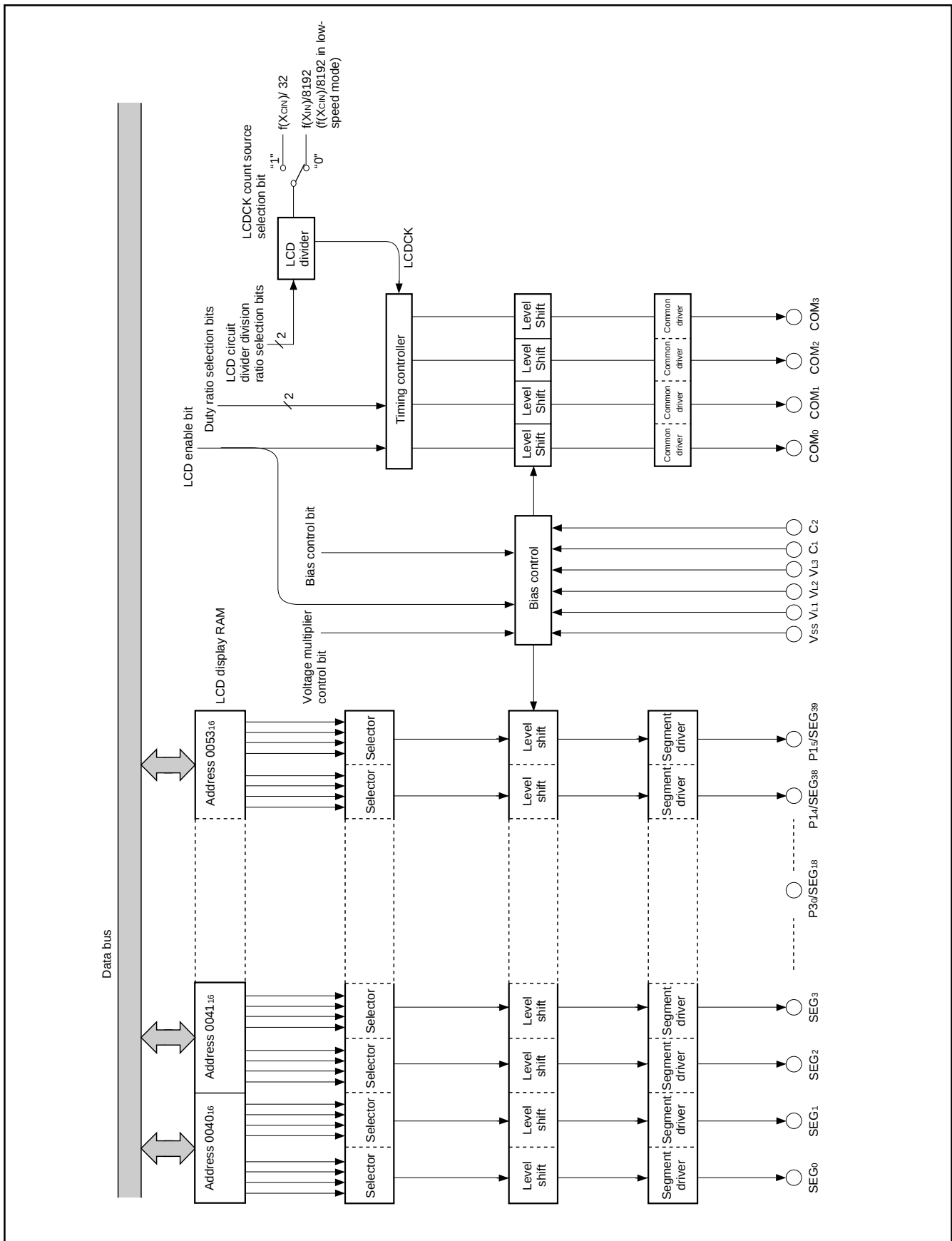


Fig. 29 Block diagram of LCD controller/driver

Voltage Multiplier (3 Times)

The voltage multiplier performs threefold boosting. This circuit inputs a reference voltage for boosting from LCD power input pin VL1. (However, when using a 1/2 bias, connect VL1 and VL2 and apply voltage by external resistor division.)

The voltage multiplier control bit (bit 4 of the LCD mode register) controls the voltage multiplier.

When voltage is input to the VL1 pin during operating the voltage multiplier, voltage that is twice as large as VL1 occurs at the VL2 pin, and voltage that is three times as large as VL1 occurs at the VL3 pin.

When using the voltage multiplier; after applying $1.3\text{ V} \leq \text{Voltage} \leq 2.3\text{ V}$ to the VL1 pin, set the voltage multiplier control bit to "1" to select the voltage multiplier enable.

When not using the voltage multiplier, apply proper voltage to the LCD power input pins (VL1–VL3).

Bias Control and Applied Voltage to LCD Power Input Pins

To the LCD power input pins (VL1–VL3), apply the voltage shown in Table 9 according to the bias value.

Select a bias value by the bias control bit (bit 2 of the LCD mode register).

Common Pin and Duty Ratio Control

The common pins (COM0–COM3) to be used are determined by duty ratio.

Select duty ratio by the duty ratio selection bits (bits 0 and 1 of the LCD mode register).

Table 9. Bias control and applied voltage to VL1–VL3

Bias value	Voltage value
1/3 bias	VL3=VLCD VL2=2/3 VLCD VL1=1/3 VLCD
1/2 bias	VL3=VLCD VL2=VL1=1/2 VLCD

Note : VLCD is the maximum value of supplied voltage for the LCD panel.

Table 10. Duty ratio control and common pins used

Duty ratio	Duty ratio selection bit		Common pins used
	Bit 1	Bit 0	
2	0	1	COM0, COM1 (Note 1)
3	1	0	COM0–COM2 (Note 2)
4	1	1	COM0–COM3

Notes 1: COM2 and COM3 are open

2: COM3 is open

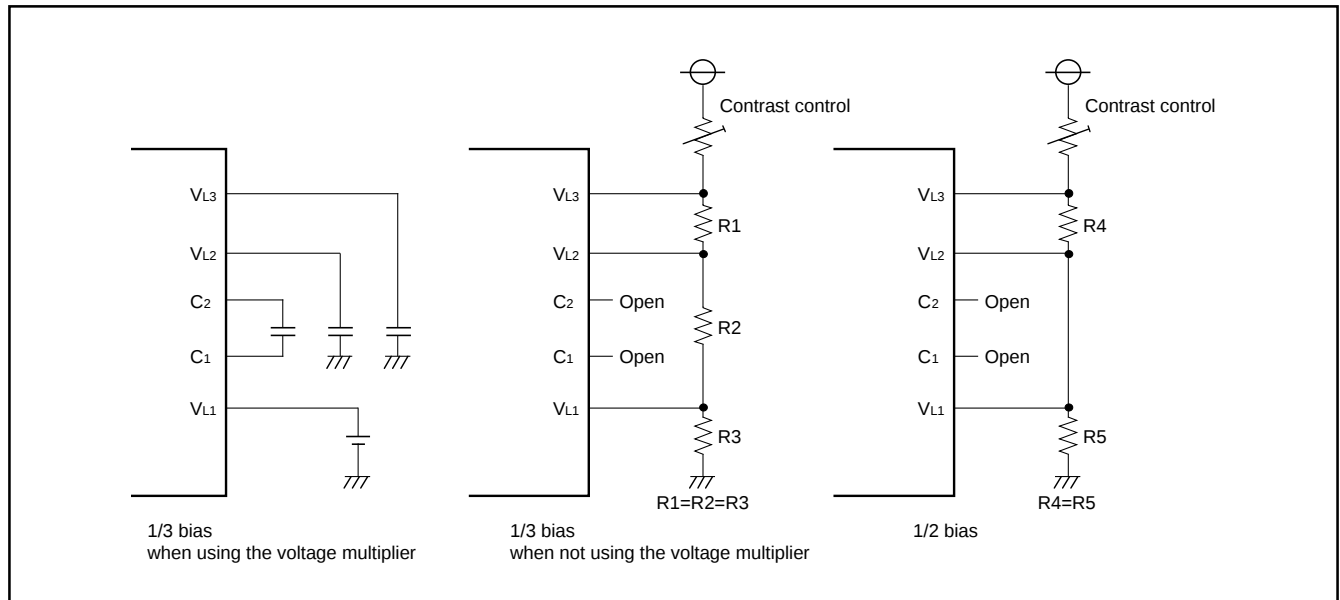


Fig. 30 Example of circuit at each bias

LCD Display RAM

Address 0040₁₆ to 0053₁₆ is the designated RAM for the LCD display. When "1" are written to these addresses, the corresponding segments of the LCD display panel are turned on.

LCD Drive Timing

The LCDCK timing frequency (LCD drive timing) is generated internally and the frame frequency can be determined with the following equation;

$$f(\text{LCDCK}) = \frac{(\text{frequency of count source for LCDCK})}{(\text{divider division ratio for LCD})}$$

$$\text{Frame frequency} = \frac{f(\text{LCDCK})}{\text{duty ratio}}$$

Bit Address	7	6	5	4	3	2	1	0
	COM ₃	COM ₂	COM ₁	COM ₀	COM ₃	COM ₂	COM ₁	COM ₀
0040 ₁₆	SEG ₁				SEG ₀			
0041 ₁₆	SEG ₃				SEG ₂			
0042 ₁₆	SEG ₅				SEG ₄			
0043 ₁₆	SEG ₇				SEG ₆			
0044 ₁₆	SEG ₉				SEG ₈			
0045 ₁₆	SEG ₁₁				SEG ₁₀			
0046 ₁₆	SEG ₁₃				SEG ₁₂			
0047 ₁₆	SEG ₁₅				SEG ₁₄			
0048 ₁₆	SEG ₁₇				SEG ₁₆			
0049 ₁₆	SEG ₁₉				SEG ₁₈			
004A ₁₆	SEG ₂₁				SEG ₂₀			
004B ₁₆	SEG ₂₃				SEG ₂₂			
004C ₁₆	SEG ₂₅				SEG ₂₄			
004D ₁₆	SEG ₂₇				SEG ₂₆			
004E ₁₆	SEG ₂₉				SEG ₂₈			
004F ₁₆	SEG ₃₁				SEG ₃₀			
0050 ₁₆	SEG ₃₃				SEG ₃₂			
0051 ₁₆	SEG ₃₅				SEG ₃₄			
0052 ₁₆	SEG ₃₇				SEG ₃₆			
0053 ₁₆	SEG ₃₉				SEG ₃₈			

Fig. 31 LCD display RAM map

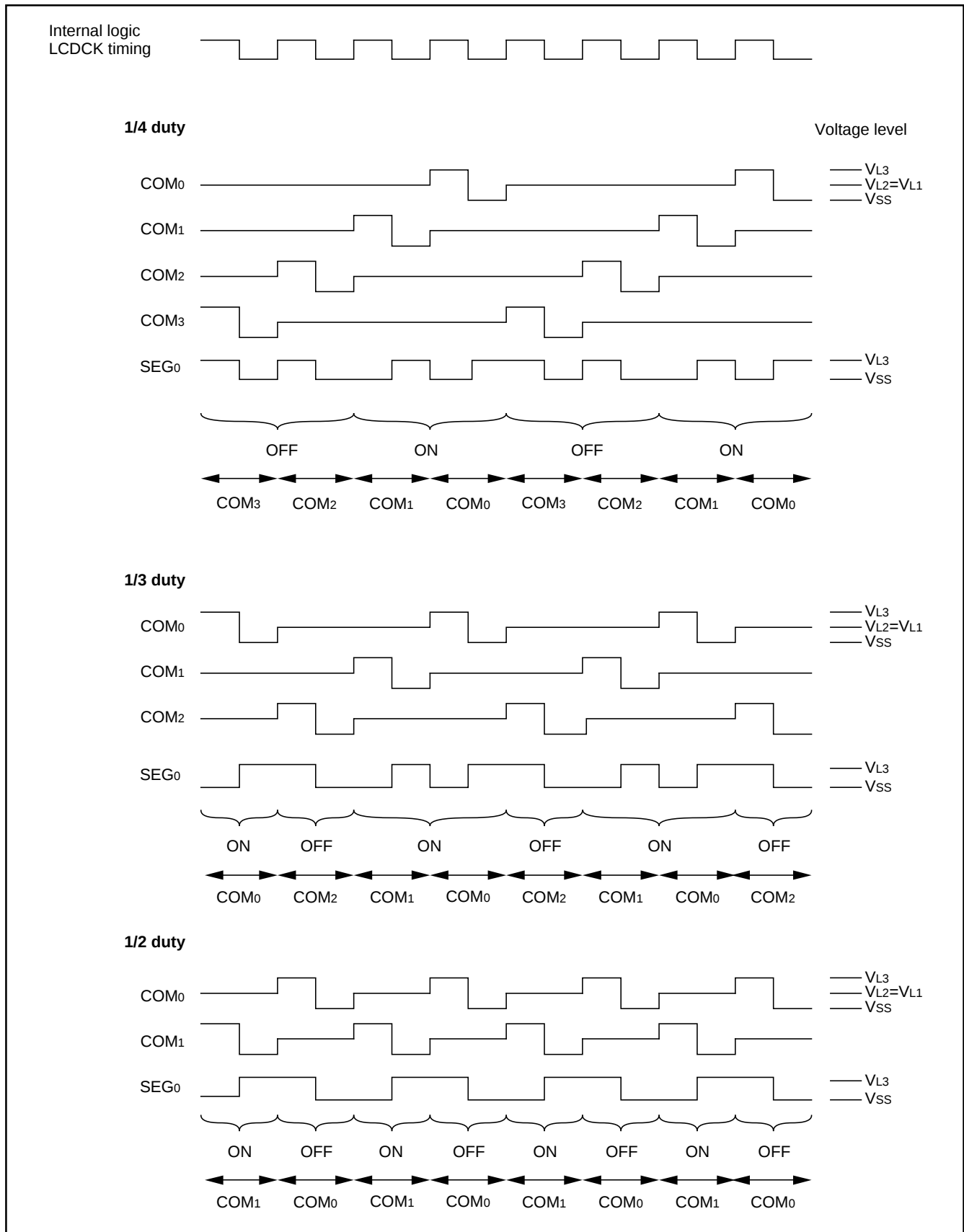


Fig. 32 LCD drive waveform (1/2 bias)

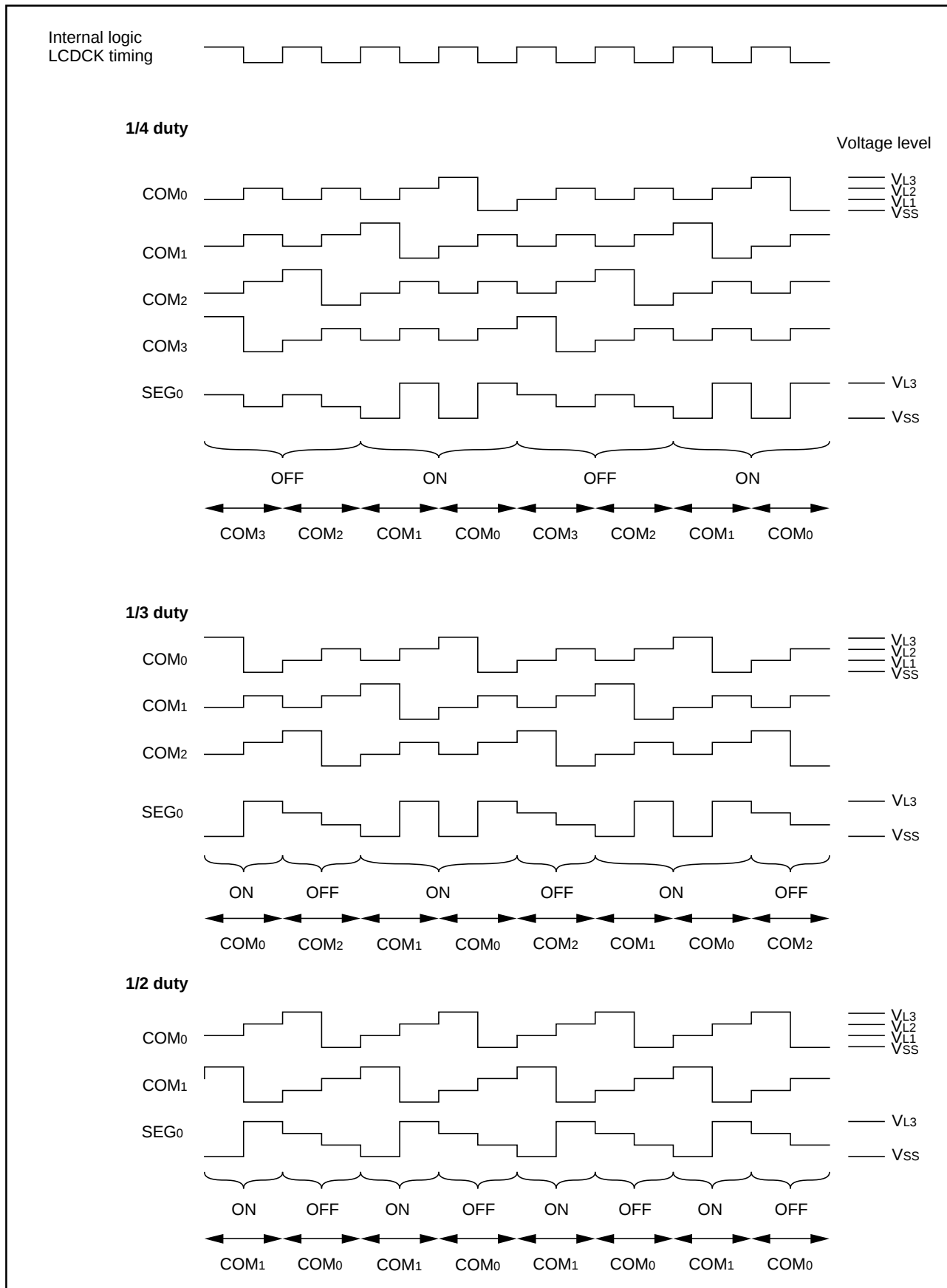


Fig. 33 LCD drive waveform (1/3 bias)

CLOCK OUTPUT FUNCTION

Input/output ports P40 and P41 can output clock. The input/output ports and clock output function are put under double function controlled by the clock output control register (address 002A₁₆).

Selection of Input/Output Ports and Clock Output Function

Bits 0 and 1 of the clock output control register can select between the input/output ports and the clock output function.

When selecting the clock output function, clocks are output while the direction register of ports P40 and P41 are set to output.

At the next cycle of rewriting the clock output control bit, P40 is switched between the port output and the clock output.

In synchronization with the fall of the clock (resulting from dividing X_{IN} by 5) on rewriting the clock output control bit, P41 is switched between the port output and the clock output.

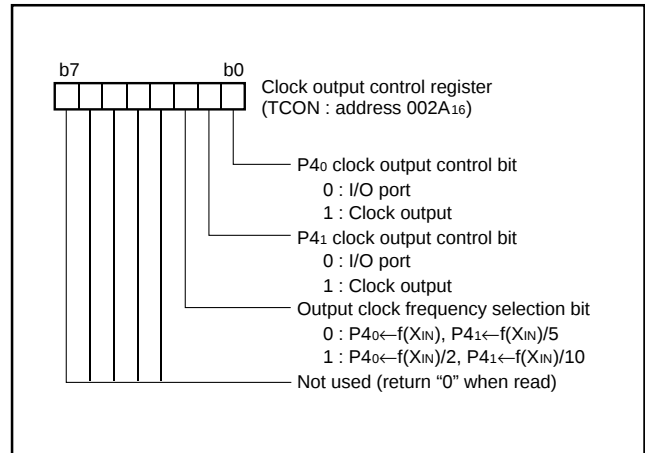


Fig. 34 Structure of clock output control register

Selection of Output Clock Frequency

Bit 2 (output clock frequency selection bit) of the clock output control register selects an output clock frequency.

When setting the output clock frequency selection bit to "0", port P40 becomes the frequency of $f(X_{IN})$ and port P41 becomes the frequency of $f(X_{IN})/5$.

At this time, the output pulse of port P40 depends on the X_{IN} input pulse, while the output pulse of port P41 has duty ratio of about 40%.

When setting the output clock frequency selection bit to "1", port P40 becomes the frequency of $f(X_{IN})/2$ and port P41 becomes the frequency of $f(X_{IN})/10$. At this time, the output pulses of both ports P40 and P41 have duty ratio of 50%.

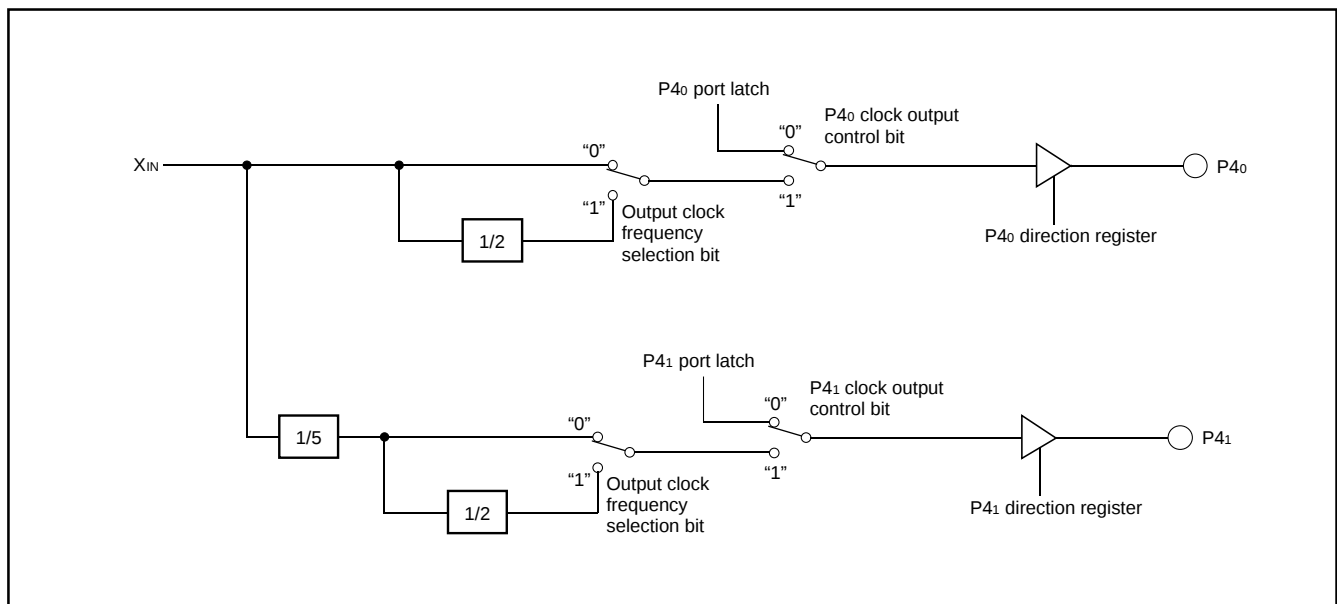


Fig. 35 Clock output function block diagram

RESET CIRCUIT

To reset the microcomputer, **RESET** pin should be held at an “L” level for 2 μ s or more. Then the **RESET** pin is returned to an “H” level (the power source voltage should be between Vcc (Min.) and 5.5 V, and the oscillation should be stable), and reset is released. After the reset is completed, the program starts from the address FFFD₁₆ (high-order byte) and address FFFC₁₆ (low-order byte). Make sure that the reset input voltage is less than 0.2 V for Vcc (Min.).

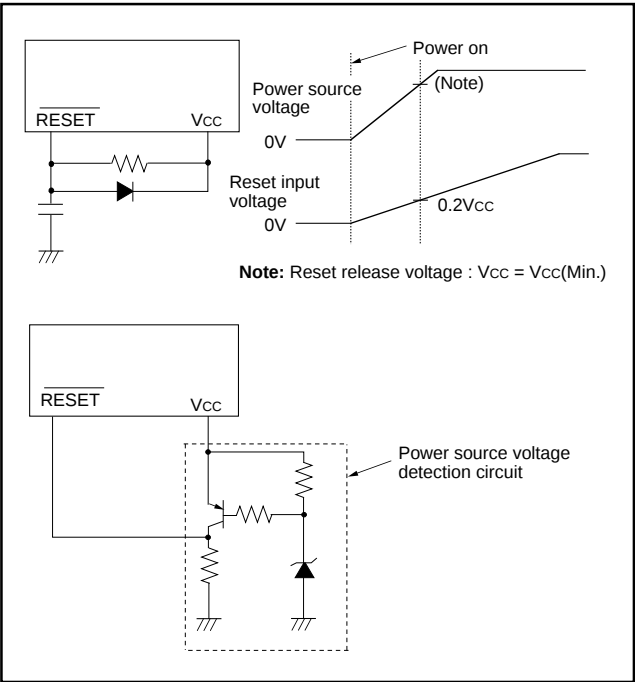


Fig. 36 Example of reset circuit

	Address	Register contents
(1) Port P0	0 0 0 0 ₁₆	00 ₁₆
(2) Port P1	0 0 0 2 ₁₆	00 ₁₆
(3) Port P1 output control register	0 0 0 3 ₁₆	00 ₁₆
(4) Port P2	0 0 0 4 ₁₆	00 ₁₆
(5) Port P2 direction register	0 0 0 5 ₁₆	00 ₁₆
(6) Port P3	0 0 0 6 ₁₆	00 ₁₆
(7) Port P4	0 0 0 8 ₁₆	00 ₁₆
(8) Port P4 direction register	0 0 0 9 ₁₆	00 ₁₆
(9) Port P5	0 0 0 A ₁₆	00 ₁₆
(10) Port P5 direction register	0 0 0 B ₁₆	00 ₁₆
(11) Port P6	0 0 0 C ₁₆	00 ₁₆
(12) Port P6 direction register	0 0 0 D ₁₆	00 ₁₆
(13) Port P7	0 0 0 E ₁₆	00 ₁₆
(14) Port P7 direction register	0 0 0 F ₁₆	00 ₁₆
(15) Port P8	0 0 1 0 ₁₆	00 ₁₆
(16) Port P8 direction register	0 0 1 1 ₁₆	00 ₁₆
(17) PULL register A	0 0 1 6 ₁₆	01 ₁₆
(18) PULL register B	0 0 1 7 ₁₆	00 ₁₆
(19) Serial I/O status register	0 0 1 9 ₁₆	1 0 0 0 0 0 0 0
(20) Serial I/O control register	0 0 1 A ₁₆	00 ₁₆
(21) UART control register	0 0 1 B ₁₆	1 1 1 0 0 0 0 0
(22) Timer X (low)	0 0 2 0 ₁₆	FF ₁₆
(23) Timer X (high)	0 0 2 1 ₁₆	FF ₁₆
(24) Timer Y (low)	0 0 2 2 ₁₆	FF ₁₆
(25) Timer Y (high)	0 0 2 3 ₁₆	FF ₁₆
(26) Timer 1	0 0 2 4 ₁₆	FF ₁₆
(27) Timer 2	0 0 2 5 ₁₆	01 ₁₆
(28) Timer 3	0 0 2 6 ₁₆	FF ₁₆
(29) Timer X mode register	0 0 2 7 ₁₆	00 ₁₆
(30) Timer Y mode register	0 0 2 8 ₁₆	00 ₁₆
(31) Timer 123 mode register	0 0 2 9 ₁₆	00 ₁₆
(32) Clock output control register	0 0 2 A ₁₆	00 ₁₆
(33) A-D control register	0 0 3 4 ₁₆	0 0 0 0 1 0 0 0
(34) Segment output enable register	0 0 3 8 ₁₆	00 ₁₆
(35) LCD mode register	0 0 3 9 ₁₆	00 ₁₆
(36) Interrupt edge selection register	0 0 3 A ₁₆	00 ₁₆
(37) CPU mode register	0 0 3 B ₁₆	0 1 0 0 1 0 0 0
(38) Interrupt request register 1	0 0 3 C ₁₆	00 ₁₆
(39) Interrupt request register 2	0 0 3 D ₁₆	00 ₁₆
(40) Interrupt control register 1	0 0 3 E ₁₆	00 ₁₆
(41) Interrupt control register 2	0 0 3 F ₁₆	00 ₁₆
(42) Processor status register	(P S)	X X X X X 1 X X
(43) Program counter	(P C H)	Contents of address FFFD ₁₆
	(P C L)	Contents of address FFFC ₁₆

Note : The contents of all other registers and RAM are undefined after reset, so they must be initialized by software.
X : Undefined

Fig. 37 Internal state of microcomputer immediately after re-set

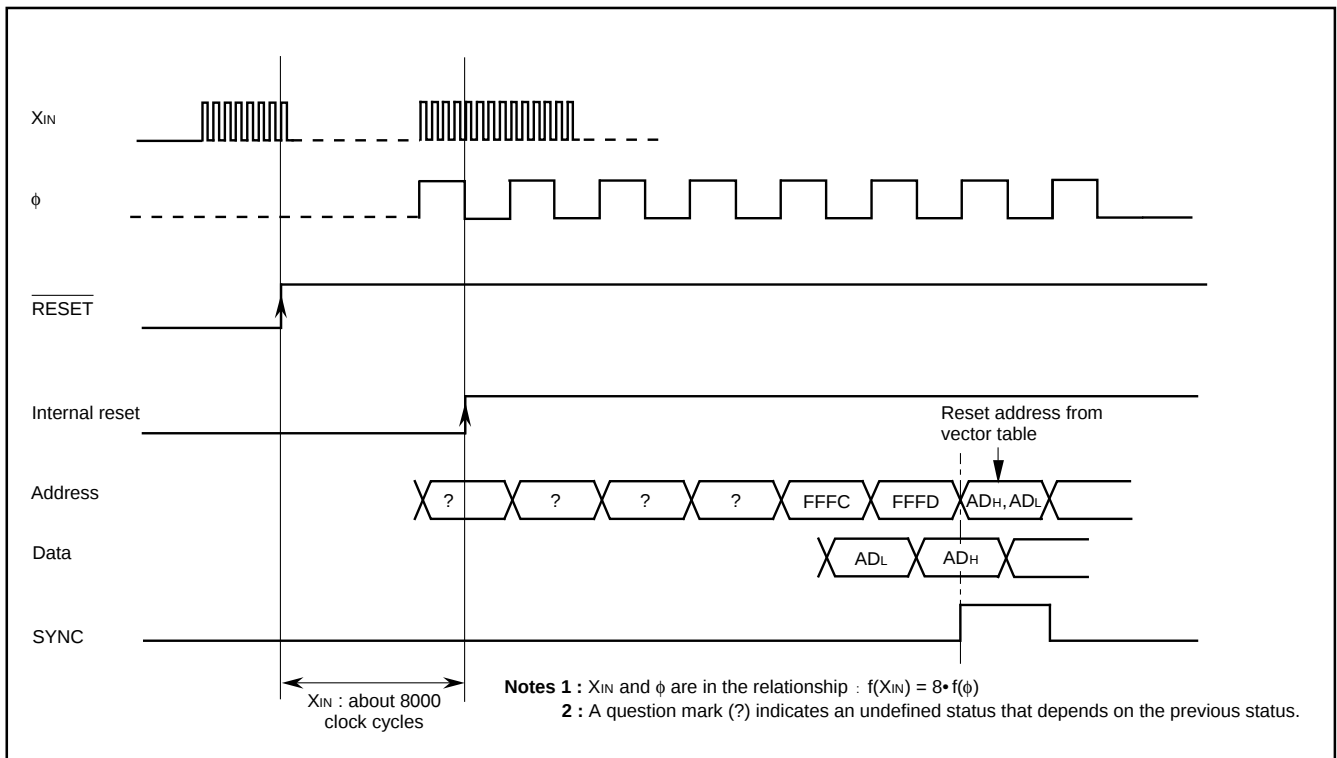


Fig. 38 Reset sequence

CLOCK GENERATING CIRCUIT

The 3825 group has two built-in oscillation circuits. An oscillation circuit can be formed by connecting a resonator between X_{IN} and X_{OUT} (X_{CIN} and X_{COUT}). Use the circuit constants in accordance with the resonator manufacturer's recommended values. No external resistor is needed between X_{IN} and X_{OUT} since a feed-back resistor exists on-chip. However, an external feed-back resistor is needed between X_{CIN} and X_{COUT} .

To supply a clock signal externally, input it to the X_{IN} pin and make the X_{OUT} pin open. The sub-clock X_{CIN} - X_{COUT} oscillation circuit cannot directly input clocks that are externally generated. Accordingly, be sure to cause an external resonator to oscillate.

Immediately after power-on, only the X_{IN} oscillation circuit starts oscillating, and X_{CIN} and X_{COUT} pins function as I/O ports. The pull-up resistor of X_{CIN} and X_{COUT} pins must be made invalid to use the sub-clock.

Frequency Control

(1) Middle-speed mode

The internal clock ϕ is the frequency of X_{IN} divided by 8. After reset, this mode is selected.

(2) High-speed mode

The internal clock ϕ is half the frequency of X_{IN} .

(3) Low-speed mode

- The internal clock ϕ is half the frequency of X_{CIN} .
 - A low-power consumption operation can be realized by stopping the main clock X_{IN} in this mode. To stop the main clock, set bit 5 of the CPU mode register to "1".
- When the main clock X_{IN} is restarted, set enough time for oscillation to stabilize by programming.

Note: If you switch the mode between middle/high-speed and low-speed, stabilize both X_{IN} and X_{CIN} oscillations. The sufficient time is required for the sub-clock to stabilize, especially immediately after power-on and at returning from stop mode. When switching the mode between middle/high-speed and low-speed, set the frequency in the condition that $f(X_{IN}) > 3 \cdot f(X_{CIN})$.

Oscillation Control

(1) Stop mode

If the STP instruction is executed, the internal clock ϕ stops at an "H" level, and X_{IN} and X_{CIN} oscillators stop. Timer 1 is set to "FF16" and timer 2 is set to "0116".

Either X_{IN} or X_{CIN} divided by 16 is input to timer 1 as count source, and the output of timer 1 is connected to timer 2.

The bits of the timer 123 mode register except bit 4 are cleared to "0". Set the timer 1 and timer 2 interrupt enable bits to disabled ("0") before executing the STP instruction.

Oscillator restarts at reset or when an external interrupt is received, but the internal clock ϕ is not supplied to the CPU until timer 2 underflows. This allows time for the clock circuit oscillation to stabilize.

(2) Wait mode

If the WIT instruction is executed, the internal clock ϕ stops at an "H" level. The states of X_{IN} and X_{CIN} are the same as the state before the executing the WIT instruction. The internal clock restarts at reset or when an interrupt is received. Since the oscillator does not stop, normal operation can be started immediately after the clock is restarted.

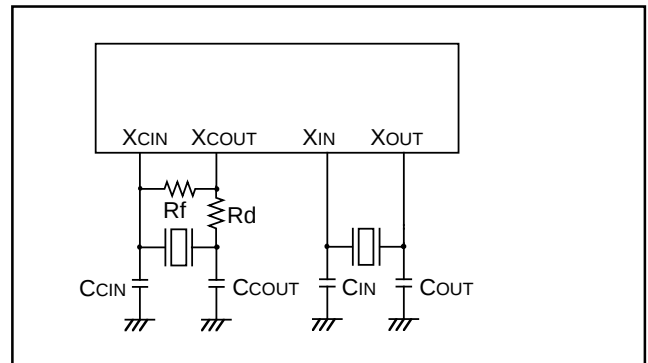


Fig. 39 Ceramic resonator circuit

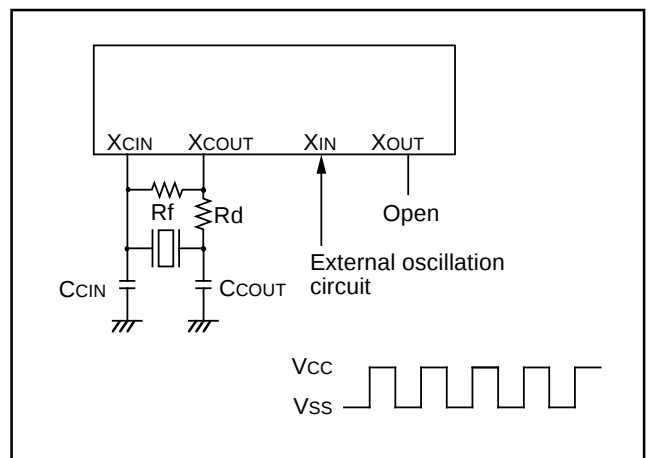


Fig. 40 External clock input circuit

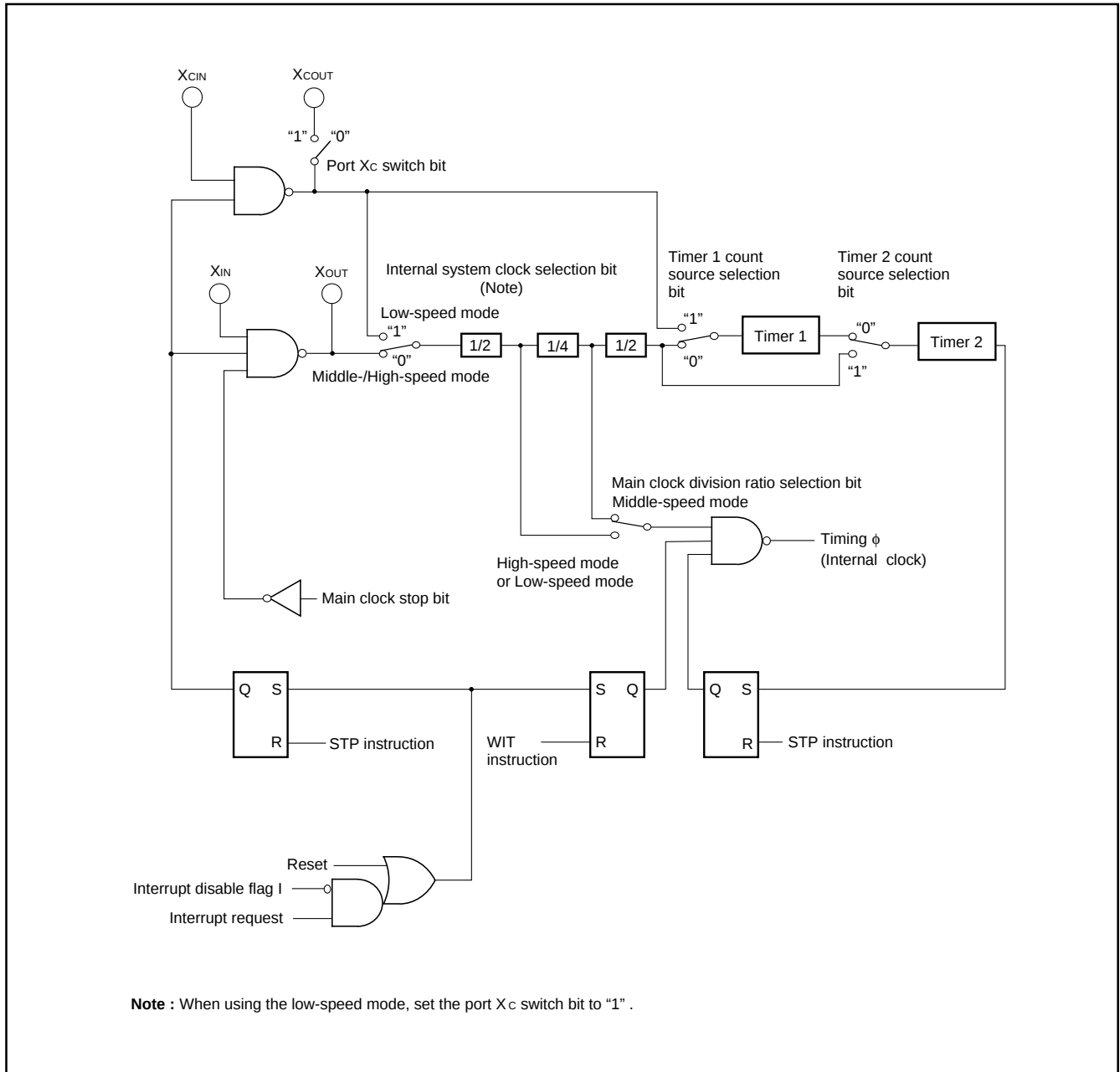
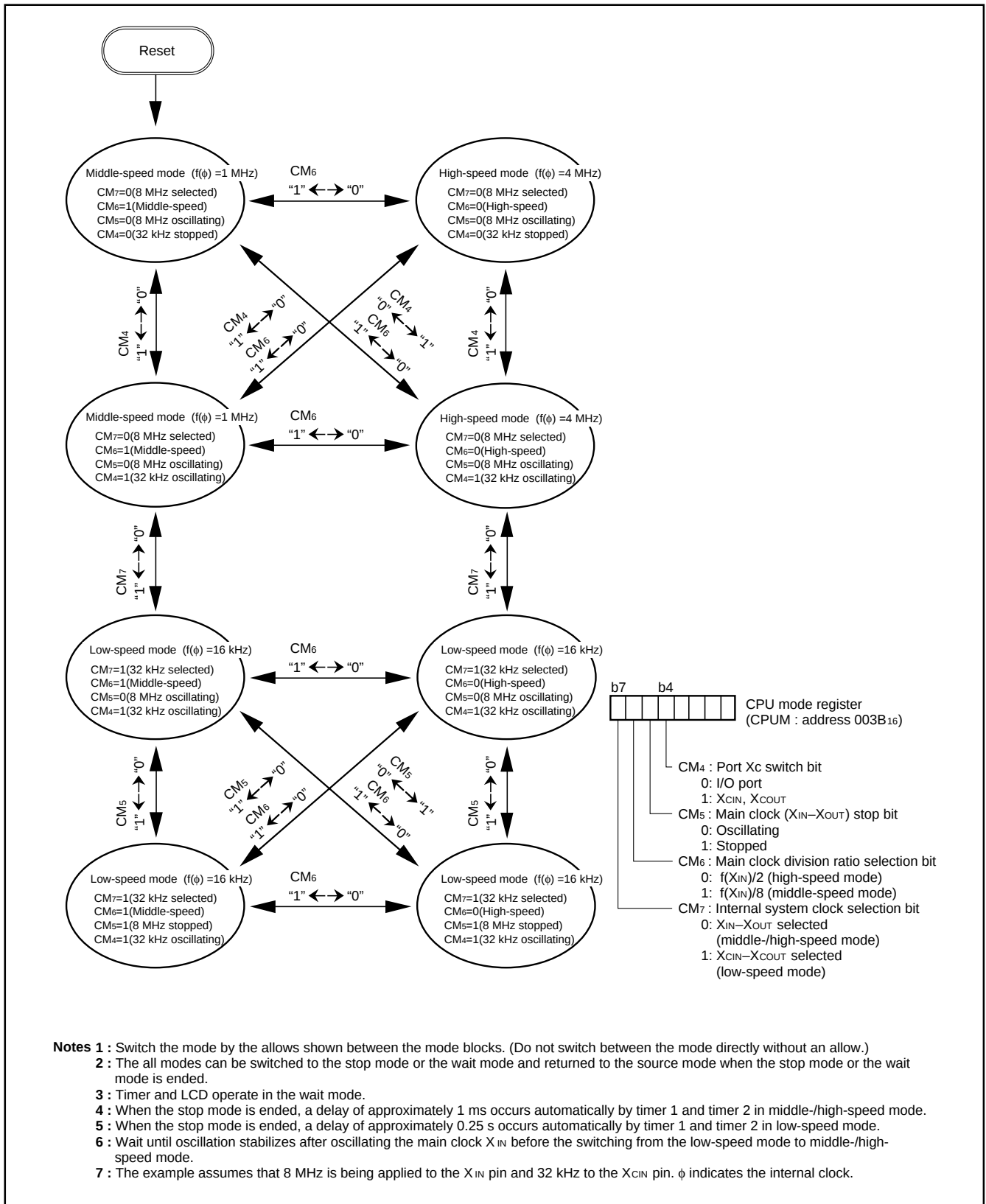


Fig. 41 Clock generating circuit block diagram


Fig. 42 State transitions of internal clock ϕ

NOTES ON PROGRAMMING

Processor Status Register

The contents of the processor status register (PS) after a reset are undefined, except for the interrupt disable flag (I) which is "1". After a reset, initialize flags which affect program execution.

In particular, it is essential to initialize the index X mode (T) and the decimal mode (D) flags because of their effect on calculations.

Interrupt

The contents of the interrupt request bits do not change immediately after they have been written. After writing to an interrupt request register, execute at least one instruction before performing a BBC or BBS instruction.

Decimal Calculations

To calculate in decimal notation, set the decimal mode flag (D) to "1", then execute an ADC or SBC instruction. Only the ADC and SBC instructions yield proper decimal results. After executing an ADC or SBC instruction, execute at least one instruction before executing a SEC, CLC, or CLD instruction.

In decimal mode, the values of the negative (N), overflow (V), and zero (Z) flags are invalid.

The carry flag can be used to indicate whether a carry or borrow has occurred. Initialize the carry flag before each calculation. Clear the carry flag before an ADC and set the flag before an SBC.

Timers

If a value n (between 0 and 255) is written to a timer latch, the frequency division ratio is $1/(n + 1)$.

Multiplication and Division Instructions

The index mode (T) and the decimal mode (D) flags do not affect the MUL and DIV instruction.

The execution of these instructions does not change the contents of the processor status register.

Ports

The contents of the port direction registers cannot be read.

The following cannot be used:

- The data transfer instruction (LDA, etc.)
- The operation instruction when the index X mode flag (T) is "1"
- The addressing mode which uses the value of a direction register as an index
- The bit-test instruction (BBC or BBS, etc.) to a direction register
- The read-modify-write instruction (ROR, CLB, or SEB, etc.) to a direction register

Use instructions such as LDM and STA, etc., to set the port direction registers.

Serial I/O

In clock synchronous serial I/O, if the receive side is using an external clock and it is to output the $\overline{\text{SRDY}}$ signal, set the transmit enable bit, the receive enable bit, and the $\overline{\text{SRDY}}$ output enable bit to "1".

Serial I/O continues to output the final bit from the TxD pin after transmission is completed.

A-D Converter

The comparator uses internal capacitors whose charge will be lost if the clock frequency is too low.

Make sure that $f(\text{XIN})$ is at least 500kHz during an A-D conversion. Do not execute the STP or WIT instruction during an A-D conversion.

Instruction Execution Time

The instruction execution time is obtained by multiplying the frequency of the internal clock ϕ by the number of cycles needed to execute an instruction.

The number of cycles required to execute an instruction is shown in the list of machine instructions.

The frequency of the internal clock ϕ is half of the XIN frequency.

DATA REQUIRED FOR MASK ORDERS

The following are necessary when ordering a mask ROM production:

- 1.Mask ROM Order Confirmation Form
- 2.Mark Specification Form
- 3.Data to be written to ROM, in EPROM form (three identical copies) or one floppy disk

DATA REQUIRED FOR ROM WRITING ORDERS

The following are necessary when ordering a ROM writing:

- 1.ROM Writing Confirmation Form
- 2.Mark Specification Form
- 3.Data to be written to ROM, in EPROM form (three identical copies) or one floppy disk

ROM PROGRAMMING METHOD

The built-in PROM of the blank One Time PROM version and built-in EPROM version can be read or programmed with a general-purpose PROM programmer using a special programming adapter. Set the address of PROM programmer in the user ROM area.

Table 11. Programming adapter

Package	Name of Programming Adapter
100PFB-A	PCA4738H-100A
100P6Q-A	PCA4738G-100A
100P6S-A	PCA4738F-100A
100D0	PCA4738L-100A

The PROM of the blank One Time PROM version is not tested or screened in the assembly process and following processes. To ensure proper operation after programming, the procedure shown in Figure 43 is recommended to verify programming.

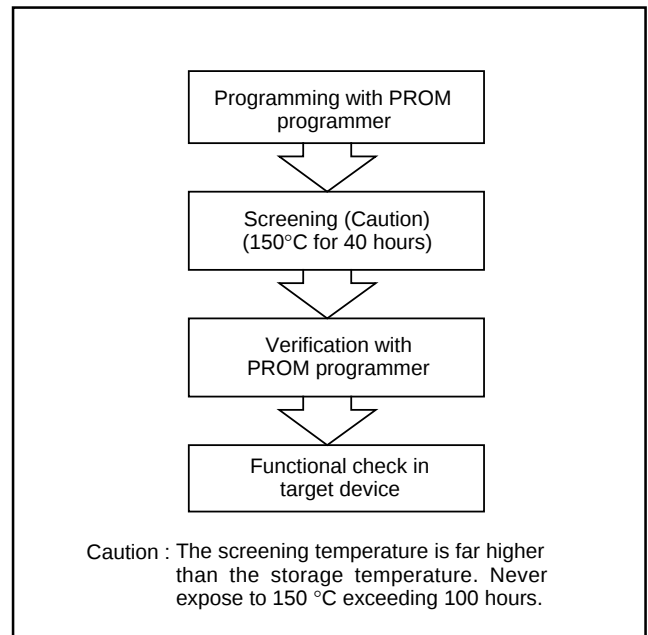


Fig. 43 Programming and testing of One Time PROM version

ELECTRICAL CHARACTERISTICS

Table 12. Absolute maximum ratings

Symbol	Parameter	Conditions	Ratings	Unit
V _{CC}	Power source voltage	All voltages are based on V _{SS} . Output transistors are cut off.	−0.3 to 7.0	V
V _I	Input voltage P16, P17, P20–P27, P40–P47, P50–P57, P60–P67, P80, P81		−0.3 to V _{CC} +0.3	V
V _I	Input voltage P70–P77		−0.3 to V _{CC} +0.3	V
V _I	Input voltage VL1		−0.3 to VL2	V
V _I	Input voltage VL2		VL1 to VL3	V
V _I	Input voltage VL3		VL2 to 7.0	V
V _I	Input voltage C1, C2		−0.3 to 7.0	V
V _I	Input voltage RESET, X _{IN}		−0.3 to V _{CC} +0.3	V
V _O	Output voltage C1, C2		−0.3 to 7.0	V
V _O	Output voltage P00–P07, P10–P15, P30–P37	At output port	−0.3 to V _{CC}	V
		At segment output	−0.3 to VL3	V
V _O	Output voltage P16, P17, P20–P27, P40–P47, P50–P57, P60–P67, P71–P77, P80, P81		−0.3 to V _{CC} +0.3	V
V _O	Output voltage VL3		−0.3 to 7.0	V
V _O	Output voltage VL2, SEG0–SEG17		−0.3 to VL3	V
V _O	Output voltage X _{OUT}		−0.3 to V _{CC} +0.3	V
P _d	Power dissipation	T _a = 25°C	300	mW
T _{opr}	Operating temperature		−20 to 85	°C
T _{stg}	Storage temperature		−40 to 125	°C

Table 13. Recommended operating conditions (V_{CC} = 2.5 to 5.5 V, T_a = −20 to 85°C, unless otherwise noted.)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
V _{CC}	Power source voltage	High-speed mode f(X _{IN}) = 8 MHz	4.0	5.0	5.5	V
		Middle-speed mode f(X _{IN}) = 8 MHz	2.5	5.0	5.5	
		Low-speed mode	2.5	5.0	5.5	
V _{SS}	Power source voltage			0		V
V _{REF}	A-D conversion reference voltage		2.0		V _{CC}	V
AV _{SS}	Analog power source voltage			0		V
V _{IA}	Analog input voltage AN0–AN7		AV _{SS}		V _{CC}	V
V _{IH}	“H” input voltage	P16, P17, P40, P41, P45, P47, P52, P53, P56, P60–P67, P70–P77, P80, P81 (CM4=0)	0.7V _{CC}		V _{CC}	V
V _{IH}	“H” input voltage	P20–P27, P42–P44, P46, P50, P51, P54, P55, P57,	0.8V _{CC}		V _{CC}	V
V _{IH}	“H” input voltage	RESET	0.8V _{CC}		V _{CC}	V
V _{IH}	“H” input voltage	X _{IN}	0.8V _{CC}		V _{CC}	V
V _{IL}	“L” input voltage	P16, P17, P40, P41, P45, P47, P52, P53, P56, P60–P67, P70–P77, P80, P81 (CM4=0)	0		0.3V _{CC}	V
V _{IL}	“L” input voltage	P20–P27, P42–P44, P46, P50, P51, P54, P55, P57	0		0.2V _{CC}	V
V _{IL}	“L” input voltage	RESET	0		0.2V _{CC}	V
V _{IL}	“L” input voltage	X _{IN}	0		0.2V _{CC}	V

Table 14. Recommended operating conditions

(V_{CC} = 2.5 to 5.5 V, T_a = -20 to 85°C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
ΣIOH(peak)	“H” total peak output current	P00–P07, P10–P17, P20–P27, P30–P37 (Note 1)			–20	mA
ΣIOH(peak)	“H” total peak output current	P40–P47,P50–P57, P60–P67, P71–P77, P80, P81 (Note 1)			–20	mA
ΣIOL(peak)	“L” total peak output current	P00–P07, P10–P17, P20–P27, P30–P37 (Note 1)			20	mA
ΣIOL(peak)	“L” total peak output current	P40–P47,P50–P57, P60–P67, P80, P81 (Note 1)			20	mA
ΣIOL(peak)	“L” total peak output current	P71–P77 (Note 1)			40	mA
ΣIOH(avg)	“H” total average output current	P00–P07,P10–P17, P20–P27, P30–P37 (Note 1)			–10	mA
ΣIOH(avg)	“H” total average output current	P40–P47, P50–P57, P60–P67, P71–P77, P80, P81 (Note 1)			–10	mA
ΣIOL(avg)	“L” total average output current	P00–P07, P10–P17, P20–P27, P30–P37 (Note 1)			10	mA
ΣIOL(avg)	“L” total average output current	P40–P47, P50–P57, P60–P67, P80, P81 (Note 1)			10	mA
ΣIOL(avg)	“L” total average output current	P71–P77 (Note 1)			20	mA
IOH(peak)	“H” peak output current	P00–P07, P10–P15, P30–P37 (Note 2)			–0.5	mA
IOH(peak)	“H” peak output current	P16, P17, P20–P27, P40–P47, P50–P57, P60–P67, P71–P77, P80, P81 (Note 2)			–5.0	mA
IOL(peak)	“L” peak output current	P00–P07, P10–P15, P30–P37 (Note 2)			5.0	mA
IOL(peak)	“L” peak output current	P16, P17, P20–P27, P40–P47, P50–P57, P60–P67, P70–P77, P80, P81 (Note 2)			10	mA
IOH(avg)	“H” average output current	P00–P07, P10–P15, P30–P37 (Note 2)			–0.1	mA
IOH(avg)	“H” average output current	P16, P17, P20–P27, P40–P47, P50–P57, P60–P67, P71–P77, P80, P81 (Note 3)			–2.5	mA
IOL(avg)	“L” average output current	P00–P07, P10–P15, P30–P37 (Note 3)			2.5	mA
IOL(avg)	“L” average output current	P16, P17, P20–P27, P40–P47, P50–P57, P60–P67, P71–P77, P80, P81 (Note 3)			5.0	mA
f(CNTR0) f(CNTR1)	Input frequency for timers X and Y (duty cycle 50%)	(4.0 V ≤ VCC ≤ 5.5 V)			4.0	MHz
		(VCC ≤ 4.0 V)			(2×VCC) –4	MHz
f(XIN)	Main clock input oscillation frequency (Note 4)	High-speed mode (4.0 V ≤ VCC ≤ 5.5 V)			8.0	MHz
		High-speed mode (VCC ≤ 4.0 V)			(4×VCC) –8	MHz
		Middle-speed mode			8.0	MHz
f(XCIN)	Sub-clock input oscillation frequency (Note 4, 5)			32.768	50	kHz

Note 1: The total output current is the sum of all the currents flowing through all the applicable ports. The total average current is an average value measured over 100 ms. The total peak current is the peak value of all the currents.

2: The peak output current is the peak current flowing in each port.

3: The average output current is an average value measured over 100 ms.

4: When the oscillation frequency has a duty cycle of 50%.

5: When using the microcomputer in low-speed mode, make sure that the sub-clock input oscillation frequency on condition that f(XCIN) < f(XIN)/3.

Table 15. Electrical characteristics ($V_{CC} = 4.0$ to 5.5 V, $T_a = -20$ to 85°C , unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{OH}	“H” output voltage P00–P07, P10–P15, P30–P37	$I_{OH} = -0.1$ mA	$V_{CC}-2.0$			V
		$I_{OH} = -25$ μA $V_{CC} = 2.5$ V	$V_{CC}-1.0$			V
V_{OH}	“H” output voltage P16, P17, P20–P27, P40–P47, P50–P57, P60–P67, P71–P77, P80, P81 (Note)	$I_{OH} = -5$ mA	$V_{CC}-2.0$			V
		$I_{OH} = -1.25$ mA	$V_{CC}-0.5$			V
		$I_{OH} = -1.25$ mA $V_{CC} = 2.5$ V	$V_{CC}-1.0$			V
V_{OL}	“L” output voltage P00–P07, P10–P15, P30–P37	$I_{OL} = 5$ mA			2.0	V
		$I_{OL} = 1.25$ mA			0.5	V
		$I_{OL} = 1.25$ mA $V_{CC} = 2.5$ V			1.0	V
V_{OL}	“L” output voltage P16, P17, P20–P27, P40–P47, P50–P57, P60–P67, P71–P77, P80, P81 (Note)	$I_{OL} = 10$ mA			2.0	V
		$I_{OL} = 2.5$ mA			0.5	V
		$I_{OL} = 2.5$ mA $V_{CC} = 2.5$ V			1.0	V
$V_{T+} - V_{T-}$	Hysteresis	INT0–INT3, ADT, CNTR0, CNTR1, P20–P27		0.5		V
$V_{T+} - V_{T-}$	Hysteresis	SCLK, RxD		0.5		V
$V_{T+} - V_{T-}$	Hysteresis	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$: $V_{CC}=2.5$ V to 5.5 V		0.5	V
I_{IH}	“H” input current	P16, P17, P20–P27, P40–P47, P50–P57, P60–P67, P70–P77, P80, P81 $V_i = V_{CC}$			5.0	μA
I_{IH}	“H” input current	$\overline{\text{RESET}}$	$V_i = V_{CC}$		5.0	μA
I_{IH}	“H” input current	XIN	$V_i = V_{CC}$	4.0		μA
I_{IL}	“L” input current P16, P17, P20–P27, P40–P47, P50–P57, P60–P67, P71–P77, P80, P81	$V_i = V_{SS}$ Pull-ups “off”			–5.0	μA
		$V_{CC} = 5$ V, $V_i = V_{SS}$ Pull-ups “on”	–30	–70	–140	μA
		$V_{CC} = 3$ V, $V_i = V_{SS}$ Pull-ups “on”	–6.0	–25	–45	μA
I_{IL}	“L” input current	P70			–5.0	μA
I_{IL}	“L” input current	$\overline{\text{RESET}}$	$V_i = V_{SS}$		–5.0	μA
I_{IL}	“L” input current	XIN	$V_i = V_{SS}$	–4.0		μA
I_{LOAD}	Output load current P00–P07, P10–P15, P30–P37	$V_{CC} = 5.0$ V, $V_o = V_{CC}$, Pull-downs “on” Output transistors “off”	30	70	140	μA
		$V_{CC} = 3.0$ V, $V_o = V_{CC}$, Pull-downs “on” Output transistors “off”	6.0	25	45	μA
I_{LEAK}	Output leak current P00–P07, P10–P15, P30–P37	$V_o = V_{CC}$, Pull-downs “off” Output transistors “off”			5.0	μA
		$V_o = V_{SS}$, Pull-downs “off” Output transistors “off”			–5.0	μA

Note: When “1” is set to port Xc switch bit (bit 4 of address 003B16) of CPU mode register, the drive ability of port P80 is different from the value above mentioned.

Table 16. Electrical characteristics

(V_{CC} = 2.5 to 5.5 V, T_a = -20 to 85°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit	
			Min.	Typ.	Max.		
VRAM	RAM retention voltage	At clock stop mode	2.0		5.5	V	
ICC	Power source current	• High-speed mode, Vcc = 5 V f(XIN) = 8 MHz f(XCIN) = 32.768 kHz Output transistors “off” A-D converter in operating		6.4	13	mA	
		• High-speed mode, Vcc = 5 V f(XIN) = 8 MHz (in WIT state) f(XCIN) = 32.768 kHz Output transistors “off” A-D converter in operating		1.6	3.2	mA	
		• Low-speed mode, Vcc = 5 V, Ta ≤ 55°C f(XIN) = stopped f(XCIN) = 32.768 kHz Output transistors “off”		25	36	μA	
		• Low-speed mode, Vcc = 5 V, Ta = 25°C f(XIN) = stopped f(XCIN) = 32.768 kHz (in WIT state) Output transistors “off”		7.0	14	μA	
		• Low-speed mode, Vcc = 3 V, Ta ≤ 55°C f(XIN) = stopped f(XCIN) = 32.768 kHz Output transistors “off”		15	22	μA	
		• Low-speed mode, Vcc = 3 V, Ta ≤ 25°C f(XIN) = stopped f(XCIN) = 32.768 kHz (in WIT state) Output transistors “off”		4.5	9.0	μA	
		All oscillation stopped (in STP state) Output transistors “off”	Ta = 25 °C		0.1	1.0	μA
			Ta = 85 °C			10	
VL1	Power source voltage	When using voltage multiplier	1.3	1.8	2.3	V	
IL1	Power source current (VL1) (Note)	VL1 = 1.8 V		3.0	6.0	μA	
		VL1 < 1.3 V		10	50		

Note : When the voltage multiplier control bit of the LCD mode register (bit 4 at address 003916) is "1".

Table 17. A-D converter characteristics

(VCC = 4.0 to 5.5 V, VSS = 0 V, Ta = -20 to 85°C, 4 MHz ≤ f(XIN) ≤ 8 MHz, in middle-/high-speed mode, unless otherwise noted.)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution				8	Bits
—	Absolute accuracy (excluding quantization error)	VCC = VREF = 5 V			±2	LSB
tCONV	Conversion time	f(XIN) = 8 MHz		12.5 (Note)		μs
RLADDER	Ladder resistor		12	35	100	kΩ
IVREF	Reference input current	VREF = 5 V	50	150	200	μA
IIA	Analog port input current				5.0	μA

Note : When an internal trigger is used in middle-speed mode, it is 14 μs.

Table 18. Timing requirements 1 ($V_{CC} = 4.0$ to 5.5 V, $V_{SS} = 0$ V, $T_a = -20$ to 85°C , unless otherwise noted.)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_w(\text{RESET})$	Reset input "L" pulse width	2			μs
$t_c(X_{IN})$	Main clock input cycle time (X_{IN} input)	125			ns
$t_{wH}(X_{IN})$	Main clock input "H" pulse width	45			ns
$t_{wL}(X_{IN})$	Main clock input "L" pulse width	40			ns
$t_c(\text{CNTR})$	CNTR0, CNTR1 input cycle time	250			ns
$t_{wH}(\text{CNTR})$	CNTR0, CNTR1 input "H" pulse width	105			ns
$t_{wL}(\text{CNTR})$	CNTR0, CNTR1 input "L" pulse width	105			ns
$t_{wH}(\text{INT})$	INT0 to INT3 input "H" pulse width	80			ns
$t_{wL}(\text{INT})$	INT0 to INT3 input "L" pulse width	80			ns
$t_c(\text{SCLK})$	Serial I/O clock input cycle time (Note)	800			ns
$t_{wH}(\text{SCLK})$	Serial I/O clock input "H" pulse width (Note)	370			ns
$t_{wL}(\text{SCLK})$	Serial I/O clock input "L" pulse width (Note)	370			ns
$t_{su}(\text{RxD-SCLK})$	Serial I/O input set up time	220			ns
$t_h(\text{SCLK-RxD})$	Serial I/O input hold time	100			ns

Note : When $f(X_{IN}) = 8$ MHz and bit 6 of address 001A16 is "1" (Clock synchronous).

Divide this value by four when $f(X_{IN}) = 8$ MHz and bit 6 of address 001A16 is "0" (UART).

Table 19. Timing requirements 2 ($V_{CC} = 2.5$ to 4.0 V, $V_{SS} = 0$ V, $T_a = -20$ to 85°C , unless otherwise noted.)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_w(\text{RESET})$	Reset input "L" pulse width	2			μs
$t_c(X_{IN})$	Main clock input cycle time (X_{IN} input)	125			ns
$t_{wH}(X_{IN})$	Main clock input "H" pulse width	45			ns
$t_{wL}(X_{IN})$	Main clock input "L" pulse width	40			ns
$t_c(\text{CNTR})$	CNTR0, CNTR1 input cycle time	500/ ($V_{CC}-2$)			ns
$t_{wH}(\text{CNTR})$	CNTR0, CNTR1 input "H" pulse width	250/ ($V_{CC}-2$)-20			ns
$t_{wL}(\text{CNTR})$	CNTR0, CNTR1 input "L" pulse width	250/ ($V_{CC}-2$)-20			ns
$t_{wH}(\text{INT})$	INT0 to INT3 input "H" pulse width	230			ns
$t_{wL}(\text{INT})$	INT0 to INT3 input "L" pulse width	230			ns
$t_c(\text{SCLK})$	Serial I/O clock input cycle time (Note)	2000			ns
$t_{wH}(\text{SCLK})$	Serial I/O clock input "H" pulse width (Note)	950			ns
$t_{wL}(\text{SCLK})$	Serial I/O clock input "L" pulse width (Note)	950			ns
$t_{su}(\text{RxD-SCLK})$	Serial I/O input set up time	400			ns
$t_h(\text{SCLK-RxD})$	Serial I/O input hold time	200			ns

Note: When $f(X_{IN}) = 8$ MHz and bit 6 of address 001A16 is "1" (Clock synchronous).

Divide this value by four when $f(X_{IN}) = 8$ MHz and bit 6 of address 001A16 is "0" (UART).

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Table 20. Switching characteristics 1 ($V_{CC} = 4.0$ to 5.5 V, $V_{SS} = 0$ V, $T_a = -20$ to 85°C , unless otherwise noted.)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{WH}(\text{SCLK})$	Serial I/O clock output "H" pulse width	$t_c(\text{SCLK})/2-30$			ns
$t_{WL}(\text{SCLK})$	Serial I/O clock output "L" pulse width	$t_c(\text{SCLK})/2-30$			ns
$t_d(\text{SCLK-TxD})$	Serial I/O output delay time (Note 1)			140	ns
$t_v(\text{SCLK-TxD})$	Serial I/O output valid time (Note 1)	-30			ns
$t_r(\text{SCLK})$	Serial I/O clock output rising time			30	ns
$t_f(\text{SCLK})$	Serial I/O clock output falling time			30	ns
$t_r(\text{CMOS})$	CMOS output rising time (Note 2)		10	30	ns
$t_f(\text{CMOS})$	CMOS output falling time (Note 2)		10	30	ns

Notes 1 : When the P45/TxD P-channel output disable bit of the UART control register (bit 4 of address 001B16) is "0".

2 : XOUT and Xcout pins are excluded.

Table 21. Switching characteristics 2 ($V_{CC} = 2.5$ to 4.0 V, $V_{SS} = 0$ V, $T_a = -20$ to 85°C , unless otherwise noted.)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{WH}(\text{SCLK})$	Serial I/O clock output "H" pulse width	$t_c(\text{SCLK})/2-50$			ns
$t_{WL}(\text{SCLK})$	Serial I/O clock output "L" pulse width	$t_c(\text{SCLK})/2-50$			ns
$t_d(\text{SCLK-TxD})$	Serial I/O output delay time (Note 1)			350	ns
$t_v(\text{SCLK-TxD})$	Serial I/O output valid time (Note 1)	-30			ns
$t_r(\text{SCLK})$	Serial I/O clock output rising time			50	ns
$t_f(\text{SCLK})$	Serial I/O clock output falling time			50	ns
$t_r(\text{CMOS})$	CMOS output rising time (Note 2)		20	50	ns
$t_f(\text{CMOS})$	CMOS output falling time (Note 2)		20	50	ns

Notes 1 : When the P45/TxD P-channel output disable bit of the UART control register (bit 4 of address 001B16) is "0".

2 : XOUT and Xcout pins are excluded.

ELECTRICAL CHARACTERISTICS (Extended Operating Temperature Version)

Table 22. Absolute maximum ratings (Extended operating temperature version)

Symbol	Parameter	Conditions	Ratings	Unit
V _{CC}	Power source voltage	All voltages are based on V _{SS} . Output transistors are cut off.	−0.3 to 7.0	V
V _I	Input voltage P16, P17, P20–P27, P40–P47, P50–P57, P60–P67, P80, P81		−0.3 to V _{CC} +0.3	V
V _I	Input voltage P70–P77		−0.3 to V _{CC} +0.3	V
V _I	Input voltage V _{L1}		−0.3 to V _{L2}	V
V _I	Input voltage V _{L2}		V _{L1} to V _{L3}	V
V _I	Input voltage V _{L3}		V _{L2} to 7.0	V
V _I	Input voltage C1, C2		−0.3 to 7.0	V
V _I	Input voltage RESET, X _{IN}		−0.3 to V _{CC} +0.3	V
V _O	Output voltage C1, C2		−0.3 to 7.0	V
V _O	Output voltage P00–P07, P10–P15, P30–P37	At output port	−0.3 to V _{CC}	V
		At segment output	−0.3 to V _{L3}	V
V _O	Output voltage P16, P17, P20–P27, P40–P47, P50–P57, P60–P67, P71–P77 P80, P81		−0.3 to V _{CC} +0.3	V
V _O	Output voltage V _{L3}		−0.3 to 7.0	V
V _O	Output voltage V _{L2} , SEG0–SEG17		−0.3 to V _{L3}	V
V _O	Output voltage X _{OUT}		−0.3 to V _{CC} +0.3	V
P _d	Power dissipation	T _a = 25°C	300	mW
T _{opr}	Operating temperature		−40 to 85	°C
T _{stg}	Storage temperature		−65 to 150	°C

Table 23. Recommended operating conditions (Extended operating temperature version)

(V_{CC} = 2.5 to 5.5 V, T_a = −20 to 85°C, and V_{CC} = 3.0 to 5.5 V, T_a = −40 to −20°C, unless otherwise noted.)

Symbol	Parameter			Limits			Unit
				Min.	Typ.	Max.	
VCC	Power source voltage	High-speed mode f(XIN)=8 MHz		4.0	5.0	5.5	
		Middle-speed mode f(XIN) = 8 MHz	Ta = −20 to 85°C	2.5	5.0	5.5	
			Ta = −40 to −20°C	3.0	5.0	5.5	
		Low-speed mode	Ta = −20 to 85°C	2.5	5.0	5.5	
			Ta = −40 to −20°C	3.0	5.0	5.5	
VSS	Power source voltage				0		V
VREF	A-D conversion reference voltage			2.0		VCC	V
AVSS	Analog power source voltage				0		V
VIA	Analog input voltage	AN0–AN7		AVSS		VCC	V
VIH	“H” input voltage	P16, P17, P40, P41, P45, P47, P52, P53, P56, P60–P67, P70–P77, P80, P81 (CM4=0)		0.7VCC		VCC	V
VIH	“H” input voltage	P20–P27, P42–P44, P46, P50, P51, P54, P55, P57		0.8VCC		VCC	V
VIH	“H” input voltage	RESET		0.8VCC		VCC	V
VIH	“H” input voltage	XIN		0.8VCC		VCC	V
VIL	“L” input voltage	P16, P17, P40, P41, P45, P47, P52, P53, P56, P60–P67, P70–P77, P80, P81 (CM4=0)		0		0.3VCC	V
VIL	“L” input voltage	P20–P27, P42–P44, P46, P50, P51, P54, P55, P57		0		0.2VCC	V
VIL	“L” input voltage	RESET		0		0.2VCC	V
VIL	“L” input voltage	XIN		0		0.2VCC	V

Table 24. Recommended operating conditions (Extended operating temperature version)

(V_{CC} = 2.5 to 5.5 V, T_a = –20 to 85°C, and V_{CC} = 3.0 to 5.5 V, T_a = –40 to –20°C, unless otherwise noted.)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
ΣIOH(peak)	“H” total peak output current P00–P07, P10–P17, P20–P27, P30–P37 (Note 1)			–20	mA
ΣIOH(peak)	“H” total peak output current P40–P47, P50–P57, P60–P67, P71–P77, P80, P81 (Note 1)			–20	mA
ΣIOL(peak)	“L” total peak output current P00–P07, P10–P17, P20–P27, P30–P37 (Note 1)			20	mA
ΣIOL(peak)	“L” total peak output current P40–P47, P50–P57, P60–P67, P80, P81 (Note 1)			20	mA
ΣIOL(peak)	“L” total peak output current P71–P77 (Note 1)			40	mA
ΣIOH(avg)	“H” total average output current P00–P07, P10–P17, P20–P27, P30–P37 (Note 1)			–10	mA
ΣIOH(avg)	“H” total average output current P40–P47, P50–P57, P60–P67, P70–P71, P80, P81 (Note 1)			–10	mA
ΣIOL(avg)	“L” total average output current P00–P07, P10–P17, P20–P27, P30–P37 (Note 1)			10	mA
ΣIOL(avg)	“L” total average output current P40–P47, P50–P57, P60–P67, P80, P81 (Note 1)			10	mA
ΣIOL(avg)	“L” total average output current P71–P77 (Note 1)			20	mA
IOH(peak)	“H” peak output current P00–P07, P10–P15, P30–P37 (Note 2)			–0.5	mA
IOH(peak)	“H” peak output current P16, P17, P20–P27, P40–P47, P50–P57, P60–P67, P71–P77, P80, P81 (Note 2)			–5.0	mA
IOL(peak)	“L” peak output current P00–P07, P10–P15, P30–P37 (Note 2)			5.0	mA
IOL(peak)	“L” peak output current P16, P17, P20–P27, P40–P47, P50–P57, P60–P67, P71–P77, P80, P81 (Note 2)			10	mA
IOH(avg)	“H” average output current P00–P07, P10–P15, P30–P37 (Note 3)			–0.1	mA
IOH(avg)	“H” average output current P16, P17, P20–P27, P40–P47, P50–P57, P60–P67, P71–P77, P80, P81 (Note 3)			–2.5	mA
IOL(avg)	“H” average output current P00–P07, P10–P15, P30–P37 (Note 3)			2.5	mA
IOL(avg)	“H” average output current P16, P17, P20–P27, P40–P47, P50–P57, P60–P67, P71–P77, P80, P81 (Note 3)			5.0	mA
f(CNTR0) f(CNTR1)	Input frequency for timers X and Y (duty cycle 50%)	(4.0 V ≤ V _{CC} ≤ 5.5 V)		4.0	MHz
		(V _{CC} ≤ 4.0 V)		(2×V _{CC})–4	MHz
f(XIN)	Main clock input oscillation frequency (Note 4)	High-speed mode (4.0 V ≤ V _{CC} ≤ 5.5 V)		8.0	MHz
		High-speed mode (V _{CC} ≤ 4.0 V)		(4×V _{CC})–8	MHz
		Middle-speed mode		8.0	MHz
f(XCIN)	Sub-clock input oscillation frequency (Note 4, 5)		32.768	50	kHz

Notes 1 : The total output current is the sum of all the currents flowing through all the applicable ports. The total average current is an average value measured over 100 ms. The total peak current is the peak value of all the currents.

2 : The peak output current is the peak current flowing in each port.

3 : The average output current is an average value measured over 100 ms.

4 : When the oscillation frequency has a duty cycle of 50%.

5 : When using the microcomputer in low-speed mode, make sure that the sub-clock input oscillation frequency on condition that f(XCIN) < f(XIN)/3.

Table 25. Electrical characteristics (Extended operating temperature version) (1)(V_{CC} = 2.5 to 5.5 V, T_a = –20 to 85°C, and V_{CC} = 3.0 to 5.5V, T_a = –40 to –20°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V _{OH}	“H” output voltage P00–P07, P10–P15, P30–P37	I _{OH} = –2.5 mA	V _{CC} –2.0			V
		I _{OH} = –0.6 mA	V _{CC} –0.9			V
		V _{CC} = 3.0 V				
V _{OH}	“H” output voltage P16, P17, P20–P27, P40–P47, P50–P57, P60–P67, P71–P77, P80, P81 (Note)	I _{OH} = –5 mA	V _{CC} –2.0			V
		I _{OH} = –1.25 mA	V _{CC} –0.5			V
		I _{OH} = –1.25 mA V _{CC} = 3.0 V	V _{CC} –0.9			V
V _{OL}	“L” output voltage P00–P07, P10–P15, P30–P37	I _{OL} = 5 mA			2.0	V
		I _{OL} = 1.25 mA			0.5	V
		I _{OL} = 1.25 mA V _{CC} = 3.0 V			1.1	V
V _{OL}	“L” output voltage P16, P17, P20–P27, P40–P47, P50–P57, P60–P67, P71–P77, P80, P81 (Note)	I _{OL} = 10 mA			2.0	V
		I _{OL} = 2.5 mA			0.5	V
		I _{OL} = 2.5 mA V _{CC} = 3.0 V			1.1	V
V _{T+} – V _{T–}	Hysteresis	INT0–INT3, ADT, CNTR0, CNTR1, P20–P27		0.5		V
V _{T+} – V _{T–}	Hysteresis	SCLK, RxD		0.5		V
V _{T+} – V _{T–}	Hysteresis	RESET	RESET: V _{CC} =2.5 V to 5.5 V	0.5		V
I _{IH}	“H” input current	P16, P17, P20–P27, P40–P47, P50–P57, P60–P67, P70–P77, P80, P81	V _I = V _{CC}		5.0	μA
I _{IH}	“H” input current	RESET	V _I = V _{CC}		5.0	μA
I _{IH}	“H” input current	XIN	V _I = V _{CC}	4.0		μA
I _{IL}	“L” input current P16, P17, P20–P27, P40–P47, P50–P57, P60–P67, P71–P77, P80, P81	V _I = V _{SS} Pull-ups “off”			–5.0	μA
		V _{CC} = 5 V, V _I = V _{SS} Pull-ups “on”	–30	–70	–140	μA
		V _{CC} = 3 V, V _I = V _{SS} Pull-ups “on”	–6.0	–25	–45	μA
I _{IL}	“L” input current	P70			–5.0	μA
I _{IL}	“L” input current	RESET	V _I = V _{SS}		–5.0	μA
I _{IL}	“L” input current	XIN	V _I = V _{SS}	–4.0		μA
I _{LOAD}	Output load current P00–P07, P10–P15, P30–P37	V _{CC} = 5.0 V, V _O = V _{CC} , Pull-downs “on” Output transistors “off”	30	70	170	μA
		V _{CC} = 3.0 V, V _O = V _{CC} , Pull-downs “on” Output transistors “off”	6.0	25	55	μA
I _{LEAK}	Output leak current P00–P07, P10–P15, P30–P37	V _O = V _{CC} , Pull-downs “off” Output transistors “off”			5.0	μA
		V _O = V _{SS} , Pull-downs “off” Output transistors “off”			–5.0	μA

Note : When “1” is set to port Xc switch bit (bit 4 of address 003B16) of CPU mode register, the drive ability of port P80 is different from the value above mentioned.

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Table 26. Electrical characteristics (Extended operating temperature version)(V_{CC} = 2.5 to 5.5 V, T_a = –20 to 85°C, and V_{CC} = 3.0 to 5.5 V, T_a = –40 to –20°C, unless otherwise noted.)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
VRAM	RAM retention voltage	At clock stop mode	2.0		5.5	V
I _{CC}	Power source current	• High-speed mode, V _{CC} = 5 V f(X _{IN}) = 8 MHz f(X _{CIN}) = 32.768 kHz Output transistors "off" A-D converter in operating		6.4	13	mA
		• High-speed mode, V _{CC} = 5 V f(X _{IN}) = 8 MHz (in WIT state) f(X _{CIN}) = 32.768 kHz Output transistors "off" A-D converter in operating		1.6	3.2	mA
		• Low-speed mode, V _{CC} = 5 V, T _a ≤ 55°C f(X _{IN}) = stopped f(X _{CIN}) = 32.768 kHz Output transistors "off"		25	36	μA
		• Low-speed mode, V _{CC} = 5 V, T _a = 25°C f(X _{IN}) = stopped f(X _{CIN}) = 32.768 kHz (in WIT state) Output transistors "off"		7.0	14	μA
		• Low-speed mode, V _{CC} = 3 V, T _a ≤ 55°C f(X _{IN}) = stopped f(X _{CIN}) = 32.768 kHz Output transistors "off"		15	22	μA
		• Low-speed mode, V _{CC} = 3 V, T _a ≤ 25°C f(X _{IN}) = stopped f(X _{CIN}) = 32.768 kHz (in WIT state) Output transistors "off"		4.5	9.0	μA
		All oscillation stopped (in STP state) Output transistors "off"	T _a = 25°C T _a = 85°C	0.1 10	1.0 10	μA
VL1	Power source voltage	When using voltage multiplier	1.3	1.8	2.3	V
IL1	Power source current (VL1) (Note)	V _{L1} = 1.8 V		3.0	6.0	μA
		V _{L1} < 1.3 V		10	50	

Note : When the voltage multiplier control bit of the LCD mode register (bit 4 at address 003916) is "1".**Table 27. A-D converter characteristics (Extended operating temperature version)**(V_{CC} = 4.0 to 5.5 V, V_{SS} = 0 V, T_a = –40 to 85°C, 4 MHz ≤ f(X_{IN}) ≤ 8 MHz, in middle-/high-speed mode, unless otherwise noted.)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
–	Resolution				8	Bits
–	Absolute accuracy (excluding quantization error)	V _{CC} = V _{REF} = 5 V			±2	LSB
t _{CONV}	Conversion time	f(X _{IN}) = 8 MHz		12.5 (Note)		μs
RLADDER	Ladder resistor		12	35	100	kΩ
I _{VREF}	Reference input current	V _{REF} = 5 V	50	150	200	μA
I _{IA}	Analog iinput current				5.0	μA

Note : When an internal trigger is used in middle-speed mode, it is 14 μs.

Table 28. Timing requirements 1 (Extended operating temperature version)

(V_{CC} = 4.0 to 5.5 V, V_{SS} = 0 V, T_a = –40 to 85°C, unless otherwise noted.)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t _w (RESET)	Reset input “L” pulse width	2			μs
t _c (X _{IN})	Main clock input cycle time (X _{IN} input)	125			ns
t _{wH} (X _{IN})	Main clock input “H” pulse width	45			ns
t _{wL} (X _{IN})	Main clock input “L” pulse width	40			ns
t _c (CNTR)	CNTR0, CNTR1 input cycle time	250			ns
t _{wH} (CNTR)	CNTR0, CNTR1 input “H” pulse width	105			ns
t _{wL} (CNTR)	CNTR0, CNTR1 input “L” pulse width	105			ns
t _{wH} (INT)	INT0 to INT3 input “H” pulse width	80			ns
t _{wL} (INT)	INT0 to INT3 input “L” pulse width	80			ns
t _c (SCLK)	Serial I/O clock input cycle time (Note)	800			ns
t _{wH} (SCLK)	Serial I/O clock input “H” pulse width (Note)	370			ns
t _{wL} (SCLK)	Serial I/O clock input “L” pulse width (Note)	370			ns
t _{su} (RxD–SCLK)	Serial I/O input set up time	220			ns
t _h (SCLK–RxD)	Serial I/O input hold time	100			ns

Note : When f(X_{IN}) = 8 MHz and bit 6 of address 001A₁₆ is “1” (Clock synchronous).

Divide this value by four when f(X_{IN}) = 8 MHz and bit 6 of address 001A₁₆ is “0” (UART).

Table 29. Timing requirements 2 (Extended operating temperature version)

(V_{CC} = 2.5 to 4.0 V, V_{SS} = 0 V, T_a = –20 to 85°C, and V_{CC} = 3.0 to 4.0 V, V_{SS} = 0 V, T_a = –40 to –20°C, unless otherwise noted.)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t _w (RESET)	Reset input “L” pulse width	2			μs
t _c (X _{IN})	Main clock input cycle time (X _{IN} input)	125			ns
t _{wH} (X _{IN})	Main clock input “H” pulse width	45			ns
t _{wL} (X _{IN})	Main clock input “L” pulse width	40			ns
t _c (CNTR)	CNTR0, CNTR1 input cycle time	500/ (V _{CC} –2)			ns
t _{wH} (CNTR)	CNTR0, CNTR1 input “H” pulse width	250/ (V _{CC} –2)–20			ns
t _{wL} (CNTR)	CNTR0, CNTR1 input “L” pulse width	250/ (V _{CC} –2)–20			ns
t _{wH} (INT)	INT0 to INT3 input “H” pulse width	230			ns
t _{wL} (INT)	INT0 to INT3 input “L” pulse width	230			ns
t _c (SCLK)	Serial I/O clock input cycle time (Note)	2000			ns
t _{wH} (SCLK)	Serial I/O clock input “H” pulse width (Note)	950			ns
t _{wL} (SCLK)	Serial I/O clock input “L” pulse width (Note)	950			ns
t _{su} (RxD–SCLK)	Serial I/O input set up time	400			ns
t _h (SCLK–RxD)	Serial I/O input hold time	200			ns

Note: When f(X_{IN}) = 8 MHz and bit 6 of address 001A₁₆ is “1” (Clock synchronous).

Divide this value by four when f(X_{IN}) = 8 MHz and bit 6 of address 001A₁₆ is “0” (UART).

Table 30. Switching characteristics 1 (Extended operating temperature version)

(V_{CC} = 4.0 to 5.5 V, V_{SS} = 0 V, T_a = -40 to 85°C, unless otherwise noted.)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t _{WH} (SCLK)	Serial I/O clock output "H" pulse width	t _c (SCLK)/2-30			ns
t _{WL} (SCLK)	Serial I/O clock output "L" pulse width	t _c (SCLK)/2-30			ns
t _d (SCLK-TxD)	Serial I/O output delay time (Note 1)			140	ns
t _v (SCLK-TxD)	Serial I/O output valid time (Note 1)	-30			ns
t _r (SCLK)	Serial I/O clock output rising time			30	ns
t _f (SCLK)	Serial I/O clock output falling time			30	ns
t _r (CMOS)	CMOS output rising time (Note 2)		10	30	ns
t _f (CMOS)	CMOS output falling time (Note 2)		10	30	ns

Notes 1 : When the P45/TxD P-channel output disable bit of the UART control register (bit 4 of address 001B16) is "0".

2 : XOUT and Xcout pins are excluded.

Table 31. Switching characteristics 2 (Extended operating temperature version)

(V_{CC} = 2.5 to 4.0 V, V_{SS} = 0 V, T_a = -20 to 85°C, and V_{CC} = 3.0 to 4.0 V, V_{SS} = 0 V, T_a = -40 to -20°C, unless otherwise noted.)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t _{WH} (SCLK)	Serial I/O clock output "H" pulse width	t _c (SCLK)/2-50			ns
t _{WL} (SCLK)	Serial I/O clock output "L" pulse width	t _c (SCLK)/2-50			ns
t _d (SCLK-TxD)	Serial I/O output delay time (Note 1)			350	ns
t _v (SCLK-TxD)	Serial I/O output valid time (Note 1)	-30			ns
t _r (SCLK)	Serial I/O clock output rising time			50	ns
t _f (SCLK)	Serial I/O clock output falling time			50	ns
t _r (CMOS)	CMOS output rising time (Note 2)		20	50	ns
t _f (CMOS)	CMOS output falling time (Note 2)		20	50	ns

Notes 1 : When the P45/TxD P-channel output disable bit of the UART control register (bit 4 of address 001B16) is "0".

2 : XOUT and Xcout pins are excluded.

ELECTRICAL CHARACTERISTICS (Low Power Source Version)

Table 32. Absolute maximum ratings (Low power source version)

Symbol	Parameter	Conditions	Ratings	Unit
V _{CC}	Power source voltage	All voltages are based on V _{SS} . Output transistors are cut off.	−0.3 to 7.0	V
V _I	Input voltage P16, P17, P20–P27, P40–P47, P50–P57, P60–P67, P80, P81		−0.3 to V _{CC} +0.3	V
V _I	Input voltage P70–P77		−0.3 to V _{CC} +0.3	V
V _I	Input voltage V _{L1}		−0.3 to V _{L2}	V
V _I	Input voltage V _{L2}		V _{L1} to V _{L3}	V
V _I	Input voltage V _{L3}		V _{L2} to 7.0	V
V _I	Input voltage C1, C2		−0.3 to 7.0	V
V _I	Input voltage RESET, X _{IN}		−0.3 to V _{CC} +0.3	V
V _O	Output voltage C1, C2		−0.3 to 7.0	V
V _O	Output voltage P00–P07, P10–P15, P30–P37	At output port	−0.3 to V _{CC}	V
		At segment output	−0.3 to V _{L3}	V
V _O	Output voltage P16, P17, P20–P27, P40–P47, P50–P57, P60–P67, P71–P77, P80, P81		−0.3 to V _{CC} +0.3	V
V _O	Output voltage V _{L3}		−0.3 to 7.0	V
V _O	Output voltage V _{L2} , SEG0–SEG17		−0.3 to V _{L3}	V
V _O	Output voltage X _{OUT}		−0.3 to V _{CC} +0.3	V
P _d	Power dissipation	T _a = 25°C	300	mW
T _{opr}	Operating temperature		−20 to 85	°C
T _{stg}	Storage temperature		−40 to 125	°C

Table 33. Recommended operating conditions (Low power source version)

(V_{CC} = 2.2 to 5.5 V, T_a = −20 to 85°C, unless otherwise noted.)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
V _{CC}	Power source voltage	High-speed mode, f(X _{IN})=8 MHz	4.0	5.0	5.5	V
		Middle-speed mode, f(X _{IN}) = 8 MHz	2.2	5.0	5.5	
		Low-speed mode	2.2	5.0	5.5	
V _{SS}	Power source voltage			0		V
V _{REF}	A-D conversion reference voltage		2.0		V _{CC}	V
AV _{SS}	Analog power source voltage			0	V _{CC}	V
V _{IA}	Analog input voltage	AN0–AN7	AV _{SS}		V _{CC}	V
V _{IH}	“H” input voltage	P16, P17, P40, P41, P45, P47, P52, P53, P56, P60–P67, P70–P77, P80, P81 (CM4=0)	0.7V _{CC}		V _{CC}	V
V _{IH}	“H” input voltage	P20–P27, P42–P44, P46, P50, P51, P54, P55, P57	0.8V _{CC}		V _{CC}	V
V _{IH}	“H” input voltage	RESET	0.8V _{CC}		V _{CC}	V
V _{IH}	“H” input voltage	X _{IN}	0.8V _{CC}		V _{CC}	V
V _{IL}	“L” input voltage	P16, P17, P40, P41, P45, P47, P52, P53, P56, P60–P67, P70–P77, P80, P81 (CM4=0)	0		0.3V _{CC}	V
V _{IL}	“L” input voltage	P20–P27, P42–P44, P46, P50, P51, P54, P55, P57	0		0.2V _{CC}	V
V _{IL}	“L” input voltage	RESET	0		0.2V _{CC}	V
V _{IL}	“L” input voltage	X _{IN}	0		0.2V _{CC}	V

Table 34. Recommended operating conditions (Low power source version)(V_{CC} = 2.2 to 5.5 V, T_a = -20 to 85°C, unless otherwise noted.)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
ΣIOH(peak)	“H” total peak output current	P00–P07, P10–P17, P20–P27, P30–P37 (Note 1)			–20	mA
ΣIOH(peak)	“H” total peak output current	P40–P47,P50–P57, P60–P67, P71–P77, P80, P81 (Note 1)			–20	mA
ΣIOL(peak)	“L” total peak output current	P00–P07, P10–P17, P20–P27, P30–P37 (Note 1)			20	mA
ΣIOL(peak)	“L” total peak output current	P40–P47,P50–P57, P60–P67, P80, P81 (Note 1)			20	mA
ΣIOL(peak)	“L” total peak output current	P71–P77 (Note 1)			40	mA
ΣIOH(avg)	“H” total average output current	P00–P07, P10–P17, P20–P27, P30–P37 (Note 1)			–10	mA
ΣIOH(avg)	“H” total average output current	P40–P47, P50–P57, P60–P67, P70–P71, P80, P81 (Note 1)			–10	mA
ΣIOL(avg)	“L” total average output current	P00–P07, P10–P17, P20–P27, P30–P37 (Note 1)			10	mA
ΣIOL(avg)	“L” total average output current	P40–P47, P50–P57, P60–P67, P80, P81 (Note 1)			10	mA
ΣIOL(avg)	“L” total average output current	P71–P77 (Note 1)			20	mA
IOH(peak)	“H” peak output current	P00–P07, P10–P15, P30–P37 (Note 2)			–0.5	mA
IOH(peak)	“H” peak output current	P16, P17, P20–P27, P40–P47, P50–P57, P60–P67, P71–P77, P80, P81 (Note 2)			–5.0	mA
IOL(peak)	“L” peak output current	P00–P07, P10–P15, P30–P37 (Note 2)			5.0	mA
IOL(peak)	“L” peak output current	P16, P17, P20–P27, P40–P47, P50–P57, P60–P67, P71–P77, P80, P81 (Note 2)			10	mA
IOH(avg)	“H” average output current	P00–P07, P10–P15, P30–P37 (Note 3)			–0.1	mA
IOH(avg)	“H” average output current	P16, P17, P20–P27, P40–P47, P50–P57, P60–P67, P71–P77, P80, P81 (Note 3)			–2.5	mA
IOL(avg)	“H” average output current	P00–P07, P10–P15, P30–P37 (Note 3)			2.5	mA
IOL(avg)	“H” average output current	P16, P17, P20–P27, P40–P47, P50–P57, P60–P67, P71–P77, P80, P81 (Note 3)			5.0	mA
f(CNTR0) f(CNTR1)	Input frequency for timers X and Y (duty cycle 50%)	(4.0 V ≤ Vcc ≤ 5.5 V)			4.0	MHz
		(2.2 V ≤ Vcc ≤ 4.0 V)			(10 × Vcc – 4) / 9	MHz
f(XIN)	Main clock input oscillation frequency (Note 4)	High-speed mode (4.0 V ≤ Vcc ≤ 5.5 V)			8.0	MHz
		High-speed mode (2.2 V ≤ Vcc ≤ 4.0 V)			(20 × Vcc – 8) / 9	MHz
		Middle-speed mode			8.0	MHz
f(XCIN)	Sub-clock input oscillation frequency (Note 4, 5)			32.768	50	kHz

Notes 1 : The total output current is the sum of all the currents flowing through all the applicable ports. The total average current is an average value measured over 100 ms. The total peak current is the peak value of all the currents.

2 : The peak output current is the peak current flowing in each port.

3 : The average output current is an average value measured over 100 ms.

4 : When the oscillation frequency has a duty cycle of 50%.

5 : When using the microcomputer in low-speed mode, make sure that the sub-clock input oscillation frequency on condition that $f(XCIN) < f(XIN)/3$.

Table 35. Electrical characteristics (Low power source version)(V_{CC} = 2.2 to 5.5 V, T_a = -20 to 85°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V _{OH}	“H” output voltage P00–P07, P10–P15, P30–P37	I _{OH} = -2.5 mA	V _{CC} -2.0			V
		I _{OH} = -0.25 mA	V _{CC} -0.8			V
		V _{CC} = 2.2 V				
V _{OH}	“H” output voltage P16, P17, P20–P27, P40–P47, P50–P57, P60–P67, P71–P77, P80, P81 (Note)	I _{OH} = -5 mA	V _{CC} -2.0			V
		I _{OH} = -1.25 mA	V _{CC} -0.5			V
		I _{OH} = -1.25 mA	V _{CC} -0.8			V
V _{OL}	“L” output voltage P00–P07, P10–P15, P30–P37	I _{OL} = 5 mA			2.0	V
		I _{OL} = 1.25 mA			0.5	V
		I _{OL} = 1.25 mA			0.8	V
V _{OL}	“L” output voltage P16, P17, P20–P27, P40–P47, P50–P57, P60–P67, P71–P77, P80, P81 (Note)	I _{OL} = 10 mA			2.0	V
		I _{OL} = 2.5 mA			0.5	V
		I _{OL} = 2.5 mA			0.8	V
V _{T+} – V _{T-}	Hysteresis	INT0–INT3, ADT, CNTR0, CNTR1, P20–P27		0.5		V
V _{T+} – V _{T-}	Hysteresis	SCLK, RxD		0.5		V
V _{T+} – V _{T-}	Hysteresis	RESET	RESET: V _{CC} =2.2 V to 5.5 V	0.5		V
I _{IH}	“H” input current	P16, P17, P20–P27, P40–P47, P50–P57, P60–P67, P70–P77, P80, P81	V _I = V _{CC}		5.0	μA
I _{IH}	“H” input current	RESET	V _I = V _{CC}		5.0	μA
I _{IH}	“H” input current	XIN	V _I = V _{CC}	4.0		μA
I _{IL}	“L” input current P16, P17, P20–P27, P40–P47, P50–P57, P60–P67, P71–P77, P80, P81	V _I = V _{SS} Pull-ups “off”			-5.0	μA
		V _{CC} = 5 V, V _I = V _{SS} Pull-ups “on”	-30	-70	-140	μA
		V _{CC} = 2.2 V, V _I = V _{SS} Pull-ups “on”	-6.0	-25	-45	μA
I _{IL}	“L” input current	P70			-5.0	μA
I _{IL}	“L” input current	RESET	V _I = V _{SS}		-5.0	μA
I _{IL}	“L” input current	XIN	V _I = V _{SS}	-4.0		μA
I _{LOAD}	Output load current P00–P07, P10–P15, P30–P37	V _{CC} = 5.0 V, V _O = V _{CC} , Pull-downs “on” Output transistors “off”	30	70	140	μA
		V _{CC} = 2.2 V, V _O = V _{CC} , Pull-downs “on” Output transistors “off”	6.0	25	45	μA
I _{LEAK}	Output leak current P00–P07, P10–P15, P30–P37	V _O = V _{CC} , Pull-downs “off” Output transistors “off”			5.0	μA
		V _O = V _{SS} , Pull-downs “off” Output transistors “off”			-5.0	μA

Note : When “1” is set to port Xc switch bit (bit 4 of address 003B16) of CPU mode register, the drive ability of port P80 is different from the value above mentioned.

Table 36. Electrical characteristics (Low power source version)(V_{CC} = 2.2 to 5.5 V, T_a = -20 to 85°C, unless otherwise noted.)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
VRAM	RAM retention voltage	At clock stop mode	2.0		5.5	V
I _{CC}	Power source current	• High-speed mode, V _{CC} = 5 V f(X _{IN}) = 8 MHz f(X _{CIN}) = 32.768 kHz Output transistors "off" A-D converter in operating		6.4	13	mA
		• High-speed mode, V _{CC} = 5 V f(X _{IN}) = 8 MHz (in WIT state) f(X _{CIN}) = 32.768 kHz Output transistors "off" A-D converter in operating		1.6	3.2	mA
		• Low-speed mode, V _{CC} = 5 V, T _a ≤ 55°C f(X _{IN}) = stopped f(X _{CIN}) = 32.768 kHz Output transistors "off"		25	36	μA
		• Low-speed mode, V _{CC} = 5 V, T _a = 25°C f(X _{IN}) = stopped f(X _{CIN}) = 32.768 kHz (in WIT state) Output transistors "off"		7.0	14	μA
		• Low-speed mode, V _{CC} = 3 V, T _a ≤ 55°C f(X _{IN}) = stopped f(X _{CIN}) = 32.768 kHz Output transistors "off"		15	22	μA
		• Low-speed mode, V _{CC} = 3 V, T _a ≤ 25°C f(X _{IN}) = stopped f(X _{CIN}) = 32.768 kHz (in WIT state) Output transistors "off"		4.5	9.0	μA
		All oscillation stopped (in STP state) Output transistors "off"	T _a = 25°C T _a = 85°C	0.1	1.0 10	μA
VL1	Power source voltage	When using voltage multiplier	1.3	1.8	2.3	V
IL1	Power source current (VL1) (Note)	VL1 = 1.8 V		3.0	6.0	μA
		VL1 < 1.3 V		10	50	

Note : When the voltage multiplier control bit of the LCD mode register (bit 4 at address 003916) is "1".**Table 37. A-D converter characteristics (Low power source version)**(V_{CC} = 4.0 to 5.5 V, V_{SS} = 0 V, T_a = -20 to 85°C, 4 MHz ≤ f(X_{IN}) ≤ 8 MHz, in middle-/high-speed mode, unless otherwise noted.)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution				8	Bits
—	Absolute accuracy (excluding quantization error)	V _{CC} = V _{REF} = 5 V			±2	LSB
t _{CONV}	Conversion time	f(X _{IN}) = 8 MHz		12.5 (Note)		μs
RLADDER	Ladder resistor		12	35	100	kΩ
IVREF	Reference input current	V _{REF} = 5 V	50	150	200	μA
I _{IA}	Analog input current				5.0	μA

Note : When an internal trigger is used in middle-speed mode, it is 14 μs.

Table 38. Timing requirements 1 (Low power source Version)

(V_{CC} = 4.0 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 85°C, unless otherwise noted.)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t _w (RESET)	Reset input “L” pulse width	2			μs
t _c (X _{IN})	Main clock input cycle time (X _{IN} input)	125			ns
t _{wH} (X _{IN})	Main clock input “H” pulse width	45			ns
t _{wL} (X _{IN})	Main clock input “L” pulse width	40			ns
t _c (CNTR)	CNTR0, CNTR1 input cycle time	250			ns
t _{wH} (CNTR)	CNTR0, CNTR1 input “H” pulse width	105			ns
t _{wL} (CNTR)	CNTR0, CNTR1 input “L” pulse width	105			ns
t _{wH} (INT)	INT0 to INT3 input “H” pulse width	80			ns
t _{wL} (INT)	INT0 to INT3 input “L” pulse width	80			ns
t _c (SCLK)	Serial I/O clock input cycle time (Note)	800			ns
t _{wH} (SCLK)	Serial I/O clock input “H” pulse width (Note)	370			ns
t _{wL} (SCLK)	Serial I/O clock input “L” pulse width (Note)	370			ns
t _{su} (RxD–SCLK)	Serial I/O input set up time	220			ns
t _h (SCLK–RxD)	Serial I/O input hold time	100			ns

Note : When f(X_{IN}) = 8 MHz and bit 6 of address 001A₁₆ is “1” (Clock synchronous).

Divide this value by four when f(X_{IN}) = 8 MHz and bit 6 of address 001A₁₆ is “0” (UART).

Table 39. Timing requirements 2 (Low power source Version)

(V_{CC} = 2.2 to 4.0 V, V_{SS} = 0 V, T_a = –20 to 85°C, unless otherwise noted.)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t _w (RESET)	Reset input “L” pulse width	2			μs
t _c (X _{IN})	Main clock input cycle time (X _{IN} input)	125			ns
t _{wH} (X _{IN})	Main clock input “H” pulse width	45			ns
t _{wL} (X _{IN})	Main clock input “L” pulse width	40			ns
t _c (CNTR)	CNTR0, CNTR1 input cycle time	900 / (V _{CC} – 0.4)			ns
t _{wH} (CNTR)	CNTR0, CNTR1 input “H” pulse width	450 / (V _{CC} – 0.4) – 20			ns
t _{wL} (CNTR)	CNTR0, CNTR1 input “L” pulse width	450 / (V _{CC} – 0.4) – 20			ns
t _{wH} (INT)	INT0 to INT3 input “H” pulse width	230			ns
t _{wL} (INT)	INT0 to INT3 input “L” pulse width	230			ns
t _c (SCLK)	Serial I/O clock input cycle time (Note)	2000			ns
t _{wH} (SCLK)	Serial I/O clock input “H” pulse width (Note)	950			ns
t _{wL} (SCLK)	Serial I/O clock input “L” pulse width (Note)	950			ns
t _{su} (RxD–SCLK)	Serial I/O input set up time	400			ns
t _h (SCLK–RxD)	Serial I/O input hold time	200			ns

Note: When f(X_{IN}) = 8 MHz and bit 6 of address 001A₁₆ is “1” (Clock synchronous).

Divide this value by four when f(X_{IN}) = 8 MHz and bit 6 of address 001A₁₆ is “0” (UART).

Table 40. Switching characteristics 1 (Low power source version)

(V_{CC} = 4.0 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 85°C, unless otherwise noted.)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t _{wH} (SCLK)	Serial I/O clock output "H" pulse width	t _c (SCLK)/2–30			ns
t _{wL} (SCLK)	Serial I/O clock output "L" pulse width	t _c (SCLK)/2–30			ns
t _d (SCLK–TxD)	Serial I/O output delay time (Note 1)			140	ns
t _v (SCLK–TxD)	Serial I/O output valid time (Note 1)	–30			ns
t _r (SCLK)	Serial I/O clock output rising time			30	ns
t _f (SCLK)	Serial I/O clock output falling time			30	ns
t _r (CMOS)	CMOS output rising time (Note 2)		10	30	ns
t _f (CMOS)	CMOS output falling time (Note 2)		10	30	ns

Notes 1 : When the P45/TxD P-channel output disable bit of the UART control register (bit 4 of address 001B₁₆) is "0".

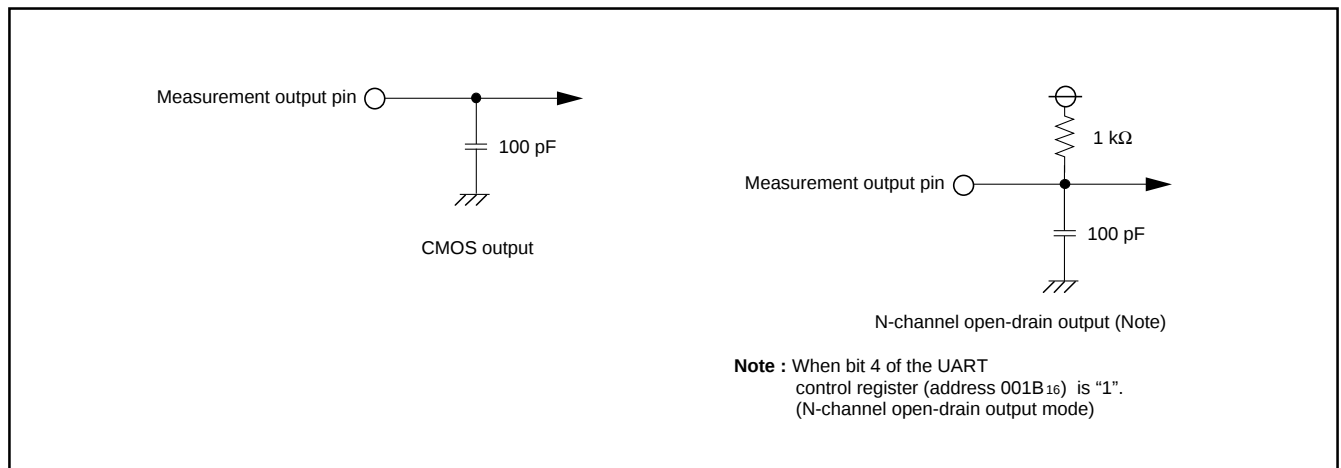
2 : XOUT and Xcout pins are excluded.

Table 41. Switching characteristics 2 (Low power source version)

(V_{CC} = 2.2 to 4.0 V, V_{SS} = 0 V, T_a = –20 to 85°C, unless otherwise noted.)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t _{wH} (SCLK)	Serial I/O clock output "H" pulse width	t _c (SCLK)/2–50			ns
t _{wL} (SCLK)	Serial I/O clock output "L" pulse width	t _c (SCLK)/2–50			ns
t _d (SCLK–TxD)	Serial I/O output delay time (Note 1)			350	ns
t _v (SCLK–TxD)	Serial I/O output valid time (Note 1)	–30			ns
t _r (SCLK)	Serial I/O clock output rising time			50	ns
t _f (SCLK)	Serial I/O clock output falling time			50	ns
t _r (CMOS)	CMOS output rising time (Note 2)		20	50	ns
t _f (CMOS)	CMOS output falling time (Note 2)		20	50	ns

Notes 1 : When the P45/TxD P-channel output disable bit of the UART control register (bit 4 of address 001B₁₆) is "0".

2 : XOUT and Xcout pins are excluded.

Fig. 44 Circuit for measuring output switching characteristics

TIMING DIAGRAM

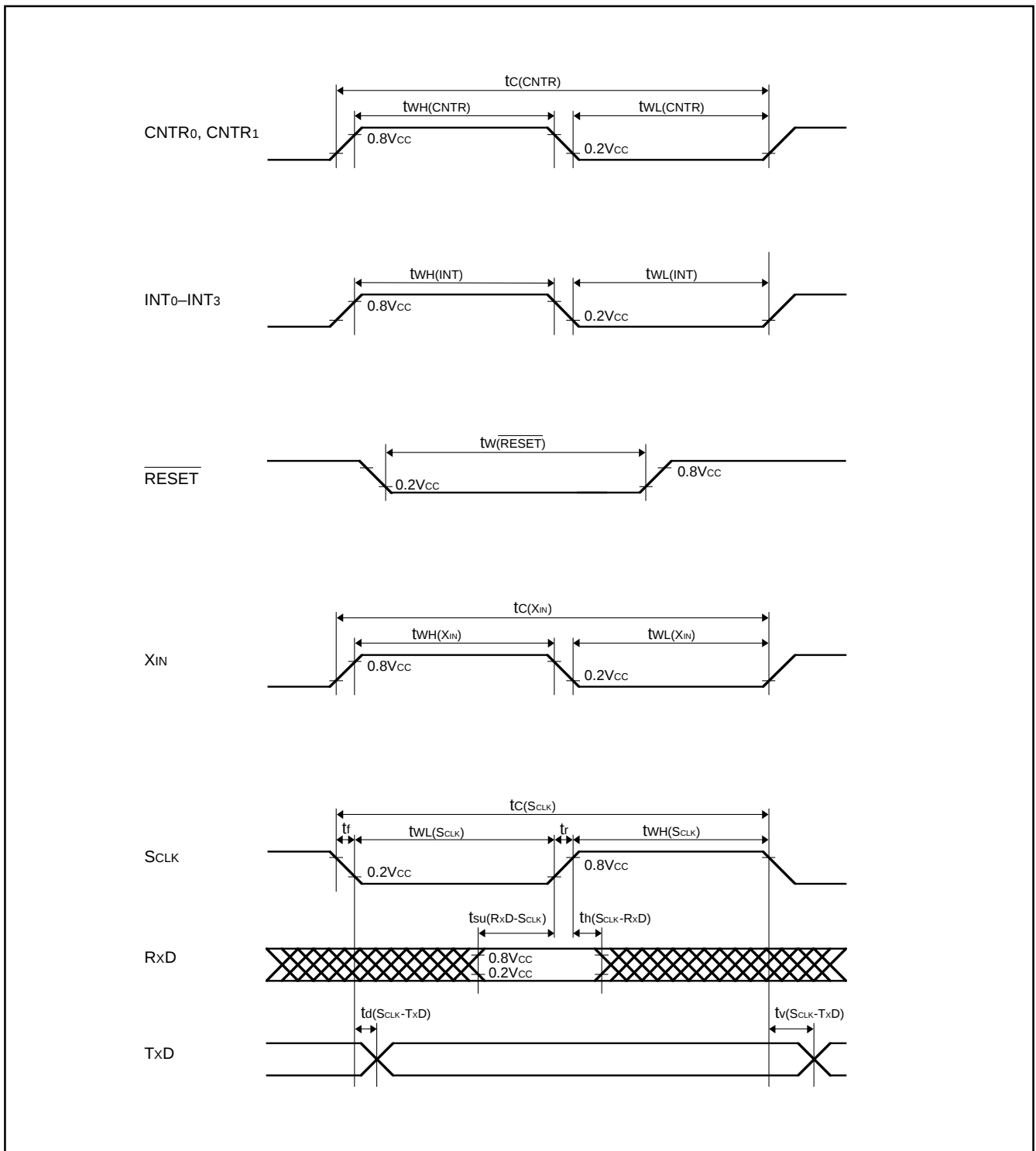


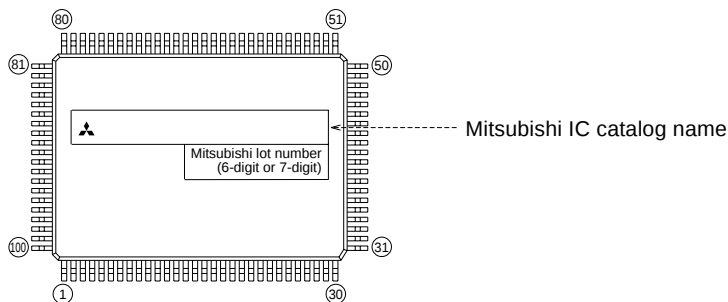
Fig. 45 Timing diagram

MARK SPECIFICATION FORM
100P6S (100-PIN QFP) MARK SPECIFICATION FORM

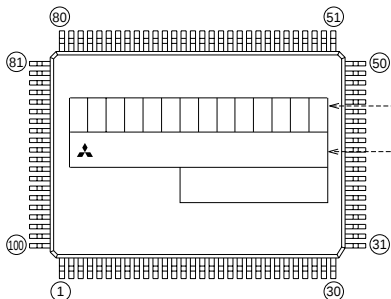
Mitsubishi IC catalog name

Please choose one of the marking types below (A, B, C), and enter the Mitsubishi catalog name and the special mark (if needed).

A. Standard Mitsubishi Mark

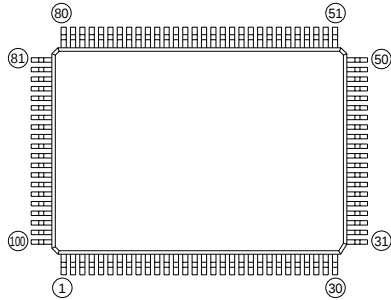


B. Customer's Parts Number + Mitsubishi catalog name



- Customer's Parts Number
Note : The fonts and size of characters are standard Mitsubishi type.
Mitsubishi IC catalog name
Note1 : The mark field should be written right aligned.
2 : The fonts and size of characters are standard Mitsubishi type.
3 : Customer's Parts Number can be up to 14 characters : Only 0 ~ 9, A ~ Z, +, -, /, (,), &, ©, . (periods), , (commas) are usable.
4 : If the Mitsubishi logo  is not required, check the box below.
☐ Mitsubishi logo is not required

C. Special Mark Required



- Note1 : If the Special Mark is to be Printed, indicate the desired layout of the mark in the left figure. The layout will be duplicated as close as possible.
Mitsubishi lot number (6-digit or 7-digit) and Mask ROM number (3-digit) are always marked.
2 : If the customer's trade mark logo must be used in the Special Mark, check the box below.
Please submit a clean original of the logo.
For the new special character fonts a clean font original (ideally logo drawing) must be submitted.

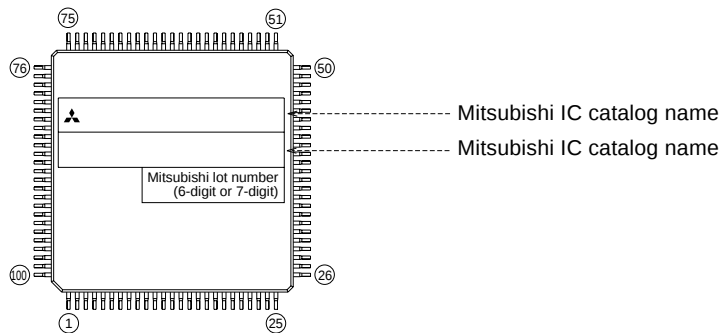
Special logo required
☐

100P6Q (100-PIN LQFP) MARK SPECIFICATION FORM

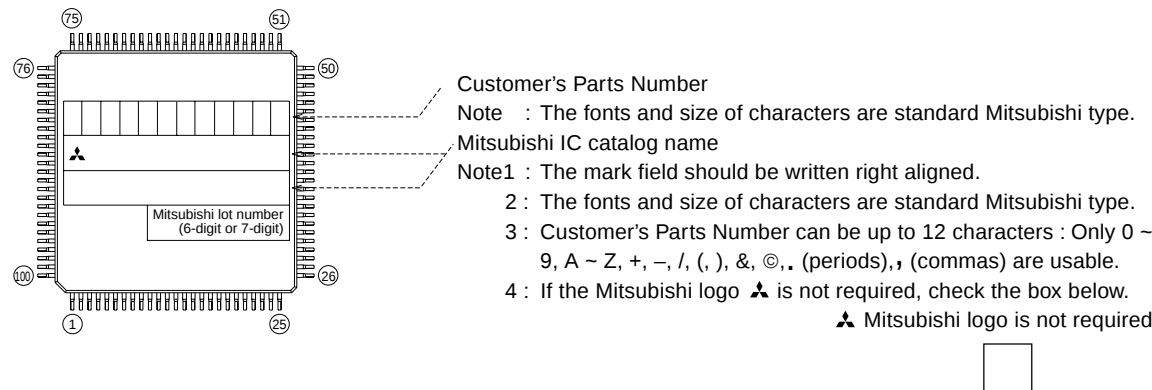
Mitsubishi IC catalog name

Please choose one of the marking types below (A, B, C), and enter the Mitsubishi catalog name and the special mark (if needed).

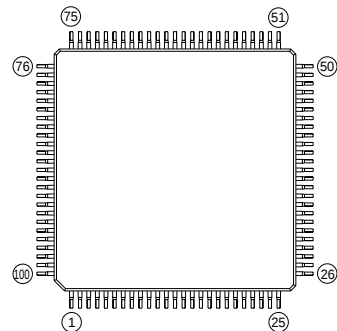
A. Standard Mitsubishi Mark



B. Customer's Parts Number + Mitsubishi catalog name



C. Special Mark Required



Note1 : If the Special Mark is to be Printed, indicate the desired layout of the mark in the left figure. The layout will be duplicated as close as possible.

Mitsubishi lot number (6-digit or 7-digit) and Mask ROM number (3-digit) are always marked.

2 : If the customer's trade mark logo must be used in the Special Mark, check the box below.

Please submit a clean original of the logo.

For the new special character fonts a clean font original (ideally logo drawing) must be submitted.

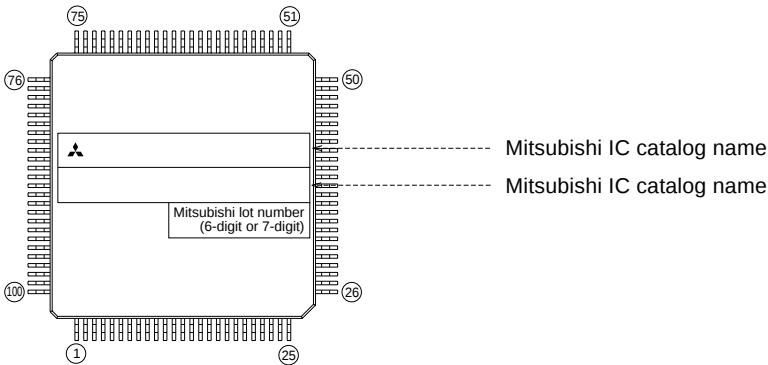
Special logo required ☐

100PFB (100-PIN TQFP) MARK SPECIFICATION FORM

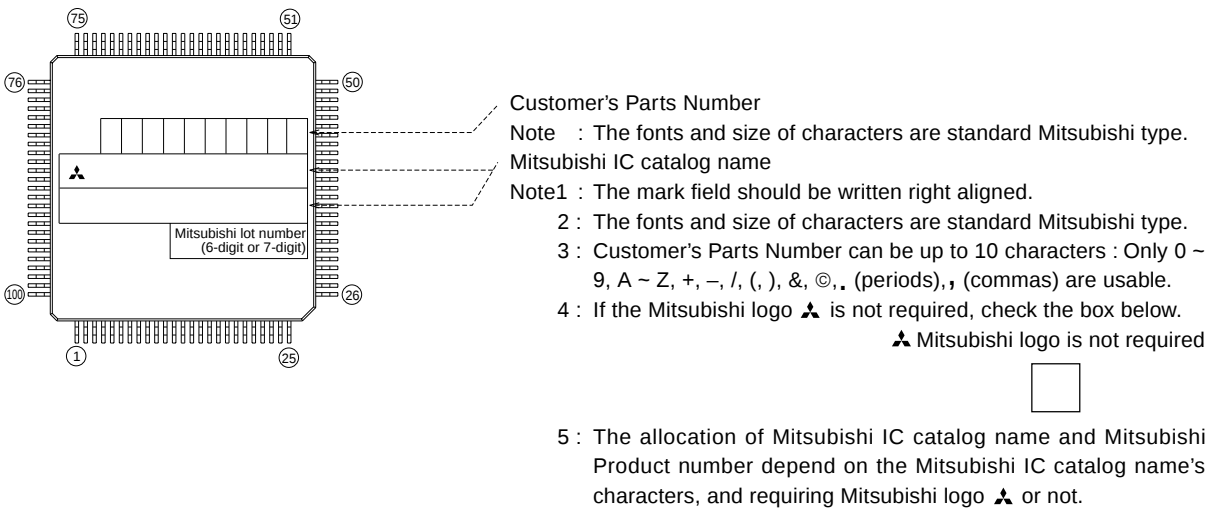
Mitsubishi IC catalog name

Please choose one of the marking types below (A, B, C), and enter the Mitsubishi catalog name and the special mark (if needed).

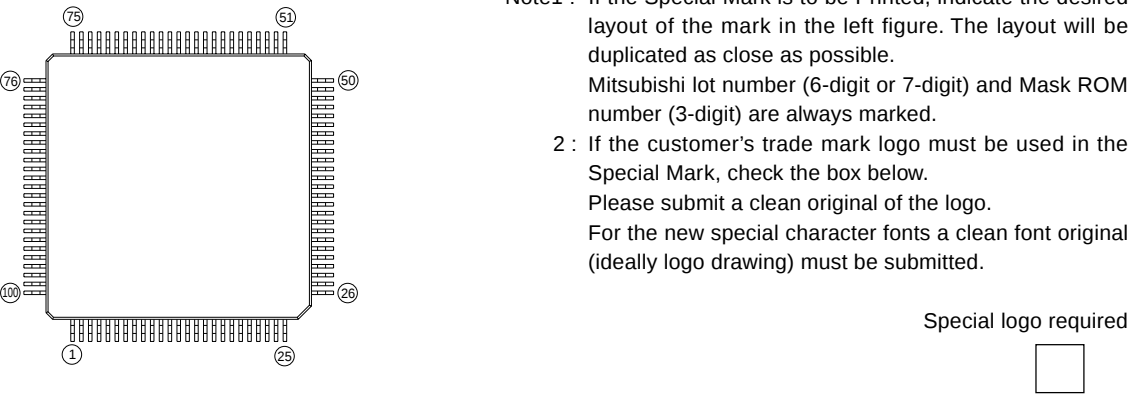
A. Standard Mitsubishi Mark



B. Customer's Parts Number + Mitsubishi catalog name



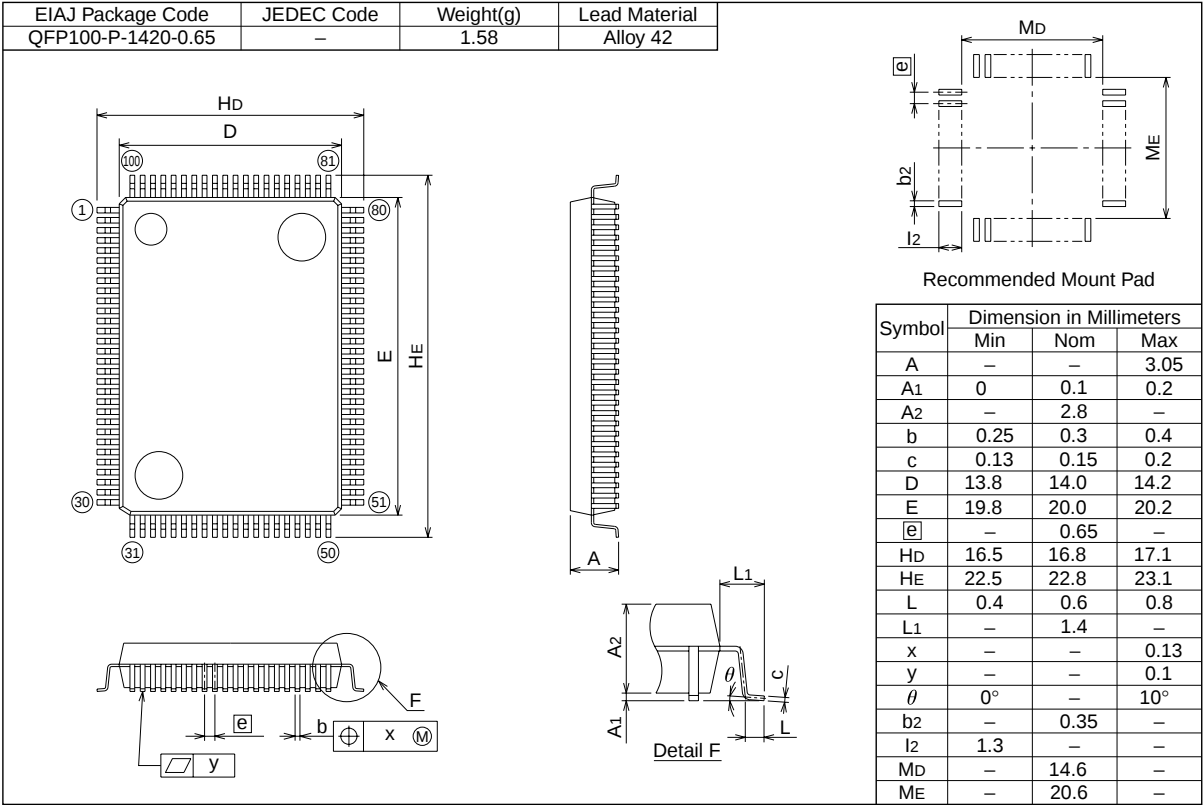
C. Special Mark Required



PACKAGE OUTLINES

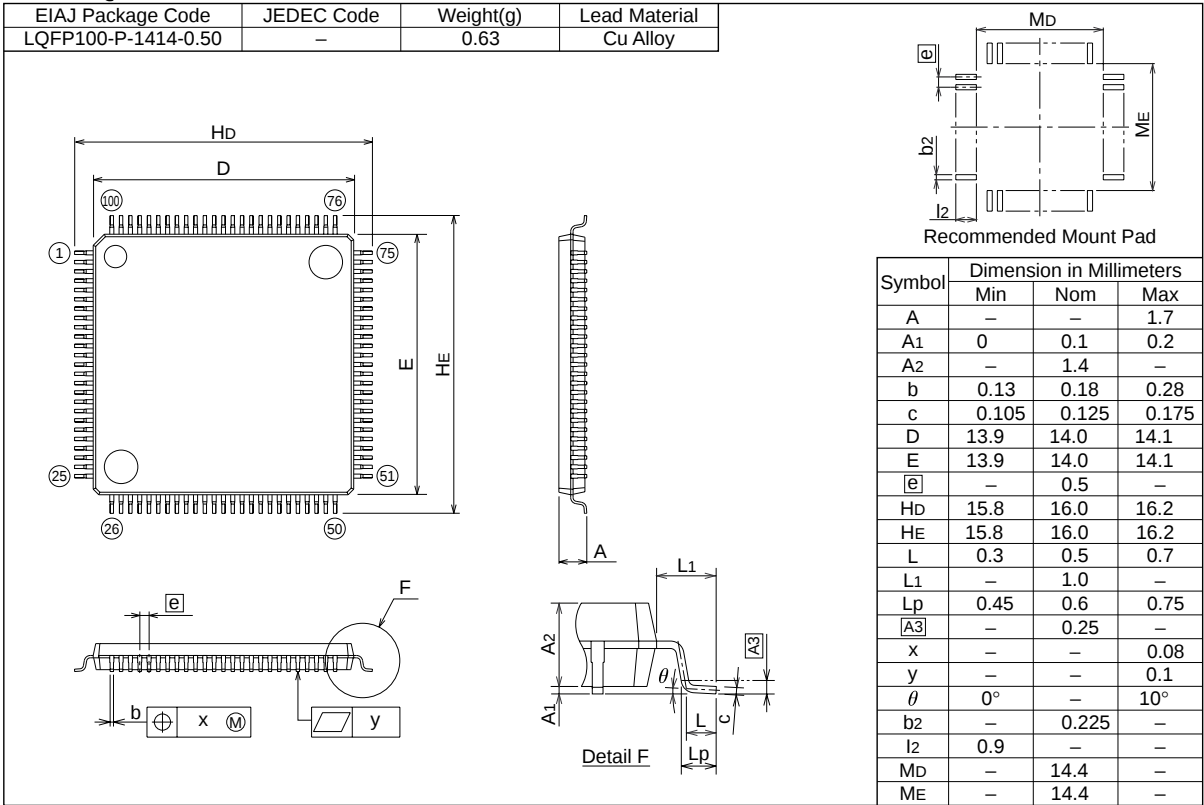
100P6S-A

Plastic 100pin 14X20mm body QFP



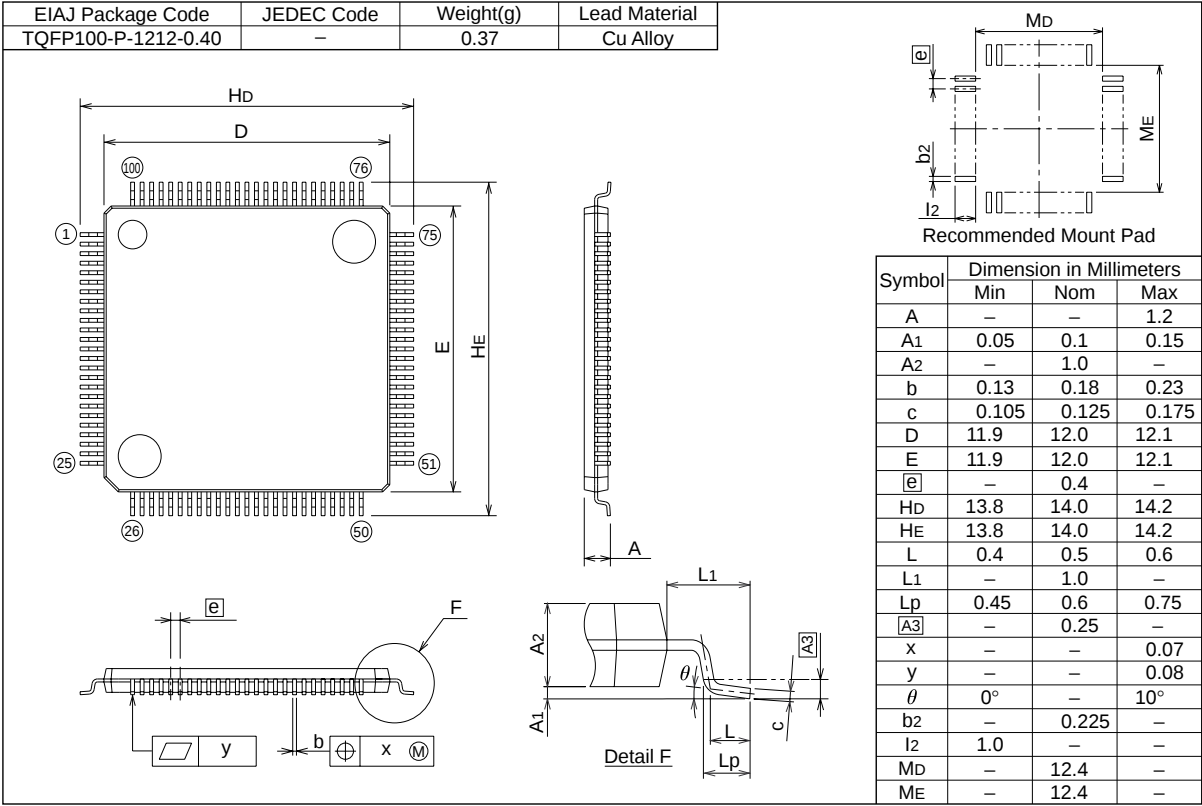
100P6Q-A

Plastic 100pin 14X14mm body LQFP



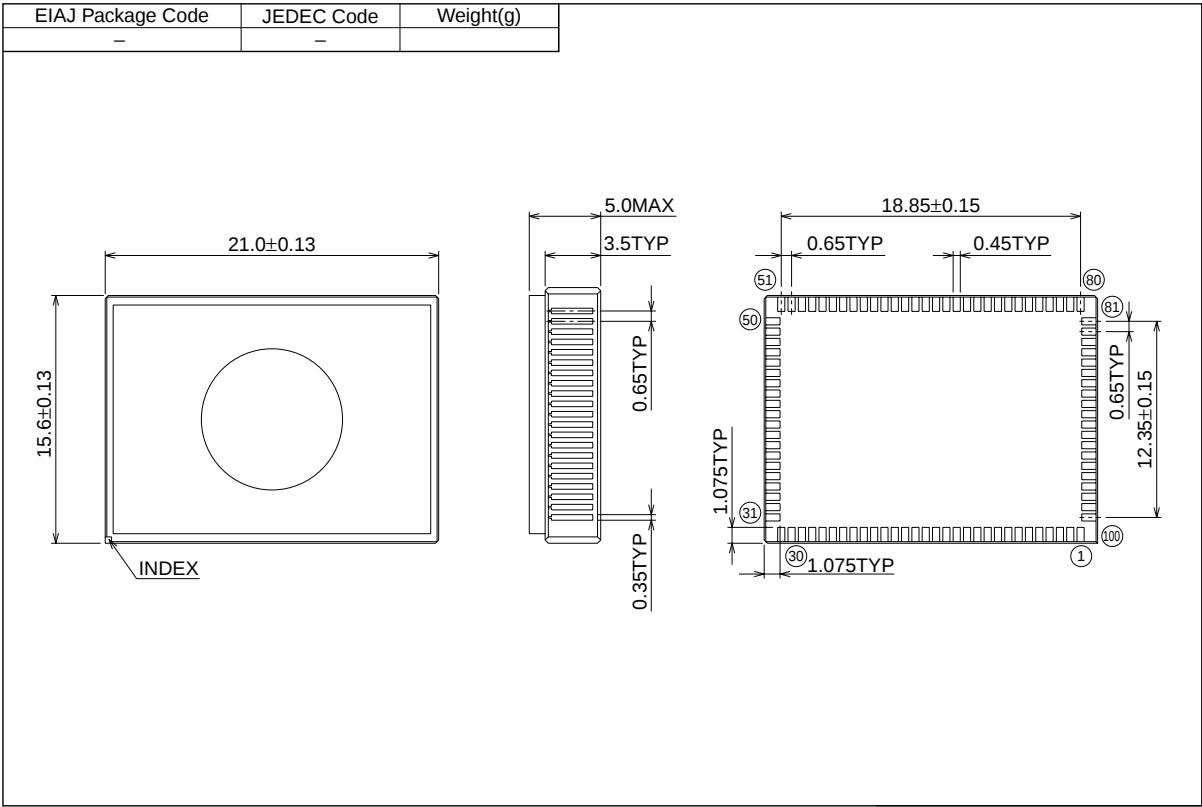
100PFB-A

Plastic 100pin 12X12mm body TQFP



100D0

Glass seal 100pin QFN



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REVISION DESCRIPTION LIST

3825 GROUP DATA SHEET

Rev. No.	Revision Description	Rev. date
1.0	First Edition	980123
2.0	Low power source version is added.	980515
2.1	The followings are mainly revised: On pages 7 to 10; the group expansion On page 17; (11) Port P7o of port block diagram On page 43; the name in Table 11 On pages 53 and 59; the “L” input current parameter of I_{IL} in Tables 25 and 35 is not P7o–P77 but P71–P77.	990713



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