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JTAG-SMT™ Programming Module for Xilinx® FPGAs

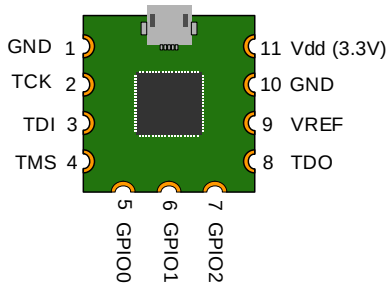
Revised March 2, 2015
This manual applies to the JTAG-SMT2 rev. D

Overview

The Joint Test Action Group (JTAG)-SMT2 is a compact, complete and fully self-contained surface-mount programming module for Xilinx field-programmable gate arrays (FPGAs). The module can be accessed directly from all Xilinx Tools, including iMPACT, Chipscope™, and EDK. Users can load the module directly onto a target board and reflow it like any other component.

The JTAG-SMT2 uses a 3.3V main power supply and a separate Vref supply to drive the JTAG signals. All JTAG signals use high speed, 24mA, three-state buffers that allow signal voltages from 1.8V to 5V and bus speeds of up to 30MBit/sec. The JTAG bus can be shared with other devices as systems hold JTAG signals at high-impedance, except when actively driven during programming. The SMT2 module is CE certified and fully compliant with EU RoHS and REACH directives. The module uses a standard Type-A to Micro-USB cable available for purchase from Digilent, Inc.





Features include:

- Small, complete, all-in-one JTAG programming/debugging solution for Xilinx FPGAs
- Compatible with all Xilinx Tools
- Compatible with IEEE 1149.7-2009 Class T0 – Class T4 (includes 2-Wire JTAG)
- GPIO pin allows debugging software to reset the processor core of Xilinx's Zynq® platform
- Single 3.3V supply
- Separate Vref drives JTAG signal voltages; Vref can be any voltage between 1.8V and 5V.
- High-Speed USB2 port that can drive JTAG/SPI bus at up to 30Mbit/sec (frequency settable by user)
- SPI programming solution (modes 0 and 2 up to 30Mbit/sec, modes 1 and 3 up to 2Mbit/sec)
- Uses micro-AB USB2 connector
- Small form-factor surface-mount module can be directly loaded on target boards
- A similar circuit is available as a stand-alone programming cable; see Digilent's JTAG-HS2.

Users can connect JTAG signals directly to the corresponding FPGA signals, as shown in Fig. 1. For best results, mount the module adjacent to the edge of the host PCB over a ground plane. Although users may run signal traces on top of the host PCB beneath the SMT2, Digilent recommends keeping the area immediately beneath the SMT2 clear.

Note: Keep the impedance between the SMT2 and FPGA below 100 Ohms to operate the JTAG at maximum speed.

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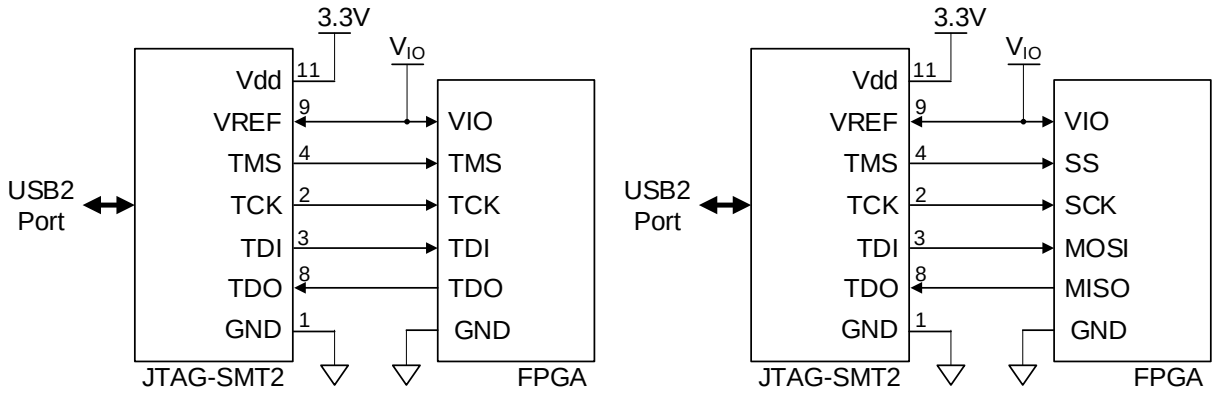


Figure 1. JTAG-SMT2 port connections.

The SMT2 improves upon the SMT1 with the addition of three general purpose IO pins (GPIO0 – GPIO2) and support for interfacing IEEE 1149.7-2009 JTAG targets in both 2 and 4-wire modes.

In addition to supporting JTAG, the JTAG-SMT2 also features eight highly configurable Serial Peripheral Interface (SPI) ports that allow communication with virtually any SPI peripheral (see Fig. 2). All eight SPI ports share the same SCK, MOSI, and MISO pins, so users may enable only one port at any given time. Table 1 summarizes the features supported by each port. The HS2 supports SPI modes 0, 1, 2, and 3.

Chip Select Signal	Port Number	SPI Mode	Shift LSB First	Shift MSB First	Selectable SCK Frequency	Max SCK Frequency	Min SCK Frequency	Inter-byte Delay
TMS/CS0	0	0	Yes	Yes	Yes	30 MHz	8 KHz	0 – 1000 µS
		2	Yes	Yes	Yes	30 MHz	8 KHz	0 – 1000 µS
	1	0	Yes	Yes	Yes	2.066 MHz	485 KHz	0 – 1000 µS
		1	Yes	Yes	Yes	2.066 MHz	485 KHz	0 – 1000 µS
		2	Yes	Yes	Yes	2.066 MHz	485 KHz	0 – 1000 µS
		3	Yes	Yes	Yes	2.066 MHz	485 KHz	0 – 1000 µS
GPIO0/CS1	2	0	Yes	Yes	Yes	30 MHz	8 KHz	0 – 1000 µS
		2	Yes	Yes	Yes	30 MHz	8 KHz	0 – 1000 µS
	3	0	Yes	Yes	Yes	2.066 MHz	485 KHz	0 – 1000 µS
		1	Yes	Yes	Yes	2.066 MHz	485 KHz	0 – 1000 µS
		2	Yes	Yes	Yes	2.066 MHz	485 KHz	0 – 1000 µS
		3	Yes	Yes	Yes	2.066 MHz	485 KHz	0 – 1000 µS
GPIO1/CS2	4	0	Yes	Yes	Yes	30 MHz	8 KHz	0 – 1000 µS
		2	Yes	Yes	Yes	30 MHz	8 KHz	0 – 1000 µS
	5	0	Yes	Yes	Yes	2.066 MHz	485 KHz	0 – 1000 µS
		1	Yes	Yes	Yes	2.066 MHz	485 KHz	0 – 1000 µS
		2	Yes	Yes	Yes	2.066 MHz	485 KHz	0 – 1000 µS
		3	Yes	Yes	Yes	2.066 MHz	485 KHz	0 – 1000 µS
GPIO2/CS3	6	0	Yes	Yes	Yes	30 MHz	8 KHz	0 – 1000 µS
		2	Yes	Yes	Yes	30 MHz	8 KHz	0 – 1000 µS
	7	0	Yes	Yes	Yes	2.066 MHz	485 KHz	0 – 1000 µS
		1	Yes	Yes	Yes	2.066 MHz	485 KHz	0 – 1000 µS
		2	Yes	Yes	Yes	2.066 MHz	485 KHz	0 – 1000 µS
		3	Yes	Yes	Yes	2.066 MHz	485 KHz	0 – 1000 µS

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Note: The Xilinx Tools expect GPIO2/CS3 to be connected to the SRST_B pin on a Zynq chip. As a result, SPI ports 6 and 7 may not be used for SPI communication if the Xilinx Tools are going to be used to communicate with the SMT2.

1 Software Support

In addition to working seamlessly with all Xilinx Tools, Digilent's Adept software and the Adept software development kit (SDK) support the SMT2 module. For added convenience, customers may freely download the SDK from Digilent's website. This Adept software includes a full-featured programming environment and a set of public application programming interfaces (API) that allow user applications to directly drive the JTAG chain.

With the Adept SDK, users can create custom applications that will drive JTAG ports on virtually any device. Users may utilize the APIs provided by the SDK to create applications that can drive any SPI device supporting those modes. Please see the Adept SDK reference manual for more information.

2 IEEE 1149.7-2009 Compatibility

The JTAG-HS2 supports several scan formats, including the JScan0-JScan3, MScan, and OScan0 - OScan7. It is capable of communicating in 4-wire and 2-wire scan chains that consist of Class T0 – T4 JTAG Target Systems (TS) (see Figs. 3 & 4).

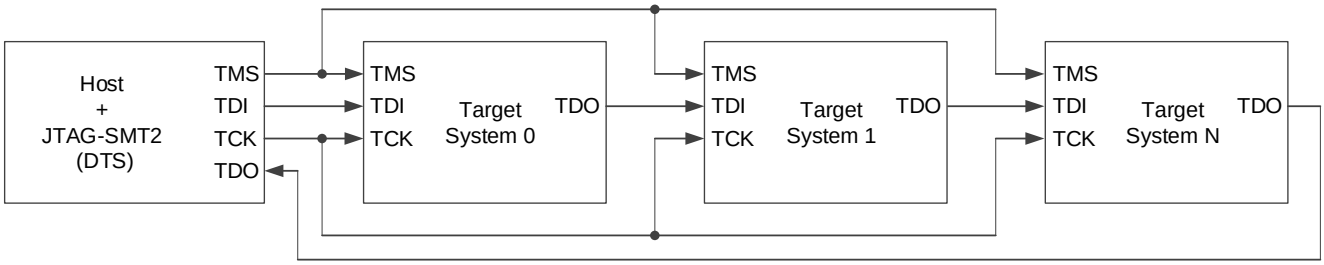


Figure 3. 4-Wire series topology.

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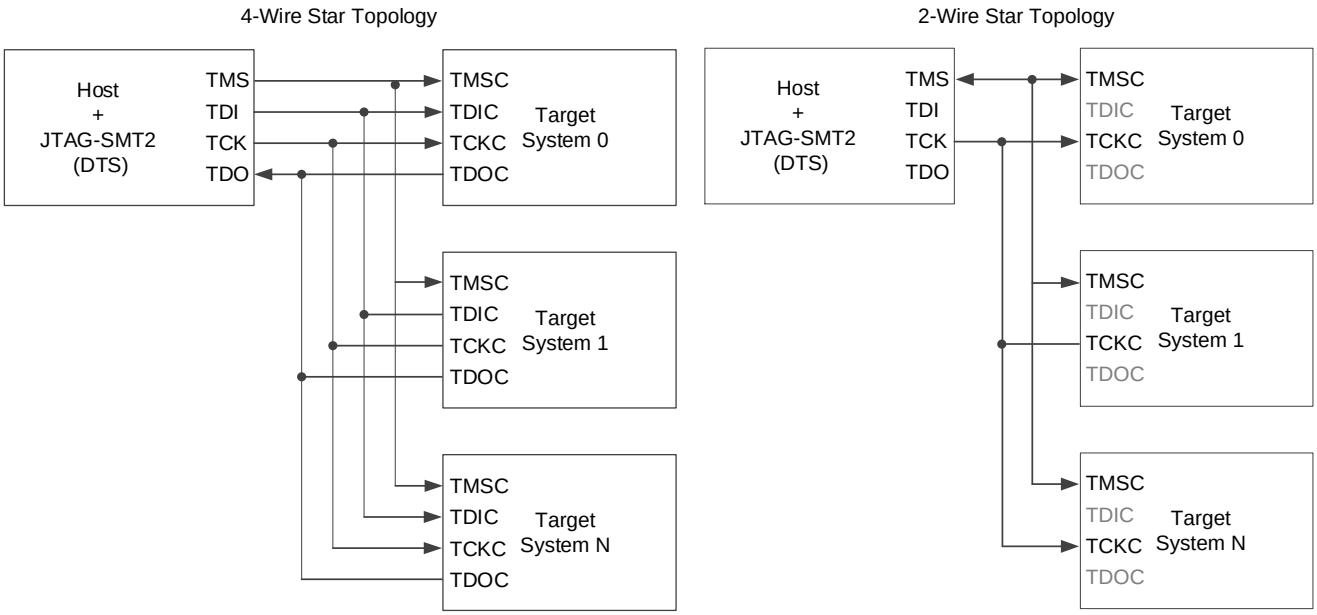


Figure 4. 4-Wire and 2-Wire star topology.

The IEEE 1149.7-2009 specification requires any device that functions as a debug and test system (DTS) to provide a pull-up bias on the TMS and TDO pins. In order to meet this requirement, the JTAG-SMT2 features weak pull-ups (100K ohm) on the TMS, TDI, TDO, and TCK signals. Though not required in the specifications, the pull-ups on the TDI and TCK signals ensure that neither signal floats while another source is not driving them (see Fig. 5).

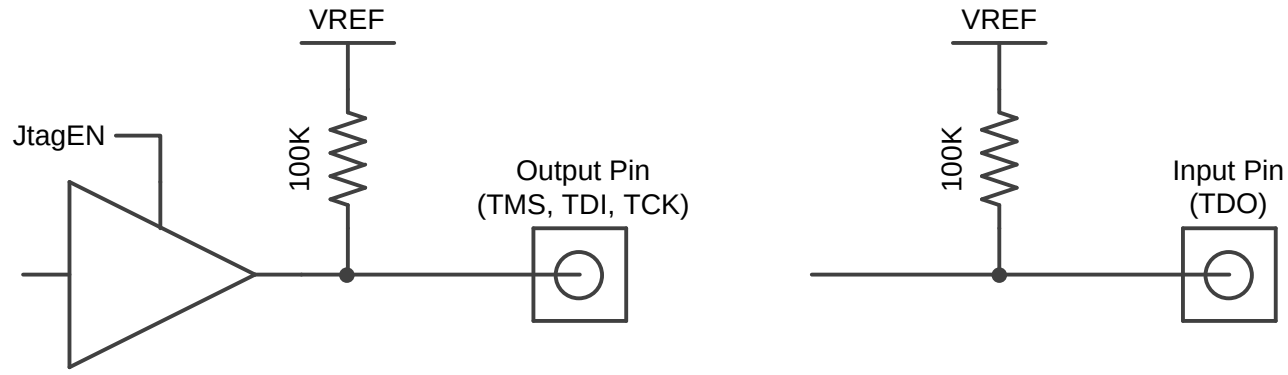


Figure 5. Pull-ups on TMS, TDI, TDO, and TCK signals.

Users should place a current limiting resistor between the TMS pin of the SMT2 and the TMSC pin of the TS when using the JTAG-SMT2 to interface with an 1149.7 compatible TS. If a drive conflict occurs, this resistor should prevent damage to components by limiting the amount of current flowing between the pins of each device. A 200 ohm resistor will limit the maximum current to 16.5mA when using a 3.3V reference (see Figs. 6 & 7). While this level of resistance should be sufficient for most applications, the value of the resistor may need to be adjusted to meet the requirements of the TS.

In most cases users can avoid a drive conflict by having applications that use the SMT2 communicate with the TS in two-wire mode. Use the applications to reconfigure the TS to use the JScan0, JScan1, JScan2, or JScan3 scan format prior to disabling the SMT2's JTAG port.

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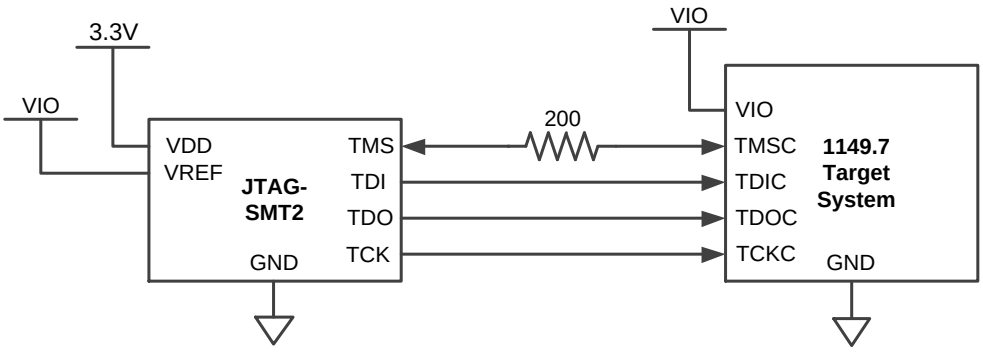


Figure 6. Adding a current limiting resistor.

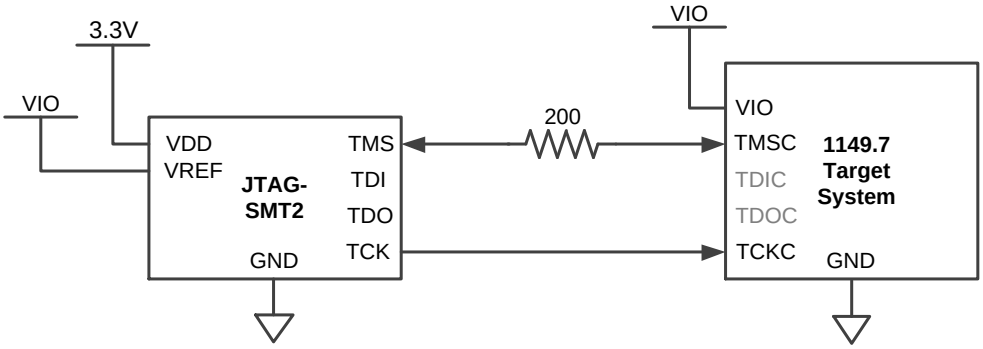


Figure 7. 200 Ohm resistor limiting current flow.

The Adept SDK provides an example application that demonstrates how to communicate with a Class T4 TAP controller using the MScan, OScan0, and OScan1 scan formats.

3 GPIO Pins

The JTAG-SMT2 has three general purpose IO pins (GPIO0, GPIO1, and GPIO2) that are useful for a variety of different applications. Each pin features high speed, three-state input and output buffers. At power up, the JTAG-SMT2 disables these output buffers and places the signals in a high-impedance state. Each signal remains in a high-impedance state until a host application enables DPIO port 0 and configures the applicable pin as an output. When the host application disables DPIO port 0, all GPIO pins revert to a high-impedance state. Weak pull-ups (100K ohm) ensure that the GPIO signals do not float while not being actively driven (see Fig. 8).

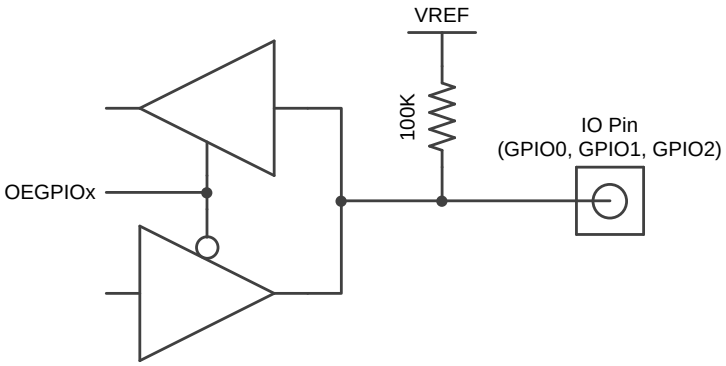


Figure 8. GPIO signals.

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When customers use the JTAG-SMT2 to interface the scan chain of Xilinx's Zynq platform, they should connect the GPIO2 pin of the SMT2 to the Zynq's PS_SRST_B pin. This connection allows the Xilinx Tools to reset the Zynq's processor core at various times during debugging operations. Please see the following "Application Examples" section for more information.

Note: The Xilinx tools expect GPIO2 to be connected to the SRST_B pin on a Zynq chip. As a result, GPIO2 may not be used as a general purpose I/O if the Xilinx Tools are going to be used to communicate with the SMT2.

Note: DPIO port 0 can only be used while both JTAG and SPI are disabled.

4 Application Examples

Example 1: Interfacing a Zynq-7000 when VCCO_0 and VCCO_MIO1 use a common supply

Figure 9demonstrates how to connect the JTAG-SMT2 to Xilinx's Zynq-7000 silicon when the same voltage supplies both the VCCO_0 (Programmable Logic Bank 0 Power Supply) and the VCCO_MIO1 (Processor MIO Bank 1 Power Supply).

In this case the SMT2 has a 100K pull-up to VREF, which operates at the same voltage as VCCO_MIO1. This similar voltage makes it possible to eliminate the external pull-up that is normally required for the PS_SRST_B pin.

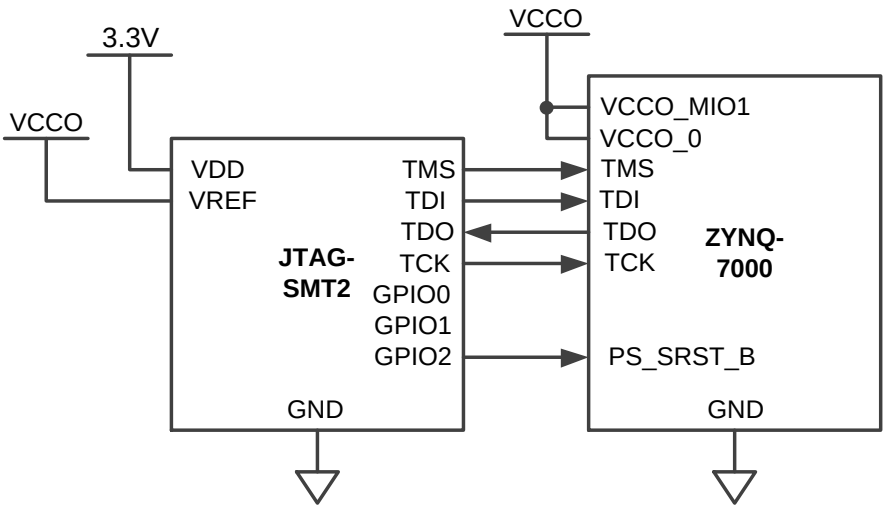


Figure 9. Connecting the JTAG-SMT2 to Xilinx's Zynq-7000.

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Example 2: Interfacing a Zynq-7000 that uses different voltages for VCCO_0 and VCCO_MIO1

Figure 10 demonstrates how to connect the JTAG-SMT2 to Xilinx's Zynq-7000 silicon when different voltages supply the VCCO_0 (Programmable Logic Bank 0 Power Supply) and VCCO_MIO1 (Processor MIO Bank 1 Power Supply). If the Zynq's JTAG pins are operating at a different voltage than the PS_SRST_B, it requires an external buffer to adjust the level of the GPIO2 signal. The example in Fig. 10 demonstrates the use of an open drain buffer to allow for the possibility of adding a reset button.

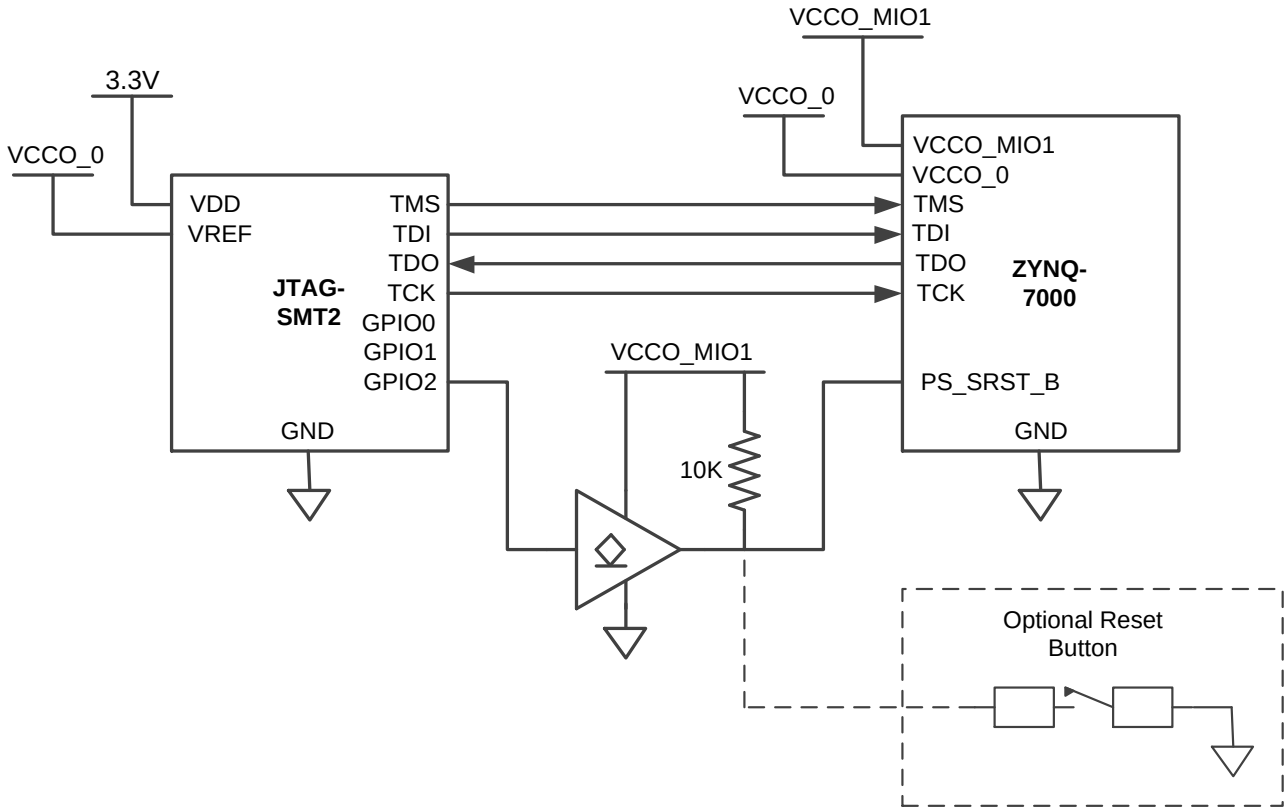


Figure 10. Use of an open drain buffer.

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Example 3: Interfacing a Zynq-7000 while retaining the Xilinx JTAG Header

Figure 11 below demonstrates how to connect the JTAG-SMT2 to Xilinx's Zynq-7000 silicon alongside Xilinx's 14-pin JTAG header. In this example the open drain buffers allow both the SMT2 and Xilinx JTAG Header to drive the PS_SRST_B pin, which may operate a different voltage than the Zynq's JTAG pins.

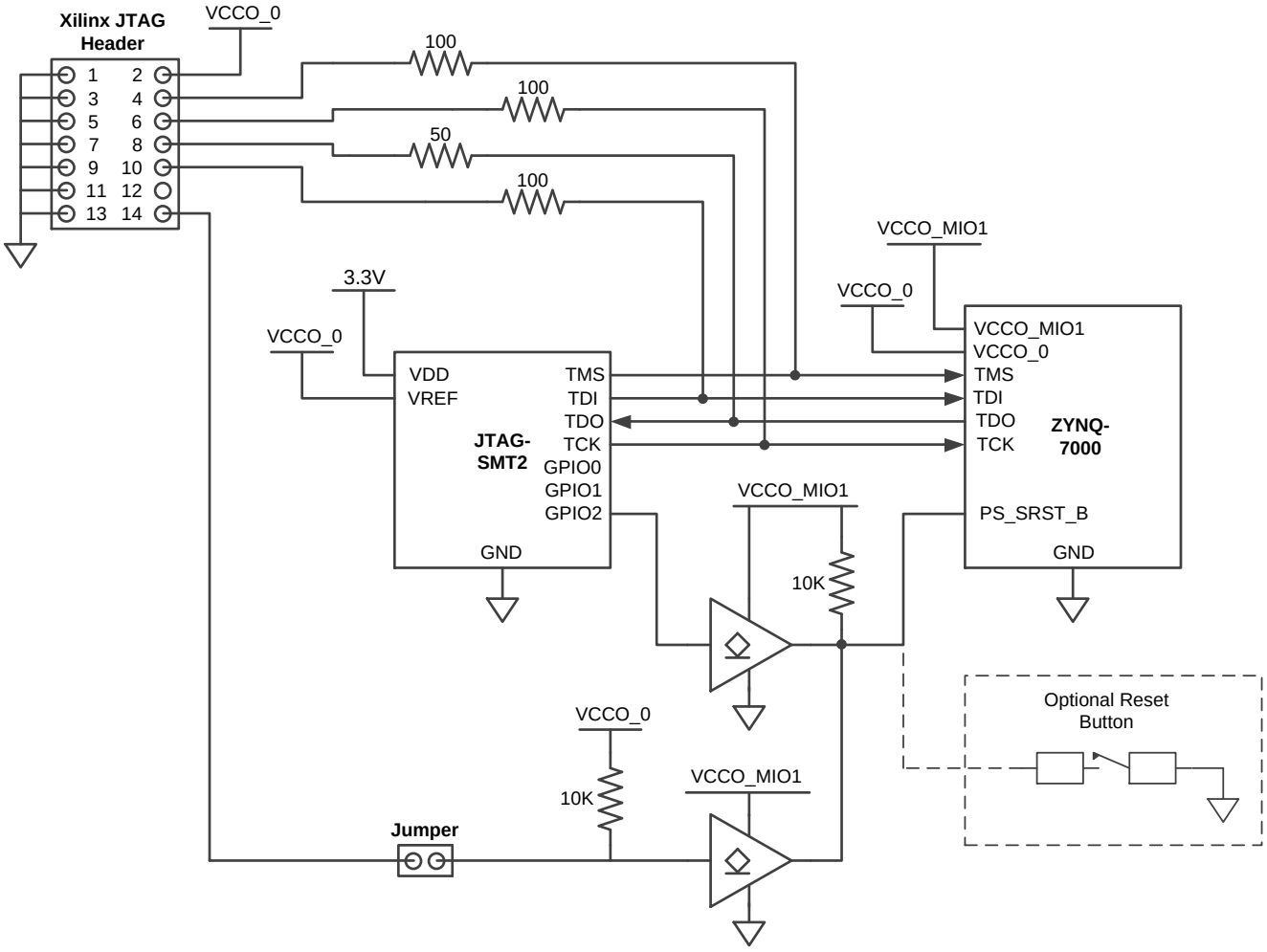
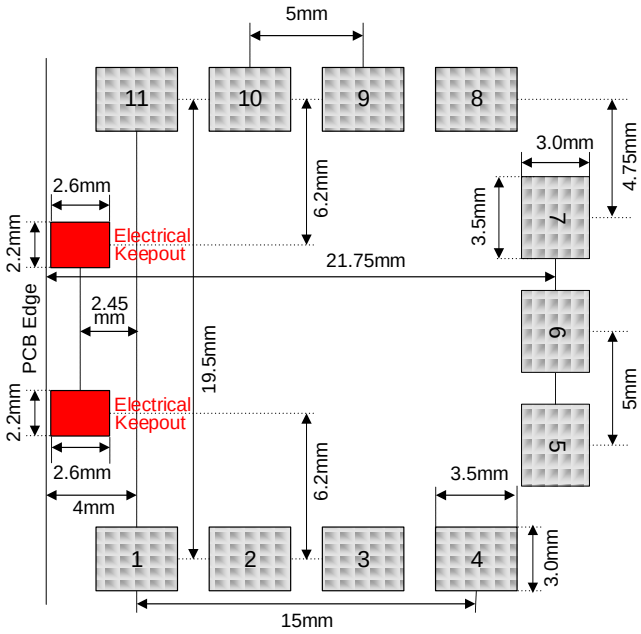


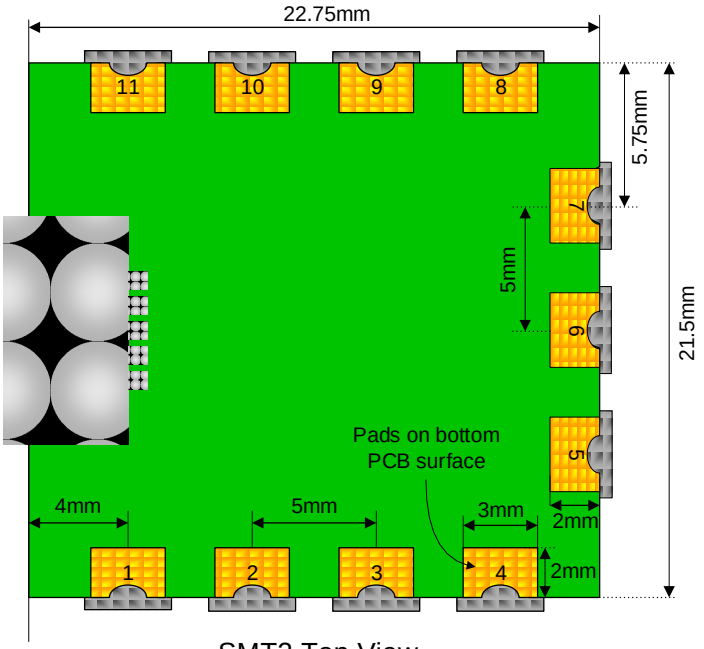
Figure 11. Open drain buffers allowing the SMT2 and JTAG Header to drive the PS_SRST_B pin.

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5 Mechanical Information



Recommended PCB Land Pattern



SMT2 Top View

6 Absolute Maximum Ratings

Symbol	Parameter	Condition	Min	Max	Unit
Vdd	Operating supply voltage		-0.3	4.0	V
Vref	I/O reference/supply voltage		-0.3	6	V
VIO	Signal Voltage		-0.3	6	V
I_{IK},I_{OK}	TMS, TCK, TDI, TDO, GPIO0, GPIO1, GPIO2 DC Input/Output Diode Current	VIO < -0.3V		-50	mA
		VIO > 6V		+20	
I_{OUT}	DC Output Current			±50	mA
T_{STG}	Storage Temperature		-20	+120	ºC
ESD	Human Body Model JESD22-A114			4000	V
	Charge Device Model JESD22-C101			2000	V

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7 DC Operating Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
Vdd	Operating supply voltage	2.97	3.3	3.63	Volts
Vref	I/O reference/supply voltage	1.65	2.5/3.3	5.5	Volts
TDO, GPIO0, GPIO1, GPIO2	Input High Voltage (V_{IH})	1.62		5.5	Volts
	Input Low Voltage (V_{IL})	0		0.65	Volts
TMS, TCK, TDI, GPIO0, GPIO1, GPIO2	Output High (V_{OH})	0.85 x Vref	0.95 x Vref	Vref	Volts
	Output Low (V_{OL})	0	0.05 x Vref	0.15 x Vref	Volts
T_A	Operating Temperature	0		70	ºC

8 AC Operating Characteristics

The JTAG-SMT2's JTAG signals operate according to the timing diagram in Fig. 12. The SMT2 supports JTAG/TCK frequencies from 30 MHz to 8 KHz at integer divisions of 30 MHz from 1 to 3750. Common frequencies include 30 MHz, 15 MHz, 10 Mhz, 7.5 MHz, and 6 MHz (see Table 2). The JTAG/TCK operating frequency can be set within the Xilinx Tools. *Note: Please refer to Xilinx's iMPACT documentation for more information.*

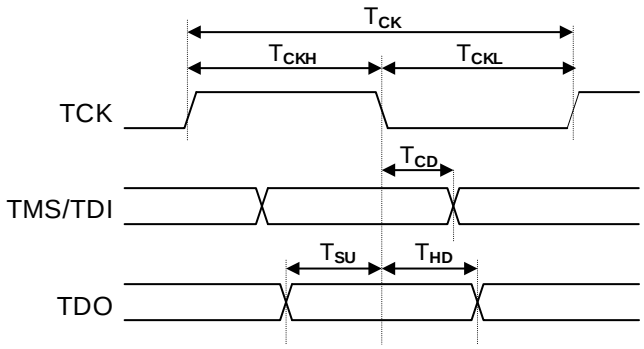


Figure 12. Timing diagram.

Symbol	Parameter	Min	Max
T_{CK}	T_{CK} period	33ns	2.185ms
T_{CKH}, T_{CKL}	T_{CLK} pulse width	20ns	1.1ms
T_{CD}	T_{CLK} to TMS, TDI	0	15ns
T_{SU}	TDO Setup time	19ns	
T_{HD}	TDO Hold time	0	

Table 2. JTAG frequency support.

9 Mounting to Host PCBs

The JTAG-SMT2 module has a moisture sensitivity level (MSL) of 6. Prior to reflow, the JTAG-SMT2 module must be dried by baking it at 125° C for 17 hours. Once this process has been completed, the module has a MSL of 3 and is suitable for reflow for up to 168 hours without additional drying.

The factory finishes the JTAG-SMT2 signal pads with the ENIG process using 2u" gold over 150u" electroless nickel. This makes the SMT2 compatible with most mounting and reflow processes (see Fig. 13). The binding force of the solder is sufficient to hold the SMT2 firmly in place so mounting should require no additional adhesives.

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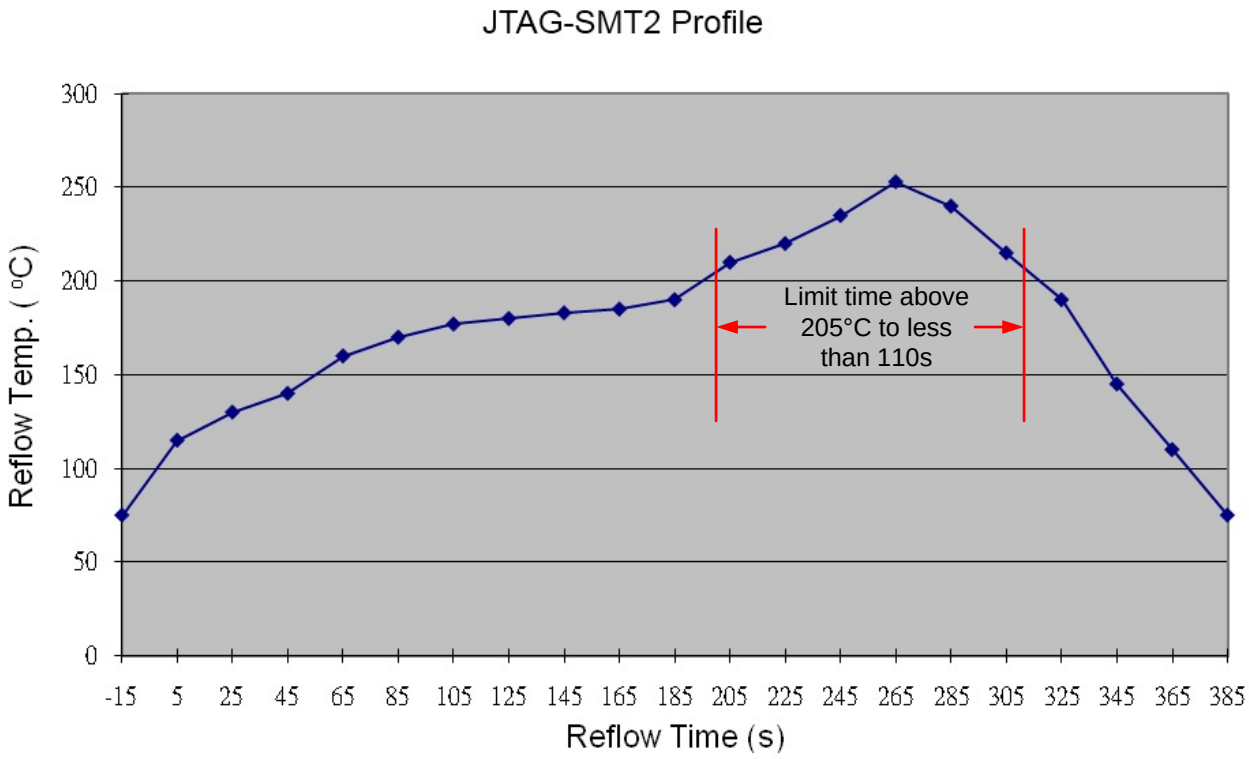


Figure 13.JTAG-SMT2 reflow temperature over time.

10 Packaging

Digilent ships small quantities of less than 20 per order individually packaged in antistatic bags. Digilent will pack and ship larger quantities in groups of 80 positioned in an antistatic bubble tray (see Fig. 14).

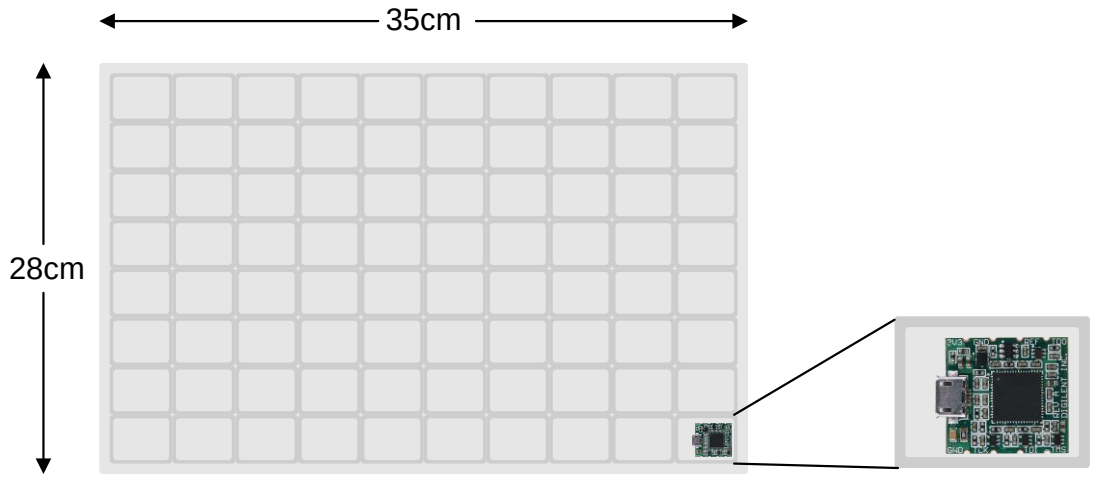


Figure 14. JTAG-SMT2 shipping arrangement.

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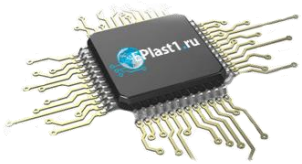
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