MAX17019 High-Input-Voltage Quad-Output Controller

General Description

The MAX17019 is a high-input-voltage quad-output controller (up to 38V). The MAX17019 provides a compact, low-cost controller capable of providing four independent regulators—a main stage, a $3A_{P-P}$ internal stepdown, a $5A_{P-P}$ internal step-down, and a 2A source/sink linear regulator. The input voltage is up to 38V.

The internal switching regulators include 5V synchronous MOSFETs that can be powered directly from a single Li+ cell or from the main 3.3V/5V power stages. Finally, the linear regulator is capable of sourcing and sinking 2A to support DDR termination requirements or to generate a fixed output voltage.

The step-down converters use a peak current-mode, fixed-frequency control scheme—an easy to implement architecture that does not sacrifice fast-transient response. This architecture also supports peak current-limit protection and pulse-skipping operation to maintain high efficiency under light-load conditions.

Separate enable inputs and independent open-drain power-good outputs allow flexible power sequencing. A soft-start function gradually ramps up the output voltage to reduce the inrush current. Disabled regulators enter high-impedance states to avoid negative output voltage created by rapidly discharging the output through the low-side MOSFET. The MAX17019 also includes output undervoltage, output overvoltage, and thermal-fault protection.

The MAX17019 is available in a 48-pin, 6mm x 6mm thin QFN package.

Applications

- Embedded Control Systems
- Set-Top Boxes

Benefits and Features

- Fixed-Frequency, Current-Mode Controllers
- 5.5V to 38V Input Range (Step-Down)
- 1x Step-Down Controller
- 1x Internal $5A_{P-P}$ Step-Down Regulator
- 1x Internal $3A_{P-P}$ Step-Down Regulator
- 1x 2A Source/Sink Linear Regulator with Dynamic REFIN
- Internal BST Diodes
- Internal 5V 50mA Linear Regulator
- Fault Protection—Undervoltage, Overvoltage, Thermal, Peak Current Limit
- Independent Enable Inputs and Power-Good Outputs
- Voltage-Controlled Soft-Start
- High-Impedance Shutdown
- 10μA (typ) Shutdown Current

***Ordering Information** appears at end of data sheet.*

Absolute Maximum Ratings

INLDO, $\overline{SHDN}$ to GND ....-0.3V to +43V
LDO5, INA, V_{DD}, V_{CC} to GND................................-0.3V to +6V
DHA to LXA..-0.3V to (V_{BSTA} + 0.3V)
ONA, ONB, ONC, OND to GND..............................-0.3V to +6V
POKA, POKB, POKC, $\overline{POKD}$ to GND.........-0.3V to (V_{CC} + 0.3V)
REF, REFIND, FREQ, $\overline{UP}$/DN,
SYNC to GND.......................................-0.3V to (V_{CC} + 0.3V)
FBA, FBB, FBC, FBD to GND.....................-0.3V to (V_{CC} + 0.3V)
BYP to GND..-0.3V to (V_{LDO5} + 0.3V)
CSPA, CSNA to GND ....-0.3V to (V_{CC} + 0.3V)
DLA to GND...-0.3V to (V_{DD} + 0.3V)
INBC, IND to GND..-0.3V to +6V
OUTD to GND..-0.3V to (V_{IND} + 0.3V)
VTTR to GND...-0.3V to (V_{BYP} + 0.3V)
LXB, LXC to GND...................................-1.0V to (V_{INBC} + 0.3V)
BSTB to GND.................................(V_{DD} - 0.3V) to (V_{LXB} + 6V)
BSTC to GND................................(V_{DD} - 0.3V) to (V_{LXC} + 6V)
BSTA to GND.................................(V_{DD} - 0.3V) to (V_{LXA} + 6V)
REF Short-Circuit Current..1mA
Continuous Power Dissipation (T_A = +70°C)
TQFN (derate 37mW/°C above +70°C)..........................2.9W
(Multilayer Board)
Operating Temperature Range ....-40°C to +105°C
Junction Temperature...+150°C
Storage Temperature Range ....-65°C to +150°C
Lead Temperature (soldering, 10s)..................................+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

PACKAGE TYPE: 48-PIN TQFN	
Package Code	T4866+2
Outline Number	**21-0141**
Land Pattern Number	**90-0007**

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Electrical Characteristics (T_A = 0°C to +85°C)

(*Standard Application Circuit*, V_{INLDO} = 12V, V_{INA} = V_{INBC} = V_{DD} = V_{CC} = V_{BYP} = V_{CSPA} = V_{CSNA} = 5V, V_{IND} = 1.8V, $V_{\overline{SHDN}}$ = V_{ONA} = V_{ONB} = V_{ONC} = V_{OND} = 5V, I_{REF} = I_{LDO5} = I_{OUTD} = no load, FREQ = GND, $\overline{UP}$/DN = V_{CC}, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage Range		$\overline{UP}$/DN = LDO5, INLDO, INA = LDO5	5.5		38	V
INA Undervoltage Threshold	$V_{INA(UVLO)}$	$\overline{UP}$/DN = LDO5, INA = V_{CC}, rising edge, hysteresis = 160mV	4.0	4.2	4.4	V
INBC Input Voltage Range			2.3		5.5	V
SUPPLY CURRENTS						
V_{INLDO} Shutdown Supply Current	$I_{IN(\overline{SHDN})}$	V_{INLDO} = 5.5V to 38V, $\overline{SHDN}$ = GND		10	15	µA
V_{INLDO} Suspend Supply Current	$I_{IN(SUS)}$	V_{INLDO} = 5.5V to 38V, ON_ = GND, $\overline{SHDN}$ = INLDO		50	80	µA
V_{CC} Shutdown Supply Current		$\overline{SHDN}$ = ONA = ONB = ONC = OND = GND, T_A = +25°C		0.1	1	µA
V_{DD} Shutdown Supply Current		$\overline{SHDN}$ = ONA = ONB = ONC = OND = GND, T_A = +25°C		0.1	1	µA
INA Shutdown Current	I_{INA}	$\overline{SHDN}$ = ONA = ONB = ONC = OND = GND, $\overline{UP}$/DN = V_{CC}		7	10	µA

Electrical Characteristics (T_A = 0°C to +85°C) (continued)

(*Standard Application Circuit*, V_{INLDO} = 12V, V_{INA} = V_{INBC} = V_{DD} = V_{CC} = V_{BYP} = V_{CSPA} = V_{CSNA} = 5V, V_{IND} = 1.8V, $V_{\overline{SHDN}}$ = V_{ONA} = V_{ONB} = V_{ONC} = V_{OND} = 5V, I_{REF} = I_{LDO5} = I_{OUTD} = no load, FREQ = GND, $\overline{UP}$/DN = V_{CC}, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
5V LINEAR REGULATOR (LDO5)						
V_{CC} Supply Current Main Step-Down and Regulator B		ONA = ONB = V_{CC}, ONC = OND = GND; does not include switching losses, measured from V_{CC}		280	350	µA
V_{CC} Supply Current Main Step-Down and Regulator C		ONA = ONC = V_{CC}, ONB = OND = GND; does not include switching losses, measured from V_{CC}		280	350	µA
V_{CC} Supply Current Main Step-Down and Regulator D		ONA = OND = V_{CC}, ONB = ONC = GND; does not include switching losses, measured from V_{CC}		2.2	3	mA
INA Supply Current	I_{INA}	ONA = V_{CC}, $\overline{UP}$/DN = V_{CC}		40	60	µA
5V LINEAR REGULATOR (LDO5)						
LDO5 Output Voltage	V_{LDO5}	V_{INLDO} = 5.5V to 38V, I_{LDO5} = 0 to 50mA, BYP = GND	4.75	5.0	5.2	V
LDO5 Short-Circuit Current Limit		LDO5 = BYP = GND, V_{INLDO} = 5.5V	70	160	250	mA
BYP Switchover Threshold	V_{BYP}	Rising edge		4.65		V
LDO5-to-BYP Switch Resistance	R_{BYP}	LDO5 to BYP, V_{BYP} = 5V, I_{LDO5} = 50mA		1.5	4	Ω
1.25V REFERENCE						
Reference Output Voltage	V_{REF}	No load	1.237	1.25	1.263	V
Reference Load Regulation	ΔV_{REF}	I_{REF} = -1µA to +50µA		3	10	mV
Reference Undervoltage Lockout	$V_{REF(UVLO)}$			1.0		V
OSCILLATOR						
Oscillator Frequency	f_{OSC}	FREQ = V_{CC}		500		kHz
		FREQ = REF		750		kHz
		FREQ = GND	0.9	1.0	1.1	MHz
Switching Frequency	f_{SWA}	Regulator A		1/2 f_{OSC}		MHz
	f_{SWB}	Regulator B		f_{OSC}		
	f_{SWC}	Regulator C		1/2 f_{OSC}		
Maximum Duty Cycle (All Switching Regulators)	D_{MAX}		90	93.5		%
Minimum On-Time (All Switching Regulators)	$t_{ON(MIN)}$	FREQ = V_{CC} or GND		90		ns
		FREQ = REF		75		ns

Idle Mode is a trademark of Maxim Integrated Products, Inc.

Electrical Characteristics (T_A = 0°C to +85°C) (continued)

(*Standard Application Circuit*, V_{INLDO} = 12V, V_{INA} = V_{INBC} = V_{DD} = V_{CC} = V_{BYP} = V_{CSPA} = V_{CSNA} = 5V, V_{IND} = 1.8V, $V_{\overline{SHDN}}$ = V_{ONA} = V_{ONB} = V_{ONC} = V_{OND} = 5V, I_{REF} = I_{LDO5} = I_{OUTD} = no load, FREQ = GND, $\overline{UP}$/DN = V_{CC}, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
REGULATOR A (Main Step-Down)						
Output Voltage-Adjust Range		Step-down configuration ($\overline{UP}$/DN = V_{CC})	1.0		V_{CC} + 0.3	V
FBA Regulation Voltage	V_{FBA}	Step-down configuration ($\overline{UP}$/DN = V_{CC}), V_{CSPA} - V_{CSNA} = 0 to 20mV, 90% duty cycle	0.968	0.97	1.003	V
FBA Regulation Voltage (Overload)	V_{FBA}	Step-down configuration ($\overline{UP}$/DN = V_{CC}), V_{CSPA} - V_{CSNA} = 0 to 20mV, 90% duty cycle	0.930		1.003	V
FBA Load Regulation	ΔV_{FBA}	Step-down configuration ($\overline{UP}$/DN = V_{CC}), V_{CSPA} - V_{CSNA} = 0 to 20mV		16		mV
FBA Line Regulation		$\overline{UP}$/DN = V_{CC}, 0 to 100% duty cycle; Step-down ($\overline{UP}$/DN = V_{CC})	10	16	22	mV
FBA Input Current	I_{FBA}	$\overline{UP}$/DN = GND or V_{CC}, T_A = +25°C	-100	-5	+100	nA
Current-Sense Input Common-Mode Range	V_{CSA}		0		V_{CC} + 0.3V	V
Current-Sense Input Bias Current	I_{CSA}	T_A = +25°C		40	60	µA
Idle Mode™ Threshold	V_{IDLEA}			4		mV
Current-Limit Threshold (Positive)	V_{ILIMA}		18	20	22	mV
Zero-Crossing Threshold	V_{IZX}			1		mV
DHA Gate Driver On-Resistance	R_{DH}	DHA forced high and low		2.5	5	Ω
DLA Gate Driver On-Resistance	R_{DL}	DLA forced high		2.5	5	Ω
		DLA forced low		1.5	3	
DHA Gate Driver Source/Sink Current	I_{DH}	DHA forced to 2.5V		0.7		A
DLA Gate Driver Source/Sink Current	$I_{DL(SRC)}$	DLA forced to 2.5V		0.7		A
	$I_{DL(SNK)}$	DLA forced to 2.5V		1.5		
REGULATOR B (Internal 3A Step-Down Converter)						
FBB Regulation Voltage		I_{LXB} = 0% duty cycle (Note 2)	0.747	0.755	0.762	V
FBB Regulation Voltage (Overload)	V_{FBB}	I_{LXB} = 0 to 2.5A, 0% duty cycle (Note 2)	0.720		0.762	V
FBB Load Regulation	$\Delta V_{FBB}/\Delta I_{LXB}$	I_{LXB} = 0 to 2.5A		-5		mV/A
FBB Line Regulation		0 to 100% duty cycle	7	8	10	mV
FBB Input Current	I_{FBB}	T_A = +25°C	-100	-5	+100	nA
Internal MOSFET On-Resistance		High-side n-channel		75	150	mΩ
		Low-side n-channel		40	80	
LXB Peak Current Limit	I_{PKB}		3.0	3.45	4.0	A
LXB Idle-Mode Trip Level	I_{IDLEB}			0.8		A
LXB Zero-Crossing Trip Level	I_{ZXB}			100		mA

Electrical Characteristics (T_A = 0°C to +85°C) (continued)

(*Standard Application Circuit*, V_{INLDO} = 12V, V_{INA} = V_{INBC} = V_{DD} = V_{CC} = V_{BYP} = V_{CSPA} = V_{CSNA} = 5V, V_{IND} = 1.8V, $V_{\overline{SHDN}}$ = V_{ONA} = V_{ONB} = V_{ONC} = V_{OND} = 5V, I_{REF} = I_{LDO5} = I_{OUTD} = no load, FREQ = GND, $\overline{UP}$/DN = V_{CC}, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
REGULATOR C (Internal 5A Step-Down Converter)							
FBC Regulation Voltage		I_{LXC} = 0A, 0% duty cycle (Note 2)		0.747	0.755	0.762	V
FBC Regulation Voltage (Overload)	V_{FBC}	I_{LXC} = 0 to 4A, 0% duty cycle (Note 2)		0.710		0.762	V
FBC Load Regulation	$\Delta V_{FBC}/\Delta I_{LXC}$	I_{LXC} = 0 to 4A			-7		mV/A
FBC Line Regulation		0 to 100% duty cycle		12	14	16	mV
FBC Input Current	I_{FBC}	T_A = +25°C		-100	-5	+100	nA
Internal MOSFET On-Resistance		High-side n-channel			50	100	mΩ
		Low-side n-channel			25	40	
LXC Peak Current Limit	I_{PKC}			5.0	5.75	6.5	A
LXC Idle-Mode Trip Level	I_{IDLEC}				1.2		A
LXC Zero-Crossing Trip Level	I_{ZXC}				100		mA
REGULATOR D (Source/Sink Linear Regulator and VTTR Buffer)							
IND Input Voltage Range	V_{IND}			1		2.8	V
IND Supply Current		OND = V_{CC}			10	50	µA
IND Shutdown Current		OND = GND, T_A = +25°C				10	µA
REFIND Input Range				0.5		1.5	V
REFIND Input Bias Current		V_{REFIND} = 0 to 1.5V, T_A = +25°C		-100		+100	nA
OUTD Output Voltage Range	V_{OUTD}			0.5		1.5	V
FBD Output Accuracy	V_{FBD}	V_{FBD} with respect to V_{REFIND}, OUTD = FBD, I_{OUTD} = +50µA (source load)		-10		0	mV
		V_{FBD} with respect to V_{REFIND}, OUTD = FBD, I_{OUTD} = -50µA (sink load)		0		+10	
FBD Load Regulation		I_{OUTD} = ±1A		-17	-13		mV/A
FBD Line Regulation		V_{IND} = 1.0V to 2.8V, I_{OUTD} = ±200mA			1		mV
FBD Input Current		V_{FBD} = 0 to 1.5V, T_A = +25°C			0.1	0.5	µA
OUTD Linear-Regulator Current Limit		Source load		+2		+4	A
		Sink load		-2		-4	
Current-Limit Soft-Start Time		With respect to internal OND signal			160		µs
Internal MOSFET On-Resistance		High-side on-resistance			120	250	mΩ
		Low-side on-resistance			180	450	
VTTR Output Accuracy		REFIND to VTTR	I_{VTTR} = ±0.5mA	-10		+10	mV
			I_{VTTR} = ±3mA	-20		+20	
VTTR Maximum Current Rating					±5		mA

Electrical Characteristics (T_A = 0°C to +85°C) (continued)

(*Standard Application Circuit*, V_{INLDO} = 12V, V_{INA} = V_{INBC} = V_{DD} = V_{CC} = V_{BYP} = V_{CSPA} = V_{CSNA} = 5V, V_{IND} = 1.8V, $V_{\overline{SHDN}}$ = V_{ONA} = V_{ONB} = V_{ONC} = V_{OND} = 5V, I_{REF} = I_{LDO5} = I_{OUTD} = no load, FREQ = GND, $\overline{UP}$/DN = V_{CC}, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
FAULT PROTECTION						
SMPS POK and Fault Thresholds		Upper threshold rising edge, hysteresis = 50mV	9	12	14	%
		Lower threshold falling edge, hysteresis = 50mV	-14	-12	-9	
VTT LDO POKD and Fault Threshold		Upper threshold rising edge, hysteresis = 50mV	6	12	16	%
		Lower threshold falling edge, hysteresis = 50mV	-16	-12	-6	
POK Propagation Delay	t_{POK}	FB_ forced 50mV beyond POK_ trip threshold		5		µs
Overvoltage Fault Latch Delay	t_{OVP}	FB_ forced 50mV above POK_ upper trip threshold		5		µs
SMPS Undervoltage Fault Latch Delay	t_{UVP}	FBA, FBB, or FBC forced 50mV below POK_ lower trip threshold		5		µs
VTT LDO Undervoltage Fault Latch Delay	t_{UVP}	FBD forced 50mV below POKD lower trip threshold		5000		µs
POK Output Low Voltage	V_{POK}	I_{SINK} = 3mA			0.4	V
POK Leakage Currents	I_{POK}	V_{FBA} = 1.05V, V_{FBB} = V_{FBC} = 0.8V, V_{FBD} = V_{REFIND} + 50mV (POK high impedance); POK_ forced to 5V, T_A = +25°C			1	µA
Thermal-Shutdown Threshold	T_{SHDN}	Hysteresis = 15°C		+160		°C
GENERAL LOGIC LEVELS						
$\overline{SHDN}$ Input Logic Threshold		Hysteresis = 20mV	0.5		1.6	V
$\overline{SHDN}$ Input Bias Current		T_A = +25°C, $\overline{SHDN}$ = 0~16V	-2		+2	µA
		T_A = +25°C, $\overline{SHDN}$ = 17V~38V	-2		+150	
ON_ Input Logic Threshold		Hysteresis = 170mV	0.5		1.6	V
ON_ Input Bias Current		T_A = +25°C	-1		+1	µA
$\overline{UP}$/DN Input Logic Threshold			0.5		1.6	V
$\overline{UP}$/DN Input Bias Current		T_A = +25°C	-1		+1	µA
FREQ Input Voltage Levels		High (V_{CC})	V_{CC} - 0.4V			V
		Unconnected/REF	1.65		3.8	
		Low (GND)			0.5	
FREQ Input Bias Current		T_A = +25°C	-2		+2	µA
SYNC Input Logic Threshold			1.5		3.5	V
SYNC Input Bias Current		T_A = +25°C	-1		+1	µA

Electrical Characteristics (T_A = -40°C to +105°C)

(*Standard Application Circuit*, V_{INLDO} = 12V, V_{INA} = V_{INBC} = V_{DD} = V_{CC} = V_{BYP} = V_{CSPA} = V_{CSNA} = 5V, V_{IND} = 1.8V, $V_{\overline{SHDN}}$ = V_{ONA} = V_{ONB} = V_{ONC} = V_{OND} = 5V, I_{REF} = I_{LDO5} = I_{OUTD} = no load, FREQ = GND, $\overline{UP}$/DN = V_{CC}, **T_A = -40°C to +105°C**.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage Range		$\overline{UP}$/DN = LDO5, INLDO, INA = LDO5	5.5		24	V
INA Undervoltage Threshold	$V_{INA(UVLO)}$	$\overline{UP}$/DN = LDO5, INA = V_{CC}, rising edge, hysteresis = 160mV	3.9		4.5	V
INBC Input Voltage Range			2.3		5.5	V
SUPPLY CURRENTS						
V_{INLDO} Shutdown Supply Current	$I_{IN(\overline{SHDN})}$	V_{INLDO} = 5.5V to 38V, $\overline{SHDN}$ = GND			15	µA
V_{INLDO} Suspend Supply Current	$I_{IN(SUS)}$	V_{INLDO} = 5.5V to 38V, ON_ = GND, $\overline{SHDN}$ = INLDO			80	µA
INA Shutdown Current	I_{INA}	$\overline{SHDN}$ = ONA = ONB = ONC = OND = GND, $\overline{UP}$/DN = V_{CC}			10	µA
V_{CC} Supply Current Main Step-Down Only		ONA = V_{CC}, ONB = ONC = OND = GND; does not include switching losses, measured from V_{CC}			350	µA
V_{CC} Supply Current Main Step-Down and Regulator B		ONA = ONB = V_{CC}, ONC = OND = GND; does not include switching losses, measured from V_{CC}			400	µA
V_{CC} Supply Current Main Step-Down and Regulator C		ONA = ONC = V_{CC}, ONB = OND = GND, does not include switching losses, measured from V_{CC}			400	µA
INA Supply Current (Step-Down)	I_{INA}	ONA = V_{CC}, $\overline{UP}$/DN = V_{CC} (step-down)			75	µA
5V LINEAR REGULATOR						
LDO5 Output Voltage	V_{LDO5}	V_{INLDO} = 5.5V to 38V, I_{LDO5} = 0 to 50mA, BYP = GND	4.75		5.25	V
LDO5 Short-Circuit Current Limit		LDO5 = BYP = GND, V_{INLDO} = 5.5V	55			mA
1.25V REFERENCE						
Reference Output Voltage	V_{REF}	No load	1.237		1.263	V
Reference Load Regulation	ΔV_{REF}	I_{REF} = -1µA to +50µA			12	mV
OSCILLATOR						
Oscillator Frequency	f_{OSC}	FREQ = GND	0.9		1.1	MHz
Maximum Duty Cycle (All Switching Regulators)	D_{MAX}		89			%

Electrical Characteristics (T_A = -40°C to +105°C) (continued)

(*Standard Application Circuit*, V_{INLDO} = 12V, V_{INA} = V_{INBC} = V_{DD} = V_{CC} = V_{BYP} = V_{CSPA} = V_{CSNA} = 5V, V_{IND} = 1.8V, $V_{\overline{SHDN}}$ = V_{ONA} = V_{ONB} = V_{ONC} = V_{OND} = 5V, I_{REF} = I_{LDO5} = I_{OUTD} = no load, FREQ = GND, $\overline{UP}$/DN = V_{CC}, **T_A = -40°C to +105°C**.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
REGULATOR A (Main Step-Down)						
Output Voltage Adjust Range		Step-down configuration ($\overline{UP}$/DN = V_{CC})	1.0		V_{CC} + 0.3V	V
FBA Regulation Voltage	V_{FBA}	Step-down configuration, V_{CSPA} - V_{CSNA} = 0mV, 90% duty cycle	0.963		1.008	V
FBA Regulation Voltage (Overload)	V_{FBA}	Step-down configuration ($\overline{UP}$/DN = V_{CC}), V_{CSPA} - V_{CSNA} = 0 to 20mV, 90% duty cycle	0.925		1.008	V
FBA Line Regulation		Step-down ($\overline{UP}$/DN = V_{CC})	10		33	mV
Current-Sense Input Common-Mode Range	V_{CSA}		0		V_{CC} + 0.3V	V
Current-Limit Threshold (Positive)	V_{ILIMA}		17		23	mV
REGULATOR B (Internal 3A Step-Down Converter)						
FBB Regulation Voltage	V_{FBB}	I_{LXB} = 0A, 0% duty cycle (Note 2)	0.742		0.766	V
FBB Regulation Voltage (Overload)	V_{FBB}	I_{LXB} = 0 to 2.5A , 0% duty cycle (Note 2)	0.715		0.766	V
FBB Line Regulation			6		12	mV
LXB Peak Current Limit	I_{PKB}		2.7		4.2	A
REGULATOR C (Internal 5A Step-Down Converter)						
FBC Regulation Voltage	V_{FBC}	I_{LXC} = 0A, 0% duty cycle (Note 2)	0.742		0.766	V
FBC Regulation Voltage (Overload)	V_{FBC}	I_{LXC} = 0 to 4A, 0% duty cycle (Note 2)	0.705		0.766	V
FBC Line Regulation			11		20	mV
LXC Peak Current Limit	I_{PKC}		5.0		6.5	A
REGULATOR D (Source/Sink Linear Regulator and VTTR Buffer)						
IND Input Voltage Range	V_{IND}		1		2.8	V
IND Supply Current		OND = V_{CC}			70	µA
REFIND Input Range			0.5		1.5	V
OUTD Output Voltage Range	V_{OUTD}		0.5		1.5	V
FBD Output Accuracy	V_{FBD}	V_{FBD} with respect to V_{REFIND}, OUTD = FBD, I_{OUTD} = +50µA (source load)	-12		0	mV
FBD Output Accuracy	V_{FBD}	V_{FBD} with respect to V_{REFIND}, OUTD = FBD, I_{OUTD} = -50µA (sink load)	0		+12	mV
FBD Load Regulation		I_{OUTD} = ±1A	-20			mV/A
OUTD Linear-Regulator Current Limit		Source load	+2		+4	A
OUTD Linear-Regulator Current Limit		Sink load	-2		-4	A
Internal MOSFET On-Resistance		High-side on-resistance			300	mΩ
Internal MOSFET On-Resistance		Low-side on-resistance			475	mΩ
VTTR Output Accuracy		REFIND to VTTR, I_{VTTR} = ±3mA	-20		+20	mV

Electrical Characteristics (T_A = -40°C to +105°C) (continued)

(*Standard Application Circuit*, V_{INLDO} = 12V, V_{INA} = V_{INBC} = V_{DD} = V_{CC} = V_{BYP} = V_{CSPA} = V_{CSNA} = 5V, V_{IND} = 1.8V, $V_{\overline{SHDN}}$ = V_{ONA} = V_{ONB} = V_{ONC} = V_{OND} = 5V, I_{REF} = I_{LDO5} = I_{OUTD} = no load, FREQ = GND, $\overline{UP}$/DN = V_{CC}, **T_A = -40°C to +105°C**.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
FAULT PROTECTION						
SMPS POK and Fault Thresholds		Upper threshold rising edge, hysteresis = 50mV	8		16	%
		Lower threshold falling edge, hysteresis = 50mV	-16		-8	
VTT LDO POKD and Fault Threshold		Upper threshold rising edge, hysteresis = 50mV	6		16	%
		Lower threshold falling edge, hysteresis = 50mV	-16		-6	
POK Output Low Voltage	V_{POK}	I_{SINK} = 3mA			0.4	V
GENERAL LOGIC LEVELS						
$\overline{SHDN}$ Input Logic Threshold		Hysteresis = 20mV	0.5		1.6	V
ON_ Input Logic Threshold		Hysteresis = 170mV	0.5		1.6	V
$\overline{UP}$/DN Input Logic Threshold			0.5		1.6	V
FREQ Input Voltage Levels		High (V_{CC})	V_{CC} - 0.4V			V
		Unconnected/REF	1.65		3.8	
		Low (GND)			0.5	
SYNC Input Logic Threshold			1.5		3.5	V

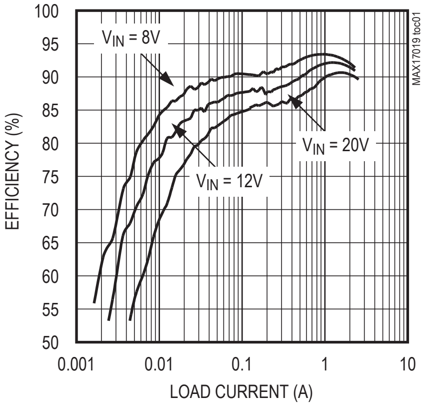
Note 1: Limits are 100% production tested at T_A = +25°C. Maximum and minimum limits are guaranteed by design and characterization.

Note 2: Regulation voltage tested with slope compensation. Typical value is equivalent to 0% duty cycle. In real applications, the regulation voltage is higher due to the line regulation times the duty cycle.

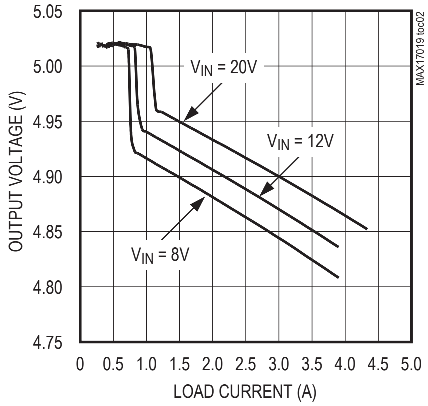
Typical Operating Characteristics

(T_A = +25°C, *Standard Application Circuit*, unless otherwise noted.)

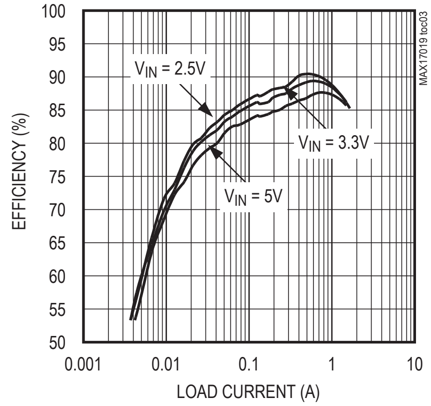
SMPS REGULATOR A EFFICIENCY vs. LOAD CURRENT



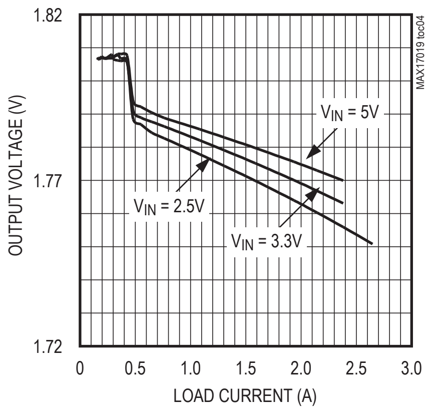
SMPS REGULATOR A OUTPUT VOLTAGE vs. LOAD CURRENT



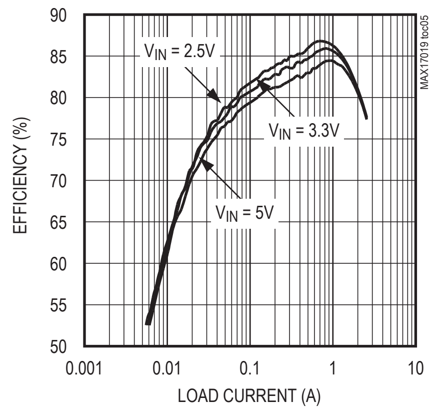
SMPS REGULATOR B EFFICIENCY vs. LOAD CURRENT



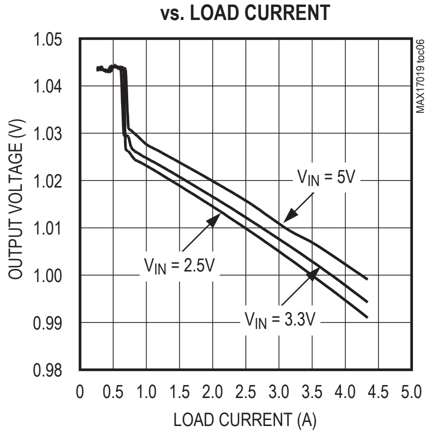
SMPS REGULATOR B OUTPUT VOLTAGE vs. LOAD CURRENT



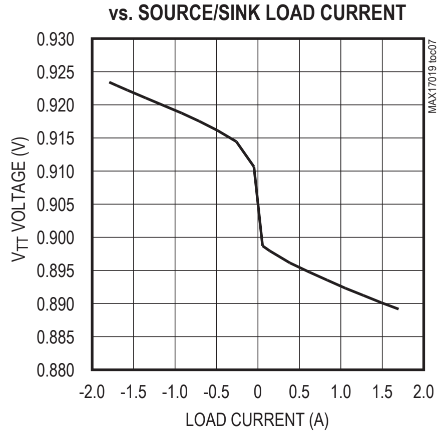
SMPS REGULATOR C EFFICIENCY vs. LOAD CURRENT



SMPS REGULATOR C OUTPUT VOLTAGE vs. LOAD CURRENT



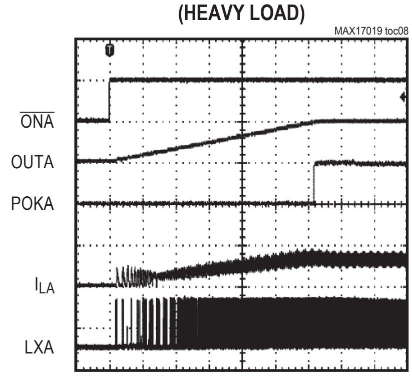
REGULATOR D VOLTAGE vs. SOURCE/SINK LOAD CURRENT



Typical Operating Characteristics (continued)

(T_A = +25°C, *Standard Application Circuit*, unless otherwise noted.)

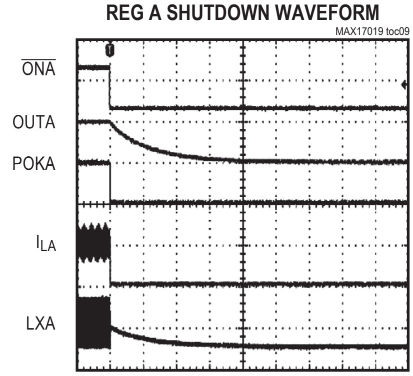
REG A STARTUP WAVEFORM (HEAVY LOAD)



400µs/div

$\overline{\text{ONA}}$: 5V/div
OUTA: 5V/div
POKA: 5V/div
I_{LA}: 5A/div
LXA: 10V/div
R_{LOAD} = 1.6Ω

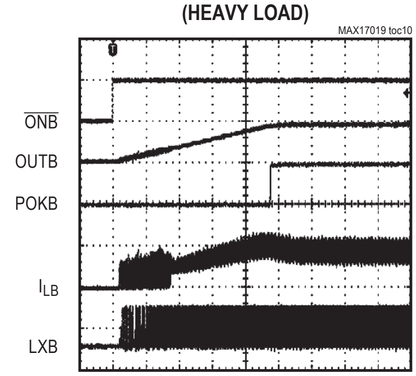
REG A SHUTDOWN WAVEFORM



400µs/div

$\overline{\text{ONA}}$: 5V/div
OUTA: 5V/div
POKA: 5V/div
I_{LA}: 5A/div
LXA: 10V/div
R_{LOAD} = 2.5Ω

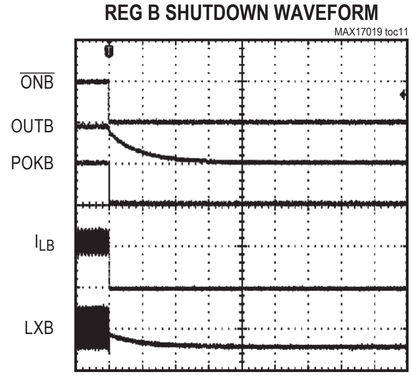
REG B STARTUP WAVEFORM (HEAVY LOAD)



400µs/div

$\overline{\text{ONB}}$: 5V/div
OUTB: 2V/div
POKB: 5V/div
I_{LB}: 2A/div
LXB: 5V/div
R_{LOAD} = 1.01Ω

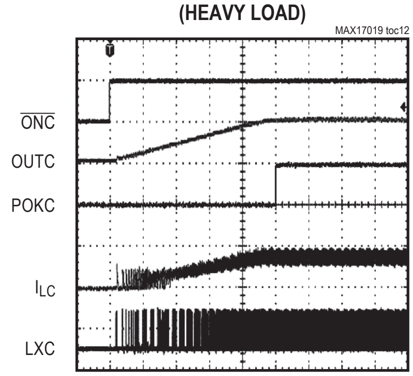
REG B SHUTDOWN WAVEFORM



400µs/div

$\overline{\text{ONB}}$: 5V/div
OUTB: 2V/div
POKB: 5V/div
I_{LB}: 2A/div
LXB: 5V/div
R_{LOAD} = 0.8Ω

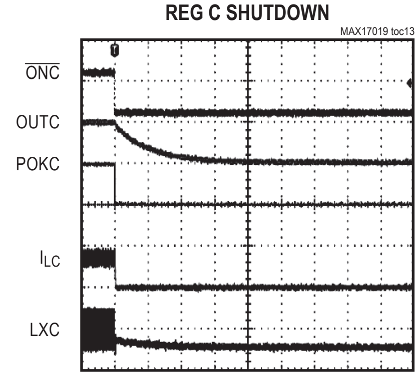
REG C STARTUP WAVEFORM (HEAVY LOAD)



400µs/div

$\overline{\text{ONC}}$: 5V/div
OUTC: 1V/div
POKC: 5V/div
I_{LC}: 5A/div
LXC: 5V/div
R_{LOAD} = 0.25Ω

REG C SHUTDOWN



100µs/div

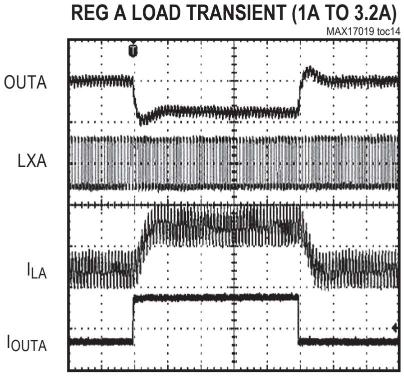
$\overline{\text{ONC}}$: 5V/div
OUTC: 1V/div
POKC: 5V/div
I_{LC}: 5A/div
LXC: 5V/div
R_{LOAD} = 0.25Ω

Typical Operating Characteristics (continued)

(T_A = +25°C, *Standard Application Circuit*, unless otherwise noted.)

REG A LOAD TRANSIENT (1A TO 3.2A)

MAX17019 toc14



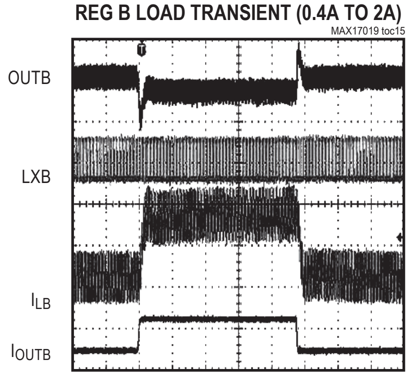
20µs/div

OUTA: 100mV/div
LXA: 10V/div
I_{LA}: 2A/div
I_{OUTA}: 2A/div

V_{INA} = 12V, LOAD TRANSIENT IS FROM 1A TO 3.2A

REG B LOAD TRANSIENT (0.4A TO 2A)

MAX17019 toc15



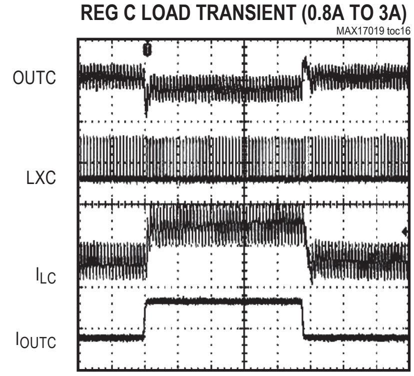
20µs/div

OUTB: 50mV/div
LXB: 5V/div
I_{LB}: 1A/div
I_{OUTB}: 2A/div

V_{INBC} = 5V, 0.4A TO 2.0A LOAD TRANSIENT

REG C LOAD TRANSIENT (0.8A TO 3A)

MAX17019 toc16



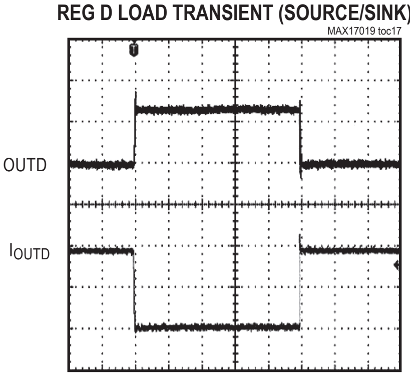
20µs/div

OUTC: 50mV/div
LXC: 5V/div
I_{LC}: 2A/div
I_{OUTC}: 2A/div

V_{INBC} = 5V, 0.8A TO 3.0A LOAD TRANSIENT

REG D LOAD TRANSIENT (SOURCE/SINK)

MAX17019 toc17



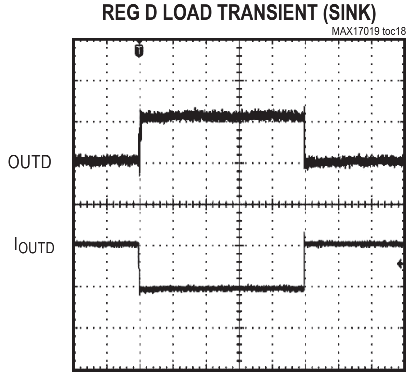
20µs/div

OUTD: 20mV/div
I_{OUTD}: 1A/div

V_{IND} = 1.8V, V_{REFIND} = 0.9V, C_{OUT} = 2 x 10µF, LOAD TRANSIENT IS FROM 1A SOURCING TO 1A SINKING

REG D LOAD TRANSIENT (SINK)

MAX17019 toc18



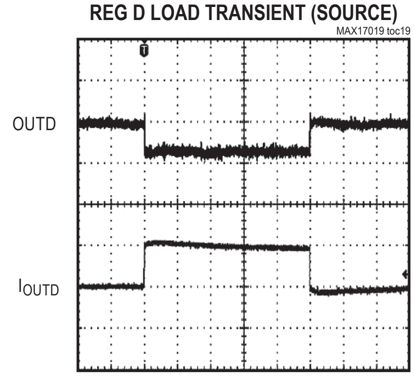
20µs/div

OUTD: 10mV/div
I_{OUTD}: 1A/div

V_{IND} = 1.8V, V_{REFIND} = 0.9V, C_{OUT} = 2 x 10µF, LOAD TRANSIENT IS FROM 0 TO 1A SINKING

REG D LOAD TRANSIENT (SOURCE)

MAX17019 toc19

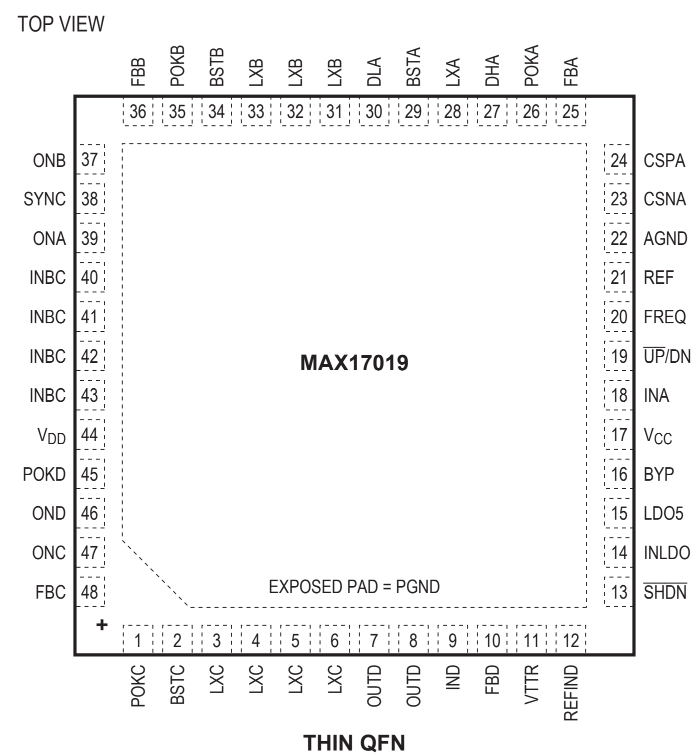


20µs/div

OUTD: 10mV/div
I_{OUTD}: 1A/div

V_{IND} = 1.8V, V_{REFIND} = 0.9V, C_{OUT} = 2 x 10µF, LOAD TRANSIENT IS FROM 0 TO 1A SOURCING

Pin Configuration



Pin Description

PIN	NAME	FUNCTION
1	POKC	Open-Drain Power-Good Output for the Internal 5A Step-Down Converter. POKC is low if FBC is more than 12% (typ) above or below the nominal 0.75V feedback regulation threshold. POKC is held low during startup and in shutdown. POKC becomes high impedance when FBC is in regulation.
2	BSTC	Boost Flying Capacitor Connection for the Internal 5A Step-Down Converter. The MAX17019 includes an internal boost switch/diode connected between V_{DD} and BSTC. Connect to an external capacitor as shown in the *Standard Application Circuit*.
3–6	LXC	Inductor Connection for the Internal 5A Step-Down Converter. Connect LXC to the switched side of the inductor.
7, 8	OUTD	Source/Sink Linear-Regulator Output. Bypass OUTD with 2x 10µF or greater ceramic capacitors to ground. Dropout needs additional output capacitance (see the *VTT LDO Output Capacitor Selection (C_{OUTD})* section).
9	IND	Source/Sink Linear-Regulator Input. Bypass IND with a 10µF or greater ceramic capacitor to ground.
10	FBD	Feedback Input for the Internal Source/Sink Linear Regulator. FBD tracks and regulates to the REFIND voltage.
11	VTTR	Ouput of Reference Buffer. Bypass with 0.22µF for ±3mA of output current.
12	REFIND	Dynamic Reference Input Voltage for the Source/Sink Linear Regulator and the Reference Buffer. The linear-regulator feedback threshold (FBD) tracks the REFIND voltage.

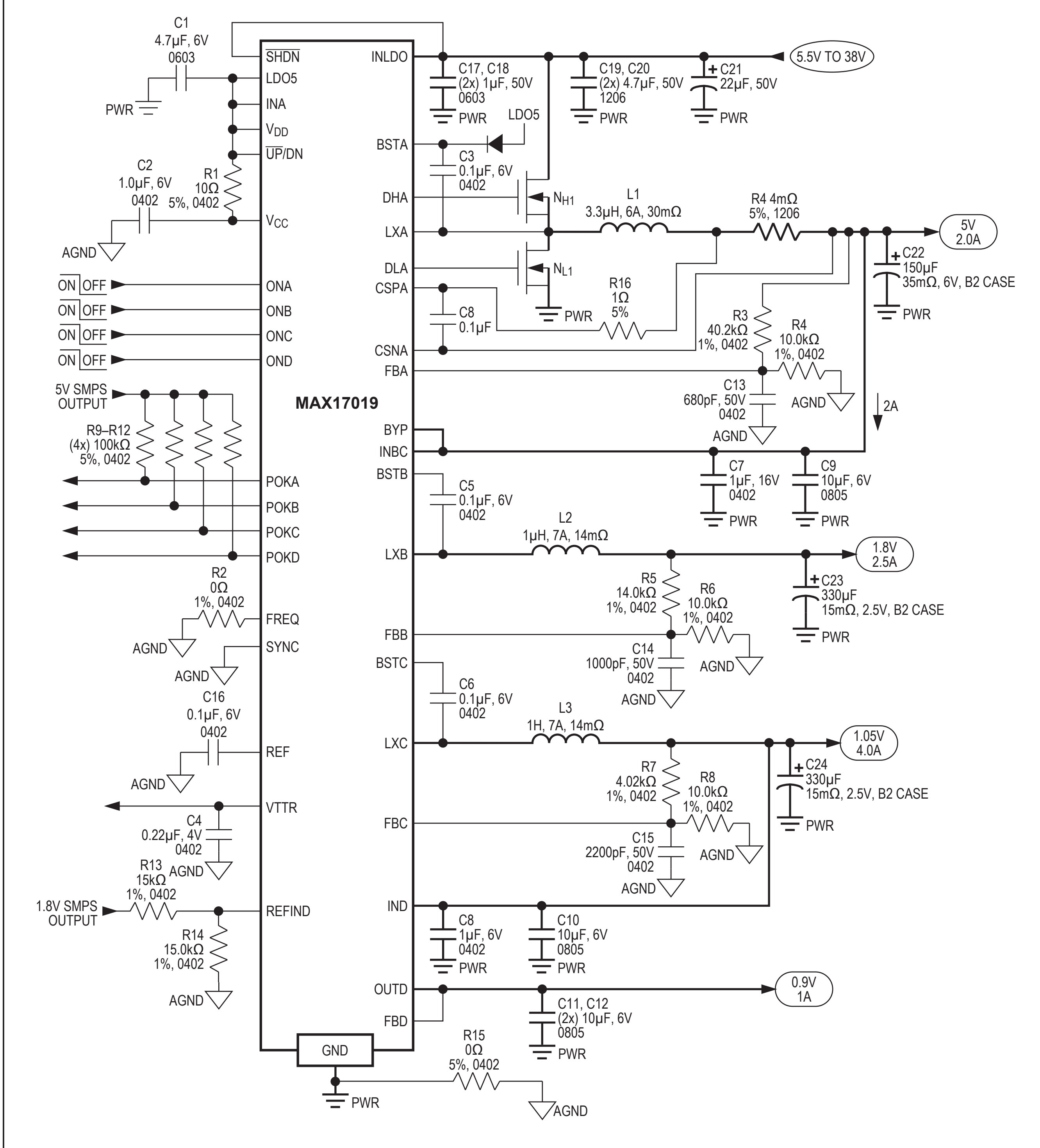
Pin Description (continued)

PIN	NAME	FUNCTION
13	$\overline{SHDN}$	Shutdown Control Input. The device enters its 5µA supply current shutdown mode if $V_{\overline{SHDN}}$ is less than the $\overline{SHDN}$ input falling-edge trip level and does not restart until $V_{\overline{SHDN}}$ is greater than the $\overline{SHDN}$ input rising-edge trip level. Connect $\overline{SHDN}$ to V_{INLDO} for automatic startup of LDO5.
14	INLDO	Input of the Startup Circuitry and the LDO5 Internal 5V Linear Regulator. Bypass to GND with a 0.1µF or greater ceramic capacitor close to the controller. In the single-cell step-up applications, the 5V linear regulator is no longer necessary for the 5V bias supply. Connect BYP and INLDO to the system's 5V supply to effectively disable the linear regulator.
15	LDO5	5V Internal Linear-Regulator Output. Bypass with 4.7µF or greater ceramic capacitor. The 5V linear regulator provides the bias power for the gate drivers (V_{DD}) and analog control circuitry (V_{CC}). The linear regulator sources up to 50mA (max guaranteed). When BYP exceeds 4.65V (typ), the MAX17019 bypasses the linear regulator through a 1.5Ω bypass switch. When the linear regulator is bypassed, LDO5 supports loads up to 100mA. In the single-cell step-up applications, the 5V linear regulator is no longer necessary for the 5V bias supply. Bypass $\overline{SHDN}$ to ground and leave LDO5 unconnected. Connect BYP and INLDO to effectively disable the linear regulator.
16	BYP	Linear-Regulator Bypass Input. When BYP exceeds 4.65V, the controller shorts LDO5 to BYP through a 1.5Ω bypass switch and disables the linear regulator. When BYP is low, the linear regulator remains active. The BYP input also serves as the VTTR buffer supply, allowing VTTR to remain active even when the source/sink linear regulator (OUTD) has been disabled under system standby/suspend conditions. In the single-cell step-up applications, the 5V linear regulator is no longer necessary for the 5V bias supply. Bypass LDO5 to ground with a 1µF capacitor and leave this output unconnected. Connect BYP and INLDO to the system's 5V supply to effectively disable the linear regulator.
17	V_{CC}	5V Analog Bias Supply. V_{CC} powers all the analog control blocks (error amplifiers, current-sense amplifiers, fault comparators, etc.) and control logic. Connect V_{CC} to the 5V system supply with a series 10Ω resistor, and bypass to analog ground using a 1µF or greater ceramic capacitor.
18	INA	Input to the Circuit in Reg A in Boost Mode. Connect INA to LDO5 in step-down mode ($\overline{UP}$/DN = V_{CC}).
19	$\overline{UP}$/DN	Converter Configuration Selection Input for Regulator A. When $\overline{UP}$/DN is pulled high ($\overline{UP}$/DN = V_{CC}), regulator A operates as a step-down converter (*Standard Application Circuit*). When $\overline{UP}$/DN is pulled low ($\overline{UP}$/DN = GND), regulator A operates as a low-voltage step-up converter. (Refer to the MAX17017 data sheet for step-up configuration.)
20	FREQ	Trilevel Oscillator Frequency Selection Input: FREQ = V_{CC}: RegA = 250kHz, RegB = 500kHz, RegC = 250kHz FREQ = REF: RegA = 375kHz, RegB = 750kHz, RegC = 375kHz FREQ = GND: RegA = 500kHz, RegB = 1MHz, RegC = 500kHz
21	REF	1.25V Reference-Voltage Output. Bypass REF to analog ground with a 0.1µF ceramic capacitor. The reference sources up to 50µA for external loads. Loading REF degrades output voltage accuracy according to the REF load-regulation error. The reference shuts down when the system pulls $\overline{SHDN}$ low in buck mode ($\overline{UP}$/DN = GND).
22	AGND	Analog Ground
23	CSNA	Negative Current-Sense Input for the Main Switching Regulator. Connect to the negative terminal of the current-sense resistor. Due to the CSNA bias current requirements, limit the series impedance to less than 10Ω.
24	CSPA	Positive Current-Sense Input for the Main Switching Regulator. Connect to the positive terminal of the current-sense resistor. Due to the CSPA bias current requirements, limit the series impedance to less than 10Ω.
25	FBA	Feedback Input for the Main Switching Regulator. FBA regulates to 1.0V.

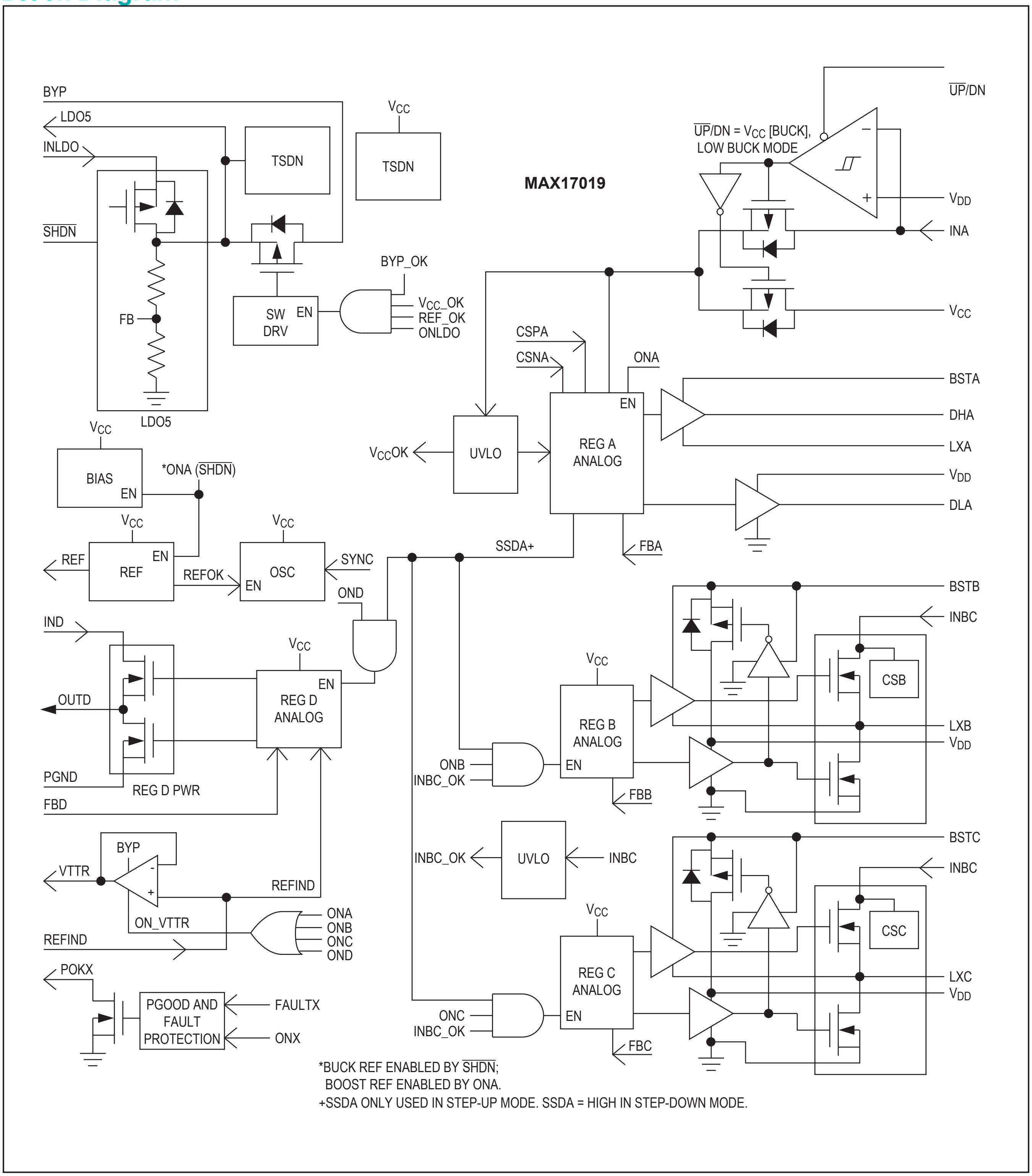
Pin Description (continued)

PIN	NAME	FUNCTION
26	POKA	Open-Drain Power-Good Output for the Main Switching Regulator. POKA is low if FBA is more than 12% (typ) above or below the nominal 1.0V feedback regulation point. POKA is held low during soft-start and in shutdown. POKA becomes high impedance when FBA is in regulation.
27	DHA	High-Side Gate-Driver Output for the Main Switching Regulator. DHA swings from LXA to BSTA.
28	LXA	Inductor Connection of Converter A. Connect LXA to the switched side of the inductor.
29	BSTA	Boost Flying Capacitor Connection of Converter A. The MAX17019 needs an external boost switch/diode connected between V_{DD} and BSTA. Connect to an external capacitor as shown in the *Standard Application Circuit*.
30	DLA	Low-Side Gate-Driver Output for the Main Switching Regulator. DLA swings from GND to V_{DD}.
31, 32, 33	LXB	Inductor Connection for the Internal 3A Step-Down Converter. Connect LXB to the switched side of the inductor.
34	BSTB	Boost Flying Capacitor Connection for the Internal 3A Step-Down Converter. The MAX17019 includes an internal boost switch/diode connected between V_{DD} and BSTB. Connect to an external capacitor as shown in the *Standard Application Circuit*.
35	POKB	Open-Drain Power-Good Output for the Internal 3A Step-Down Converter. POKB is low if FBB is more than 12% (typ) above or below the nominal 0.75V feedback-regulation threshold. POKB is held low during soft-start and in shutdown. POKB becomes high impedance when FBB is in regulation.
36	FBB	Feedback Input for the Internal 3A Step-Down Converter. FBB regulates to 0.75V.
37	ONB	Switching Regulator B Enable Input. When ONB is pulled low, LXB is high impedance. When ONB is driven high, the controller enables the 3A internal switching regulator.
38	SYNC	External Synchronization Input. Used to override the internal switching frequency.
39	ONA	Switching Regulator A Enable Input. When ONA is pulled low, DLA and DHA are pulled low. When ONA is driven high, the controller enables the step-up/step-down converter.
40–43	INBC	Input for Regulators B and C. **Power INBC from a 2.5V to 5.5V supply**. Internally connected to the drain of the high-side MOSFETs for both regulator B and regulator C. Bypass to PGND with 2x 10μF or greater ceramic capacitors to support the RMS current.
44	V_{DD}	5V Bias Supply Input for the Internal Switching Regulator Drivers. Bypass with a 1μF or greater ceramic capacitor. Provides power for the BSTB and BSTC driver supplies.
45	POKD	Open-Drain Power-Good Output for the Internal Source/Sink Linear Regulator. POKD is low if FBD is more than 10% (typ) above or below the REFIND regulation threshold. POKD is held low during soft-start and in shutdown. POKD becomes high impedance when FBD is in regulation.
46	OND	Source/Sink Linear Regulator (Regulator D) and Reference Buffer Enable Input. When OND is pulled low, OUTD is high impedance. When OND is driven high, the controller enables the source/sink linear regulator.
47	ONC	Switching Regulator C Enable Input. When ONC is pulled low, LXC is high impedance. When ONC is driven high, the controller enables the 5A internal switching regulator.
48	FBC	Feedback Input for the Internal 5A Step-Down Converter. FBC regulates to 0.75V.
EP	PGND	**Power Ground. The source of the low-side MOSFETs (REG B and REG C), the drivers for all switching regulators, and the sink MOSFET of the VTT LDO are all internally connected to the exposed pad. Connect the exposed backside pad to system power ground planes through multiple vias.**

Standard Application Circuit



Block Diagram



Detailed Description

The MAX17019 standard application circuit (*Standard Application Circuit*) provides a 5V/5A_{P-P} main stage, a 1.8V/3A_{P-P} VDDQ and 0.9A/2A VTT outputs for DDR, and a 1.05V/5A_{P-P} chipset supply.

The MAX17019 supports four power outputs—one high-voltage step-down controller, two internal MOSFET step-down switching regulators, and one high-current source/sink linear regulator. The step-down switching regulators use a current-mode fixed-frequency architecture compensated by the output capacitance. An internal 50mA 5V linear regulator provides the bias supply and driver supplies, allowing the controller to power up from input supplies greater than 5.5V.

Fixed 5V Linear Regulator (LDO5)

An internal linear regulator produces a preset 5V lowcurrent output from INLDO. LDO5 powers the gate drivers for the external MOSFETs, and provides the bias supply required for the SMPS analog controller, reference, and logic blocks. LDO5 supplies at least 50mA for external and internal loads, including the MOSFET gate drive, which typically varies from 5mA to 15mA per switching regulator, depending on the switching frequency. Bypass LDO5 with a 4.7µF or greater ceramic capacitor to guarantee stability under the fullload conditions.

The MAX17019 switch-mode step-down switching regulators require a 5V bias supply in addition to the mainpower input supply. This 5V bias supply is generated by the controller's internal 5V linear regulator (LDO5). This bootstrappable LDO allows the controller to power up independently. The gate driver V_{DD} input supply is typically connected to the fixed 5V linear regulator output (LDO5). Therefore, the 5V LDO supply must provide LDO5 (PWM controller) and the gatedrive power during power-up.

LDO5 Bootstrap Switchover

When the bypass input (BYP) exceeds the LDO5 bootstrap-switchover threshold for more than 500µs, an internal 1.5Ω (typ) p-channel MOSFET shorts BYP to LDO5, while simultaneously disabling the LDO5 linear regulator. This bootstraps the controller, allowing power for the internal circuitry and external LDO5 loading to be generated by the output of a 5V switching regulator. Bootstrapping reduces power dissipation due to driver and quiescent losses by providing power from a switch-mode source, rather than from a much-less-efficient linear regulator. The current capability increases from 50mA to 100mA when the LDO5 output is switched over to BYP. When BYP drops below the bootstrap threshold, the controller immediately disables the bootstrap switch and reenables the 5V LDO.

Reference (REF)

The 1.25V reference is accurate to ±1% over temperature and load, making REF useful as a precision system reference. Bypass REF to GND with a 0.1µF or greater ceramic capacitor. The reference sources up to 50µA and sinks 5µA to support external loads. If highly accurate specifications are required for the main SMPS output voltages, the reference should not be loaded. Loading the reference slightly reduces the output voltage accuracy because of the reference load-regulation error.

SMPS Detailed Description

Fixed-Frequency, Current-Mode PWM Controller

The heart of each current-mode PWM controller is a multi-input, open-loop comparator that sums multiple signals: the output voltage-error signal with respect to the reference voltage, the current-sense signal, and the slope compensation ramp (Figure 1). The MAX17019 uses a direct-summing configuration, approaching ideal cycle-to-cycle control over the output voltage without a traditional error amplifier and the phase shift associated with it.

Frequency Selection (FREQ)

The FREQ input selects the PWM mode switching frequency. Table 1 shows the switching frequency based on the FREQ connection. High-frequency (FREQ = GND) operation optimizes the application for the smallest component size, trading off efficiency due to higher switching losses. This might be acceptable in ultraportable devices where the load currents are lower. Low-frequency (FREQ = 5V) operation offers the best overall efficiency at the expense of component size and board space.

Light-Load Operation Control

The MAX17019 uses a light-load pulse-skipping operating mode for all switching regulators. The switching regulators turn off the low-side MOSFETs when the current sense detects zero inductor current. This keeps the inductor from discharging the output capacitors and forces the switching regulator to skip pulses under light-load conditions to avoid overcharging the output.

Idle-Mode Current-Sense Threshold

When pulse-skipping mode is enabled, the on-time of the step-down controller terminates when the output voltage exceeds the feedback threshold and when the current-sense voltage exceeds the idle-mode current-sense threshold. Under light-load conditions, the ontime duration depends solely on the idle-mode current-sense threshold. This forces the controller to source a minimum

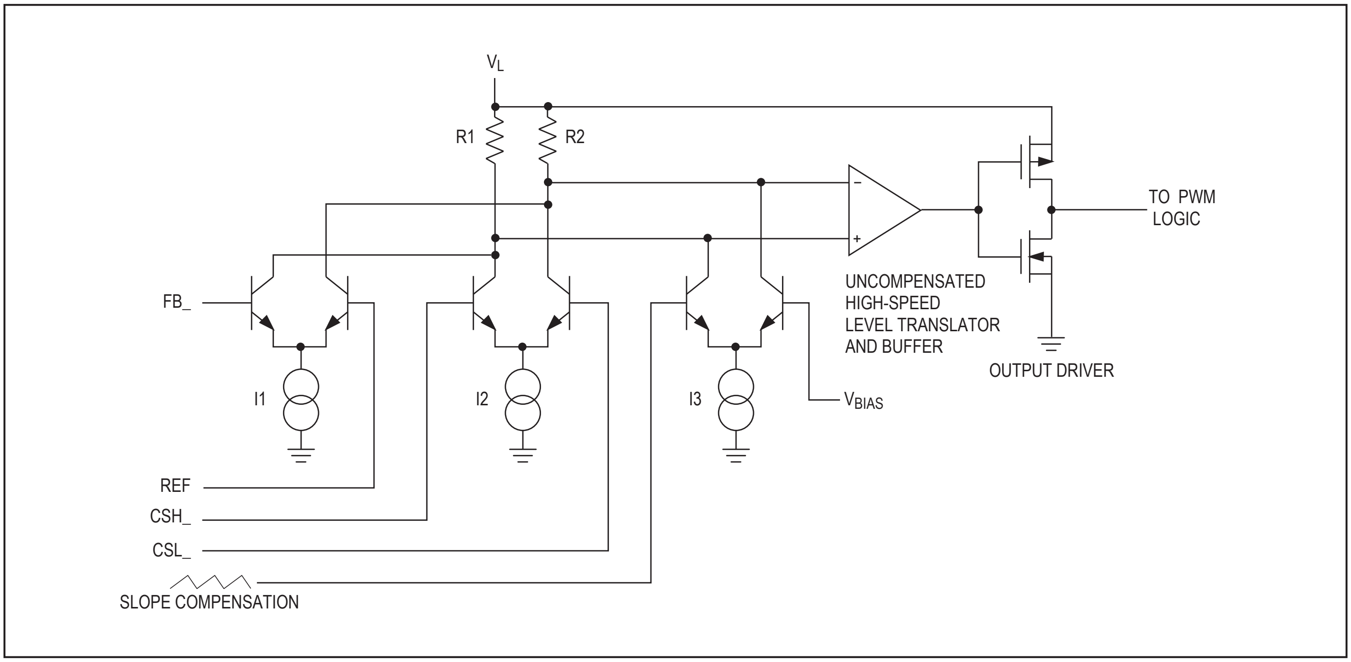


Figure 1. PWM Comparator Functional Diagram

Table 1. FREQ Table

PIN SELECT	REG A AND REG C			REG B		
	SWITCHING FREQUENCY	**SOFT-START TIME**	**STARTUP BLANKING TIME**	**SWITCHING FREQUENCY**	**SOFT-START TIME**	**STARTUP BLANKING TIME**
	f_{SWA} AND f_{SWC}	**REG A: 1200/f_{SWA} REG C: 900/f_{SWC}**	**1500/f_{SWA}**	**f_{SWB}**	**1800/f_{SWB}**	**3000/f_{SWB}**
LDO5	250kHz	REG A: 4.8ms REG C: 3.6ms	6ms	**500kHz**	3.6ms	6ms
REF	375kHz	REG A: 3.2ms REG C: 2.4ms	4ms	**750kHz**	2.4ms	4ms
GND	500kHz	REG A: 2.4ms REG C: 1.8ms	3ms	**1MHz**	1.8ms	3ms
SYNC	0.5 x f_{SYNC}	—	—	f_{SYNC}	—	—

amount of power with each cycle. To avoid overcharging the output, another on-time cannot begin until the output voltage drops below the feedback threshold. Since the zero-crossing comparator prevents the switching regulator from sinking current, the MAX17019 switching regulators must skip pulses. Therefore, the controller regulates the valley of the output ripple under light-load conditions.

Automatic Pulse-Skipping Crossover

In skip mode, an inherent automatic switchover to PFM takes place at light loads. This switchover is affected by a comparator that truncates the low-side switch on-time at the inductor current's zero crossing. The zero-crossing comparator senses the inductor current during the offtime. For regulator A, once V_{CSPA} - V_{CSNA} drops below the 1mV zero-crossing current-sense threshold, the comparator turns off the low-side MOSFET (DLA pulled low). For regulators B and C, once the current through the lowside MOSFET drops below 100mA, the zero-crossing comparator turns off the low-side MOSFET.

The minimum idle-mode current requirement causes the threshold between pulse-skipping PFM operation and constant PWM operation to coincide with the boundary between continuous and discontinuous inductor-current operation (also known as the critical conduction point). The load-current level at which PFM/PWM crossover occurs ($I_{LOAD(SKIP)}$) is equivalent to half the idle-mode current threshold (see the *Electrical Characteristics* table for the idle-mode thresholds of each regulator). The switching waveforms can appear noisy and asynchronous when light loading causes pulse-skipping operation, but this is a normal operating condition that results in high light-load efficiency. Trade-offs in PFM noise vs. light-load efficiency are made by varying the inductor value. Generally, low inductor values produce a broader efficiency vs. load curve, while higher values result in higher full-load efficiency (assuming that the coil resistance remains fixed) and less output voltage ripple. Penalties for using higher inductor values include larger physical size and degraded load-transient response (especially at low input-voltage levels).

SMPS POR, UVLO, and Soft-Start

Power-on reset (POR) occurs when V_{CC} rises above approximately 1.9V, resetting the undervoltage, overvoltage, and thermal-shutdown fault latches. The POR circuit also ensures that the low-side drivers are pulled low until the SMPS controllers are activated. The V_{CC} input undervoltage lockout (UVLO) circuitry prevents the switching regulators from operating if the 5V bias supply (V_{CC} and V_{DD}) is below its 4.2V UVLO threshold.

Regulator A Startup

Once the 5V bias supply rises above this input UVLO threshold and ONA is pulled high, the main step-down controller (regulator A) is enabled and begins switching. The internal voltage soft-start gradually increments the feedback voltage by 10mV every 12 switching cycles. Therefore, OUTA reaches its nominal regulation voltage $1200/f_{SWA}$ after regulator A is enabled (see the REG A Startup Waveform (Heavy Load) graph in the *Typical Operating Characteristics*).

Regulator B and C Startup

The internal step-down controllers start switching and the output voltages ramp up using soft-start. If the bias supply voltage drops below the UVLO threshold, the controller stops switching and disables the drivers (LX_becomes high impedance) until the bias supply voltage recovers.

Once the 5V bias supply and INBC rise above their respective input UVLO thresholds ($\overline{SHDN}$ must be pulled high to enable the reference), and ONB or ONC is pulled high, the respective internal step-down controller (regulator B or C) becomes enabled and begins switching. The internal voltage soft-start gradually increments the feedback voltage by 10mV every 24 switching cycles for regulator B or every 12 switching cycles for regulator C. Therefore, OUTB reaches its nominal regulation voltage $1800/f_{SWB}$ after regulator B is enabled, and OUTC reaches its nominal regulation voltage $900/f_{SWC}$ after regulator C is enabled (see the REG B Startup Waveform (Heavy Load) and REG C Startup Waveform (Heavy Load) graphs in the *Typical Operating Characteristics*).

SMPS Power-Good Outputs (POK)

POKA, POKB, and POKC are the open-drain outputs of window comparators that continuously monitor each output for undervoltage and overvoltage conditions. POK_ is actively held low in shutdown ($\overline{SHDN}$ = GND), standby (ONA = ONB = ONC = GND), and soft-start. Once the soft-start sequence terminates, POK_ becomes high impedance as long as the output remains within ±8% (min) of the nominal regulation voltage set by FB_. POK_ goes low once its corresponding output drops 12% (typ) below its nominal regulation point, an output overvoltage fault occurs, or the output is shut down. For a logic-level POK_ output voltage, connect an external pullup resistor between POK_ and LDO5. A 100kΩ pullup resistor works well in most applications.

SMPS Fault Protection

Output Overvoltage Protection (OVP)

If the output voltage rises above 112% (typ) of its nominal regulation voltage, the controller sets the fault latch, pulls POK_ low, shuts down the respective regulator, and immediately pulls the output to ground through its low-side MOSFET. Turning on the low-side MOSFET with 100% duty cycle rapidly discharges the output capacitors and clamps the output to ground. However, this commonly undamped response causes negative output voltages due to the energy stored in the output LC at the instant the OVP occurs. If the load cannot tolerate a negative voltage, place a power Schottky diode across the output to act as a reverse-polarity clamp. If the condition that caused the overvoltage persists (such as a shorted high-side MOSFET), the input source also fails (short-circuit fault). Cycle V_{CC} below 1V or toggle the respective enable input to clear the fault latch and restart the regulator.

Output Undervoltage Protection (UVP)

Each MAX17019 includes an output UVP circuit that begins to monitor the output once the startup blanking period has ended. If any output voltage drops below 88% (typ) of its nominal regulation voltage, the UVP protection immediately sets the fault latch, pulls the respective POK output low, forces the high-side and low-side MOSFETs into high-impedance states (DH = DL = low), and shuts down the respective regulator. Cycle V_{CC} below 1V or toggle the respective enable input to clear the fault latch and restart the regulator.

Thermal-Fault Protection

The MAX17019 features a thermal fault-protection circuit. When the junction temperature rises above +160°C, a thermal sensor activates the fault latch, pulls **all** $\overline{\text{POK}}$ outputs low, and shuts down **all** regulators. Toggle $\overline{\text{SHDN}}$ to clear the fault latch and restart the controllers after the junction temperature cools by 15°C.

VTT LDO Detailed Description

VTT LDO Power-Good Output (POKD)

POKD is the open-drain output of a window comparator that continuously monitors the VTT LDO output for undervoltage and overvoltage conditions. POKD is actively held low when the VTT LDO is disabled (OND = GND) and in soft-start. Once the startup blanking time expires, POKD becomes high impedance as long as the output remains within ±6% (min) of the nominal regulation voltage set by REFIND. POKD goes low once its corresponding output drops or rises 12% (typ) beyond its nominal regulation point or the output is shut down. For a logic-level POKD output voltage, connect an external pullup resistor between POKD and LDO5. A 100kΩ pullup resistor works well in most applications.

VTT LDO Fault Protection

LDO Output OVP

If the output voltage rises above 112% (typ) of its nominal regulation voltage, the controller sets the fault latch, pulls POKD low, shuts down the source/sink linear regulator, and immediately pulls the output to ground through its low-side MOSFET. Turning on the low-side MOSFET with 100% duty cycle rapidly discharges the output capacitors and clamps the output to ground. Cycle V_{CC} below 1V or toggle OND to clear the fault latch and restart the linear regulator.

LDO Output UVP

Each MAX17019 includes an output UVP circuit that begins to monitor the output once the startup blanking period has ended. If the source/sink LDO output voltage drops below 88% (typ) of its nominal REFIND regulation voltage for 5ms, the UVP sets the fault latch, pulls the POKD output low, forces the output into a highimpedance state, and shuts down the linear regulator. Cycle V_{CC} below 1V or toggle OND to clear the fault latch and restart the regulator.

SMPS Design Procedure (Step-Down Regulators)

Firmly establish the input voltage range and maximum load current before choosing a switching frequency and inductor operating point (ripple-current ratio). The primary design trade-off lies in choosing a good switching frequency and inductor operating point, and the following four factors dictate the rest of the design:

- **Input voltage range.** The maximum value ($V_{IN(MAX)}$) must accommodate the worst-case, high ACadapter voltage. The minimum value ($V_{IN(MIN)}$) must account for the lowest battery voltage after drops due to connectors, fuses, and battery selector switches. If there is a choice at all, lower input voltages result in better efficiency.
- **Maximum load current.** There are two values to consider. The peak load current ($I_{LOAD(MAX)}$) determines the instantaneous component stresses and filtering requirements and thus drives output capacitor selection, inductor saturation rating, and the design of the current-limit circuit. The continuous load current

(I_{LOAD}) determines the thermal stresses and thus drives the selection of input capacitors, MOSFETs, and other critical heat-contributing components.

- **Switching frequency.** This choice determines the basic trade-off between size and efficiency. The optimal frequency is largely a function of maximum input voltage, due to MOSFET switching losses that are proportional to frequency and V_{IN}^2.
- **Inductor operating point.** This choice provides trade-offs between size vs. efficiency and transient response vs. output ripple. Low inductor values provide better transient response and smaller physical size, but also result in lower efficiency, higher output ripple, and lower maximum load current due to increased ripple currents. The minimum practical inductor value is one that causes the circuit to operate at the edge of critical conduction (where the inductor current just touches zero with every cycle at maximum load). Inductor values lower than this grant no further size-reduction benefit. The optimum operating point is usually found between 20% and 50% ripple current. When pulse skipping (light loads), the inductor value also determines the loadcurrent value at which PFM/PWM switchover occurs.

Step-Down Inductor Selection

The switching frequency and inductor operating point determine the inductor value as follows:

$$L = \frac{V_{OUT}(V_{IN} - V_{OUT})}{V_{IN} f_{SW} I_{LOAD(MAX)} LIR}$$

Find a low-loss inductor having the lowest possible DC resistance that fits in the allotted dimensions. Most inductor manufacturers provide inductors in standard values, such as 1.0µH, 1.5µH, 2.2µH, 3.3µH, etc. Also look for nonstandard values, which can provide a better compromise in LIR across the input voltage range. If using a swinging inductor (where the no-load inductance decreases linearly with increasing current), evaluate the LIR with properly scaled inductance values. For the selected inductance value, the actual peak-to-peak inductor ripple current ($\Delta I_{INDUCTOR}$) is defined by:

$$\Delta I_{INDUCTOR} = \frac{V_{OUT}(V_{IN} - V_{OUT})}{V_{IN} f_{SW} L}$$

Ferrite cores are often the best choice, although soft saturating molded core inductors are inexpensive and can work well at 500kHz. The core must be large enough not to saturate at the peak inductor current (I_{PEAK}):

$$I_{PEAK} = I_{LOAD(MAX)} + \left(\frac{\Delta I_{INDUCTOR}}{2}\right)$$

SMPS Output Capacitor Selection

The output filter capacitor selection requires careful evaluation of several different design requirements—stability, transient response, and output ripple voltage—that place limits on the output capacitance and ESR. Based on these requirements, the typical application requires a low-ESR polymer capacitor (lower cost but higher output-ripple voltage) or bulk ceramic capacitors (higher cost but low output-ripple voltage).

SMPS Loop Compensation

Voltage positioning dynamically lowers the output voltage in response to the load current, reducing the loop gain. This reduces the output capacitance requirement (stability and transient) and output power dissipation requirements as well. The load-line is generated by sensing the inductor current through the high-side MOSFET on-resistance, and is internally preset to -5mV/A (typ) for regulator B and -7mV/A (typ) for regulator C. The loadline ensures that the output voltage remains within the regulation window over the full-load conditions.

The load line of the internal SMPS regulators also provides the AC ripple voltage required for stability. To maintain stability, the output capacitive ripple must be kept smaller than the internal AC ripple voltage, and crossover must occur before the Nyquist pole—(1 + duty)/($2f_{SW}$)—occurs. Based on these loop requirements, a minimum output capacitance can be determined from the following:

$$C_{OUT} > \left(\frac{1}{2 f_{SW} R_{DROOP}}\right)\left(\frac{V_{REF}}{V_{OUT}}\right)\left(1 + \frac{V_{OUT}}{V_{IN}}\right)$$

where R_{DROOP} is $2R_{SENSE}$ for regulator A, 5mV/A for regulator B, or 7mV/A for regulator C as defined in the *Electrical Characteristics* table, and f_{SW} is the switching frequency selected by the FREQ setting (see Table 1).

Additionally, an additional feedback pole—capacitor from FB to analog ground (C_{FB})—might be necessary to cancel the unwanted ESR zero of the output capacitor. In general, if the ESR zero occurs before the Nyquist pole, then canceling the ESR zero is recommended:

If:

$$ESR > \left(\frac{1+D}{4\pi f_{SW}C_{OUT}}\right)$$

Then:

$$C_{FB} > \left(\frac{C_{OUT}ESR}{R_{FB}}\right)$$

where R_{FB} is the parallel impedance of the FB resistive divider.

SMPS Output Ripple Voltage

With polymer capacitors, the effective series resistance (ESR) dominates and determines the output ripple voltage. The step-down regulator's output ripple voltage (V_{RIPPLE}) equals the total inductor ripple current ($\Delta I_{INDUCTOR}$) multiplied by the output capacitor's ESR. Therefore, the maximum ESR to meet the output ripple voltage requirement is:

$$R_{ESR} \le \left[\frac{V_{IN}f_{SW}L}{(V_{IN} - V_{OUT})V_{OUT}}\right]V_{RIPPLE}$$

where f_{SW} is the switching frequency. The actual capacitance value required relates to the physical case size needed to achieve the ESR requirement, as well as to the capacitor chemistry. Thus, polymer capacitor selection is usually limited by ESR and voltage rating rather than by capacitance value. Alternatively, combining ceramics (for the low ESR) and polymers (for the bulk capacitance) helps balance the output capacitance vs. output ripple-voltage requirements.

Internal SMPS Transient Response

The load-transient response depends on the overall output impedance over frequency, and the overall amplitude and slew rate of the load step. In applications with large, fast load transients (load step > 80% of full load and slew rate > 10A/µs), the output capacitor's high-frequency response—ESL and ESR—needs to be considered. To prevent the output voltage from spiking too low under a load-transient event, the ESR is limited by the following equation (ignoring the sag due to finite capacitance):

$$R_{ESR} \le \left(\frac{V_{STEP}}{\Delta I_{LOAD(MAX)}} - R_{PCB}\right)$$

where V_{STEP} is the allowed voltage drop, $\Delta I_{LOAD(MAX)}$ is the maximum load step, and R_{PCB} is the parasitic board resistance between the load and output capacitor.

The capacitance value dominates the midfrequency output impedance and dominates the load-transient response as long as the load transient's slew rate is less than two switching cycles. Under these conditions, the sag and soar voltages depend on the output capacitance, inductance value, and delays in the transient response. Low inductor values allow the inductor current to slew faster, replenishing charge removed from or added to the output filter capacitors by a sudden load step, especially with low differential voltages across the inductor. The sag voltage (V_{SAG}) that occurs after applying the load current can be estimated by the following:

$$V_{SAG} = \frac{L\left(\Delta I_{LOAD(MAX)}\right)^2}{2C_{OUT}\left(V_{IN} \times D_{MAX} - V_{OUT}\right)} + \frac{\Delta I_{LOAD(MAX)}(T - \Delta T)}{C_{OUT}}$$

where D_{MAX} is the maximum duty factor (see the *Electrical Characteristics* table), T is the switching period ($1/f_{OSC}$), and ΔT equals V_{OUT}/V_{IN} x T when in PWM mode, or L x $I_{IDLE}/(V_{IN} - V_{OUT})$ when in pulse-skipping mode. The amount of overshoot voltage (V_{SOAR}) that occurs after load removal (due to stored inductor energy) can be calculated as:

$$V_{SOAR} \approx \frac{\left(\Delta I_{LOAD(MAX)}\right)^2 L}{2C_{OUT}V_{OUT}}$$

When using low-capacity ceramic filter capacitors, capacitor size is usually determined by the capacity needed to prevent V_{SOAR} from causing problems during load transients. Generally, once enough capacitance is added to meet the overshoot requirement, undershoot at the rising load edge is no longer a problem.

Input Capacitor Selection

The input capacitor must meet the ripple current requirement (I_{RMS}) imposed by the switching currents. The I_{RMS} requirements of an individual regulator can be determined by the following equation:

$$I_{RMS} = \left(\frac{I_{LOAD}}{V_{IN}}\right)\sqrt{V_{OUT}\left(V_{IN} - V_{OUT}\right)}$$

The worst-case RMS current requirement occurs when operating with V_{IN} = $2V_{OUT}$. At this point, the above equation simplifies to I_{RMS} = 0.5 x I_{LOAD}. However, the MAX17019 uses an interleaved fixed-frequency architecture, which helps reduce the overall input RMS current on the INBC input supply.

For the MAX17019 system (INA) supply, nontantalum chemistries (ceramic, aluminum, or OS-CON) are preferred due to their resistance to inrush surge currents typical of systems with a mechanical switch or connector in series with the input. For the MAX17019 INBC input supply, ceramic capacitors are preferred on input due to their low parasitic inductance, which helps reduce the high-frequency ringing on the INBC supply when the internal MOSFETs are turned off. Choose an input capacitor that exhibits less than +10°C temperature rise at the RMS input current for optimal circuit longevity.

BST Capacitors

The boost capacitors (C_{BST}) must be selected large enough to handle the gate charging requirements of the high-side MOSFETs. For these low-power applications, 0.1µF ceramic capacitors work well.

Regulator A Power-MOSFET Selection

Most of the following MOSFET guidelines focus on the challenge of obtaining high load-current capability when using high-voltage (> 20V) AC adapters. Low current applications usually require less attention.

The high-side MOSFET (N_H) must be able to dissipate the resistive losses plus the switching losses at both $V_{IN(MIN)}$ and $V_{IN(MAX)}$. Ideally, the losses at $V_{IN(MIN)}$ should be roughly equal to the losses at $V_{IN(MAX)}$, with lower losses in between. If the losses at $V_{IN(MIN)}$ are significantly higher, consider increasing the size of N_H. Conversely, if the losses at $V_{IN(MAX)}$ are significantly higher, consider reducing the size of N_H. If V_{IN} does not vary over a wide range, maximum efficiency is achieved by selecting a high-side MOSFET (N_H) that has conduction losses equal to the switching losses.

Choose a low-side MOSFET (N_L) that has the lowest possible on-resistance ($R_{DS(ON)}$), comes in a moderate-sized package (i.e., 8-pin SO, DPAK, or D^2PAK), and is reasonably priced. Ensure that the MAX17019 DLA gate driver can supply sufficient current to support the gate charge and the current injected into the parasitic drain-to-gate capacitor caused by the high-side MOSFET turning on; otherwise, cross-conduction problems might occur. Switching losses are not an issue for the low-side MOSFET since it is a zero-voltage switched device when used in the step-down topology.

Power-MOSFET Dissipation

Worst-case conduction losses occur at the duty factor extremes. For the high-side MOSFET (N_H), the worstcase power dissipation due to resistance occurs at minimum input voltage:

$$PD(N_H \text{Resistive}) = \left(\frac{V_{OUT}}{V_{IN}}\right)(I_{LOAD})^2 R_{DS(ON)}$$

Generally, use a small high-side MOSFET to reduce switching losses at high input voltages. However, the $R_{DS(ON)}$ required to stay within package power-dissipation limits often limits how small the MOSFET can be. The optimum occurs when the switching losses equal the conduction ($R_{DS(ON)}$) losses. High-side switching losses do not become an issue until the input is greater than approximately 15V.

Calculating the power dissipation in high-side MOSFETs (N_H) due to switching losses is difficult, since it must allow for difficult-to-quantify factors that influence the turn-on and turn-off times. These factors include the internal gate resistance, gate charge, threshold voltage, source inductance, and PCB layout characteristics. The following switching loss calculation provides only a very rough estimate and is no substitute for breadboard evaluation, preferably including verification using a thermocouple mounted on N_H:

$$PD(N_H \text{Switching}) = \left(\frac{I_{LOAD} Q_{G(SW)}}{I_{GATE}} + \frac{C_{OSS} V_{IN(MAX)}}{2}\right) V_{IN(MAX)} f_{SW}$$

where C_{OSS} is the output capacitance of N_H, $Q_{G(SW)}$ is the charge needed to turn on the N_H MOSFET, and I_{GATE} is the peak gate-drive source/sink current (1A typ).

Switching losses in the high-side MOSFET can become a heat problem when maximum AC adapter voltages are applied, due to the squared term in the switchingloss equation (C x V_{IN}^2 x f_{SW}). If the high-side MOSFET chosen for adequate $R_{DS(ON)}$ at low battery voltages becomes extraordinarily hot when subjected to $V_{IN(MAX)}$, consider choosing another MOSFET with lower parasitic capacitance.

For the low-side MOSFET (N_L) the worst-case power dissipation always occurs at maximum battery voltage:

$$PD(N_L \text{Resistive}) = \left[1 - \left(\frac{V_{OUT}}{V_{IN(MAX)}}\right)\right](I_{LOAD})^2 R_{DS(ON)}$$

The absolute worst case for MOSFET power dissipation occurs under heavy overload conditions that are greater than $I_{LOAD(MAX)}$, but are not high enough to exceed the current limit and cause the fault latch to trip. To protect against this possibility, “overdesign” the circuit to tolerate:

$$I_{LOAD} = I_{LIMIT} - \left(\frac{\Delta I_{INDUCTOR}}{2}\right)$$

where I_{LIMIT} is the peak current allowed by the current-limit circuit, including threshold tolerance and sense-resistance variation. The MOSFETs must have a relatively large heatsink to handle the overload power dissipation.

Choose a Schottky diode (D_L) with a forward voltage drop low enough to prevent the low-side MOSFET's body diode from turning on during the dead time. As a general rule, select a diode with a DC current rating equal to 1/3 the load current. This diode is optional and can be removed if efficiency is not critical.

VTT LDO Design Procedure

IND Input Capacitor Selection (C_{IND})

The value of the IND bypass capacitor is chosen to limit the amount of ripple and noise at IND, and the amount of voltage sag during a load transient. Typically, IND connects to the output of a step-down switching regulator, which already has a large bulk output capacitor. Nevertheless, a ceramic capacitor equivalent to half the VTT output capacitance should be added and placed as close as possible to IND. The necessary capacitance value must be increased with larger load current, or if the trace from IND to the power source is long and results in relatively high input impedance.

VTT LDO Output Voltage (FBD)

The VTT output stage is powered from the IND input. The VTT output voltage is set by the REFIND input. REFIND sets the VTT LDO feedback regulation voltage ($V_{FBD} = V_{REFIND}$) and the VTTR output voltage. The VTT LDO (FBD voltage) and VTTR track the REFIND voltage over a 0.5V to 1.5V range. This reference input feature makes the MAX17019 ideal for memory applications in which the termination supply must track the supply voltage.

VTT LDO Output Capacitor Selection (C_{OUTD})

A minimum value of 20µF or greater ceramic is needed to stabilize the VTT output (OUTD). This value of capacitance limits the switching regulator's unity-gain bandwidth frequency to approximately 1.2MHz (typ) to allow adequate phase margin for stability. To keep the capacitor acting as a capacitor within the switching regulator's bandwidth, it is important that ceramic capacitors with low ESR and ESL be used.

Since the gain bandwidth is also determined by the transconductance of the output MOSFETs, which increases with load current, the output capacitor might need to be greater than 20µF if the load current exceeds 1.5A, but can be smaller than 20µF if the maximum load current is less than 1.5A. As a guideline, choose the minimum capacitance and maximum ESR for the output capacitor using the following:

$$C_{OUT\_MIN} = 20\mu F \times \sqrt{\frac{I_{LOAD}}{1.5A}}$$

and:

$$R_{ESR\_MAX} = 5m\Omega \times \sqrt{\frac{I_{LOAD}}{1.5A}}$$

R_{ESR} value is measured at the unity-gain-bandwidth frequency given by approximately:

$$f_{GBW} = \frac{36}{C_{OUT}} \times \sqrt{\frac{I_{LOAD}}{1.5A}}$$

Once these conditions for stability are met, additional capacitors, including those of electrolytic and tantalum types, can be connected in parallel to the ceramic capacitor (if desired) to further suppress noise or voltage ripple at the output.

VTTR Output Capacitor Selection

The VTTR buffer is a scaled-down version of the VTT regulator, with much smaller output transconductance. Therefore, the VTTR compensation requirements also scale. For typical applications requiring load currents up to ±3mA, a 0.22µF or greater ceramic capacitor is recommended ($R_{ESR} < 0.3\Omega$).

VTT LDO Power Dissipation

Power loss in the MAX17019 VTT LDO is significant and can become a limiting design factor in the overall MAX17019 design:

$$PD_{VTT} = 2A \times 0.9V = 1.8W$$

The 1.8W total power dissipation is within the 40-pin TQFN multilayer board power-dissipation specification of 2.9W. The typical DDR termination application does not actually continuously source or sink high currents. The actual VTT current typically remains around 100mA to 200mA under steady-state conditions. VTTR is down in the microampere range, though the Intel specification requires 3mA for DDR1 and 1mA for DDR2. True worst-case power dissipation occurs on an output short-circuit condition with worst-case current limit. The MAX17019 does not employ any foldback current limiting, and relies on the internal thermal shutdown for protection. Both the VTT and VTTR output voltages are referenced to the same REFIND input.

Applications Information

Minimum Input Voltage

The minimum input operating voltage (dropout voltage) is restricted by the maximum duty-cycle specification (see the *Electrical Characteristics* table). For the best dropout performance, use the slowest switching frequency setting (FREQ = GND). However, keep in mind that the transient performance gets worse as the stepdown regulators approach the dropout voltage, so bulk output capacitance must be added (see the voltage sag and soar equations in the *SMPS Design Procedure (Step-Down Regulators)* section). The absolute point of dropout occurs when the inductor current ramps down during the off-time (ΔI_{DOWN}) as much as it ramps up during the on-time (ΔI_{UP}). This results in a minimum operating voltage defined by the following equation:

$$V_{IN(MIN)} = V_{OUT} + V_{CHG} + h\left(\frac{1}{D_{MAX}} - 1\right)\left(V_{OUT} + V_{DIS}\right)$$

where V_{CHG} and V_{DIS} are the parasitic voltage drops in the charge and discharge paths, respectively. A reasonable minimum value for h is 1.5, while the absolute minimum input voltage is calculated with h = 1.

Maximum Input Voltage

The MAX17019 controller includes a minimum on-time specification, which determines the maximum input operating voltage that maintains the selected switching frequency (see the *Electrical Characteristics* table). Operation above this maximum input voltage results in pulse skipping to avoid overcharging the output. At the beginning of each cycle, if the output voltage is still above the feedback threshold voltage, the controller does not trigger an on-time pulse, effectively skipping a cycle. This allows the controller to maintain regulation above the maximum input voltage, but forces the controller to effectively operate with a lower switching frequency. This results in an input threshold voltage at which the controller begins to skip pulses ($V_{IN(SKIP)}$):

$$V_{IN(SKIP)} = V_{OUT}\left(\frac{1}{f_{OSC} t_{ON(MIN)}}\right)$$

where f_{OSC} is the switching frequency selected by FREQ.

PCB Layout Guidelines

Careful PCB layout is critical to achieving low switching losses and clean, stable operation. The switching power stage requires particular attention. If possible, mount all the power components on the top side of the board, with their ground terminals flush against one another.

Follow the MAX17019 evaluation kit layout and use the following guidelines for good PCB layout:

- Keep the high-current paths short, especially at the ground terminals. This practice is essential for stable, jitter-free operation.
- Keep the power traces and load connections short. This practice is essential for high efficiency. Using thick copper PCBs (2oz vs. 1oz) can enhance fullload efficiency by 1% or more. Correctly routing PCB traces is a difficult task that must be approached in terms of fractions of centimeters, where a single milliohm of excess trace resistance causes a measurable efficiency penalty.
- Minimize current-sensing errors by connecting CSPA and CSNA directly across the current-sense resistor ($R_{SENSE\_}$).
- When trade-offs in trace lengths must be made, it is preferable to allow the inductor charging path to be made longer than the discharge path. For example, it is better to allow some extra distance between the input capacitors and the high-side MOSFET than to allow distance between the inductor and the lowside MOSFET or between the inductor and the output filter capacitor.
- Route high-speed switching nodes (BST_, LX_, DHA, and DLA) away from sensitive analog areas (REF, REFIND, FB_, CSPA, CSNA).

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX17019ATM+	-40°C to +105°C	48 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.

**EP = Exposed pad.*

Chip Information

PROCESS: BiCMOS

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	8/08	Initial release	—
1	10/14	Removed automotive references from the *General Description* and *Applications*	1
2	5/18	Removed automotive references from the *General Description* and *Applications*	6–8, 25

Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов;
- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits,General Dynamics и др.);

Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.

Как с нами связаться

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