

# 74ALVCH16500

18-bit universal bus transceiver; 3-state

Rev. 3 — 11 December 2017

Product data sheet

## 1 General description

The 74ALVCH16500 is a high-performance CMOS product. This device is an 18-bit universal transceiver featuring non-inverting 3-state bus compatible outputs in both send and receive directions. Data flow in each direction is controlled by output enable (OEAB and  $\overline{\text{OEBA}}$ ), latch enable (LEAB and LEBA), and clock ( $\overline{\text{CPAB}}$  and  $\overline{\text{CPBA}}$ ) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is HIGH. When LEAB is LOW, the A data is latched if  $\overline{\text{CPAB}}$  is held at a HIGH or LOW logic level. If LEAB is LOW, the A data is stored in the latch/flip-flop on the HIGH-to-LOW transition of  $\overline{\text{CPAB}}$ . When OEAB is HIGH, the outputs are active. When OEAB is LOW, the outputs are in the high-impedance state.

Data flow for B-to-A is similar to that of A-to-B but uses  $\overline{\text{OEBA}}$ , LEBA and  $\overline{\text{CPBA}}$ . The output enables are complimentary (OEAB is active HIGH, and  $\overline{\text{OEBA}}$  is active LOW).

To ensure the high impedance state during power up or power down,  $\overline{\text{OEBA}}$  should be tied to  $V_{CC}$  through a pullup resistor and OEAB should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking/current-sourcing capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

## 2 Features and benefits

- CMOS low power consumption
- MultiByte flow-through standard pin-out architecture
- Low inductance multiple  $V_{CC}$  and GND pins for minimum noise and ground bounce
- Direct interface with TTL levels (2.7 V to 3.6 V)
- Bus hold on data inputs
- Output drive capability 50  $\Omega$  transmission lines at 85 °C
- Current drive  $\pm 24$  mA at 3.0 V
- Complies with JEDEC standards:
  - JESD8-5 (2.3 V to 2.7 V)
  - JESD8B/JESD36 (2.7 V to 3.6 V)
- ESD protection:
  - HBM ANSI/ESDA/JEDEC JS-001 exceeds 2000 V
  - CDM JESD22-C101E exceeds 1000 V

3 Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74ALVCH16500DGG	-40 °C to +85 °C	TSSOP56	plastic thin shrink small outline package; 56 leads; body width 6.1 mm	SOT364-1

4 Functional diagram

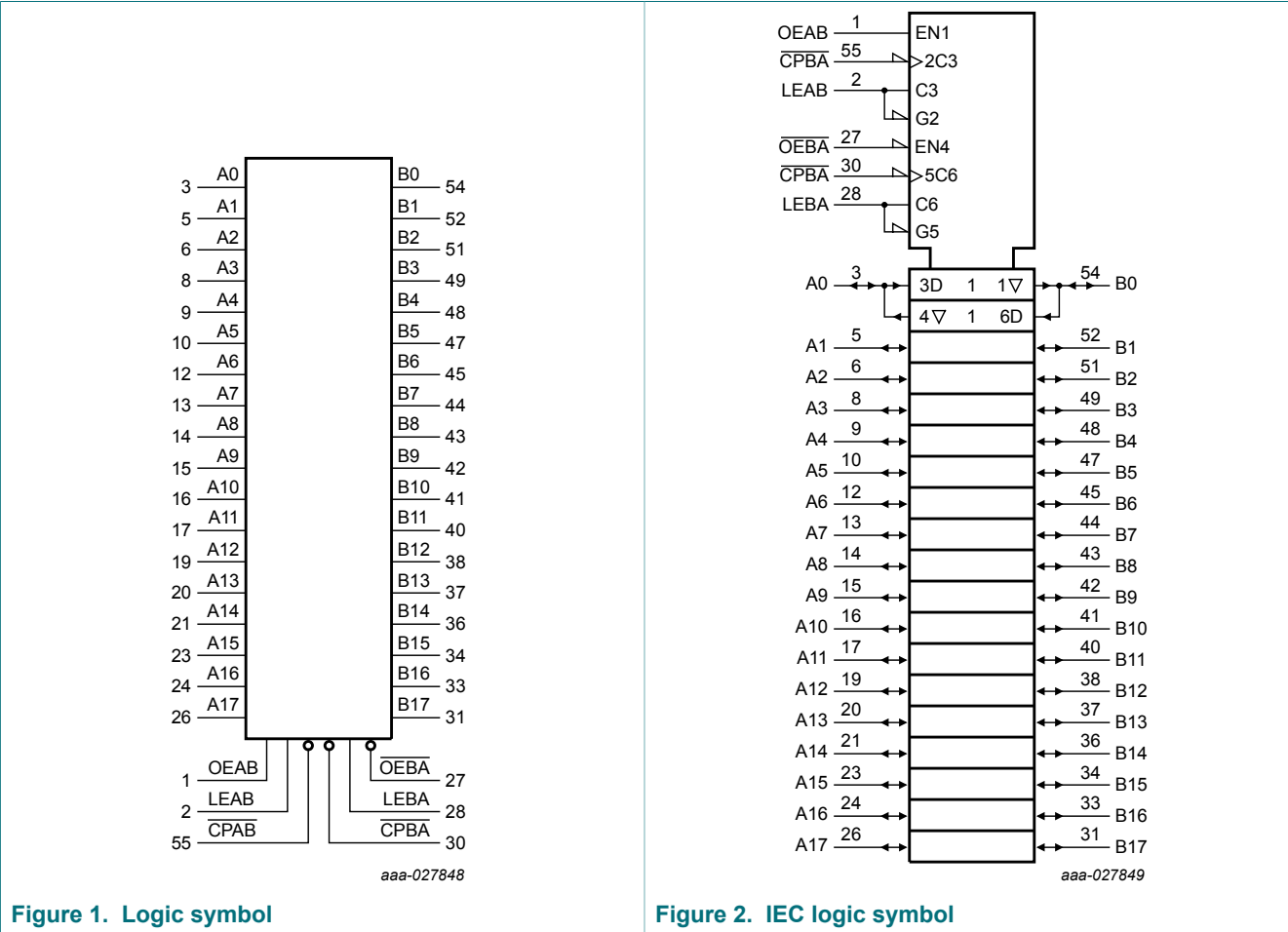


Figure 1. Logic symbol

Figure 2. IEC logic symbol

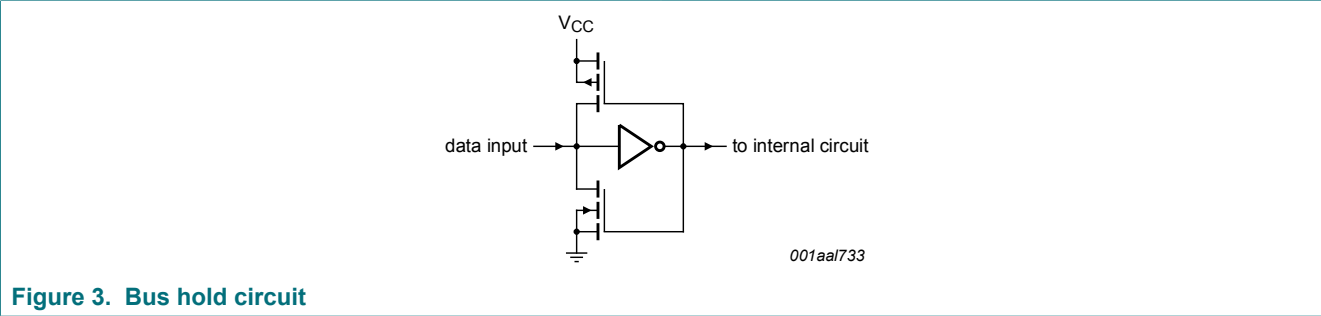


Figure 3. Bus hold circuit

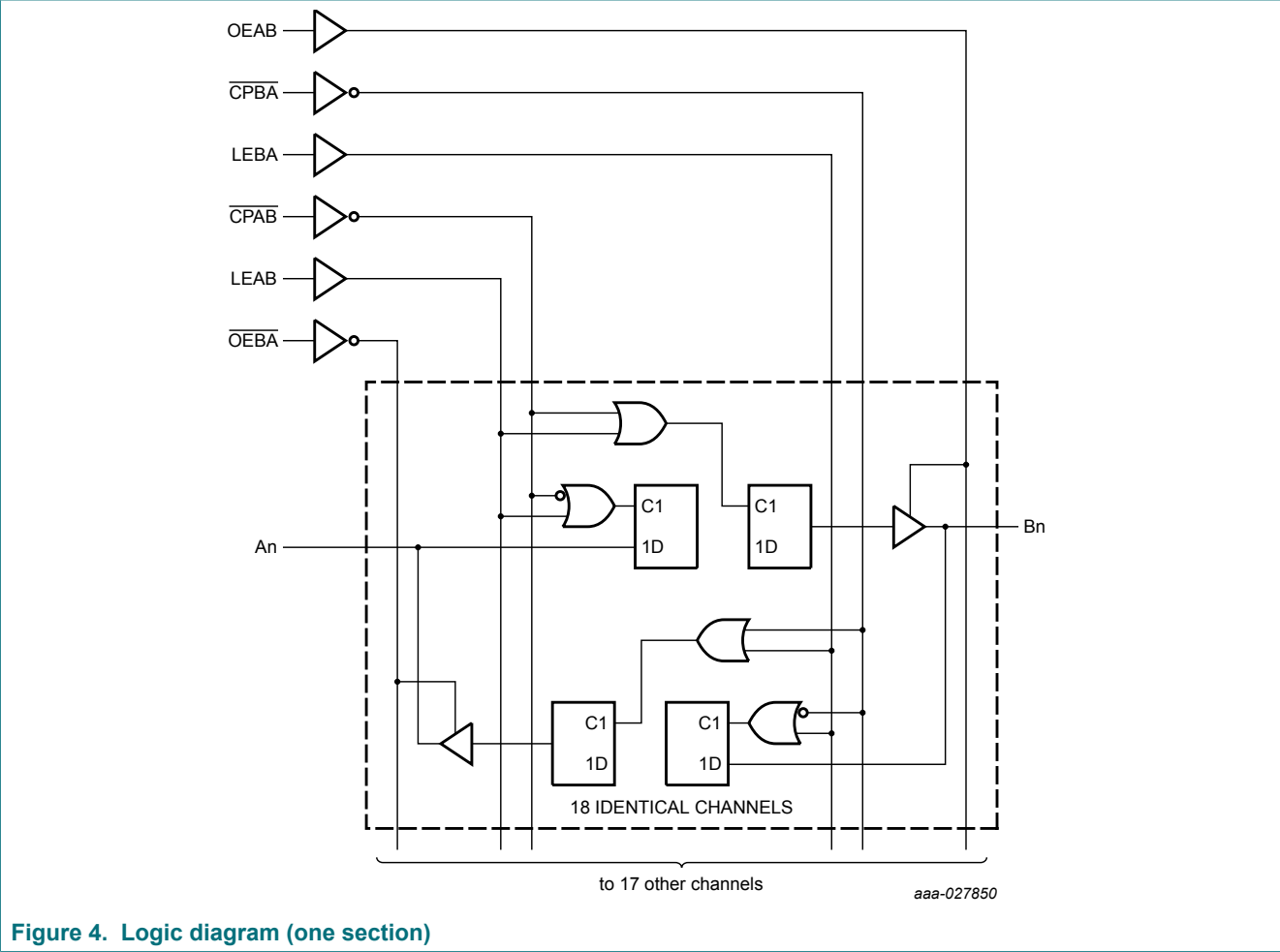
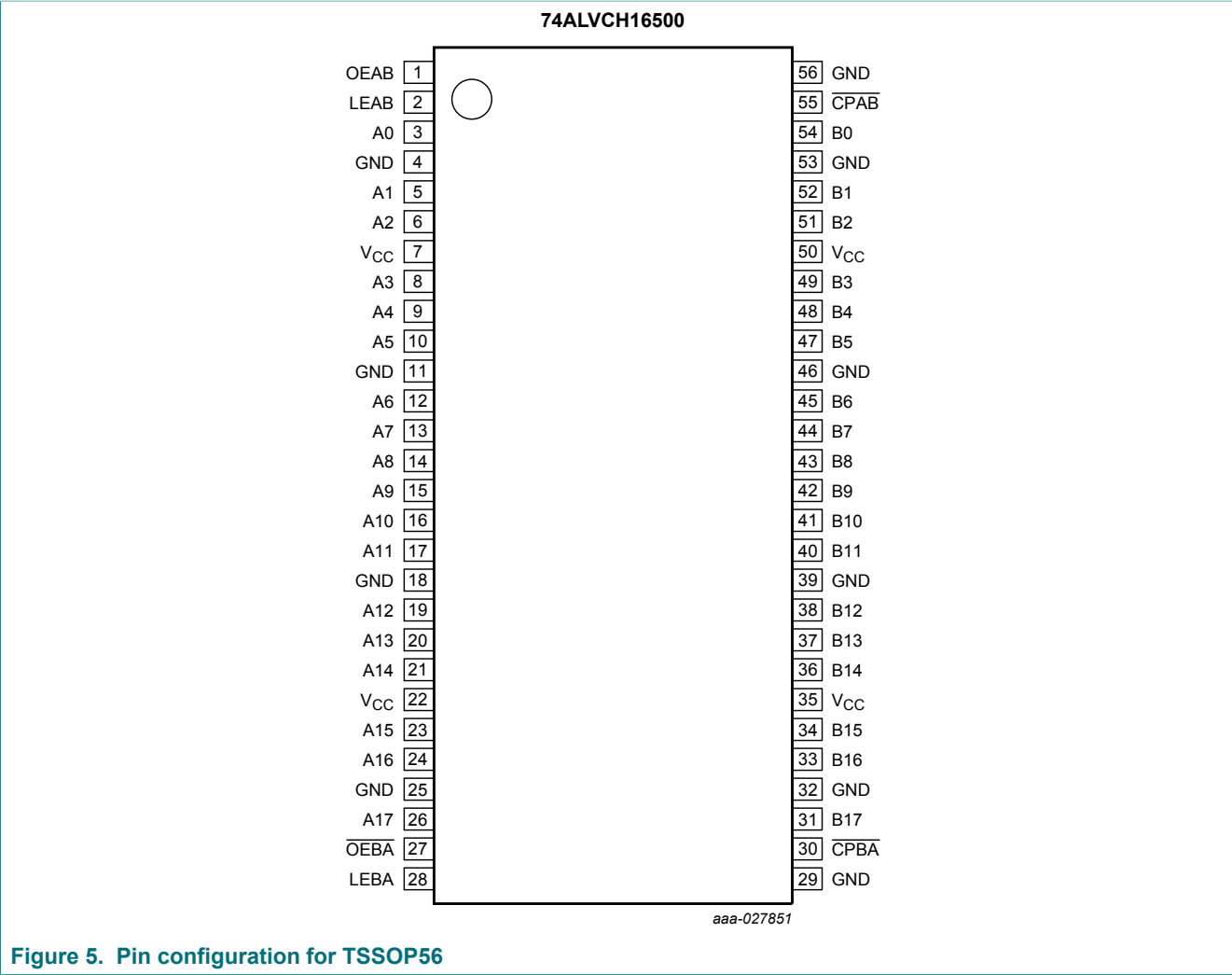


Figure 4. Logic diagram (one section)

5 Pinning information

5.1 Pinning



## 5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
A0, A1, A2, A3, A4, A5, A6, A7, A8, A9, A10, A11, A12, A13, A14, A15, A16, A17	3, 5, 6, 8, 9, 10, 12, 13, 14, 15, 16, 17, 19, 20, 21, 23, 24, 26	data inputs/outputs
B0, B1, B2, B3, B4, B5, B6, B7, B8, B9, B10, B11, B12, B13, B14, B15, B16, B17	54, 52, 51, 49, 48, 47, 45, 44, 43, 42, 41, 40, 38, 37, 36, 34, 33, 31	data outputs/inputs
OEAB	1	A to B output enable input (active HIGH)
OEBA	27	B to A output enable input (active LOW)
LEAB, LEBA	2, 28	A to B / B to A latch enable inputs (active HIGH)
CPBA, CPAB	30, 55	B to A / A to B clock inputs (active LOW)
GND	4, 11, 18, 25, 29, 32, 39, 46, 53, 56	ground (0 V)
V <sub>CC</sub>	7, 22, 35, 50	supply voltage

## 6 Functional description

Table 3. Function selection <sup>[1] [2]</sup>

Operating mode	Inputs				Outputs
	OEAB	LEAB	CPAB	An	Bn
Disabled	L	H	X	X	Z
Transparent	H	H	X	H	H
	H	H	X	L	L
Latch data & display	H	↓	X	h	H
	H	↓	X	l	L
Clock data & display	H	L	↓	h	H
	H	L	↓	l	L
Hold data & display	H	L	H or L	X	H
	H	L	H or L	X	L

[1] A-to-B data flow is shown; B-to-A flow is similar but uses OEBA, LEBA, and CPBA.

[2] H = HIGH voltage level;

h = HIGH voltage level one set-up time prior to the enable or clock transition;

L = LOW voltage level;

l = LOW voltage level one set-up time prior to the enable or clock transition;

X = don't care;

↓ = HIGH-to-LOW enable or clock transition;

Z = high-impedance OFF-state.

## 7 Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+4.6	V
$V_I$	input voltage	data inputs [1]	-0.5	$V_{CC} + 0.5$	V
		control inputs [1]	-0.5	+4.6	V
$V_O$	output voltage	[1]	-0.5	$V_{CC} + 0.5$	V
$I_{IK}$	input clamping current	$V_I < 0$ V	-50	-	mA
$I_{OK}$	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V	-	$\pm 50$	mA
$I_O$	output current	$V_O = 0$ V to $V_{CC}$	-	$\pm 50$	mA
$I_{CC}$	supply current		-	100	mA
$I_{GND}$	ground current		-100	-	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40$ °C to +85 °C [2]	-	600	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For TSSOP56 packages: above 55 °C derate linearly with 8 mW/K.

## 8 Recommended operating conditions

**Table 5. Recommended operating conditions**

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage	for maximum speed performance at $C_L = 30$ pF	2.3	2.7	V
		for maximum speed performance at $C_L = 50$ pF	3.0	3.6	V
$V_I$	input voltage		0	$V_{CC}$	V
$V_O$	output voltage		0	$V_{CC}$	V
$T_{amb}$	ambient temperature	in free air	-40	+85	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 2.3$ V to 3.0 V	-	20	ns/V
		$V_{CC} = 3.0$ V to 3.6 V	-	10	ns/V

## 9 Static characteristics

**Table 6. Static characteristics**

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ <sup>[1]</sup>	Max	Unit
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 2.3 to 2.7 V	1.7	1.2	-	V
		V <sub>CC</sub> = 2.7 to 3.6 V	2.0	1.5	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 2.3 to 2.7 V	-	1.2	0.7	V
		V <sub>CC</sub> = 2.7 to 3.6 V	-	1.5	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>				
		I <sub>O</sub> = -100 µA; V <sub>CC</sub> = 2.3 V to 3.6 V	V <sub>CC</sub> - 0.2	V <sub>CC</sub>	-	V
		I <sub>O</sub> = -6 mA; V <sub>CC</sub> = 2.3 V	V <sub>CC</sub> - 0.3	V <sub>CC</sub> - 0.08	-	V
		I <sub>O</sub> = -12 mA; V <sub>CC</sub> = 2.3 V	V <sub>CC</sub> - 0.6	V <sub>CC</sub> - 0.26	-	V
		I <sub>O</sub> = -12 mA; V <sub>CC</sub> = 2.7 V	V <sub>CC</sub> - 0.5	V <sub>CC</sub> - 0.14	-	V
		I <sub>O</sub> = -12 mA; V <sub>CC</sub> = 3.0 V	V <sub>CC</sub> - 0.6	V <sub>CC</sub> - 0.09	-	V
		I <sub>O</sub> = -24 mA; V <sub>CC</sub> = 3.0 V	V <sub>CC</sub> - 1.0	V <sub>CC</sub> - 0.28	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>				
		I <sub>O</sub> = 100 µA; V <sub>CC</sub> = 2.3 V to 3.6 V	-	GND	0.20	V
		I <sub>O</sub> = 6 mA; V <sub>CC</sub> = 2.3 V	-	0.07	0.40	V
		I <sub>O</sub> = 12 mA; V <sub>CC</sub> = 2.3 V	-	0.15	0.70	V
		I <sub>O</sub> = 12 mA; V <sub>CC</sub> = 2.7 V	-	0.14	0.40	V
		I <sub>O</sub> = 24 mA; V <sub>CC</sub> = 3.0 V	-	0.27	0.55	V
I <sub>I</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 2.3 V to 3.6 V	-	0.1	5	µA
I <sub>BHL</sub>	bus hold LOW current	V <sub>CC</sub> = 2.3 V; V <sub>I</sub> = 0.7 V	45	-	-	µA
		V <sub>CC</sub> = 3.0 V; V <sub>I</sub> = 0.8 V	75	150	-	µA
I <sub>BHH</sub>	bus hold HIGH current	V <sub>CC</sub> = 2.3 V; V <sub>I</sub> = 1.7 V	-45	-	-	µA
		V <sub>CC</sub> = 3.0 V; V <sub>I</sub> = 2.0 V	-75	-175	-	µA
I <sub>BHLO</sub>	bus hold LOW overdrive current	V <sub>CC</sub> = 3.6 V	500	-	-	µA
I <sub>BHHO</sub>	bus hold HIGH overdrive current	V <sub>CC</sub> = 3.6 V	-500	-	-	µA
I <sub>OZ</sub>	OFF-state output current	V <sub>CC</sub> = 2.7 V to 3.6 V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = V <sub>CC</sub> or GND	-	0.1	10	µA
I <sub>CC</sub>	supply current	V <sub>CC</sub> = 2.3 to 3.6 V; V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A	-	0.2	40	µA
ΔI <sub>CC</sub>	additional supply current	V <sub>I</sub> = V <sub>CC</sub> - 0.6 V; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 2.3 V to 3.6 V	-	150	750	µA
C <sub>I</sub>	input capacitance		-	4.0	-	pF
C <sub>I/O</sub>	input/output capacitance		-	8.0	-	pF

[1] All typical values are measured at T<sub>amb</sub> = 25 °C.

## 10 Dynamic characteristics

**Table 7. Dynamic characteristics**

Voltages are referenced to GND (ground = 0 V). For test circuit, see [Figure 10](#).

Symbol	Parameter	Conditions	Min	Typ <sup>[1]</sup>	Max	Unit
$t_{pd}$	propagation delay	An to Bn; Bn to An; <a href="#">Figure 6</a> <sup>[2]</sup>				
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.0	3.1	5.2	ns
		$V_{CC} = 2.7 \text{ V}$	-	3.1	4.7	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	1.0	2.9	4.2	ns
		LEAB to Bn; LEBA to An; <a href="#">Figure 7</a> <sup>[2]</sup>				
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.0	3.6	6.2	ns
		$V_{CC} = 2.7 \text{ V}$	-	3.4	5.5	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	1.0	3.1	4.9	ns
		$\overline{CPAB}$ to Bn; $\overline{CPBA}$ to An; <a href="#">Figure 7</a> <sup>[2]</sup>				
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.0	3.7	6.6	ns
		$V_{CC} = 2.7 \text{ V}$	-	3.8	6.6	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	1.1	3.3	5.5	ns
$t_{en}$	enable time	$\overline{OEBA}$ to An; <a href="#">Figure 8</a> <sup>[2]</sup>				
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.0	3.1	6.2	ns
		$V_{CC} = 2.7 \text{ V}$	-	3.3	6.2	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	1.0	2.8	5.2	ns
		$\overline{OEAB}$ to Bn; <a href="#">Figure 8</a> <sup>[2]</sup>				ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.0	2.7	5.7	ns
		$V_{CC} = 2.7 \text{ V}$	-	2.7	5.4	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	1.0	2.5	4.6	ns
$t_{dis}$	disable time	$\overline{OEBA}$ to An; <a href="#">Figure 8</a> <sup>[2]</sup>				
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.0	2.8	5.4	ns
		$V_{CC} = 2.7 \text{ V}$	-	3.3	4.6	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	1.0	3.2	4.3	ns
		$\overline{OEAB}$ to Bn; <a href="#">Figure 8</a> <sup>[2]</sup>				ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.0	2.7	6.1	ns
		$V_{CC} = 2.7 \text{ V}$	-	3.6	5.7	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	1.5	3.2	5.0	ns



Symbol	Parameter	Conditions	Min	Typ <sup>[1]</sup>	Max	Unit
$t_w$	pulse width	LEAB HIGH; LEBA HIGH; <a href="#">Figure 7</a>				
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	3.3	0.8	-	ns
		$V_{CC} = 2.7 \text{ V}$	3.3	0.7	-	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	3.3	0.9	-	ns
		$\overline{CPAB}$ , $\overline{CPBA}$ HIGH or LOW; <a href="#">Figure 7</a>				
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	3.3	2.0	-	ns
		$V_{CC} = 2.7 \text{ V}$	3.3	1.4	-	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	3.3	1.1	-	ns
$t_{su}$	set-up time	An to $\overline{CPAB}$ ; Bn to $\overline{CPBA}$ ; <a href="#">Figure 9</a>				
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7	0.1	-	ns
		$V_{CC} = 2.7 \text{ V}$	1.4	0.1	-	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	1.3	0.2	-	ns
		An to LEAB; Bn to LEBA; <a href="#">Figure 9</a>				
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.9	0.1	-	ns
		$V_{CC} = 2.7 \text{ V}$	1.6	-0.2	-	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	1.4	0.3	-	ns
$t_h$	hold time	An to $\overline{CPAB}$ ; Bn to $\overline{CPBA}$ ; <a href="#">Figure 9</a>				
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7	0.2	-	ns
		$V_{CC} = 2.7 \text{ V}$	1.6	0.3	-	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	1.3	-0.1	-	ns
		An to LEAB; Bn to LEBA; <a href="#">Figure 9</a>				
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	2.0	0.2	-	ns
		$V_{CC} = 2.7 \text{ V}$	1.8	0.1	-	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	1.5	0.1	-	ns
$f_{max}$	maximum frequency	$\overline{CPAB}$ , $\overline{CPBA}$ ; <a href="#">Figure 7</a>				
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	150	333	-	MHz
		$V_{CC} = 2.7 \text{ V}$	150	333	-	MHz
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	150	340	-	MHz
$C_{PD}$	power dissipation capacitance	per latch; $V_I = \text{GND to } V_{CC}$ <sup>[3]</sup>				
		output enabled	-	21	-	pF
		output disabled	-	3	-	pF

[1] Typical values are measured at  $T_{amb} = 25^\circ\text{C}$

Typical values for  $V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$  are measured at  $V_{CC} = 2.5 \text{ V}$

Typical values for  $V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$  are measured at  $V_{CC} = 3.3 \text{ V}$

[2]  $t_{pd}$  is the same as  $t_{PHL}$  and  $t_{PLH}$ ;  $t_{en}$  is the same as  $t_{PZH}$  and  $t_{PZL}$ ;  $t_{dis}$  is the same as  $t_{PHZ}$  and  $t_{PLZ}$ .

[3]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ):

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o)$  where:

$f_i$  = input frequency in MHz;

$f_o$  = output frequency in MHz;

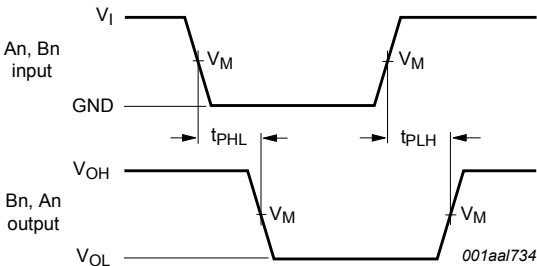
$C_L$  = output load capacitance in pF;

$V_{CC}$  = supply voltage in V;

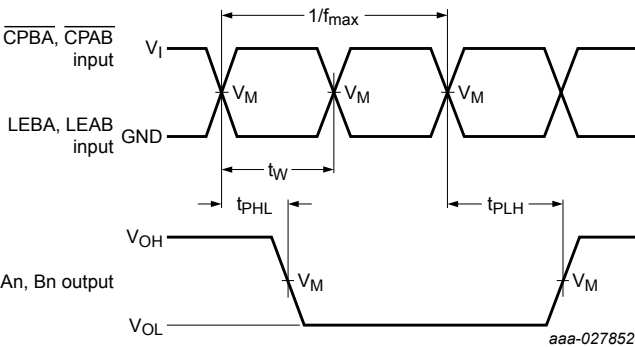
$N$  = number of inputs switching;

$\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs.

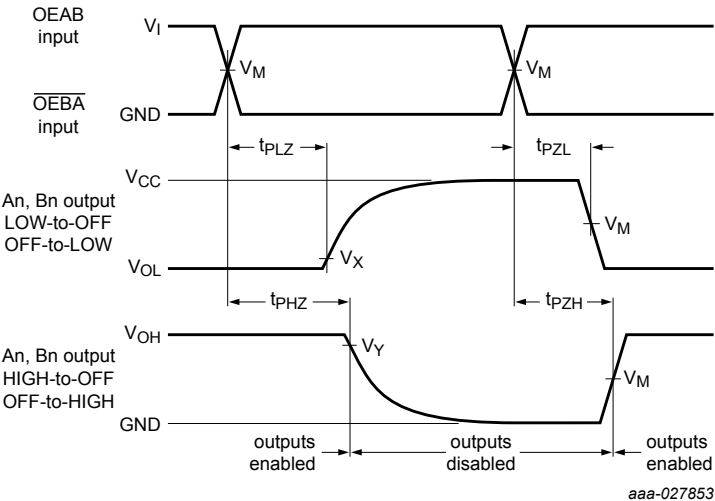
10.1 Waveforms and test circuit



Measurement points are given in [Table 8](#).  
 $V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.  
**Figure 6. The input An, Bn to output Bn, An propagation delay times.**



Measurement points are given in [Table 8](#).  
 $V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.  
**Figure 7. Latch enable input LEAB, LEBA and clock input CPAB, CPBA to output Bn, An propagation delay times; pulse width and  $f_{max}$  of CPAB and CPBA**



Measurement points are given in [Table 8](#).  
 $V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.  
**Figure 8. 3-state enable and disable times.**

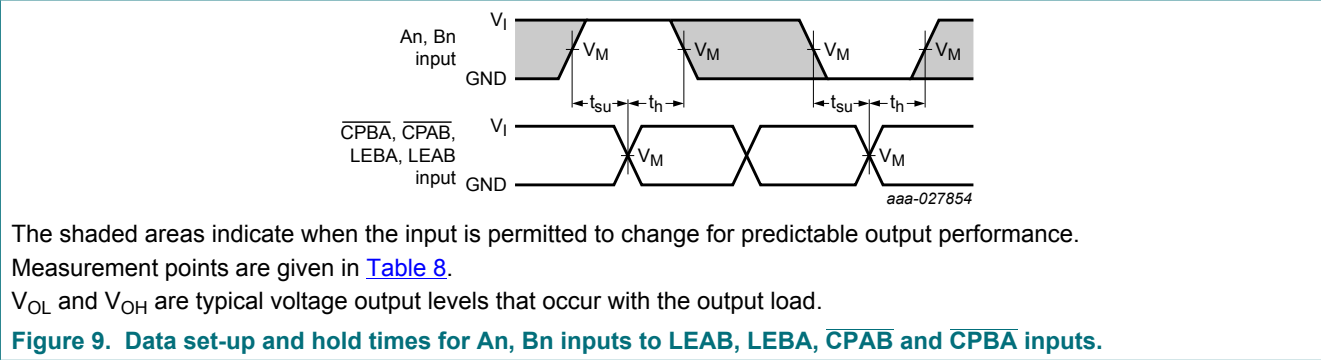
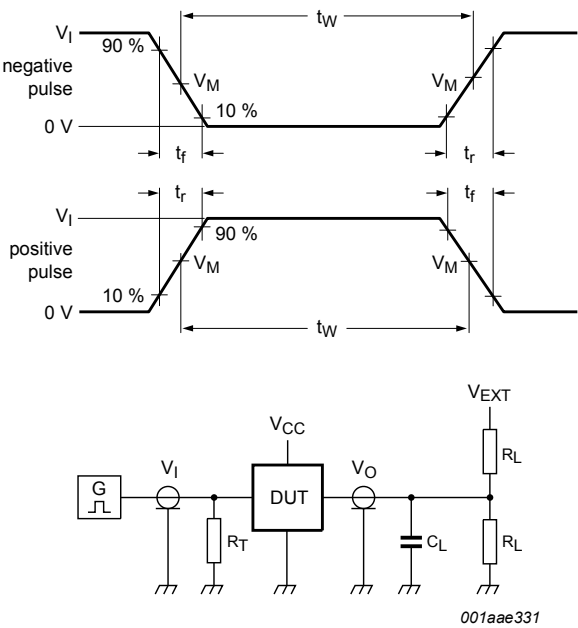


Table 8. Measurement points

Supply voltage	Input		Output		
$V_{CC}$	$V_I$	$V_M$	$V_M$	$V_X$	$V_Y$
2.3 V to 2.7 V	$V_{CC}$	$0.5 V_{CC}$	$0.5 V_{CC}$	$V_{OL} + 0.15 V$	$V_{OH} - 0.15 V$
2.7 V	2.7 V	1.5 V	1.5 V	$V_{OL} + 0.3 V$	$V_{OH} - 0.3 V$
3.0 V to 3.6 V	2.7 V	1.5 V	1.5 V	$V_{OL} + 0.3 V$	$V_{OH} - 0.3 V$



Test data is given in [Table 9](#).  
Definitions for test circuit:  
 $R_L$  = Load resistance.  
 $C_L$  = Load capacitance including jig and probe capacitance.  
 $R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.  
 $V_{EXT}$  = External voltage for measuring switching times.

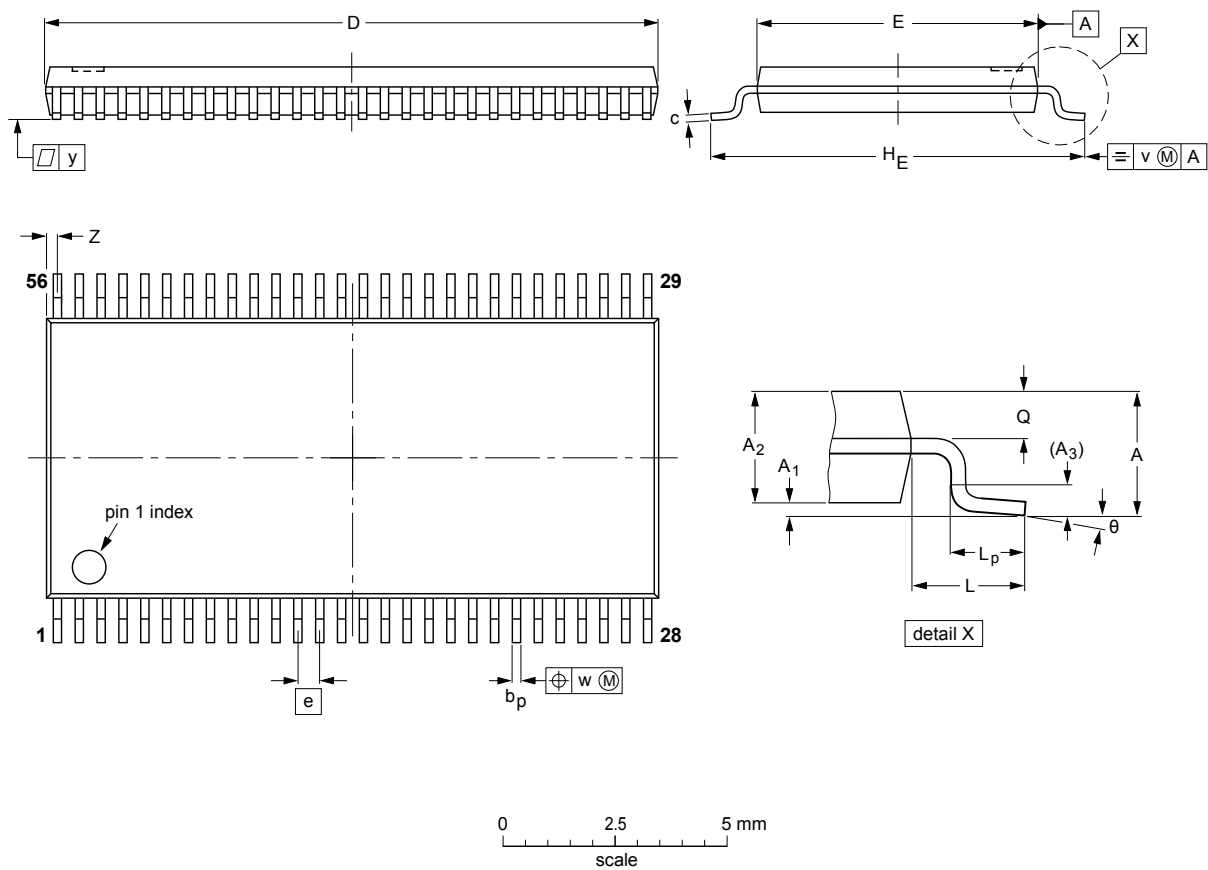
Figure 10. Test circuit for measuring switching times

Table 9. Test data

Supply voltage	Input		Load		$V_{EXT}$		
$V_{CC}$	$V_I$	$t_r, t_f$	$C_L$	$R_L$	$t_{PLH}, t_{PHL}$	$t_{PLZ}, t_{PZL}$	$t_{PHZ}, t_{PZH}$
2.3 V to 2.7 V	$V_{CC}$	$\leq 2.0$ ns	30 pF	500 $\Omega$	open	$2 \times V_{CC}$	GND
2.7 V	2.7 V	$\leq 2.5$ ns	50 pF	500 $\Omega$	open	$2 \times V_{CC}$	GND
3.0 V to 3.6 V	2.7 V	$\leq 2.5$ ns	50 pF	500 $\Omega$	open	$2 \times V_{CC}$	GND

11 Package outline

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1 mm SOT364-1



DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	0.2 0.1	14.1 13.9	6.2 6.0	0.5	8.3 7.9	1	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.5 0.1	8° 0°

Notes

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT364-1		MO-153				99-12-27 03-02-19

Figure 11. Package outline SOT364-1 (TSSOP56)

## 12 Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic

## 13 Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74ALVCH16500 v.3	20171211	Product data sheet	-	74ALVCH16500 v.2
Modifications:	<ul style="list-style-type: none"><li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li><li>Legal texts have been adapted to the new company name where appropriate.</li><li><a href="#">Figure 2</a>: IEC logic symbol updated</li></ul>			
74ALVCH16500 v.2	19980924	Product specification	-	74ALVCH16500 v.1
74ALVCH16500 v.1	19980831	Product specification	-	-

## 14 Legal information

### 14.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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