



ACTT12B-800CT

AC Thyristor Triac power switch

12 September 2014

Product data sheet

1. General description

AC Thyristor Triac power switch in a SOT404 (D2PAK) surface mountable plastic package with self-protective clamping capabilities against low and high energy transients. This "series CT" triac will commute the full RMS current at the maximum rated junction temperature ($T_{j(max)} = 150\text{ °C}$) without the aid of a snubber. It is used in applications where "high junction operating temperature capability" is required.

2. Features and benefits

- Clamping structure ensuring safe high over-voltage withstand capability
- High junction operating temperature capability
- Full cycle AC conduction
- Over-voltage withstand capability to IEC 61000-4-5
- Pin compatible with standard triacs
- Planar passivated for voltage ruggedness and reliability
- Protective self turn-on capability for high energy transients
- Safe clamping capability for low energy over-voltage transients
- Less sensitive gate for high noise immunity
- Surface mountable package
- Triggering in three quadrants only
- Very high immunity to false turn-on by dV/dt

3. Applications

- AC fan, pump and compressor controls
- Highly inductive, resistive and safety loads
- Large and small appliances (White Goods)
- Reversing induction motor controls
- Applications subject to high temperature

4. Quick reference data

Table 1. Quick reference data

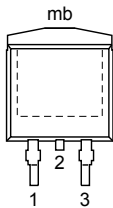
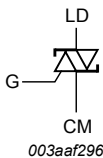
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	-	800	V
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{j(init)} = 25\text{ °C}$; $t_p = 20\text{ ms}$; Fig. 4 ; Fig. 5	-	-	120	A
T_j	junction temperature		-	-	150	°C



Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{mb} \leq 120\text{ }^{\circ}\text{C}$; Fig. 1 ; Fig. 2 ; Fig. 3	-	-	12	A
V_{PP}	peak pulse voltage	$T_j = 25\text{ }^{\circ}\text{C}$; non-repetitive, off-state; Fig. 6	-	-	2	kV
Static characteristics						
I_{GT}	gate trigger current	$V_D = 12\text{ V}$; $I_T = 100\text{ mA}$; LD+ G+; $T_j = 25\text{ }^{\circ}\text{C}$; Fig. 8	-	-	35	mA
		$V_D = 12\text{ V}$; $I_T = 100\text{ mA}$; LD+ G-; $T_j = 25\text{ }^{\circ}\text{C}$; Fig. 8	-	-	35	mA
		$V_D = 12\text{ V}$; $I_T = 100\text{ mA}$; LD- G-; $T_j = 25\text{ }^{\circ}\text{C}$; Fig. 8	-	-	35	mA
V_{CL}	clamping voltage	$I_{CL} = 0.1\text{ mA}$; $t_p = 1\text{ ms}$; $T_j = 25\text{ }^{\circ}\text{C}$	850	-	-	V
Dynamic characteristics						
dV_D/dt	rate of rise of off-state voltage	$V_{DM} = 536\text{ V}$; $T_j = 150\text{ }^{\circ}\text{C}$; ($V_{DM} = 67\%$ of V_{DRM}); exponential waveform; gate open circuit	500	-	-	V/ μs
dI_{com}/dt	rate of change of commutating current	$V_D = 400\text{ V}$; $T_j = 150\text{ }^{\circ}\text{C}$; $I_{T(RMS)} = 12\text{ A}$; $dV_{com}/dt = 20\text{ V}/\mu\text{s}$; (snubberless condition); gate open circuit	5	-	-	A/ms

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	CM	common	 <p>D2PAK (SOT404)</p>	 <p>003aaf296</p>
2	LD	load		
3	G	gate		
mb	LD	mounting base; load		

6. Ordering information

Table 3. Ordering information

Type number	Package		Version
	Name	Description	
ACTT12B-800CT	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404

7. Marking

Table 4. Marking codes

Type number	Marking code
ACTT12B-800CT	ACTT12B-800CT

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{mb} \leq 120\text{ }^{\circ}\text{C}$; Fig. 1 ; Fig. 2 ; Fig. 3	-	12	A
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{j(\text{init})} = 25\text{ }^{\circ}\text{C}$; $t_p = 20\text{ ms}$; Fig. 4 ; Fig. 5	-	120	A
		full sine wave; $T_{j(\text{init})} = 25\text{ }^{\circ}\text{C}$; $t_p = 16.7\text{ ms}$	-	132	A
I^2t	I^2t for fusing	$t_p = 10\text{ ms}$; sine-wave pulse	-	72	A^2s
di_T/dt	rate of rise of on-state current	$I_T = 12\text{ A}$; $I_G = 0.2\text{ A}$; $di_G/dt = 0.2\text{ A}/\mu\text{s}$	-	100	$\text{A}/\mu\text{s}$
I_{GM}	peak gate current	$t = 20\text{ }\mu\text{s}$	-	2	A
P_{GM}	peak gate power		-	5	W
$P_{G(AV)}$	average gate power	over any 20 ms period	-	0.5	W
T_{stg}	storage temperature		-40	150	$^{\circ}\text{C}$
T_j	junction temperature		-	150	$^{\circ}\text{C}$
V_{PP}	peak pulse voltage	$T_j = 25\text{ }^{\circ}\text{C}$; non-repetitive, off-state; Fig. 6	-	2	kV

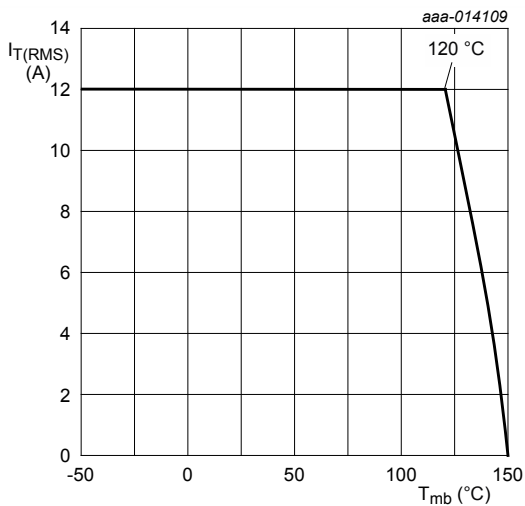
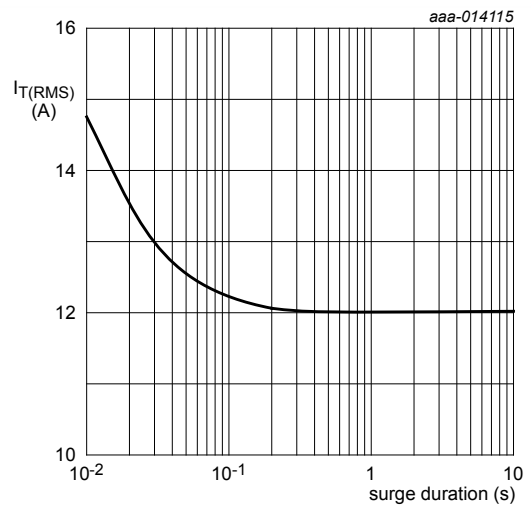


Fig. 1. RMS on-state current as a function of mounting base temperature; maximum values



$f = 50\text{ Hz}$; $T_{mb} = 120\text{ }^{\circ}\text{C}$

Fig. 2. RMS on-state current as a function of surge duration; maximum values

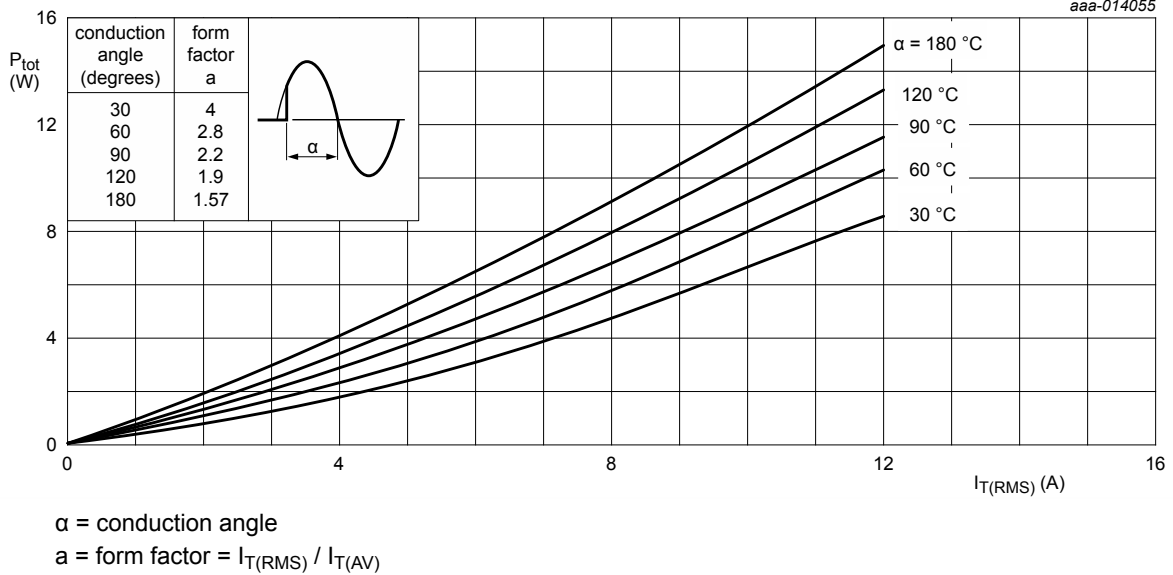


Fig. 3. Total power dissipation as a function of RMS on-state current; maximum values

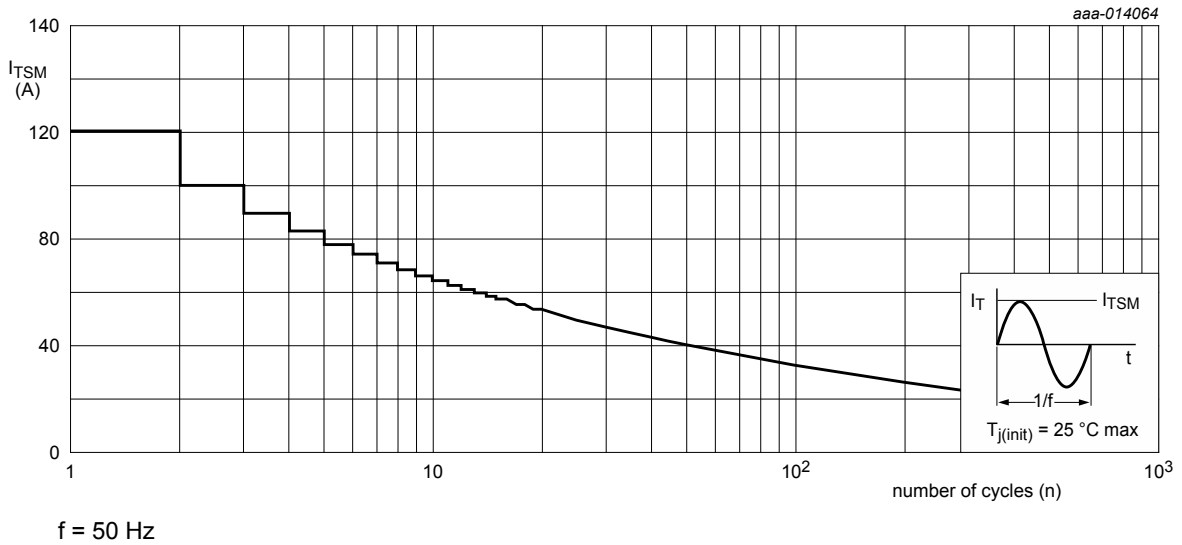


Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values

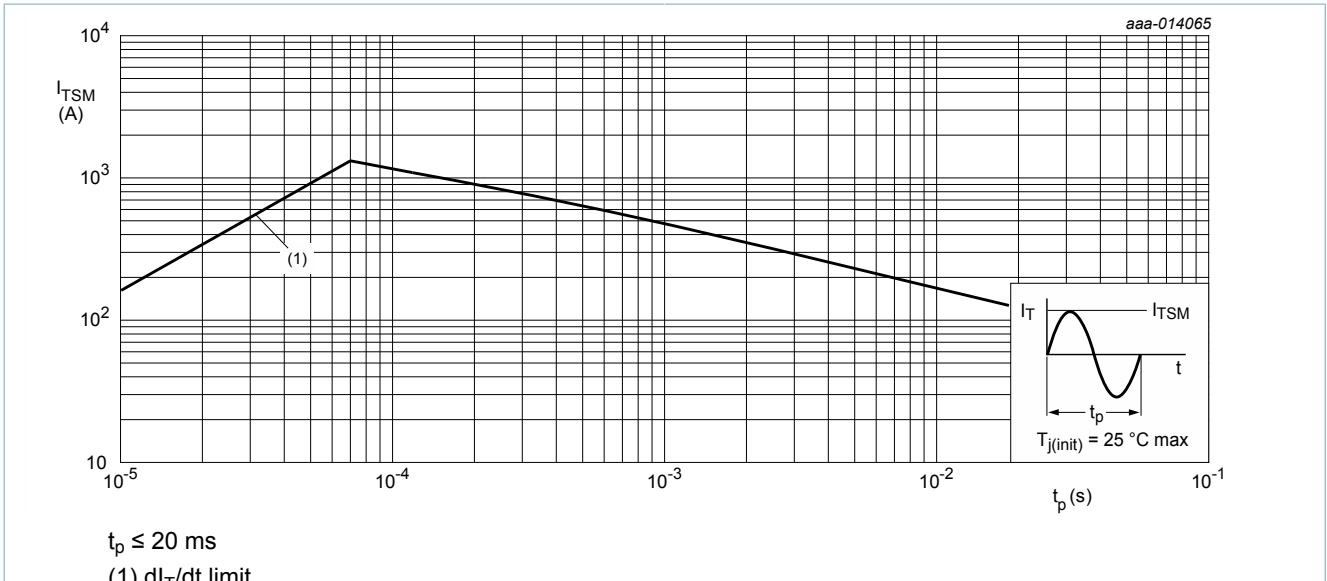


Fig. 5. Non-repetitive peak on-state current as a function of pulse width; maximum values

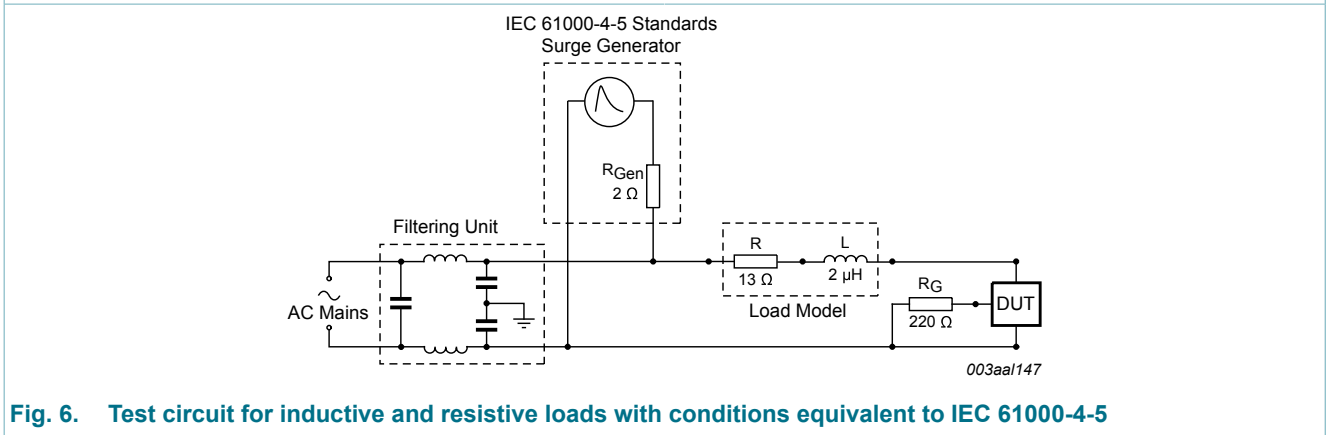


Fig. 6. Test circuit for inductive and resistive loads with conditions equivalent to IEC 61000-4-5

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	full cycle; Fig. 7	-	-	2	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air; printed circuit board (FR4) mounted	-	60	-	K/W

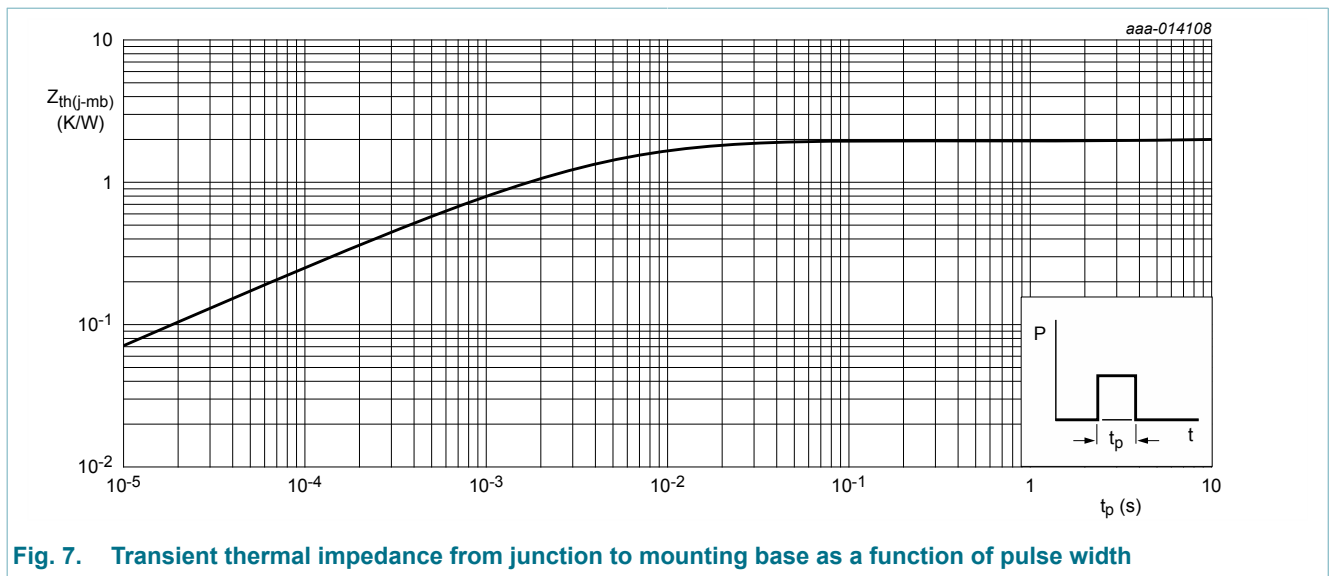
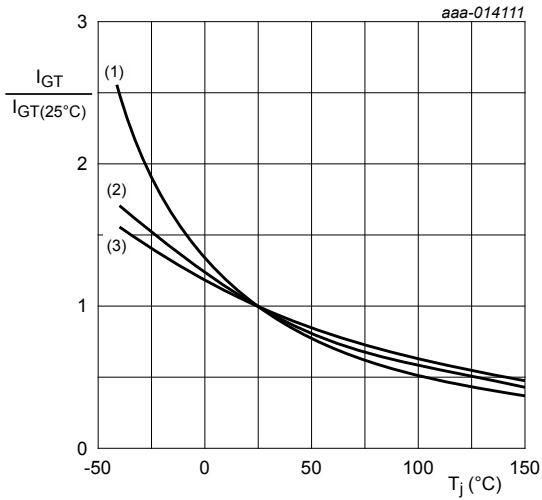


Fig. 7. Transient thermal impedance from junction to mounting base as a function of pulse width

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
I _{GT}	gate trigger current	V _D = 12 V; I _T = 100 mA; LD+ G+; T _j = 25 °C; Fig. 8	-	-	35	mA
		V _D = 12 V; I _T = 100 mA; LD+ G-; T _j = 25 °C; Fig. 8	-	-	35	mA
		V _D = 12 V; I _T = 100 mA; LD- G-; T _j = 25 °C; Fig. 8	-	-	35	mA
I _L	latching current	V _D = 12 V; I _G = 100 mA; LD+ G+; T _j = 25 °C; Fig. 9	-	-	50	mA
		V _D = 12 V; I _G = 100 mA; LD+ G-; T _j = 25 °C; Fig. 9	-	-	70	mA
		V _D = 12 V; I _G = 100 mA; LD- G-; T _j = 25 °C; Fig. 9	-	-	50	mA
I _H	holding current	V _D = 12 V; T _j = 25 °C; Fig. 10	-	-	50	mA
V _T	on-state voltage	I _T = 17 A; T _j = 25 °C; Fig. 11	-	1.25	1.5	V
V _{GT}	gate trigger voltage	V _D = 12 V; I _T = 100 mA; T _j = 25 °C; Fig. 12	-	0.8	1	V
		V _D = 400 V; I _T = 100 mA; T _j = 150 °C; Fig. 12	0.2	0.45	-	V
I _D	off-state current	V _D = 800 V; T _j = 25 °C	-	-	10	μA
		V _D = 800 V; T _j = 150 °C	-	-	2	mA
V _{CL}	clamping voltage	I _{CL} = 0.1 mA; t _p = 1 ms; T _j = 25 °C	850	-	-	V
Dynamic characteristics						
dV _D /dt	rate of rise of off-state voltage	V _{DM} = 536 V; T _j = 150 °C; (V _{DM} = 67% of V _{DRM}); exponential waveform; gate open circuit	500	-	-	V/μs
di _{com} /dt	rate of change of commutating current	V _D = 400 V; T _j = 150 °C; I _{T(RMS)} = 12 A; dV _{com} /dt = 20 V/μs; (snubberless condition); gate open circuit	5	-	-	A/ms



- (1) LD- G-
- (2) LD+ G+
- (3) LD+ G-

Fig. 8. Normalized gate trigger current as a function of junction temperature

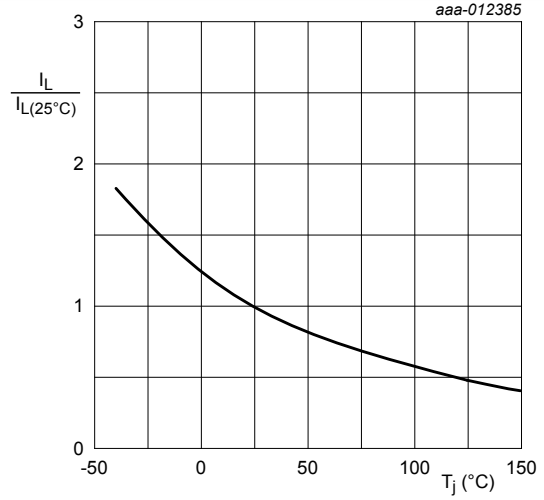


Fig. 9. Normalized latching current as a function of junction temperature

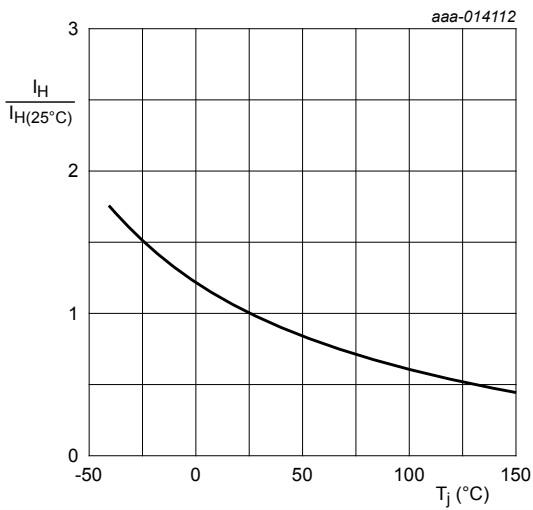
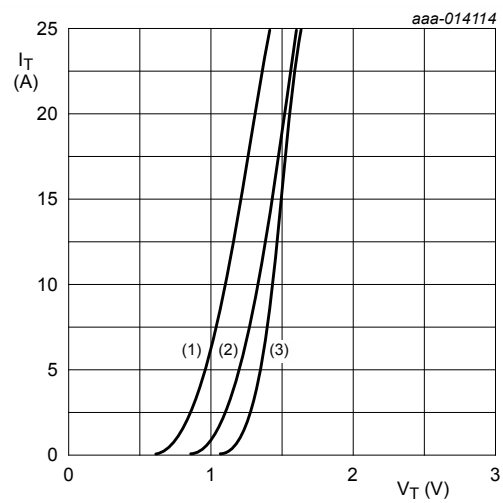


Fig. 10. Normalized holding current as a function of junction temperature



$V_o = 0.982\text{ V}$; $R_s = 0.029\ \Omega$

- (1) $T_j = 150^\circ\text{C}$; typical values
- (2) $T_j = 150^\circ\text{C}$; maximum values
- (3) $T_j = 25^\circ\text{C}$; maximum values

Fig. 11. On-state current as a function of on-state voltage

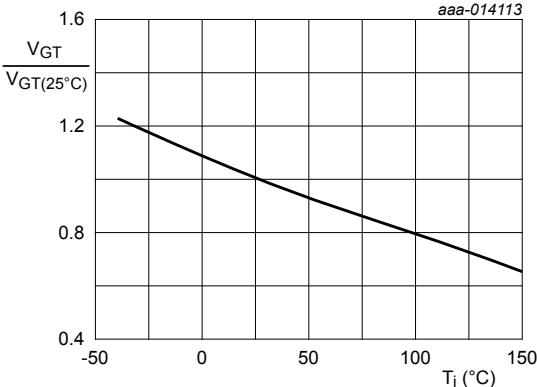


Fig. 12. Normalized gate trigger voltage as a function of junction temperature

11. Package outline

Plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped) SOT404



Dimensions (mm are the original dimensions)

Unit	A	A ₁	b	b ₂	c	D	D ₁	E	e	H _D	L _p	Q
max	4.5	1.40	0.85	1.45	0.64	11	1.6	10.3		15.8	2.9	2.6
nom									2.54			
min	4.1	1.27	0.60	1.05	0.46		1.2	9.7		14.8	2.1	2.2

sot404_po

Outline version	References			European projection	Issue date
	IEC	JEDEC	JEITA		
SOT404					-06-03-16- 13-02-25

Fig. 13. Package outline D2PAK (SOT404)

12. Legal information

12.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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13. Contents

1	General description	1
2	Features and benefits	1
3	Applications	1
4	Quick reference data	1
5	Pinning information	2
6	Ordering information	2
7	Marking	3
8	Limiting values	4
9	Thermal characteristics	7
10	Characteristics	8
11	Package outline	11
12	Legal information	12
12.1	Data sheet status	12
12.2	Definitions	12
12.3	Disclaimers	12
12.4	Trademarks	13

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