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VYBRIDRSERIESEC

VF3xxR, VF5xxR

Features

- Operating characteristics
  - Voltage range 3 V to 3.6 V
  - Temperature range(ambient) -40 °C to 85 °C
- ARM® Cortex® A5 Core features
  - Up to 400 MHz ARM® Cortex® A5 core
  - 32 KB/32 KB I/D L1 Cache
  - 1.6 DMIPS/MHz based on ARMv7 architecture
  - NEON™ MPE (Media Processing Engine) Co-processor
  - Double Precision Floating Point Unit
  - 512 KB L2 cache (on selected part numbers only)
- ARM Cortex M4 Core features
  - Up to 133 MHz ARM Cortex M4
  - Integrated DSP capability
  - 64 KB Tightly Coupled Memory (TCM)
  - 16 KB/16 KB I/D L1 Cache
  - 1.25 DMIPS/MHz based on ARMv7 architecture
- Clocks
  - 24 MHz crystal oscillator
  - 32 kHz crystal oscillator
  - Internal reference clocks (128 KHz and 24 MHz)
  - Phase Locked Loops (PLLs)
  - Low Jitter Digital PLLs
- System debug, protection, and power management
  - Various stop, wait, and run modes to provide low power based on application needs
  - Peripheral clock enable register can disable clocks to unused modules, thereby reducing currents
  - Low voltage warning and detect with selectable trip points
  - Illegal opcode and illegal address detection with programmable reset or processor exception response
  - Hardware CRC module to support fast cyclic redundancy checks (CRC)
  - 128-bit unique chip identifier
  - Hardware watchdog
  - External Watchdog Monitor (EWM)
  - Dual DMA controller with 32 channels (with DMAMUX)
- Debug
  - Standard JTAG
  - 16-bit Trace port
- Timers
  - Motor control/general purpose timer (FTM)
  - Periodic Interrupt Timers (PITs)
  - Low-power timer (LPTMR0)
  - IEEE 1588 Timer per MAC interface (part of Ethernet Subsystem)
- Communications
  - Six Universal asynchronous receivers/transmitters (UART)/Serial communications interface (SCI) with LIN, ISO7816, IrDA, and hardware flow control
  - Four Deserial Serial peripheral interface (DSPI)
  - Four Inter-Integrated Circuit (I2C) with SMBUS support
  - Dual USB OTG Controller + PHY
  - Dual 4/8 bit Secure Digital Host controller
  - Local Media Bus (MLB50)
  - Dual 10/100 Ethernet (IEEE 1588)
  - Dual FlexCAN3
- Security
  - ARM TrustZone including the TZ architecture
  - Secure Non-Volatile Storage (SNVS)
  - Real Time Clock
  - Real Time Integrity Checker (RTIC)
  - TrustZone Watchdog (TZ WDOG)
  - Trust Zone Address Space Controller
  - Random Number Generator
  - Hashing
  - Secure JTAG
- Memory Interfaces
  - 8/16-bit DRAM Controller with support for LPDDR2/DDR3 - Up to 400 MHz (ECC supported for 8-bit only and not 16-bit)
  - 8/16-bit NAND Flash controller with ECC (ECC supported for 8-bit only and not 16-bit)
  - Dual Quad SPI with XIP (Execute-In-Place)
  - 8/16/32-bit External bus (Flexbus)

NXP reserves the right to change the production detail specifications as may be required to permit improvements in the design of its products.

- Display and Video
  - Dual Display Control Unit (DCU) with support for color TFT display up to WVGA
  - Segmented LCD (3V Glass only) configurable as 40x4, 38x8, and 36x6
  - Video Interface Unit (VIU) for camera
  - Open VG Graphics Processing Unit (GPU)
  - VideoADC
- Analog
  - Dual 12-bit SAR ADC with 1MS/s
  - Dual 12-bit DAC
- Audio
  - Four Synchronous Audio Interface (SAI)
  - Enhanced Serial Audio Interface (ESAI)
  - Sony Philips Digital Interface (SPDIF), Rx and Tx
  - Asynchronous Sample Rate Converter (ASRC)
- Human-Machine Interface (HMI)
  - GPIO pins with interrupt support, DMA request capability, digital glitch filter.
  - Hysteresis and configurable pull up/down device on all input pins
  - Configurable slew rate and drive strength on all output pins
- On-Chip Memory
  - 512 KB On-chip SRAM with ECC
  - 1 MB On-chip graphics SRAM (no ECC). This depends on the part selected. Alternate configuration could be 512 KB graphics and 512 KB L2 cache.
  - 96 KB Boot ROM

Table of Contents

1 Ordering parts....5
1.1 Determining valid orderable parts....5
2 Part identification....5
2.1 Description....5
2.2 Part Number Format....5
2.3 Part Numbers....6
3 Terminology and guidelines....7
3.1 Definition: Operating requirement....7
3.2 Definition: Operating behavior....8
3.3 Definition: Attribute....8
3.4 Definition: Rating....8
3.5 Result of exceeding a rating....9
3.6 Relationship between ratings and operating requirements....9
3.7 Guidelines for ratings and operating requirements....10
3.8 Definition: Typical value....10
3.9 Typical Value Conditions....11
4 Handling ratings....11
4.1 ESD handling ratings....11
4.2 Thermal handling ratings....12
4.3 Moisture handling ratings....12
5 Operating Requirements....12
5.1 Thermal operating requirements....12
6 General....12
6.1 AC electrical characteristics....12
6.2 Nonswitching electrical specifications....13
6.2.1 VREG electrical specifications....13
6.2.1.1 HPREG electrical characteristics....13
6.2.1.2 LPREG electrical characteristics....14
6.2.1.3 ULPREG electrical characteristics....14
6.2.1.4 WBREG electrical characteristics....15
6.2.1.5 External NPN Ballast....15
6.2.2 LVD electrical specifications....17
6.2.2.1 Main Supply electrical characteristics 17
6.2.2.2 LVD DIG characteristics....18
6.2.3 LDO electrical specifications....18
6.2.3.1 LDO_1P1....18
6.2.3.2 LDO_2P5....19
6.2.3.3 LDO_3P0....19
6.2.4 Power consumption operating behaviors....20
6.2.5 USB PHY current consumption....20
6.2.5.1 Power Down Mode....20
6.2.6 EMC radiated emissions operating behaviors....21
6.2.7 EMC Radiated Emissions Web Search Procedure boilerplate....21
6.2.8 Capacitance attributes....21
7 I/O parameters....22
7.1 GPIO parameters....22
7.1.1 Output Buffer Impedance measurement....24
7.2 DDR parameters....24
8 Power supplies and sequencing....28
8.1 Power sequencing....28
8.2 Power supply....29
8.3 Absolute maximum ratings....31
8.4 Recommended operating conditions....32
8.5 Recommended Connections for Unused Analog Interfaces....33
9 Peripheral operating requirements and behaviours....34
9.1 Analog....34
9.1.1 12-bit ADC electrical characteristics....34
9.1.1.1 12-bit ADC operating conditions....34
9.1.1.2 12-bit ADC characteristics....35
9.1.2 12-bit DAC electrical characteristics....39
9.1.2.1 12-bit DAC operating requirements....39
9.1.2.2 12-bit DAC operating behaviors....39
9.1.3 VideoADC Specifications....43
9.2 Display and Video interfaces....45
9.2.1 DCU Switching Specifications....45
9.2.1.1 Interface to TFT panels (DCU0/1)....45
9.2.1.2 Interface to TFT LCD Panels—Pixel Level Timings....46
9.2.1.3 Interface to TFT LCD panels—access level....47
9.2.2 Video Input Unit timing....48
9.2.3 LCD driver electrical characteristics....49
9.3 Ethernet specifications....50
9.3.1 Ethernet Switching Specifications....50
9.3.2 Receive and Transmit signal timing specifications 50
9.3.3 Receive and Transmit signal timing specifications for MII interfaces....51
9.4 Audio interfaces....53

9.4.1 Enhanced Serial Audio Interface (ESAI) Timing Parameters....53
9.4.2 SPDIF Timing Parameters....55
9.4.3 SAI/I2S Switching Specifications....56
9.5 Memory interfaces....58
9.5.1 QuadSPI timing....58
9.5.2 NAND flash controller specifications....61
9.5.3 FlexBus timing specifications....64
9.5.4 DDR controller specifications....66
9.5.4.1 DDR3 Timing Parameters....66
9.5.4.2 DDR3 Read Cycle....68
9.5.4.3 DDR3 Write cycle....69
9.5.4.4 LPDDR2 Timing Parameter....70
9.5.4.5 LPDDR2 Read Cycle....71
9.5.4.6 LPDDR2 Write Cycle....72
9.6 Communication interfaces....73
9.6.1 MediaLB (MLB) DC Characteristics....73
9.6.2 MediaLB (MLB) Controller AC Timing Electrical Specifications....73
9.6.3 DSPI timing specifications....75
9.6.4 I2C timing....78
9.6.5 SDHC specifications....80
9.6.6 USB PHY specifications....81
9.7 Clocks and PLL Specifications....81
9.7.1 24 MHz Oscillator Specifications....81
9.7.2 32 KHz Oscillator Specifications....82
9.7.3 Fast internal RC oscillator (24 MHz) electrical characteristics....83
9.7.4 Slow internal RC oscillator (128 KHz) electrical characteristics....84
9.7.5 PLL1 and PLL2 (528 MHz System PLL) Electrical Parameters....84
9.7.6 PLL3 and PLL7 (480 MHz USB PLL) Electrical Parameters....84
9.7.7 PLL5 (Ethernet PLL) Electrical Parameters....85
9.7.8 PLL4 (Audio PLL) Electrical Parameters....85
9.7.9 PLL6 (Video PLL) Electrical Parameters....85
9.8 Debug specifications....86
9.8.1 JTAG electricals....86
9.8.2 Debug trace timing specifications....88
10 Thermal attributes....89
10.1 Thermal attributes....89
11 Dimensions....90
11.1 Obtaining package dimensions....90
12 Pinouts....91
12.1 Pinouts....91
12.2 Pinout diagrams....103
12.2.1 GPIO Mapping....105
12.2.2 Special Signal....109
13 Power Supply Pins....111
13.1 Power Supply Pins....111
14 Functional Assignment Pins....112
14.1 Functional Assignment Pins....112
15 Revision History....121

1 Ordering parts

1.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web.

1. To determine the orderable part numbers for this device, go to www.nxp.com and search the required part number. The part numbering format is described in the section that follows.

2 Part identification

2.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

2.2 Part Number Format

The figure below represents the format of part number of this device.

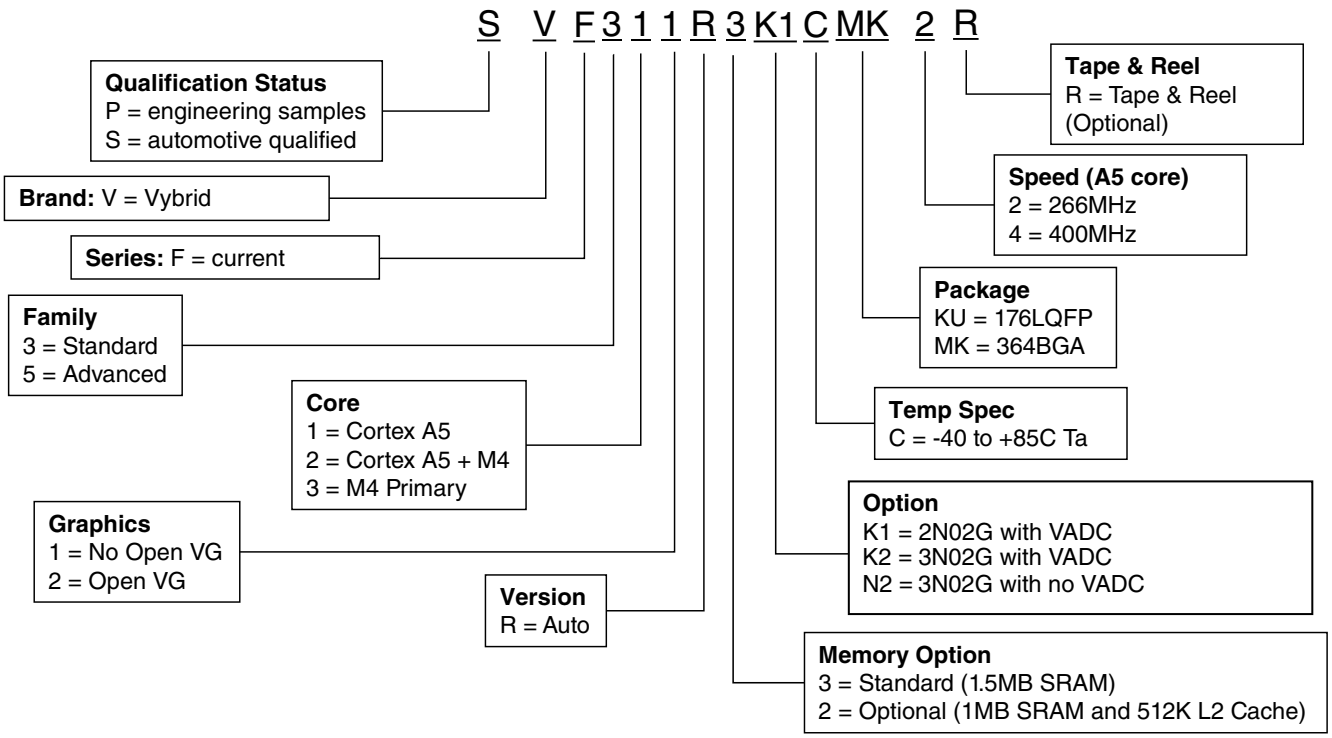


Figure 1. Part Number Format

2.3 Part Numbers

This table lists the part numbers on the device.

Part Number	Mask	VADC	Package	Description
SVF311R3K2CKU2	3N02G	YES	LQFP-EP 176 24*24*1.6	A5-266, 176LQFP-EP
SVF312R3K2CKU2	3N02G	YES	LQFP-EP 176 24*24*1.6	A5-266, OpenVG GPU, 176LQFP-EP
SVF321R3K2CKU2	3N02G	YES	LQFP-EP 176 24*24*1.6	A5-266, M4, 176LQFP-EP
SVF322R3K2CKU2	3N02G	YES	LQFP-EP 176 24*24*1.6	A5-266, M4, OpenVG GPU, 176LQFP
SVF331R3K2CKU2	3N02G	YES	LQFP-EP 176 24*24*1.6	A5-266, M4 Primary, 176LQFP-EP
SVF332R3K2CKU2	3N02G	YES	LQFP-EP 176 24*24*1.6	A5-266, M4 Primary, OpenVG GPU, 176LQFP-EP
SVF511R3K2CMK4	3N02G	YES	MAP 364 17*17*1.5 P0.8	A5-400, 364BGA
SVF512R3K2CMK4	3N02G	YES	MAP 364 17*17*1.5 P0.8	A5-400, OpenVG GPU, 364BGA
SVF521R3K2CMK4	3N02G	YES	MAP 364 17*17*1.5 P0.8	A5-400, M4, 364BGA
SVF522R2K2CMK4	3N02G	YES	MAP 364 17*17*1.5 P0.8	A5-400, M4, L2 Cache, OpenVG GPU, 364BGA
SVF522R3K2CMK4	3N02G	YES	MAP 364 17*17*1.5 P0.8	A5-400, M4, OpenVG GPU, 364BG

Table continues on the next page...

Part Number	Mask	VADC	Package	Description
SVF531R3K2CMK4	3N02G	YES	MAP 364 17*17*1.5 P0.8	A5-400, M4 Primary, 364BG
SVF532R2K2CMK4	3N02G	YES	MAP 364 17*17*1.5 P0.8	A5-400, M4 Primary, L2 Cache OpenVG GPU, 364BGA
SVF532R3K2CMK4	3N02G	YES	MAP 364 17*17*1.5 P0.8	A5-400, M4 Primary, OpenVG GPU, 364BGA
SVF311R3N2CKU2	3N02G	NO	LQFP-EP 176 24*24*1.6	A5-266, 176LQFP-EP
SVF312R3N2CKU2	3N02G	NO	LQFP-EP 176 24*24*1.6	A5-266, OpenVG GPU, 176LQFP-EP
SVF321R3N2CKU2	3N02G	NO	LQFP-EP 176 24*24*1.6	A5-266, M4, 176LQFP-EP
SVF322R3N2CKU2	3N02G	NO	LQFP-EP 176 24*24*1.6	A5-266, M4, OpenVG GPU, 176LQFP
SVF331R3N2CKU2	3N02G	NO	LQFP-EP 176 24*24*1.6	A5-266, M4 Primary, 176LQFP-EP
SVF332R3N2CKU2	3N02G	NO	LQFP-EP 176 24*24*1.6	A5-266, M4 Primary, OpenVG GPU, 176LQFP-EP
SVF511R3N2CMK4	3N02G	NO	MAP 364 17*17*1.5 P0.8	A5-400, 364BGA
SVF512R3N2CMK4	3N02G	NO	MAP 364 17*17*1.5 P0.8	A5-400, OpenVG GPU, 364BGA
SVF521R3N2CMK4	3N02G	NO	MAP 364 17*17*1.5 P0.8	A5-400, M4, 364BGA
SVF522R2N2CMK4	3N02G	NO	MAP 364 17*17*1.5 P0.8	A5-400, M4, L2 Cache, OpenVG GPU, 364BGA
SVF522R3N2CMK4	3N02G	NO	MAP 364 17*17*1.5 P0.8	A5-400, M4, OpenVG GPU, 364BG
SVF531R3N2CMK4	3N02G	NO	MAP 364 17*17*1.5 P0.8	A5-400, M4 Primary, 364BG
SVF532R2N2CMK4	3N02G	NO	MAP 364 17*17*1.5 P0.8	A5-400, M4 Primary, L2 Cache OpenVG GPU, 364BGA
SVF532R3N2CMK4	3N02G	NO	MAP 364 17*17*1.5 P0.8	A5-400, M4 Primary, OpenVG GPU, 364BGA

3 Terminology and guidelines

3.1 Definition: Operating requirement

An *operating requirement* is a specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip.

3.1.1 Example

This is an example of an operating requirement:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	0.9	1.1	V

3.2 Definition: Operating behavior

Unless otherwise specified, an *operating behavior* is a specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions.

3.2.1 Example

This is an example of an operating behavior:

Symbol	Description	Min.	Max.	Unit
I_{WP}	Digital I/O weak pullup/ pulldown current	10	130	µA

3.3 Definition: Attribute

An *attribute* is a specified value or range of values for a technical characteristic that are guaranteed, regardless of whether you meet the operating requirements.

3.3.1 Example

This is an example of an attribute:

Symbol	Description	Min.	Max.	Unit
CIN_D	Input capacitance: digital pins	—	7	pF

3.4 Definition: Rating

A *rating* is a minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:

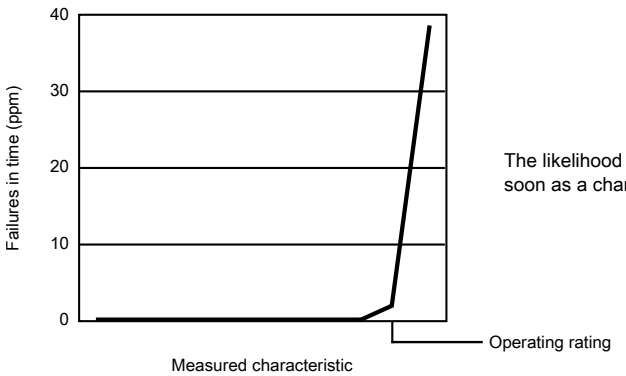
- *Operating ratings* apply during operation of the chip.
- *Handling ratings* apply when the chip is not powered.

3.4.1 Example

This is an example of an operating rating:

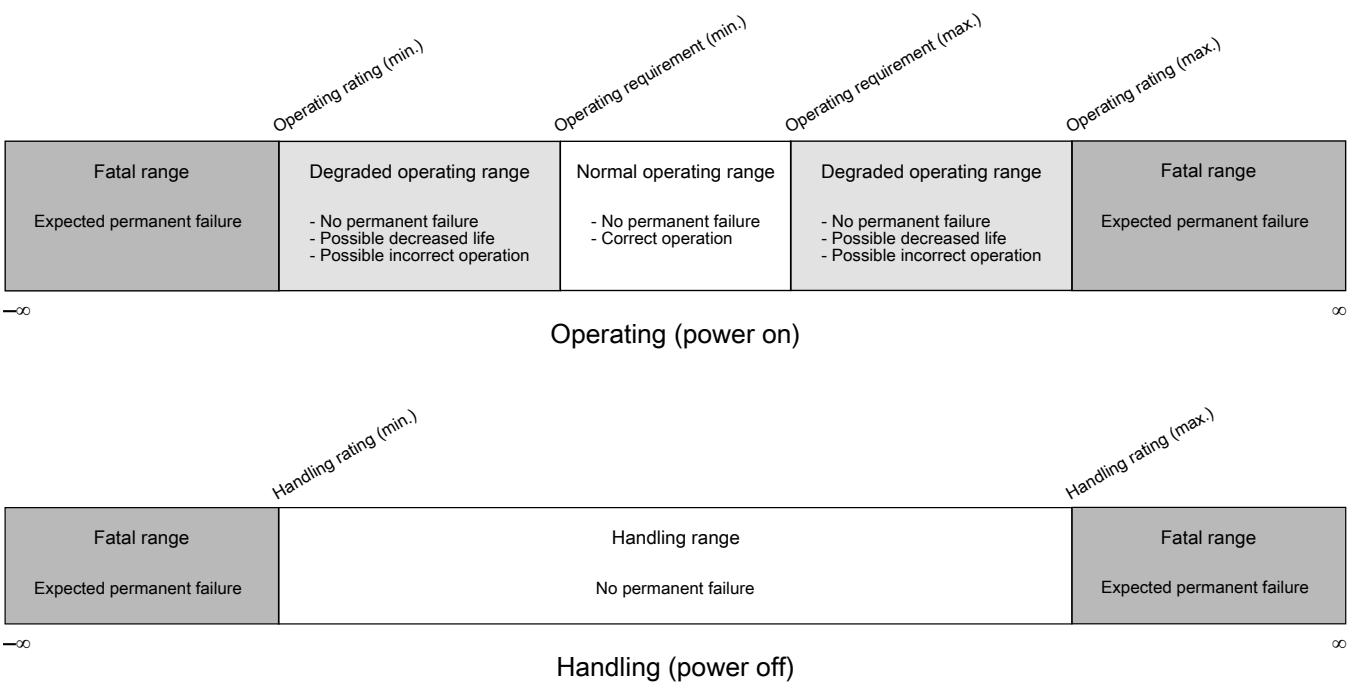
Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	–0.3	1.2	V

3.5 Result of exceeding a rating



The likelihood of permanent chip failure increases rapidly as soon as a characteristic begins to exceed one of its operating ratings.

3.6 Relationship between ratings and operating requirements



3.7 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

3.8 Definition: Typical value

A *typical value* is a specified value for a technical characteristic that:

- Lies within the range of values specified by the operating behavior
- Given the typical manufacturing process, is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions

Typical values are provided as design guidelines and are neither tested nor guaranteed.

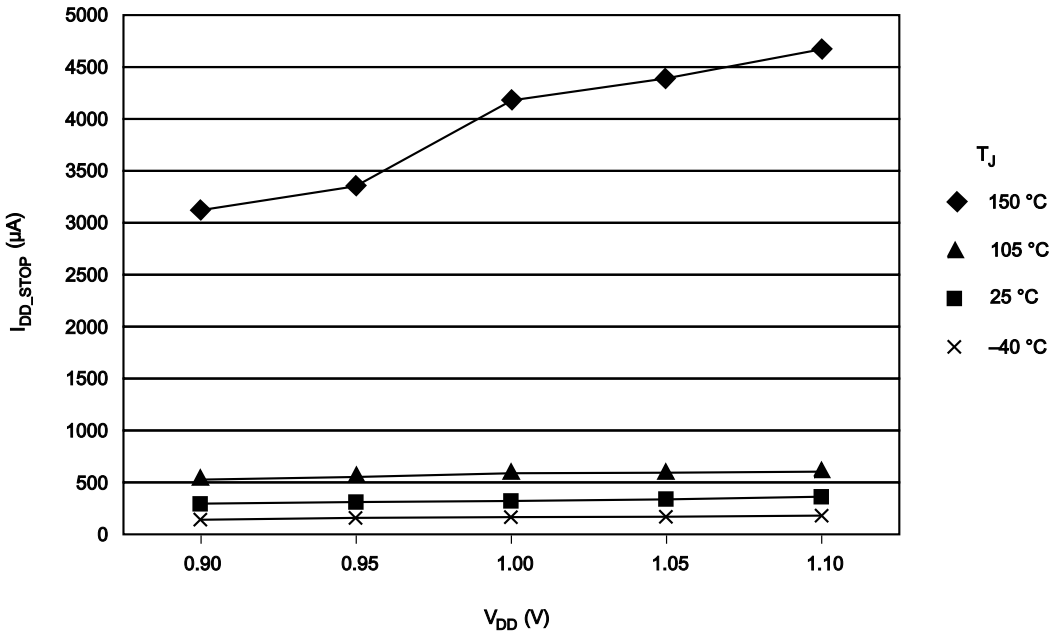
3.8.1 Example 1

This is an example of an operating behavior that includes a typical value:

Symbol	Description	Min.	Typ.	Max.	Unit
I_{WP}	Digital I/O weak pullup/pulldown current	10	70	130	µA

3.8.2 Example 2

This is an example of a chart that shows typical values for various voltage and temperature conditions:



3.9 Typical Value Conditions

Typical values assume you meet the following conditions (or other conditions as specified):

Symbol	Description	Value	Unit
T_A	Ambient temperature	25	°C
V_{DD}	3.3 V supply voltage	3.3	V

4 Handling ratings

4.1 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human body model	-2000	2000	V	1
V_{CDM}	Electrostatic discharge voltage, charged-device model	-500	500	V	2
I_{LAT}	Latch-up Current at ambient temperature of 85 °C	-100	100	mA	

1. Determined according to the AEC spec AEC-Q100-002 for HBM
2. Determined according to AEC spec AEC-Q100-011

4.2 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T_{STG}	Storage temperature	–55	150	°C	1
T_{SDR}	Solder temperature, lead-free	—	260	°C	2
	Solder temperature, leaded	—	245		

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

4.3 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

5 Operating Requirements

5.1 Thermal operating requirements

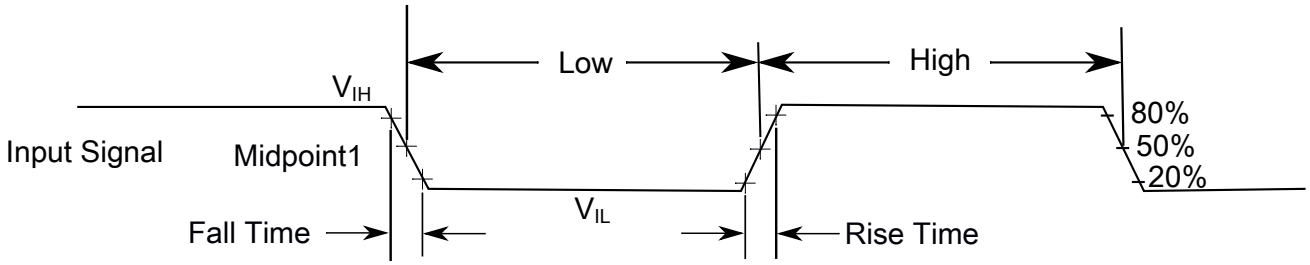
Table 1. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit
T_A	Ambient temperature	–40	85	°C
T_J	Junction temperature	—	105	°C

6 General

6.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.



The midpoint is $V_{IL} + (V_{IH} - V_{IL}) / 2$

Figure 2. Input signal measurement reference

6.2 Nonswitching electrical specifications

6.2.1 VREG electrical specifications

6.2.1.1 HPREG electrical characteristics

Table 2. HPREG electrical characteristics

Parameters	Min	Typ	Max	Unit	Comments
Power supply	3.0	3.3	3.6	V	-
Current Consumption	-	1.2	1.5	mA	@ no load
	-	2.0	2.5	mA	@ full load
Output current capacity	-	600	1200[1]	mA	DC load current
Output voltage @ no load		1.23	1.26	V	
Output voltage @ full load	1.20	1.21		V	
External decoupling cap	4.7		-	µF	-
	0.05		0.1	Ohms	ESR of external cap
			20	mOhms	Total effective PAD+PCB trace resistances
PSRR with 4.7uF output cap					
@ DC @noload			-48	dB	
@ DC @full load			-40		
@ worst case any frequency			-20		

1. This is peak and not continuous maximum value.

6.2.1.2 LPREG electrical characteristics

Table 3. LPREG electrical characteristics

Parameters	Min	Typ	Max	Unit	Comments
Power supply	3.0	3.3	3.6	V	
Current Consumption	350	400		µA	@ no load
	-	500	650	µA	@ full load
Output current capacity		100	200	mA	DC load current
Output voltage @ no load		1.22	1.240	V	
Output voltage @ full load	1.180			V	
External decoupling cap	4.7			µF	
	0.05		0.1	Ohms	ESR of external cap
			20	mOhms	Total PAD+PCB trace resistance
PSRR with 4.7uF output cap					
@ DC @noload			-40	dB	
@ DC @full load			-35		
Worst case @ any frequency			-12		

6.2.1.3 ULPREG electrical characteristics

Table 4. ULPREG electrical characteristics

Parameters	Min	Typ	Max	Unit	Comments
Power supply	3.0	3.3	3.6	V	
Current Consumption	1.88	2.3	2.86	µA	@ no load
	-	610	670	µA	@ full load
Output current capacity			20	mA	DC load current
Output voltage @ no load			1.175	V	
Output voltage @ full load	1.125			V	
PSRR with 500 pF output cap	-20			dB	Worst case at any frequency across corners
@ DC @noload			-50	dB	
@200KHz @noload			-37		
@ DC @full load			-42		
@200KHz @full load			-37		
Worst case @ any frequency @ any load			-15		

6.2.1.4 WBREG electrical characteristics

Table 5. WBREG electrical characteristics

Parameters	Min	Typ	Max	Unit	Comments
Power supply	3	3.3	3.6	V	-
Current Consumption	-	2	5	µA	@ no load
	-	2	5	µA	@ full load
Output current capacity	-	1	2	mA	DC load current
Output voltage @ no load		1.4	1.425	V	
Output voltage @ full load	1.375	1.398		V	
Output voltage programmability	1.4	1.4	1.7	V	16 steps of 25 mV each

6.2.1.5 External NPN Ballast

The internal main regulator requires an external NPN ballast transistor to be connected as shown in the following figure as well as an external capacitance to be connected to the device in order to provide a stable 1.2V digital supply to the device. The HPREG design allows for collector voltage lower than VDDREG value. See AN4807 at www.nxp.com .

NOTE

To not overload BCTRL output, collector voltage should appear no later than VDDREG / VDD33 (3.3V).

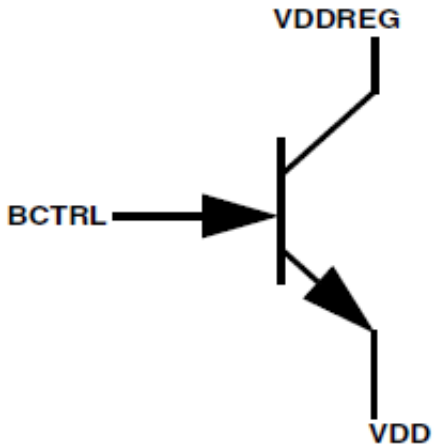


Figure 3. External NPN Ballast connections

Table 6. BCTRL OUTPUT specification

Parameter	Value	Comments
BCTRL OUTPUT specification	20mA	BCTRL driver can not drive more than 20mA current
Maximum pin voltage	VDDREG-0.5V	For Example, VDDREG =3.0V BCTRL should not exceed 2.5V.

Table 7. Assumptions For calculations

Parameter	Value
VDDREG	3.0V to 3.6V with typical value of 3.3V
Max DC Collector current	0.85A @85 °C
Emitter voltage	1.2V to 1.25V
Collector voltage	Equal to VDDREG

Table 8. General guidelines for selection of NPN ballast

Symbol	Parameters	Value	Unit	Comments
Hfe	Minimum DC current gain (Beta)	42.5		As BCTRL pin can not drive more than 20mA Minimum value of beta for a collector current of 0.85A comes out to be 42.5.
PD (Junction to ambient)	Minimum power dissipation @ TA=85 °C	2.04	W	Assuming 0.85A collector current with Collector voltage of Ballast 3.6V(max) we get VCE= 3.6V-1.2V=2.4V So power dissipated is 2.4V*0.85A=2.04W . This should be met for junction to ambient power dissipation spec of ballast

Table continues on the next page...

Table 8. General guidelines for selection of NPN ballast (continued)

Symbol	Parameters	Value	Unit	Comments
IcmaxDC peak	Maximum peak DC collector current	0.85	A	1.2A and above capacity device preferable
VBE	Maximum voltage that BCTRL pin can drive	1.25V for 0.85A @ 85 °C	V	For a VDDREG of 3.0 V (min.), BCTRL pin can drive voltage up to VDDREG - 0.5 V = 2.5 V. Since emitter of ballast is fixed at 1.25 V (max) if chosen ballast can supply 0.85 A collector current @ 85 °C with a base-to-emitter voltage of 1.25 V or lower, it is suitable for application.
Ft	Unity current gain Frequency of Ballast	50	MHz	

Reducing the collector-to-emitter voltage drop lowers the ballast transistor heat dissipation. This can be implemented in two ways:

1. By introducing series resistor or diode(s) between the collector and VDDREG (placed far enough from the transistor for proper cooling)
2. By connecting the collector to a separate lower-voltage supply

In both of the above cases the transistor has to stay away from the deep saturation region; otherwise, due to significant Hfe degradation, its base current exceeds the BCTRL output maximum value.

In general, the transistor must be selected such that its Vce saturation voltage is lower than the expected minimum Collector-Emitter voltage, and at the same time, the base current is less than 20 mA for the maximum expected collector current. More information can be found in collateral documentation at http://www.nxp.com

6.2.2 LVD electrical specifications

6.2.2.1 Main Supply electrical characteristics

Table 9. LVD_MAIN supply electrical characteristics

Main Supply LVD Parameters	Min	Typ	Max	Unit	Comments
Power supply	3.0	3.3	3.6	V	
Upper voltage threshold (value @27ºC)		2.76	2.915	V	
Lower voltage threshold (value @27ºC)	2.656	2.73		V	
Time constant of RC filter at LVD input (0.69*RC)	3.3			µs	3.3 V noise rejection at LVD comparator input

6.2.2.2 LVD DIG characteristics

Table 10. LVD DIG electrical specifications [HPREG(RUN MODE) and LPREG(STOP MODE)]

LVD DIG Parameters	Min	Typ	Max	Unit	Comments
Power supply	3.0	3.3	3.6	V	
Upper voltage threshold	1.135	1.16	1.185	V	
Lower voltage threshold	1.105	1.13	1.155	V	
Time constant of RC filter at LVD input	200			ns	1.2V noise rejection at the input of LVD comparator

Table 11. LVD DIG electrical specifications [ULPREG(STANDBY MODE)]

LVD DIG Parameters	Min	Typ	Max	Unit	Comments
Power supply	3.0	3.3	3.6	V	
Upper voltage threshold	1.105	1.13	1.155	V	
Lower voltage threshold	1.075	1.10	1.125	V	
Time constant of RC filter at LVD input	200			ns	1.2V noise rejection at the input of LVD comparator

6.2.3 LDO electrical specifications

6.2.3.1 LDO_1P1

Table 12. LDO_1P1 parameters

Specification	Min	Typ	Max	Unit	Comments
VDDIO	3	3.3	3.6	V	IO supply
VDD1P1_OUT	0.9	1.1	1.2	V	Regulator output
I_out	-		150	mA	>= 300mV drop out
Regulator output programming range	0.8	1.1	1.4	V	Programmable in 25mV steps
Brownout Voltage	0.85	0.94		V	
Brownout offset step	0	-	175	mV	Programmable in 25mV steps
Minimum external decoupling capacitor	1	-	-	µF	low ESR

For additional information, see the device reference manual.

6.2.3.2 LDO_2P5

Table 13. LDO_2P5 parameters

Specification	Min	Typ	Max	Unit	Comments
VDDIO	3	3.3	3.6	V	IO supply
VDD2P5_OUT	2.3	2.5	2.6	V	Regulator output
I_out	-		350	mA	@500mV drop out
Regulator output programming range	2.0	2.5	2.75	V	Programmable in 25mV steps
[P:][C:] Brownout Voltage	2.25	2.33		V	
Brownout offset step	0	-	175	mV	Programmable in 25mV steps
Minimum external decoupling capacitor	1	-	-	µF	low ESR

For additional information, see the reference manual.

6.2.3.3 LDO_3P0

Table 14. LDO_3P0 parameters

Specification	Min	Typ	Max	Unit	Comments
Input OTG VBUS Supply	4.4		5.25	V	
Input HOST VBUS Supply	4.4		5.25	V	
VDD3P0_OUT	2.9	3.0	3.1	V	Regulator output at default setting
I_out	-		50	mA	500 mV drop-out voltage
Regulator output programming range	2.625		3.4	V	Programmable in 25mV steps
[P:][C:] Brownout Voltage	2.75	2.85		V	
Brownout offset step	0	-	175	mV	Programmable in 25mV steps
Minimum external decoupling capacitor	1	-	-	µF	low ESR

NOTE

These values are with Anadig_REG_3P0[ENABLE_ILIMIT]= 0 and Anadig_REG_3P0[ENABLE_LINREG]= 1. It is required to set these values before using USB.

6.2.4 Power consumption operating behaviors

Table 15. Power consumption operating behaviors

Symbol	Description	Typ.[1]	Max.[2]	Unit	Notes
IDD_RUN	Run mode current — All functionalities of the chip available	400	850	mA	
IDD_WAIT	Wait mode high frequency current at 3.3 V ± 10%	80	500	mA	3
IDD_LPRUN	Low-power run mode current at 3.3 V ± 10%, 24MHz operation, PLL Bypass.	13	325	mA	4
IDD_ULPRUN	Ultra-low-power run mode current at 3.3 V ± 10%	12	395	mA	5
IDD_STOP	Stop mode current at 3.3 V ± 10%	7	300	mA	6
IDD_LPS2_{FIRC}/IDD_LPS3_{FIRC}	Low power stop 2/low power stop 3 with FIRC enabled, current at 3.3 V ± 10%	300	1300	uA	7
IDD_LPS2/IDD_LPS3	Low power stop 2/low power stop 3 with FIRC disabled, current at 3.3 V ± 10%	50	875	uA	7
IDD_VBAT	Battery backup mode	5	45	uA	8

1. The Typ numbers represent the average value taken from a matrix lot of parts across normal process variation at ambient temperature.
2. The Max numbers represent the single worst case value taken from a matrix lot of parts across normal process variation at maximum temperature.
3. CA5, CM4 cores halted
4. 24MHz operation, PLL Bypass
5. 32 kHz /128 kHz operation, PLL Off
6. Lowest power mode with all power retained, RAM retention and LVD protection.
7. Standby Mode. 64K and 16K RAM retention. ADCs/DACs optionally power-gated. RTC functional. Wakeup from interrupts.
8. All supplies OFF, SRTC, 32kXOSC ON, tampers and monitors ON. 128k IRC optionally ON.

6.2.5 USB PHY current consumption

6.2.5.1 Power Down Mode

Everything powered down, including the VBUS valid detectors, typ condition.

Table 16. USB PHY Current Consumption in Normal Mode

	USBx_VBUS (3.0V) Avg	VDD33_LDOIN (2.5V) Avg	VDD33_LDOIN (1.1V) Avg
Current	5.1 µA	1.7 µA	<0.5 µA

NOTE

The currents on the 2.5 voltage regulator and 3.0 voltage regulator were identified to be the voltage divider circuits in the USB-specific level shifters.

6.2.6 EMC radiated emissions operating behaviors

Table 17. EMC radiated emissions operating behaviors

Symbol	Condition[1]	Clocks	Frequency band [2]	Level (Typ)[3]	Unit
V_{EME}	Device Configuration, test conditions and EM testing per standard IEC 61967-2; Supply voltages: VDD= 5.0 V VDD33 = 3.3 V VDD15 = 1.5 V VDD12 = 1.2 V Temp = 25°C	FCPU = 396 MHz FBUS = 66 MHz External Crystal = 24 MHz	150 KHz – 50 MHz	22	dBµV
			50 MHz – 150 MHz	24	
			150 MHz – 500 MHz	25	
			500–1000	20	
			IEC level[4]	K	—

1. Measurements were made per IEC 61967-2 while the device was running basic application code.
2. Measurements were performed on the BGA364 version of the device
3. The reported emission level is the value of the maximum measured emission, rounded up to the next whole number, from among the measured orientations in each frequency range.
4. IEC Level Maximums: N ≤ 12dBmV, M ≤ 18dBmV, L ≤ 24dBmV, K ≤ 30dBmV, I ≤ 36dBmV, H ≤ 42dBmV

6.2.7 EMC Radiated Emissions Web Search Procedure boilerplate

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to www.nxp.com.
2. Perform a keyword search for “EMC design.”

6.2.8 Capacitance attributes

Table 18. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
C_{IN_A}	Input capacitance: analog pins	—	7	pF
C_{IN_D}	Input capacitance: digital pins	—	7	pF

7 I/O parameters

7.1 GPIO parameters

Table 19. GPIO DC operating conditions

Symbol	Parameter	Min	Typ	Max	Unit
vddi[1]	Core internal supply voltage		1.2		V
ovdd	I/O output supply voltage	3	3.3	3.6	V

1. This is internally controlled.

Table 20. GPIO DC Electrical characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
Voh	High-level output voltage	Ioh= -1mA VOH/VOL values are with respect to DSE=001[1]	ovdd-0.15			V
Vol	Low-level output voltage	Iol= 1mA			0.15	V
Vih [2]	High-Level DC input voltage		0.7*ovdd		ovdd	V
Vil[2]	Low-Level DC input voltage		0		0.3*ovdd	V
Vhys	Input Hysteresis	ovdd=3.3 V	250			mV
Vt+[2, 3]	Schmitt trigger VT+		0.5*ovdd			V
Vt-[2, 3]	Schmitt trigger VT-				0.5*ovdd	V
Iin[4]	Input current (no pull-up/down)	Vin = ovdd or 0	-1		1	uA
Iin_22pu	Input current (22KOhm PU)	Vin = 0			212	uA
		Vin = ovdd			1	
Iin_47pu	Input current (47KOhm PU)	Vin = 0			100	
		Vin = ovdd			1	
Iin_100pu	Input current (100KOhm PU)	Vin = 0			50	
		Vin = ovdd			1	
Iin_100pd	Input current (100KOhm PD)	Vin = 0			1	
		Vin = ovdd			50	

Table continues on the next page...

Table 20. GPIO DC Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
R_Keeper	Keeper Circuit Resistance	Vin = 0.3 x OVDD VI = 0.7 x OVDD	105		175	Ohm
Issod	Sink current in open drain mode	Vin = ovdd			7	mA
Issop	Sink/source current in Push Pull mode	Vin = ovdd			7	mA

1. For details about Software MUX Pad Control Register DSE bit, see IOMUX Controller chapter of the device reference manual.
2. To maintain a valid level, the transitioning edge of the input must sustain a constant slew rate (monotonic) from the current DC level through to the target DC level, VIL or VIH. Monotonic input transition time is from 0.1ns to 1s. Vil and Vih do not apply when hysteresis is enabled.
3. Hysteresis of 250 mV is guaranteed over all operating conditions when hysteresis is enabled.
4. Typ condition: typ model, 3.3V, and 25°C. Max condition: bcs model, 3.6V, and -40°C. Min condition: wcs model, 3.0V and 85 °C. These values are for digital IO buffer cells.

Table 21. GPIO AC Electrical Characteristics (3.3V power mode)

Symbol	Parameter	Drive strength[1]	Slew rate	Test conditions	Min	Max	Unit
tpr	IO Output Transition Times (PA1), rise/fall	Max 1 1 1	slow	15pF Cload on pad, input edge rate 200ps	1.70	1.81	ns
			fast		1.04	1.18	
		High 1 0 1	slow		2.30	2.44	
			fast		1.69	1.79	
		Medium 1 0 0	slow		3.07	3.31	
			fast		2.45	2.61	
		Low 0 1 1	slow		5.13	5.44	
			fast		4.79	5.18	
tpo	IO Output Propagation Delay (PA2), rise/fall	Max 1 1 1	slow	15pF Cload on pad, input edge rate 200ps	5.01	5.04	ns
			fast		3.06	3.10	
		High 1 0 1	slow		5.55	5.68	
			fast		3.52	3.55	
		Medium 1 0 0	slow		6.37	6.67	
			fast		4.04	4.11	
		Low 0 1 1	slow		7.39	7.60	
			fast		5.54	6.10	
tpv	Output Enable to Output Valid Delay, rise/fall	Max 1 1 1	slow	15pF Cload on pad, input edge rate 200ps, 0->1, 1->0 pad transitions	5.12	5.21	ns
			fast		3.18	3.28	
		High 1 0 1	slow		5.72	5.80	
			fast		3.67	3.71	
		Medium 1 0 0	slow		6.55	6.80	

Table continues on the next page...

Table 21. GPIO AC Electrical Characteristics (3.3V power mode) (continued)

Symbol	Parameter	Drive strength[1]	Slew rate	Test conditions	Min	Max	Unit
			fast		4.06	4.09	
		Low 0 1 1	slow		7.80	8.19	
			fast		5.72	6.22	
tpi	Input Pad Propagation Delay rise/fall	without hysteresis	-	150f Cload on, input edge rate from pad =1.2ns	1.06	1.31	ns
		with hysteresis	-		1.22	1.41	

1. The drive strengths are controlled by the DSE bit of the Software MUX Pad Control Register. For details, see IOMUX Controller chapter of the device reference manual.

7.1.1 Output Buffer Impedance measurement

Table 22. Output Buffer Average Impedance (3.3V power mode)

Symbol	Parameter	Drive strength[1]	Min	Typ	Max	Unit
Rdrv	Output driver impedance	0 0 1	116	150	220	Ohm
		0 1 0	58	75	110	
		0 1 1	39	50	73	
		1 0 0	30	37	58	
		1 0 1	24	30	46	
		1 1 0 Extra drive strength	20	25	38	
		1 1 1	17	20	32	

1. The drive strengths are controlled by the DSE bit of the Software MUX Pad Control Register. For details, see IOMUX Controller chapter of the device reference manual.

7.2 DDR parameters

Table 23. DDR operating conditions

Symbol	Parameter	Min	Typ	Max	Unit
vddi	Core internal supply voltage	1.16	1.23	1.26	V
ovdd	I/O output supply voltage (DDR3 mode)	1.425	1.5	1.575	V
ovdd	I/O output supply voltage (LPDDR2 mode)	1.14	1.2	1.26	V
vdd2p5	I/O PD predriver and level shifters supply voltage	2.25	2.5	2.75	V

Table 24. LPDDR2 mode DC Electrical characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Notes
Voh	High-level output voltage		0.9*ovdd			V	Note that the JEDEC LPDDR2 specification (JESD209_2B) supersedes any specification in this document.
Vol	Low-level output voltage				0.1*ovdd	V	
Vref	Input reference voltage		0.49*ovdd	0.5*ovdd	0.51*ovdd	V	
Vih(dc)	DC input high voltage		Vref+0.13		ovdd	V	
Vil(dc)	DC input low voltage		ovss		Vref-0.13	V	
Vih(diff)	DC differential input logic high		0.26		Note[1]	V	
Vil(diff)	DC differential input logic low		Note[1]		-0.26	V	
Iin[2]	Input current (no pull-up/ down)	Vin = ovdd or 0			2.5	uA	
Tri-state I/O supply current[2]	Icc-ovdd	Vin = ovdd or 0			4		
Tri-state vdd2p5 supply current[2]	Icc-vdd2p5	Vi = vddi or 0			1.5		
Tri-state core supply current[2]	Icc-vddi				1		
Driver unit (240 Ohm) calibration resolution	Rres				10	Ohm	

1. The single-ended signals need to be within the respective limits (Vih(dc) max, Vil(dc) min) for single-ended signals as well as the limitations for overshoot and undershoot.
2. Typ condition: typ model, 1.2 V, and 25 °C junction. Max condition: bcs model, 1.26V, and -40 °C. Min condition: wcs model, 1.14V, and Tj 125 °C.

Table 25. DDR3 mode DC Electrical characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Notes
Voh	High-level output voltage		0.8*ovdd			V	Note that the JEDEC JESD79_3E specification supersedes any
Vol	Low-level output voltage	Iol= 1mA			0.2*ovdd	V	

Table continues on the next page...

Table 25. DDR3 mode DC Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit	Notes
Vref	Input reference voltage		0.49*ovdd	0.5*ovdd	0.51*ovdd	V	specification in this document
Vih(dc)	DC input high voltage		Vref+0.1		ovdd	V	
Vil(dc)	DC input low voltage		ovss		Vref-0.1	V	
Vih(diff)	DC differential input logic high		0.2		Note[1]	V	
Vil(diff)	DC differential input logic low		Note[1]		-0.2	V	
Vtt[2]	Termination voltage	Vin = ovdd or 0	0.49*ovdd	0.5*ovdd	0.51*ovdd		
Iin[3]	Input current (no pullup/ pulldown)	Vi = 0 Vi = ovdd			3	uA	
Tri-state I/O supply current[3]	Icc-ovdd	Vin = ovdd or 0			5		
Tri-state vdd2p5 supply current[3]	Icc-vdd2p5	Vi = vddi or 0			1.5		
Tri-state core supply current[3]	Icc-vddi				1		
Driver unit (240 Ohm) calibration resolution	Rres				10	Ohm	

1. The single-ended signals need to be within the respective limits (Vih(dc) max, Vil(dc) min) for single-ended signals as well as the limitations for overshoot and undershoot.
2. Vtt is expected to track ovdd/2.
3. Typ condition: typ model, 1.5 V, and 25 °C. Max condition: bcs model, 1.575V, and -40 °C. Min condition: wcs model, 1.425V, and max Tj °C 125 °C junction

Table 26. LPDDR2 mode AC Electrical characteristics

Symbol	Parameter	Test condition	Min	Max	Unit	Notes
Vih(ac)	AC input logic high		Vref+0.22	ovdd	V	Note that the Jedec LPDDR2 specification (JESD209-2B) supersedes any specification in this document.
Vil(ac)	AC input logic low			Vref-0.22	V	
Vidh(ac)[1]	AC differential input high voltage		0.44	-	V	

Table continues on the next page...

Table 26. LPDDR2 mode AC Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min	Max	Unit	Notes
Vidl(ac)[1]	AC differential input low voltage			0.44	V	
Vix(ac)[2]	AC differential input crosspoint voltage	Relative to ovdd/2	-0.12	0.12	V	
Vpeak	Over/undershoot peak			0.35	V	
Varea	Over/undershoot area (above ovdd or below ovss)	at 800MHz data rate		0.3	V*ns	
tsr	Single output slew rate		0.4	2	V/ns	
tskd	Skew between pad rise/fall asymmetry + skew cased by SSN			0.2	ns	

1. Vid(ac) specifies the input differential voltage |Vtr-Vcp| required for switching, where Vtr is the “true” input signal and Vcp is the “complementary” input signal. The Minimum value is equal to Vih(ac)-Vil(ac).
2. The typical value of Vix(ac) is expected to be about 0.5*ovdd, and Vix(ac) is expected to track variation of ovdd. Vix(ac) indicates the voltage at which differential input signal must cross.

Table 27. DDR3 mode AC Electrical characteristics

Symbol	Parameter	Test condition	Min	Max	Unit	Notes
Vih(ac)	AC input logic high		Vref+0.175	ovdd	V	Note that the JEDEC JESD79_3E specification supersedes any specification in this document
Vil(ac)	AC input logic low		ovss	Vref-0.175	V	
Vidh(ac)[1]	AC differential input high voltage		0.35	-	V	
Vidl(ac)[1]	AC differential input low voltage		0.35		V	
Vix(ac)[2]	AC differential input crosspoint voltage	relative to ovdd/2	Vref-0.15	Vref+0.15	V	
Vpeak	Over/undershoot peak			0.4	V	
Varea	Over/undershoot area (above ovdd or below ovss)	at 800 MHz data rate		0.5	V*ns	
tsr	Single output slew rate		0.4	2	V/ns	

Table continues on the next page...

Table 27. DDR3 mode AC Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min	Max	Unit	Notes
tskd	Skew between pad rise/fall asymmetry + skew cased by SSN			0.2	ns	

1. Vid(ac) specifies the input differential voltage |Vtr-Vcp| required for switching, where Vtr is the “true” input signal and Vcp is the “complementary” input signal. The Minimum value is equal to Vih(ac)-Vil(ac).
2. The typical value of Vix(ac) is expected to be about 0.5*ovdd, and Vix(ac) is expected to track variation of ovdd. Vix(ac) indicates the voltage at which differential input signal must cross.

8 Power supplies and sequencing

8.1 Power sequencing

Table 28. Power sequencing

Power Supply (PKG Level)	Board Level Power Nets	Parameters	Power Order	Comment
VBAT	VBAT	Battery supply in case of LDOIN fails	NA	
VDD33_LDOIN	VDD33	LDO input supply (LDO1P1, LDO2P5, LDO1P1_RTC)	1	VDD33_LDOIN,VDDREG and VDD33 should come from a common supply source (represented as 3.3V SMPS in the Figure 4)
VDDREG	VDD33	Device PMU regulator and External ballast supply	1	
VDD33	VDD33	GPIO 3.3V IO supply, LCD Supply	1	
SDRAMC_VDD1P5	SDRAMC_VDD1P5	1.2/1.5 DDR Main IO supply	NA	In case the Ballast transistor’s collector is connected to the 1.5V DRAM supply (instead of the 3.3V supply), turn this 1.5V supply on before turning on the 3.3V.
VDDA33_ADC	VDDA33_ADC	3.3V supply for ADC, DAC and IO segment	1	
VREFH_ADC	VREFH_ADC	High Reference of ADC, DAC	1	
VDDA33_AFE	VDDA33_AFE	3.3V supply of AFE (Video ADC)	1	
VDD12_AFE	VDD	1.2V supply for AFE (Video ADC)	2	
FA_VDD	VDD	Shorted with VDD at Board Level in 364BGA (Test pin only)	NA	
VDD	VDD	1.2V core supply from External ballast	2	
USB0_VBUS 1	USB_VBUS	VBUS supply for USB	NA	
USB1_VBUS 2	USB_VBUS	VBUS supply for USB	NA	

1. Power sequencing of USB0_VBUS is independent of any other power supply.

2. Power sequencing of USB1_VBUS is independent of any other power supply.

NOTE

NA stands for no sequencing needs, for example, the supply can come in any order.

NOTE

All supplies grouped together e.g. 1,2, others. These have no power sequencing restriction in between them.

NOTE

If none of the SDRAMC pins are connected on the board, the SDRAMC supply could be left floating.

NOTE

At power up, 1.2V supply will follow 3.3V supply. At power down, it should be checked that 1.2V falls before 3.3V.

NOTE

The standby current on USBx_VBUS is 300 - 500 uA. This is well below the 2.5 mA limit set by the USB 2.0 specification. This supply will be ON for applications that need to monitor the USB bus during standby. This supply can be turned-off during standby in applications that cannot tolerate the standby current and do not monitor the USB bus.

8.2 Power supply

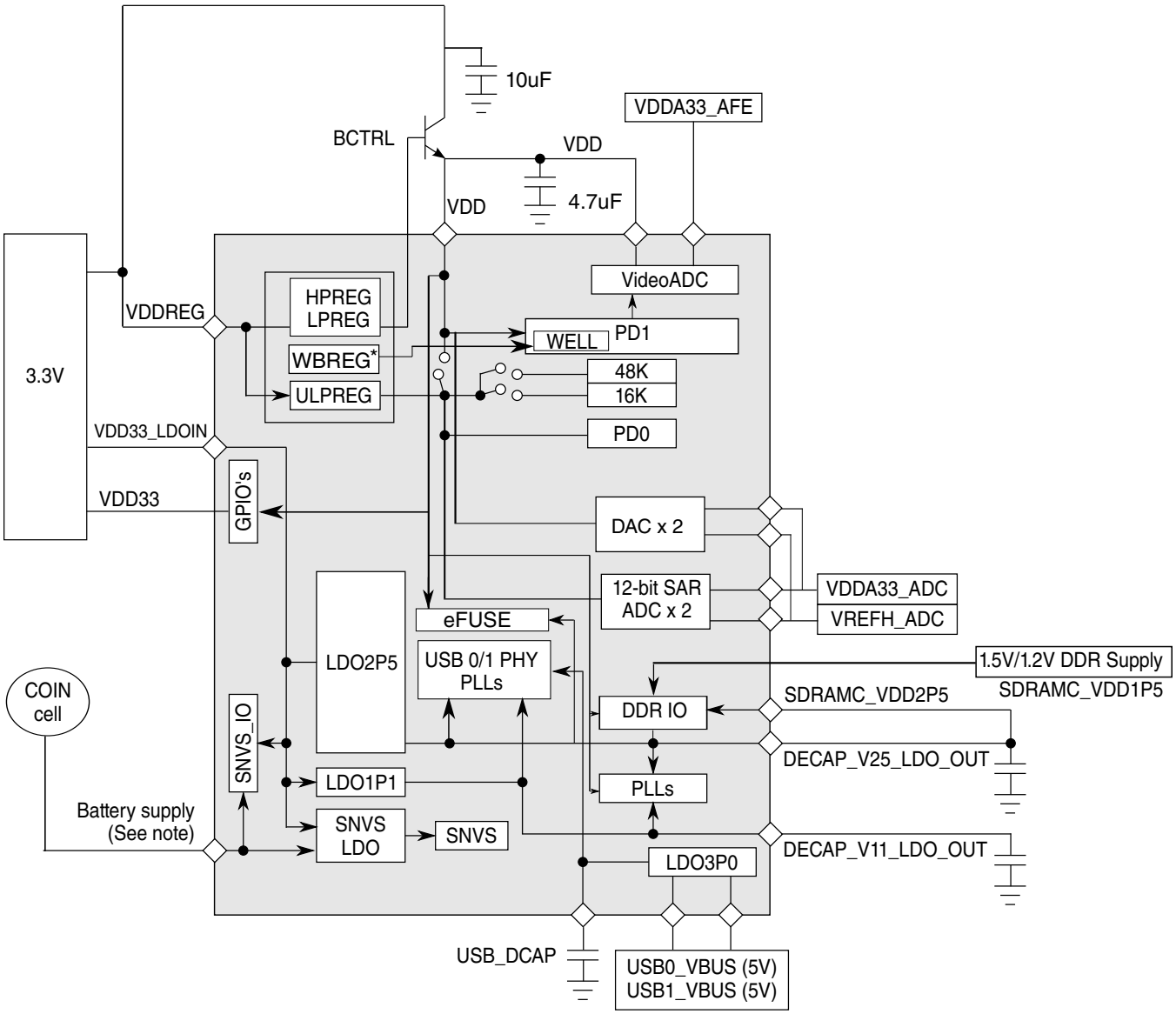


Figure 4. Power supply

NOTE

VBAT is the backup battery supply. If not required, then VBAT should be tied to VDDREG.

NOTE

WBREG is the Well Bias Regulator. Supplies PD1 WELL during well bias modes.

8.3 Absolute maximum ratings

NOTE

These are the values above which device can get damaged. Refer to the recommended operating conditions table for intended use case values

Table 29. Absolute maximum ratings

Symbol	Parameters	Min	Max	Unit
USB0_VBUS	VBUS supply for USB	-	5.25	V
USB1_VBUS	VBUS supply for USB	-	5.25	V
USB_DCAP	USB LDO 5V->3.3V Outpu	-0.3	3.6	V
USB0_DP	USB*x* data line input voltage	-0.3	3.6	V
USB0_DN				
USB1_DP				
USB1_DN				
VBAT	Battery supply in case of LDOIN fails	-0.3	3.6	V
VDD33_LDOIN	LDO input supply	-0.3	3.6	V
DECAP_V11_LDO_OUT	LDO 3.3V -> 1.1V Output	-0.3	1.3	V
DECAP_V25_LDO_OUT	LDO 3.3V -> 2.5 Output for PLL, DDR, EFUSE	-0.3	3.6	V
VDD33	GPIO 3.3V IO supply	-0.3	3.6	V
VDDREG	Device PMU regulator and External ballast supply	-0.3	3.6	V
VDDA33_ADC	3.3V supply for ADC, DAC and IO segment	-0.3	3.6	V
VREFH_ADC	3.3V supply of AFE (Video ADC)	-0.3	3.6	V
VDDA33_AFE	3.3V supply of AFE (Video ADC)	-0.3	3.6	V
VDD12_AFE	1.2V supply for AFE (Video ADC)	-0.3	1.3	V
FA_VDD	Test purpose only	-0.3	1.3	V
VDD	1.2V core supply	-0.3	1.3	V
SDRAMC_VDD1P5	1.2/1.5 DDR Main IO supply	-0.3	1.975	V
SDRAMC_VDD2P5	2.5V DDR pre-drive supply DD2P5_LDO_OUT	-0.3	3.6	V

8.4 Recommended operating conditions

Table 30. Recommended operating conditions

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
USB0_VBUS	VBUS supply for USB w.r.t USB0_GND		4.4	5	5.25	V
USB1_VBUS	VBUS supply for USB w.r.t USB1_GND		4.4	5	5.25	V
USB_DCAP	USB LDO 5V->3 V Output	External DCAP (10uF termination for USBREG)		3		V
VBAT	Battery supply in case of LDOIN fails	External CAP 0.1uF	2.4	3.3	3.6	V
VDD33_LDOIN	LDO input supply		3	3.3	3.6	V
DECAP_V11_LDO_OUT	LDO 3.3V -> 1.1V Output	Recommended External DCAP: 1uF(Min) 10uF (Max)		1.1		V
DECAP_V25_LDO_OUT	LDO 3.3V -> 2.5 Output for PLL, DDR pre-driver, EFUSE	Recommended External DCAP: 1uF(Min) 10uF (Max)		2.5		V
VDD33	GPIO 3.3V IO supply	External CAP (10uF)	3	3.3	3.6	V
VDDREG	Device PMU regulator and External ballast supply	External CAP (10uF)	3	3.3	3.6	V
VDDA33_ADC	3.3V supply for ADC, DAC and IO segment	External CAP (10uF)	3	3.3	3.6	V
VREFH_ADC	High reference voltage for ADC and DAC	Relation with VDDDA33_ADC (1uF)	2.5	3.3	VDDA33_ADC	V
VREFL_ADC	Low reference voltage for ADC and DAC	External CAP (10uF)		0		V
VDDA33_AFE	3.3V supply of AFE (Video ADC)	External CAP 10uF	3	3.3	3.6	V
VDD12_AFE	1.2V supply for AFE (Video ADC)		1.16	1.23	1.26	V
FA_VDD	For testing purpose only should be shorted to VDD on board.		1.16	1.23	1.26	V
VDD[1]	1.2V core supply	4.7uF with a low ESR value (100 milliohms)	1.16	1.23	1.26	V
USB0_GND	Ground supply for USB			0		V
USB1_GND	Ground supply for USB			0		V
VSS_KEL0	USB LDO ground output			0		V
VSS	VSS ground			0		V
VSSA33_ADC	Ground supply for ADC, DAC and IO segment			0		V

Table continues on the next page...

Table 30. Recommended operating conditions (continued)

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
VSSA33_AFE	Ground supply of AFE (Video ADC)			0		V
VSS12_AFE	Ground supply for AFE (Video ADC)			0		V
SDRAMC_VDD1P5	LPDDR2	External CAP 10uF	1.142	1.2	1.26	V
SDRAMC_VDD1P5	DDR3	External CAP 10uF	1.425	1.5	1.575	V
SDRAMC_VDD2P5	2.5V DDR pre-drive supply DD2P5_LDO_OUT	External CAP 10uF	2.25	2.5	2.75	V
-	Maximum power supply ramp rate (Slew limit for power-up)		-		0.1	V/us

1. For customer applications, this is governed by ballast output which is controlled by the device and appropriate voltage ranges are maintained.

8.5 Recommended Connections for Unused Analog Interfaces

NOTE

There are two options to handle unused power pins:

1. Connect all unused supplies to their respective voltage. To save the power, do not enable the module and/or do not enable clock gate to the module.
2. Keep all unused supplies floating.

If pin is shared by several peripheral, then all peripherals connected to multiplexer have to be powered. For example: if pin is shared by GPIO and ADC input and GPIO functionality is used, then ADC has to be powered due to internal structure of the multiplexer. Keep unused input signals grounded if power pins are powered. Keep unused input signals floating if power pins are floating. Keep unused output signals floating.

Module	Name	Recommendation if Unused
ADC	VDDA33_ADC	3.3V or float (Note: Powers both ADC and DAC)
	VREFH_ADC, VREFL_ADC	VREFH_ADC same as VDDA33_ADC VREFL_ADC ground or float
	ADC0SE8, ADC0SE9, ADC1SE8, ADC1SE9	Ground or float
CCM	LVDS0P, LVDS0N	Float
DAC	DACO0, DACO1	Float

Table continues on the next page...

Module	Name	Recommendation if Unused
USB	USB_DCAP, USB0_VBUS, USB1_VBUS	Connect USBx_VBUS and USB_DCAP together and tie to ground through a 10K ohm resistor. Do NOT tie directly to ground, latch-up risk.
	USB0_GND, USB1_GND	Ground
	USB0_VBUS_DETECT, USB1_VBUS_DETECT	Float
	USB0_DM, USB0_DP, USB1_DM, USB1_DP	Float
Video ADC	VDDA33_AFE	3.3V or Float
	VDD12_AFE	1.2V or Float
	VADC_AFE_BANDGAP	Float
	VADCSE0, VADCSE1, VADCSE2, VADCSE3	Ground or Float

9 Peripheral operating requirements and behaviours

9.1 Analog

9.1.1 12-bit ADC electrical characteristics

9.1.1.1 12-bit ADC operating conditions

Table 31. 12-bit ADC Operating Conditions

Characteristic	Conditions	Symb	Min	Typ [1]	Max	Unit	Comment
Supply voltage	Absolute	V_{DDAD}	2.5	-	3.6	V	-
	Delta to V_{DDAD} (VDD-VDDAD) [2]	ΔVDDAD	-100	0	100	mV	-
Ground voltage	Delta to V_{SSAD} (VSS-VSSAD) [2]	ΔVSSAD	-100	0	100	mV	-
Ref Voltage High	-	V_{REFH}	1.5	V_{DDAD}	V_{DDAD}	V	-
Ref Voltage Low	-	V_{REFL}	V_{SSAD}	V_{SSAD}	V_{SSAD}	V	-
Input Voltage	-	V_{ADIN}	V_{REFL}	-	V_{REFH}	V	-
Input Capacitance	8/10/12 bit modes	C_{ADIN}	-	1.5	2	pF	-
Input Resistance	ADLPC=0, ADHSC=1	R_{ADIN}	-	5	7	kohms	-
	ADLPC=0, ADHSC=0		-	12.5	15	kohms	-
	ADLPC=1, ADHSC=0		-	25	30	kohms	-

Table continues on the next page...

Table 31. 12-bit ADC Operating Conditions (continued)

Characteristic	Conditions	Symb	Min	Typ [1]	Max	Unit	Comment
Analog Source Resistance	12 bit mode f_{ADCK} = 40MHz ADLSMP=0, ADSTS=10, ADHSC=1	R_{AS}	-	-	1	kohms	T_{samp}=150 ns
R_{AS} depends on Sample Time Setting (ADLSMP, ADSTS) and ADC Power Mode (ADHSC, ADLPC). See charts for Minimum Sample Time vs R_{AS}							
ADC Conversion Clock Frequency	ADLPC=0, ADHSC=1 12 bit mode	f_{ADCK}	4	-	40	MHz	-
	ADLPC=0, ADHSC=0 12 bit mode		4	-	30	MHz	-
	ADLPC=1, ADHSC=0 12 bit mode		4	-	20	MHz	-

1. Typical values assume VDDAD = 3.3 V, Temp = 25°C, f_{ADCK}=20 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
2. DC potential difference

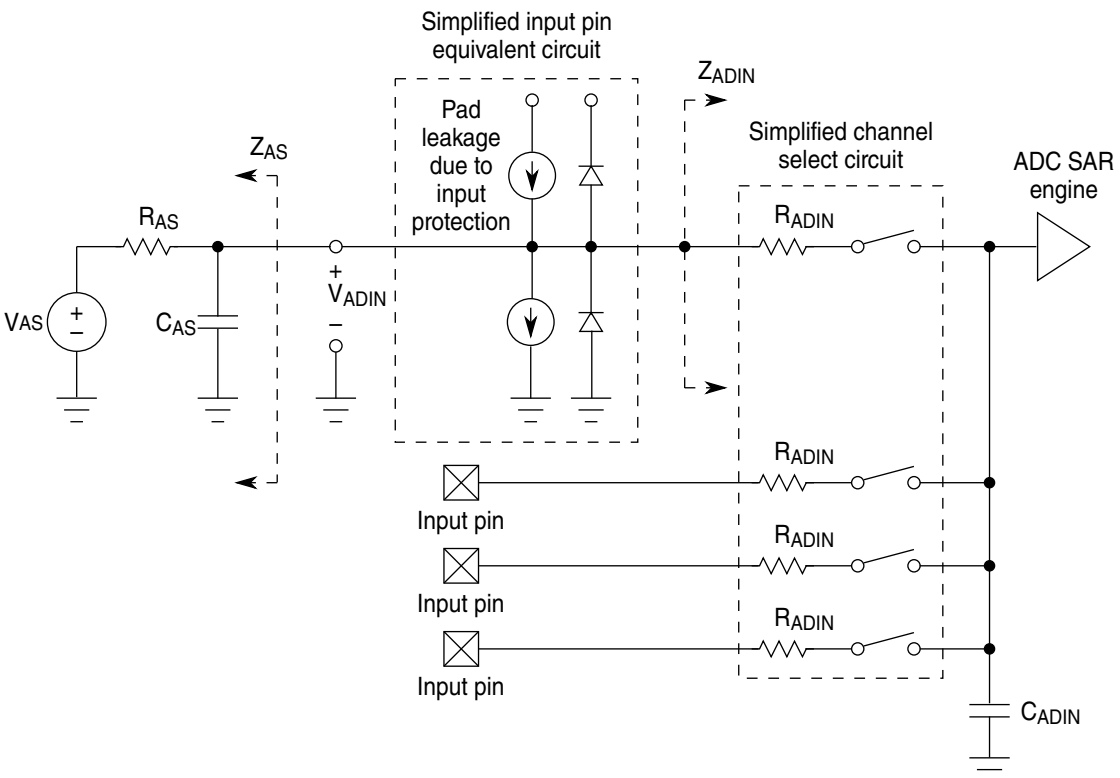


Figure 5. 12-bit ADC Input Impedance Equivalency Diagram

9.1.1.2 12-bit ADC characteristics

Table 32. 12-bit ADC Characteristics (V_{REFH} = V_{DDAD}, V_{REFL} = V_{SSAD})

Characteristic	Conditions[1]	Symb	Min	Typ [2]	Max	Unit	Comment
Supply Current	ADLPC=1, ADHSC=0	I_{DDAD}		250		µA	ADLSMP=0 ADSTS=10 ADCO=1
	ADLPC=0, ADHSC=0			350			
	ADLPC=0, ADHSC=1			400			
Supply Current	Stop, Reset, Module Off	I_{DDAD}		0.01	0.8	µA	
ADC Asynchronous Clock Source	ADHSC=0	f_{ADACK}		10		MHz	t_{ADACK} = 1/f_{ADACK}
	ADHSC=1			20			
Sample Cycles	ADLSMP=0, ADSTS=00	Csamp		2		cycles	
	ADLSMP=0, ADSTS=01			4			
	ADLSMP=0, ADSTS=10			6			
	ADLSMP=0, ADSTS=11			8			
	ADLSMP=1, ADSTS=00			12			
	ADLSMP=1, ADSTS=01			16			
	ADLSMP=1, ADSTS=10			20			
	ADLSMP=1, ADSTS=11			24			
Conversion Cycles	ADLSMP=0 ADSTS=00	Cconv		28		cycles	
	ADLSMP=0 ADSTS=01			30			
	ADLSMP=0 ADSTS=10			32			
	ADLSMP=0 ADSTS=11			34			
	ADLSMP=1 ADSTS=00			38			
	ADLSMP=1 ADSTS=01			42			
	ADLSMP=1 ADSTS=10			46			
	ADLSMP=1, ADSTS=11			50			
Conversion Time	ADLSMP=0 ADSTS=00	Tconv		0.7		µs	Fadc=40 MHz
	ADLSMP=0 ADSTS=01			0.75			

Table continues on the next page...

Table 32. 12-bit ADC Characteristics (V_{REFH} = V_{DDAD}, V_{REFL} = V_{SSAD}) (continued)

Characteristic	Conditions[1]	Symb	Min	Typ [2]	Max	Unit	Comment
	ADLSMP=0 ADSTS=10			0.8			
	ADLSMP=0 ADSTS=11			0.85			
	ADLSMP=1 ADSTS=00			0.95			
	ADLSMP=1 ADSTS=01			1.05			
	ADLSMP=1 ADSTS=10			1.15			
	ADLSMP=1, ADSTS=11			1.25			
Total Unadjusted Error	12 bit mode	TUE	-2	-	+5	LSB[3]	With Max Averaging
	10 bit mode		-0.5	-	+2		
	8 bit mode		-0.25	-	+1.5		
Differential Non-Linearity	12 bit mode	DNL	-	±0.6	±1.5	LSB[3]	Waiting for histogram method confirmation
	10bit mode		-	±0.5	±1		
	8 bit mode		-	±0.25	±0.5		
Integral Non-Linearity	12 bit mode	INL	-	±2	±4	LSB[3]	Waiting for histogram method confirmation
	10bit mode		-	±1	±2		
	8 bit mode		-	±0.5	±1		
Zero-Scale Error	12 bit mode	E_{ZS}	-	+1.0	±1.6	LSB[3]	VADIN = V_{REFL} With Max Averaging
	10bit mode		-	±0.4	±0.8		
	8 bit mode		-	±0.1	±0.4		
Full-Scale Error	12 bit mode	E_{FS}	-	±2	±3.5	LSB[3]	VADIN = V_{REFH} With Max Averaging
	10bit mode		-	±0.5	±1		
	8 bit mode		-	±0.25	±0.75		
Quantization Error	12 bit mode	E_Q	-	±1 to 0		LSB[3]	
	10bit mode		-	±0.5			
	8 bit mode		-	±0.5			
Effective Number of Bits	12 bit mode	ENOB	10.1	10.7	-	Bits	Fin = 100Hz
Signal to Noise plus Distortion	See ENOB	SINAD	SINAD = 6.02 x ENOB + 1.76			dB	
Input Leakage Error	all modes	EIL	I_{In} x RAS			mV	I_{In} = 400 nA leakage current
Temperature Sensor Slope	Across the full temperature range of the device	m	--	1.84	--	mV/°C	
Temperature Sensor Voltage	25°C	V_{TEMP25}	-	696	-	mV	

1. All accuracy numbers assume the ADC is calibrated with V_{REFH}=V_{DDAD}
2. Typical values assume V_{DDAD} = 3.3 V, Temp = 25°C, F_{adck}=20 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

3. 1 LSB = (V_{REFH} - V_{REFL})/2N

NOTE

The ADC electrical spec would be met with the calibration enabled configuration.

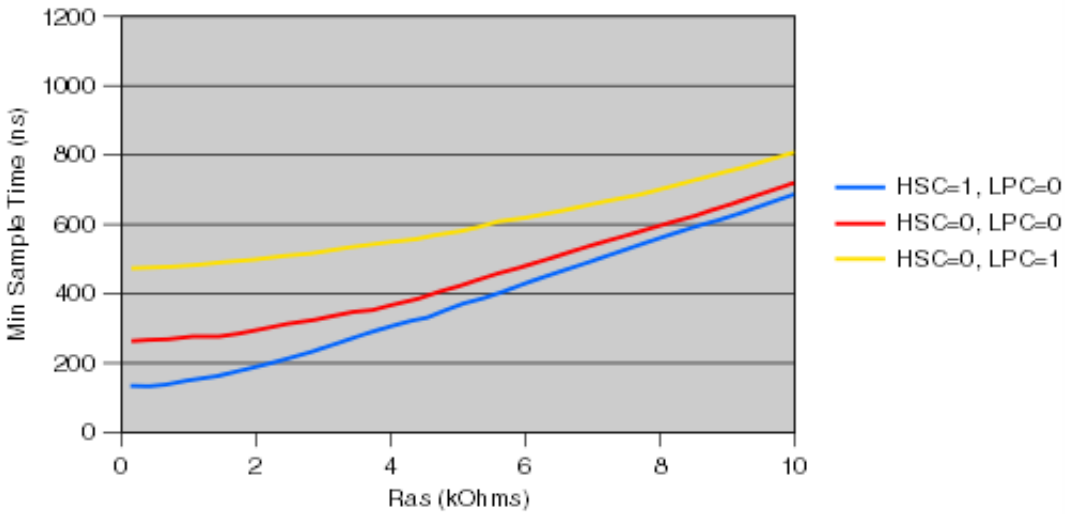


Figure 6. Minimum Sample Time Vs Ras (Cas = 2pF)

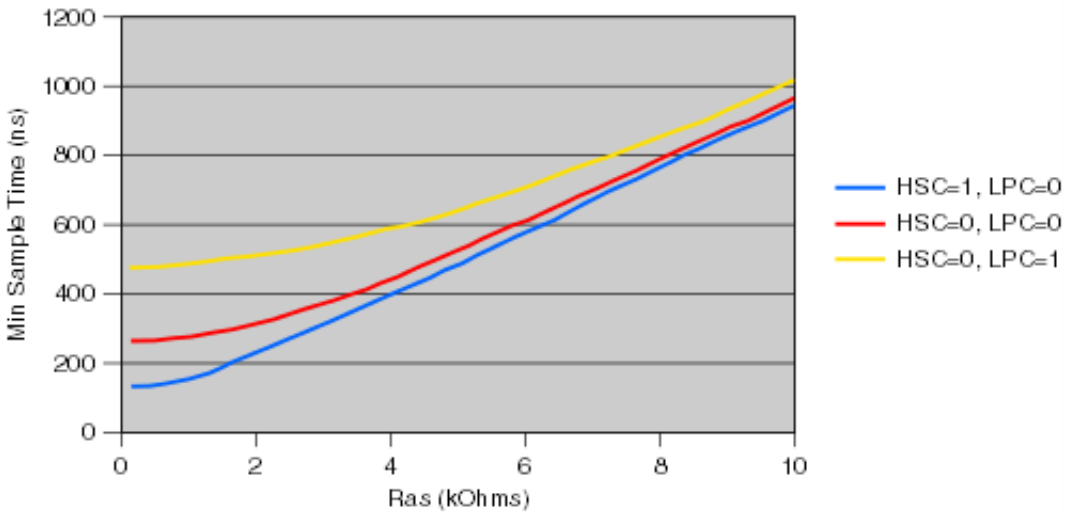


Figure 7. Minimum Sample Time Vs Ras (Cas = 5pF)

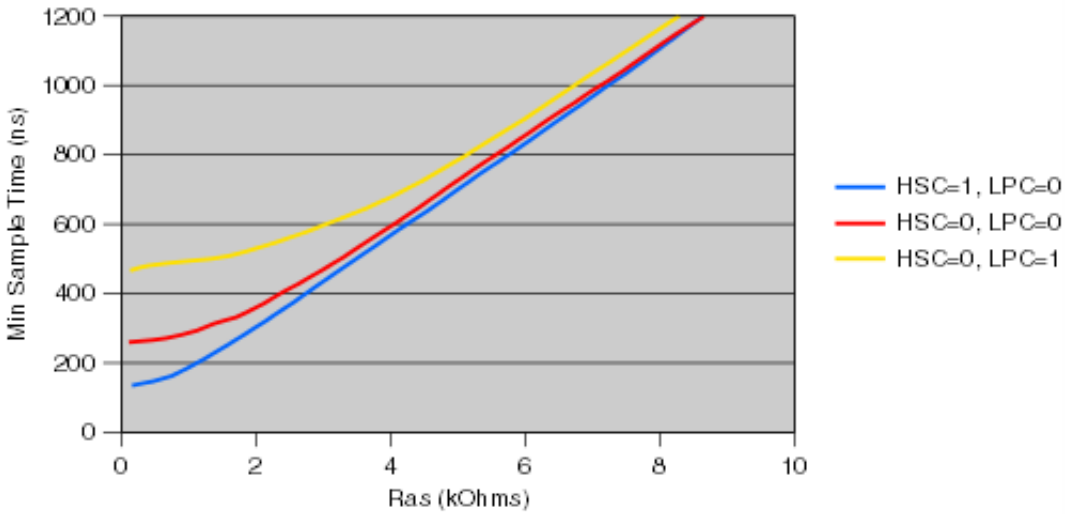


Figure 8. Minimum Sample Time Vs Ras (Cas = 10pF)

9.1.2 12-bit DAC electrical characteristics

9.1.2.1 12-bit DAC operating requirements

Table 33. 12-bit DAC operating requirements

Symbol	Desciption	Min.	Typ	Max.	Unit	Notes
VDDA33_ADC	Supply voltage	3.0	3.3	3.6	V	
VREFH_ADC	Reference voltage	2.5	3.3	VDDA33_ADC	V	1
C_L	Output load capacitance	—		100	pF	2
I_L	Output load current	—		1	mA	

1. User will need to set up DACx_STATCTRL [DACRFS]=1 to select the valid VREFH_ADC reference. When DACx_STATCTRL [DACRFS]=0, the DAC reference is connected to an internal ground node and is not a valid voltage reference. Note that the DAC and ADC share the VREFH_ADC reference simultaneously.)
2. A small load capacitance (47 pF) can improve the bandwidth performance of the DAC

9.1.2.2 12-bit DAC operating behaviors

Table 34. 12-bit DAC operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DDA_DACLP}	Supply current — low-power mode	—	—	100	µA	
I_{DDA_DACHP}	Supply current — high-power mode	—	—	500	µA	
t_{DACLP}	Full-scale settling time (0x080 to 0xF7F) — low-power mode	—	10	15	µs	1

Table continues on the next page...

Table 34. 12-bit DAC operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{DACHP}	Full-scale settling time (0x080 to 0xF7F) — high-power mode	—	3	5	µs	1
$t_{CCDACLP}$	Code-to-code settling time (0xBF8 to 0xC08)				µs	1
	low-power mode	—	5	—		
	high-power mode	—	1	—		
$V_{dacoutl}$	DAC output voltage range low — high-speed mode, no load, DAC set to 0x000	—	—	100	mV	
$V_{dacouth}$	DAC output voltage range high — high-speed mode, no load, DAC set to 0xFFF	V_{DACR} −100	—	V_{DACR}	mV	
INL	Integral non-linearity error — high speed mode	—	—	±8	LSB	2
DNL	Differential non-linearity error — V_{DACR} = VREF_OUT	—	—	±1	LSB	3
V_{OFFSET}	Offset error	—	±0.4	±0.8	%FSR	4
E_G	Gain error	—	±0.1	±0.6	%FSR	4
PSRR	Power supply rejection ratio, V_{DDA} =3 V, T = 25 C		70		dB	
T_{CO}	Temperature coefficient offset voltage	—	3.7	—	µV/C	5
T_{GE}	Temperature coefficient gain error	—	0.000421	—	%FSR/C	
A_C	Offset aging coefficient	—	—	100	µV/yr	
Rop	Output resistance load = 3 kΩ	—	—	250	Ω	
SR	Slew rate -80h→ F7Fh→ 80h				V/µs	
	High power (SP_{HP})		1.7	3		
	Low power (SP_{LP})		0.3	0.6		
CT	Channel to channel cross talk	—	70		dB	

1. Settling within ±1 LSB
2. The INL is measured for 0+100mV to V_{DACR}−100 mV
3. The DNL is measured for 0+100mV to V_{DACR}−100 mV
4. Calculated by a best fit curve from V_{SS}+100 mV to V_{DACR}−100 mV
5. VDDA = 3.3 V, reference select set for VDDA (DACx_CO:DACRFS = 1), high power mode (DACx_C0:LPEN = 0), DAC set to 0x800, Temp range from -40 °C to 85 °C

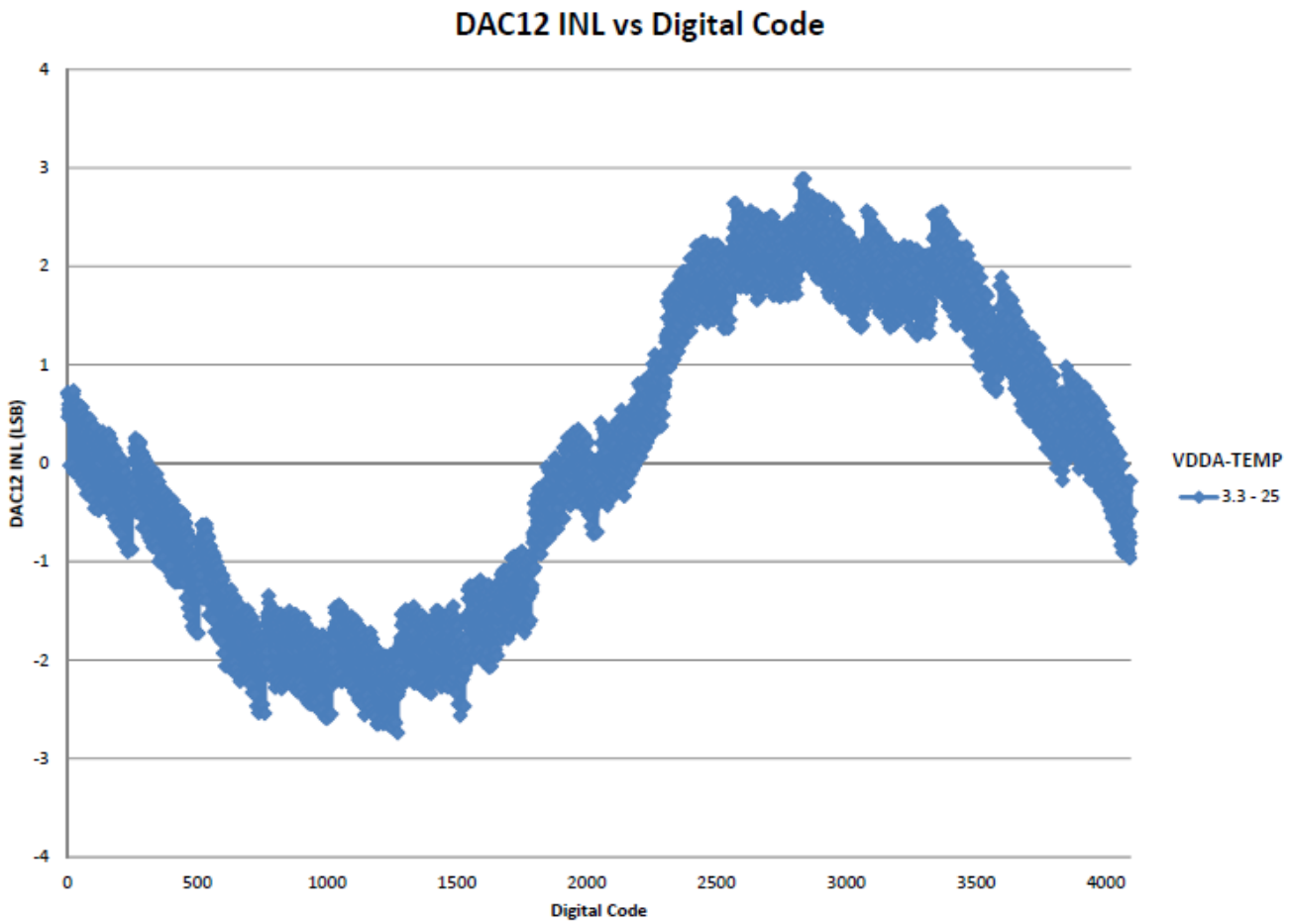


Figure 9. INL error vs. digital code

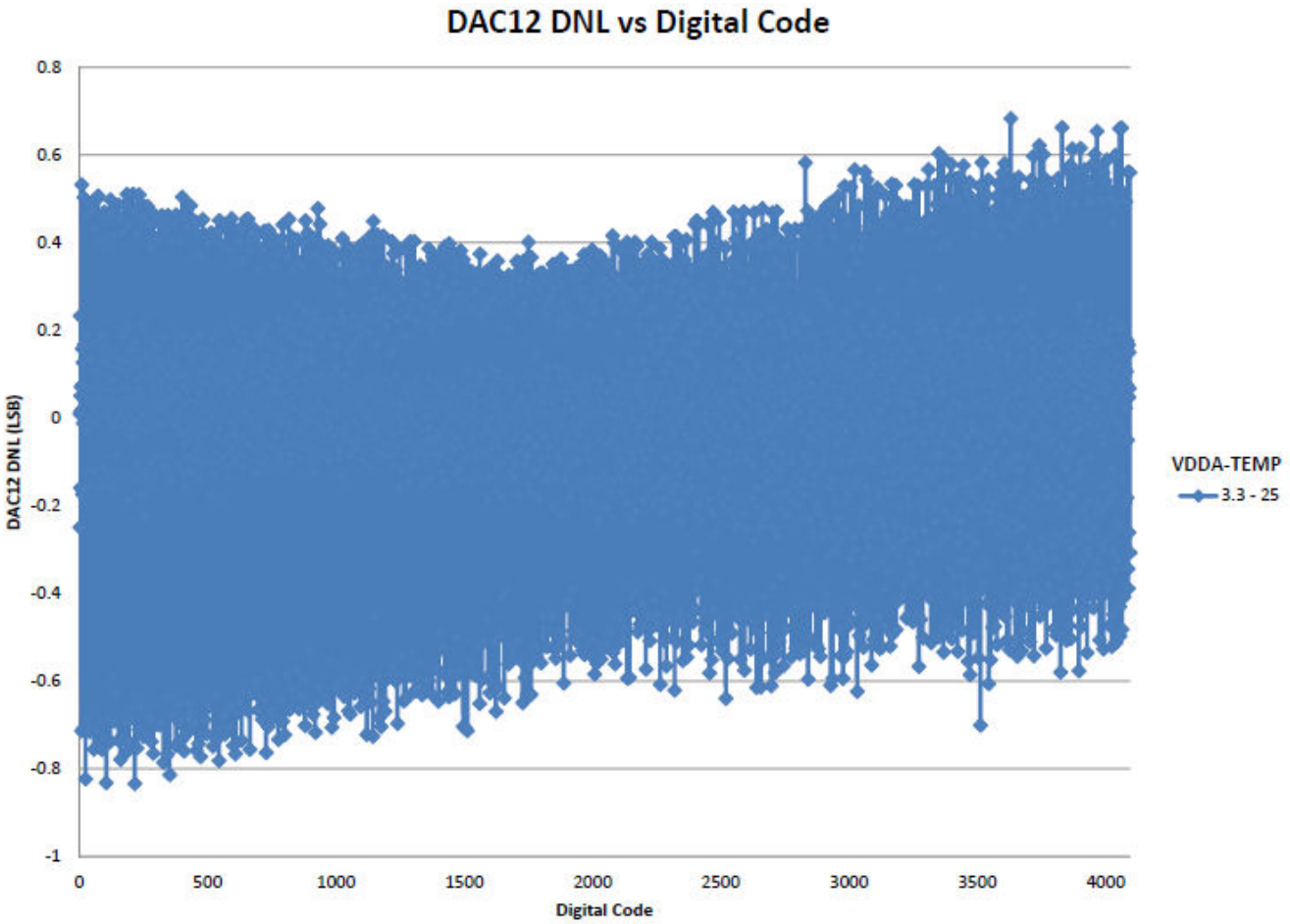


Figure 10. DNL error vs. digital code

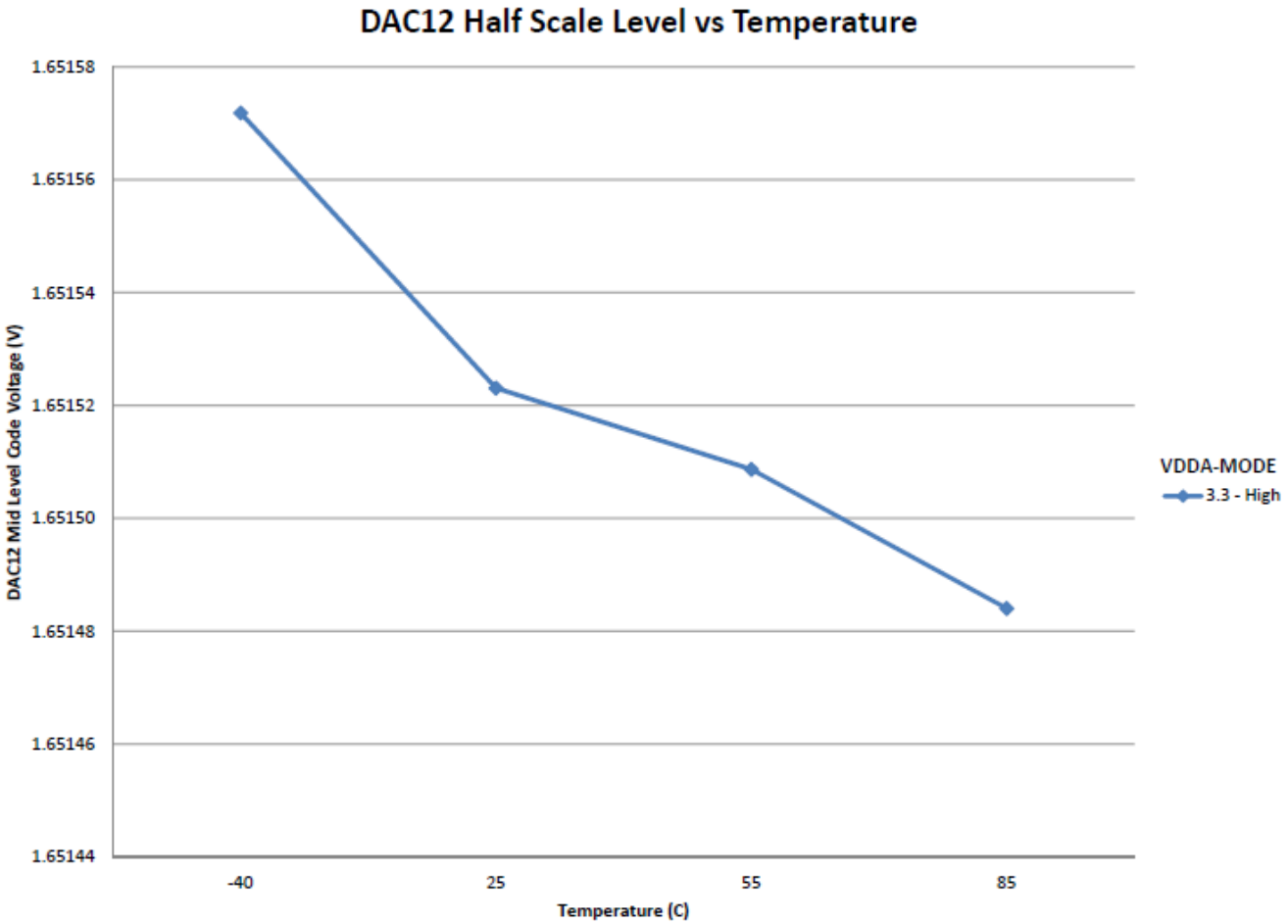


Figure 11. Offset at half scale vs. temperature

9.1.3 VideoADC Specifications

This section describes the electrical specification and characteristics of the VideoADC Analog Front End.

Table 35. VideoADC Specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
VDDA33_AFE	Supply voltage	3.0	3.3	3.6	V	—
	Supply current	—	—	41	mA	—
VDDA12_AFE	Supply voltage	1.1	1.2	1.26	V	—
	Supply current	—	—	14	mA	—
V_{in}	Input signal voltage range	0	0.5	1.4	V	—
	External AC coupling	10	47		nF	The external AC coupling capacitance cannot be too large.

Table continues on the next page...

Table 35. VideoADC Specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{BG}	Bandgap voltage	—	0.6	—	V	Bandgap voltage on VADC_AFE_BANDGAP pin. Pin should be decoupled with a 100nF capacitor

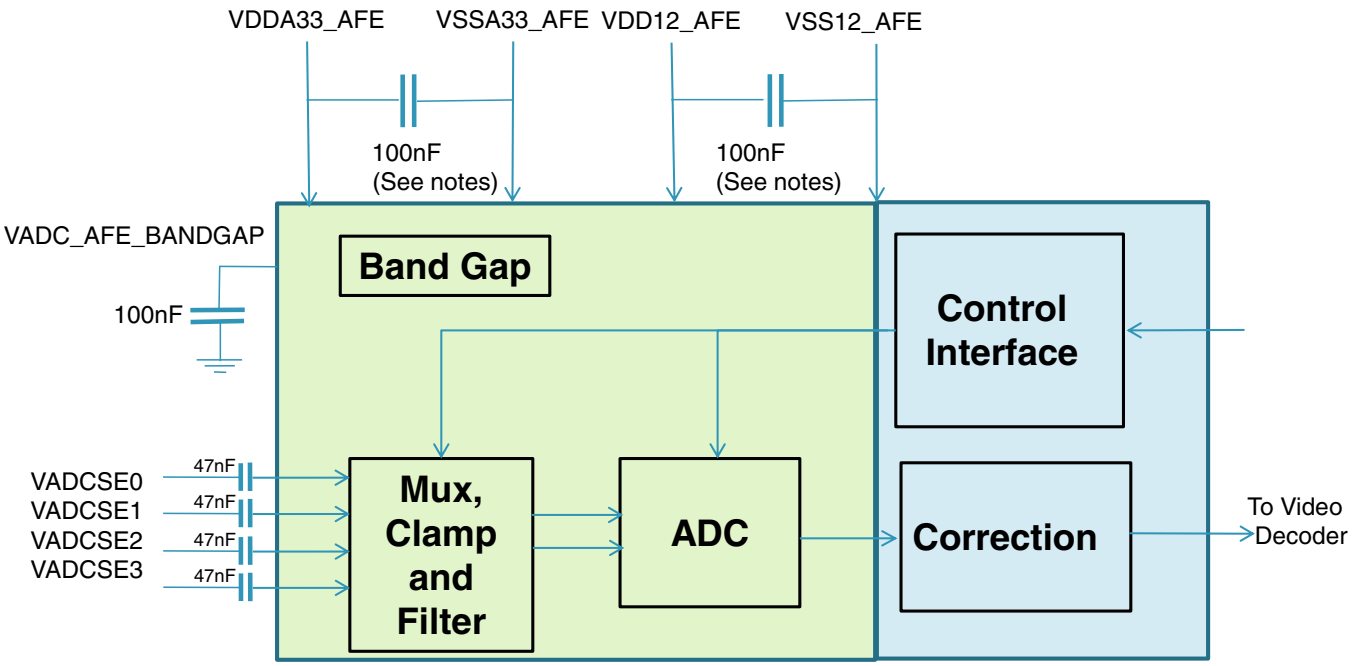


Figure 12. VideoADC supply scheme

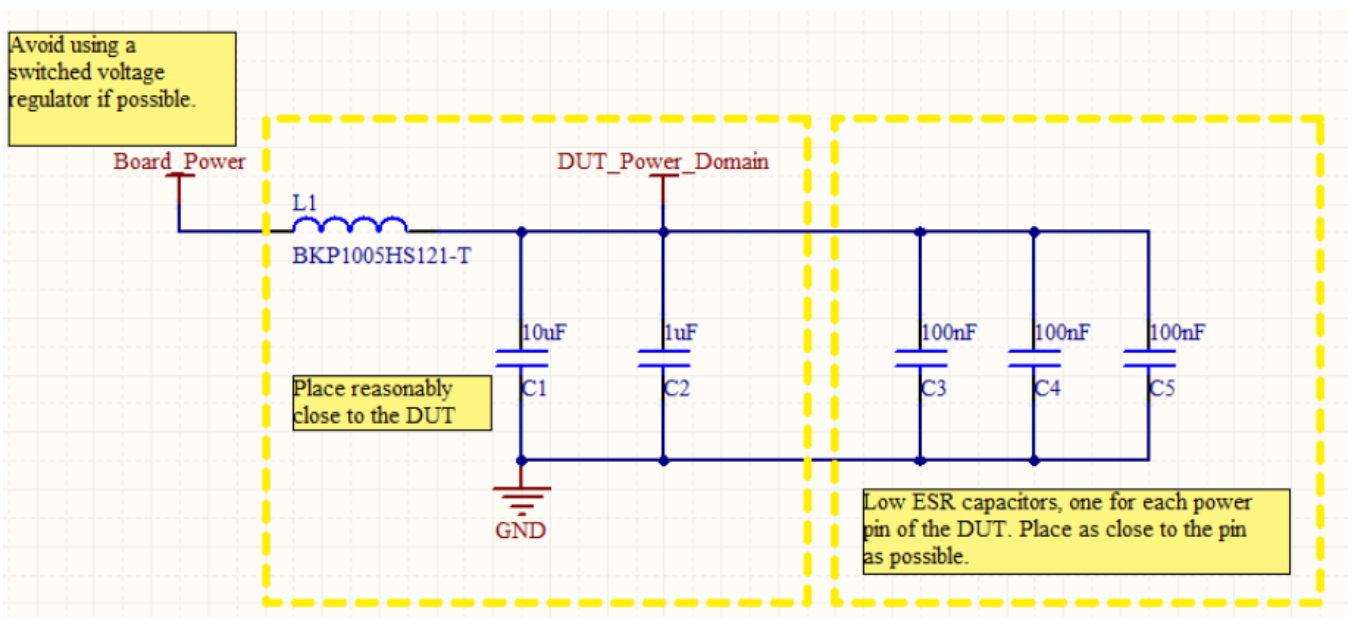


Figure 13. VideoADC supply decoupling

NOTE

VideoADC 3.3V and 1.2V power supply pins should be decoupled to their respective grounds using low-ESR 100nF capacitors

NOTE

If possible, avoid using switched voltage regulators for the AFE power domains. Use linear voltage regulators instead.

NOTE

The 3.3V and 1.2V power domains should be separated from other circuitry on the board by inductors/beads to filter out high frequency noise.

9.2 Display and Video interfaces

9.2.1 DCU Switching Specifications

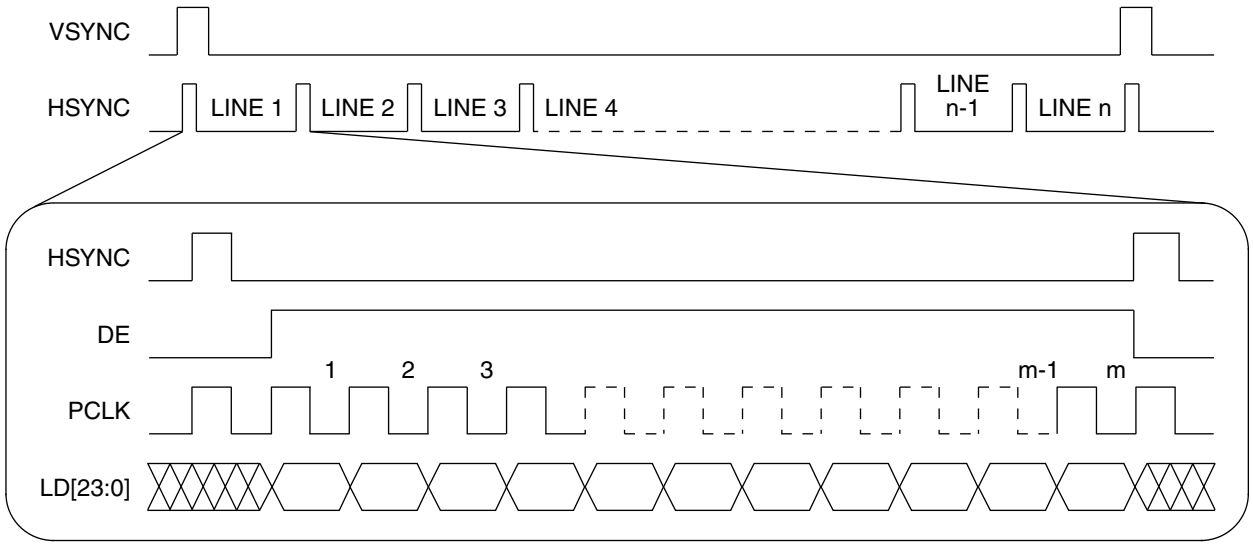
9.2.1.1 Interface to TFT panels (DCU0/1)

This section provides the LCD interface timing for a generic active matrix color TFT panel. In the figure below, signals are shown with positive polarity. The sequence of events for active matrix interface timing:

- PCLK latches data into the panel on its positive edge (when positive polarity is selected). In active mode, PCLK runs continuously. This signal frequency could be from 5 to 66 MHz depending on the panel type.
- HSYNC causes the panel to start a new line. It always encompasses at least one PCLK pulse.
- VSYNC causes the panel to start a new frame. It always encompasses at least one HSYNC pulse.
- DE acts like an output enable signal to the LCD panel. This output enables the data to be shifted onto the display. When disabled, the data is invalid and the trace is off.

Figure 14. TFT LCD interface timing overview[1]

1. In the figure, LD[23:0]" signal is "line data," an aggregation of the DCU's RGB signals—R[0:7], G[0:7] and B[0:7].



9.2.1.2 Interface to TFT LCD Panels—Pixel Level Timings

This section provides the horizontal timing (timing of one line), including both the horizontal sync pulse and data. All parameters shown in the figure below are programmable. This timing diagram corresponds to positive polarity of the PCLK signal (meaning the data and sync signals change on the rising edge) and active-high polarity of the HSYNC, VSYNC and DE signals. The user can select the polarity of the HSYNC and VSYNC signals via the SYN_POL register, whether active-high or active-low. The default is active-high. The DE signal is always active-high. Pixel clock inversion and a flexible programmable pixel clock delay are also supported. They are programmed via the clock divide . The DELTA_X and DELTA_Y parameters are programmed via the DISP_SIZE register. The PW_H, BP_H and FP_H parameters are programmed via the HSYN PARA register. The PW_V, BP_V and FP_V parameters are programmed via the VSYN_PARA register.

Table 36. LCD interface timing parameters—horizontal and vertical

Symbol	Characteristic		Unit
t_{PCP}	Display pixel clock period	11.2	ns
t_{PWH}	HSYNC pulse width	PW_H * t_{PCP}	ns
t_{BPH}	HSYNC back porch width	BP_H * t_{PCP}	ns
t_{FPH}	HSYNC front porch width	FP_H * t_{PCP}	ns
t_{SW}	Screen width	DELTA_X * t_{PCP}	ns
t_{HSP}	HSYNC (line) period	(PW_H + BP_H + FP_H + DELTA_X) * t_{PCP}	ns
t_{PWV}	VSYNC pulse width	PWV * t_{HSP}	ns
t_{BPV}	VSYNC back porch width	BP_V * t_{HSP}	ns
t_{FPV}	VSYNC front porch width	FP_V * t_{HSP}	ns
t_{SH}	Screen height	DELTA_Y * t_{HSP}	ns
t_{VSP}	VSYNC (frame) period	(PW_V + BP_V + FP_V + DELTA_Y) * t_{HSP}	ns

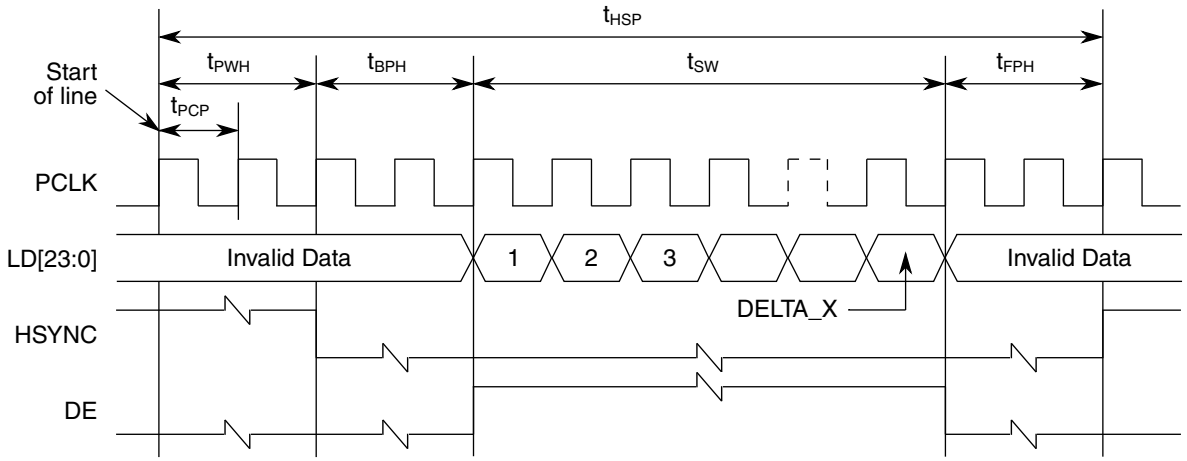


Figure 15. Horizontal sync timing

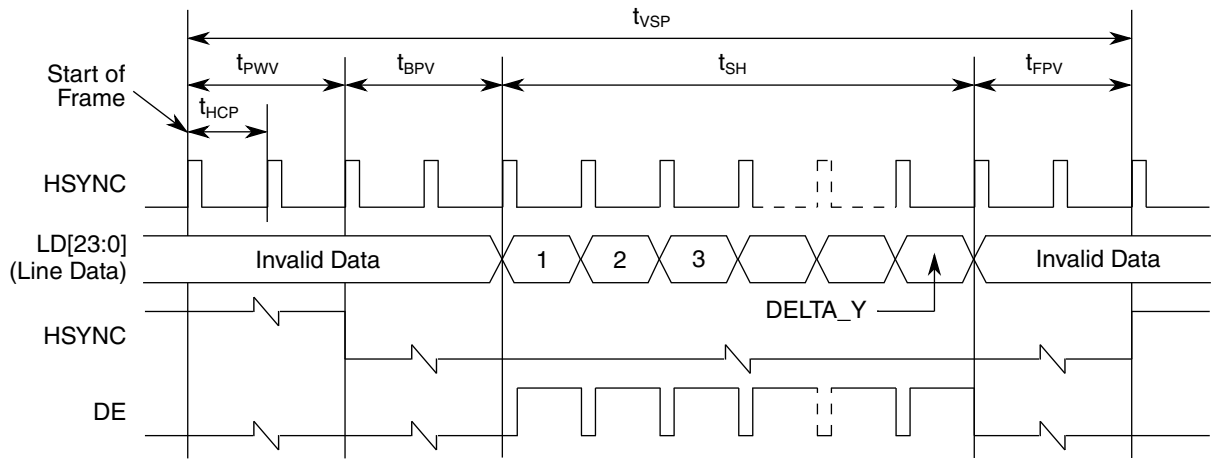


Figure 16. Vertical sync pulse

9.2.1.3 Interface to TFT LCD panels—access level

This section provides the access level timing parameters of the LCD interface.

Table 37. LCD Interface Timing Parameters[1], [2], [3]—Access Level

Symbol	Description	Min	Max	Unit
t_{CKP}	Pixel Clock Period	11.2	_	ns
t^{DV}	TFT interface data valid after pixel clock	_	4.4	ns
t^{DV}	TFT interface HSYNC valid after pixel clock	_	4.4	ns
t^{DV}	TFT interface VSYNC valid after pixel clock	_	4.4	ns
t^{DV}	TFT interface DE valid after pixel clock	_	4.4	ns
t^{HO}	TFT interface output hold time for data and control bits	0	_	ns
	Relative skew between the data bits	_	4.4	ns

1. The characteristics in this table are based on the assumption that data is output at +ve edge and displays latch data on -ve edg6

2. Intra bit skew is less than 2 ns
3. Load CL = 50 pf

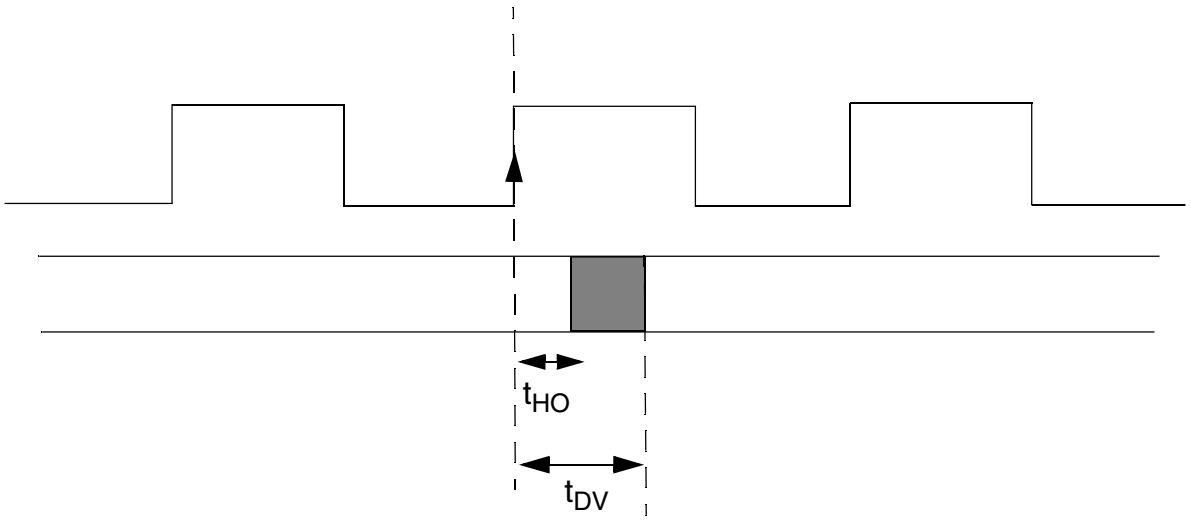


Figure 17. LCD Interface Timing Parameters—Access Level

9.2.2 Video Input Unit timing

This section provides the timing parameters of the Video Input Unit (VIU) interface.

These are the clocking requirements of the VIU interface:

- The platform bus clock must be 2.5x pixel clock
- If the VIU3 does 2x horizontal upscaling, the ratio must be 3x

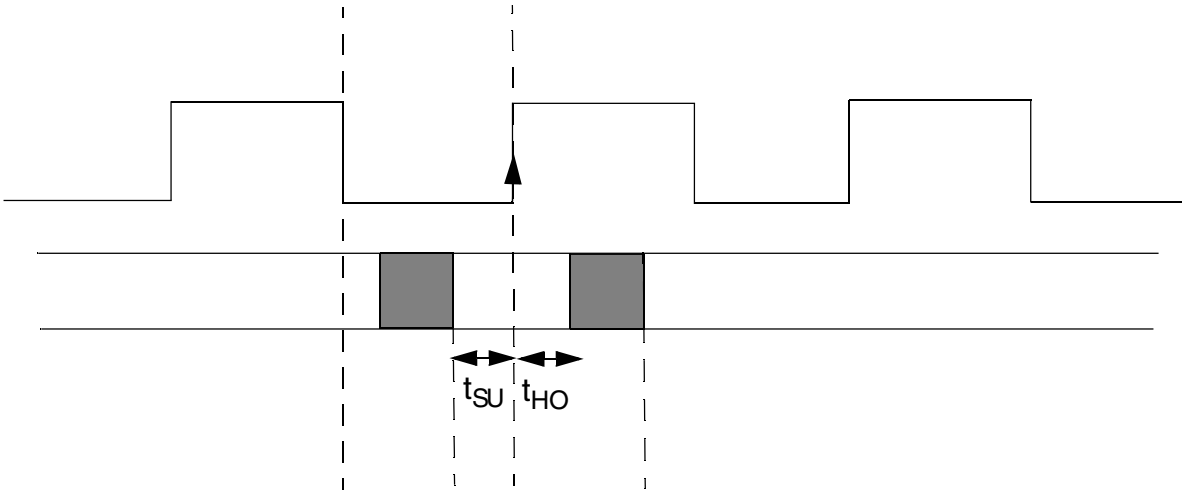


Figure 18. VIU Timing Parameters

Table 38. VIU Timing Parameters

Symbol	Characteristic	Min Value	Max Value	Unit
f_{PIX_CK}	VIU pixel clock frequency	_	64	MHz
t_{DSU}	VIU data setup time	4	_	ns
t_{DHD}	VIU data hold time	1	_	ns

9.2.3 LCD driver electrical characteristics

This section provides LCD driver electrical specification at V_{DD33} = 3.3 V ± 10%.

Table 39. LCD driver specifications

Symbol	Parameter	Min	Typical	Max	Unit
VLCD	Voltage on VLCD (LCD supply) pin with respect to VSS	0		VDD33 + 0.3	V
$Z_{BP/FP}$	LCD output impedance (BP[n-1:0],FP[m-1:0]) for output levels VDDE, VSS	_	_	5.0	KΩ
$I_{BP/FP}$	LCD output current (BP[n-1:0],FP[m-1:0]) for outputs charge/discharge voltage levels VDDE2/3, VDDE1/2, VDDE/3)[1]	_	25	_	µA

1. With PWR=10, BSTEN=0, and BSTAO=0

9.3 Ethernet specifications

9.3.1 Ethernet Switching Specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface. All Ethernet signals use pad type pad_fsr. The timing specifications described i the section assume a pad slew rate setting of 11 and a load of 50 pF[2].

9.3.2 Receive and Transmit signal timing specifications

This section provides timing specs that meet the requirements for RMII interfaces for a range of transceiver devices.

Table 40. Receive signal timing for RMII interfaces

	Characteristic	RMII Mode		Unit
		Min	Max	
—	EXTAL frequency (RMII input clock RMII_CLK)	—	50	MHz
E3, E7	RMII_CLK pulse width high	35%	65%	RMII_CLK period
E4, E8	RMII_CLK pulse width low	35%	65%	RMII_CLK period
E1	RXD[1:0], CVS_DV, RXER to RMII_CLK setup	4	—	ns
E2	RMII_CLK to RXD[1:0], CRS_DV, RXER hold	2	—	ns
E6	RMII_CLK to TXD[1:0], TXEN valid	—	14	ns
E5	RMII_CLK to TXD[1:0], TXEN invalid	4	—	ns

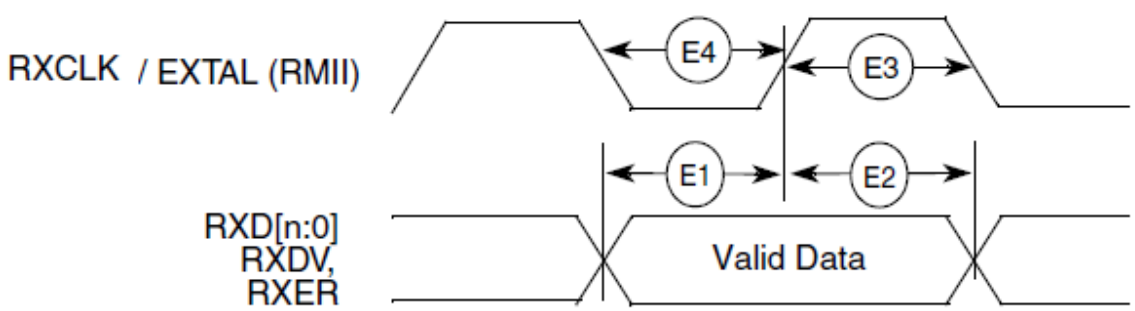


Figure 19. RMII receive signal timing diagram

2. These timing parameters are specified assuming maximum operating frequency and the fastest pad slew rate setting (11). When operating this interface at lower frequencies, increase the slew rate by using the 10, 01, or 00 setting to increase edge rise and fall times, thus reducing EMI.

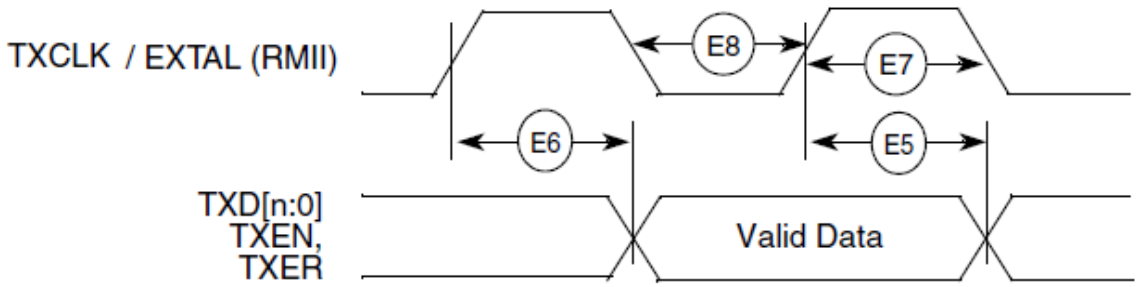


Figure 20. RMII transmit signal timing diagram

NOTE

See the most current device errata document when using the internally generated RXCLK and TXCLK clocks.

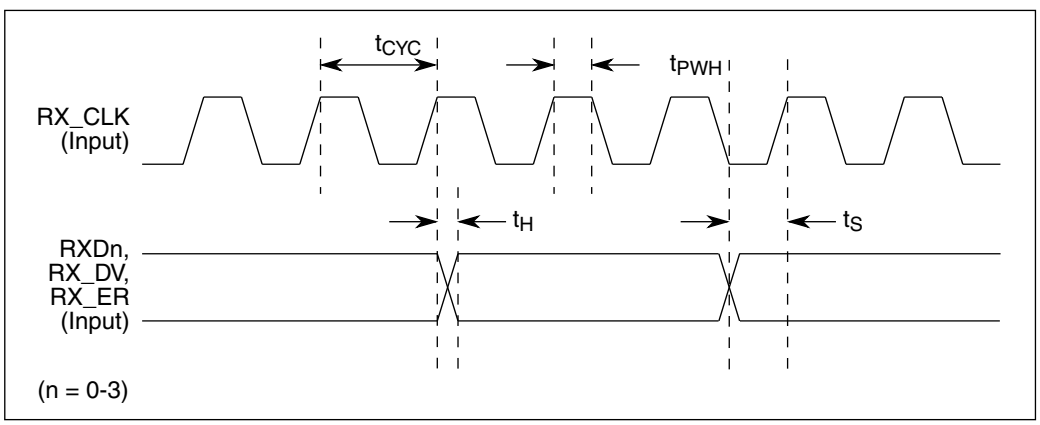


Figure 21. MII receive signal timing diagram

Table 41. Receive signal timing for MII interfaces

Characteristic		MII Mode			Unit
		Min	Typ	Max	
RX_CLK clock period (100/10 MBPS)	t_{CYC}		40/400		ns
RX_CLK duty cycle, t_{PWH}/t_{CYC}		45	50	55	%
Input setup time before RX_CLK	t_S	5			ns
Input setup time after RX_CLK	t_H	5			ns

9.3.3 Receive and Transmit signal timing specifications for MII interfaces

This section provides timing specs that meet the requirements for MII interfaces for a range of transceiver devices.

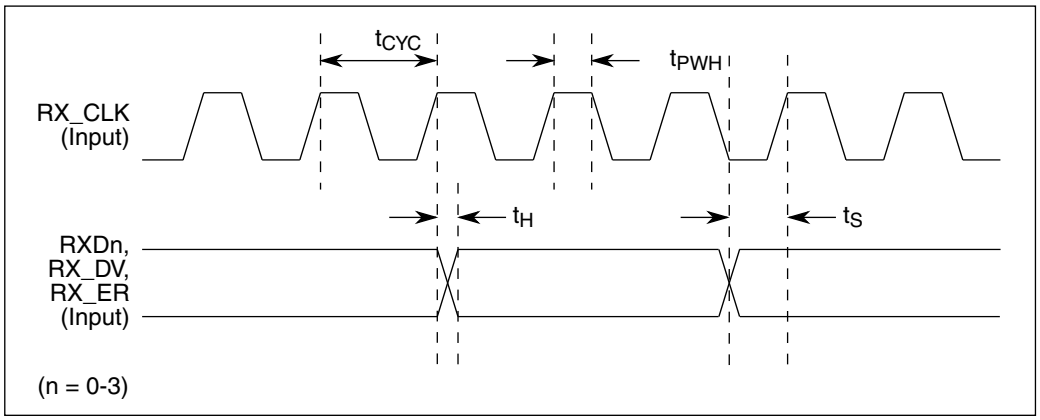
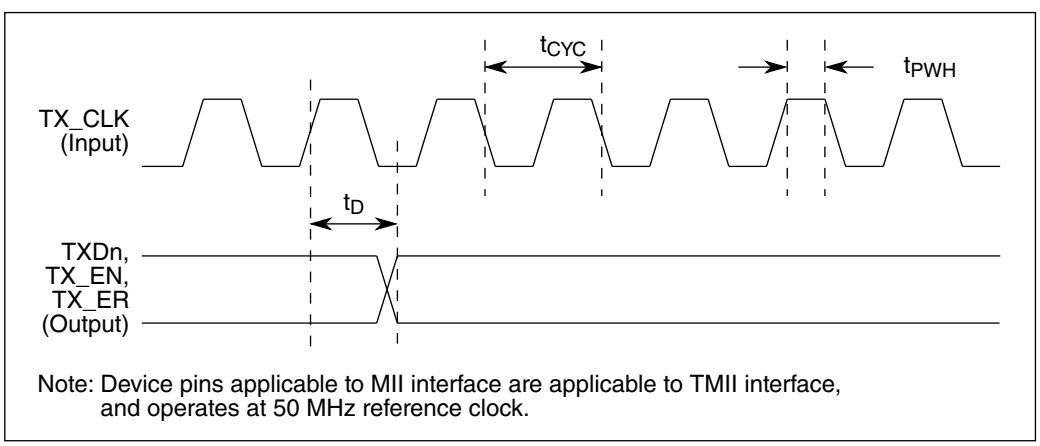


Figure 22. MII receive signal timing diagram

Table 42. Receive signal timing for MII interfaces

Characteristic		MII Mode			Unit
		Min	Typ	Max	
RX_CLK clock period (100/10 MBPS)	t_{CYC}		40/400		ns
RX_CLK duty cycle, t_{PWH}/t_{CYC}		45	50	55	%
Input setup time before RX_CLK	t_s	5			ns
Input hold time after RX_CLK	t_h	5			ns



Note: Device pins applicable to MII interface are applicable to TMII interface, and operates at 50 MHz reference clock.

Figure 23. MII transmit signal timing diagram

Table 43. Transmit signal timing for MII interfaces

Characteristic		MII Mode			Unit
		Min	Typ	Max	
TX_CLK clock period (100/10 MBPS)	t_{CYC}		40/400		ns
TX_CLK duty cycle, t_{PWH}/t_{CYC}		45	50	55	%
Out delay from TX_CLK	t_D	2		25	ns

9.4 Audio interfaces

9.4.1 Enhanced Serial Audio Interface (ESAI) Timing Parameters

The ESAI consists of independent transmitter and receiver sections, each section with its own clock generator. The following table shows the interface timing values.

Table 44. Enhanced Serial Audio Interface (ESAI) Timing

No	Characteristics	Symbol	Min	Max	Condition[1]	Unit
1	Clock cycle[2]	t_{SSICC}	30.0 $(4 \times T_c)$	— —	master	ns
2	Clock high period: • master • slave	— —	6 $(2 \times T_c - 9.0)$ 15 $(2 \times T_c)$	— —	— —	ns
3	Clock low period: • master • slave	— —	6 $(2 \times T_c - 9.0)$ 15 $(2 \times T_c)$	— —	— —	ns
4	FSR Input and Data Input setup time before SCKR (SCK in synchronous mode) falling edge	— —	6 15	— —	Slave Master	ns
5	FSR Input and Data Input hold time after SCKR falling edge	— —	2 0	— —	Slave Master	ns
6	SCKT rising edge to FST out and Data out valid	— —	— —	15 6	Slave Master	ns
7	SCKT rising edge to FST out and Data out hold	— —	— —	0 0	Slave Master	ns
8	FST input setup time before SCKT falling edge	— —	6 15	— —	Slave Master	ns
9	FST input hold time after SCKT falling edge	— —	2 0	— —	Slave Master	ns
10	HCKR/HCKT clock cycle	—	15 $(2 \times T_C)$	—	—	ns
11	HCKT input rising edge to SCKT output	—	—	18.0	—	ns
12	HCKR input rising edge to SCKR output	—	—	18.0	—	ns

1. SCKT(SCKT pin) = transmit clock SCKR(SCKR pin) = receive clock FST(FST pin) = transmit frame sync FSR(FSR pin) = receive frame sync HCKT(HCKT pin) = transmit high frequency clock HCKR(HCKR pin) = receive high frequency clock
2. For the internal clock, the external clock cycle is defined by Icyc and the ESAI control register.

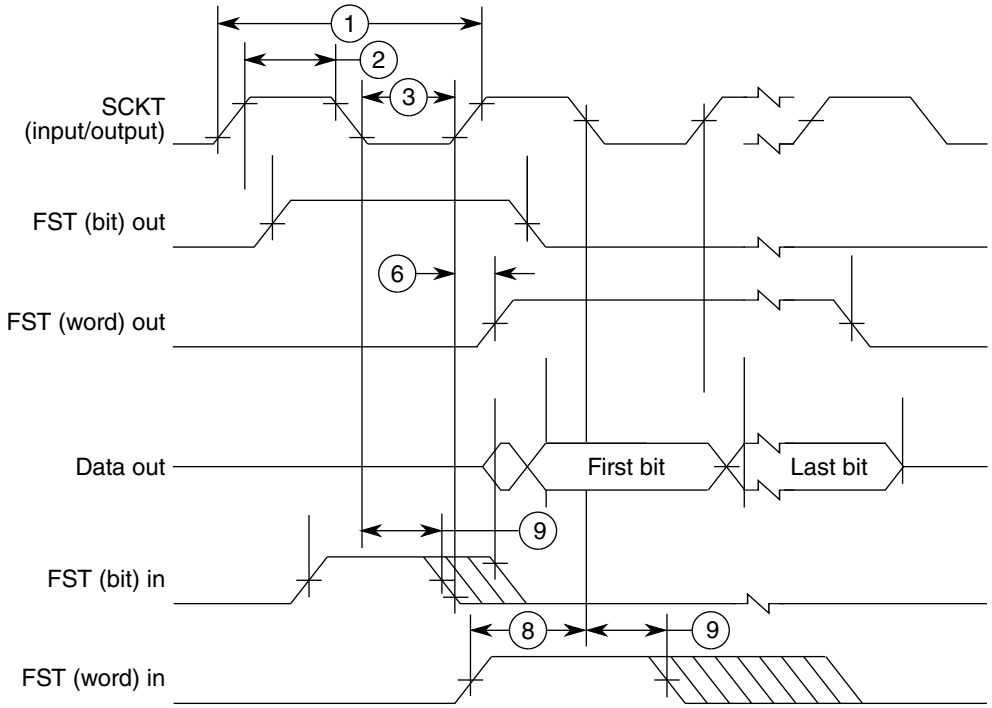


Figure 24. ESAI Transmitter Timing

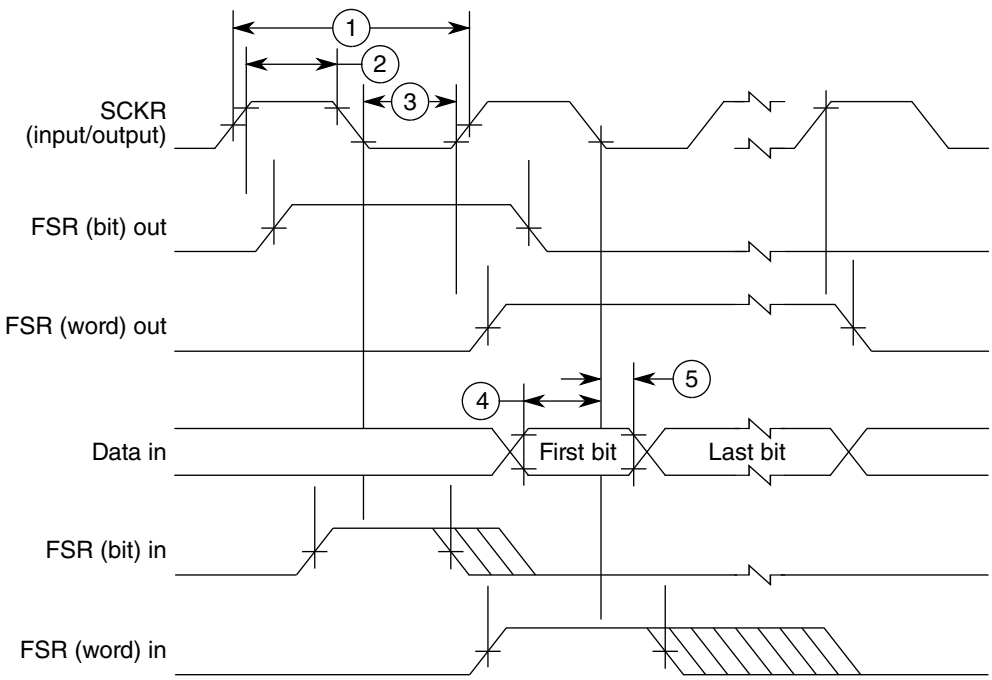


Figure 25. ESAI Receiver Timing

9.4.2 SPDIF Timing Parameters

The Sony/Philips Digital Interconnect Format (SPDIF) data is sent using the bi-phase marking code. When encoding, the SPDIF data signal is modulated by a clock that is twice the bit rate of the data signal. Table and Figure below show SPDIF timing parameters for the Sony/Philips Digital Interconnect Format (SPDIF), including the timing of the modulating Rx clock (SRCK) for SPDIF in Rx mode and the timing of the modulating Tx clock (STCLK) for SPDIF in Tx mode.

Table 45. SPDIF Timing Parameters

Characteristic	Symbol	Timing Parameter Range		Unit
		Min	Max	
SPDIFIN Skew: asynchronous inputs, no specs apply			0.7	ns
SPDIFOUT output (Load = 50pf) • Skew • Transition rising • Transition falling			• 1.5 • 24.2 • 31.3	ns
SPDIFOUT1 output (Load = 30pf) - Skew			1.5	ns
• Transition rising • Transition falling		Refer Table 21		
Modulating Rx clock (SRCK) period	srckp	40		ns
SRCK high period	srckph	16		ns
SRCK low period	srckpl	16		ns
Modulating Tx clock (STCLK) period	stclkp	40		ns
STCLK high period	stclkph	16		ns
STCLK low period	stclkpl	16		ns

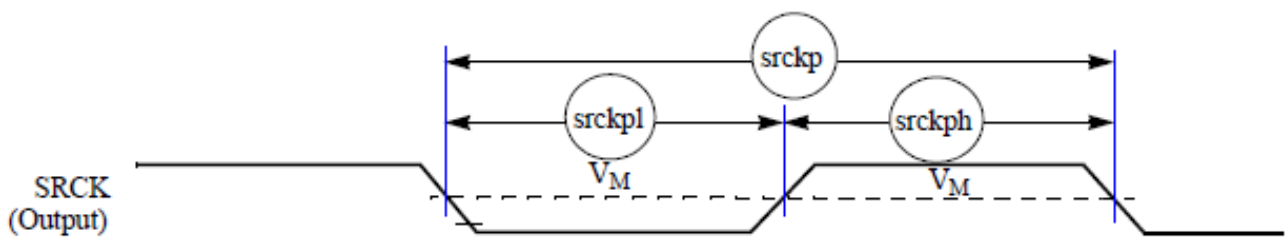


Figure 26. SRCK Timing Diagram

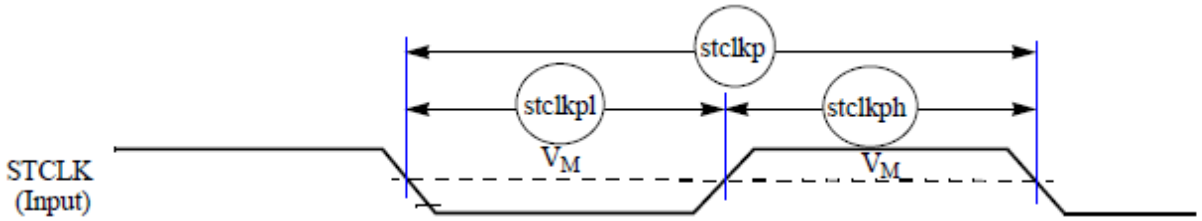


Figure 27. STCLK Timing Diagram

9.4.3 SAI/I²S Switching Specifications

This section provides the AC timings for the SAI in master (clocks driven) and slave modes (clocks input). All timings are given for non-inverted serial clock polarity (SAI_TCR[TSCKP] = 0, SAI_RCR[RSCKP] = 0) and a non-inverted frame sync (SAI_TCR[TFSI] = 0, SAI_RCR[RFSI] = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timings remain valid by inverting the clock signal (SAI_BCLK) and/or the frame sync (SAI_FS) shown in the figures below.

Table 46. Master Mode SAI Timing

Num	Characteristic	Min	Max	Unit
S1	SAI_MCLK cycle time	2 x t_{SYS}	—	ns
S2	SAI_MCLK pulse width high/low	40%	60%	MCLK period
S3	SAI_BCLK cycle time	4 x t_{SYS}	—	ns
S4	SAI_BCLK pulse width high/low	40%	60%	BCLK period
S5	SAI_BCLK to SAI_FS output valid	—	15	ns
S6	SAI_BCLK to SAI_FS output invalid	0	—	ns
S7	SAI_BCLK to SAI_TXD valid	—	15	ns
S8	SAI_BCLK to SAI_TXD invalid	0	—	ns
S9	SAI_RXD/SAI_FS input setup before SAI_BCLK	15	—	ns
S10	SAI_RXD/SAI_FS input hold after SAI_BCLK	0	—	ns

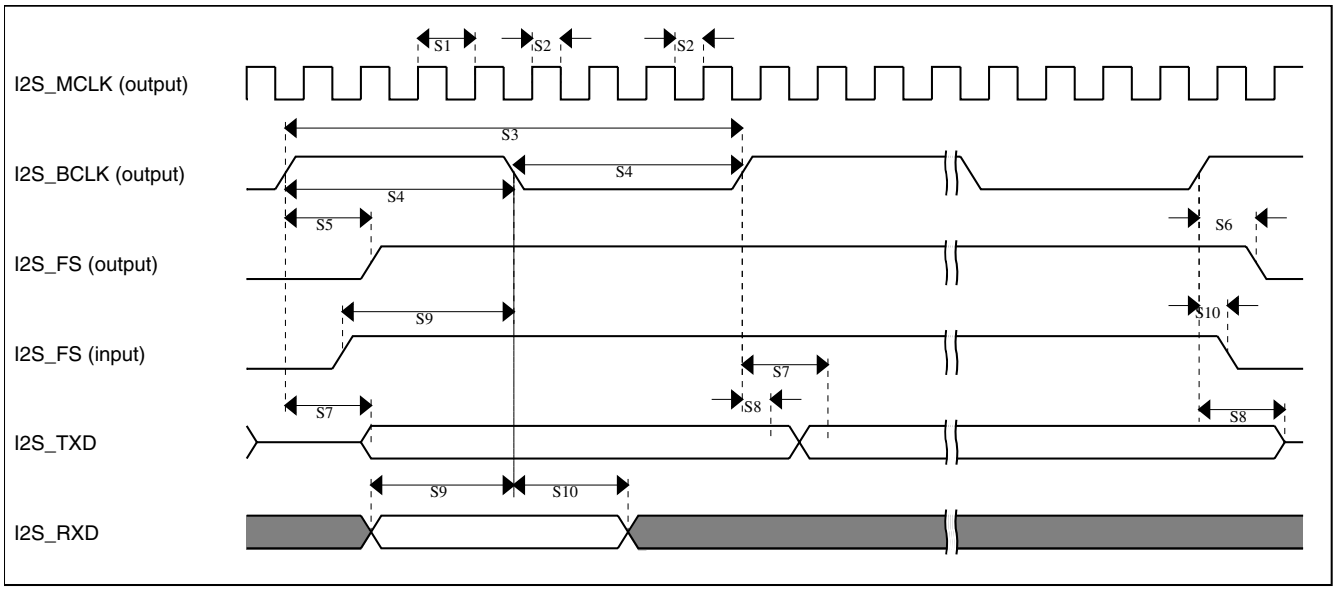


Figure 28. SAI Timing — Master Modes

Table 47. Slave Mode SAI Timing

Num	Characteristic	Min	Max	Unit
S11	SAI_BCLK cycle time (input)	4 x t_{SYS}	—	ns
S12	SAI_BCLK pulse width high/low (input)	40%	60%	BCLK period
S13	SAI_FS input setup before SAI_BCLK	10	—	ns
S14	SAI_FS input hold after SAI_BCLK	2	—	ns
S15	SAI_BCLK to SAI_TXD/SAI_FS output valid	—	20	ns
S16	SAI_BCLK to SAI_TXD/SAI_FS output invalid	0	—	ns
S17	SAI_RXD setup before SAI_BCLK	10	—	ns
S18	SAI_RXD hold after SAI_BCLK	2	—	ns

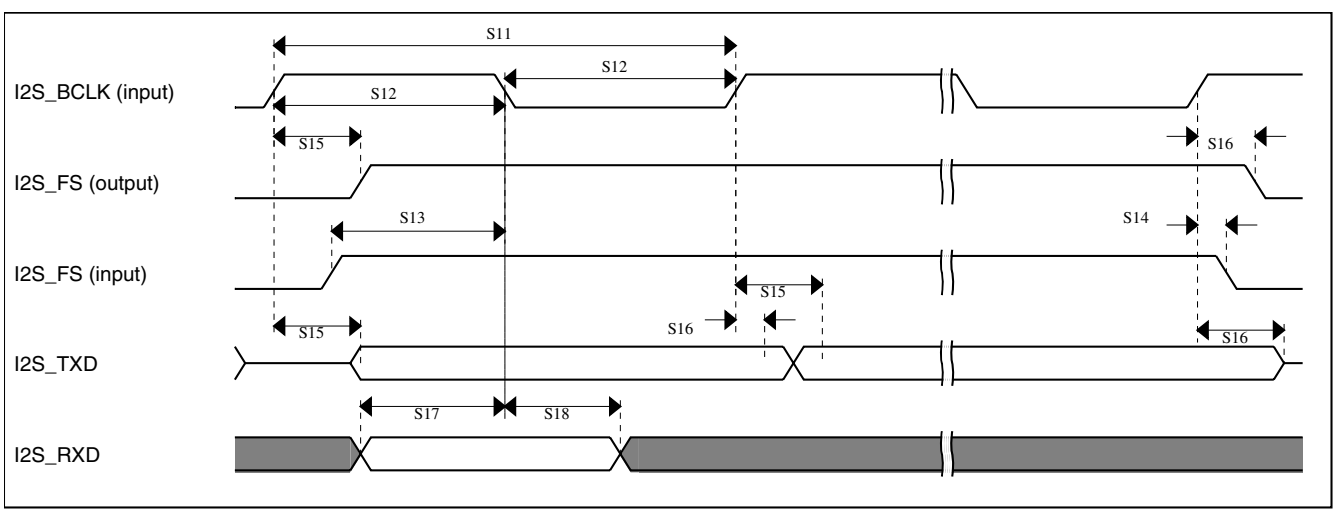


Figure 29. SAI Timing — Slave Modes

9.5 Memory interfaces

9.5.1 QuadSPI timing

- All data is based on a negative edge data launch from the device and a negative edge data capture, as shown in the timing diagrams in this section. This corresponds to the N/1 sample point as shown in the reference manual QSPI section "Internal Sampling of Serial Flash Input Data."
- Measurements are with a load of 35 pF on output pins. I/P Slew : 1ns
- Timings assume a setting of 0x0000_000x for QSPI_SMPR register (see the reference manual for details).

SDR mode

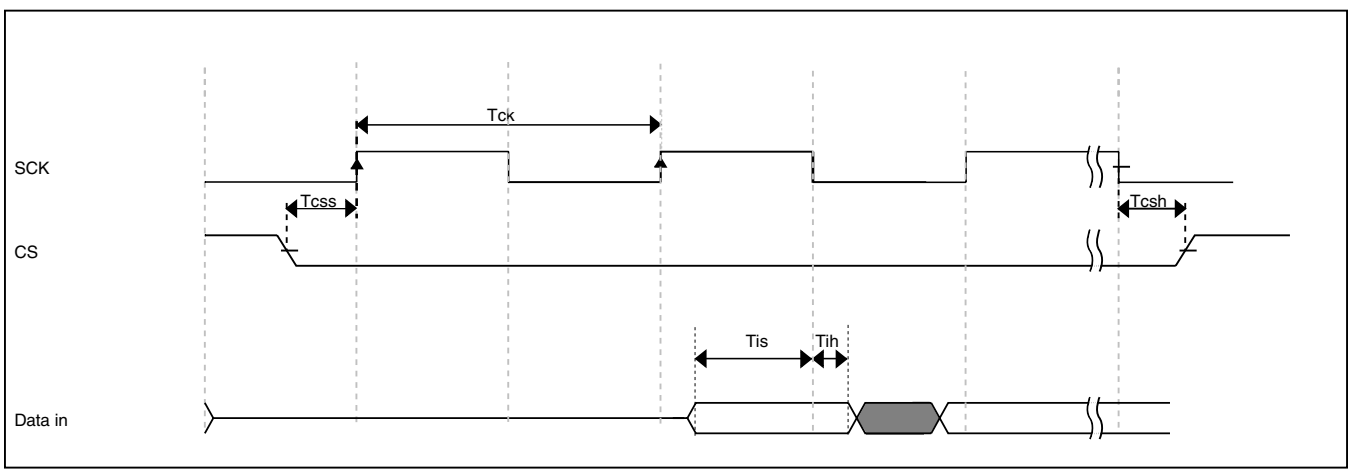


Figure 30. QuadSPI Input/Read timing (SDR mode)

Table 48. QuadSPI Input/Read timing (SDR mode)

Symbol	Parameter	Value		Unit
		Min	Max	
T_{is}	Setup time for incoming data	5.4	—	ns
T_{ih}	Hold time requirement for incoming data	0	—	ns

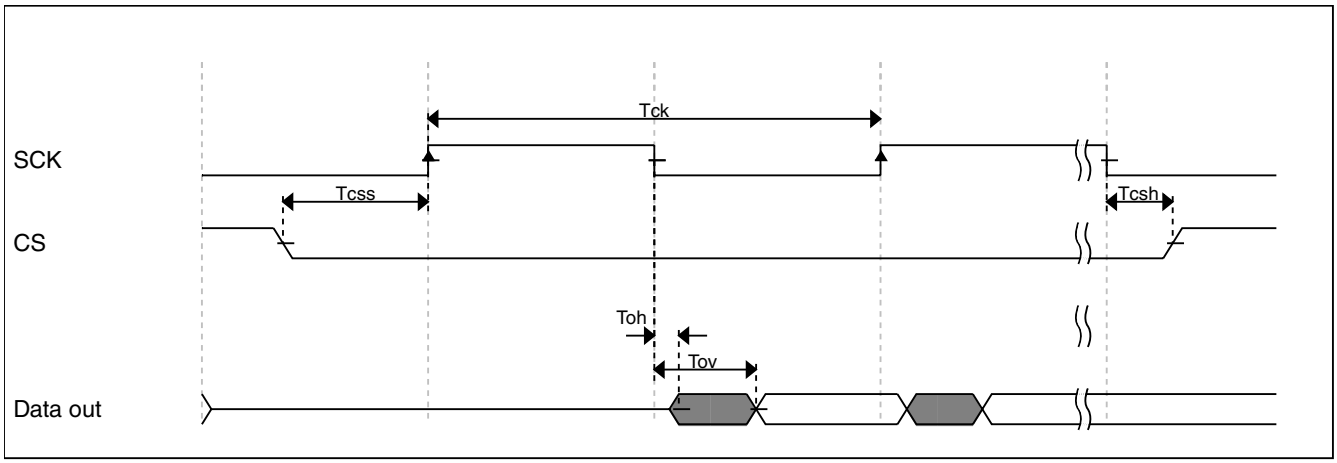


Figure 31. QuadSPI Output/Write timing (SDR mode)

Table 49. QuadSPI Output/Write timing (SDR mode)

Symbol	Parameter	Value		Unit
		Min	Max	
T_{ov}	Output Data Valid	-	3.2	ns
T_{oh}	Output Data Hold	0	-	ns
T_{ck}	SCK clock period	-	80	MHz
T_{css}	Chip select output setup time	3	-	SCK clock cycles
T_{csh}	Chip select output hold time	3	-	SCK clock cycles

NOTE

- Tcss and Tcsh are set by QuadSPI_FLSCH register, the minimum values of 3 shown are the register default values, refer to Reference Manual for further details.
- The timing in the datasheet is based on default values for the QuadSPI-SMPR register and is the recommended setting for highest SCK frequency in SDR mode.
- A negative time indicates the actual capture edge inside the device is earlier than clock appearing at pad.
- Frequency calculator guideline (Max read frequency): Tck > (Flash access time)max + (Tis)max
- A negative input hold time has no bearing on the maximum achievable operating frequency.

DDR Mode

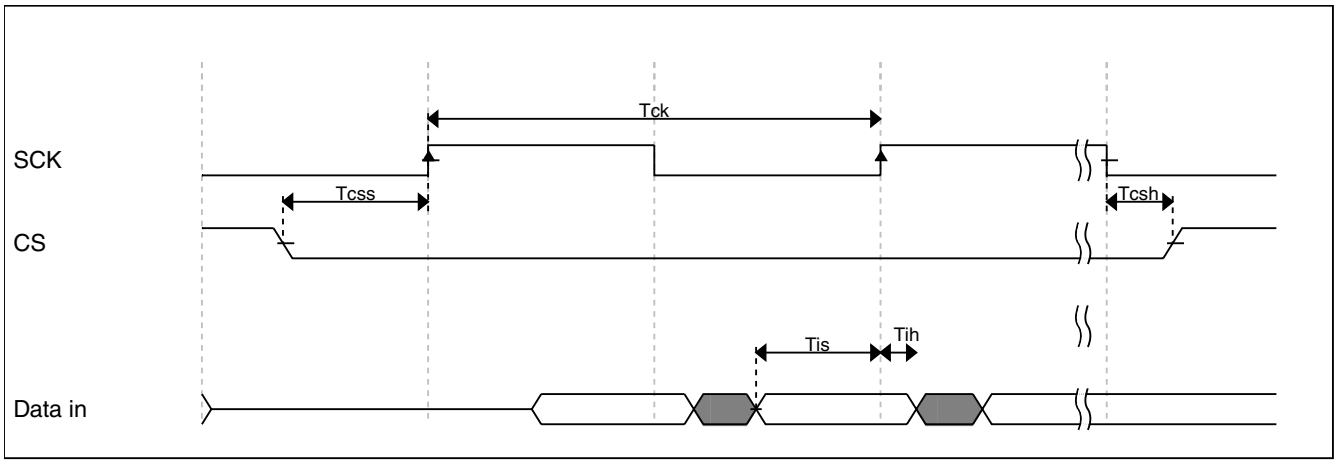


Figure 32. QuadSPI Input/Read timing (DDR mode)

NOTE

- The numbers are for a setting of 0x1 in register QuadSPI_SMPR[DDRSMP]
- Read frequency calculations should be: Tck/2 > (flash access time) + Setup (Tis) - (QuadSPI_SMPR[DDRSMP])x Tck/4
- Frequency calculator guideline (Max read frequency): Tck/2 > (Flash access time)max + (Tis)max - (QuadSPI_SMPR[DDRSMP]) x Tck/4
- Hold timing: flash_access (min) + flash_data_valid (min) > Tck/2 + HOLD(Tih) + (QuadSPI_SMPR[DDRSMP])Tck/4

Table 50. QuadSPI Input/Read timing (DDR mode)

Symbol	Parameter	Value		Unit
		Min	Max	
T_{is}	Setup time for incoming data	6.5	—	ns
T_{ih}	Hold time requirement for incoming data	0	—	ns

NOTE

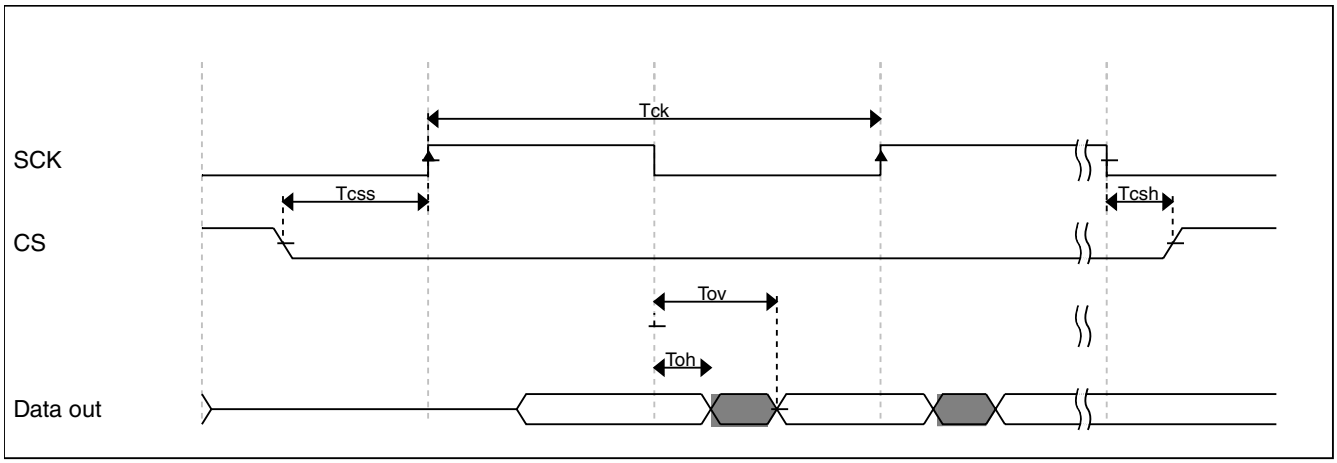


Figure 33. QuadSPI Output/Write timing (DDR mode)

Table 51. QuadSPI Output/Write timing (DDR mode)

Symbol	Parameter	Value		Unit
		Min	Max	
T_{ov}	Output Data Valid	—	3.9	ns
T_{oh}	Output Data Hold	0	—	ns
T_{ck}	SCK clock period	-	45	MHz
T_{css}	Chip select output setup time	3	-	Clk(sck)
T_{csh}	Chip select output hold time	3	-	Clk(sck)

9.5.2 NAND flash controller specifications

The NAND flash controller (NFC) implements the interface to standard NAND flash memory devices. This section describes the timing parameters of the NFC.

In the following table:

- T_H is the flash clock high time and
- T_L is flash clock low time,

which are defined as:

$T_{NFC} = T_H + T_L$

NOTE

See the CCM section of the product reference manual for further details on setting up the NFC clocks (CCM_CSCDR2[NFC_FRAC_DIV_EN + NFC_FRAC_DIV] and CCM_CSCDR3[NFC_PRE_DIV]).

Table 52. NFC specifications

Num	Description	Min.	Max.	Unit
t_{CLS}	NFC_CLE setup time	$2T_H + T_L - 1$	—	ns
t_{CLH}	NFC_CLE hold time	$T_H + T_L - 1$	—	ns
t_{CS}	$\overline{\text{NFC_CEn}}$ setup time	$2T_H + T_L - 1$	—	ns
t_{CH}	$\overline{\text{NFC_CEn}}$ hold time	$T_H + T_L$	—	ns
t_{WP}	$\overline{\text{NFC_WP}}$ pulse width	$T_L - 1$	—	ns
t_{ALS}	NFC_ALE setup time	$2T_H + T_L$	—	ns
t_{ALH}	NFC_ALE hold time	$T_H + T_L$	—	ns
t_{DS}	Data setup time	$T_L - 1$	—	ns
t_{DH}	Data hold time	$T_H - 1$	—	ns
t_{WC}	Write cycle time	$T_H + T_L - 1$	—	ns
t_{WH}	$\overline{\text{NFC_WE}}$ hold time	$T_H - 1$	—	ns
t_{RR}	Ready to $\overline{\text{NFC_RE}}$ low	$4T_H + 3T_L + 90$	—	ns
t_{RP}	$\overline{\text{NFC_RE}}$ pulse width	$T_L + 1$	—	ns
t_{RC}	Read cycle time	$T_L + T_H - 1$	—	ns
t_{REH}	$\overline{\text{NFC_RE}}$ high hold time	$T_H - 1$	—	ns
t_{IS}	Data input setup time	11	—	ns

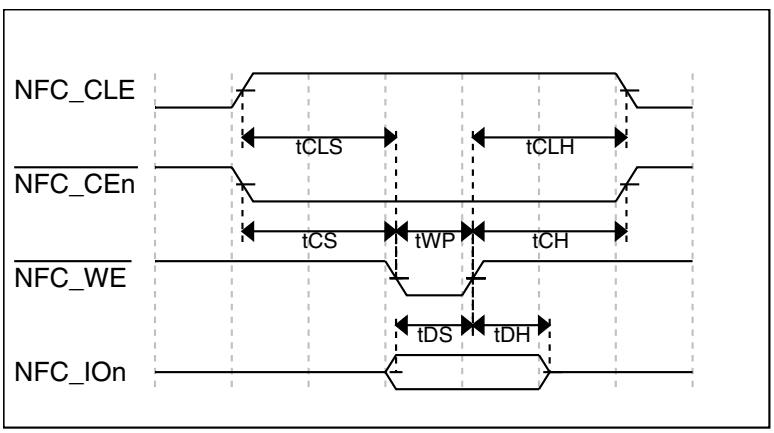


Figure 34. Command latch cycle timing

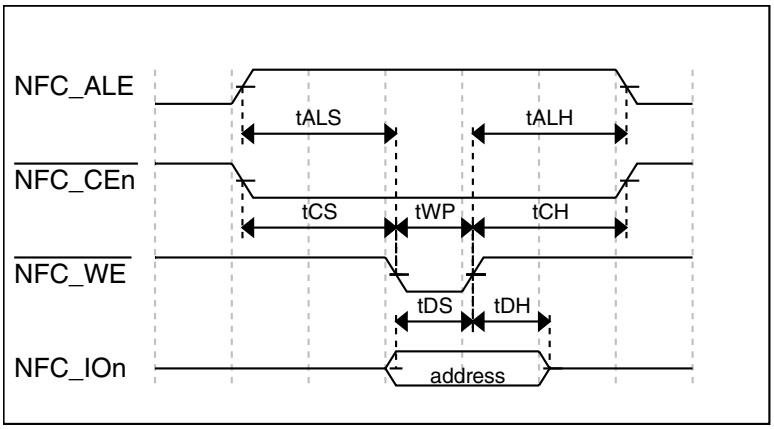


Figure 35. Address latch cycle timing

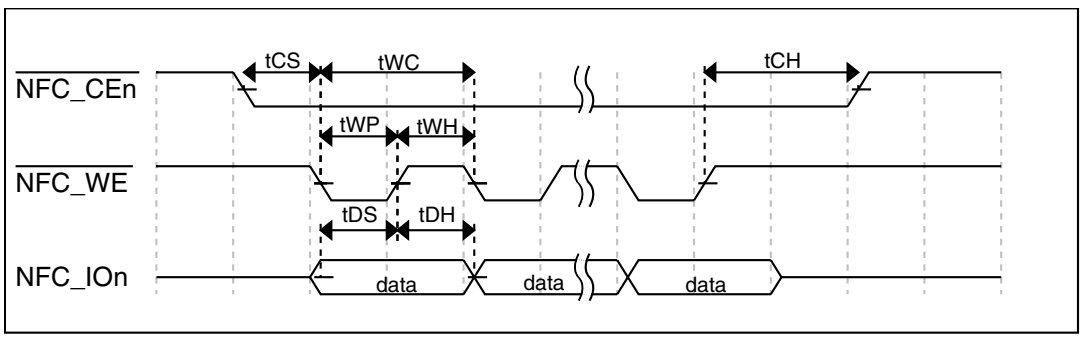


Figure 36. Write data latch cycle timing

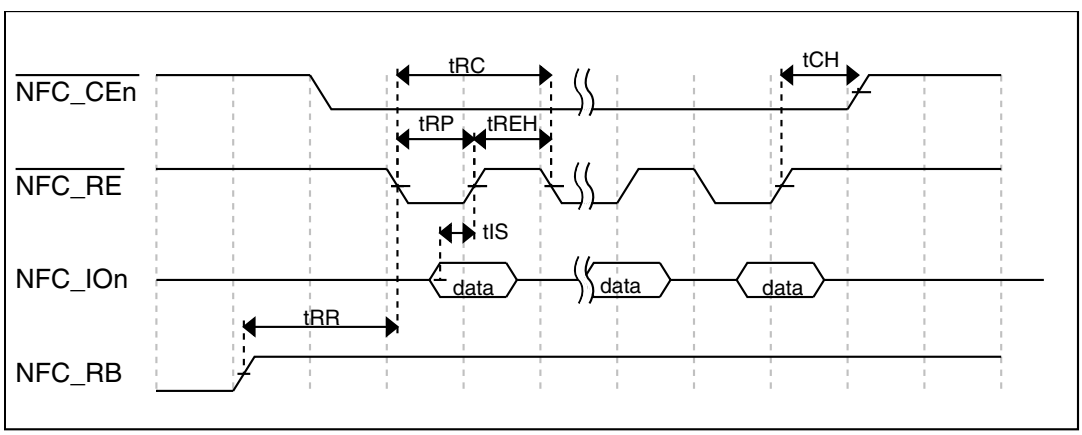


Figure 37. Read data latch cycle timing in Slow mode

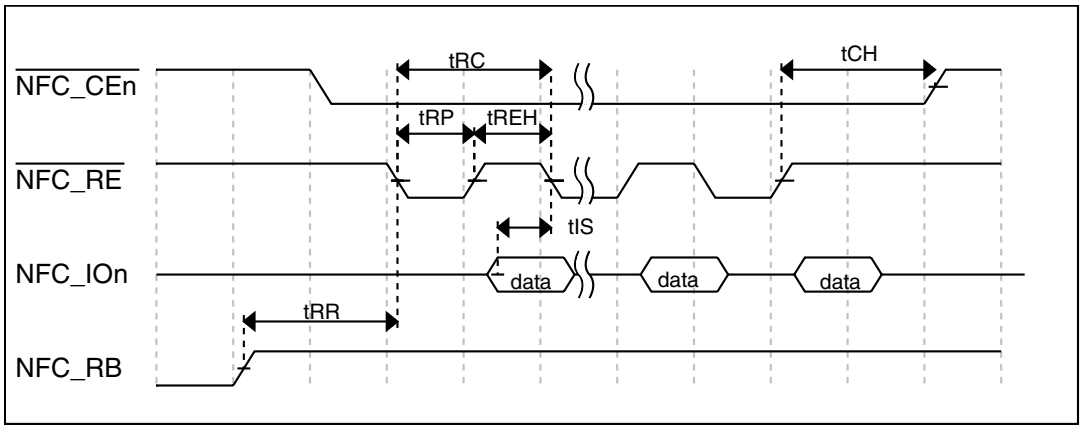


Figure 38. Read data latch cycle timing in Fast mode and EDO mode

9.5.3 FlexBus timing specifications

This section provides FlexBus timing parameters. All processor bus timings are synchronous; input setup/hold and output delay are given in respect to the rising edge of a reference clock, FB_CLK. The FB_CLK frequency may be the same as the internal system bus frequency.

The following timing numbers indicate when data is latched or driven onto the external bus, relative to the FlexBus output clock (FB_CLK). All other timing relationships can be derived from these values.

All FlexBus signals use pad type pad_fsr. The following timing specifications assume a pad slew rate setting of 11 and a load of 50 pF[3]

Table 53. FlexBus timing specifications

Num	Characteristic	Min	Max	Unit
	Frequency of operation	—	83[1] (with Wait state)	MHz
			57[2] without Wait state [1]	
FB1	Clock Period	12	—	ns
FB4	Input setup	10.6	—	ns
FB5	Input hold	0	—	ns
FB2	Output valid	—	6.4	ns
FB3	Output hold	0	—	ns

1. Freq = 1000/(11+ access time of external memory+ trace delay for clk and data)
2. Freq = 1000/(17+access time of external memory)

3. These timing parameters are specified assuming maximum operating frequency and the fastest pad slew rate setting (11).

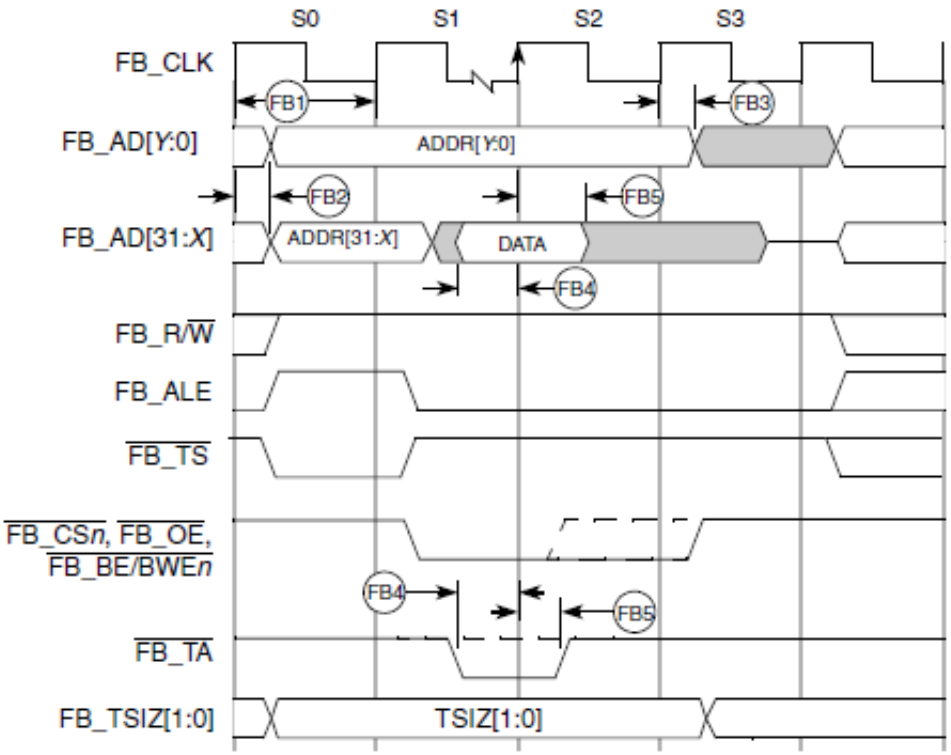


Figure 39. FlexBus read timing

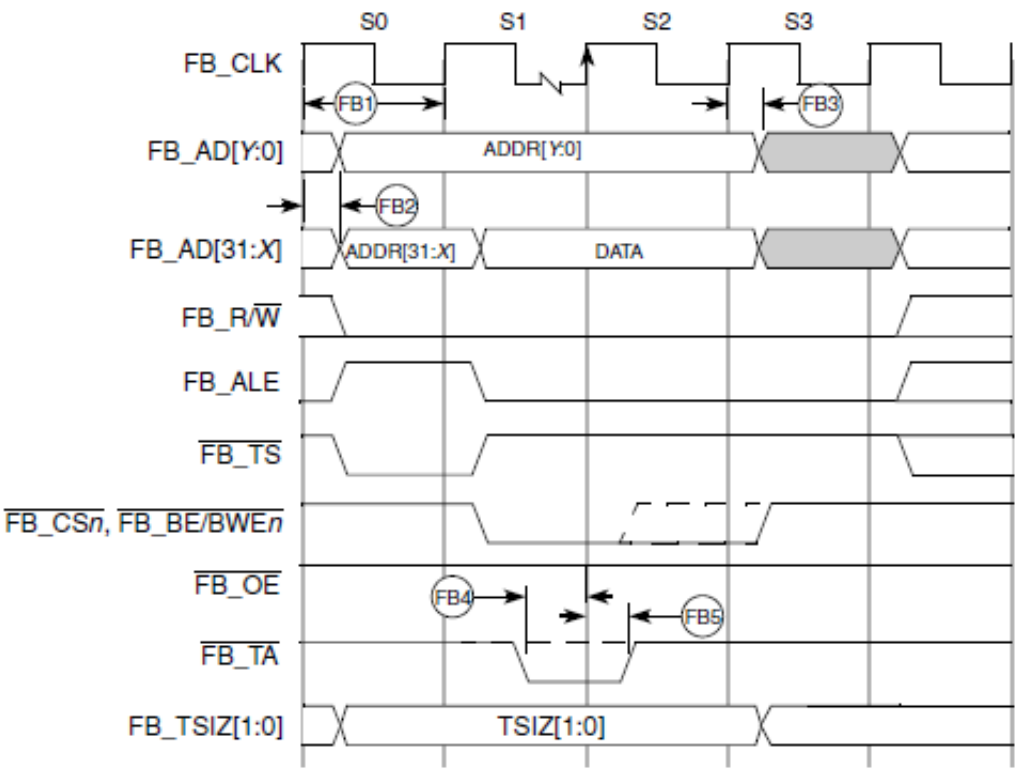


Figure 40. FlexBus write timing

9.5.4 DDR controller specifications

9.5.4.1 DDR3 Timing Parameters

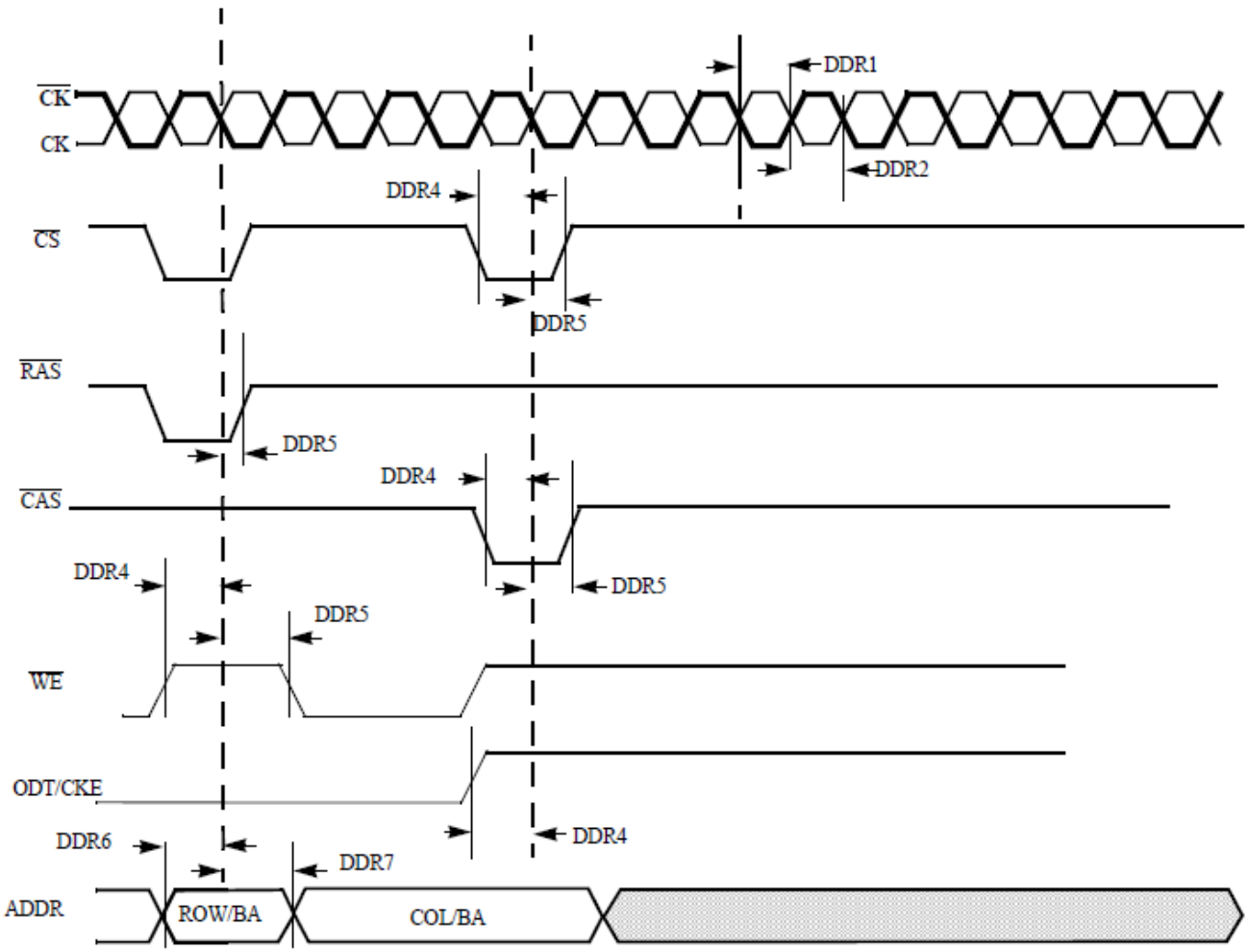


Figure 41. DDR3 Command and Address Timing Parameters

NOTE

RESET pin has a external weak pull DOWN requirement if DDR3 memory is NOT required to support content retention in the device low power modes where core voltage is off but DRAM voltage is on.

NOTE

RESET pin has a external weak pull UP requirement if DDR3 memory is required to support content retention in the device low power modes where core voltage is off but DRAM voltage is on.

NOTE

CKE pin has a external weak pull down requirement.

Table 54. DDR3 Timing Parameter

ID	Parameter	Symbol	CK = 400 MHz		Unit
			Min	Max	
DDR1	CK clock high-level width	tCH	0.47	0.53	tCK
DDR2	CK clock low-level width	tCL	0.47	0.53	tCK
DDR4	CS, RAS, CAS, CKE, WE, ODT setup time	tIS	440	-	ps
DDR5	CS, RAS, CAS, CKE, WE, ODT hold time	tIH	315	-	ps
DDR6	Address output setup time	tIS	440	-	ps
DDR7	Address output hold time	tIH	315	-	ps

NOTE

All measurements are in reference to Vref level.

NOTE

Measurements were done using balanced load and 25 ohms resistor from outputs to VDD_REF.

9.5.4.2 DDR3 Read Cycle

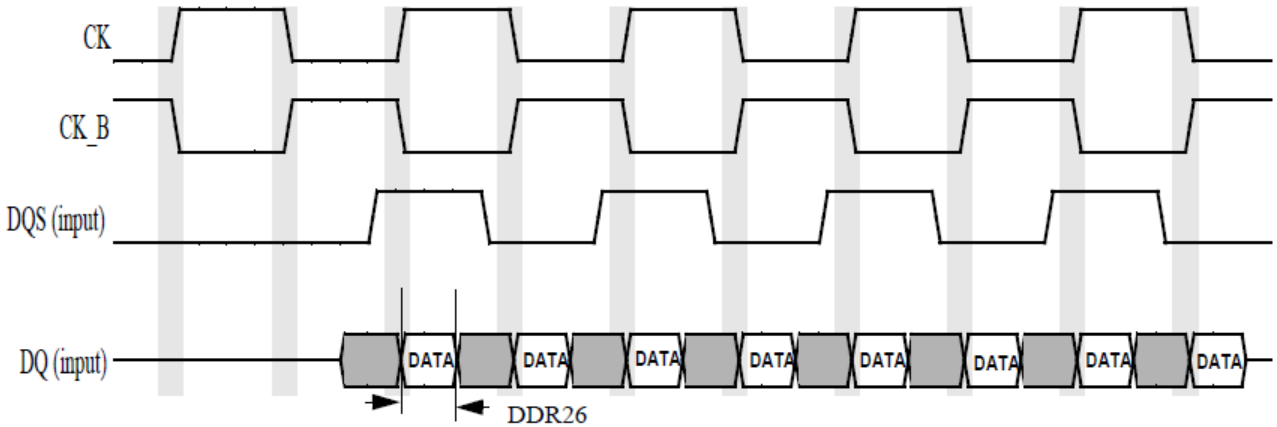


Figure 42. DDR3 Read Cycle

Table 55. DDR3 Read Cycle

ID	Parameter	Symbol	CK = 400 MHz		Unit
			Min	Max	
DDR26	Minimum required DQ valid window width	-	750	-	ps

NOTE

To receive the reported setup and hold values, read calibration should be performed in order to locate the DQS in the middle of DQ window.

NOTE

All measurements are in reference to Vref level.

NOTE

Measurements were done using balanced load and 25 ohms resistor from outputs to VDD_REF

9.5.4.3 DDR3 Write cycle

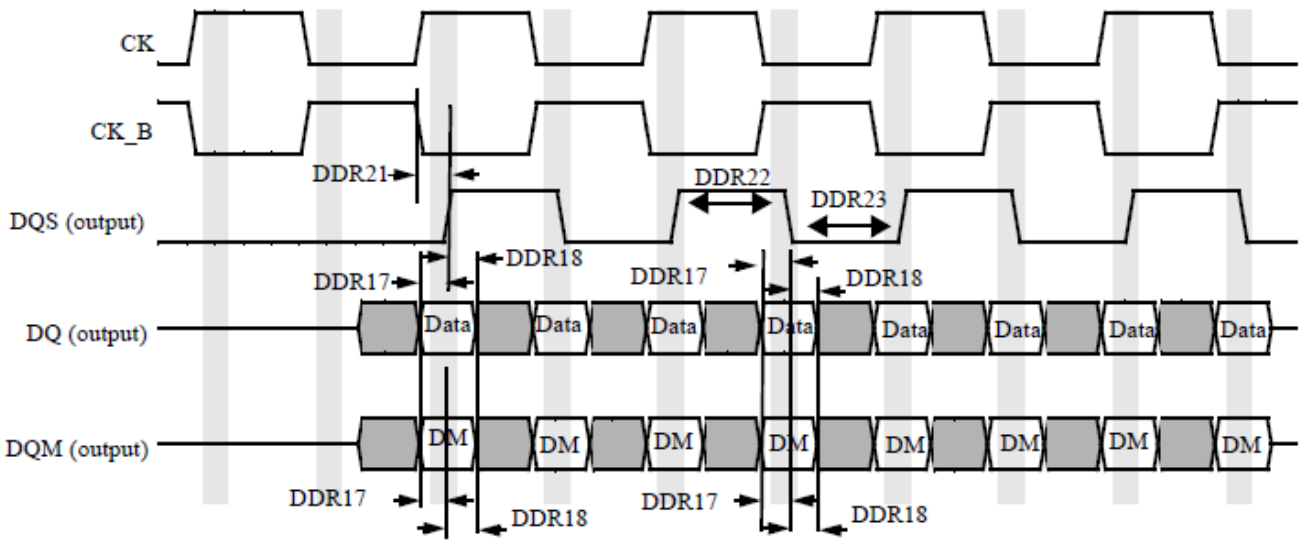


Figure 43. DDR3 Write cycle

Table 56. DDR3 Write cycle

ID	Parameter	Symbol	CK = 400 MHz		Unit
			Min	Max	
DDR17	DQ and DQM setup time to DQS (differential strobe)	tDS	240	—	ps
DDR18	DQ and DQM hold time to DQS (differential strobe)	tDH	215	—	ps
DDR21	DQS latching rising transitions to associated clock edges	tDQSS	-0.25	+0.25	tCK
DDR22	DQS high level width	tDQSH	0.45	0.55	tCK
DDR22	DQS low level width	tDQSL	0.45	0.55	tCK

NOTE

To receive the reported setup and hold values, write calibration should be performed in order to locate the DQS in the middle of DQ window.

NOTE

All measurements are in reference to Vref level.

NOTE

Measurements were done using balanced load and 25 ohms resistor from outputs to VDD_REF.

9.5.4.4 LPDDR2 Timing Parameter

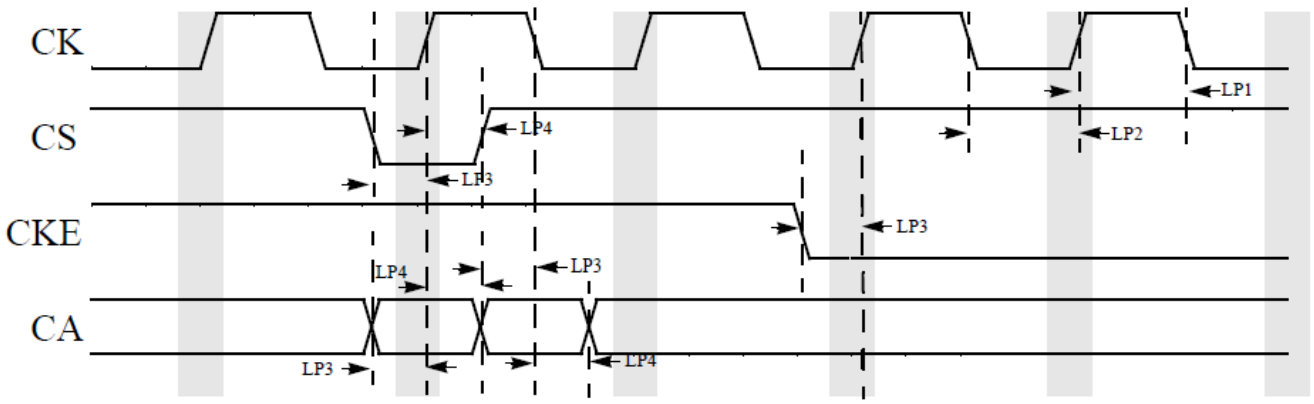


Figure 44. LPDDR2 Command and Address timing parameter

NOTE

RESET pin has a external weak pull DOWN requirement if LPDDR2 memory is NOT required to support content retention in the device low power modes where core voltage is off but DRAM voltage is on.

NOTE

RESET pin has a external weak pull UP requirement if LPDDR2 memory is required to support content retention in the device low power modes where core voltage is off but DRAM voltage is on.

NOTE

CKE pin has a external weak pull down requirement.

Table 57. LPDDR2 Timing Parameter

ID	Parameter	Symbol	CK = 400 MHz		Unit
			Min	Max	
LP1	SDRAM clock high-level width	tCH	0.45	0.55	tCK
LP2	SDRAM clock LOW-level width	tCL	0.45	0.55	tCK
LP3	CS, CKE setup time	tIS	230	-	ps
LP4	CS, CKE hold time	tIH	230	-	ps
LP3	CA setup time	tIS	230	-	ps
LP4	CA hold time	tIH	230	-	ps

NOTE

All measurements are in reference to Vref level.

NOTE

Measurements were done using balanced load and 25 ohms resistor from outputs to VDD_REF.

9.5.4.5 LPDDR2 Read Cycle

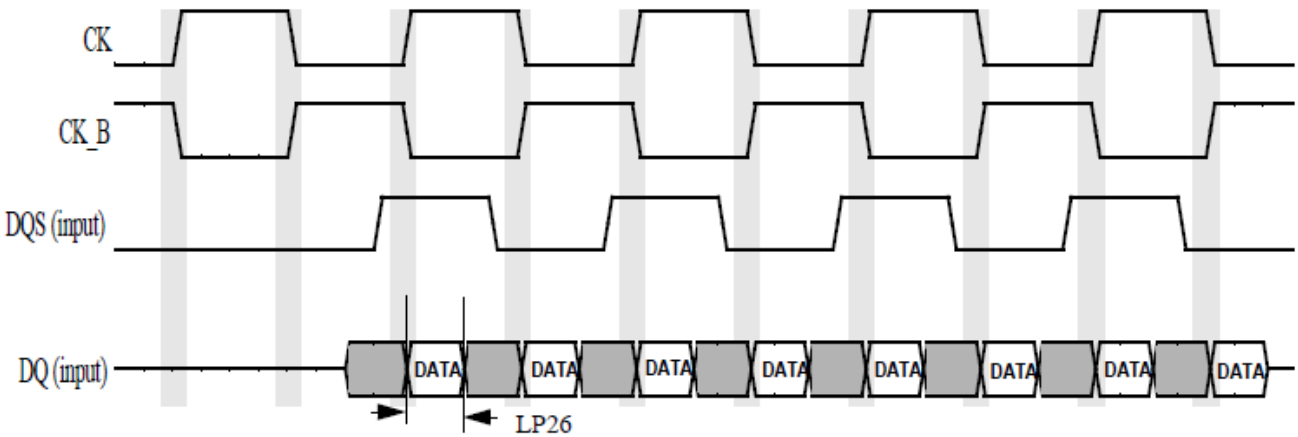


Figure 45. LPDDR2 Read cycle

Table 58. LPDDR2 Read Cycle

ID	Parameter	Symbol	CK = 400 MHz		Unit
			Min	Max	
LP26	Minimum required DQ valid window width for LPDDR2	-	270	-	ps

NOTE

To receive the reported setup and hold values, read calibration should be performed in order to locate the DQS in the middle of DQ window.

NOTE

All measurements are in reference to Vref level.

NOTE

Measurements were done using balanced load and 25 ohms resistor from outputs to VDD_REF

9.5.4.6 LPDDR2 Write Cycle

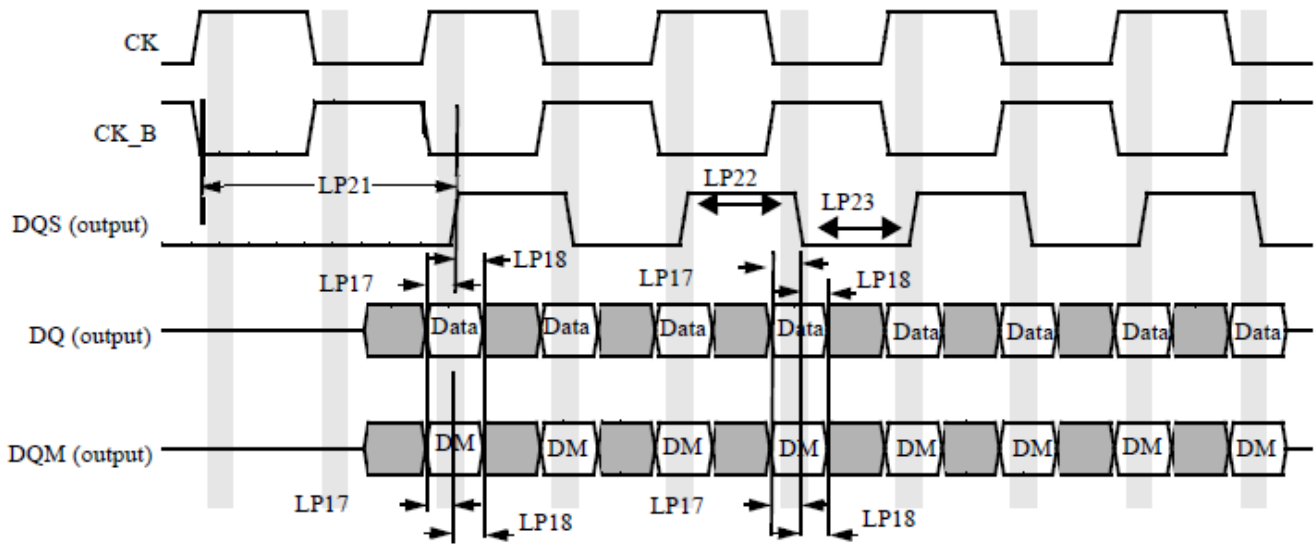


Figure 46. LPDDR3 Write Cycle

Table 59. LPDDR2 Write Cycle

ID	Parameter	Symbol	CK = 400 MHz		Unit
			Min	Max	
LP17	DQ and DQM setup time to DQS (differential strobe)	tDS	220	0.55	ps
LP18	DQ and DQM hold time to DQS (differential strobe)	tDH	220	0.55	ps
LP21	DQS latching rising transitions to associated clock edges	tDQSS	-0.25	+0.25	tCK
LP22	DQS high level width	tDQSH	0.4	-	tCK
LP23	DQS low level width	tDQSL	0.4	-	tCK

NOTE

To receive the reported setup and hold values, write calibration should be performed in order to locate the DQS in the middle of DQ window.

NOTE

All measurements are in reference to Vref level.

NOTE

Measurements were done using balanced load and 25 ohms resistor from outputs to VDD_REF.

9.6 Communication interfaces

9.6.1 MediaLB (MLB) DC Characteristics

The section lists the MediaLB 3-pin interface electrical characteristics.

Table 60. MediaLB 3-Pin Interface Electrical DC Specifications

Parameter	Symbol	Test Conditions	Min	Max	Unit
Maximum input voltage	—	—	—	3.6	V
Low level input threshold	V_{IL}	—	—	0.7	V
High level input threshold	V_{IH}	See Note[1]	1.8	—	V
Low level output threshold	V_{OL}	I_{OL} = –6 mA	—	0.4	V
High level output threshold	V_{OH}	I_{OH} = –6 mA	2.0	—	V
Input leakage current	$_{IL}$	0 < Vin < VDD	—	±10	µA

1. Higher V_{IH} thresholds can be used; however, the risks associated with less noise margin in the system must be evaluated and assumed by the customer.

9.6.2 MediaLB (MLB) Controller AC Timing Electrical Specifications

This section describes the timing electrical information of the MediaLB module.

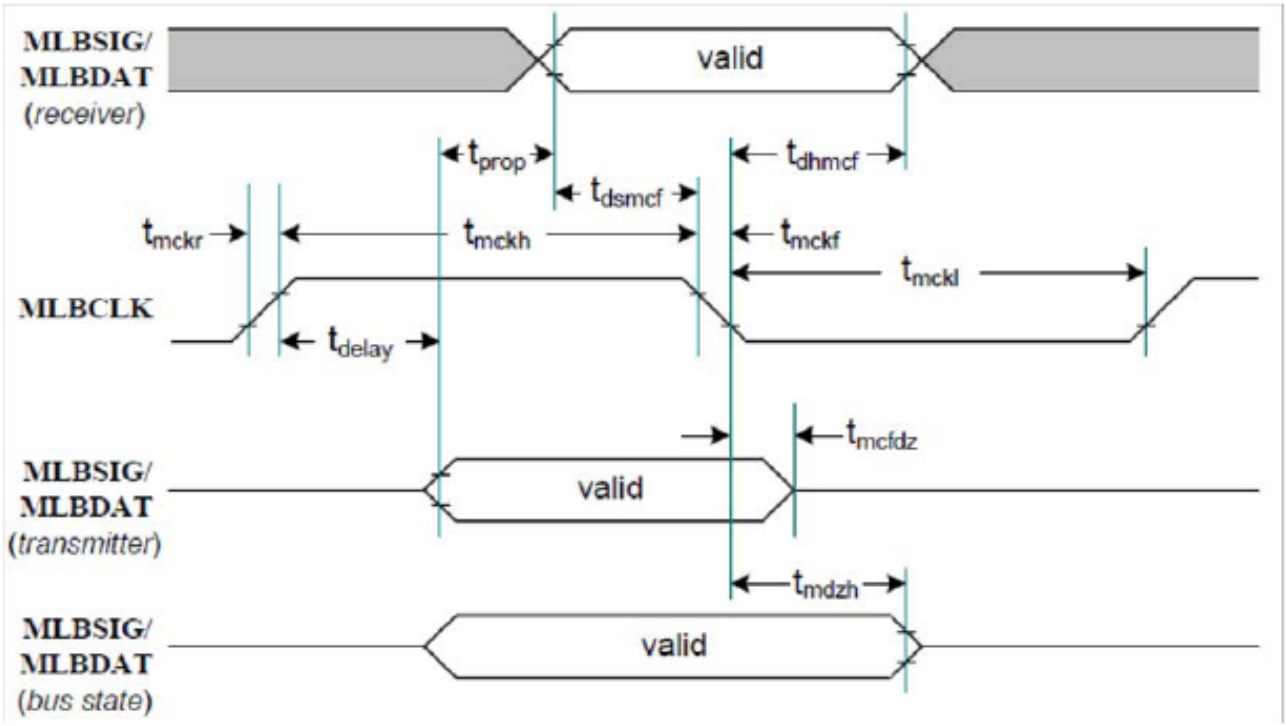


Figure 47. MediaLB 3-PinTiming

Ground = 0.0 V; Load Capacitance = 40 pF, input transition= 1 ns; MediaLB speed = 256/512 Fs; Fs = 48 kHz; all timing parameters specified from the valid voltage threshold as listed below; unless otherwise noted.

Table 61. MLB 256/512 Fs Timing Parameters

Parameter	Symbol	Min	Max	Unit	Comment
MLBCLK operating frequency	f_{mck}	11.264	25.6	MHz	256xFs at 44.0 kHz, 512xFs at 50.0 kHz
MLBCLK rise time	$t_{mck}r$	Refer Table 21		ns	$V_{IL\ to\ V_{IH}}$
MLBCLK fall time	$t_{mck}f$			ns	$V_{IH\ to\ V_{IL}}$
MLBCLK low time[1]	$t_{mck}l$	30, 14	—	ns	256xFs, 512xFs
MLBCLK high time	$t_{mck}h$	30, 14	—	ns	256xFs, 512xFs
MLBSIG/MLBDAT receiver input setup to MLBCLK falling	t_{dsmcf}	3	—	ns	—
MLBSIG/MLBDAT receiver input hold from MLBCLK low	t_{dhmcf}	2	—	ns	—
MLBSIG/MLBDAT output valid from MLBCLK low	t_{mcfdz}	0	16	ns	2
Bus output hold from MLBCLK low	t_{mdzh}	2	—	ns	—

1. MLBCLK low/high time includes the pluse width variation.

2. The MediaLB driver can release the MLBDAT/MLBSIG line as soon as MLBCLK is low; however, the logic state of the final driven bit on the line must remain on the bus for tmdzh. Therefore, coupling must be minimized while meeting the maximum load capacitance listed.

Table 62. MLB 1024 Fs Timing Parameters

Parameter	Symbol	Min	Max	Unit	Comment
MLBCLK Operating Frequency[1]	f_{mck}	45.056	51.2	MHz	1024xfs at 44.0 kHz 1024xfs at 50.0 kHz
MLBCLK rise time	f_{mckr}	Refer Table 21		ns	$V_{IL\ to}$ V_{IH}
MLBCLK fall time	f_{mckf}			ns	$V_{IH\ to}$ V_{IL}
MLBCLK low time	t_{mckl}	6.1	—	ns	2
MLBCLK high time	t_{mckh}	9.3	—	ns	
MLBSIG/MLBDAT receiver input setup to MLBCLK falling	t_{dsmcf}	3	—	ns	
MLBSIG/MLBDAT receiver input hold from MLBCLK low	t_{dhmcf}	2	—	ns	
MLBSIG/MLBDAT output valid from MLBCLK low	t_{mcfdz}	-	16	ns	3
Bus Hold from MLBCLK low	t_{mdzh}	2	—	ns	

1. The controller can shut off MLBCLK to place MediaLB in a low-power state. Depending on the time the clock is shut off, a runt pulse can occur on MLBCLK.
2. MLBCLK low/high time includes the pluse width variation.
3. The MediaLB driver can release the MLBDAT/MLBSIG line as soon as MLBCLK is low; however, the logic state of the final driven bit on the line must remain on the bus for tmdzh. Therefore, coupling must be minimized while meeting the maximum load capacitance listed.

9.6.3 DSPI timing specifications

Table 63. DSPI timing

No.	Symbol	Characteristic	Condition	Min	Max	Unit
1	t_{SCK}	SCK Cycle Time	—	t_{SYS} * 2	—	ns
4	t_{SDC}	SCK Clock Pulse Width	—	40%	60%	t_{SCK}
2	t_{CSC}	CS to SCK Delay	Master	16	—	ns
3	t_{ASC}	After SCK Delay	Master	16	—	ns
5	t_A	Slave Access Time (SS active to SOUT driven)	Slave	—	15	ns
6	t_{DI}	Slave Disable Time (SS inactive to SOUT High-Z or invalid)	Slave	—	10	ns
9	t_{SUI}	Data Setup Time for Inputs	Master	9	—	ns

Table continues on the next page...

Table 63. DSPI timing (continued)

No.	Symbol	Characteristic	Condition	Min	Max	Unit
			Slave	4	—	
10	t_{HI}	Data Hold Time for Inputs	Master	0	—	ns
			Slave	2	—	
11	t_{DV}	Data Valid (after SCK edge) for Outputs	Master	—	5	ns
			Slave	—	10	
12	t_{HO}	Data Hold Time for Outputs	Master	0	—	ns
			Slave	0	—	

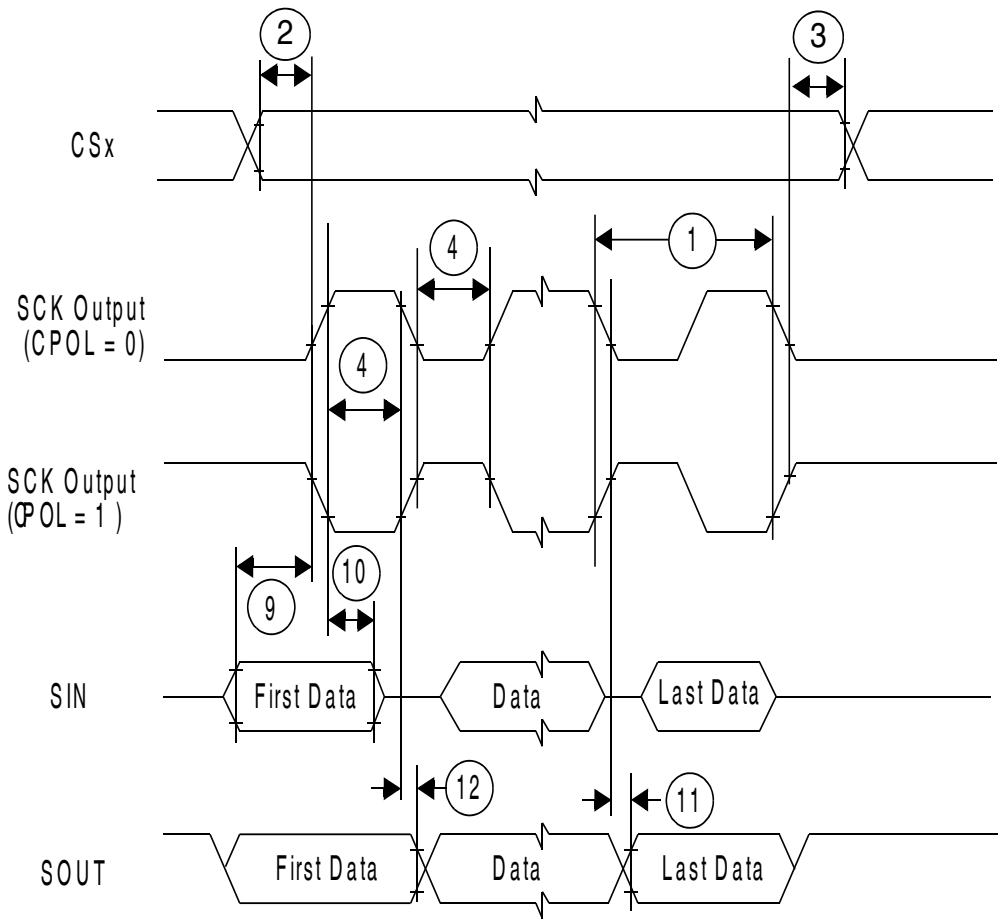


Figure 48. DSPI classic SPI timing master, CPHA=0

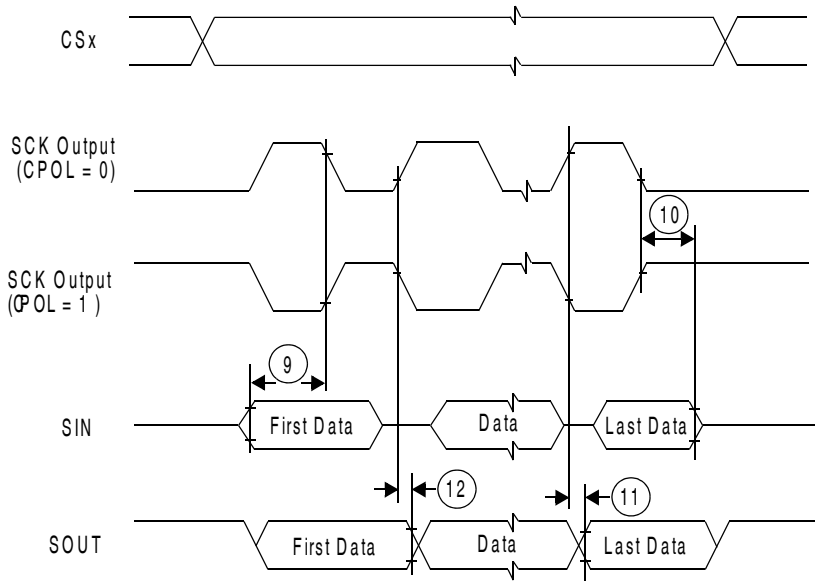


Figure 49. DSPI classic SPI timing master, CPHA=1

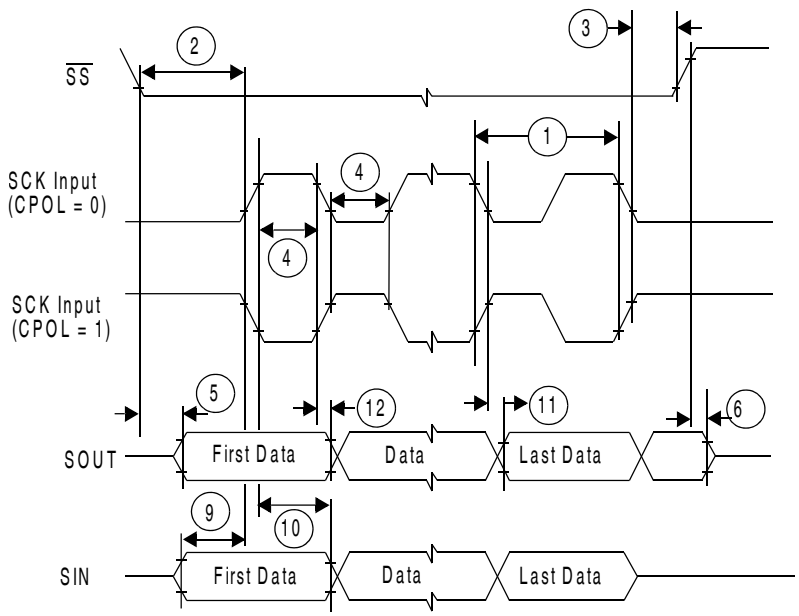


Figure 50. DSPI classic SPI timing slave, CPHA=0

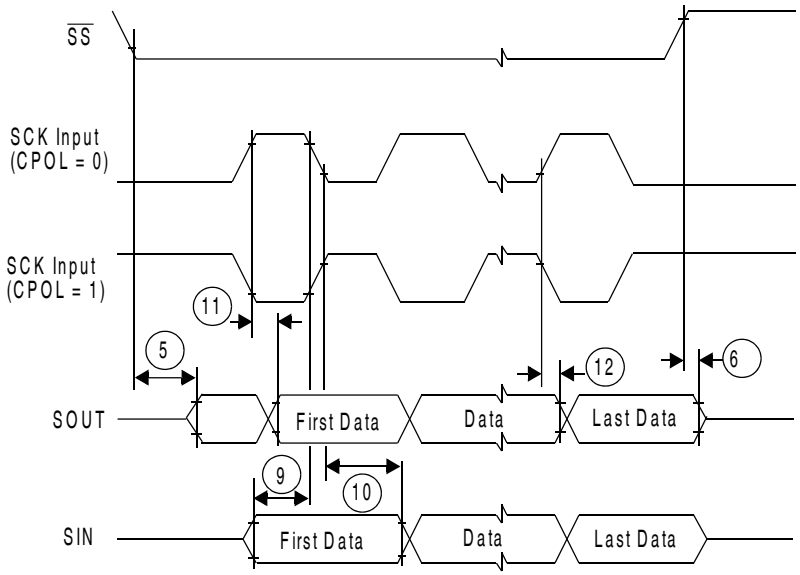


Figure 51. DSPI classic SPI timing slave, CPHA=1

9.6.4 I2C timing

Table 64. I2C input timing specifications — SCL and SDA [1]

No.	Parameter	Min.	Max.	Unit
1	Start condition hold time	2	—	PER_CLK Cycle[2]
2	Clock low time	8	—	PER_CLK Cycle
3	Bus free time between Start and Stop condition	4.7	—	µs
4	Data hold time	0.0	—	µs
5	Clock high time	4	—	PER_CLK Cycle
6	Data setup time	0.0	—	ns
7	Start condition setup time (for repeated start condition only)	2	—	PER_CLK Cycle
8	Stop condition setup time	2	—	PER_CLKCycle

1. I2C input timing is valid for Automotive and TTL inputs levels, hysteresis enabled, and an input edge rate no slower than 1 ns (10% – 90%).
2. PER_CLK is the IPG Clock which drives the I2C BIU and module clock inputs. Typically this is 66 MHz. See the Clocking Overview chapter in the device reference manual for more details.

Table 65. I2C output timing specifications — SCL and SDA [1, 2, 3, 4]

No.	Parameter	Min	Max	Unit
1	Start condition hold time	6	—	PER_CLK Cycle[5]

Table continues on the next page...

Table 65. I2C output timing specifications — SCL and SDA [1, 2, 3, 4] (continued)

No.	Parameter	Min	Max	Unit
2	Clock low time	10	—	PER_CLK Cycle
3	Bus free time between Start and Stop condition	4.7	—	µs
4	Data hold time	7	—	PER_CLK Cycle
5	Clock high time	10	—	PER_CLK Cycle
6	Data setup time	2	—	PER_CLK Cycle
7	Start condition setup time (for repeated start condition only)	20	—	PER_CLK Cycle
8	Stop condition setup time	10	—	PER_CLK Cycle

1. All output timing is worst case and includes the mismatching of rise and fall times of the output pads.
2. Output parameters are valid for CL = 25 pF, where CL is the external load to the device (lumped). The internal package capacitance is accounted for, and does not need to be subtracted from the 25 pF value.
3. Timing is guaranteed to same drive capabilities for all signals, mixing of pad drives may reduce operating speedsand may cause incorrect operation.
4. Programming the IBFD register (I2C bus Frequency Divider) with the maximum frequency results in the minimum output timings listed. The I2C interface is designed to scale the data transition time, moving it to the middle of the SCL low period. The actual position is affected by the pre-scale and division values programmed in the IBC field of the IBFD register.
5. PER_CLK is the IPG Clock which drives the I2C BIU and module clock inputs. Typically this is 66 MHz. See the Clocking Overview chapter in the device reference manual for more details.

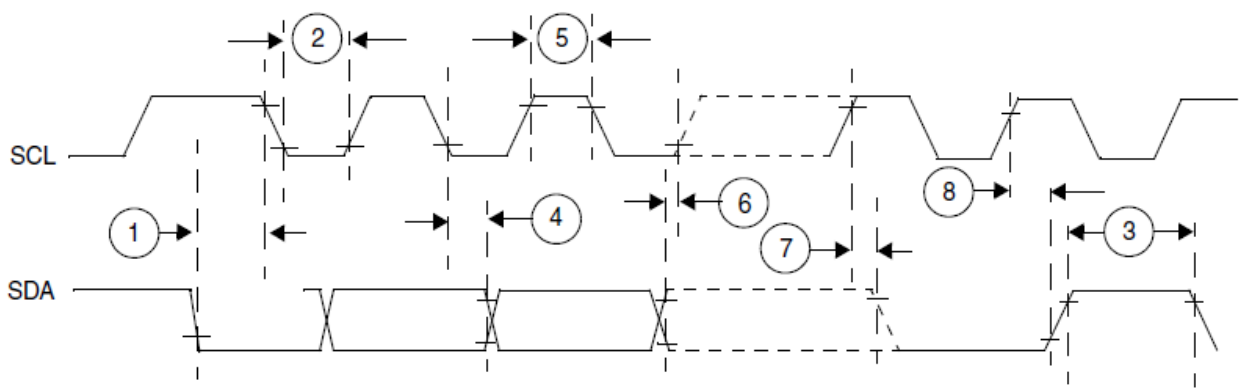


Figure 52. I2C input/output timing

9.6.5 SDHC specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface. A load of 50 pF is assumed.

Table 66. SDHC switching specifications

Num	Symbol	Description	Min.	Max.	Unit
		Operating voltage	1.71	3.6	V
	Card input clock				
SD1	fpp	Clock frequency (low speed)	0	400	kHz
	fpp	Clock frequency (SD\SDIO full speed\high speed)	0	25\50	MHz
	fpp	Clock frequency (MMC full speed\high speed)	0	20\50	MHz
	f_{OD}	Clock frequency (identification mode)	0	400	kHz
SD2	t_{WL}	Clock low time	7	—	ns
SD3	t_{WH}	Clock high time	7	—	ns
SD4	t_{TLH}	Clock rise time	—	3	ns
SD5	t_{THL}	Clock fall time	—	3	ns
	SDHC output / card inputs SDHC_CMD, SDHC_DAT (reference to SDHC_CLK)				
SD6	t_{OD}	SDHC output delay (output valid)	-5	4	ns
	SDHC input / card inputs SDHC_CMD, SDHC_DAT (reference to SDHC_CLK)				
SD7	t_{ISU}	SDHC input setup time	5	—	ns
SD8	t_{IH}	SDHC input hold time	0	—	ns

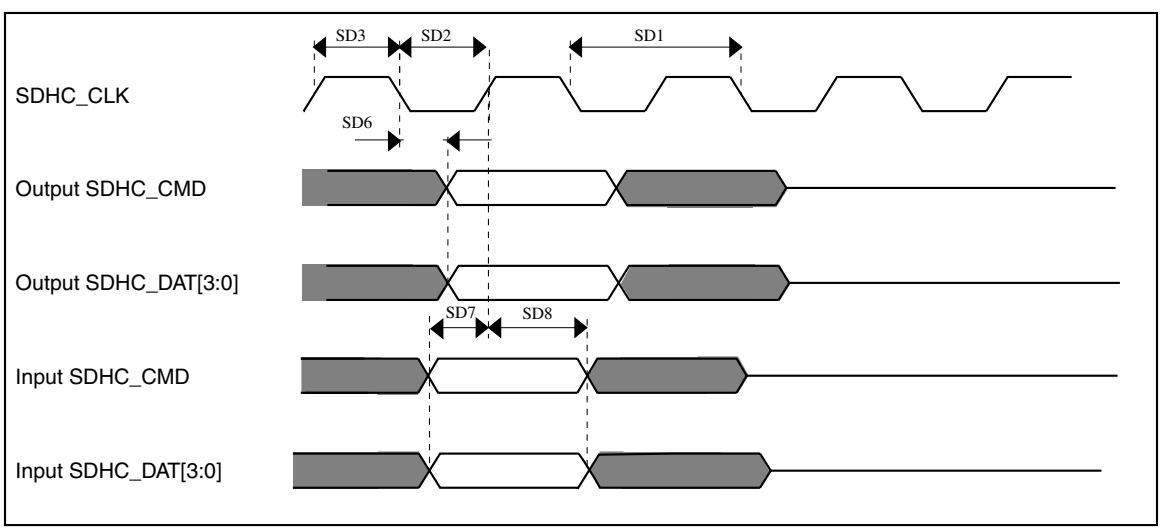


Figure 53. SDHC timing

9.6.6 USB PHY specifications

This section describes the USB-OTG PHY and the USB Host port PHY parameters.

The USB PHY meets the electrical compliance requirements defined in the Universal Serial Bus Revision 2.0 OTG, USB Host with the amendments below (On-The-Go and Embedded Host Supplement to the USB Revision 2.0 Specification is not applicable to Host port).

- USB ENGINEERING CHANGE NOTICE
  - Title: 5V Short Circuit Withstand Requirement Change
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- Errata for USB Revision 2.0 April 27, 2000 as of 12/7/2000
- USB ENGINEERING CHANGE NOTICE
  - Title: Pull-up/Pull-down resistors
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- USB ENGINEERING CHANGE NOTICE
  - Title: Suspend Current Limit Changes
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- On-The-Go and Embedded Host Supplement to the USB Revision 2.0 Specification
  - Revision 2.0 plus errata and ecn June 4, 2010
- Battery Charging Specification (available from USB-IF)
  - Revision 1.2, December 7, 2010

9.7 Clocks and PLL Specifications

9.7.1 24 MHz Oscillator Specifications

The system crystal oscillator consists of a Pierce-type structure running off the digital supply. A straight forward biased-inverter implementation is used. The crystal must be rated for a drive level of 250 μW or higher. An ESR (equivalent series resistance) of 80 Ω or less is recommended to achieve a gain margin of 5.

Table 67. 24MHz external oscillator electrical characteristics

Symbol	Parameter	Condition	Value			Unit
			Min	Typ	Max	
f_{osc}	Crystal oscillator range	—	—	24	—	MHz
I_{osc}	Startup current	—	—	< 5	—	mA
t_{uposc}	Oscillator startup time	—	—	< 5	—	ms

Table continues on the next page...

Table 67. 24MHz external oscillator electrical characteristics (continued)

Symbol	Parameter	Condition	Value			Unit
			Min	Typ	Max	
C_{IN}	Input Capacitance	EXTAL and XTAL pins	—	9	—	pF
VIH	XTAL pin input high voltage	—	0.8 x Vdd[1]	—	Vdd +0.3	V
VIL	XTAL pin input low voltage	—	Vss -0.3	—	0.2 x Vdd	V

1. V_{DD} =1.1 V ± 10%, TA = -40 to +85 °C, unless otherwise specified.

9.7.2 32 KHz Oscillator Specifications

This block implements an amplifier that when combined with a suitable quartz crystal and external load capacitors implements a low power oscillator. It also implements a power mux such that it can be powered from either a ~3 V backup battery or VDDIO such as the oscillator consumes power from VDDIO when that supply is available and transitions to the back up battery when VDDIO is lost.

In addition, if the clock monitor determines that the OSC32K is not present, then the source of the 32 K will automatically switch to the 128kHz internal RC clock divided by 4.

The OSC32k runs from vdd_rtc supply, generated inside OSC32k itself from VDDIO/ VBAT. The target battery is a ~3 V coin cell. Proper choice of coin cell type is necessary for chosen VDDIO range. Appropriate series resistor (Rs) must be used when connecting the coin cell. Rs depends on the charge current limit that depends on the chosen coin cell.

For example:

- Average Discharge Voltage is 2.5 V
- Maximum Charge Current is 0.6 mA

For a charge voltage of 3.2 V, Rs = (3.2-2.5)/0.6 m = 1.17 k

Table 68. OSC32K Main Characteristics

	Notes	Min	Typ	Max
F_{OSC}	This frequency is nominal and determined mainly by the crystal selected. 32.0 K would work as well.		32.768 KHz	
Current consumption	The 4 µA is the consumption of the oscillator alone (OSC32k). Total supply consumption will depend on what the digital portion of the RTC consumes. The ring oscillator consumes 1 µA when ring oscillator is inactive, 20 µA when the ring		4 µA	

Table continues on the next page...

Table 68. OSC32K Main Characteristics (continued)

	Notes	Min	Typ	Max
	oscillator is running. Another 1.5 µA is drawn from vdd_rtc in the power_detect block. So, the total current is 6.5 µA on vdd_rtc when the ring oscillator is not running.			
Bias resistor	This the integrated bias resistor that sets the amplifier into a high gain state. Any leakage through the ESD network, external board leakage, or even a scope probe that is significant relative to this value will debias the amp. The debiasing will result in low gain, and will impact the circuit's ability to start up and maintain oscillations.		14 MΩ	
Crystal Properties				
Cload	Usually crystals can be purchased tuned for different Cloads. This Cload value is typically 1/2 of the capacitances realized on the PCB on either side of the quartz. A higher Cload will decrease oscillation margin, but increases current oscillating through the crystal		12.5 pF	
ESR	Equivalent series resistance of the crystal. Choosing a crystal with a higher value will decrease the oscillating margin.		50 kΩ	

9.7.3 Fast internal RC oscillator (24 MHz) electrical characteristics

This section describes a fast internal RC oscillator (FIRC). This is used as the default clock at the power-up of the device.

Table 69. Fast internal oscillator electrical characteristics

Symbol	Parameter	Condition[1]	Value			
			Min	Typ	Max	Unit
f_{RCM}	RC oscillator high frequency	T_A= 25 °C, trimmed	—	24	—	MHz
I_{RCMRUN}	RC oscillator high frequency current in running mode	T_A= 25 °C, trimmed	—	55		µA
I_{RCMPWD}	RC oscillator high frequency current in power down mode	T_A= 25 °C		100		nA
RCMTRIM	RC oscillator precision after trimming of f_{RC}	T_A= 25 °C	-1	—	+1	%
RCMVAR	RC oscillator variation in temperature and supply with respect to f_{RC} at T_A = 55 °C in high frequency configuration		-5		+5	%

1. V_{DD} = 1.2 V , T_A = -40 to +85 °C, unless otherwise specified.

9.7.4 Slow internal RC oscillator (128 KHz) electrical characteristics

This section describes a slow internal RC oscillator (SIRC). This can be used as the reference clock for the RTC module.

Table 70. Slow internal RC oscillator electrical characteristics

Symbol	Parameter	Condition[1]	Value			
			Min	Typ	Max	Unit
f_{RCL}	RC oscillator low frequency	T_A= 25 °C, trimmed	—	128	—	kHz
I_{RCL}	RC oscillator low frequency current	T_A= 25 °C, trimmed	—	3.1		µA
RCLTRIM	RC oscillator precision after trimming of f_{RCL}	T_A= 25 °C	-1	—	+1	%
RCLVAR 3	RC oscillator variation in temperature and supply with respect to f_{RC} at T_A = 55 °C in high frequency configuration	High frequency configuration	-5	—	+5	%

1. V_{DD} = 1.2 V , T_A = -40 to +85 °C, unless otherwise specified.

9.7.5 PLL1 and PLL2 (528 MHz System PLL) Electrical Parameters

Table 71. PLL1 and PLL2 Electrical Parameters

Parameter	Value
Clock output range	528 MHz PLL output
Reference clock	24 MHz
Lock time	<7500 reference cycles
Period jitter(p2p)	<140ps
Duty Cycle	48.9%~51.7% PLL output

9.7.6 PLL3 and PLL7 (480 MHz USB PLL) Electrical Parameters

Table 72. PLL3 and PLL7 Electrical Parameters

Parameter	Value
Clock output range	480 MHz PLL output
Reference clock	24 MHz
Lock time	<425 reference cycles
Period jitter(p2p)	<140 ps
Duty Cycle	48.9%~51.7% PLL output

9.7.7 PLL5 (Ethernet PLL) Electrical Parameters

Table 73. PLL5 Electrical Parameters

Parameter	Value
Clock output range	500 MHz
Reference clock	24 MHz
Lock time	<7500 reference cycles
Cycle to cycle jitter (p2p)[1]	<400ps @ 50 MHz
Duty Cycle	45%~55%

1. Jitter numbers are measured at divided PLL clock because high frequency cannot be brought-out IO pad.

9.7.8 PLL4 (Audio PLL) Electrical Parameters

Table 74. PLL4 Electrical Parameters

Parameter	Value
Clock output range	650 MHz ~1.3 GHz
Reference clock	24 MHz
Lock time	<7500 reference cycles
Long term jitter(RMS)	<42ps @1128MHz
Period jitter(p2p)[1]	<115ps@1128MHz
Duty Cycle	43%~57%

1. Jitter numbers are measured at divided PLL clock because high frequency cannot be brought-out on IO pad.

9.7.9 PLL6 (Video PLL) Electrical Parameters

Table 75. PLL6 Electrical Parameters

Parameter	Value
Clock output range	650 MHz ~1.3 GHz
Reference clock	24 MHz
Lock time	<7500 reference cycles
Long term jitter(RMS)[1]	<42ps @ 1128 MHz
Period jitter(p2p)	<130ps @960MHz
Duty Cycle	43%~57%

1. Jitter numbers are measured at divided PLL clock because high frequency cannot be brought-out on IO pad & at use case frequency.

9.8 Debug specifications

9.8.1 JTAG electricals

Table 76. JTAG limited voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
J1	TCLK frequency of operation			MHz
	• Boundary Scan	-	25	
	• JTAG and CJTAG	-	25	
	• Serial Wire Debug	-	25	
J2	TCLK cycle period	1/J1	—	ns
J3	TCLK clock pulse width			
	• Boundary Scan	20	—	ns
	• JTAG and CJTAG	20	—	ns
	• Serial Wire Debug	20	—	ns
J4	TCLK rise and fall times	Refer Table 21		ns
J5	Boundary scan input data setup time to TCLK rise	8	—	ns
J6	Boundary scan input data hold time after TCLK rise	1.3	—	ns
J7	TCLK low to boundary scan output data valid	—	17	ns
J8	TCLK low to boundary scan output high-Z	—	17	ns
J9	TMS, TDI input data setup time to TCLK rise	8	—	ns
J10	TMS, TDI input data hold time after TCLK rise	1.3	—	ns
J11	TCLK low to TDO data valid	—	17	ns
J12	TCLK low to TDO high-Z	—	17	ns

NOTE

Input transition (1ns), output load (25 pf) and SRE (000), DSE (111), FSEL(011).

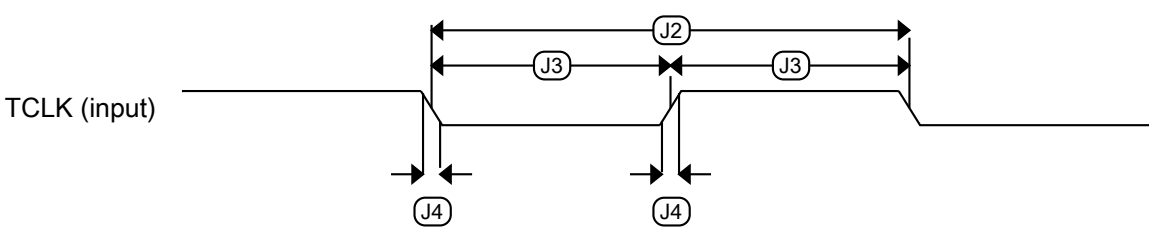


Figure 54. Test clock input timing

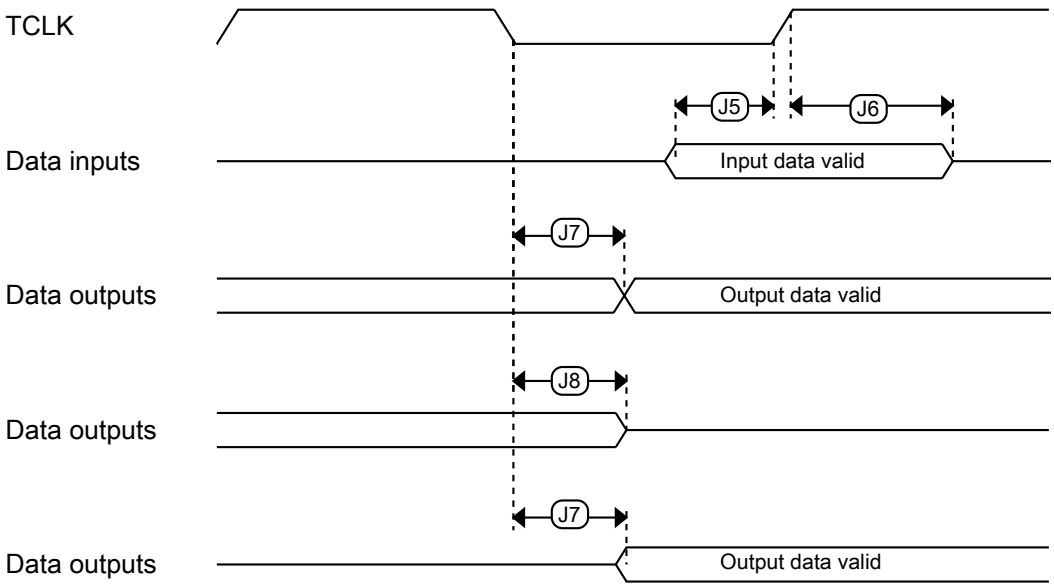


Figure 55. Boundary scan (JTAG) timing

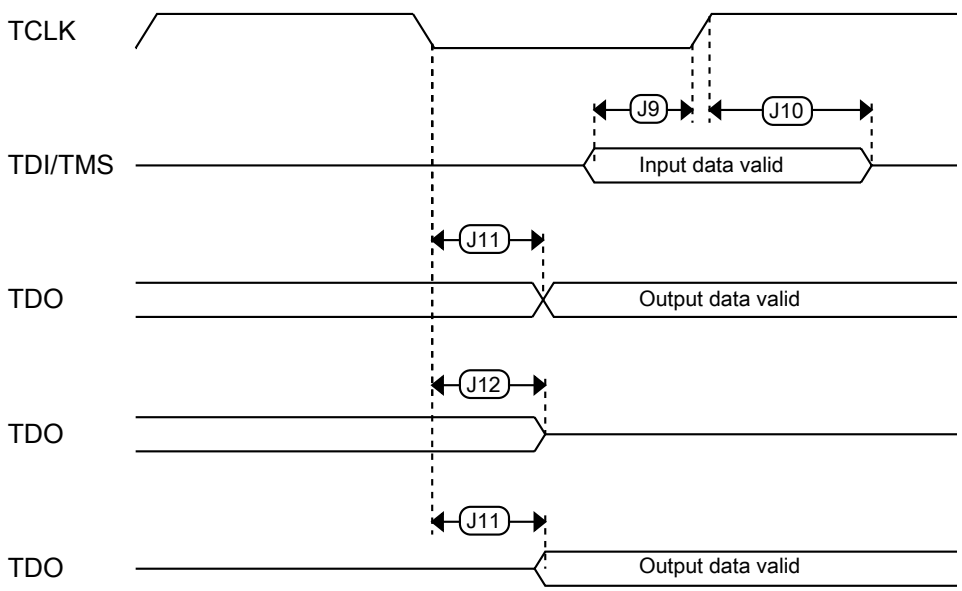


Figure 56. Test Access Port timing

9.8.2 Debug trace timing specifications

Table 77. Debug trace operating behaviors

Symbol	Description	Min.	Max.	Unit
T_{cyc}	Clock period	50		MHz
T_{wl}	Low pulse width	2	—	ns
T_{wh}	High pulse width	2	—	ns
T_r	Clock and data rise time	Refer Table 21		ns
T_f	Clock and data fall time Refer			ns
tDV	Data output valid	3	—	ns
tHO	Data output hold	1	—	ns

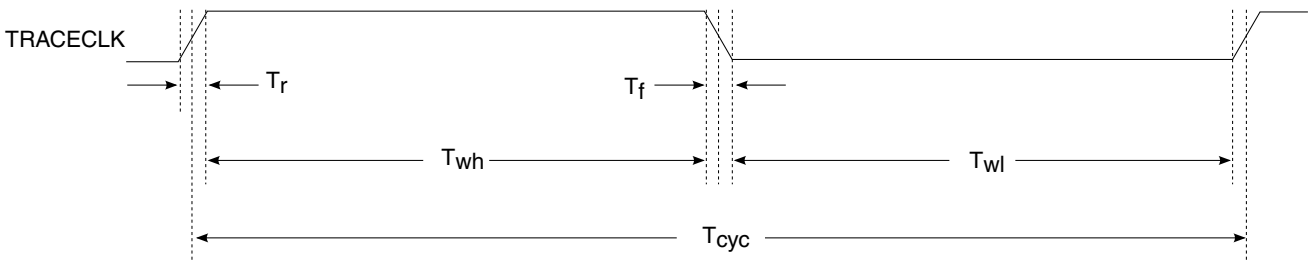


Figure 57. TRACE_CLKOUT specifications

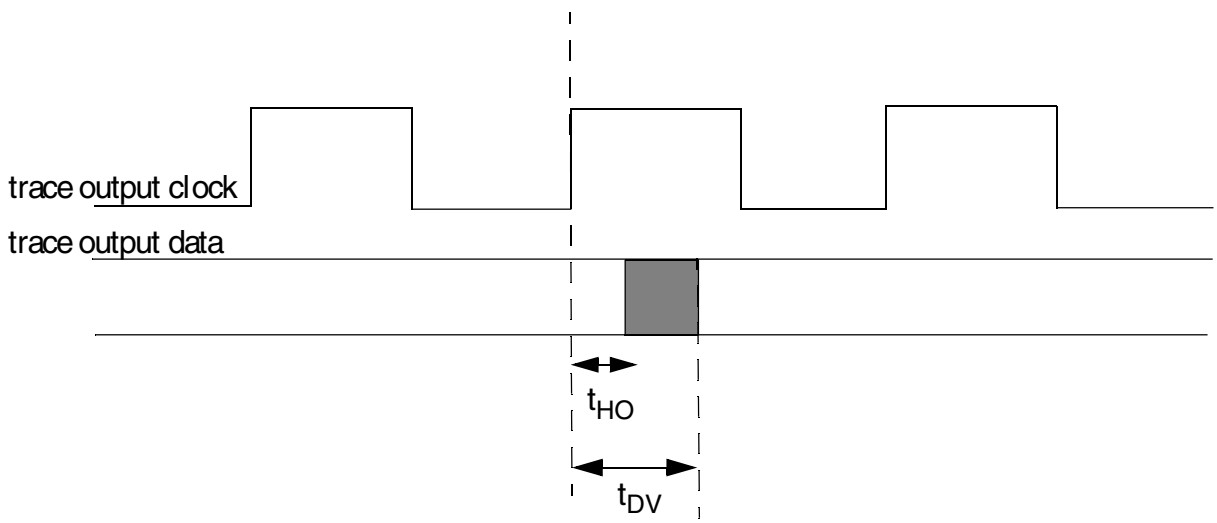


Figure 58. Trace data specifications

10 Thermal attributes

10.1 Thermal attributes

This table shows the thermal attributes for the 176 LQFP package.

Board type	Symbol	Description	176 LQFP	Unit	Notes
Single-layer (1s)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	50	°C/W	1, 2
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	32	°C/W	1,3
Single-layer (1s)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./ min. air speed)	40	°C/W	1, 3
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./ min. air speed)	25	°C/W	1, 3
—	$R_{\theta JB}$	Thermal resistance, junction to board	21	°C/W	4
—	$R_{\theta JCtop}$	Thermal resistance, junction to case top	12	°C/W	5
—	Ψ_{JT}	Thermal characterization parameter, junction to package top (natural convection)	3	°C/W	6

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance
2. Per JEDEC JESD51-2 with the single layer board (JESD51-3) horizontal
3. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

This table shows the thermal attributes for the 364 MAPBGA package.

Board type	Symbol	Description	364 MAPBGA	Unit	Notes
Single-layer (1s)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	45	°C/W	1, 2
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	28	°C/W	1, 3
Single-layer (1s)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./ min. air speed)	37	°C/W	1,3
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./ min. air speed)	24	°C/W	1,3
—	$R_{\theta JB}$	Thermal resistance, junction to board	17	°C/W	4
—	$R_{\theta JC}$	Thermal resistance, junction to case	10	°C/W	5
—	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	2	°C/W	6

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with the single layer board horizontal. Board meets JESD51-9 specification.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2.

11 Dimensions

11.1 Obtaining package dimensions

Package dimensions are provided in package drawing.

To find a package drawing, go to www.nxp.com and perform a keyword search for the drawing's document number:

Package	Document Number
176-pin LQFP	98ASA00452D
364 MAPBGA	98ASA00418D

12 Pinouts

12.1 Pinouts

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The IOMUX Controller Module is responsible for selecting which ALT functionality is available on each pin.

364 MAP BGA	176 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
Y2	—	ADC0SE8	N/A		ADC0_SE8							
W2	—	ADC0SE9			ADC0_SE9							
W3	—	ADC1SE8			ADC1_SE8							
Y3	—	ADC1SE9			ADC1_SE9							
W1	34	VREFH_ADC			VREFH_ADC							
U3	33	VREFL_ADC			VREFL_ADC							
V1	31	VDDA33_ADC			VDDA33_ADC							
V2	32	VSSA33_ADC			VSSA33_ADC							
U1	29	DACO0			DACO0							
U2	30	DACO1			DACO1							
Y4	35	VADCSE0			VADCSE0							
U4	37	VADCSE1			VADCSE1							
W4	—	VADCSE2			VADCSE2							
V5	—	VADCSE3			VADCSE3							
V3	40	VDDA33_AFE			VDDA33_AFE							
V4	39	VSSA33_AFE			VSSA33_AFE							
T5	36	VDD12_AFE			VDD12_AFE							
R5	38	VSS12_AFE			VSS12_AFE							
U5	41	VADC_AFE_BANDGAP			VADC_AFE_BANDGAP							
Y13	73	EXTAL			EXTAL							
W13	72	XTAL			XTAL							
Y12	70	EXTAL32			EXTAL32							

364 MAP BGA	176 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
W12	71	XTAL32			XTAL32							
T4	28	RESETB/ RESET_OUT	RESETB/ RESET_OUT		RESETB/ RESET_OUT							
N5	19	PTA6		PTA6	RMII_ CLKOUT	RMII_CLKIN/ MII0_TXCLK		DCU1_ TCON11			DCU1_R2	
T3	27	TEST			TEST							
T1	23	Ext_POR			TEST2							
V12	69	DECAP_ V11_LDO_ OUT			DECAP_ V11_LDO_ OUT							
T11	65	DECAP_ V25_LDO_ OUT			DECAP_ V25_LDO_ OUT							
T2	26	BCTRL			BCTRL							
P5	24	VDDREG			VDDREG							
T12	68	VDD33_ LDOIN			VDD33_ LDOIN							
V11	67	VSS			VSS							
U11	66	VSS_KEL0			VSS_KEL0							
W14	—	LVDS0P			LVDS0P							
Y14	—	LVDS0N			LVDS0N							
K4	3	JTCLK/ SWCLK	JTCLK/ SWCLK	PTA8	JTCLK/ SWCLK			DCU0_R0			MLBCLK	
K2	4	JTDI	JTDI	PTA9	JTDI	RMII_ CLKOUT	RMII_CLKIN/ MII0_TXCLK	DCU0_R1		WDOG_b		
K1	5	JTDO	JTDO/ TRACESWO	PTA10	JTDO	EXT_AUDIO_ MCLK		DCU0_G0		ENET_TS_ CLKIN	MLBSIGNAL	
L1	6	JTMS/ SWDIO	JTMS/ SWDIO	PTA11	JTMS/ SWDIO			DCU0_G1			MLBDATA	
L3	7	PTA12		PTA12	TRACECK	EXT_AUDIO_ MCLK				VIU_DATA13	I2C0_SCL	
Y5	43	PTA16		PTA16	TRACED0	USB0_ VBUS_EN	ADC1_SE0	LCD29	SAI2_TX_ BCLK	VIU_DATA14	I2C0_SDA	
Y6	44	PTA17		PTA17	TRACED1	USB0_ VBUS_OC	ADC1_SE1	LCD30	USB0_SOF_ PULSE	VIU_DATA15	I2C1_SCL	
V6	46	PTA18		PTA18	TRACED2	ADC0_SE0	FTM1_QD_ PHA	LCD31	SAI2_TX_ DATA	VIU_DATA16	I2C1_SDA	
U6	47	PTA19		PTA19	TRACED3	ADC0_SE1	FTM1_QD_ PHB	LCD32	SAI2_TX_ SYNC	VIU_DATA17	QSPI1_A_ SCK	
B18	143	PTA20		PTA20	TRACED4			LCD33		SCI3_TX	DCU1_ HSYNC/ DCU1_ TCON1	
D18	145	PTA21		PTA21/ MII0_RXCLK	TRACED5				SAI2_RX_ BCLK	SCI3_RX	DCU1_ VSYNC/ DCU1_ TCON2	

364 MAP BGA	176 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
E17	147	PTA22		PTA22	TRACED6				SAI2_RX_DATA	I2C2_SCL	DCU1_TAG/DCU1_TCON0	
C17	148	PTA23		PTA23	TRACED7				SAI2_RX_SYNC	I2C2_SDA	DCU1_DE/DCU1_TCON3	
R16	—	PTA24		PTA24	TRACED8	USB1_VBUS_EN			SDHC1_CLK	DCU1_TCON4		
R17	—	PTA25		PTA25	TRACED9	USB1_VBUS_OC			SDHC1_CMD	DCU1_TCON5		
R19	—	PTA26		PTA26	TRACED10	SAI3_TX_BCLK			SDHC1_DAT0	DCU1_TCON6		
R20	—	PTA27		PTA27	TRACED11	SAI3_RX_BCLK			SDHC1_DAT1	DCU1_TCON7		
P20	—	PTA28		PTA28	TRACED12	SAI3_RX_DATA	ENET1_1588_TMR0	SCI4_TX	SDHC1_DAT2	DCU1_TCON8		
P18	—	PTA29		PTA29	TRACED13	SAI3_TX_DATA	ENET1_1588_TMR1	SCI4_RX	SDHC1_DAT3	DCU1_TCON9		
P17	—	PTA30		PTA30	TRACED14	SAI3_RX_SYNC	ENET1_1588_TMR2	SCI4_RTS	I2C3_SCL		SCI3_TX	
P16	—	PTA31		PTA31	TRACED15	SAI3_TX_SYNC	ENET1_1588_TMR3	SCI4_CTS	I2C3_SDA		SCI3_RX	
T6	49	PTB0		PTB0	FTM0_CH0	ADC0_SE2	TRACECTL	LCD34	SAI2_RX_BCLK	VIU_DATA18	QSPI1_A_CS0	
T7	50	PTB1	RCON30	PTB1	FTM0_CH1	ADC0_SE3	RCON30	LCD35	SAI2_RX_DATA	VIU_DATA19	QSPI1_A_DATA3	
V7	51	PTB2	RCON31	PTB2	FTM0_CH2	ADC1_SE2	RCON31	LCD36	SAI2_RX_SYNC	VIU_DATA20	QSPI1_A_DATA2	
W7	53	PTB3		PTB3	FTM0_CH3	ADC1_SE3	EXTRIG	LCD37		VIU_DATA21	QSPI1_A_DATA1	
Y7	54	PTB4		PTB4	FTM0_CH4	SCI1_TX	ADC0_SE4	LCD38	VIU_FID	VIU_DATA22	QSPI1_A_DATA0	
Y8	55	PTB5		PTB5	FTM0_CH5	SCI1_RX	ADC1_SE4	LCD39	VIU_DE	VIU_DATA23	QSPI1_A_DQS	
W8	56	PTB6		PTB6	FTM0_CH6	SCI1_RTS	QSPI0_A_CS1	LCD40	FB_CLKOUT	VIU_HSYNC	SCI2_TX	
D13	166	PTB7		PTB7	FTM0_CH7	SCI1_CTS	QSPI0_B_CS1	LCD41		VIU_VSYNC	SCI2_RX	
J16	121	PTB8		PTB8	FTM1CH0		FTM1_QD_PHA		VIU_DE		DCU1_R6	
J19	123	PTB9		PTB9	FTM1CH1		FTM1_QD_PHB				DCU1_R7	
B15	159	PTB10		PTB10	SCI0_TX			DCU0_TCON4	VIU_DE	CKO1	ENET_TS_CLKIN	
D14	164	PTB11		PTB11	SCI0_RX			DCU0_TCON5	SNVS_ALARM_OUT_B	CKO2	ENET0_1588_TMR0	

364 MAP BGA	176 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
E13	165	PTB12	NMI	PTB12	SCI0_RTS		SPI0_PCS5	DCU0_ TCON6	FB_AD1	NMI	ENET0_ 1588_TMR1	
D15	156	PTB13		PTB13	SCI0_CTS		SPI0_PCS4	DCU0_ TCON7	FB_AD0	TRACECTL		
B14	162	PTB14		PTB14	CAN0_RX	I2C0_SCL		DCU0_ TCON8			DCU1_PCLK	
A14	161	PTB15		PTB15	CAN0_TX	I2C0_SDA		DCU0_ TCON9			VIU_PIX_ CLK	
C14	163	PTB16		PTB16	CAN1_RX	I2C1_SCL		DCU0_ TCON10				
A15	160	PTB17		PTB17	CAN1_TX	I2C1_SDA		DCU0_ TCON11				
B12	171	PTB18		PTB18	SPI0_PCS1	EXT_AUDIO_ MCLK				VIU_DATA9	CCM_OBS0	
C13	167	PTB19		PTB19	SPI0_PCS0					VIU_DATA10	CCM_OBS1	
A13	169	PTB20		PTB20	SPI0_SIN			LCD42		VIU_DATA11	CCM_OBS2	
E12	173	PTB21		PTB21	SPI0_SOUT			LCD43		VIU_DATA12	DCU1_PCLK	
D12	172	PTB22		PTB22	SPI0_SCK				VIU_FID			
V10	61	USB0_GND			USB0_GND							
T10	63	USB0_DP			USB0_DP							
T9	62	USB0_DM			USB0_DM							
W11	60	USB0_VBUS			USB0_VBUS							
Y10	59	USB_DCAP			USB_DCAP							
Y11	64	USB0_ VBUS_ DETECT			USB0_ VBUS_ DETECT							
Y9	—	USB1_GND			USB1_GND							
W9	—	USB1_DP			USB1_DP							
V9	—	USB1_DM			USB1_DM							
W10	—	USB1_VBUS			USB1_VBUS							
U9	—	USB1_ VBUS_ DETECT			USB1_ VBUS_ DETECT							
L4	8	PTC0		PTC0	RMII0_MDC/ MII0_MDC	FTM1CH0	SPI0_PCS3	ESAI_SCKT	SDHC0_CLK	VIU_DATA0	RCON18	
L5	9	PTC1		PTC1	RMII0_MDIO/ MII0_MDIO	FTM1CH1	SPI0_PCS2	ESAI_FST	SDHC0_CMD	VIU_DATA1	RCON19	
M5	11	PTC2		PTC2	RMII0_CRS_ DV	SCI1_TX		ESAI_SDO0	SDHC0_ DAT0	VIU_DATA2	RCON20	
M3	12	PTC3		PTC3	RMII0_RXD1/ MII0_RXD[1]	SCI1_RX		ESAI_SDO1	SDHC0_ DAT1	VIU_DATA3	DCU0_R0	
L2	14	PTC4		PTC4	RMII0_RXD0/ MII0_RXD[0]	SCI1_RTS	SPI1_PCS1	ESAI_SDO2/ ESAI_SDI3	SDHC0_ DAT2	VIU_DATA4	DCU0_R1	
M1	15	PTC5		PTC5	RMII0_RXER/ MII0_RXER	SCI1_CTS	SPI1_PCS0	ESAI_SDO3/ ESAI_SDI2	SDHC0_ DAT3	VIU_DATA5	DCU0_G0	

364 MAP BGA	176 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
N1	16	PTC6		PTC6	RMII0_TXD1/ MII0_TXD[1]		SPI1_SIN	ESAI_SDO5/ ESAI_SDI0	SDHC0_WP	VIU_DATA6	DCU0_G1	
N2	17	PTC7		PTC7	RMII0_TXD0/ MII0_TXD[0]		SPI1_SOUT	ESAI_SDO4/ ESAI_SDI1		VIU_DATA7	DCU0_B0	
N4	18	PTC8		PTC8	RMII0_TXEN/ MII0_TXEN		SPI1_SCK			VIU_DATA8	DCU0_B1	
T15	—	PTC9		PTC9	RMII1_MDC		ESAI_SCKT			MLBCLK		
U15	—	PTC10		PTC10	RMII1_MDIO		ESAI_FST			MLBSIGNAL		
P4	—	PTC11		PTC11	RMII1_CRS_ DV		ESAI_SDO0			MLBDATA		
P3	—	PTC12		PTC12	RMII1_RXD1		ESAI_SDO1		SAI2_TX_ BCLK			
P1	—	PTC13		PTC13	RMII1_RXD0		ESAI_SDO2/ ESAI_SDI3		SAI2_RX_ BCLK			
R1	—	PTC14		PTC14	RMII1_RXER		ESAI_SDO3/ ESAI_SDI2	SCI5_TX	SAI2_RX_ DATA	ADC0_SE6		
P2	—	PTC15		PTC15	RMII1_TXD1		ESAI_SDO5/ ESAI_SDI0	SCI5_RX	SAI2_TX_ DATA	ADC0_SE7		
R3	—	PTC16		PTC16	RMII1_TXD0		ESAI_SDO4/ ESAI_SDI1	SCI5_RTS	SAI2_RX_ SYNC	ADC1_SE6		
R4	—	PTC17		PTC17	RMII1_TXEN		ADC1_SE7	SCI5_CTS	SAI2_TX_ SYNC	USB1_SOF_ PULSE		
B10	—	DDR_A[15]			DDR_A15							
D9	—	DDR_A[14]			DDR_A14							
A10	—	DDR_A[13]			DDR_A13							
C10	—	DDR_A[12]			DDR_A12							
D10	—	DDR_A[11]			DDR_A11							
D7	—	DDR_A[10]			DDR_A10							
B9	—	DDR_A[9]			DDR_A9							
A11	—	DDR_A[8]			DDR_A8							
A7	—	DDR_A[7]			DDR_A7							
A9	—	DDR_A[6]			DDR_A6							
B6	—	DDR_A[5]			DDR_A5							
A6	—	DDR_A[4]			DDR_A4							
B7	—	DDR_A[3]			DDR_A3							
A8	—	DDR_A[2]			DDR_A2							
C11	—	DDR_A[1]			DDR_A1							
C7	—	DDR_A[0]			DDR_A0							
D8	—	DDR_BA[2]			DDR_BA2							
C9	—	DDR_BA[1]			DDR_BA1							
C8	—	DDR_BA[0]			DDR_BA0							
B4	—	DDR_CAS_b			DDR_CAS_b							
A5	—	DDR_CKE[0]			DDR_CKE0							

364 MAP BGA	176 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
A2	—	DDR_CLK[0]			DDR_CLK0							
B2	—	DDR_CLK_b[0]			DDR_CLK_b0							
C5	—	DDR_CS_b[0]			DDR_CS_b0							
D2	—	DDR_D[15]			DDR_D15							
H2	—	DDR_D[14]			DDR_D14							
C1	—	DDR_D[13]			DDR_D13							
G1	—	DDR_D[12]			DDR_D12							
E2	—	DDR_D[11]			DDR_D11							
H1	—	DDR_D[10]			DDR_D10							
D1	—	DDR_D[9]			DDR_D9							
J1	—	DDR_D[8]			DDR_D8							
G3	—	DDR_D[7]			DDR_D7							
C3	—	DDR_D[6]			DDR_D6							
J3	—	DDR_D[5]			DDR_D5							
F3	—	DDR_D[4]			DDR_D4							
G4	—	DDR_D[3]			DDR_D3							
D4	—	DDR_D[2]			DDR_D2							
H3	—	DDR_D[1]			DDR_D1							
F4	—	DDR_D[0]			DDR_D0							
G2	—	DDR_DQM[1]			DDR_DQM1							
J4	—	DDR_DQM[0]			DDR_DQM0							
E1	—	DDR_DQS[1]			DDR_DQS1							
D3	—	DDR_DQS[0]			DDR_DQS0							
F1	—	DDR_DQS_b[1]			DDR_DQS_b1							
E3	—	DDR_DQS_b[0]			DDR_DQS_b0							
A4	—	DDR_RAS_b			DDR_RAS_b							
C6	—	DDR_WE_b			DDR_WE_b							
C4	—	DDR_ODT[0]			DDR_ODT0							
B1	—	DDR_ODT[1]			DDR_ODT1							
G5	—	DDR_VREF			DDR_VREF							
A3	—	DDR_ZQ			DDR_ZQ							
D6	—	DDR_RESET			DDR_RESET							
J20	—	PTD31		PTD31	FB_AD31	NF_IO15		FTM3_CH0	SPI2_PCS1			
H20	—	PTD30		PTD30	FB_AD30	NF_IO14		FTM3_CH1	SPI2_PCS0			
H18	—	PTD29		PTD29	FB_AD29	NF_IO13		FTM3_CH2	SPI2_SIN			
H17	—	PTD28		PTD28	FB_AD28	NF_IO12	I2C2_SCL	FTM3_CH3	SPI2_SOUT			
H16	—	PTD27		PTD27	FB_AD27	NF_IO11	I2C2_SDA	FTM3_CH4	SPI2_SCK			

364 MAP BGA	176 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
G16	—	PTD26		PTD26	FB_AD26	NF_IO10		FTM3_CH5	SDHC1_WP			
G18	—	PTD25		PTD25	FB_AD25	NF_IO9		FTM3_CH6				
G19	—	PTD24		PTD24	FB_AD24	NF_IO8		FTM3_CH7				
G20	124	PTD23		PTD23/ MII0_ RXDATA[3]	FB_AD23	NF_IO7	FTM2CH0	ENET0_ 1588_TMR0	SDHC0_ DAT4	SCI2_TX	DCU1_R3	
F20	126	PTD22		PTD22/ MII0_ RXDATA[2]	FB_AD22	NF_IO6	FTM2CH1	ENET0_ 1588_TMR1	SDHC0_ DAT5	SCI2_RX	DCU1_R4	
F19	128	PTD21		PTD21/ MII0_CRS	FB_AD21	NF_IO5		ENET0_ 1588_TMR2	SDHC0_ DAT6	SCI2_RTS	DCU1_R5	
F17	129	PTD20		PTD20/ MII0_COL	FB_AD20	NF_IO4		ENET0_ 1588_TMR3	SDHC0_ DAT7	SCI2_CTS	DCU1_R0	
F16	130	PTD19		PTD19	FB_AD19	NF_IO3	ESAI_SCKR	I2C0_SCL	FTM2_QD_ PHA	MII0_ TXDATA[3]	DCU1_R1	
E18	131	PTD18		PTD18	FB_AD18	NF_IO2	ESAI_FSR	I2C0_SDA	FTM2_QD_ PHB	MII0_ TXDATA[2]	DCU1_G0	
E20	132	PTD17		PTD17	FB_AD17	NF_IO1	ESAI_HCKR	I2C1_SCL		MII0_TXERR	DCU1_G1	
D20	133	PTD16		PTD16	FB_AD16	NF_IO0	ESAI_HCKT	I2C1_SDA			DCU1_G2	
Y17	86	PTD0		PTD0	QSPI0_A_ SCK	SCI2_TX		FB_AD15	SPDIF_ EXTCLK			
Y18	87	PTD1		PTD1	QSPI0_A_ CS0	SCI2_RX		FB_AD14	SPDIF_IN1			
V18	88	PTD2		PTD2	QSPI0_A_ DATA3	SCI2_RTS	SPI1_PCS3	FB_AD13	SPDIF_OUT1			
Y19	89	PTD3		PTD3	QSPI0_A_ DATA2	SCI2_CTS	SPI1_PCS2	FB_AD12	SPDIF_ PLOCK			
W19	90	PTD4		PTD4	QSPI0_A_ DATA1		SPI1_PCS1	FB_AD11	SPDIF_ SRCLK			
W20	91	PTD5		PTD5	QSPI0_A_ DATA0		SPI1_PCS0	FB_AD10				
V20	92	PTD6		PTD6	QSPI0_A_ DQS		SPI1_SIN	FB_AD9				
V19	93	PTD7		PTD7	QSPI0_B_ SCK		SPI1_SOUT	FB_AD8				
U17	94	PTD8		PTD8	QSPI0_B_ CS0	FB_CLKOUT	SPI1_SCK	FB_AD7				
U18	97	PTD9		PTD9	QSPI0_B_ DATA3	SPI3_PCS1		FB_AD6		SAI1_TX_ SYNC	DCU1_B0	
U20	98	PTD10		PTD10	QSPI0_B_ DATA2	SPI3_PCS0		FB_AD5			DCU1_B1	
T20	99	PTD11		PTD11	QSPI0_B_ DATA1	SPI3_SIN		FB_AD4				
T19	100	PTD12		PTD12	QSPI0_B_ DATA0	SPI3_SOUT		FB_AD3				
T18	101	PTD13		PTD13	QSPI0_B_ DQS	SPI3_SCK		FB_AD2				

364 MAP BGA	176 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
A19	141	PTB23		PTB23	SAI0_TX_BCLK	SCI1_TX		FB_MUXED_ALE	FB_TS_b	SCI3_RTS	DCU1_G3	
A18	142	PTB24		PTB24	SAI0_RX_BCLK	SCI1_RX		FB_MUXED_TSIZ0	NF_WE_b	SCI3_CTS	DCU1_G4	
B17	149	PTB25		PTB25	SAI0_RX_DATA	SCI1_RTS		FB_CS1_b	NF_CE0_b		DCU1_G5	
A17	150	PTB26	RCON21	PTB26	SAI0_TX_DATA	SCI1_CTS	RCON21	FB_CS0_b	NF_CE1_b		DCU1_G6	
U8	57	PTB27	RCON22	PTB27	SAI0_RX_SYNC		RCON22	FB_OE_b	FB_MUXED_TBST_b	NF_RE_b	DCU1_G7	
A16	151	PTB28	RCON23	PTB28	SAI0_TX_SYNC		RCON23	FB_RW_b			DCU1_B6	
D16	153	PTC26	RCON24	PTC26	SAI1_TX_BCLK	SPI0_PCS5	RCON24	FB_TA_b	NF_RB_b		DCU1_B7	
E16	154	PTC27	RCON25	PTC27	SAI1_RX_BCLK	SPI0_PCS4	RCON25	FB_BE3_b	FB_CS3_b	NF_ALE	DCU1_B2	
E15	155	PTC28	RCON26	PTC28	SAI1_RX_DATA	SPI0_PCS3	RCON26	FB_BE2_b	FB_CS2_b	NF_CLE	DCU1_B3	
C16	152	PTC29	RCON27	PTC29	SAI1_TX_DATA	SPI0_PCS2	RCON27	FB_BE1_b	FB_MUXED_TSIZ1		DCU1_B4	
T8	58	PTC30	RCON28	PTC30	SAI1_RX_SYNC	SPI1_PCS2	RCON28	FB_MUXED_BE0_b	FB_TSIZ0	ADC0_SE5	DCU1_B5	
W5	42	PTC31	RCON29	PTC31	SAI1_TX_SYNC		RCON29			ADC1_SE5	DCU1_B6	
N16	103	PTE0	BOOTMOD1	PTE0	DCU0_HSYNC/DCU0_TCON1	BOOTMOD1		LCD0				
N18	104	PTE1	BOOTMOD0	PTE1	DCU0_VSYNC/DCU0_TCON2	BOOTMOD0		LCD1				
N19	105	PTE2		PTE2	DCU0_PCLK			LCD2				
Y15	77	PTE3		PTE3	DCU0_TAG/DCU0_TCON0			LCD3				
N20	106	PTE4		PTE4	DCU0_DE/DCU0_TCON3			LCD4				
T16	80	PTE5		PTE5	DCU0_R0			LCD5				
W16	81	PTE6		PTE6	DCU0_R1			LCD6				
M20	109	PTE7	RCON0	PTE7	DCU0_R2		RCON0	LCD7				
M19	110	PTE8	RCON1	PTE8	DCU0_R3		RCON1	LCD8				
M17	111	PTE9	RCON2	PTE9	DCU0_R4		RCON2	LCD9				
M16	112	PTE10	RCON3	PTE10	DCU0_R5		RCON3	LCD10				
L16	113	PTE11	RCON4	PTE11	DCU0_R6		RCON4	LCD11				
L17	114	PTE12	RCON5	PTE12	DCU0_R7	SPI1_PCS3	RCON5	LCD12			LPT_ALT0	

364 MAP BGA	176 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
Y16	78	PTE13		PTE13	DCU0_G0			LCD13				
W15	76	PTE14		PTE14	DCU0_G1			LCD14				
L18	115	PTE15	RCON6	PTE15	DCU0_G2		RCON6	LCD15				
L20	116	PTE16	RCON7	PTE16	DCU0_G3		RCON7	LCD16				
K20	117	PTE17	RCON8	PTE17	DCU0_G4		RCON8	LCD17				
K19	118	PTE18	RCON9	PTE18	DCU0_G5		RCON9	LCD18				
K18	119	PTE19	RCON10	PTE19	DCU0_G6		RCON10	LCD19	I2C0_SCL			
A12	170	PTE20	RCON11	PTE20	DCU0_G7		RCON11	LCD20	I2C0_SDA		EWM_in	
V16	79	PTE21		PTE21	DCU0_B0			LCD21				
W17	84	PTE22		PTE22	DCU0_B1			LCD22				
J17	122	PTE23	RCON12	PTE23	DCU0_B2		RCON12	LCD23				
D19	134	PTE24	RCON13	PTE24	DCU0_B3		RCON13	LCD24				
C19	135	PTE25	RCON14	PTE25	DCU0_B4		RCON14	LCD25				
C20	137	PTE26	RCON15	PTE26	DCU0_B5		RCON15	LCD26				
B20	138	PTE27	RCON16	PTE27	DCU0_B6		RCON16	LCD27	I2C1_SCL			
K16	120	PTE28	RCON17	PTE28	DCU0_B7		RCON17	LCD28	I2C1_SDA		EWM_out	
V15	75	PTA7		PTA7	VIU_PIX_ CLK							
T14	—	EXT_ TAMPER0			EXT_ TAMPER0							
U14	—	EXT_ TAMPER1			EXT_ TAMPER1							
T13	—	EXT_ TAMPER2/ EXT_WM0_ TAMPER_IN			EXT_ TAMPER2/ EXT_WM0_ TAMPER_IN							
U13	—	EXT_ TAMPER3/ EXT_WM0_ TAMPER_ OUT			EXT_ TAMPER3/ EXT_WM0_ TAMPER_ OUT							
U12	—	EXT_ TAMPER4/ EXT_WM1_ TAMPER_IN			EXT_ TAMPER4/ EXT_WM1_ TAMPER_IN							
U10	—	EXT_ TAMPER5/ EXT_WM1_ TAMPER_ OUT			EXT_ TAMPER5/ EXT_WM1_ TAMPER_ OUT							
G7	2	VDD			VDD							
J7	22	VDD			VDD							
L7	48	VDD			VDD							
H8	—	VDD			VDD							
K8	85	VDD			VDD							

364 MAP BGA	176 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
M8	102	VDD			VDD							
P8	125	VDD			VDD							
G9	136	VDD			VDD							
N9	174	VDD			VDD							
H10	—	VDD			VDD							
P10	—	VDD			VDD							
G11	—	VDD			VDD							
N11	—	VDD			VDD							
H12	—	VDD			VDD							
P12	—	VDD			VDD							
G13	—	VDD			VDD							
J13	—	VDD			VDD							
L13	—	VDD			VDD							
N13	—	VDD			VDD							
H14	—	VDD			VDD							
K14	—	VDD			VDD							
M14	—	VDD			VDD							
P14	—	VDD			VDD							
A1	1	VSS			VSS							
A20	13	VSS			VSS							
B3	20	VSS			VSS							
B5	25	VSS			VSS							
B8	45	VSS			VSS							
B11	—	VSS			VSS							
B13	—	VSS			VSS							
B16	—	VSS			VSS							
B19	—	VSS			VSS							
C2	—	VSS			VSS							
D17	—	VSS			VSS							
E5	—	VSS			VSS							
E8	—	VSS			VSS							
E11	—	VSS			VSS							
E14	—	VSS			VSS							
E19	—	VSS			VSS							
F2	—	VSS			VSS							
G17	—	VSS			VSS							
H4	—	VSS			VSS							
J2	—	VSS			VSS							
J18	—	VSS			VSS							
M2	—	VSS			VSS							

364 MAP BGA	176 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
M4	—	VSS			VSS							
M18	—	VSS			VSS							
R2	—	VSS			VSS							
R18	—	VSS			VSS							
U7	—	VSS			VSS							
U19	—	VSS			VSS							
V13	—	VSS			VSS							
W6	—	VSS			VSS							
V17	—	VSS			VSS							
Y1	—	VSS			VSS							
Y20	—	VSS			VSS							
H19	—	VSS			VSS							
L19	—	VSS			VSS							
P19	—	VSS			VSS							
J5	—	SDRAMC_ VDD2P5			SDRAMC_ VDD2P5							
E6	—	SDRAMC_ VDD2P5			SDRAMC_ VDD2P5							
E10	—	SDRAMC_ VDD2P5			SDRAMC_ VDD2P5							
E4	—	SDRAMC_ VDD1P5			SDRAMC_ VDD1P5							
D5	—	SDRAMC_ VDD1P5			SDRAMC_ VDD1P5							
F5	—	SDRAMC_ VDD1P5			SDRAMC_ VDD1P5							
H5	—	SDRAMC_ VDD1P5			SDRAMC_ VDD1P5							
K5	—	SDRAMC_ VDD1P5			SDRAMC_ VDD1P5							
E7	—	SDRAMC_ VDD1P5			SDRAMC_ VDD1P5							
E9	—	SDRAMC_ VDD1P5			SDRAMC_ VDD1P5							
D11	—	SDRAMC_ VDD1P5			SDRAMC_ VDD1P5							
K3	10	VDD33			VDD33							
N3	21	VDD33			VDD33							
V8	52	VDD33			VDD33							
C12	—	VDD33			VDD33							
C15	83	VDD33			VDD33							
U16	95	VDD33			VDD33							
K17	108	VDD33			VDD33							

364 MAP BGA	176 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
N17	127	VDD33			VDD33							
T17	140	VDD33			VDD33							
C18	146	VDD33			VDD33							
F18	158	VDD33			VDD33							
W18	168	VDD33			VDD33							
H7	—	VSS			VSS							
K7	74	VSS			VSS							
M7	82	VSS			VSS							
P7	96	VSS			VSS							
G8	107	VSS			VSS							
J8	—	VSS			VSS							
L8	139	VSS			VSS							
N8	—	VSS			VSS							
H9	157	VSS			VSS							
J9	175	VSS			VSS							
K9	176	VSS			VSS							
L9	—	VSS			VSS							
M9	—	VSS			VSS							
P9	—	VSS			VSS							
G10	—	VSS			VSS							
J10	—	VSS			VSS							
K10	—	VSS			VSS							
L10	—	VSS			VSS							
M10	—	VSS			VSS							
N10	—	VSS			VSS							
H11	—	VSS			VSS							
J11	—	VSS			VSS							
K11	—	VSS			VSS							
L11	—	VSS			VSS							
M11	—	VSS			VSS							
P11	—	VSS			VSS							
G12	—	VSS			VSS							
J12	—	VSS			VSS							
K12	—	VSS			VSS							
L12	—	VSS			VSS							
M12	—	VSS			VSS							
N12	—	VSS			VSS							
H13	—	VSS			VSS							
K13	—	VSS			VSS							
M13	—	VSS			VSS							

364 MAP BGA	176 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
P13	—	VSS			VSS							
G14	—	VSS			VSS							
J14	—	VSS			VSS							
L14	—	VSS			VSS							
N14	—	VSS			VSS							
N7	—	FA_VDD			FA_VDD							
V14	—	VBAT			VBAT							
—	FLG	VSS			VSS							

12.2 Pinout diagrams

NOTE

The 176 LQFP parts are not pin compatible between the F and R series families devices.

NOTE

If tamper detection is not required, the tamper pins must be tied to ground.

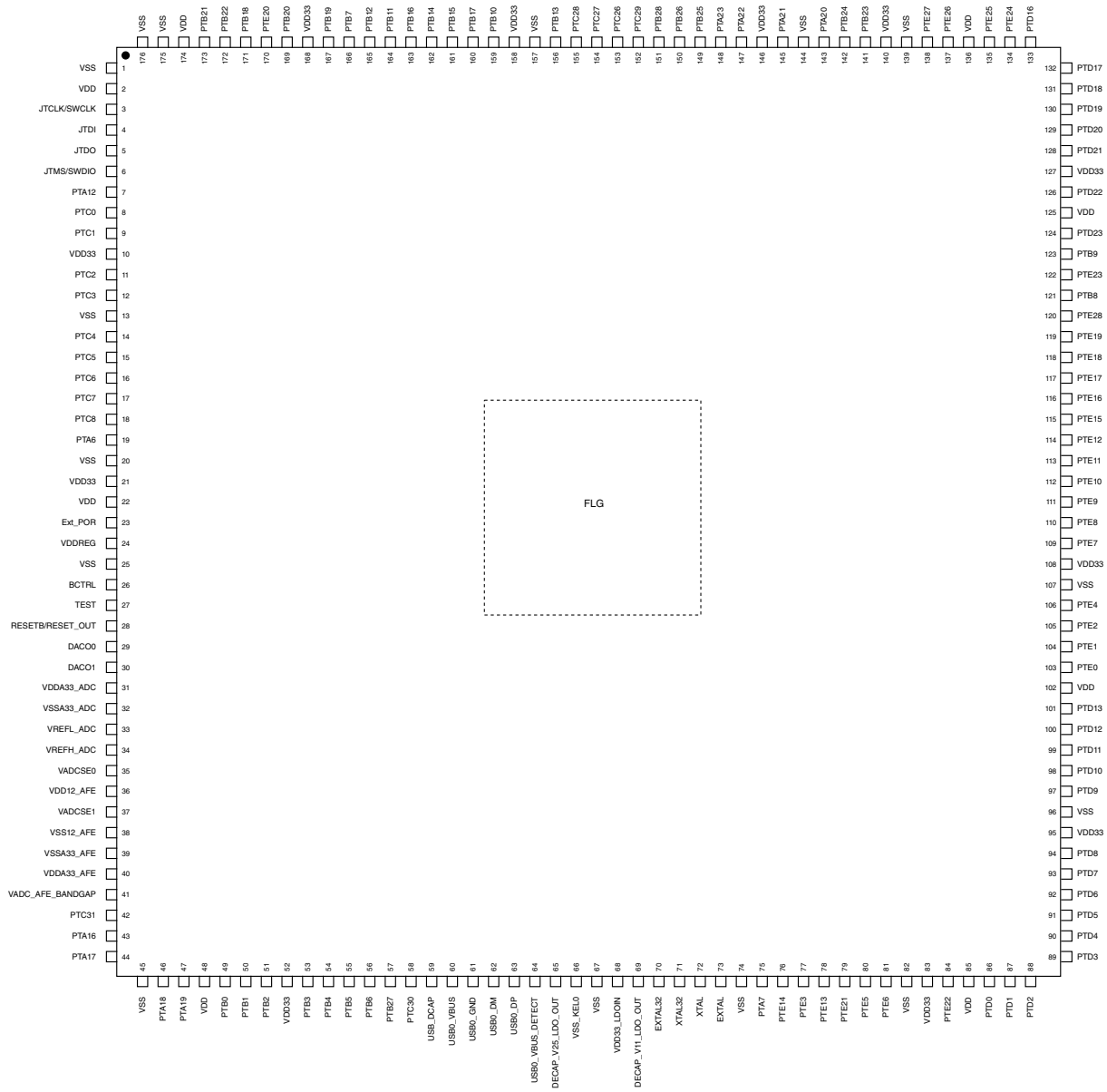
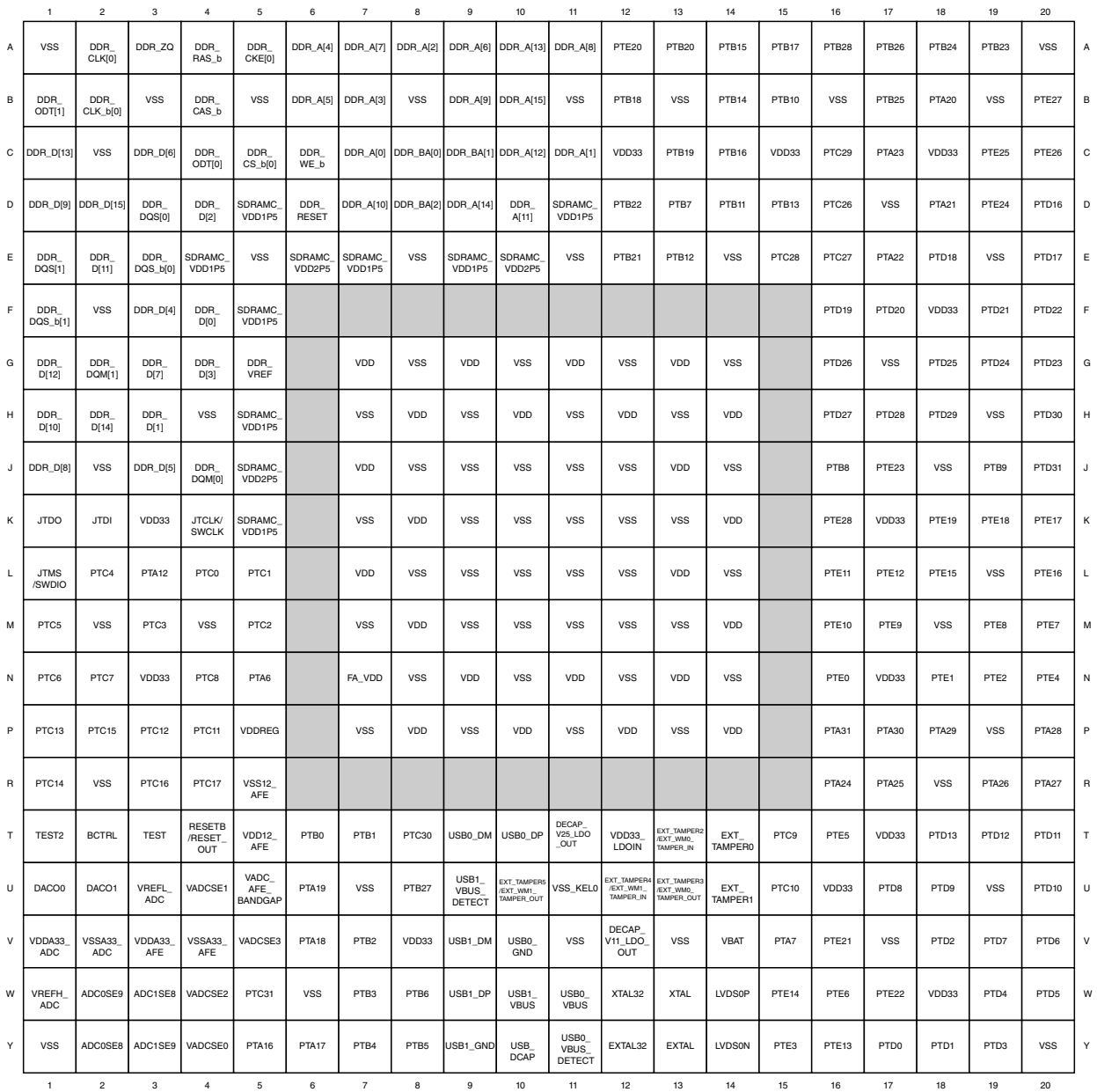


Figure 59. 176 LQFP Pinout Diagram



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
A	VSS	DDR_ CLK[0]	DDR_ZQ	DDR_ RAS_b	DDR_ CKE[0]	DDR_A[4]	DDR_A[7]	DDR_A[2]	DDR_A[6]	DDR_A[13]	DDR_A[8]	PTE20	PTB20	PTB15	PTB17	PTB28	PTB26	PTB24	PTB23	VSS	A
B	DDR_ ODT[1]	DDR_ CLK_b[0]	VSS	DDR_ CAS_b	VSS	DDR_A[5]	DDR_A[3]	VSS	DDR_A[9]	DDR_A[15]	VSS	PTB18	VSS	PTB14	PTB10	VSS	PTB25	PTA20	VSS	PTE27	B
C	DDR_D[13]	VSS	DDR_D[6]	DDR_ ODT[0]	DDR_ CS_b[0]	DDR_ WE_b	DDR_A[0]	DDR_BA[0]	DDR_BA[1]	DDR_A[12]	DDR_A[1]	VDD33	PTB19	PTB16	VDD33	PTC29	PTA23	VDD33	PTE25	PTE26	C
D	DDR_D[9]	DDR_D[15]	DDR_ DQS[0]	DDR_ D[2]	SDRAMC_ VDD1P5	DDR_ RESET	DDR_A[10]	DDR_BA[2]	DDR_A[14]	DDR_ A[11]	SDRAMC_ VDD1P5	PTB22	PTB7	PTB11	PTB13	PTC26	VSS	PTA21	PTE24	PTD16	D
E	DDR_ DQS[1]	DDR_ D[11]	DDR_ DQS_b[0]	SDRAMC_ VDD1P5	VSS	SDRAMC_ VDD2P5	SDRAMC_ VDD1P5	VSS	SDRAMC_ VDD1P5	SDRAMC_ VDD2P5	VSS	PTB21	PTB12	VSS	PTC28	PTC27	PTA22	PTD18	VSS	PTD17	E
F	DDR_ DQS_b[1]	VSS	DDR_D[4]	DDR_ D[0]	SDRAMC_ VDD1P5											PTD19	PTD20	VDD33	PTD21	PTD22	F
G	DDR_ D[12]	DDR_ DQM[1]	DDR_ D[7]	DDR_ D[3]	DDR_ VREF		VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS		PTD26	VSS	PTD25	PTD24	PTD23	G
H	DDR_ D[10]	DDR_ D[14]	DDR_ D[1]	VSS	SDRAMC_ VDD1P5		VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD		PTD27	PTD28	PTD29	VSS	PTD30	H
J	DDR_D[8]	VSS	DDR_D[5]	DDR_ DQM[0]	SDRAMC_ VDD2P5		VDD	VSS	VSS	VSS	VSS	VSS	VDD	VSS		PTB8	PTE23	VSS	PTB9	PTD31	J
K	JTDO	JTDI	VDD33	JTCLK/ SWCLK	SDRAMC_ VDD1P5		VSS	VDD	VSS	VSS	VSS	VSS	VSS	VDD		PTE28	VDD33	PTE19	PTE18	PTE17	K
L	JTMS /SWDIO	PTC4	PTA12	PTC0	PTC1		VDD	VSS	VSS	VSS	VSS	VSS	VDD	VSS		PTE11	PTE12	PTE15	VSS	PTE16	L
M	PTC5	VSS	PTC3	VSS	PTC2		VSS	VDD	VSS	VSS	VSS	VSS	VSS	VDD		PTE10	PTE9	VSS	PTE8	PTE7	M
N	PTC6	PTC7	VDD33	PTC8	PTA6		FA_VDD	VSS	VDD	VSS	VDD	VSS	VDD	VSS		PTE0	VDD33	PTE1	PTE2	PTE4	N
P	PTC13	PTC15	PTC12	PTC11	VDDREG		VSS	VDD	VSS	VDD	VSS	VDD	VSS	VDD		PTA31	PTA30	PTA29	VSS	PTA28	P
R	PTC14	VSS	PTC16	PTC17	VSS12_ AFE											PTA24	PTA25	VSS	PTA26	PTA27	R
T	TEST2	BCTRL	TEST	RESETB /RESET_ OUT	VDD12_ AFE	PTB0	PTB1	PTC30	USB0_DM	USB0_DP	DECAP_ V25_LDO _OUT	VDD33_ LDOIN	EXT_TAMPER2 /EXT_WM0_ TAMPER_IN	EXT_ TAMPER0	PTC9	PTE5	VDD33	PTD13	PTD12	PTD11	T
U	DACO0	DACO1	VREFL_ ADC	VADCSE1	VADC_ AFE_ BANDGAP	PTA19	VSS	PTB27	USB1_ VBUS_ DETECT	EXT_TAMPER5 /EXT_WM1_ TAMPER_OUT	VSS_KEL0	EXT_TAMPER4 /EXT_WM1_ TAMPER_IN	EXT_TAMPER3 /EXT_WM0_ TAMPER_OUT	EXT_ TAMPER1	PTC10	VDD33	PTD8	PTD9	VSS	PTD10	U
V	VDDA33_ ADC	VSSA33_ ADC	VDDA33_ AFE	VSSA33_ AFE	VADCSE3	PTA18	PTB2	VDD33	USB1_DM	USB0_ GND	VSS	DECAP_ V11_LDO_ OUT	VSS	VBAT	PTA7	PTE21	VSS	PTD2	PTD7	PTD6	V
W	VREFH_ ADC	ADC0SE9	ADC1SE8	VADCSE2	PTC31	VSS	PTB3	PTB6	USB1_DP	USB1_ VBUS	USB0_ VBUS	XTAL32	XTAL	LVDS0P	PTE14	PTE6	PTE22	VDD33	PTD4	PTD5	W
Y	VSS	ADC0SE8	ADC1SE9	VADCSE0	PTA16	PTA17	PTB4	PTB5	USB1_GND	USB_ DCAP	USB0_ VBUS_ DETECT	EXTAL32	EXTAL	LVDS0N	PTE3	PTE13	PTD0	PTD1	PTD3	VSS	Y
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	

Figure 60. 364-pin BGA package ballmap

12.2.1 GPIO Mapping

Table 78. RGPIO versus Pins

RGPIO	In GPIO module	Corresponding Pin on the chip	IOMUX register name	IOMUX register address
RGPIO[0]	PORT0[0]	PTA6	IOMUXC_PTA6	40048000

Table continues on the next page...

Table 78. RGPIO versus Pins (continued)

RGPIO	In GPIO module	Corresponding Pin on the chip	IOMUX register name	IOMUX register address
RGPIO[1]	PORT0[1]	PTA8	IOMUXC_PTA8	40048004
RGPIO[2]	PORT0[2]	PTA9	IOMUXC_PTA9	40048008
RGPIO[3]	PORT0[3]	PTA10	IOMUXC_PTA10	4004800C
RGPIO[4]	PORT0[4]	PTA11	IOMUXC_PTA11	40048010
RGPIO[5]	PORT0[5]	PTA12	IOMUXC_PTA12	40048014
RGPIO[6]	PORT0[6]	PTA16	IOMUXC_PTA16	40048018
RGPIO[7]	PORT0[7]	PTA17	IOMUXC_PTA17	4004801C
RGPIO[8]	PORT0[8]	PTA18	IOMUXC_PTA18	40048020
RGPIO[9]	PORT0[9]	PTA19	IOMUXC_PTA19	40048024
RGPIO[10]	PORT0[10]	PTA20	IOMUXC_PTA20	40048028
RGPIO[11]	PORT0[11]	PTA21	IOMUXC_PTA21	4004802C
RGPIO[12]	PORT0[12]	PTA22	IOMUXC_PTA22	40048030
RGPIO[13]	PORT0[13]	PTA23	IOMUXC_PTA23	40048034
RGPIO[14]	PORT0[14]	PTA24	IOMUXC_PTA24	40048038
RGPIO[15]	PORT0[15]	PTA25	IOMUXC_PTA25	4004803C
RGPIO[16]	PORT0[16]	PTA26	IOMUXC_PTA26	40048040
RGPIO[17]	PORT0[17]	PTA27	IOMUXC_PTA27	40048044
RGPIO[18]	PORT0[18]	PTA28	IOMUXC_PTA28	40048048
RGPIO[19]	PORT0[19]	PTA29	IOMUXC_PTA29	4004804C
RGPIO[20]	PORT0[20]	PTA30	IOMUXC_PTA30	40048050
RGPIO[21]	PORT0[21]	PTA31	IOMUXC_PTA31	40048054
RGPIO[22]	PORT0[22]	PTB0	IOMUXC_PTB0	40048058
RGPIO[23]	PORT0[23]	PTB1	IOMUXC_PTB1	4004805C
RGPIO[24]	PORT0[24]	PTB2	IOMUXC_PTB2	40048060
RGPIO[25]	PORT0[25]	PTB3	IOMUXC_PTB3	40048064
RGPIO[26]	PORT0[26]	PTB4	IOMUXC_PTB4	40048068
RGPIO[27]	PORT0[27]	PTB5	IOMUXC_PTB5	4004806C
RGPIO[28]	PORT0[28]	PTB6	IOMUXC_PTB6	40048070
RGPIO[29]	PORT0[29]	PTB7	IOMUXC_PTB7	40048074
RGPIO[30]	PORT0[30]	PTB8	IOMUXC_PTB8	40048078
RGPIO[31]	PORT0[31]	PTB9	IOMUXC_PTB9	4004807C
RGPIO[32]	PORT1[0]	PTB10	IOMUXC_PTB10	40048080
RGPIO[33]	PORT1[1]	PTB11	IOMUXC_PTB11	40048084
RGPIO[34]	PORT1[2]	PTB12	IOMUXC_PTB12	40048088
RGPIO[35]	PORT1[3]	PTB13	IOMUXC_PTB13	4004808C
RGPIO[36]	PORT1[4]	PTB14	IOMUXC_PTB14	40048090
RGPIO[37]	PORT1[5]	PTB15	IOMUXC_PTB15	40048094
RGPIO[38]	PORT1[6]	PTB16	IOMUXC_PTB16	40048098
RGPIO[39]	PORT1[7]	PTB17	IOMUXC_PTB17	4004809C

Table continues on the next page...

Table 78. RGPIO versus Pins (continued)

RGPIO	In GPIO module	Corresponding Pin on the chip	IOMUX register name	IOMUX register address
RGPIO[40]	PORT1[8]	PTB18	IOMUXC_PTB18	400480A0
RGPIO[41]	PORT1[9]	PTB19	IOMUXC_PTB19	400480A4
RGPIO[42]	PORT1[10]	PTB20	IOMUXC_PTB20	400480A8
RGPIO[43]	PORT1[11]	PTB21	IOMUXC_PTB21	400480AC
RGPIO[44]	PORT1[12]	PTB22	IOMUXC_PTB22	400480B0
RGPIO[45]	PORT1[13]	PTC0	IOMUXC_PTC0	400480B4
RGPIO[46]	PORT1[14]	PTC1	IOMUXC_PTC1	400480B8
RGPIO[47]	PORT1[15]	PTC2	IOMUXC_PTC2	400480BC
RGPIO[48]	PORT1[16]	PTC3	IOMUXC_PTC3	400480C0
RGPIO[49]	PORT1[17]	PTC4	IOMUXC_PTC4	400480C4
RGPIO[50]	PORT1[18]	PTC5	IOMUXC_PTC5	400480C8
RGPIO[51]	PORT1[19]	PTC6	IOMUXC_PTC6	400480CC
RGPIO[52]	PORT1[20]	PTC7	IOMUXC_PTC7	400480D0
RGPIO[53]	PORT1[21]	PTC8	IOMUXC_PTC8	400480D4
RGPIO[54]	PORT1[22]	PTC9	IOMUXC_PTC9	400480D8
RGPIO[55]	PORT1[23]	PTC10	IOMUXC_PTC10	400480DC
RGPIO[56]	PORT1[24]	PTC11	IOMUXC_PTC11	400480E0
RGPIO[57]	PORT1[25]	PTC12	IOMUXC_PTC12	400480E4
RGPIO[58]	PORT1[26]	PTC13	IOMUXC_PTC13	400480E8
RGPIO[59]	PORT1[27]	PTC14	IOMUXC_PTC14	400480EC
RGPIO[60]	PORT1[28]	PTC15	IOMUXC_PTC15	400480F0
RGPIO[61]	PORT1[29]	PTC16	IOMUXC_PTC16	400480F4
RGPIO[62]	PORT1[30]	PTC17	IOMUXC_PTC17	400480F8
RGPIO[63]	PORT1[31]	PTD31	IOMUXC_PTD31	400480FC
RGPIO[64]	PORT2[0]	PTD30	IOMUXC_PTD30	40048100
RGPIO[65]	PORT2[1]	PTD29	IOMUXC_PTD29	40048104
RGPIO[66]	PORT2[2]	PTD28	IOMUXC_PTD28	40048108
RGPIO[67]	PORT2[3]	PTD27	IOMUXC_PTD27	4004810C
RGPIO[68]	PORT2[4]	PTD26	IOMUXC_PTD26	40048110
RGPIO[69]	PORT2[5]	PTD25	IOMUXC_PTD25	40048114
RGPIO[70]	PORT2[6]	PTD24	IOMUXC_PTD24	40048118
RGPIO[71]	PORT2[7]	PTD23	IOMUXC_PTD23	4004811C
RGPIO[72]	PORT2[8]	PTD22	IOMUXC_PTD22	40048120
RGPIO[73]	PORT2[9]	PTD21	IOMUXC_PTD21	40048124
RGPIO[74]	PORT2[10]	PTD20	IOMUXC_PTD20	40048128
RGPIO[75]	PORT2[11]	PTD19	IOMUXC_PTD19	4004812C
RGPIO[76]	PORT2[12]	PTD18	IOMUXC_PTD18	40048130
RGPIO[77]	PORT2[13]	PTD17	IOMUXC_PTD17	40048134
RGPIO[78]	PORT2[14]	PTD16	IOMUXC_PTD16	40048138

Table continues on the next page...

Table 78. RGPIO versus Pins (continued)

RGPIO	In GPIO module	Corresponding Pin on the chip	IOMUX register name	IOMUX register address
RGPIO[79]	PORT2[15]	PTD0	IOMUXC_PTD0	4004813C
RGPIO[80]	PORT2[16]	PTD1	IOMUXC_PTD1	40048140
RGPIO[81]	PORT2[17]	PTD2	IOMUXC_PTD2	40048144
RGPIO[82]	PORT2[18]	PTD3	IOMUXC_PTD3	40048148
RGPIO[83]	PORT2[19]	PTD4	IOMUXC_PTD4	4004814C
RGPIO[84]	PORT2[20]	PTD5	IOMUXC_PTD5	40048150
RGPIO[85]	PORT2[21]	PTD6	IOMUXC_PTD6	40048154
RGPIO[86]	PORT2[22]	PTD7	IOMUXC_PTD7	40048158
RGPIO[87]	PORT2[23]	PTD8	IOMUXC_PTD8	4004815C
RGPIO[88]	PORT2[24]	PTD9	IOMUXC_PTD9	40048160
RGPIO[89]	PORT2[25]	PTD10	IOMUXC_PTD10	40048164
RGPIO[90]	PORT2[26]	PTD11	IOMUXC_PTD11	40048168
RGPIO[91]	PORT2[27]	PTD12	IOMUXC_PTD12	4004816C
RGPIO[92]	PORT2[28]	PTD13	IOMUXC_PTD13	40048170
RGPIO[93]	PORT2[29]	PTB23	IOMUXC_PTB23	40048174
RGPIO[94]	PORT2[30]	PTB24	IOMUXC_PTB24	40048178
RGPIO[95]	PORT2[31]	PTB25	IOMUXC_PTB25	4004817C
RGPIO[96]	PORT3[0]	PTB26	IOMUXC_PTB26	40048180
RGPIO[97]	PORT3[1]	PTB27	IOMUXC_PTB27	40048184
RGPIO[98]	PORT3[2]	PTB28	IOMUXC_PTB28	40048188
RGPIO[99]	PORT3[3]	PTC26	IOMUXC_PTC26	4004818C
RGPIO[100]	PORT3[4]	PTC27	IOMUXC_PTC27	40048190
RGPIO[101]	PORT3[5]	PTC28	IOMUXC_PTC28	40048194
RGPIO[102]	PORT3[6]	PTC29	IOMUXC_PTC29	40048198
RGPIO[103]	PORT3[7]	PTC30	IOMUXC_PTC30	4004819C
RGPIO[104]	PORT3[8]	PTC31	IOMUXC_PTC31	400481A0
RGPIO[105]	PORT3[9]	PTE0	IOMUXC_PTE0	400481A4
RGPIO[106]	PORT3[10]	PTE1	IOMUXC_PTE1	400481A8
RGPIO[107]	PORT3[11]	PTE2	IOMUXC_PTE2	400481AC
RGPIO[108]	PORT3[12]	PTE3	IOMUXC_PTE3	400481B0
RGPIO[109]	PORT3[13]	PTE4	IOMUXC_PTE4	400481B4
RGPIO[110]	PORT3[14]	PTE5	IOMUXC_PTE5	400481B8
RGPIO[111]	PORT3[15]	PTE6	IOMUXC_PTE6	400481BC
RGPIO[112]	PORT3[16]	PTE7	IOMUXC_PTE7	400481C0
RGPIO[113]	PORT3[17]	PTE8	IOMUXC_PTE8	400481C4
RGPIO[114]	PORT3[18]	PTE9	IOMUXC_PTE9	400481C8
RGPIO[115]	PORT3[19]	PTE10	IOMUXC_PTE10	400481CC
RGPIO[116]	PORT3[20]	PTE11	IOMUXC_PTE11	400481D0
RGPIO[117]	PORT3[21]	PTE12	IOMUXC_PTE12	400481D4

Table continues on the next page...

Table 78. RGPIO versus Pins (continued)

RGPIO	In GPIO module	Corresponding Pin on the chip	IOMUX register name	IOMUX register address
RGPIO[118]	PORT3[22]	PTE13	IOMUXC_PTE13	400481D8
RGPIO[119]	PORT3[23]	PTE14	IOMUXC_PTE14	400481DC
RGPIO[120]	PORT3[24]	PTE15	IOMUXC_PTE15	400481E0
RGPIO[121]	PORT3[25]	PTE16	IOMUXC_PTE16	400481E4
RGPIO[122]	PORT3[26]	PTE17	IOMUXC_PTE17	400481E8
RGPIO[123]	PORT3[27]	PTE18	IOMUXC_PTE18	400481EC
RGPIO[124]	PORT3[28]	PTE19	IOMUXC_PTE19	400481F0
RGPIO[125]	PORT3[29]	PTE20	IOMUXC_PTE20	400481F4
RGPIO[126]	PORT3[30]	PTE21	IOMUXC_PTE21	400481F8
RGPIO[127]	PORT3[31]	PTE22	IOMUXC_PTE22	400481FC
RGPIO[128]	PORT4[0]	PTE23	IOMUXC_PTE23	40048200
RGPIO[129]	PORT4[1]	PTE24	IOMUXC_PTE24	40048204
RGPIO[130]	PORT4[2]	PTE25	IOMUXC_PTE25	40048208
RGPIO[131]	PORT4[3]	PTE26	IOMUXC_PTE26	4004820C
RGPIO[132]	PORT4[4]	PTE27	IOMUXC_PTE27	40048210
RGPIO[133]	PORT4[5]	PTE28	IOMUXC_PTE28	40048214
RGPIO[134]	PORT4[6]	PTA7	IOMUXC_PTA7	40048218

12.2.2 Special Signal

Table 79. Special Signal Considerations

Special Signal	Comments
DDR_VREF	When using DDR_VREF with DDR I/O, the nominal reference voltage must be half of the SDRAMC_VDD1P5 supply. The user must tie DDR_VREF to a precision external resistor divider. Shunt each resistor with a closely-mounted 0.1 µF capacitor.
DDR_ZQ	DRAM calibration resistor 240 Ω 1% used as reference during DRAM output buffer driver calibration should be connected between this pad and GND
DECAP_V25_LDO_OUT	DCAP_V25_LDO_OUT can be tied to SDRAMC_VDD2P5 to provide the predriver supply for the DDR I/O segment. SDRAMC_VDD1P5 requires an external regulated supply. If SDRAMC_VDD2P5 uses an external 2.5V supply, do NOT tie it to DCAP_V25_LDO_OUT.
EXT_POR, TEST	Factory use only, tie to ground..
EXT_TAMPER0, EXT_TAMPER1, EXT_TAMPER2, EXT_TAMPER3, EXT_TAMPER4, EXT_TAMPER5	Security related tamper detection inputs, if not in use they must be tied to ground.
FA_VDD	Factory use only, tie to VDD.

Table continues on the next page...

Table 79. Special Signal Considerations (continued)

Special Signal	Comments
JTCLK, JTDI, JTDO, JTMS	For JTAG the use of external resistors is unnecessary. However, if external resistors are used, the user must ensure that the on-chip pull-up/down configuration is matched. For example, do not use an external pull down on an input that has on-chip pull-up. JTDO is configured with a keeper circuit such that the floating condition is eliminated if an external pull resistor is not present. An external pull resistor on JTDO is detrimental and should be avoided.
LVDS0N, LVDS0P	Not recommended for application use, intended for clock observation purposes during debug only.
RESETB/RESET_OUT	Active low input used to generate a system wide reset (except the SRTC). A glitch filter is include to help prevent unexpected resets, a minimum pulse width of 125 nsecs is required to guarantee a reset is detected.
XTAL, EXTAL	A 24.0 MHz fundamental mode crystal should be connected between XTAL and EXTAL. The crystal must be rated for a drive level of 250 µW or higher. An ESR (equivalent series resistance) of 80 Ω or less is recommended. This clock is used as a reference for USB, so there are strict frequency tolerance and jitter requirements. The crystal can be eliminated if an external 24 MHz oscillator is available in the system. In this case, XTAL must be directly driven by the external oscillator and EXTAL floated. The XTAL signal level must swing from ~0.8 x DECAP_V11_ LDO_OUT to ~0.2 V.
XTAL32, EXTAL32	If the user wishes to configure XTAL32 and EXTAL32 as an RTC oscillator, a 32.768 kHz crystal, (≤50 kΩ ESR, 10 pF load) should be connected between XTAL32 and EXTAL32. Keep in mind the capacitors implemented on either side of the crystal are about twice the crystal load capacitor. To hit the exact oscillation frequency, the board capacitors need to be reduced to account for board and chip parasitics. The integrated oscillation amplifier is self biasing, but relatively weak. Care must be taken to limit parasitic leakage from XTAL32 and EXTAL32 to either power or ground (>100 MΩ). This will debias the amplifier and cause a reduction of startup margin. Typically XTAL32 and EXTAL32 should bias to approximately 0.5 V. If it is desired to feed an external low frequency clock into XTAL32 the EXTAL32 pin should be left floating or driven with a complimentary signal. The logic level of this forcing clock should not exceed DECAP_V11_ LDO_OUT level and the frequency should be <100 kHz under typical conditions. In the case where the SIRC is used, it is recommended to connect XTAL32 to ground and leave EXTAL32 floating.

13 Power Supply Pins

13.1 Power Supply Pins

Table 80. Power Supply Pins

Supply Rail Name	364 MAP BGA	176 LQFP (R-series ONLY)	Comment
DECAP_V11_ LDO_OUT	V12	69	On-chip 1.1V LDO output
DECAP_V25_ LDO_OUT	T11	65	On-chip 2.5V LDO output (Intended to supply DRAM IO when required)
FA_VDD	N7	—	Factory Use Only (Connect to VDD, internally bonded in LQFP)
SDRAMC_ VDD1P5	D5, D11, E4, E7, E9, F5, H5, K5	DRAM not supported in LQFP	1.5V DDR3 DRAM Supply (1.2V for LPDDR2)
SDRAMC_ VDD2P5	E6, E10, J5	DRAM not supported in LQFP	2.5V DRAM Supply
USB_DCAP	Y10	59	On-chip 3V LDO output (Intended to be fed by external USB VBUS supply)
USB0_GND	V10	61	
USB1_GND	Y9	USB1 not supported in LQFP	
VADC_AFE_ BANDGAP	U5	41	Video ADC Bandgap Output
VBAT	V14	VBAT not supported in LQFP	On-chip SNVS regulator battery back-up supply option
VDD	G7, G9, G11, G13, H8, H10, H12, H14, J7, J13, K8, K14, L7, L13, M8, M14, N9, N11, N13, P8, P10, P12, P14	2, 22, 48, 85, 102, 125, 136, 174	1.2V Core Supply (Internally Regulated)
VDD33	C12, C15, C18, F18, K3, K17, N3, N17, T17, U16, V8, W18	10, 21, 52, 83, 95, 108, 127, 140, 146, 158, 168	3.3V IO Supply
VDDA33_ADC	V1	31	3.3V Analog To Digital convertor supply
VDD12_AFE	T5	36	1.2V Analog Front End supply for Video ADC
VDDA33_AFE	V3	40	3.3V Analog Front End supply for Video ADC
VDD33_ LDOIN	T12	68	On-chip 2.5V LDO, 1.1V LDO and SNVS regulators input supply
VDDREG	P5	24	On-chip HPREG, LPREG, WBREG and ULPREG regulators input supply
VREFH_ADC	W1	34	ATD High Voltage Reference
VREFL_ADC	U3	33	ATD Low Voltage Reference

Table continues on the next page...

Table 80. Power Supply Pins (continued)

Supply Rail Name	364 MAP BGA	176 LQFP (R-series ONLY)	Comment
VSS	A1, A20, B3, B5, B8, B11, B13, B16, B19, C2, D17, E5, E8, E11, E14, E19, F2, G8, G10, G12, G14, G17, H4, H7, H9, H11, H13, H19, J2, J8, J9, J10, J11, J12, J14, J18, K7, K9, K10, K11, K12, K13, L8, L9, L10, L11, L12, L14, L19, M2, M4, M7, M9, M10, M11, M12, M13, M18, N8, N10, N12, N14, P7, P9, P11, P13, P19, R2, R18, U7, U19, V11, V13, V17, W6, Y1, Y20	1, 13, 20, 25, 45, 67, 74, 82, 96, 107, 139, 144, 157, 175, 176, FLG	Ground. Connect "Flag pad (FLG)" to the internal GND plane with numerous vias—for both electrical and thermal purposes.
VSSA33_ADC	V2	32	ATD Ground
VSS12_AFE	R5	38	Video ADC Ground
VSSA33_AFE	V4	39	Video ADC Ground
VSS_KEL0	U11	66	Ground (VSS and VSS_KEL0 are NOT connected internally)

14 Functional Assignment Pins

14.1 Functional Assignment Pins

Table 81. Functional Assignment Pins

Signal Name	364 MAP BGA	176 LQFP (R-series ONLY)	Power Group	Pad Type	Default Mode (Reset)	Default Function	Input/ Output	Value
ADC0SE8	Y2	—	VDDA33_ADC	Analog	—	ADC0SE8	—	—
ADC0SE9	W2	—	VDDA33_ADC	Analog	—	ADC0SE9	—	—
ADC1SE8	W3	—	VDDA33_ADC	Analog	—	ADC1SE8	—	—
ADC1SE9	Y3	—	VDDA33_ADC	Analog	—	ADC1SE9	—	—
BCTRL	T2	26	VDDREG	Analog	—	BCTRL	—	—
DACO0	U1	29	VDDA33_ADC	Analog	—	DACO0	—	—
DACO1	U2	30	VDDA33_ADC	Analog	—	DACO1	—	—
DDR_A[0]	C7	—	SDRAMC_VDD2P5	DDR	—	DDR_A[0]	—	—

Table continues on the next page...

Table 81. Functional Assignment Pins (continued)

Signal Name	364 MAP BGA	176 LQFP (R-series ONLY)	Power Group	Pad Type	Default Mode (Reset)	Default Function	Input/ Output	Value
DDR_A[1]	C11	—	SDRAMC_ VDD2P5	DDR	—	DDR_A[1]	—	—
DDR_A[2]	A8	—	SDRAMC_ VDD2P5	DDR	—	DDR_A[2]	—	—
DDR_A[3]	B7	—	SDRAMC_ VDD2P5	DDR	—	DDR_A[3]	—	—
DDR_A[4]	A6	—	SDRAMC_ VDD2P5	DDR	—	DDR_A[4]	—	—
DDR_A[5]	B6	—	SDRAMC_ VDD2P5	DDR	—	DDR_A[5]	—	—
DDR_A[6]	A9	—	SDRAMC_ VDD2P5	DDR	—	DDR_A[6]	—	—
DDR_A[7]	A7	—	SDRAMC_ VDD2P5	DDR	—	DDR_A[7]	—	—
DDR_A[8]	A11	—	SDRAMC_ VDD2P5	DDR	—	DDR_A[8]	—	—
DDR_A[9]	B9	—	SDRAMC_ VDD2P5	DDR	—	DDR_A[9]	—	—
DDR_A[10]	D7	—	SDRAMC_ VDD2P5	DDR	—	DDR_A[10]	—	—
DDR_A[11]	D10	—	SDRAMC_ VDD2P5	DDR	—	DDR_A[11]	—	—
DDR_A[12]	C10	—	SDRAMC_ VDD2P5	DDR	—	DDR_A[12]	—	—
DDR_A[13]	A10	—	SDRAMC_ VDD2P5	DDR	—	DDR_A[13]	—	—
DDR_A[14]	D9	—	SDRAMC_ VDD2P5	DDR	—	DDR_A[14]	—	—
DDR_A[15]	B10	—	SDRAMC_ VDD2P5	DDR	—	DDR_A[15]	—	—
DDR_BA[0]	C8	—	SDRAMC_ VDD2P5	DDR	—	DDR_BA[0]	—	—
DDR_BA[1]	C9	—	SDRAMC_ VDD2P5	DDR	—	DDR_BA[1]	—	—
DDR_BA[2]	D8	—	SDRAMC_ VDD2P5	DDR	—	DDR_BA[2]	—	—
DDR_CAS_ b	B4	—	SDRAMC_ VDD2P5	DDR	—	DDR_CAS_ b	—	—
DDR_CKE[0]	A5	—	SDRAMC_ VDD2P5	DDR	—	DDR_CKE[0]	—	—
DDR_CLK[0]	A2	—	SDRAMC_ VDD2P5	DDR	—	DDR_CLK[0]	—	—

Table continues on the next page...

Table 81. Functional Assignment Pins (continued)

Signal Name	364 MAP BGA	176 LQFP (R-series ONLY)	Power Group	Pad Type	Default Mode (Reset)	Default Function	Input/ Output	Value
DDR_CLK_b[0]	B2	—	SDRAMC_VDD2P5	DDR	—	DDR_CLK_b[0]	—	—
DDR_CS_b[0]	C5	—	SDRAMC_VDD2P5	DDR	—	DDR_CS_b[0]	—	—
DDR_D[0]	F4	—	SDRAMC_VDD2P5	DDR	—	DDR_D[0]	—	—
DDR_D[1]	H3	—	SDRAMC_VDD2P5	DDR	—	DDR_D[1]	—	—
DDR_D[2]	D4	—	SDRAMC_VDD2P5	DDR	—	DDR_D[2]	—	—
DDR_D[3]	G4	—	SDRAMC_VDD2P5	DDR	—	DDR_D[3]	—	—
DDR_D[4]	F3	—	SDRAMC_VDD2P5	DDR	—	DDR_D[4]	—	—
DDR_D[5]	J3	—	SDRAMC_VDD2P5	DDR	—	DDR_D[5]	—	—
DDR_D[6]	C3	—	SDRAMC_VDD2P5	DDR	—	DDR_D[6]	—	—
DDR_D[7]	G3	—	SDRAMC_VDD2P5	DDR	—	DDR_D[7]	—	—
DDR_D[8]	J1	—	SDRAMC_VDD2P5	DDR	—	DDR_D[8]	—	—
DDR_D[9]	D1	—	SDRAMC_VDD2P5	DDR	—	DDR_D[9]	—	—
DDR_D[10]	H1	—	SDRAMC_VDD2P5	DDR	—	DDR_D[10]	—	—
DDR_D[11]	E2	—	SDRAMC_VDD2P5	DDR	—	DDR_D[11]	—	—
DDR_D[12]	G1	—	SDRAMC_VDD2P5	DDR	—	DDR_D[12]	—	—
DDR_D[13]	C1	—	SDRAMC_VDD2P5	DDR	—	DDR_D[13]	—	—
DDR_D[14]	H2	—	SDRAMC_VDD2P5	DDR	—	DDR_D[14]	—	—
DDR_D[15]	D2	—	SDRAMC_VDD2P5	DDR	—	DDR_D[15]	—	—
DDR_DQM[0]	J4	—	SDRAMC_VDD2P5	DDR	—	DDR_DQM[0]	—	—
DDR_DQM[1]	G2	—	SDRAMC_VDD2P5	DDR	—	DDR_DQM[1]	—	—
DDR_DQS[0]	D3	—	SDRAMC_VDD2P5	DDR	—	DDR_DQS[0]	—	—

Table continues on the next page...

Table 81. Functional Assignment Pins (continued)

Signal Name	364 MAP BGA	176 LQFP (R-series ONLY)	Power Group	Pad Type	Default Mode (Reset)	Default Function	Input/ Output	Value
DDR_DQS_b[0]	E3	—	SDRAMC_VDD2P5	DDR	—	DDR_DQS_b[0]	—	—
DDR_DQS[1]	E1	—	SDRAMC_VDD2P5	DDR	—	DDR_DQS[1]	—	—
DDR_DQS_b[1]	F1	—	SDRAMC_VDD2P5	DDR	—	DDR_DQS_b[1]	—	—
DDR_ODT[0]	C4	—	SDRAMC_VDD2P5	DDR	—	DDR_ODT[0]	—	—
DDR_ODT[1]	B1	—	SDRAMC_VDD2P5	DDR	—	DDR_ODT[1]	—	—
DDR_RAS_b	A4	—	SDRAMC_VDD2P5	DDR	—	DDR_RAS_b	—	—
DDR_RESET	D6	—	SDRAMC_VDD2P5	DDR	—	DDR_RESET	—	—
DDR_VREF	G5	—	SDRAMC_VDD2P5	DDR	—	DDR_VREF	—	—
DDR_WE_b	C6	—	SDRAMC_VDD2P5	DDR	—	DDR_WE_b	—	—
DDR_ZQ	A3	—	SDRAMC_VDD2P5	DDR	—	DDR_ZQ	—	—
EXT_POR	T1	23	VDD33	GPIO	—	EXT_POR	—	—
EXT_TAMPER0	T14	—	VBAT	Analog	—	EXT_TAMPER0	—	—
EXT_TAMPER1	U14	—	VBAT	Analog	—	EXT_TAMPER1	—	—
EXT_TAMPER2/ EXT_WM0_TAMPER_IN	T13	—	VBAT	Analog	—	EXT_TAMPER2/ EXT_WM0_TAMPER_IN	—	—
EXT_TAMPER3/ EXT_WM0_TAMPER_OUT	U13	—	VBAT	Analog	—	EXT_TAMPER3/ EXT_WM0_TAMPER_OUT	—	—
EXT_TAMPER4/ EXT_WM1_TAMPER_IN	U12	—	VBAT	Analog	—	EXT_TAMPER4/ EXT_WM1_TAMPER_IN	—	—
EXT_TAMPER5/ EXT_WM1_TAMPER_OUT	U10	—	VBAT	Analog	—	EXT_TAMPER5/ EXT_WM1_TAMPER_OUT	—	—

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Table 81. Functional Assignment Pins (continued)

Signal Name	364 MAP BGA	176 LQFP (R-series ONLY)	Power Group	Pad Type	Default Mode (Reset)	Default Function	Input/ Output	Value
EXTAL	Y13	73	DECAP_V11_LDO_OUT	Analog	—	EXTAL	—	—
EXTAL32	Y12	70	DECAP_V11_LDO_OUT	Analog	—	EXTAL32	—	—
JTCLK/ SWCLK	K4	3	VDD33	GPIO	ALT1	JTAG	Input	100K PU
JTDI	K2	4	VDD33	GPIO	ALT1	JTAG	Input	100K PU
JTDO	K1	5	VDD33	GPIO	ALT1	JTAG	Disabled	—
JTMS/ SWDIO	L1	6	VDD33	GPIO	ALT1	JTAG	Input	100K PU
LVDS0P	W14	—	DECAP_V25_LDO_OUT	Analog	—	LVDS0P	—	—
LVDS0N	Y14	—	DECAP_V25_LDO_OUT	Analog	—	LVDS0N	—	—
PTA6	N5	19	VDD33	GPIO	ALT0	GPIO	Disabled	
PTA7	V15	75	VDD33	GPIO	ALT0	GPIO	Disabled	
PTA12	L3	7	VDD33	GPIO	ALT0	GPIO	Disabled	
PTA16	Y5	43	VDD33	GPIO	ALT0	GPIO	Disabled	
PTA17	Y6	44	VDD33	GPIO	ALT0	GPIO	Disabled	
PTA18	V6	46	VDD33	GPIO	ALT0	GPIO	Disabled	
PTA19	U6	47	VDD33	GPIO	ALT0	GPIO	Disabled	
PTA20	B18	143	VDD33	GPIO	ALT0	GPIO	Disabled	
PTA21	D18	145	VDD33	GPIO	ALT0	GPIO	Disabled	
PTA22	E17	147	VDD33	GPIO	ALT0	GPIO	Disabled	
PTA23	C17	148	VDD33	GPIO	ALT0	GPIO	Disabled	
PTA24	R16	—	VDD33	GPIO	ALT0	GPIO	Disabled	
PTA25	R17	—	VDD33	GPIO	ALT0	GPIO	Disabled	
PTA26	R19	—	VDD33	GPIO	ALT0	GPIO	Disabled	
PTA27	R20	—	VDD33	GPIO	ALT0	GPIO	Disabled	
PTA28	P20	—	VDD33	GPIO	ALT0	GPIO	Disabled	
PTA29	P18	—	VDD33	GPIO	ALT0	GPIO	Disabled	
PTA30	P17	—	VDD33	GPIO	ALT0	GPIO	Disabled	
PTA31	P16	—	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB0	T6	49	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB1	T7	50	VDD33	GPIO	ALT3	RCON30	Input	Disabled
PTB2	V7	51	VDD33	GPIO	ALT3	RCON31	Input	Disabled

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Table 81. Functional Assignment Pins (continued)

Signal Name	364 MAP BGA	176 LQFP (R-series ONLY)	Power Group	Pad Type	Default Mode (Reset)	Default Function	Input/ Output	Value
PTB3	W7	53	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB4	Y7	54	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB5	Y8	55	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB6	W8	56	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB7	D13	166	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB8	J16	121	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB9	J19	123	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB10	B15	159	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB11	D14	164	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB12	E13	165	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB13	D15	156	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB14	B14	162	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB15	A14	161	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB16	C14	163	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB17	A15	160	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB18	B12	171	VDD33	GPIO	ALT0	GPIO	Input	Disabled
PTB19	C13	167	VDD33	GPIO	ALT0	GPIO	Input	Disabled
PTB20	A13	169	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB21	E12	173	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB22	D12	172	VDD33	GPIO	ALT0	GPIO	Disabled	
PTB23	A19	141	VDD33	GPIO	ALT3	GPIO	Disabled	
PTB24	A18	142	VDD33	GPIO	ALT3	GPIO	Disabled	
PTB25	B17	149	VDD33	GPIO	ALT3	GPIO	Disabled	
PTB26	A17	150	VDD33	GPIO	ALT3	RCON21	Input	Disabled
PTB27	U8	57	VDD33	GPIO	ALT3	RCON22	Input	Disabled
PTB28	A16	151	VDD33	GPIO	ALT3	RCON23	Input	Disabled
PTC0	L4	8	VDD33	GPIO	ALT7	RCON18	Input	Disabled
PTC1	L5	9	VDD33	GPIO	ALT7	RCON19	Input	Disabled
PTC2	M5	11	VDD33	GPIO	ALT7	RCON20	Input	Disabled
PTC3	M3	12	VDD33	GPIO	ALT0	GPIO	Disabled	
PTC4	L2	14	VDD33	GPIO	ALT0	GPIO	Disabled	
PTC5	M1	15	VDD33	GPIO	ALT0	GPIO	Disabled	
PTC6	N1	16	VDD33	GPIO	ALT0	GPIO	Disabled	
PTC7	N2	17	VDD33	GPIO	ALT0	GPIO	Disabled	
PTC8	N4	18	VDD33	GPIO	ALT0	GPIO	Disabled	
PTC9	T15	—	VDD33	GPIO	ALT0	GPIO	Disabled	
PTC10	U15	—	VDD33	GPIO	ALT0	GPIO	Disabled	

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Table 81. Functional Assignment Pins (continued)

Signal Name	364 MAP BGA	176 LQFP (R-series ONLY)	Power Group	Pad Type	Default Mode (Reset)	Default Function	Input/ Output	Value
PTC11	P4	—	VDD33	GPIO	ALT0	GPIO	Disabled	
PTC12	P3	—	VDD33	GPIO	ALT0	GPIO	Disabled	
PTC13	P1	—	VDD33	GPIO	ALT0	GPIO	Disabled	
PTC14	R1	—	VDD33	GPIO	ALT0	GPIO	Disabled	
PTC15	P2	—	VDD33	GPIO	ALT0	GPIO	Disabled	
PTC16	R3	—	VDD33	GPIO	ALT0	GPIO	Disabled	
PTC17	R4	—	VDD33	GPIO	ALT0	GPIO	Disabled	
PTC26	D16	153	VDD33	GPIO	ALT3	RCON24	Input	Disabled
PTC27	E16	154	VDD33	GPIO	ALT3	RCON25	Input	Disabled
PTC28	E15	155	VDD33	GPIO	ALT3	RCON26	Input	Disabled
PTC29	C16	152	VDD33	GPIO	ALT3	RCON27	Input	Disabled
PTC30	T8	58	VDD33	GPIO	ALT3	RCON28	Input	Disabled
PTC31	W5	42	VDD33	GPIO	ALT3	RCON29	Input	Disabled
PTD0	Y17	86	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD1	Y18	87	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD2	V18	88	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD3	Y19	89	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD4	W19	90	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD5	W20	91	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD6	V20	92	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD7	V19	93	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD8	U17	94	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD9	U18	97	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD10	U20	98	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD11	T20	99	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD12	T19	100	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD13	T18	101	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD16	D20	133	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD17	E20	132	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD18	E18	131	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD19	F16	130	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD20	F17	129	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD21	F19	128	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD22	F20	126	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD23	G20	124	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD24	G19	—	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD25	G18	—	VDD33	GPIO	ALT0	GPIO	Disabled	

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Table 81. Functional Assignment Pins (continued)

Signal Name	364 MAP BGA	176 LQFP (R-series ONLY)	Power Group	Pad Type	Default Mode (Reset)	Default Function	Input/ Output	Value
PTD26	G16	—	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD27	H16	—	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD28	H17	—	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD29	H18	—	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD30	H20	—	VDD33	GPIO	ALT0	GPIO	Disabled	
PTD31	J20	—	VDD33	GPIO	ALT0	GPIO	Disabled	
PTE0	N16	103	VDD33	GPIO	ALT2	BMODE1	Input	Disabled
PTE1	N18	104	VDD33	GPIO	ALT2	BMODE0	Input	Disabled
PTE2	N19	105	VDD33	GPIO	ALT0	GPIO	Disabled	
PTE3	Y15	77	VDD33	GPIO	ALT0	GPIO	Disabled	
PTE4	N20	106	VDD33	GPIO	ALT0	GPIO	Disabled	
PTE5	T16	80	VDD33	GPIO	ALT0	GPIO	Disabled	
PTE6	W16	81	VDD33	GPIO	ALT0	GPIO	Disabled	
PTE7	M20	109	VDD33	GPIO	ALT3	RCON0	Input	Disabled
PTE8	M19	110	VDD33	GPIO	ALT3	RCON1	Input	Disabled
PTE9	M17	111	VDD33	GPIO	ALT3	RCON2	Input	Disabled
PTE10	M16	112	VDD33	GPIO	ALT3	RCON3	Input	Disabled
PTE11	L16	113	VDD33	GPIO	ALT3	RCON4	Input	Disabled
PTE12	L17	114	VDD33	GPIO	ALT3	RCON5	Input	Disabled
PTE13	Y16	78	VDD33	GPIO	ALT0	GPIO	Disabled	
PTE14	W15	76	VDD33	GPIO	ALT0	GPIO	Disabled	
PTE15	L18	115	VDD33	GPIO	ALT3	RCON6	Input	Disabled
PTE16	L20	116	VDD33	GPIO	ALT3	RCON7	Input	Disabled
PTE17	K20	117	VDD33	GPIO	ALT3	RCON8	Input	Disabled
PTE18	K19	118	VDD33	GPIO	ALT3	RCON9	Input	Disabled
PTE19	K18	119	VDD33	GPIO	ALT3	RCON10	Input	Disabled
PTE20	A12	170	VDD33	GPIO	ALT3	RCON11	Input	Disabled
PTE21	V16	79	VDD33	GPIO	ALT0	GPIO	Disabled	
PTE22	W17	84	VDD33	GPIO	ALT0	GPIO	Disabled	
PTE23	J17	122	VDD33	GPIO	ALT3	RCON12	Input	Disabled
PTE24	D19	134	VDD33	GPIO	ALT3	RCON13	Input	Disabled
PTE25	C19	135	VDD33	GPIO	ALT3	RCON14	Input	Disabled
PTE26	C20	137	VDD33	GPIO	ALT3	RCON15	Input	Disabled
PTE27	B20	138	VDD33	GPIO	ALT3	RCON16	Input	Disabled
PTE28	K16	120	VDD33	GPIO	ALT3	RCON17	Input	Disabled
RESETB/ RESET_OUT	T4	28	VDD33	GPIO	—	RESETB/ RESET_OUT	—	—

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Table 81. Functional Assignment Pins (continued)

Signal Name	364 MAP BGA	176 LQFP (R-series ONLY)	Power Group	Pad Type	Default Mode (Reset)	Default Function	Input/ Output	Value
TEST	T3	27	VDD33	GPIO	—	TEST	—	—
USB0_DM	T9	62	USB_DCAP	Analog	—	USB0_DM	—	—
USB0_DP	T10	63	USB_DCAP	Analog	—	USB0_DP	—	—
USB0_VBUS	W11	60	USB_DCAP	Analog	—	USB0_VBUS	—	—
USB0_VBUS_ DETECT	Y11	64	USB_DCAP	Analog	—	USB0_VBUS_ DETECT	—	—
USB1_DM	V9	—	USB_DCAP	Analog	—	USB1_DM	—	—
USB1_DP	W9	—	USB_DCAP	Analog	—	USB1_DP	—	—
USB1_VBUS	W10	—	USB_DCAP	Analog	—	USB1_VBUS	—	—
USB1_VBUS_ DETECT	U9	—	USB_DCAP	Analog	—	USB1_VBUS_ DETECT	—	—
VADCSE0	Y4	35	VDDA33_ADC / VDD12_AFE / VADC_AFE_BANDGAP ?	Analog	—	VADCSE0	—	—
VADCSE1	U4	37	VDDA33_ADC / VDD12_AFE / VADC_AFE_BANDGAP ?	Analog	—	VADCSE1	—	—
VADCSE2	W4	—	VDDA33_ADC / VDD12_AFE / VADC_AFE_BANDGAP ?	Analog	—	VADCSE2	—	—
VADCSE3	V5	—	VDDA33_ADC / VDD12_AFE / VADC_AFE_BANDGAP ?	Analog	—	VADCSE3	—	—
XTAL	W13	72	DECAP_V11_ LDO_OUT	Analog	—	XTAL	—	—
XTAL32	W12	71	DECAP_V11_ LDO_OUT	Analog	—	XTAL32	—	—

15 Revision History

The following table provides a revision history for this document.

Table 82. Revision History

Rev. No.	Date	Substantial Changes
Rev 1	12/2011	Initial release
Rev 2	2/2012	Updated feature list Updated VREG electrical specifications Updated LDO_1P1, LDO2P5 tables Updated DDR IO parameters Added DDR memory controller parameters Updated Power sequencing table Added Power supply diagram Updated Recommended operating conditions Replaced DryIce Tamper Electrical Specifications with Voltage and temperature monitor electrical specifications Updated VideoADC electricals. Updated VideoADC supply scheme diagram. Added VideoADC supply_decoupling diagram Added QuadSPI DDR mode electrical specifications Updated Fast internal RC oscillator table Updated Slow internal RC oscillator table Updated Pinouts section
Rev 3	4/2012	Updated device name throughout the document Minor editorial updates in the feature list Updated VREG electrical specifications Updated LDO electrical specifications Updated Power consumption operating behaviors table Added USB PHY Current Consumption table Updated GPIO parameters Updated DDR parameters Updated Power sequencing Updated Power supply figure Updated Recommended operating conditions table Removed Reset specifications Updated 12-bit DAC operating requirements Added a note in 12-bit ADC operating conditions section

Table continues on the next page...

Table 82. Revision History (continued)

Rev. No.	Date	Substantial Changes
		Updated VideoADC Specifications table Updated LCD driver specifications table QuadSPI timing- Replaced VDDE with VDD33 Added notes in DDR3 Timing Parameters and LPDD2 Timing Parameters sections. Updated 24MHz external oscillator electrical characteristics table Updated OSC32K Main Characteristics table Updated Document Number for 144-pin LQFP Changed pin-name from EXT_POR to TEST2, VBAT to VBB Updated Pinouts section Updated GPIO Mapping
Rev 4	8/2012	Updated Part identification Editorial changes in USB PHY Current Consumption in Normal Mode, GPIO AC Electrical Characteristics (3.3V power mode) Updated Power sequencing table Updated Power supply diagram Updated AC electrical specification of following modules: DCU, 12-bit DAC, Ethernet, Enhanced Serial Audio Interface (ESAI), SAI/I2S, Flexbus, MLB, DSPI, 24MHz External Oscillator, JTAG, Debug, ESAI, QSPI Updated Thermal Attributes for 364 MAPBGA Updated document number for 176-pin LQFP and 364 MAPBGA Updated VREG specifications Added WBREG specifications Updated Recommended operating conditions table Updated DAC INL and DNL charts Updated Pinouts
Rev 5	4/2013	• Removed references to VF1xxR and refernces to F100 and 144 LQFP and 256 MAPBGA • Replaced references to Auto and IMM by R-series and F-series respectively • In the feature list, the ARM Core frequency changed to 500 MHz for F-series • In the feature list, changed the DRAM controller frequency • Updated Part Nummbering format • Clarified the Fields table as per Marketing • Sample numbers updated • From the VREG electrical specifications tables, deleted pre-trimming rows and comments • .In the HPREG electrical characteristics table, add footnote on maximum Output Current Capacity • In the ULPREG electrical characteristics table, clarified max value of Output voltage @ no load and min value of Output voltage @ full load • In the WBREG electrical characteristics table, clarified max value of Output voltage @ no load and min value of Output voltage @ full load • In the LVD electrical specifications table, added typ. values of Upper voltage threshold (value @27oC) and Lower voltage threshold (value @27oC) • In the LVD DIG electrical specifications table, removed pretrimming values and clarified other values • Updated LVD DIG electrical specifications values • Updated LDO_1P1 tables

Table continues on the next page...

Table 82. Revision History (continued)

Rev. No.	Date	Substantial Changes
		• Updated LDO_2P5 table • Updated Power consumption operating behaviors tables • Updated Absolute maximum ratings table • Removed Temperature Voltage Monitor section to security RM • Updated VideoADC Specifications table
Rev 6	1/2014	• Added QuadSPI electricals • Changed VBB references to VBAT • In the feature list, clarified that ECC supported for 8-bit mode only, not 16-bit. • Revised the part number format • Revised the field table • Added Absolute Maximum Rating table, which was madde non_cust in the previous version • In the Power Consumption Operating Behavior table, Revised min and max value of IDD_LPS3 and IDD_LPS2. Removed IDD_LPS1 row • In the USB PHY Current Consumption table, removed the Normal Mode • In the Power Sequence table, revised the Power UP/ Down Order column for USB0_VBUs and USB1_VBUS • In the Recommended operating conditions table, revised the min value of VBAT. Revised the min value of VREFH_ADC Revised the min and max values of SDRAMC_VDD1P5 • In the Recommended Connections for Unused Analog Interfaces section, added the notes. Revised the Recommendation if Unused column • In the 12-bit ADC operating conditions, revised Conditions for Ground voltage. Revised min Ref High Voltage • In the 12-bit DAC operating requirements, revised the min and max value of VREFH_ADC • In the SDHC switching specifications, revised the max value of SD6 • In the 24MHz external oscillator electrical characteristics table, revised the min value of VIH and max value of VIL
Rev 7	11/2014	• Updated list of security features on page 1. • In "Part number format" figure, updated explanation for '1'. • In "Fields" table, updated definition of 'R'. • In "Part Numbers" table, added parts SVF331R3K1CKU2, SVF531R3K1CMK4, and SVF532R2K1CMK4. • In "External NPN ballast" section, updated recommendations for transistor selection. • In "DDR parameters" section, updated table footnotes regarding typical condition. • In "Power sequencing" table, added comment regarding SDRAMC_VDD1P5: "In case the Ballast transistor's collector is connected to the 1.5 V DRAM supply (instead of the 3.3 V supply), turn this 1.5 V supply on before turning on the 3.3V." • In "VideoADC specifications" table, added supply current values. • In "Receive and Transmit signal timing specifications," added the following note: "See the most current errata document when using the internally generated RXCLK and TXCLK clocks." • Updated "QuadSPI timing" section, presenting data based on a negative edge data launch from the device and a negative edge data capture; updated the figure, "QuadSPI Input/Read timing (SDR mode)"; updated the table, "QuadSPI Input/Read timing (SDR mode)." • For the "SDHC switching specifcations" table, added the statement, "A load of 50 pF is assumed"; updated max value for SD6, SDHC output delay (output valid). • In the "24 MHz oscillator specifications" section, added the statement, "The crystal must be rated for a drive level of 250 µW or higher. An ESR (equivalent series resistance) of 80 Ω or less is recommended to achieve a gain margin of 5." • In "Pinouts" section, for the 176LQFP package, added information about exposed pad on the bottom side. • In "Special Signal Considerations" table, added that a "fundamental-mode" crystal should be connected between XTAL and EXTAL; updated maximum drive level of crystal rating to 250 µW.
Rev 8	01/2018	• Throughout: Updated references to company website • In the "Part number format" figure, updated the "Option" box with mask options

Table 82. Revision History

Rev. No.	Date	Substantial Changes

		• Deleted the "Fields" section
		• Updated part numbers in "Part numbers" section
		• In "Power consumption operating behaviors" section, updated descriptions and footnotes for IDD_LPS3 and IDD_LPS2
		• In "Absolute maximum ratings" table, added rows for USB0_DP, USB0_DN, USB1_DP, and USB1_DN
		• In the table, "12-bit ADC characteristics (V_{REFH} = V_{DDAD}, V_{REFL} = V_{SSAD})":
		  • Changed mentions of "Temp Sensor" to "Temperature Sensor"
		  • Added footnotes 2 and 3
		• In the table, "12-bit DAC operating behaviors," in footnote 5, changed "V_{DDA} = 3.0 V" to "V_{DDA} = 3.3 V"
		• In "Video Input Unit timing" section, added clocking requirements after introduction
		• Updated "QuadSPI timing" section
		• For "NFC specifications" section:
		  • Changed title to "NAND flash controller specifications"
		  • In the note, specified that the reader should see the CCM section of the product reference manual for more information
		  • Changed title of the figure "Read data latch cycle timing in non-fast mode" to "Read data latch cycle timing in Slow mode"
		  • Changed title of the figure "Read data latch cycle timing in fast mode" to "Read data latch cycle timing in Fast mode and EDO mode"
		• In the table footnotes in the "I2C timing" section, updated the frequency of the PER_CLK, from 83 MHz to 66 MHz
		• In the "Pinouts" table, for L5, changed RMII0_MDIO/MII0_MDC to RMII0_MDIO/ MII0_MDIO

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Revision 8, 01/2018

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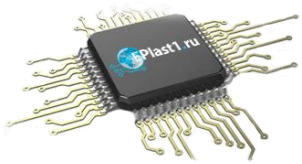

Как с нами связаться

Телефон: 8 (812) 309 58 32 (многоканальный)
Факс: 8 (812) 320-02-42
Электронная почта: org@eplast1.ru
Адрес: 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.