

M5M5V208FP,VP,RV,KV,KR -70L-W, -85L-W, -10L-W, -12L-W, -70LL-W, -85LL-W, -10LL-W, -12LL-W

PRELIMINARY

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Some parametric limits are subject to change.

2097152-BIT (262144-WORD BY 8-BIT) CMOS STATIC RAM

DESCRIPTION

The M5M5V208 is 2,097,152-bit CMOS static RAM organized as 262,144-words by 8-bit which is fabricated using high-performance quadruple-polysilicon and double metal CMOS technology. The use of thin film transistor(TFT) load cells and CMOS periphery results in a high density and low power static RAM. The M5M5V208 is designed for memory applications where high reliability, large storage, simple interfacing and battery back-up are important design objectives.

The M5M5V208VP,RV,KV,KR are packaged in a 32-pin thin small outline package which is a high reliability and high density surface mount device(SMD). Two types of devices are available.

VP,KV(normal lead bend type package),RV,KR(reverse lead bend type package). Using both types of devices, it becomes very easy to design a printed circuit board.

FEATURE

Type	Access time (max)	Power supply current	
		Active (max)	Stand-by (max)
M5M5V208FP,VP,RV,KV,KR-70L	70ns	27mA (V _{CC} =3.6V)	60μA (V _{CC} =3.6V)
M5M5V208FP,VP,RV,KV,KR-85L	85ns		
M5M5V208FP,VP,RV,KV,KR-10L	100ns		
M5M5V208FP,VP,RV,KV,KR-12L	120ns		
M5M5V208FP,VP,RV,KV,KR-70LL	70ns	10μA (V _{CC} =3.6V)	10μA (V _{CC} =3.6V)
M5M5V208FP,VP,RV,KV,KR-85LL	85ns		
M5M5V208FP,VP,RV,KV,KR-10LL	100ns		
M5M5V208FP,VP,RV,KV,KR-12LL	120ns		

- Single 2.7 ~ 3.6V power supply
- W-version: operating temperature of -20 to +70°C
- No clocks, No refresh
- All inputs and outputs are TTL compatible.
- Easy memory expansion and power down by S1 & S2
- Data retention supply voltage=2.0V
- Three-state outputs: OR-tie capability
- OE prevents data contention in the I/O bus
- Common Data I/O
- Battery backup capability
- Small stand-by current 0.3μA(typ.)

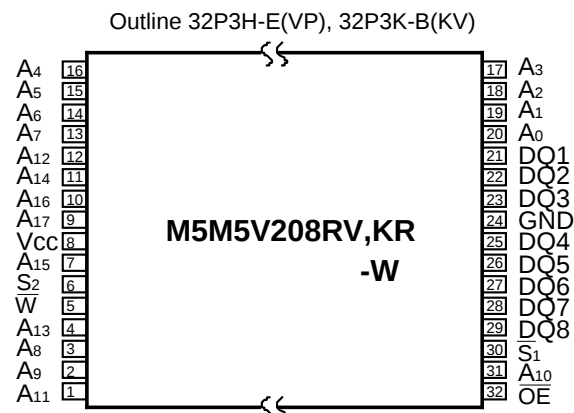
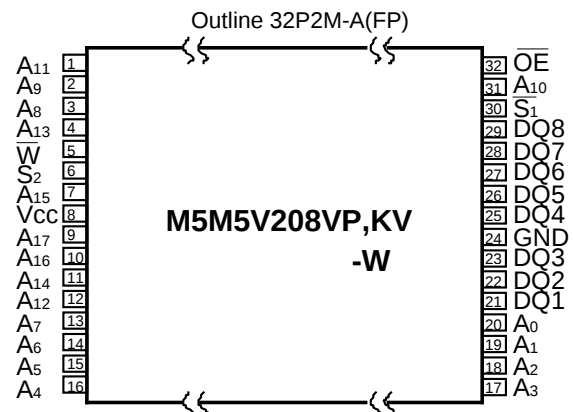
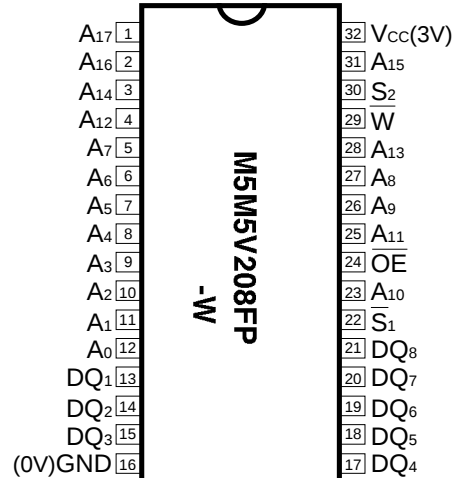
PACKAGE

M5M5V208FP : 32 pin 525 mil SOP
M5M5V208VP,RV : 32pin 8 X 20 mm2 TSOP
M5M5V208KV,KR : 32pin 8 X 13.4 mm2 TSOP

APPLICATION

Small capacity memory units
Battery operating system
Handheld communication tools

PIN CONFIGURATION (TOP VIEW)



Outline 32P3H-F(RV), 32P3K-C(KR)

**-70L-W , -85L -W, -10L-W , -12L-W ,
-70LL-W, -85LL-W, -10LL-W, -12LL-W**

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The operation mode of the M5M5V208 is determined by a combination of the device control inputs $\overline{S_1}$, $\overline{S_2}$, $\overline{W}$ and $\overline{OE}$. Each mode is summarized in the function table.

A write cycle is executed whenever the low level $\overline{W}$ overlaps with the low level $\overline{S_1}$ and the high level S_2 . The address must be set up before the write cycle and must be stable during the entire cycle. The data is latched into a cell on the trailing edge of $\overline{W}$, $\overline{S_1}$ or S_2 , whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained. The output enable OE directly controls the output stage. Setting the OE at a high level, the output stage is in a high-impedance state, and the data bus contention problem in the write cycle is eliminated.

A read cycle is executed by setting $\overline{W}$ at a high level and OE at a low level while $\overline{S_1}$ and S_2 are in an active state ($S_1 = L, S_2 = H$).

When setting $\overline{S_1}$ at a high level or S_2 at a low level, the chips are in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expansion by $\overline{S_1}$ or S_2 . The power supply current is reduced as low as the stand-by current which is specified as I_{cc3} or I_{cc4} , and the memory data can be held at +2V power supply, enabling battery back-up operation during power failure or power-down operation in the non-selected mode.

$\overline{S_1}$	S_2	$\overline{W}$	$\overline{OE}$	Mode	DQ	Icc
X	L	X	X	Non selection	High-impedance	Standby
H	X	X	X	Non selection	High-impedance	Standby
L	H	L	X	Write	D _{IN}	Active
L	H	H	L	Read	D _{OUT}	Active
L	H	H	H		High-impedance	Active

BLOCK DIAGRAM

The block diagram illustrates the internal architecture of the 262144 Words X 8 Bits memory device. The central component is the memory array, which is organized into 512 rows, 128 columns, and 32 blocks. The array is connected to an address input buffer, a row decoder, a column decoder, a clock generator, a sense amplifier, and an output buffer. The address input buffer is connected to the address input pins (A0-A17, A4-A7, A12-A15, A10-A13). The row decoder is connected to the address input buffer and the memory array. The column decoder is connected to the address input buffer and the memory array. The clock generator is connected to the address input buffer, the column decoder, and the memory array. The sense amplifier is connected to the memory array and the output buffer. The output buffer is connected to the data output pins (DQ0-DQ7). The diagram also shows the pin connections for address, data, and control signals, including VCC (3V) and GND (0V).

Pin Connections:

- Address Pins (A0-A17):** 18 pins, grouped into three sets of six (A0-A5, A6-A11, A12-A17).
- Data Pins (DQ0-DQ7):** 8 pins, grouped into two sets of four (DQ0-DQ3, DQ4-DQ7).
- Control Pins:** W (Write Enable), S1 (Sense Amplifier Enable), S2 (Sense Amplifier Enable), OE (Output Enable).
- Power Pins:** VCC (3V), GND (0V).

Internal Components:

- Address Input Buffer:** Receives address signals from the pins and provides a buffered output to the decoders.
- Row Decoder:** Decodes the row address and selects the appropriate row in the memory array.
- Column Decoder:** Decodes the column address and selects the appropriate column in the memory array.
- Clock Generator:** Generates a clock signal for the memory array and the decoders.
- Sense Amplifier:** Amplifies the data signals from the memory array and provides a buffered output to the output buffer.
- Output Buffer:** Provides a buffered output for the data signals to the data pins.

Pin Numbers: Pin numbers inside the dotted line show those of TSOP.

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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V _{CC}	Supply voltage	With respect to GND	- 0.5*~4.6	V
V _I	Input voltage		- 0.5* ~ V _{CC} + 0.5 (Max 4.6)	V
V _O	Output voltage		0 ~ V _{CC}	V
P _d	Power dissipation	T _a =25°C	700	mW
T _{opr}	Operating temperature		- 20 ~ 70	°C
T _{str}	Storage temperature		- 65 ~150	°C

* -3.0V in case of AC (Pulse width £ 30ns)

DC ELECTRICAL CHARACTERISTICS

(T_a=- 20~70°C, V_{CC}= 2.7 ~ 3.6V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V _{IH}	High-level input voltage		2.0		V _{CC} +0.3V	V
V _{IL}	Low-level input voltage		-0.3*		0.6	V
V _{OH1}	High-level output voltage 1	I _{OH} = -0.5mA	2.4			V
V _{OH2}	High-level output voltage 2	I _{OH} = -0.05mA	V _{CC} -0.5V			V
V _{OL}	Low-level output voltage	I _{OL} =2mA			0.4	V
I _I	Input current	V _I =0 ~ V _{CC}			±1	µA
I _O	Output current in off-state	$\bar{S}_1=V_{IH}$ or $S_2=V_{IL}$ or $\bar{OE}=V_{IH}$ V _{I/O} =0 ~ V _{CC}			±1	µA
I _{CC1}	Active supply current (CMOS-level Input)	$\bar{S}_1$ £ 0.2V, S_2 ≥ V _{CC} -0.2V, other inputs £ 0.2V or ≥ V _{CC} -0.2V,output-open	f= 10MHz	20	25	mA
			f= 5MHz	10	13	
I _{CC2}	Active supply current (TTL-level Input)	$\bar{S}_1=V_{IL}$, $S_2=V_{IH}$, other inputs=V _{IH} or V _{IL} output-open	f= 10MHz	22	27	mA
			f= 5MHz	12	15	
I _{CC3}	Stand-by current	1) S_2 £ 0.2V or 2) $\bar{S}_1$ ≥ V _{CC} -0.2V, S_2 ≥ V _{CC} -0.2V other inputs=0 ~ V _{CC}	-L -20 ~ +70°C		60	µA
			-20 ~ +70°C		10	
		-LL -20 ~ +40°C			1	
			+25°C	0.3	0.6	
I _{CC4}	Stand-by current	$\bar{S}_1=V_{IH}$ or $S_2=V_{IL}$, other inputs=0 ~ V _{CC}			0.33	mA

* -3.0V in case of AC (Pulse width £ 30ns)

CAPACITANCE

(T_a=- 20 ~ 70°C, V_{CC}= 2.7 ~ 3.6V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
C _I	Input capacitance	V _I =GND, V _I =25mVrms, f=1MHz			7	pF
C _O	Output capacitance	V _O =GND, V _O =25mVrms, f=1MHz			9	pF

Note 1: Direction for current flowing into an IC is positive (no mark).

2: Typical value is for V_{CC} = 3V, T_a = 25°C

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AC ELECTRICAL CHARACTERISTICS

(Ta = -20 ~ 70°C, Vcc = 2.7 ~ 3.6V, unless otherwise noted)

(1) MEASUREMENT CONDITIONS

Vcc 2.7 ~ 3.6V
Input pulse level V_{IH}=2.2V, V_{IL}=0.4V
Input rise and fall time 5ns
Reference level V_{OH}=V_{OL}=1.5V
Output loads Fig.1, CL=30pF

CL=5pF (for ten, tdis)

Transition is measured ±500mV from steady state voltage. (for ten, tdis)

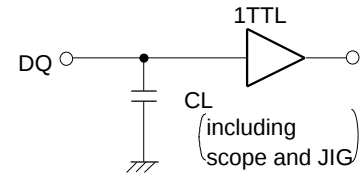


Fig.1 Output load

(2) READ CYCLE

Symbol	Parameter	Limits								Unit
		-70L,LL		-85L,LL		-10L,LL		-12L,LL		
		Min	Max	Min	Max	Min	Max	Min	Max	
t _{CR}	Read cycle time	70		85		100		120		ns
t _a (A)	Address access time		70		85		100		120	ns
t _a (S ₁)	Chip select 1 access time		70		85		100		120	ns
t _a (S ₂)	Chip select 2 access time		70		85		100		120	ns
t _a (OE)	Output enable access time		35		45		50		60	ns
t _{dis} (S ₁)	Output disable time after S ₁ high		25		30		35		40	ns
t _{dis} (S ₂)	Output disable time after S ₂ low		25		30		35		40	ns
t _{dis} (OE)	Output disable time after OE high		25		30		35		40	ns
t _{en} (S ₁)	Output enable time after S ₁ low	10		10		10		10		ns
t _{en} (S ₂)	Output enable time after S ₂ high	10		10		10		10		ns
t _{en} (OE)	Output enable time after OE low	5		5		5		5		ns
t _v (A)	Data valid time after address	10		10		10		10		ns

(3) WRITE CYCLE

Symbol	Parameter	Limits								Unit
		-70L,LL		-85L,LL		-10L,LL		-12L,LL		
		Min	Max	Min	Max	Min	Max	Min	Max	
t _{cw}	Write cycle time	70		85		100		120		ns
t _w (W)	Write pulse width	55		60		75		85		ns
t _{su} (A)	Address setup time	0		0		0		0		ns
t _{su} (A-WH)	Address setup time with respect to W	65		70		85		100		ns
t _{su} (S ₁)	Chip select 1 setup time	65		70		85		100		ns
t _{su} (S ₂)	Chip select 2 setup time	65		70		85		100		ns
t _{su} (D)	Data setup time	30		35		40		45		ns
t _h (D)	Data hold time	0		0		0		0		ns
t _{rec} (W)	Write recovery time	0		0		0		0		ns
t _{dis} (W)	Output disable time from W low		25		30		35		40	ns
t _{dis} (OE)	Output disable time from OE high		25		30		35		40	ns
t _{en} (W)	Output enable time from W high	5		5		5		5		ns
t _{en} (OE)	Output enable time from OE low	5		5		5		5		ns

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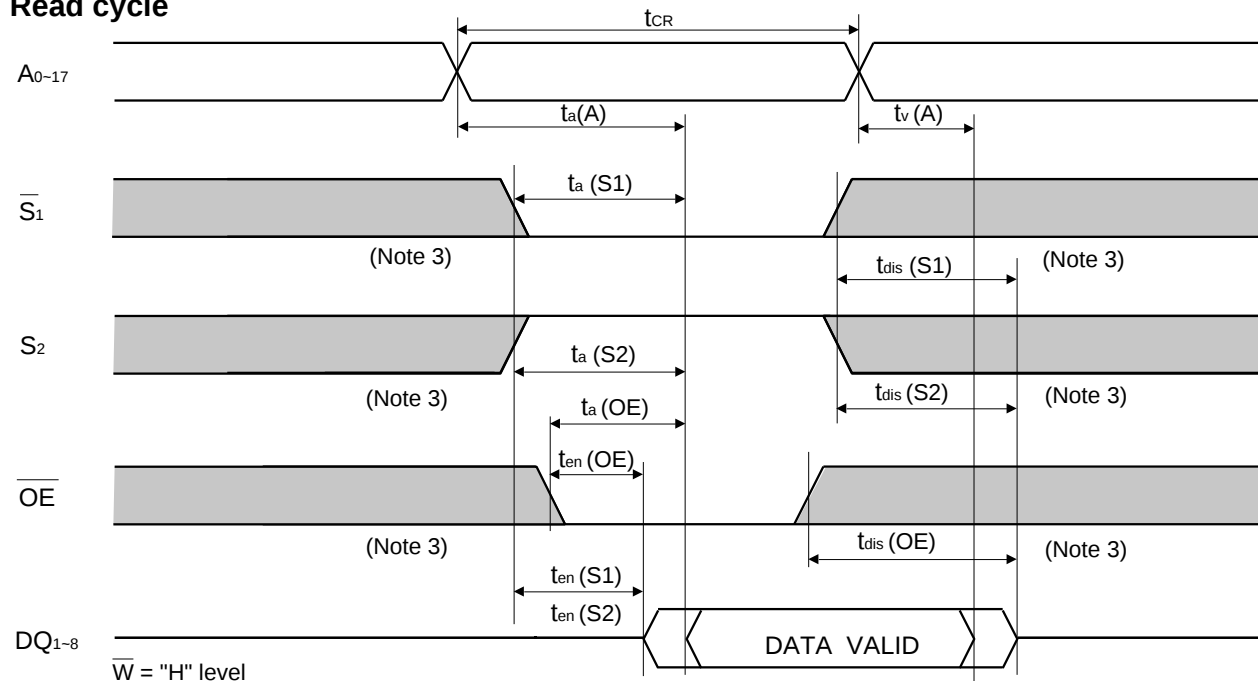
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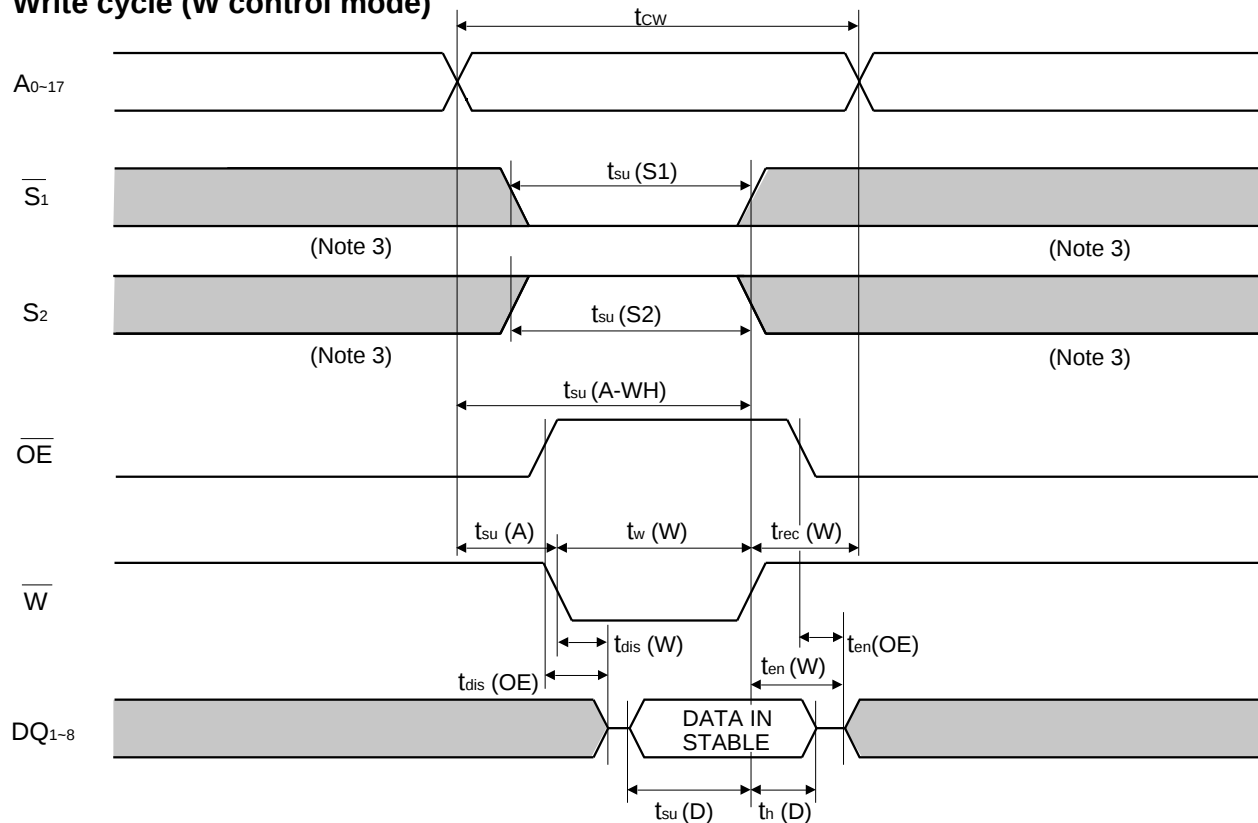
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(4) TIMING DIAGRAMS

Read cycle



Write cycle ($\overline{W}$ control mode)



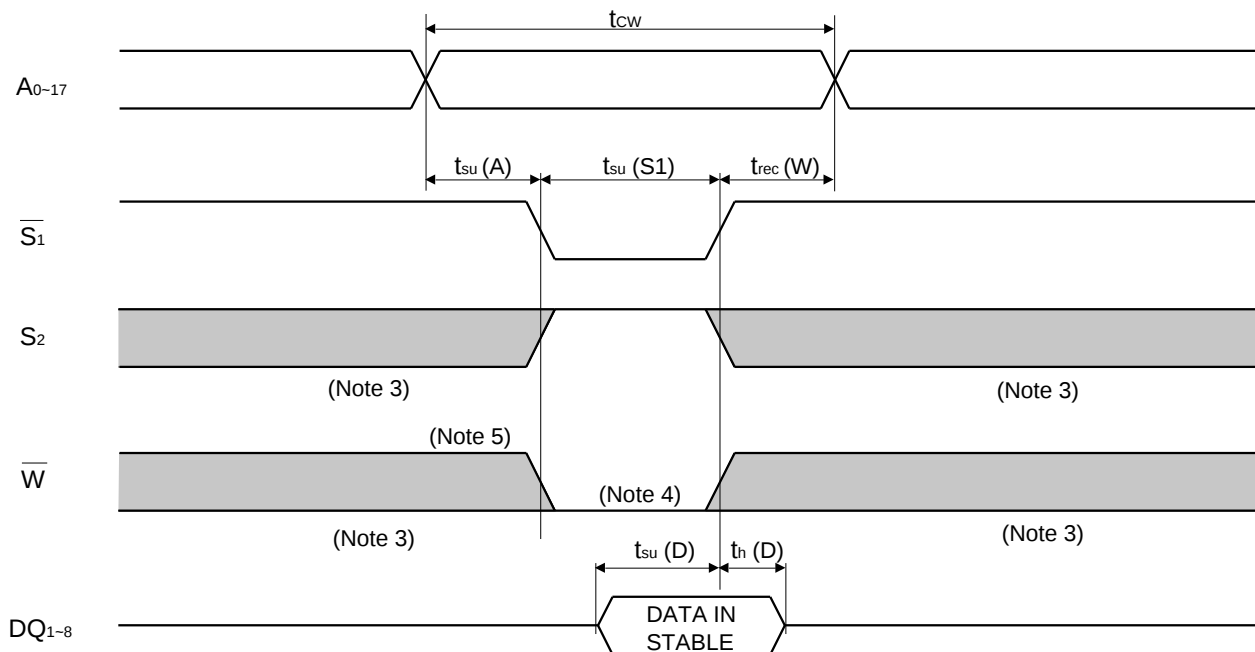
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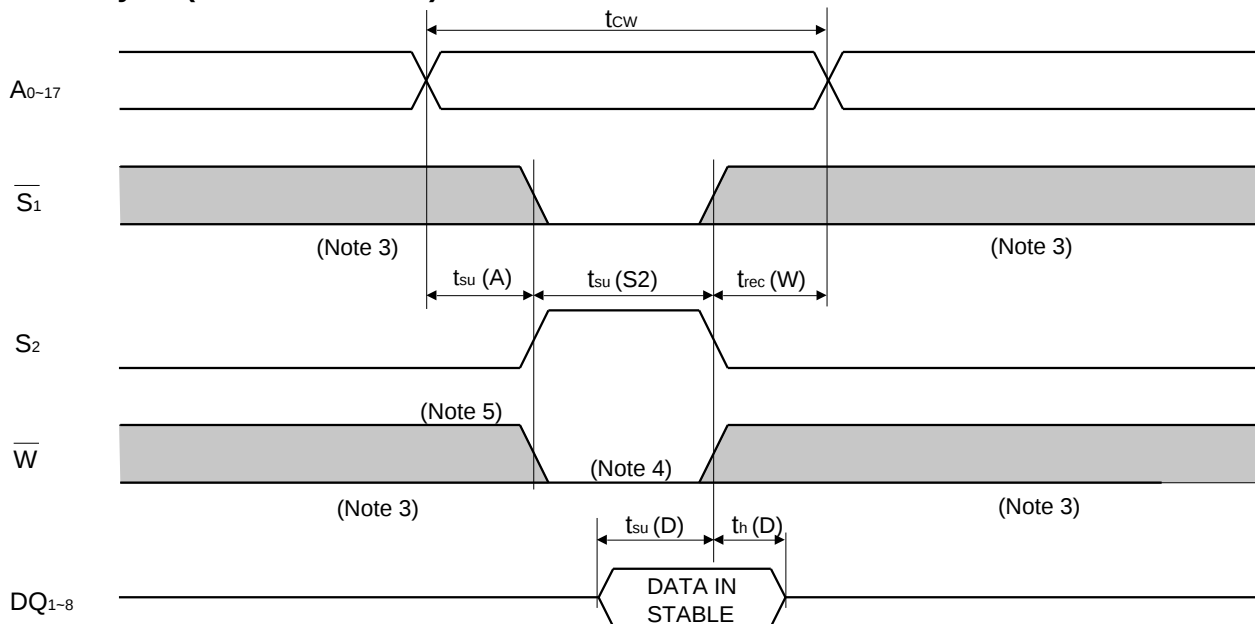
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Write cycle ($\overline{S_1}$ control mode)



Write cycle (S_2 control mode)



Note 3: Hatching indicates the state is "don't care".

4: Writing is executed while S_2 high overlaps S_1 and $\overline{W}$ low.

5: When the falling edge of $\overline{W}$ is simultaneously or prior to the falling edge of $\overline{S_1}$ or rising edge of S_2 , the outputs are maintained in the high impedance state.

6: Don't apply inverted phase signal externally when DQ pin is output mode.



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ELECTRIC

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POWER DOWN CHARACTERISTICS

(1) ELECTRICAL CHARACTERISTICS

(Ta = -20 ~ 70°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V _{CC} (PD)	Power down supply voltage		2			V
V _I ($\overline{S_1}$)	Chip select input $\overline{S_1}$		2.0			V
V _I (S ₂)	Chip select input S ₂				0.2	V
I _{CC} (PD)	Power down supply current	V _{CC} = 3.0V S ₂ $\leq$ 0.2V or $\overline{S_1} \geq V_{CC} - 0.2V, S_2 \geq V_{CC} - 0.2V$	-L		50	μA
			-LL	0.3	8 (Note 7)	

Note7: I_{CC} (PD) = 0.5 μA (Max.) in case of Ta = +25°C

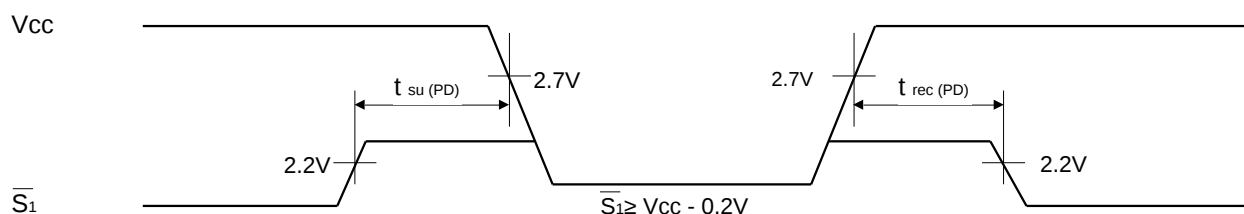
(2) TIMING REQUIREMENTS

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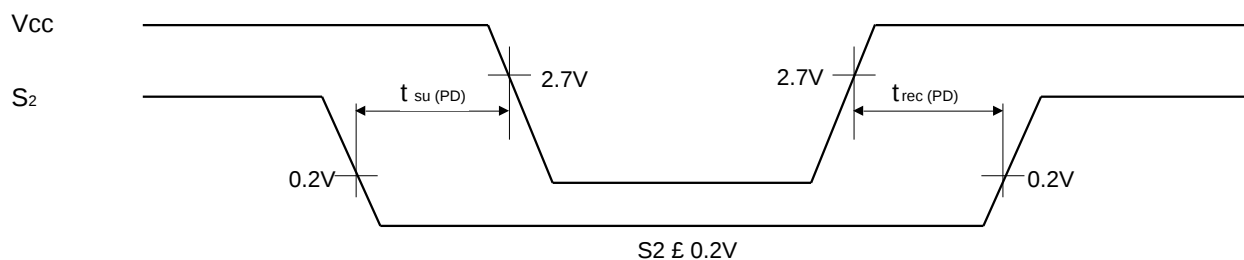
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t _{su} (PD)	Power down set up time		0			ns
t _{rec} (PD)	Power down recovery time		5			ms

(3) POWER DOWN CHARACTERISTICS

$\overline{S_1}$ control mode



S₂ control mode





Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов;
- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

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