DisplayPort™1:1 Re-Driver with Link Training

Check for Samples: SN75DP130

FEATURES

- **Supports DP v1.1a and DP v1.2 Signaling Including HBR2 Data Rates to 5.4Gbps**
- **Supports HDMI 1.4a with TMDS Clock Frequencies up to 340MHz**
- **Glue-Less interface to AMD, Intel, and NVIDIA Graphics Processors**
- **Auto-Configuration Through Link Training**
- **Output Signal Conditioning with Tunable Voltage Swing and Pre-Emphasis Gain**
- **Highly Configurable Input Variable Equalizer**
- **Two Device Options Including a Dual Power Supply Configuration for Lowest Power**
- **2kV ESD HBM Protection**
- **Temperature Range: 0°C to 85°C**
- **48 Pin 7mm × 7mm QFN Package**

APPLICATIONS

- **Notebook PC**
- **Desktop PC**
- **PC Docking Station**
- **PC Standalone Video Card**

DESCRIPTION

The SN75DP130 is a single channel DisplayPort™ (DP) re-driver that regenerates the DP high speed digital link. The device complies with the VESA DisplayPort Standard Version 1.2, and supports a four lane Main Link interface signaling up to HBR2 rates at 5.4Gbps per lane, and supports DP++ Dual-Mode; offering TMDS signaling for DVI and full HDMI Version 1.4a support.

The device compensates for PCB related frequency loss and switching related loss to provide the optimum DP electrical performance from source to sink. The Main Link signal inputs feature configurable equalizers with selectable boost settings. At the Main Link output, four primary levels of differential output voltage swing (VOD) and four primary levels of pre-emphasis are available, as well as a secondary level of boost adjustment, programmed through I^2C, for fine-tuning the Main Link output. The device can monitor the AUX channel and automatically adjust the output signaling levels and input equalizers in response to Link Training commands. Additionally, the SN75DP130 output signal conditioning and EQ parameters are fully programmable through the I^2C interface.

The SN75DP130 offers separate AUX and DDC source interfaces that connect to a single AUX sink channel. This minimizes component count when implemented with a graphics processor (GPU) comprising separate DDC and AUX interfaces. For GPUs with combined DDC/AUX, the device can operate as a FET switch to short circuit the AUX channel AC coupling caps while connected to a TMDS sink device. Other sideband circuits such as Hot Plug Detect (HPD) are optimized to reduce external components, providing a seamless connection to Intel, AMD, and NVIDIA graphics processors.

The SN75DP130 is optimized for mobile applications, and contains activity detection circuitry on the Main Link input that transitions to a low-power Output Disable mode in the absence of a valid input signal. Other low power modes are supported, including a Standby mode with typical dissipation of ~2mW when no video sink (e.g., monitor) is connected.

The device is characterized for an extended operational temperature range from 0°C to 85°C.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

TYPICAL IMPLEMENTATIONS

The configuration shown in Figure 1 supports a GPU with unified AUX/DDC interfaces. This circuit provides back current protection into the GPU AUX, HPD, and CAD inputs.

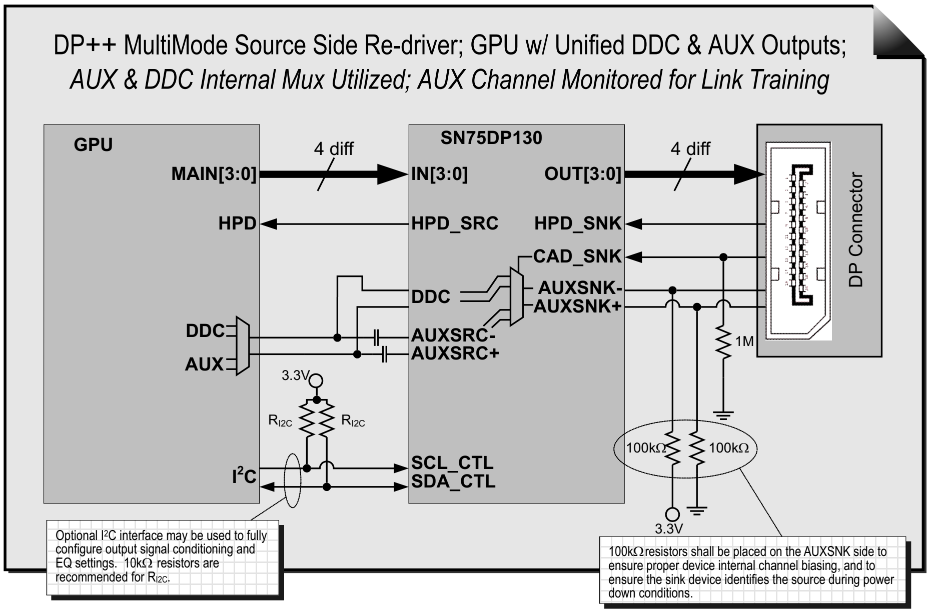

Figure 1. DP++ Dual-Mode in a Unified AUX/DDC Configuration

The configuration shown in Figure 2 supports a GPU with separate DDC and AUX interfaces, and overcomes the need for an external AUX to DDC switch. This circuit provides back current protection into the GPU AUX, HPD, and CAD inputs.

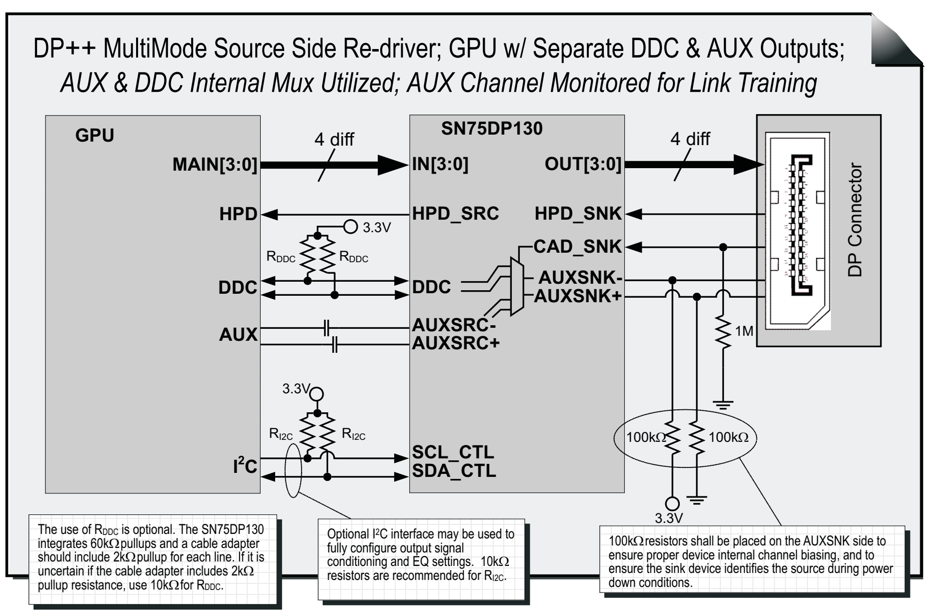

Figure 2. DP++ Dual-Mode in a Split AUX and DDC Configuration

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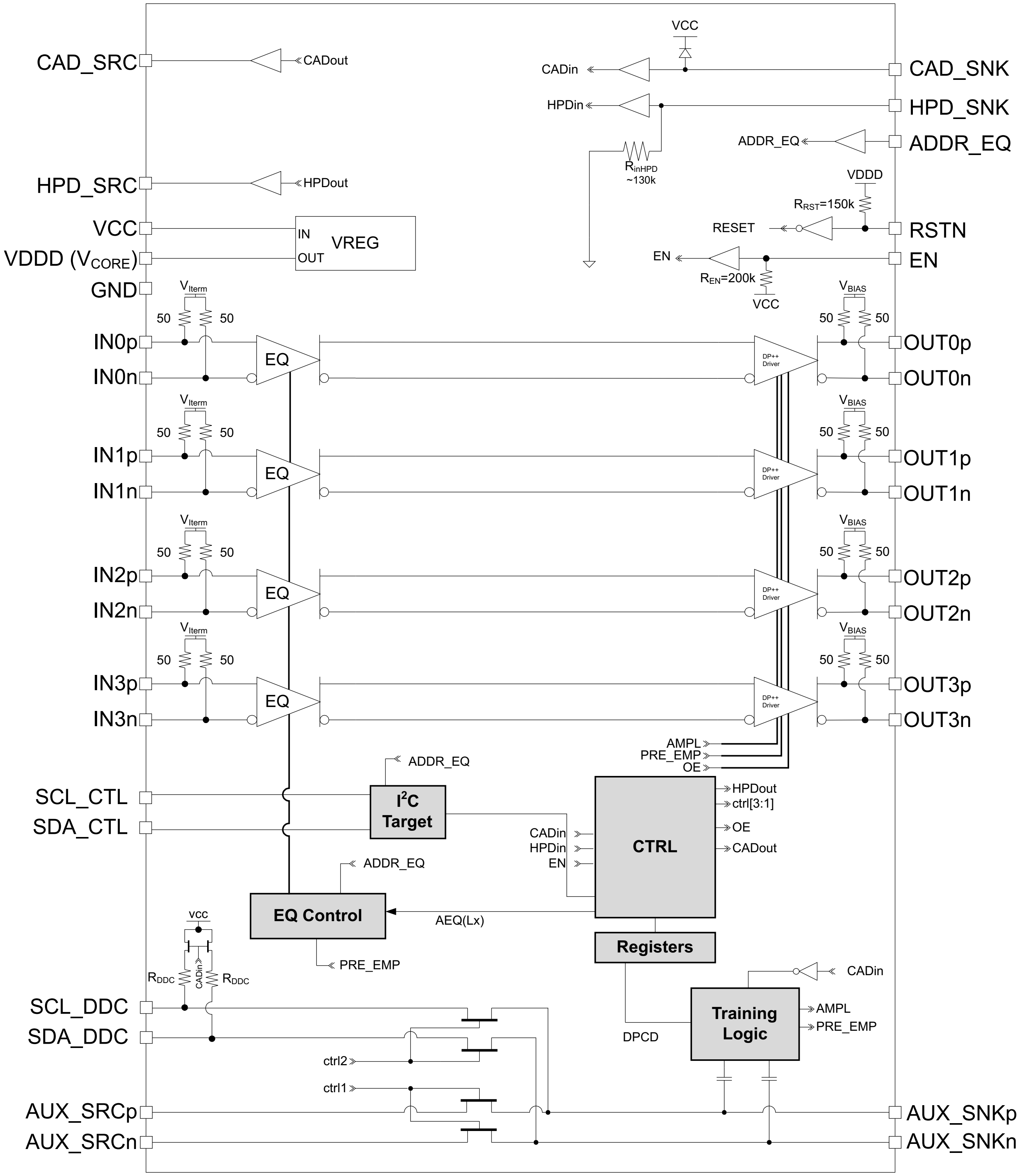
BLOCK DIAGRAM



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TERMINAL ASSIGNMENTS

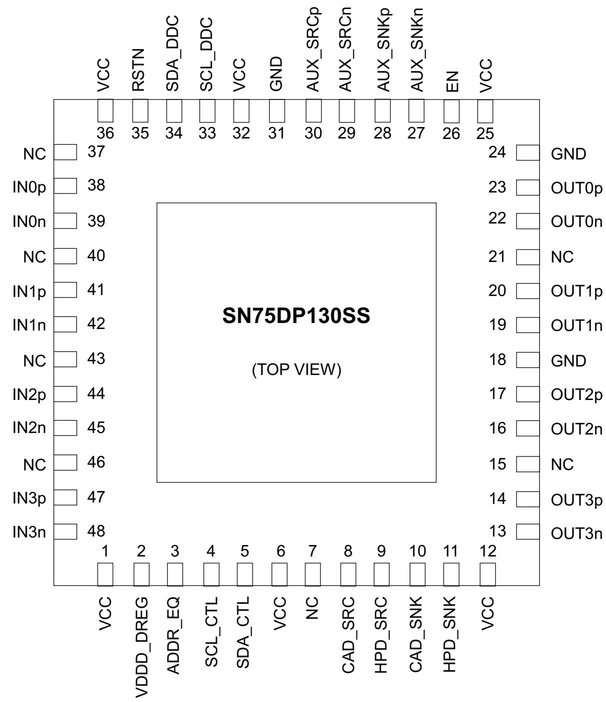

Figure 3. SN75DP130SS Single Supply

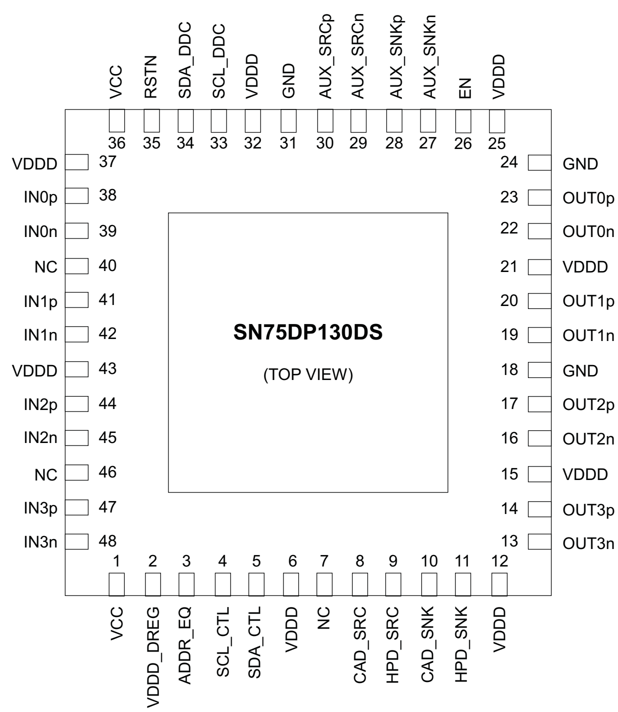

Figure 4. SN75DP130DS Dual Supply

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PIN FUNCTIONS

PIN NAME	PIN NO.	I/O	DESCRIPTION
MAIN LINK TERMINALS			
IN0p, IN0n	38, 39	Input (100Ω diff)	DisplayPort Main Link Lane 0 Differential Input
IN1p, IN1n	41, 42		DisplayPort Main Link Lane 1 Differential Input
IN2p, IN2n	44, 45		DisplayPort Main Link Lane 2 Differential Input
IN3p, IN3n	47, 48		DisplayPort Main Link Lane 3 Differential Input
OUT0p, OUT0n	23, 22	Output (100Ω diff)	DisplayPort Main Link Lane 0 Differential Output
OUT1p, OUT1n	20, 19		DisplayPort Main Link Lane 1 Differential Output
OUT2p, OUT2n	17, 16		DisplayPort Main Link Lane 2 Differential Output
OUT3p, OUT3n	14, 13		DisplayPort Main Link Lane 3 Differential Output
AUX CHANNEL AND DDC DATA TERMINALS			
AUX_SRCp, AUX_SRCn	30, 29	I/O (100Ω diff)	Source Side Bidirectional DisplayPort Auxiliary Data Channel. If the AUX_SNK channel is used for monitoring only, these signals are not used and may be left open.
AUX_SNKp, AUX_SNKn	28, 27	I/O (100Ω diff)	Sink Side Bidirectional DisplayPort Auxiliary Data Channel.
SCL_DDC, SDA_DDC	33, 34	I/O	Bidirectional I^2C Display Data Channel (DDC) for TMDS mode. These signals may be utilized together with AUX_SNK to form a FET switch to short-circuit the AC coupling capacitors during TMDS operation in a DP++ Dual-Mode configuration. These terminals include integrated 60 kΩ pull-up resistors
HPD, CAD, and CONTROL TERMINALS			
HPD_SRC	9	O	Hot Plug Detect Output to the DisplayPort Source.
HPD_SNK	11	I	DisplayPort Hot Plug Detect Input from Sink. This device input is 5V tolerant. *Note: Pull this input high during compliance testing or use I^2C control interface to go into compliance test mode and control HPD_SNK and HPD_SRC by software.*
CAD_SRC	8	O	DP Cable Adapter Detect Output. This output typically drives the GPU CAD input.
CAD_SNK	10	I	DisplayPort Cable Adapter Detect Input. This input tolerates a 5V supply with a supply impedance higher than 90kΩ. A device internal zener diode limits the input voltage to 3.3V. An external 1MΩ resistor to GND is recommended. This terminal is used to select DP mode or TMDS mode in a DP++ Dual-Mode application.
SCL_CTL, SDA_CTL	4, 5	I/O	Bidirectional I^2C interface to configure the SN75DP130. This interface is active independent of the EN input but inactive when RSTN is low.
RSTN	35	I	Active Low Device Reset. This input includes a 150kΩ resistor to the VDDD core supply. An external capacitor to GND is recommended on the RSTN input to provide a power-up delay (see the V_{IL} and V_{IH} specifications in the RECOMMENDED OPERATION CONDITIONS table). This signal is used to place the SN75DP130 into Shutdown mode for the lowest power consumption. When the RSTN input is asserted, all outputs (excluding HPD_SRC and CAD_SRC) are high-impedance, and inputs (excluding HPD_SNK and CAD_SNK) are ignored; all I^2C and DPCD registers are reset to their default values. At power up, the RSTN input must not be de-asserted until the VCC and VDDD supplies have reached at least the minimum recommended supply voltage level (see Figure 5 for timing requirements).
EN	26	I	Device Enable. This input incorporates an internal pullup of 200kΩ.
ADDR_EQ	3	3-level Input	I^2C Target Address Select and EQ Configuration Input. If the I^2C bus is used, this input setting selects the I^2C target address, as described in Table 7. This input also configures the input EQ to the device, as described in Table 5.
SUPPLY AND GROUND TERMINALS			
VDDD	SN75DP130DS 6, 12, 15, 21, 25, 32, 37, 43		Digital low voltage core and Main Link supply for SN75DP130DS device option. Nominally 1.1V.
VCC	SN75DP130SS 1, 6, 12, 25, 32, 36		3.3V Supply
	SN75DP130DS 1, 36		

PIN FUNCTIONS (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
VDDD_DREG	2		SN75DP130SS: Digital voltage regulator decoupling; install 1µF to GND. SN75DP130DS: Treat same as VDDD; this pin will be most noisy of all VDDD terminals and needs a de-coupling capacitor nearby.
GND	18, 24, 31, and Exposed Thermal Pad		Ground. Reference GND connections include the device package exposed thermal pad.
NC	SN75DP130SS 7, 15, 21, 37, 40, 43, 46		No Connect. These terminals may be left unconnected, or connect to GND.
	SN75DP130DS 7, 40, 46		

DP130 POWER SEQUENCING

The following power-up and power-down sequences describe how the RSTN signal is applied to the SN75DP130.

Power-Up Sequence:

1. Assert RSTN and de-assert EN to the device.
2. Apply V_{cc} with less than a 10-ms ramp time for the DP130SS and for the DP130DS, apply V_{ddd} then V_{cc} (both having less than 10-ms ramp time) devices. V_{ddd} must be asserted first and stable for greater than 10 µs before V_{cc} is applied.
3. RSTN must remain asserted until V_{cc}/V_{ddd} voltage has reached minimum recommended operation for more than 100 µs.
4. De-assert RSTN (Note: This RSTN is a 1.05-V interface and is internally connected to V_{ddd_dreg} through a 150-kΩ resistor).
5. Assert EN a minimum of 10 µs after RSTN has been de-asserted.
6. Device will be available for operation approximately 400 ms after a valid reset.

Power-Down Sequence:

1. De-assert EN to the device.
2. Assert RSTN to the device.
3. Remove V_{cc} and V_{ddd}.

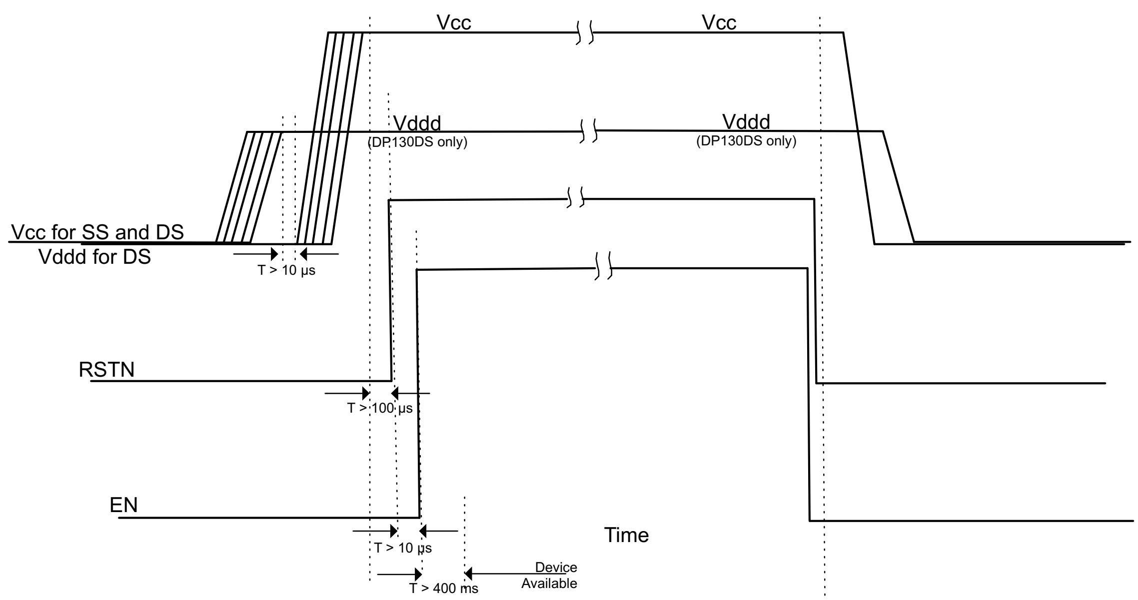

Figure 5. Power-Up and Power-Down Sequence

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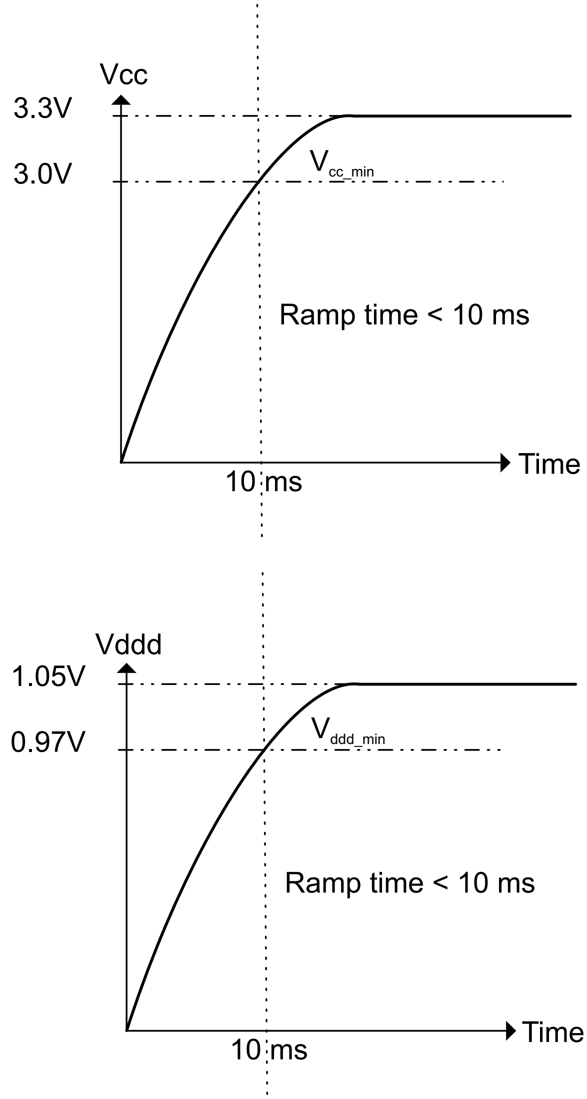

Figure 6. V_{CC}/V_{ddd} Ramp Recommendation

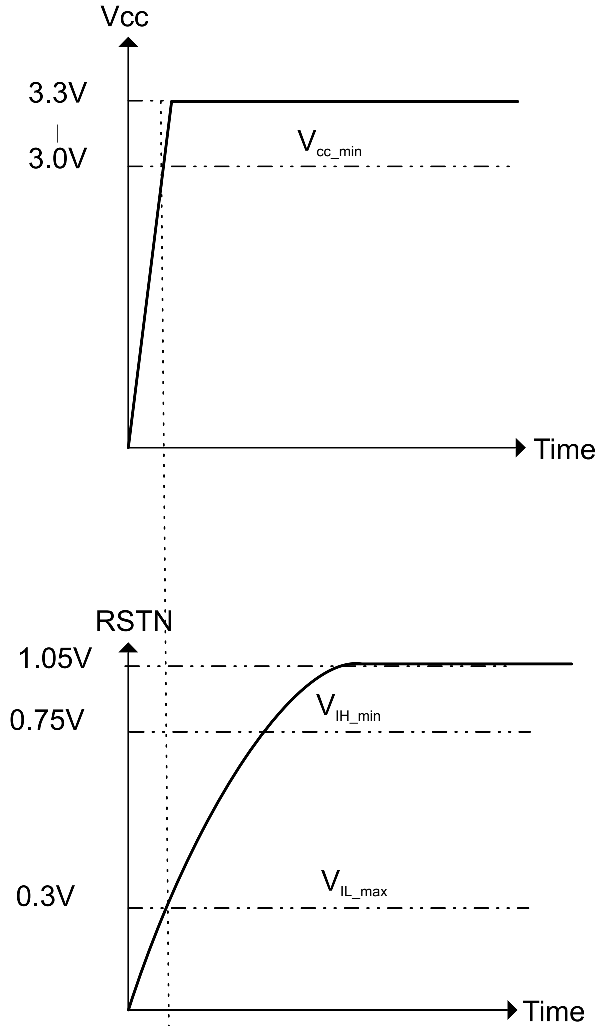

Figure 7. RSTN Voltage Thresholds

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ORDERING INFORMATION[(1)]

PART NUMBER	PART MARKING	PACKAGE
SN75DP130DSRGZR	DP130DS	48-pin QFN reel
SN75DP130SSRGZR	DP130SS	48-pin QFN reel
SN75DP130DSRGZT	DP130DS	48-pin QFN small quantity tape
SN75DP130SSRGZT	DP130SS	48-pin QFN small quantity tape

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) [(1)]

			VALUE	UNIT
Supply voltage range	V_{CC}		–0.3 to 4.0	V
	V_{DDD}, V_{DDD_DREG}		–0.3 to 1.3	V
Voltage range	Main link I/O differential voltage		–0.3 to 1.3	V
	HPD_SNK		–0.3 to 5.5	V
	All other terminals		–0.3 to 4	V
Storage temperature	T_S		–65 to 150	°C
Electrostatic discharge	Human Body Model[(2)]	Main Link I/O, AUX_SNK, HPD_SNK, CAD_SNK	±2	kV
		All Other Terminals	±2	kV
	Charged-device model[(3)]		±500	V

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Tested in accordance with JEDEC Standard 22, Test Method A114-B
(3) Tested in accordance with JEDEC Standard 22, Test Method C101-A

THERMAL INFORMATION

THERMAL METRIC[(1)]		SN75DP130	UNITS
		QFN (48) PINS	
θ_{JA}	Junction-to-ambient thermal resistance	35.1	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	21.5	
θ_{JB}	Junction-to-board thermal resistance	11.7	
ψ_{JT}	Junction-to-top characterization parameter, high-k board	1.2	
ψ_{JB}	Junction-to-board characterization parameter, high-k board	11.9	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	6.7	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

POWER DISSIPATION

PARAMETER		TEST CONDITIONS(1)	MIN	TYP	MAX	UNIT
P_N	Device power under normal operation	SN75DP130SS; 4 DP Lanes.		468	828	mW
		SN75DP130DS; 4 DP Lanes.		174	304	mW
		SN75DP130SS; 2 DP Lanes		252	450	mW
		SN75DP130DS; 2 DP Lanes.		102	178	mW
		SN75DP130SS; 1 DP Lanes		144	252	mW
		SN75DP130DS; 1 DP Lanes.		66	112	mW
P_{SD}	Shutdown mode power dissipation	SN75DP130SS; 4 DP Lanes.			14.4	mW
		SN75DP130DS; 4 DP Lanes.			7.2	mW
P_{SBY}	Standby mode power dissipation	SN75DP130SS; 4 DP Lanes.			14.4	mW
		SN75DP130DS; 4 DP Lanes.			7.2	mW
P_{D3}	D3 power down mode dissipation	SN75DP130SS; 4 DP Lanes.			54	mW
		SN75DP130DS; 4 DP Lanes.			46	mW
P_{OD}	Output disable (squelch) mode current	SN75DP130SS; 4 DP Lanes.		126	180	mW
		SN75DP130DS; 4 DP Lanes.		58	88	mW

(1) Test conditions correspond to Power Supply test conditions in Electrical Characteristics

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RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3	3.3	3.6	V
V_{DDD}	Digital core and Main Link supply voltage		0.97	1.05	1.2	V
T_A	Operating free-air temperature		0		85	°C
T_{CASE}	Case temperature				103.1	°C
$V_{IH(HPD)}$	High-level input voltage HPD_SNK		1.9		5.5	V
V_{IH}	High-level input voltage for device control signals		1.9		3.6	V
		RSTN pin (typical hysteresis of 80mV)		0.75		
V_{IL}	Low-level input voltage for device control signals		0		0.8	V
		RSTN pin (typical hysteresis of 80mV)		0.30		
MAIN LINK TERMINALS						
V_{ID}	Peak-to-peak input differential voltage; RBR, HBR, HBR2		0.30		1.40	Vpp
d_R	Data rate				5.4	Gbps
C_{AC}	AC coupling capacitance (each input and each output line)		75		200	nF
R_{tdiff}	Differential output termination resistance		80	100	120	Ω
V_{Oterm}	Output termination voltage (AC coupled)		0		2	V
$t_{SK(in\ HBR2)}$	Intra-pair skew at the input at 5.4Gbps	When used as re-driver in DP source			20	ps
		When used as receiver equalizer in DP sink			100	
$t_{SK(in\ HBR)}$	Intra-pair skew at the input at 2.7Gbps				100	ps
$t_{SK(in\ RBR)}$	Intra-pair skew at the input at 1.62Gbps				300	ps
AUX CHANNEL DATA TERMINALS						
$V_{I\text{-}DC}$	DC input voltage	AUX_SRCp and AUX_SNKp in DP mode	-0.5	0.3	0.4	V
		AUX_SRCn and AUX_SNKn in DP mode	2.0	3.0	3.6	
		AUX_SRCp/n and AUX_SNKp/n in TMDS mode	-0.5		3.6	
V_{ID}	Differential input voltage amplitude (DP mode only)		300		1400	mV_{PP}
$d_{R(AUX)}$	Data rate (before Manchester encoding)		0.8	1	1.2	Mbps
$d_{R(FAUX)}$	Data rate Fast AUX (300ppm frequency tolerance)			720		Mbps
t_{jccin_adj}	Cycle-to-cycle AUX input jitter adjacent cycle (DP mode only)				0.05	UI
t_{jccin}	Cycle-to-cycle AUX input jitter within one cycle (DP mode only)				0.1	UI
C_{AC}	AUX AC coupling capacitance (DP mode only)		75		200	nF
V_{srcCMM}	AUX source common mode voltage (only applies to DP mode) CAD = V_{IL}; measured on AUX source and sink before AC coupling caps		0		2000	mV
DDC AND I²C TERMINALS						
V_I	Input voltage		-0.5		3.6	V
d_R	Data rate				100	kbps
V_{IH}	High-level input voltage		$0.7V_{CC}$			V
V_{IL}	Low-level input voltage				$0.3V_{CC}$	V
f_{SCL}	SCL clock frequency standard I²C mode				100	kHz
$t_{w(L)}$	SCL clock low period standard I²C mode		4.7			µs
$t_{w(H)}$	SCL clock high period standard I²C mode		4.0			µs
C_{bus}	Total capacitive load for each bus line				400	pF

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POWER SUPPLY ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER[(1)]		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{CCDP1HBR2}$	Supply Current 1 DP Lanes	Maximum conditions: IN/OUT at 5.4Gbps PRBS,V_{OD} = 510mVpp, P_E = 6dB; AUX at 1Mbps PRBS, V_{ID} = 1000mVpp; EQ = 3dB Typical Conditions: IN/OUT at 5.4Gbps PRBS,V_{OD} = 510mVpp, P_E = 0dB AUX and I^2C Idle; EQ = 3dB		40	70	mA
$I_{CCDP2HBR2}$	Supply Current 2 DP Lanes			70	125	mA
$I_{CCDP4HBR2}$	Supply Current 4 DP Lanes			130	230	mA
$I_{CCDP1HBR}$	Supply Current 1 DP Lanes	Main Link at 2.7Gbps PRBS, V_{OD} =510mVpp, P_E = 0dB; AUX and I^2C Idle; EQ at 3dB fixed gain		40		mA
$I_{CCDP2HBR}$	Supply Current 2 DP Lanes			70		mA
$I_{CCDP4HBR}$	Supply Current 4 DP Lanes			130		mA
I_{CCTMDS}	Supply Current TMDS Mode	Main Link at 2.5Gbps PRBS, V_{ID} = V_{OD} = 600mVpp; AUX Idle			170	mA
I_{SD}	Shutdown supply current	Shutdown mode		3	4	mA
I_{SBY}	Standby supply current	Standby mode		3	4	mA
I_{D3}	D3 supply current	D3 power down mode		10	15	mA
I_{OD}	Squelch supply current	Output disable (Squelch) mode		35	50	mA

(1) Values are V_{DDD} supply measurements; V_{CC} supply (DS package option) measurements are 5mA (typical) and 8mA (max), with zero current in shutdown and standby modes.

MAIN LINK ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OD(L0)}$	Output differential voltage swing	$V_{PRE(L0)}$; 675Mbps D10.2 Test Pattern; BOOST=01	238	340	442	mV_{PP}
$V_{OD(L1)}$			357	510	663	mV_{PP}
$V_{OD(L2)}$			484	690	897	mV_{PP}
$V_{OD(L3)}$			700	1000	1300	mV_{PP}
$V_{OD(TMDS)}$		675Mbps D10.2 Test Pattern; BOOST=01	420	600	780	mV_{PP}
$\Delta V_{OD(L0L1)}$	Output peak-to-peak differential voltage delta	$\Delta V_{ODn} = 20\times\log(V_{ODL(n+1)} / V_{ODL(n)})$ measured in compliance with PHY CTS1.1D15 section 3.2 at test point TP2 using special CTS test board	1.7	3.5	5.3	dB
$\Delta V_{OD(L1L2)}$			1.6	2.5	3.5	dB
$\Delta V_{OD(L2L3)}$			0.8	3.5	6.0	dB
$V_{PRE(L0)}$	Driver output pre-emphasis (default)	All V_{OD} options		0	0.25	dB
$V_{PRE(L1)}$		V_{OD} = $V_{OD(L0)}$, $V_{OD(L1)}$, or $V_{OD(L2)}$; BOOST=01		3.5		dB
$V_{PRE(L2)}$		V_{OD} = $V_{OD(L0)}$ or $V_{OD(L1)}$; BOOST=01		6.0		dB
$V_{PRE(L3)}$		V_{OD} = $V_{OD(L0)}$; BOOST=01		9.5		dB
$V_{PRE(BOOST)}$	Output V_{PRE} boost	BOOST=10		10%		dB
		BOOST=00		–10%		dB
$\Delta V_{PRE(L1L0)}$	Pre-emphasis delta	Measured in compliance with PHY CTS1.1D15 section 3.3 at test point TP2 using special CTS test board	2.0			dB
$\Delta V_{PRE(L2L1)}$			1.6			dB
$\Delta V_{PRE(L3L2)}$			1.6			dB
$\Delta V_{ConsBit}$	Non-transition bit voltage variation	See CTS spec section 3.3.5			30%	
$A_{EQ(HBR)}$	Equalizer gain for RBR/HBR	See Table 5 and for EQ setting details; Max value represents the typical value for the maximum configurable EQ setting			9	dB
$A_{EQ(HBR2)}$	Equalizer gain for HBR2				18	dB
$A_{EQ(TMDS)}$	Equalizer gain for TMDS				3	dB
R_{OUT}	Driver output impedance			50		Ω
R_{IN}	Input termination impedance		40	50	60	Ω
V_{Iterm}	Input termination voltage	AC coupled; self-biased	0		2	V
$V_{OCM(SS)}$	Steady state output common-mode voltage		0		2	V

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MAIN LINK ELECTRICAL CHARACTERISTICS (continued)

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\Delta V_{OCM(SS)}$	Change in steady state output common-mode voltage between logic levels	Tested in compliance to section 3.10 in CTS 1.1a		10		mV_{PP}
$V_{OCM(PP)}$	Output common-mode noise	HBR2		20		mV_{RMS}
				30		mV_{RMS}
$V_{SQUELCH}$	Squelch threshold voltage	Programable via I^2C; default at 80mVpp typical		80		mV_{PP}
$I_{TXSHORT}$	Short circuit current limit	Main Link outputs shorted to GND			50	mA

MAIN LINK SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PD}	Propagation delay time	See Figure 8		300		ps
$t_{SK(1)}$	Intra-pair output skew	Signal input skew = 0ps; d_R = 2.7Gbps, V_{PRE} = 0dB, 800mVp-p, D10.2 clock pattern at device input; See Figure 9			20	ps
$t_{SK(2)}$	Inter-pair output skew				100	ps
Δt_{jit}	Total peak-to-peak residual jitter	$V_{OD(L0)}$; $V_{PRE(L0)}$; EQ = 8dB; clean source; minimum input and output cabling; 1.62Gbps, 2.7Gbps, and 5.4Gbps PRBS7 data pattern.			15	ps
t_{sq_enter}	Squelch entry time	Time from active DP signal turned off to ML output off with noise floor minimized	10		120	μs
t_{sq_exit}	Squelch exit time	Time from DP signal on to ML output on	0		1	μs

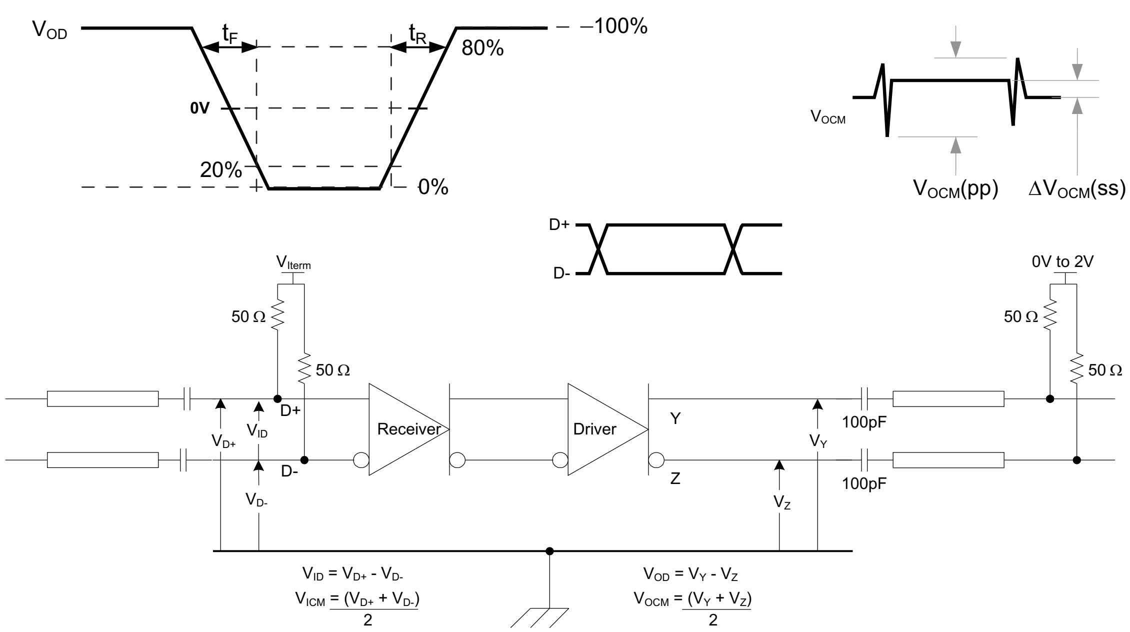

Figure 8. Main Link Test Circuit

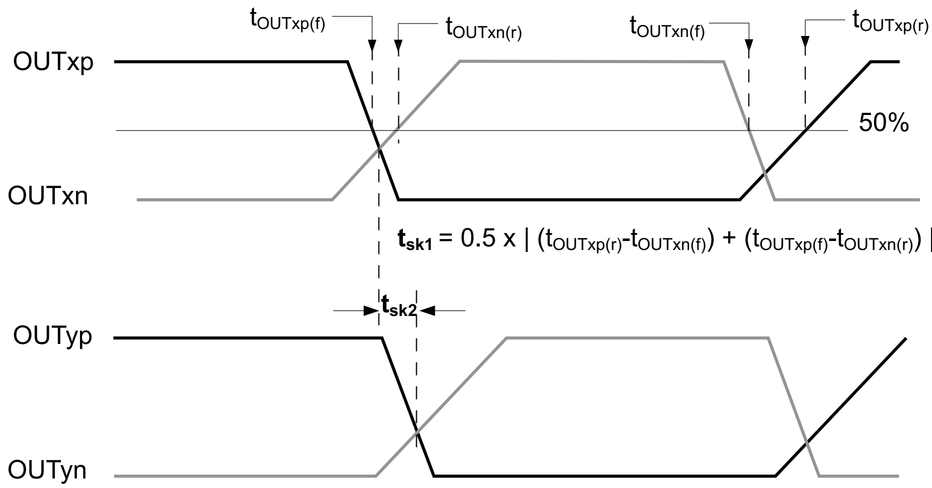

Figure 9. Main Link Skew Measurements

HPD/CAD ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
HPD_SRC, CAD_SRC						
V_{OH}	High-level output voltage	I_{OH} = 500µA	2.7		3.6	V
V_{OL}	Low-level output voltage	I_{OH} = 500µA	0		0.1	V
R_{outCAD}	CAD series output resistance (1)	EN=RSTN=V_{CC}; HPD_SNK=CAD_SNK=V_{CC}		150		Ω
R_{outHPD}	HPD series output resistance	EN=RSTN=V_{CC}; HPD_SNK=CAD_SNK=V_{CC}		150		Ω
I_{LEAK}	Leakage current (2)	V_{CC}= 0V, V(pin) = 1.2V; RSTN			20	µA
		V_{CC}= 0V, V(pin) = 3.3V; SCL/SDA_CTL, AUX_SNKp/n			20	
		V_{CC}= 0V, V(pin) = 3.3V; HPD_SNK			40	
		V_{CC}= 0V, V(pin) = 3.3V; AUX_SRCp/n			60	
HPD_SNK						
I_H	High-level input current	V_{IH} = 1.9V (leakage includes the 130kΩ pull-down resistor)	–30		30	µA
I_L	Low-level input current	V_{IL} = 0.8V (leakage includes the 130kΩ pull-down resistor)	–30		30	µA
V_{TH+}	Positive going input threshold voltage			1.4		V
R_{pdHPD}	HPD input termination to GND	V_{CC}=0V	100	130	160	kΩ
CAD_SNK						
I_H	High-level input current	V_{IH} = 1.9V	–1		1	µA
I_L	Low-level input current	V_{IL} = 0.8V	–1		1	µA
V_{TH+}	Positive going input threshold voltage			1.4		V

(1) A series output resistance of 100kΩ may be added in series to the CAD_SRC output to mimic a cable adapter.
(2) Applies to failsafe inputs: RSTN, SDA_CTL, SCL_CTL, SDA_DDC, SCL_DDC, AUX_SNK P/N, AUX_SRC P/N, HPD_SNK

HPD/CAD SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PD(HPD)}$	Propagation delay HPD_SNK to HPD_SRC	V_{CC} = 3.0V; See Figure 11			50	ns
$t_{PD(CAD)}$	Propagation delay CAD_SNK to CAD_SRC				50	ns
$t_{T(HPD)}$	HPD logic shut off time	V_{CC} = 3.0V; See Figure 12			400	ms

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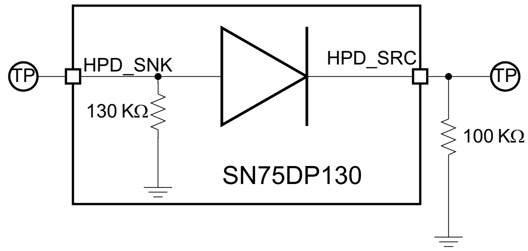

Figure 10. HPD Test Circuit

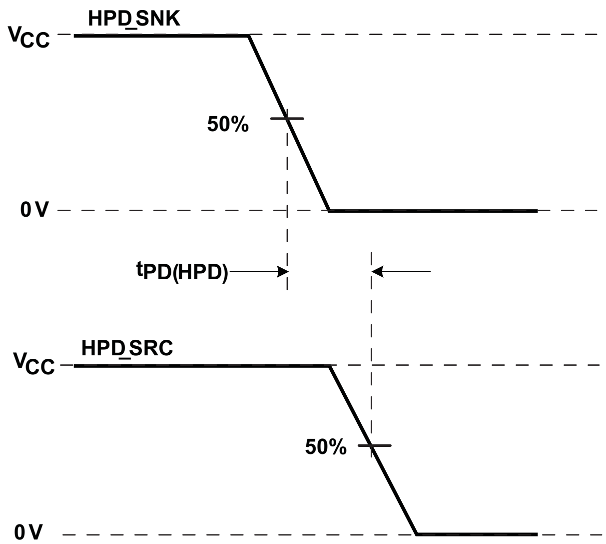

Figure 11. HPD Timing Diagram 1

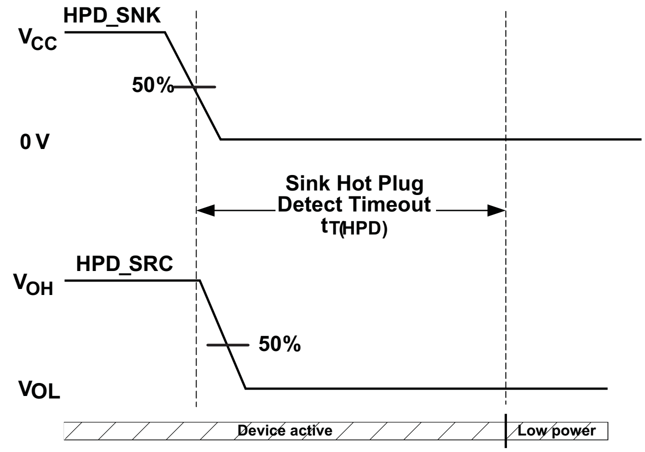

Figure 12. HPD Timing Diagram 2

AUX/DDC/I²C ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{PASS}	DDC mode passthrough voltage	$V_{CAD\_SNK} = V_{IH}$; I_O = 100 µA	1.9			V
C_{IO}	I/O capacitance	V_{IO} = 0 V; f(test) = 1 MHz		10		pF
r_{ON}	On resistance AUX_SRCn to AUX_SNKn in DP mode	V_{CC} = 3.0 V w/ V_I =2.85V or V_{CC} = 3.6 V w/ V_I = 3.4 V; I_O = 5 mA		5	10	Ω
	On resistance SCL/SDA_DDC to AUX_SNK in TMDS mode	I_O = 3 mA		15	30	Ω
	On resistance AUX_SRC to AUX_SNK in TMDS mode	I_O = 3 mA		10	20	Ω
Δr_{ON}	On resistance variation with input signal voltage change in DP mode	V_{CC} = 3.6 V, I_O = 5 mA, V_I = 2.6 to 3.4 V, V_{CC} = 3.0 V, I_O = 5 mA, V_I = 0 to 0.4 V			5	Ω
$V_{ID(HYS)}$	Differential input hysterisis	By design (simulation only)		50		mV
I_H	High-level input current	$V_I = V_{CC}$	-5		5	µA
I_L	Low-level input current	V_I = GND; CAD_SNK = V_{IH}	-5		5	µA
		V_I = GND; At DDC inputs			80	
V_{AUX+}	Voltage on the Aux+ for PHY-CTS 3.19	1M (5%) pullup to V_{CC} and 100kΩ pulldown to GND on AUX+; V_{CC} = 3.3 V	0		0.4	V
V_{AUX-}	Voltage on the Aux- for PHY-CTS 3.18	100kΩ pullup to V_{CC} and 1M (5%) pulldown to GND on AUX-; V_{CC} = 3.3 V	2.4		3.6	V
$\lvert S_{1122} \rvert$	Differential line insertion loss	V_{ID} = 400 mV, AC coupled; p-channel biasing 0.3 V and n-channel 3.0V; 360 MHz sine wave; CAD_SNK=V_{IL}		1.6	3	dB
R_{DDC}	Switcheable pul-lup resistor on DDC at source side (SCL_DDC, SDA_DDC)	CAD_SNK = V_{IH}	48	60	72	kΩ

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AUX/DDC/I²C SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{sk(AUX)}$	Intra-pair skew	V_{ID} = 400 mV, AC coupled; p-channel biasing 0.3V and n-channel 3.0V; See Figure 13			400	ps
$t_{PLH(DP)}$	Propagation delay time, low to high	CAD = V_{IL}; 1Mbps pattern;See Figure 14			3	ns
$t_{PHL(DP)}$	Propagation delay time, high to low				3	ns
$t_{PLH(DDC)}$	Propagation delay time, low to high	CAD = V_{IH}; 100kbps pattern			50	ns
$t_{PHL(DDC)}$	Propagation delay time, high to low				50	ns
$t_{PU(AUX)}$	Main Link D3 wakeup time	V_{ID} = 0.1 V, V_{ICMM} = 2 V source side (before AC coupling caps)			50	µs
I²C						
Refer to the I²C-Bus Specification, Version 2.1 (January 2000); SN75DP130 meets the switching characteristics for standard mode transfers up to 100 kbps.						

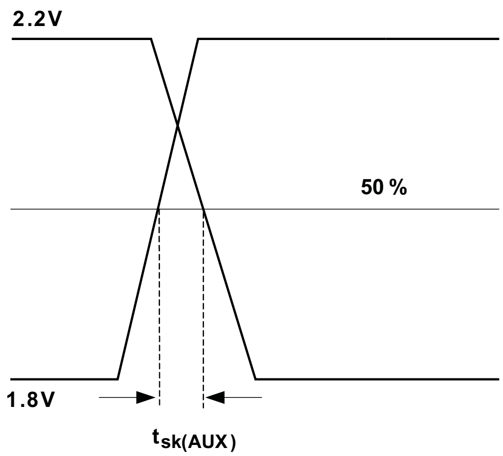

Figure 13. AUX Skew Measurement

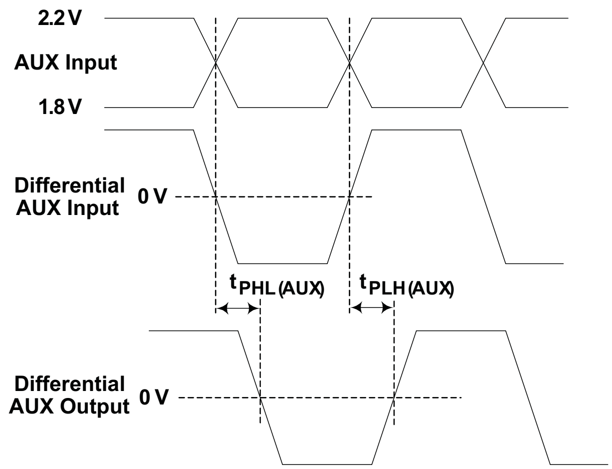

Figure 14. AUX Delay Measurement

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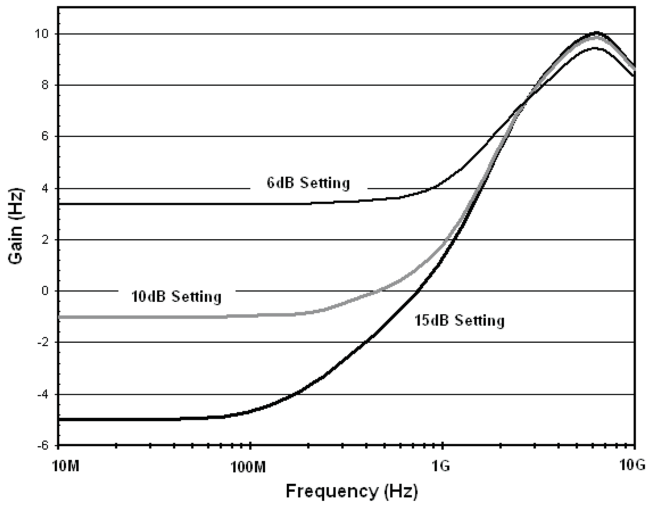
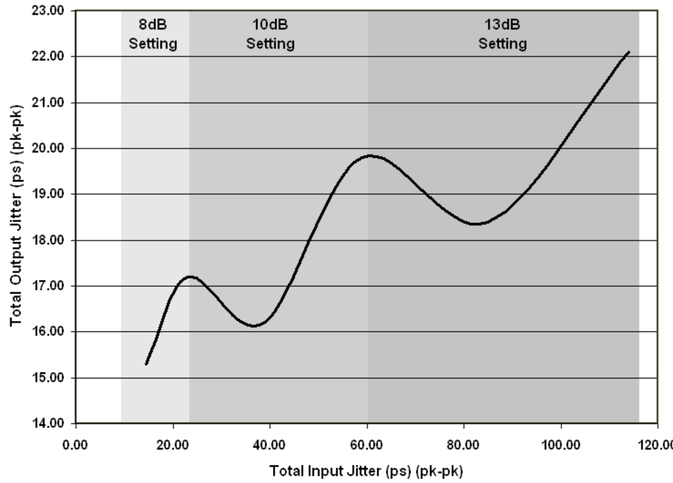
TYPICAL CHARACTERISTICS



A. Gain represents SN75DP130 design simulation

Figure 15. Typical EQ Gain Curves



A. DisplayPort output jitter measured at the surface mount pins connected to the main link output channels on the SN75DP130 characterization test board; input jitter generated from test board with variable input trace lengths using 4 mil traces of lengths 2 inches to 22 inches generating the typical input jitter as represented in Table 1.

Figure 16. DisplayPort Sink Jitter Performance with Optimal EQ Settings

Table 1. Characterization Test Board Trace Lengths Related to Input Jitter

INPUT MODE	TRACE LENGTH (inches)	TOTAL INPUT JITTER (ps)	RECOMMENDED EQ SETTING
Display Port HBR2	2	14.4	8
	6	23.1	8
	10	38.8	10
	14	58.9	10
	18	84.8	13
	22	113.9	13
TMDS 3.4 Gbps	2	15.8	6
	6	21.3	6
	10	33.2	6
	14	49.9	13
	18	70.5	13
	22	91.5	13

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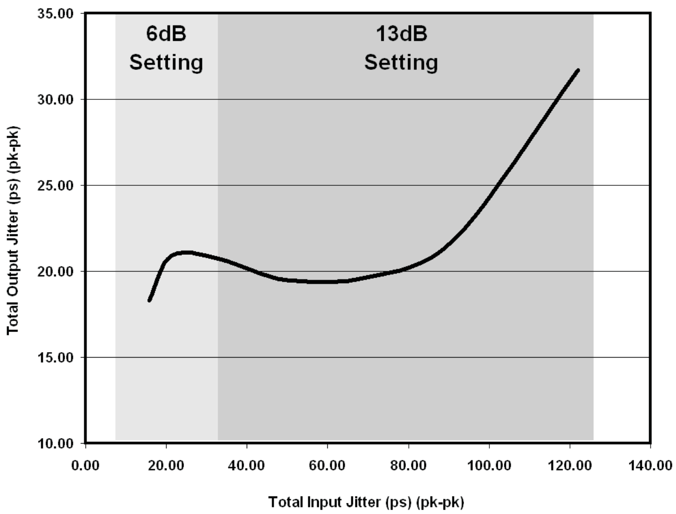

A. DisplayPort output jitter measured at the surface mount pins connected to the main link output channels on the SN75DP130 characterization test board; input jitter generated from test board with variable input trace lengths using 4 mil traces of lengths 2 inches to 22 inches generating the typical input jitter as represented in Table 1.

Figure 17. TMDS Sink jitter Performance with Optimal EQ Settings

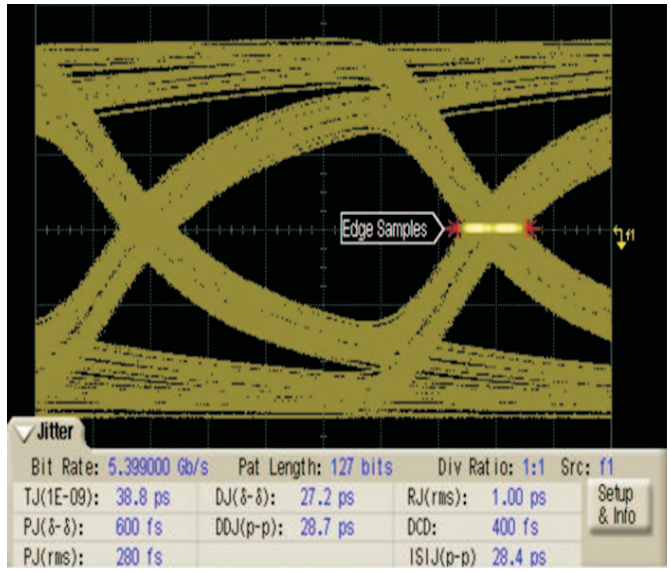

Figure 18. Main Link Input with 10 inch Trace; DisplayPort Sink

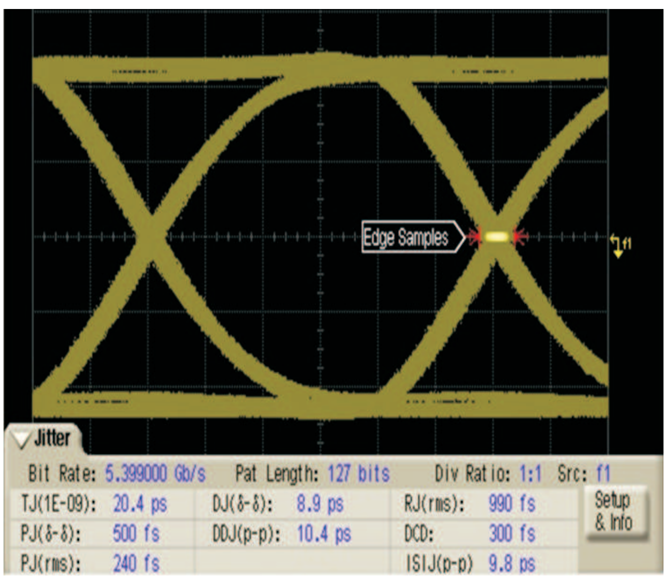

Figure 19. SN75DP130 Output; 10 inch Input Trace; 13dB EQ Setting; DP Sink

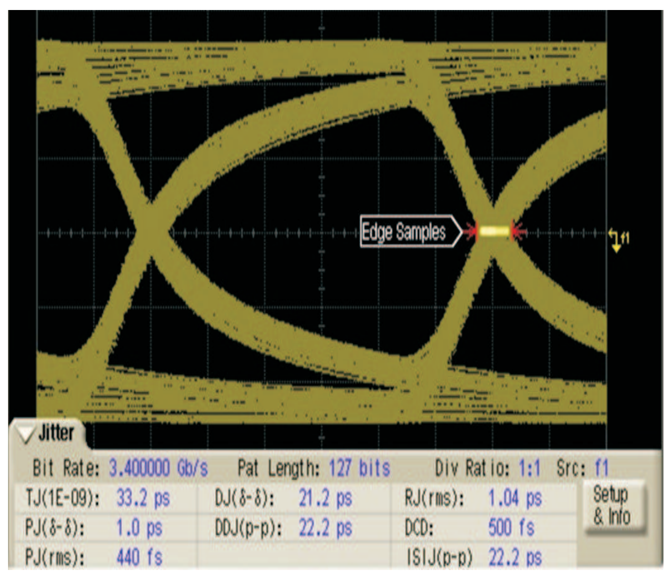

Figure 20. Main Link Input with 10 inch Trace; TMDS Sink

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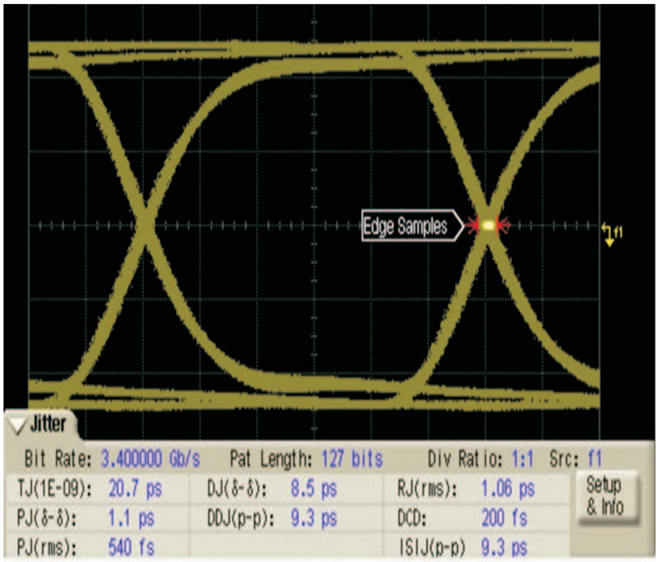

Figure 21. SN75DP130 Output; 10 inch Input Trace; 13dB EQ Setting; TMDS Sink

APPLICATION INFORMATION

ADDITIONAL TYPICAL IMPLEMENTATIONS

Theconfiguration shown in Figure 22 is preferred to avoid very long AUX signal stub lines. Furthermore, this configuration provides isolation between the DP connector and the GPU.

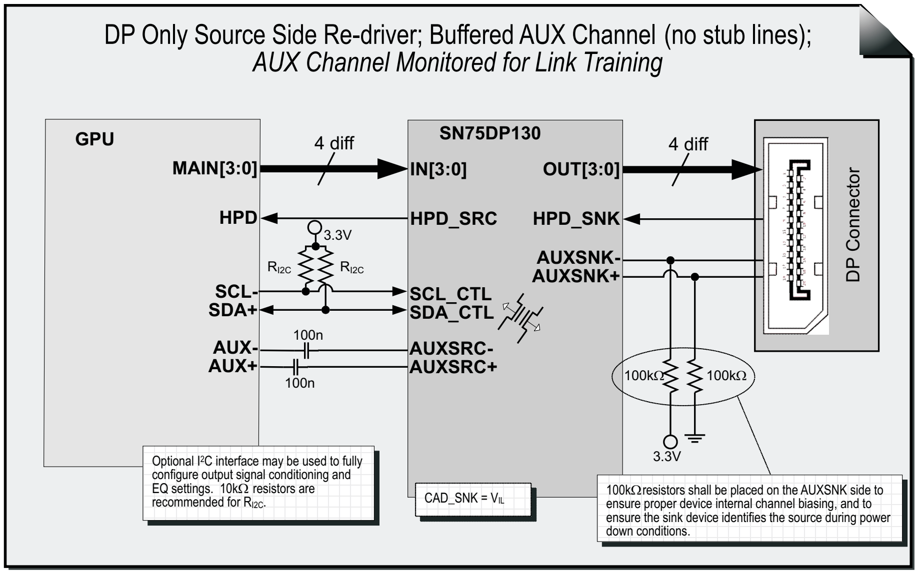

Figure 22. DP Only Configuration with AUX Pass Through

The configuration shown in Figure 23 enables the SN75DP130 in DP++ Dual-Mode with the AUX input only monitoring the AUX channel. Use this setting when AUX stub lines can be kept short and minimum AUX attenuation is desired. For DP v1.1a, the stub length shall not exceed 4cm each, and for DP v1.2 with FAUX support each stub line shall be shorter than 1cm.

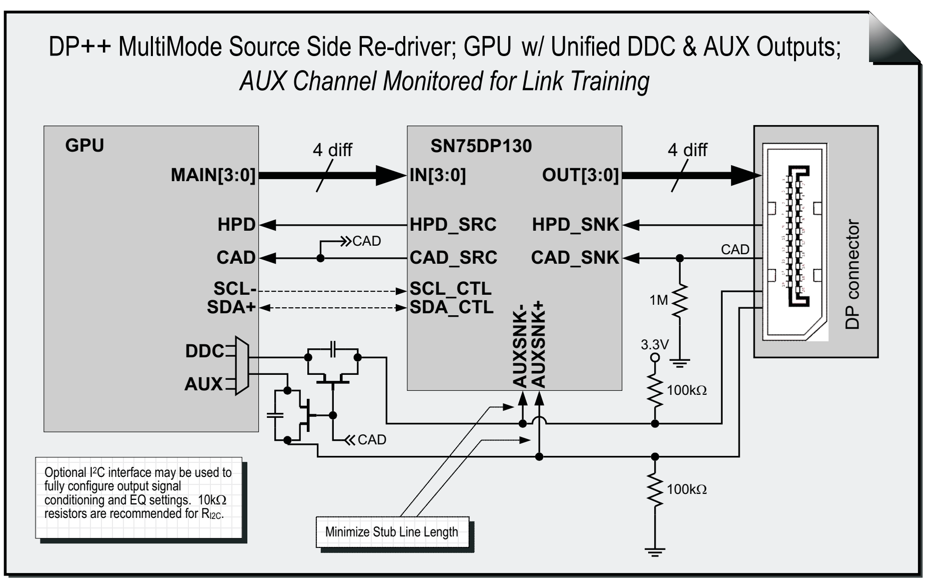

Figure 23. DP++ Dual-Mode Configuration with AUX Monitor

The alternate configuration shown in Figure 24 allows a reduced BOM by eliminating the need for external FET switches while routing AUX and DDC externally, which eliminates any insertion loss cases of AUX is brought through the SN75DP130. For DP v1.2 with FAUX support each stub line shall be shorter than 1cm.

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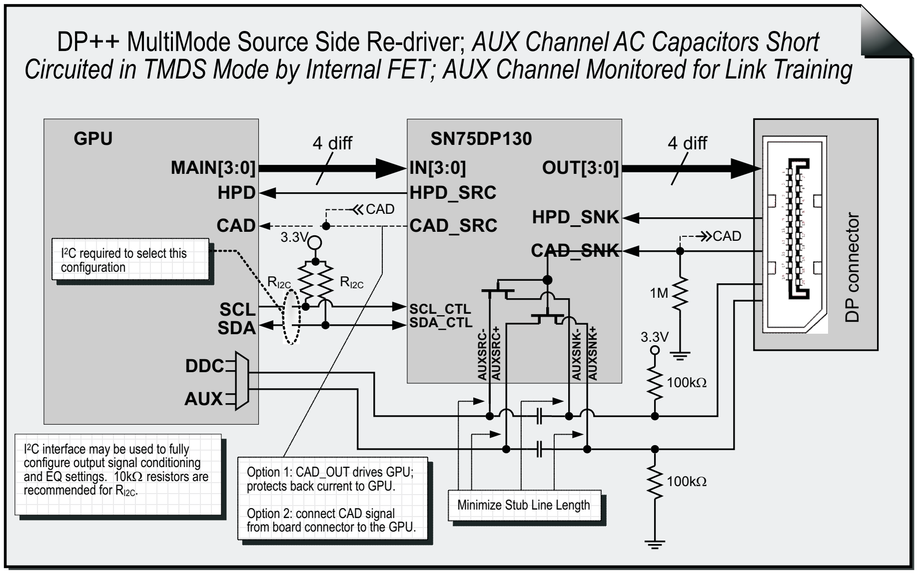

Figure 24. Alternate Low-BOM DP++ Dual-Mode Configuration

OPERATING MODES OVERVIEW

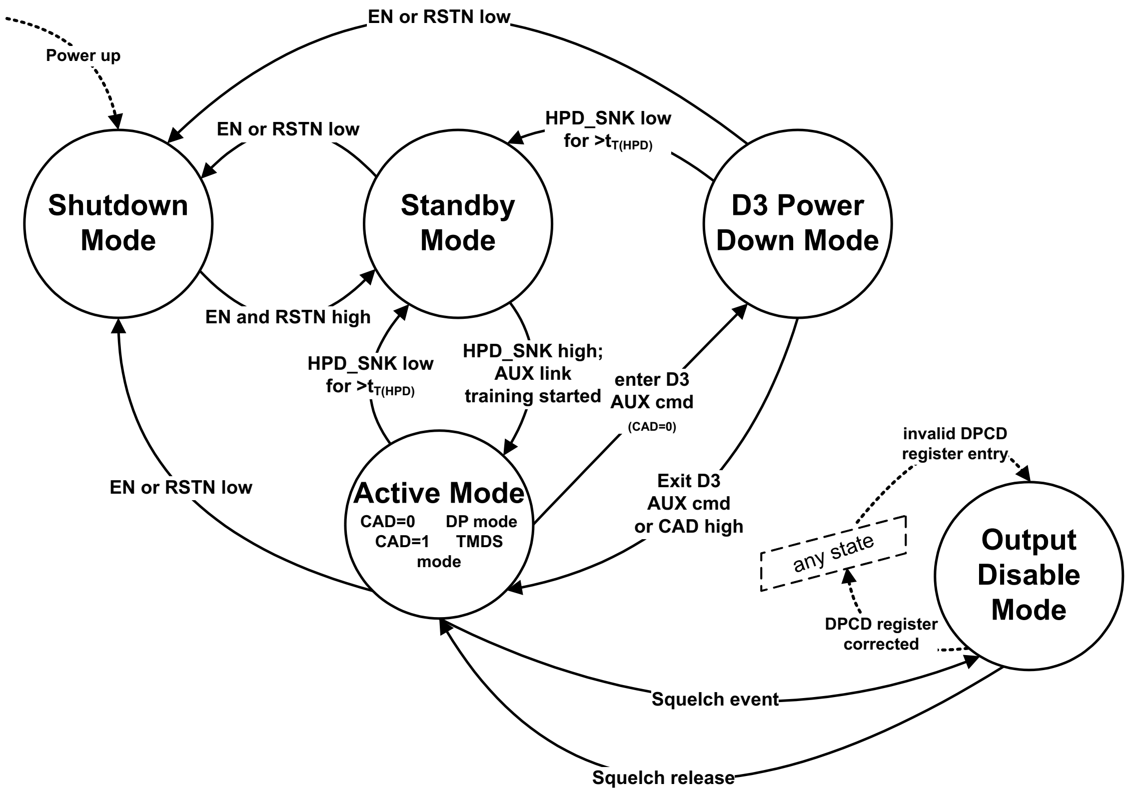

Figure 25. SN75DP130 Operating Modes Flow Diagram

Table 2. Description of SN75DP130 Operating Modes

MODE	CHARACTERISTICS	CONDITIONS
Shutdown Mode	Least amount of power consumption (most circuitry turned off); HPD_SRC reflects HPD_SNK state; all other outputs are high-impedance; if RSTN is high local I^{2}C IF remains active; if RSTN is low local I^{2}C interface is turned off, all other inputs are ignored, and AUX DPCD is reset. (EN=low does not reset DPCD)	EN or RSTN is low; Power on default mode
Standby Mode	Low power consumption (I^{2}C IF is active; AUX monitor is inactive); Main Link outputs are disabled;	EN and RSTN are high; HPD_SNK low longer than $t_{T(HPD)}$
D3 Power Down Mode	Low power consumption (I^{2}C IF is active; AUX monitor active in DP mode); Main Link outputs are disabled;	EN and RSTN are high; AUX cmd requested DP sink to enter D3 power saving mode
Active Mode	Data transfer (normal operation); The device is either in TMDS mode (CAD_SNK=high) or DP mode (CAD_SNK=low); In DP mode, the AUX monitor is actively monitoring for Link Training; the output signal swing and input equalization setting depend on the Link Training or I^{2}C settings; the AUX SRC channel is active; the AUX SNK and DDC are active unless disabled through I^{2}C IF. At power-up all Main Link outputs are disabled by default. AUX Link Training is necessary to overwrite the DPCD registers to enable Main Link outputs. In TMDS mode the output signal swing is 600mVpp unless this setting is adjusted by overwriting according registers through I^{2}C IF. Transactions on the AUX lines will be ignored.	EN and RSTN are high; HPD_SNK is high; HPD_SNK can also be low for less than $t_{Z(HPD)}$ (e.g., sink interrupt request to source)
Compliance Test Mode	Through I^{2}C registers the device can be forced into ignoring HPD_SNK and CAD_SNK, HPD_SRC and CAD_SRC are programmable; output swing, pre-emphasis and EQ setting are programmable; automatic power down features can be disabled	EN and RSTN is high; I^{2}C selects HPD and/or CAD test mode
Output Disable Mode	DPCD write commands on the AUX bus detected by the SN75DP130 will also write to the local DPCD register. The DPCD register should always be written with a valid entry. If register 101h or 103h is written with a forbidden value, the SN75DP130 disables the Main Link output signals, forcing the DP sink to issue an interrupt. The DP source can now re-train the link using valued DPCD register values. As soon as all DPCD registers contain a valid entry, the SN75DP130 switches back into the appropriate mode of operation.	EN and RSTN are high; DPCD register 101h or 103h entry is invalid

Table 3. Description of Operating Mode Transitions

MODE TRANSITION	USE CASE	TRANSITION SPECIFICS
Shutdown → Standby	Activate SN75DP130	EN and RSTN both transitioned high
Standby → Active	Turn on Main Link (DP sink plugged in)	HPD_SNK input asserts high
Active → D3 Power Down	DP source requests temporary power down for power savings	Receive D3 entry command on AUX
Active → Output Disable	Squelch event; inactive video stream	Main Link monitor detects the inactive video stream
D3 Power Down → Active	Exit temporary power down	Receive D3 exit command on AUX, or CAD_SNK input is asserted (high)
D3 Power Down → Standby	Exit temporary power down (DP sink unplugged)	HPD_SNK de-asserted to low for longer than $t_{T(HPD)}$
Active → Standby	Turn off Main Link (DP sink unplugged)	HPD_SNK de-asserted to low for longer than $t_{T(HPD)}$
Any → Shutdown	Turn off SN75DP130	EN or RSTN transitions low
Any → Output Disable	DPCD register access error condition	Invalid DPCD register access
Output Disable → Active	Squelch released; video stream re-activated	Main Link monitor detects active video stream
Output Disable → Any	DPCD register error condition is corrected	Appropriate operating mode is re-entered

IMPLEMENTING THE RSTN SIGNAL

The SN75DP130 RSTN input gives control over the device reset and to place the device into shut-down mode. When RSTN is low, all DPCD registers are reset to their default values, and all Main Link lanes are disabled. When the RSTN input returns to a high logic level, the device comes out of the Shutdown mode. To turn on the Main Link, it is necessary to either program the DPCD registers through the local I^{2}C interface or to go through a full sequence of Link Training between DP source and DP sink.

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It is critical to reset the digital logic of the SN75DP130 after the V_{DDD} supply is stable (i.e., V_{DDD} has reached the minimum recommended operating voltage). This is achieved by asserting the RSTN input from low to high. A system may provide a control signal to the RSTN signal that transitions low to high after the V_{DDD} supply is stable, or implement an external capacitor connected between RSTN and GND, to allow delaying the RSTN signal during power up. The implementations are shown in Figure 26 and Figure 27.

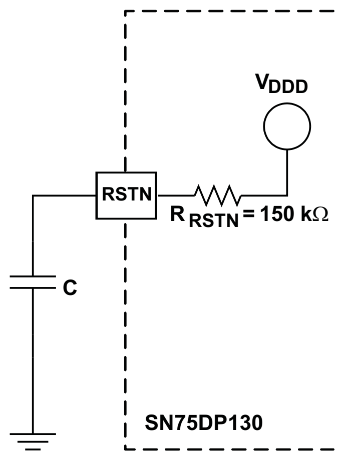

Figure 26. External Capacitor Controlled RSTN

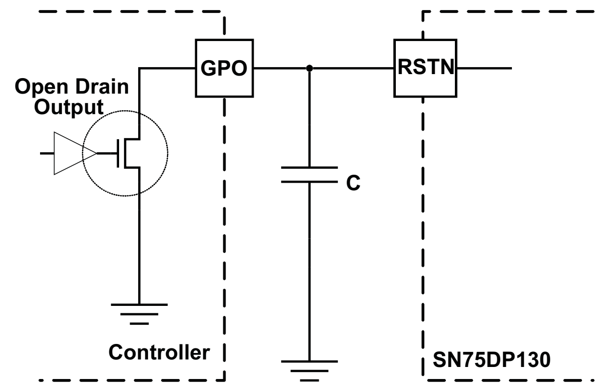

Figure 27. RSTN Input from Active Controller

When implementing the external capacitor, the size of the external capacitor depends on the power up ramp of the V_{DDD} supply where a slower ramp-up results in a larger value external capacitor.

Refer to the latest reference schematic for the SN75DP130 device and/or consider approximately 200nF capacitor as a reasonable first estimate for the size of the external capacitor.

When implementing a RSTN input from an active controller, it is recommended to use an open drain driver if the RSTN input is driven. This protects the RSTN input from damage of an input voltage greater than V_{DDD}.

HOT PLUG DETECT (HPD) AND CAD DESCRIPTION

The SN75DP130 generates the Hot Plug Detect (HPD_SRC) signal to indicate to the source that a sink has been detected. A low HPD_SNK signal input indicates no sink device is connected. When HPD_SNK is high, the CAD_SNK signal indicates whether a DP sink (CAD_SNK=low) or a TMDS sink (CAD_SNK=high).

A sink device can request a source device interrupt by pulling the HPD_SNK signal low for a duration of 0.5ms to 1.0ms. The interrupt passes through the SN75DP130. If the HPD_SNK signal goes low for longer than 2ms, the DP source determines that the sink device is disconnected. To conserve power, the SN75DP130 will go into a power saving Standby mode after the HPD signal went low for a duration of $t_{T(HPD)}$.

In the TMDS mode the AUX training logic is disabled and the Main Link transmits with a fixed output voltage swing of 600mVpp; the pre-emphasis level is set to 0dB. Output swing and pre-emphasis level are also adjustable by I^2C IF. In TMDS mode all four Main Link output lanes are enabled.

Through the local I^2C interface it is also possible to force the device to ignore HPD_SNK and CAD_SNK, and control HPD_SRC and CAD_SRC directly.

AUX AND DDC CONFIGURATION DETAILS

The SN75DP130 offers an AUX source channel (AUX_SRC), AUX sink channel (AUX_SNK), a selectable DDC interface (SDA_DDC/SCL_DDC) for TMDS mode, and a local I^2C control interface (SCL_CTL / SDA_CTL). Upon power-up, the SN75DP130 enables the connection between the AUX_SNK to the appropriate source interface based on CAD_SNK. Table 4 describes the switching logic, including the programmability through the local I^2C interface.

Note that the DDC interface incorporates 60kΩ pull-up resistors on SDA_DDC and SCL_DDC which are turned on when CAD_SNK is high (TMDS mode) but turned off when CAD_SNK is low (DP mode).

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Table 4. AUX and DDC Interface Configurations

HPD_SNK	I²C REGISTER BIT 04.0	I²C REGISTER BIT 04.1	CAD_SNK	AUX_SNK	AUX_SRC	DDC	AUX MONITOR	COMMENT
0	X	X	X	OFF	OFF	OFF	inactive	no sink detected; low power mode
1	0 (default; works for Intel, NVIDIA, and AMD)	0 (default)	0	ON	ON	OFF	active	DP sink detected; AUX_SNK connects to AUX_SRC
			1	ON	OFF	ON	inactive	TMDS cable adapter detected; DDC connects to AUX_SNK
	1 (NVIDIA, AMD special mode)		0	OFF	ON	OFF	active	DP sink detected; AUX_SNK disconnected from AUX_SRC; AUX_SNK monitors AUX training
			1	ON	ON	OFF	inactive	TMDS cable adapter detected; AUX_SNK connects to AUX_SRC and can be used to short AC coupling caps
	0	1	0	ON	ON	OFF	active	DP sink detected; AUX_SNK connects to AUX_SRC
			1				inactive	TMDS cable adapter detected; AUX_SRC connects to AUX_SNK
	1		undetermined					mode not recommended

MAIN LINK EQ CONFIGURATION DETAILS

The EQ input stage is self-configuring based on Link Training. A variety of EQ settings are available through external pin configuration to accommodate for different PCB loss and GPU settings, and the I²C interface may be utilized to fully customize EQ configuration lane-by-lane beyond the input pin configurability options, as described in Table 5.

Table 5. Main Link EQ Configurations

EQ_I2C_ENABLE (reg 05.7)	ADDR_EQ	CAD_SNK(1) VIL = DP VIH = TMDS	LINK TRAINING ON/OFF (reg 04.2)	LINK TRAINING AEQ(Lx)(2) LANE 0 to 2	LINK TRAINING AEQ(Lx)(2) LANE 3	DESCRIPTION
0 (default)	VIL	VIL	1 (default)	AEQ(L0) = 8dB at 2.7GHz AEQ(L1) = 6dB at 2.7GHz AEQ(L2) = 3.5dB at 2.7GHz AEQ(L3) = 0dB at 2.7GHz	same as Lane 0 to 2	automatic low-range EQ gain based on link training; DP mode
			0	AEQ(Lx) = 6dB at 2.7GHz		DP mode; fixed EQ
		VIH	x	EQ(Lx) = 6dB at 2.7GHz	3dB at 1.35GHz	TMDS mode; fixed EQ
	VIM	VIL	1	AEQ(Lx) = 8dB at 2.7GHz	same as Lane 0 to 2	DP mode; fixed EQ
			0	AEQ(Lx) = 8dB at 2.7GHz		DP mode; fixed EQ
		VIH	x	EQ(Lx) = 8dB at 2.7GHz	3dB at 1.35GHz	TMDS mode; fixed EQ
	VIH	VIL	1	AEQ(L0) = 15dB at 2.7GHz AEQ(L1) = 13dB at 2.7GHz AEQ(L2) = 10dB at 2.7GHz AEQ(L3) = 6dB at 2.7GHz	same as Lane 0 to 2	automatic high-range EQ gain based on link training; DP mode
			0	AEQ(Lx) = 13dB at 2.7GHz		DP mode; fixed EQ
		VIH	x	EQ(Lx) = 13dB at 2.7GHz	3dB at 1.35GHz	TMDS mode; fixed EQ
1	x	VIL	1	AEQ(Lx) = 0dB at 2.7GHz AEQ(Lx) I²C programmable	same as Lane 0 to 2	DP mode; EQ fully programmable for each training level; EQ disabled by default
			0	AEQ(L1) = 0dB at 2.7GHz AEQ(L1) I²C programmable		DP mode; EQ fully programmable by AEQ(L1) levels; default AEQ(L1) EQ setting at 6dB At 2.7GHz
		VIH	x		3dB at 1.35GHz	TMDS mode; fixed EQ

(1) Setting CAD_TEST_MODE (Reg 17.0) forces the SN75DP130 into a TMDS test mode even if no external CAD signal is present
(2) EQ setting is adjusted based on the output pre-emphasis level setting; the EQ setting is indifferent to the level of V_{OD}.

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LINK TRAINING AND DPCD DESCRIPTION

The SN75DP130 monitors the auxiliary interface access to DisplayPort Configuration Data (DPCD) registers during Link Training in DP mode to select the output voltage swing V_{OD}, output pre-emphasis, and the EQ setting of the Main Link. The AUX monitor for SN75DP130 supports Link Training in 1Mbps Manchester mode, and is disabled during TMDS mode (CAD_SNK=VIH).

The AUX channel is further monitored for the DisplayPort D3 standby command.

The DPCD registers monitored by SN75DP130 are listed in Table 6. Bit fields not listed are reserved and values written to reserved fields are ignored.

Table 6. DPCD Registers Utilized by the SN75DP130 AUX Monitor

ADDRESS	NAME	DESCRIPTION
00100h	LINK_BW_SET	Bits 7:0 = Link Bandwidth Setting Write Values: 06h – 1.62 Gbps per lane 0Ah – 2.7 Gbps per lane (default) 14h – 5.4 Gbps per lane *Note: any other value is reserved; the SN75DP130 will revert to 5.4 Gbps operation when any other value is written* Read Values: 00h – 1.62 Gbps per lane 01h – 2.7 Gbps per lane (default) 02h – 5.4 Gbps per lane
00101h	LANE_COUNT_SET	Bits 4:0 = Lane Count Write Values: 00h – All lanes disabled (default) 01h – One lane enabled 02h – Two lanes enabled 04h – Four lanes enabled *Note: any other value is invalid and disables all Main Link output lanes* Read Values: 00h – All lanes disabled (default) 01h – One lane enabled 03h – Two lanes enabled 0Fh – Four lanes enabled
00103h	TRAINING_LANE0_SET	Write Values: Bits 1:0 = Output Voltage V_{OD} Level 00 – Voltage swing level 0 (default) 01 – Voltage swing level 1 10 – Voltage swing level 2 11 – Voltage swing level 3 Bits 4:3 = Pre-emphasis Level 00 – Pre-emphasis level 0 (default) 01 – Pre-emphasis level 1 10 – Pre-emphasis level 2 11 – Pre-emphasis level 3 *Note: the following combinations are not allowed for bits [1:0]/[4:3]: 01/11, 10/10, 10/11, 11/01, 11/10, 11/11; setting to any of these invalid combinations disables all Main Link lanes until the register value is changed back to a valid entry* Read Values: Bits 1:0 = Output Voltage V_{OD} Level 00 – Voltage swing level 0 (default) 01 – Voltage swing level 1 10 – Voltage swing level 2 11 – Voltage swing level 3 Bits 3:2 = Pre-emphasis Level 00 – Pre-emphasis level 0 (default) 01 – Pre-emphasis level 1 10 – Pre-emphasis level 2 11 – Pre-emphasis level 3
00104h	TRAINING_LANE1_SET	Sets the V_{OD} and pre-emphasis levels for lane 1
00105h	TRAINING_LANE2_SET	Sets the V_{OD} and pre-emphasis levels for lane 2
00106h	TRAINING_LANE3_SET	Sets the V_{OD} and pre-emphasis levels for lane 3

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Table 6. DPCD Registers Utilized by the SN75DP130 AUX Monitor (continued)

ADDRESS	NAME	DESCRIPTION
0010F	TRAINING_LANE0_1_SET2	Write Values: Bits 1:0 = Lane 0 Post Cursor 2 00 – IN0 expects post cursor2 level 0; OUT0 transmits at post cursor 2 level 0 01 – IN0 expects post cursor2 level 1; OUT0 transmits at post cursor 2 level 0 10 – IN0 expects post cursor2 level 2; OUT0 transmits at post cursor 2 level 0 11 – IN0 expects post cursor2 level 3; OUT0 transmits at post cursor 2 level 0 Bits 5:4 = Lane 1 Post Cursor 2 00 – IN1 expects post cursor2 level 0; OUT1 transmits at post cursor 2 level 0 01 – IN1 expects post cursor2 level 1; OUT1 transmits at post cursor 2 level 0 10 – IN1 expects post cursor2 level 2; OUT1 transmits at post cursor 2 level 0 11 – IN1 expects post cursor2 level 3; OUT1 transmits at post cursor 2 level 0 Read Values: Bits 1:0 = Lane 0 Post Cursor 2 00 – IN0 expects post cursor2 level 0; OUT0 transmits at post cursor 2 level 0 01 – IN0 expects post cursor2 level 1; OUT0 transmits at post cursor 2 level 0 10 – IN0 expects post cursor2 level 2; OUT0 transmits at post cursor 2 level 0 11 – IN0 expects post cursor2 level 3; OUT0 transmits at post cursor 2 level 0 Bits 3:2 = Lane 1 Post Cursor 2 00 – IN1 expects post cursor2 level 0; OUT1 transmits at post cursor 2 level 0 01 – IN1 expects post cursor2 level 1; OUT1 transmits at post cursor 2 level 0 10 – IN1 expects post cursor2 level 2; OUT1 transmits at post cursor 2 level 0 11 – IN1 expects post cursor2 level 3; OUT1 transmits at post cursor 2 level 0
0110F	TRAINING_LANE2_3_SET2	Bit definition identical to that of TRAINING_LANE_0_1_SET2 but for lanes 2 (IN2/OUT2) and lane 3 (IN3/OUT3)
00600h	SET_POWER	Bits 1:0 = Power Mode Write Values: 01 – Normal mode (default) 10 – Power down mode; D3 Standby Mode The Main Link and all analog circuits are shut down and the AUX channel is monitored during the D3 Standby Mode. The device exits D3 Standby Mode by access to this register, when CAD_SNK goes high, or if DP_HPD_SNK goes low for longer than $t_{T(HPD)}$, which indicates that the DP sink was disconnected, or that the PRIORITY control has selected the HDMI/DVI sink. *Note: setting the register to the invalid combination 0600h[1:0] = 00 or 11 is ignored by the device and the device remains in normal mode* Read Values: 00 – Normal mode (default) 01 – Power-down mode; D3 Standby Mode

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I²C INTERFACE OVERVIEW

The SN75DP130 I²C interface is enabled when EN and RSTN are input high. The SCL_CTL and SDA_CTL terminals are used for I²C clock and I²C data respectively. The SN75DP130 I²C interface conforms to the two-wire serial interface defined by the I²C Bus Specification, Version 2.1 (January 2000), and supports the standard mode transfer up to 100 kbps.

The device address byte is the first byte received following the START condition from the master device. The 7 bit device address for SN75DP130 is factory preset to 01011xx with the two least significant bits being determined by the ADDR_EQ 3-level control input. Table 7 clarifies the SN75DP130 target address.

Table 7. SN75DP130 I²C Target Address Description

SN75DP130 I²C TARGET ADDRESS							
BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (W/R)
0	1	0	1	1	ADDR1	ADDR0	0/1

Note: ADDR_EQ = LOW: ADDR[1:0] = 00: W/R=58/59
ADDR_EQ = V_{CC}/2: ADDR[1:0] = 01: W/R=5A/5B;
ADDR_EQ = HIGH: ADDR[1:0] = 10: W/R=5C/5D

The following procedure is followed to write to the SN75DP130 I²C registers:

1. The master initiates a write operation by generating a start condition (S), followed by the SN75DP130 7-bit address and a zero-value "W/R" bit to indicate a write cycle
2. The SN75DP130 acknowledges the address cycle
3. The master presents the sub-address (I²C register within SN75DP130) to be written, consisting of one byte of data, MSB-first
4. The SN75DP130 acknowledges the sub-address cycle
5. The master presents the first byte of data to be written to the I²C register
6. The SN75DP130 acknowledges the byte transfer
7. The master may continue presenting additional bytes of data to be written, with each byte transfer completing with an acknowledge from the SN75DP130
8. The master terminates the write operation by generating a stop condition (P)

The following procedure is followed to read the SN75DP130 I²C registers:

1. The master initiates a read operation by generating a start condition (S), followed by the SN75DP130 7-bit address and a one-value "W/R" bit to indicate a read cycle
2. The SN75DP130 acknowledges the address cycle
3. The SN75DP130 transmit the contents of the memory registers MSB-first starting at register 00h.
4. The SN75DP130 will wait for either an acknowledge (ACK) or a not-acknowledge (NACK) from the master after each byte transfer; the I²C master acknowledges reception of each data byte transfer
5. If an ACK is received, the SN75DP130 transmits the next byte of data
6. The master terminates the read operation by generating a stop condition (P)

   Note that no sub-addressing is included for the read procedure, and reads start at register offset 00h and continue byte by byte through the registers until the I²C master terminates the read operation.

Refer to Table 8 for SN75DP130 local I²C register descriptions. Reads from reserved fields not described return zeros, and writes are ignored.

Table 8. SN75DP130 Local I2C Control and Status Registers

ADDRESS	BIT(S)	DESCRIPTION	ACCESS(1)
01h	1	AUTO_POWERDOWN_DISABLE 0 – The SN75DP130 automatically enters Standby mode based on HPD_SNK (default) 1 – The SN75DP130 will not automatically enter Standby mode	RW
	0	FORCE_SHUTDOWN_MODE 0 – SN75DP130 is forced to Shutdown mode 1 – Shutdown mode is determined by EN input, normal operation (default)	RW
02h	7:0	TI_TEST. This field defaults to zero value, and should not be modified.	RW
03h	5:4	SQUELCH_SENSITIVITY. Main Link squelch sensitivity is selected by this field, and determines the transitions to and from the Output Disable mode. 00 – Main Link IN0p/n squelch detection threshold set to 40mVpp 01 – Main Link IN0p/n squelch detection threshold set to 80mVpp (default) 10 – Main Link IN0p/n squelch detection threshold set to 160mVpp 11 – Main Link IN0p/n squelch detection threshold set to 250mVpp	RW
	3	SQUELCH_ENABLE 0 – Main Link IN0p/n squelch detection enabled (default) 1 – Main Link IN0p/n squelch detection disabled	RW
04h	3	TI_TEST. This field defaults to zero value, and should not be modified.	RW
	2	LINK_TRAINING_ENABLE 0 – Link Training is disabled. V_{OD} and Pre-emphasis are configured through the I2C register interface; the EQ is fixed when this bit is zero. 1 – Link Training is enabled (default)	RW
	1:0	AUX_DDC_MUX_CFG. See Table 3 for details on the programming of this field. 00 – AUX_SNK is switched to AUX_SRC for DDC source side based on CAD_SNK (default) 01 – AUX_SNK is switched to AUX_SRC based on the CAD_SNK input, and used to short circuit AC coupling capacitors in the TMDS operating mode. 10 – AUX_SNK is switched to AUX_SRC side based on the HPD_SNK inptu, while the DDC source interface remains disabled. 11 – Undefined operation	RW
05h	7	EQ_I2C_ENABLE 0 – EQ settings controlled by device inputs only (default) 1 – EQ settings controlled by I2C register settings	RW
	6:4	AEQ_L0_LANE0_SET. This field selects the EQ setting for Lane 0 when I2C_EQ_ENABLE is set, the DisplayPort sink is selected, Link Training is enabled, and the Link Training results in Level 0 pre-emphasis. 000 – 0 dB EQ gain (default); 100 – 5 dB (HBR); 10 dB (HBR2) 001 – 1.5 dB (HBR); 3.5 dB (HBR2); 101 – 6 dB (HBR); 13 dB (HBR2) 010 – 3 dB (HBR); 6 dB (HBR2); 110 – 7 dB (HBR); 15 dB (HBR2) 011 – 4 dB (HBR); 8 dB (HBR2); 111 – 9 dB (HBR); 18 dB (HBR2)	RW
	2:0	AEQ_L1_LANE0_SET. This field selects the EQ setting for Lane 0 when I2C_EQ_ENABLE is set, the DisplayPort sink is selected, Link Training is enabled, and the Link Training results in Level 1 pre-emphasis. This field also selects the fixed EQ setting for the following non-AEQ modes: • I2C_EQ_ENABLE is set, the DisplayPort sink is selected, and Link Training is disabled • I2C_EQ_ENABLE is set and the TMDS sink is selected. 000 – 0 dB EQ gain (default); 100 – 5 dB (HBR); 10 dB (HBR2) 001 – 1.5 dB (HBR); 3.5 dB (HBR2); 101 – 6 dB (HBR); 13 dB (HBR2) 010 – 3 dB (HBR); 6 dB (HBR2); 110 – 7 dB (HBR); 15 dB (HBR2) 011 – 4 dB (HBR); 8 dB (HBR2); 111 – 9 dB (HBR); 18 dB (HBR2)	RW

(1) RO = Read Only; RW = Read/Write; WO = Write Only (reads return undetermined values)

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Table 8. SN75DP130 Local I²C Control and Status Registers (continued)

ADDRESS	BIT(S)	DESCRIPTION	ACCESS(1)
06h	6:4	AEQ_L2_LANE0_SET. This field selects the EQ setting for Lane 0 when I2C_EQ_ENABLE is set, the DisplayPort sink is selected, Link Training is enabled, and the Link Training results in Level 2 pre-emphasis. 000 – 0 dB EQ gain (default) 100 – 5 dB (HBR); 10 dB (HBR2) 001 – 1.5 dB (HBR); 3.5 dB (HBR2) 101 – 6 dB (HBR); 13 dB (HBR2) 010 – 3 dB (HBR); 6 dB (HBR2) 110 – 7 dB (HBR); 15 dB (HBR2) 011 – 4 dB (HBR); 8 dB (HBR2) 111 – 9 dB (HBR); 18 dB (HBR2)	RW
	2:0	AEQ_L3_LANE0_SET. This field selects the EQ setting for Lane 0 when I2C_EQ_ENABLE is set, the DisplayPort sink is selected, Link Training is enabled, and the Link Training results in Level 3 pre-emphasis. 000 – 0 dB EQ gain (default) 100 – 5 dB (HBR); 10 dB (HBR2) 001 – 1.5 dB (HBR); 3.5 dB (HBR2) 101 – 6 dB (HBR); 13 dB (HBR2) 010 – 3 dB (HBR); 6 dB (HBR2) 110 – 7 dB (HBR); 15 dB (HBR2) 011 – 4 dB (HBR); 8 dB (HBR2) 111 – 9 dB (HBR); 18 dB (HBR2)	RW
07h	6:4	AEQ_L0_LANE1_SET. This field selects the EQ setting for Lane 1 when I2C_EQ_ENABLE is set, the DisplayPort sink is selected, Link Training is enabled, and the Link Training results in Level 0 pre-emphasis. 000 – 0 dB EQ gain (default) 100 – 5 dB (HBR); 10 dB (HBR2) 001 – 1.5 dB (HBR); 3.5 dB (HBR2) 101 – 6 dB (HBR); 13 dB (HBR2) 010 – 3 dB (HBR); 6 dB (HBR2) 110 – 7 dB (HBR); 15 dB (HBR2) 011 – 4 dB (HBR); 8 dB (HBR2) 111 – 9 dB (HBR); 18 dB (HBR2)	RW
	2:0	AEQ_L1_LANE1_SET. This field selects the EQ setting for Lane 1 when I2C_EQ_ENABLE is set, the DisplayPort sink is selected, Link Training is enabled, and the Link Training results in Level 1 pre-emphasis. This field also selects the fixed EQ setting for the following non-AEQ modes: • I2C_EQ_ENABLE is set, the DisplayPort sink is selected, and Link Training is disabled • I2C_EQ_ENABLE is set and the TMDS sink is selected. 000 – 0 dB EQ gain (default) 100 – 5 dB (HBR); 10 dB (HBR2) 001 – 1.5 dB (HBR); 3.5 dB (HBR2) 101 – 6 dB (HBR); 13 dB (HBR2) 010 – 3 dB (HBR); 6 dB (HBR2) 110 – 7 dB (HBR); 15 dB (HBR2) 011 – 4 dB (HBR); 8 dB (HBR2) 111 – 9 dB (HBR); 18 dB (HBR2)	RW
08h	6:4	AEQ_L2_LANE1_SET. This field selects the EQ setting for Lane 1 when I2C_EQ_ENABLE is set, the DisplayPort sink is selected, Link Training is enabled, and the Link Training results in Level 2 pre-emphasis. 000 – 0 dB EQ gain (default) 100 – 5 dB (HBR); 10 dB (HBR2) 001 – 1.5 dB (HBR); 3.5 dB (HBR2) 101 – 6 dB (HBR); 13 dB (HBR2) 010 – 3 dB (HBR); 6 dB (HBR2) 110 – 7 dB (HBR); 15 dB (HBR2) 011 – 4 dB (HBR); 8 dB (HBR2) 111 – 9 dB (HBR); 18 dB (HBR2)	RW
	2:0	AEQ_L3_LANE1_SET. This field selects the EQ setting for Lane 1 when I2C_EQ_ENABLE is set, the DisplayPort sink is selected, Link Training is enabled, and the Link Training results in Level 3 pre-emphasis. 000 – 0 dB EQ gain (default) 100 – 5 dB (HBR); 10 dB (HBR2) 001 – 1.5 dB (HBR); 3.5 dB (HBR2) 101 – 6 dB (HBR); 13 dB (HBR2) 010 – 3 dB (HBR); 6 dB (HBR2) 110 – 7 dB (HBR); 15 dB (HBR2) 011 – 4 dB (HBR); 8 dB (HBR2) 111 – 9 dB (HBR); 18 dB (HBR2)	RW

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Table 8. SN75DP130 Local I²C Control and Status Registers (continued)

ADDRESS	BIT(S)	DESCRIPTION	ACCESS(1)
09h	6:4	AEQ_L0_LANE2_SET. This field selects the EQ setting for Lane 2 when I2C_EQ_ENABLE is set, the DisplayPort sink is selected, Link Training is enabled, and the Link Training results in Level 0 pre-emphasis. 000 – 0 dB EQ gain (default) 100 – 5 dB (HBR); 10 dB (HBR2) 001 – 1.5 dB (HBR); 3.5 dB (HBR2) 101 – 6 dB (HBR); 13 dB (HBR2) 010 – 3 dB (HBR); 6 dB (HBR2) 110 – 7 dB (HBR); 15 dB (HBR2) 011 – 4 dB (HBR); 8 dB (HBR2) 111 – 9 dB (HBR); 18 dB (HBR2)	RW
	2:0	AEQ_L1_LANE2_SET. This field selects the EQ setting for Lane 2 when I2C_EQ_ENABLE is set, the DisplayPort sink is selected, Link Training is enabled, and the Link Training results in Level 1 pre-emphasis. This field also selects the fixed EQ setting for the following non-AEQ modes: • I2C_EQ_ENABLE is set, the DisplayPort sink is selected, and Link Training is disabled • I2C_EQ_ENABLE is set and the TMDS sink is selected. 000 – 0 dB EQ gain (default) 100 – 5 dB (HBR); 10 dB (HBR2) 001 – 1.5 dB (HBR); 3.5 dB (HBR2) 101 – 6 dB (HBR); 13 dB (HBR2) 010 – 3 dB (HBR); 6 dB (HBR2) 110 – 7 dB (HBR); 15 dB (HBR2) 011 – 4 dB (HBR); 8 dB (HBR2) 111 – 9 dB (HBR); 18 dB (HBR2)	RW
0Ah	6:4	AEQ_L2_LANE2_SET. This field selects the EQ setting for Lane 2 when I2C_EQ_ENABLE is set, the DisplayPort sink is selected, Link Training is enabled, and the Link Training results in Level 2 pre-emphasis. 000 – 0 dB EQ gain (default) 100 – 5 dB (HBR); 10 dB (HBR2) 001 – 1.5 dB (HBR); 3.5 dB (HBR2) 101 – 6 dB (HBR); 13 dB (HBR2) 010 – 3 dB (HBR); 6 dB (HBR2) 110 – 7 dB (HBR); 15 dB (HBR2) 011 – 4 dB (HBR); 8 dB (HBR2) 111 – 9 dB (HBR); 18 dB (HBR2)	RW
	2:0	AEQ_L3_LANE2_SET. This field selects the EQ setting for Lane 2 when I2C_EQ_ENABLE is set, the DisplayPort sink is selected, Link Training is enabled, and the Link Training results in Level 3 pre-emphasis. 000 – 0 dB EQ gain (default) 100 – 5 dB (HBR); 10 dB (HBR2) 001 – 1.5 dB (HBR); 3.5 dB (HBR2) 101 – 6 dB (HBR); 13 dB (HBR2) 010 – 3 dB (HBR); 6 dB (HBR2) 110 – 7 dB (HBR); 15 dB (HBR2) 011 – 4 dB (HBR); 8 dB (HBR2) 111 – 9 dB (HBR); 18 dB (HBR2)	RW
0Bh	6:4	AEQ_L0_LANE3_SET. This field selects the EQ setting for Lane 3 when I2C_EQ_ENABLE is set, the DisplayPort sink is selected, Link Training is enabled, and the Link Training results in Level 0 pre-emphasis. 000 – 0 dB EQ gain (default) 100 – 5 dB (HBR); 10 dB (HBR2) 001 – 1.5 dB (HBR); 3.5 dB (HBR2) 101 – 6 dB (HBR); 13 dB (HBR2) 010 – 3 dB (HBR); 6 dB (HBR2) 110 – 7 dB (HBR); 15 dB (HBR2) 011 – 4 dB (HBR); 8 dB (HBR2) 111 – 9 dB (HBR); 18 dB (HBR2)	RW
	2:0	AEQ_L1_LANE3_SET. This field selects the EQ setting for Lane 3 when I2C_EQ_ENABLE is set, the DisplayPort sink is selected, Link Training is enabled, and the Link Training results in Level 1 pre-emphasis. This field also selects the fixed EQ setting for the following non-AEQ mode: • I2C_EQ_ENABLE is set, the DisplayPort sink is selected, and Link Training is disabled 000 – 0 dB EQ gain (default) 100 – 5 dB (HBR); 10 dB (HBR2) 001 – 1.5 dB (HBR); 3.5 dB (HBR2) 101 – 6 dB (HBR); 13 dB (HBR2) 010 – 3 dB (HBR); 6 dB (HBR2) 110 – 7 dB (HBR); 15 dB (HBR2) 011 – 4 dB (HBR); 8 dB (HBR2) 111 – 9 dB (HBR); 18 dB (HBR2)	RW

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Table 8. SN75DP130 Local I²C Control and Status Registers (continued)

ADDRESS	BIT(S)	DESCRIPTION	ACCESS(1)
0Ch	6:4	AEQ_L2_LANE3_SET. This field selects the EQ setting for Lane 3 when I2C_EQ_ENABLE is set, the DisplayPort sink is selected, Link Training is enabled, and the Link Training results in Level 2 pre-emphasis. 000 – 0 dB EQ gain (default); 100 – 5 dB (HBR); 10 dB (HBR2) 001 – 1.5 dB (HBR); 3.5 dB (HBR2); 101 – 6 dB (HBR); 13 dB (HBR2) 010 – 3 dB (HBR); 6 dB (HBR2); 110 – 7 dB (HBR); 15 dB (HBR2) 011 – 4 dB (HBR); 8 dB (HBR2); 111 – 9 dB (HBR); 18 dB (HBR2)	RW
	2:0	AEQ_L3_LANE3_SET. This field selects the EQ setting for Lane 3 when I2C_EQ_ENABLE is set, the DisplayPort sink is selected, Link Training is enabled, and the Link Training results in Level 3 pre-emphasis. 000 – 0 dB EQ gain (default); 100 – 5 dB (HBR); 10 dB (HBR2) 001 – 1.5 dB (HBR); 3.5 dB (HBR2); 101 – 6 dB (HBR); 13 dB (HBR2) 010 – 3 dB (HBR); 6 dB (HBR2); 110 – 7 dB (HBR); 15 dB (HBR2) 011 – 4 dB (HBR); 8 dB (HBR2); 111 – 9 dB (HBR); 18 dB (HBR2)	RW
15h	4:3	BOOST. Controls the output pre-emphasis amplitude when the DisplayPort sink is selected; allows to reduce or increase all pre-emphasis settings by ~10%. Setting this field will impact V_{OD} when pre-emphasis is disabled. This setting also impacts the output in TMDS mode for the DisplayPort sink connection when the DisplayPort sink CAD_SNK input is high. 00 – Pre-emphasis reduced by ~10%; V_{OD} reduced by 10% if pre-emphasis is disabled. 01 – Pre-emphasis nominal (default) 10 – Pre-emphasis increased by ~10%; V_{OD} increased by 10% if pre-emphasis is disabled. 11 – Reserved	RW
	2	DP_TMDS_VOD. Sets the target output swing in TMDS mode when the DisplayPort sink is selected, where CAD_SNK input is high. 0 – Low TMDS output swing (default) 1 – High TMDS output swing	RW
	1:0	DP_TMDS_VPRE. Controls the output pre-emphasis in TMDS mode when the DisplayPort sink is selected, where CAD_SNK input is high. 00 – No TMDS pre-emphasis(default) 01 – Low TMDS pre-emphasis 10 – High TMDS pre-emphasis 11 – Reserved	RW
17h	3	HPD_TEST_MODE 0 – Normal HPD mode. HPD_SRC reflects the status of HPD_SNK (default) 1 – Test mode. HPD_SNK is pulled high internally, and the HPD_SRC output is driven high and the Main Link is activated, depending on the squelch setting. This mode allows execution of 17h certain tests on SN75DP130 without a connected display sink.	RW
	1	CAD_OUTPUT_INVERT 0 – CAD_SRC output high means TMDS cable adapter detected (default) 1 – CAD_SRC output low means TMDS cable adapter detected	RW
	0	CAD_TEST_MODE 0 – Normal CAD mode. CAD_SRC reflects the status of CAD_SNK, based on the value of CAD_OUTPUT_INVERT (default) 1 – Test mode. CAD_SRC indicates TMDS mode, depending on the value of CAD_OUTPUT_INVERT; CAD_SNK input is ignored. This mode allows execution of certain tests on SN75DP130 without a connected TMDS display sink.	
18h – 1Ah	7:0	TI_TEST. These registers shall not be modified.	RW

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Table 8. SN75DP130 Local I^2C Control and Status Registers (continued)

ADDRESS	BIT(S)	DESCRIPTION	ACCESS(1)
1Bh	7	I2C_SOFT_RESET. Writing a one to this register resets all I^2C registers to default values. Writing a zero to this register has no effect. Reads from this register return zero.	WO
	6	DPCD_RESET. Writing a one to this register resets the DPCD register bits (corresponding to DPCD addresses 103h – 106h, the AEQ_Lx_LANEy_SET bits). Writing a zero to this register has no effect. Reads from this register return zero.	
1Ch	3:0	DPCD_ADDR_HIGH. This value maps to bits 19:16 of the 20-bit DPCD register address accessed through the DPCD_DATA register.	RW
1Dh	7:0	DPCD_ADDR_MID. This value maps to bits 15:8 of the 20-bit DPCD register address accessed through the DPCD_DATA register.	RW
1Eh	7:0	DPCD_ADDR_LOW. This value maps to bits 7:0 of the 20-bit DPCD register address accessed through the DPCD_DATA register.	RW
1Fh	7:0	DPCD_DATA. This register contains the data to write into or read from the DPCD register addressed by DPCD_ADDR_HIGH, DPCD_ADDR_MID, and DPCD_ADDR_LOW.	RW
20h	7:1	DEV_ID_REV. This field identifies the device and revision. 0000000 – SN75DP130 Revision 0	RO
	0	BIT_INVERT. The value read from this field is the inverse of that written. Default read value is zero.	RW
21h	7:0	TI_TEST. These registers shall not be modified.	RW
22h – 27h	7:0	TI_TEST_RESERVED. These read only registers are reserved for test; writes are ignored.	RO

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REVISION HISTORY

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
SN75DP130DSRGZR	ACTIVE	VQFN	RGZ	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
SN75DP130DSRGZT	ACTIVE	VQFN	RGZ	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
SN75DP130SSRGZR	ACTIVE	VQFN	RGZ	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
SN75DP130SSRGZT	ACTIVE	VQFN	RGZ	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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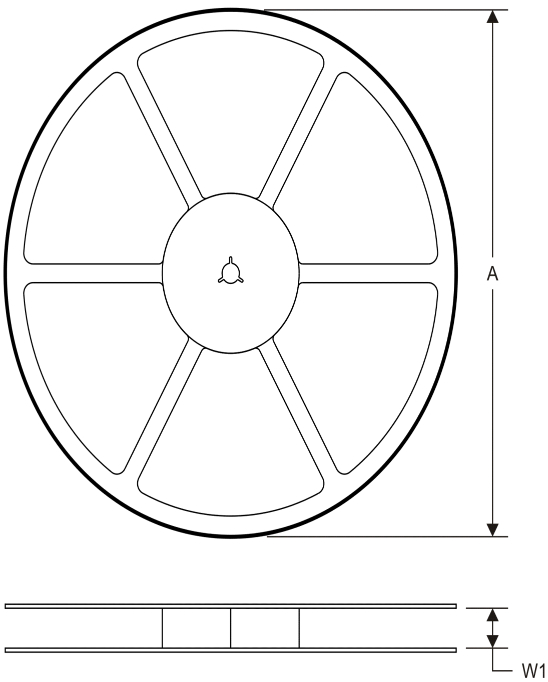
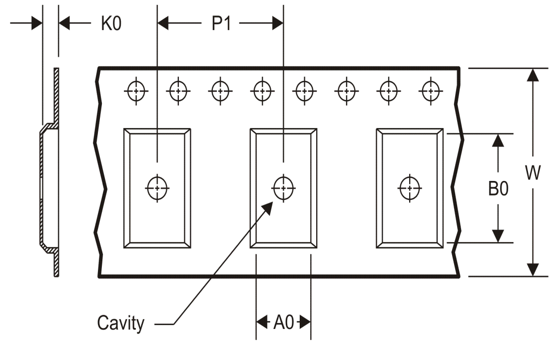
TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



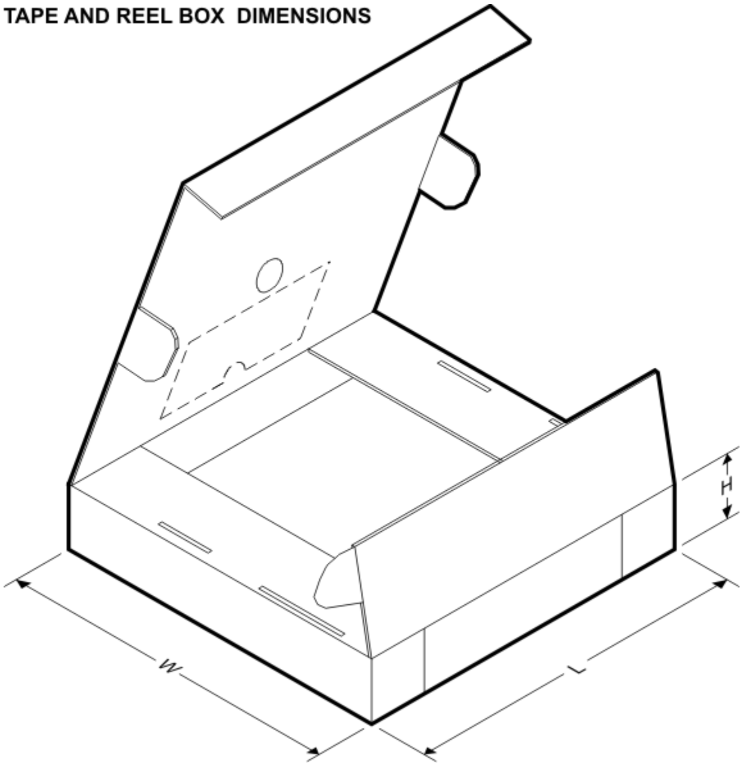
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75DP130DSRGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
SN75DP130DSRGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
SN75DP130SSRGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
SN75DP130SSRGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2

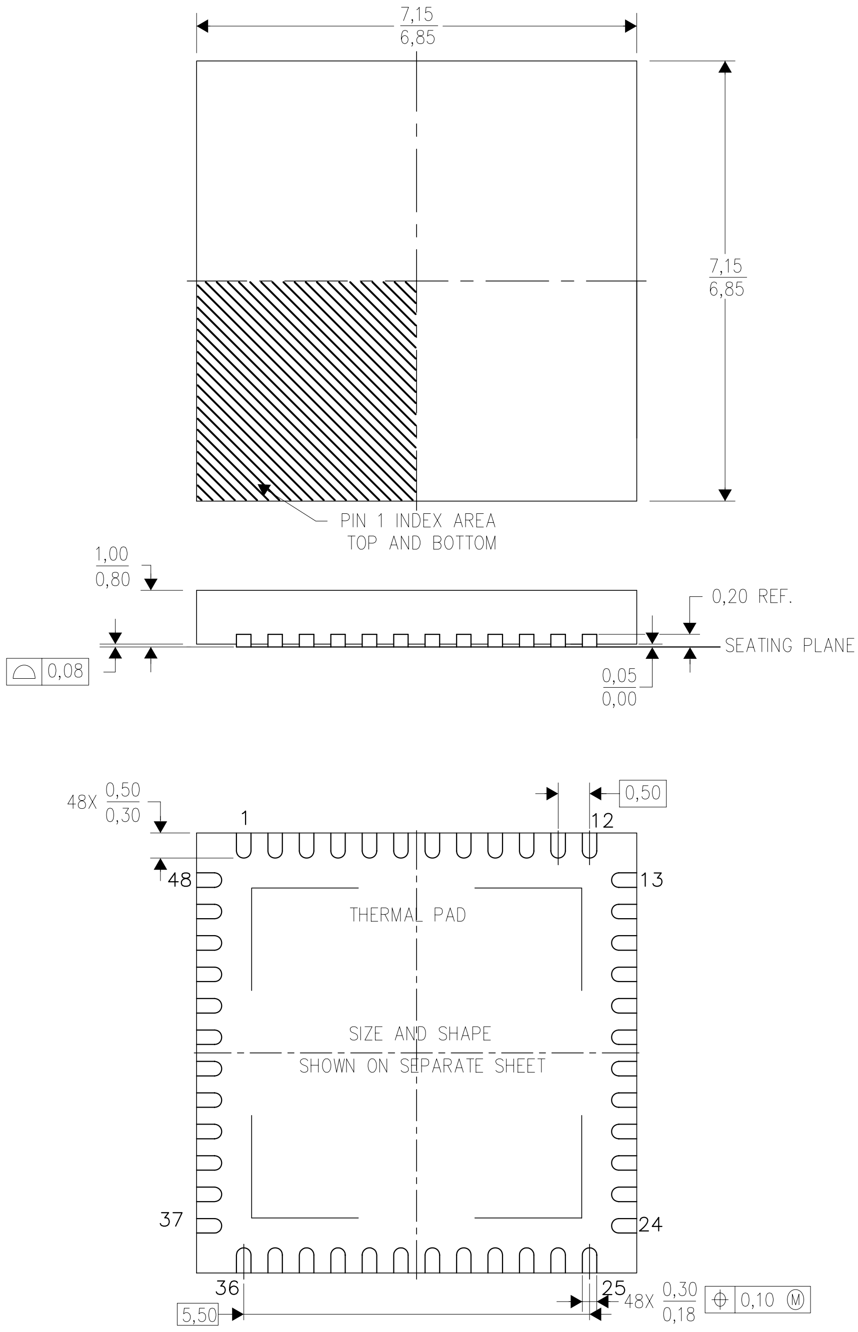
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75DP130DSRGZR	VQFN	RGZ	48	2500	367.0	367.0	38.0
SN75DP130DSRGZT	VQFN	RGZ	48	250	210.0	185.0	35.0
SN75DP130SSRGZR	VQFN	RGZ	48	2500	367.0	367.0	38.0
SN75DP130SSRGZT	VQFN	RGZ	48	250	210.0	185.0	35.0

RGZ (S-PVQFN-N48) PLASTIC QUAD FLATPACK NO-LEAD



4204101/F 06/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No-leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO-220.

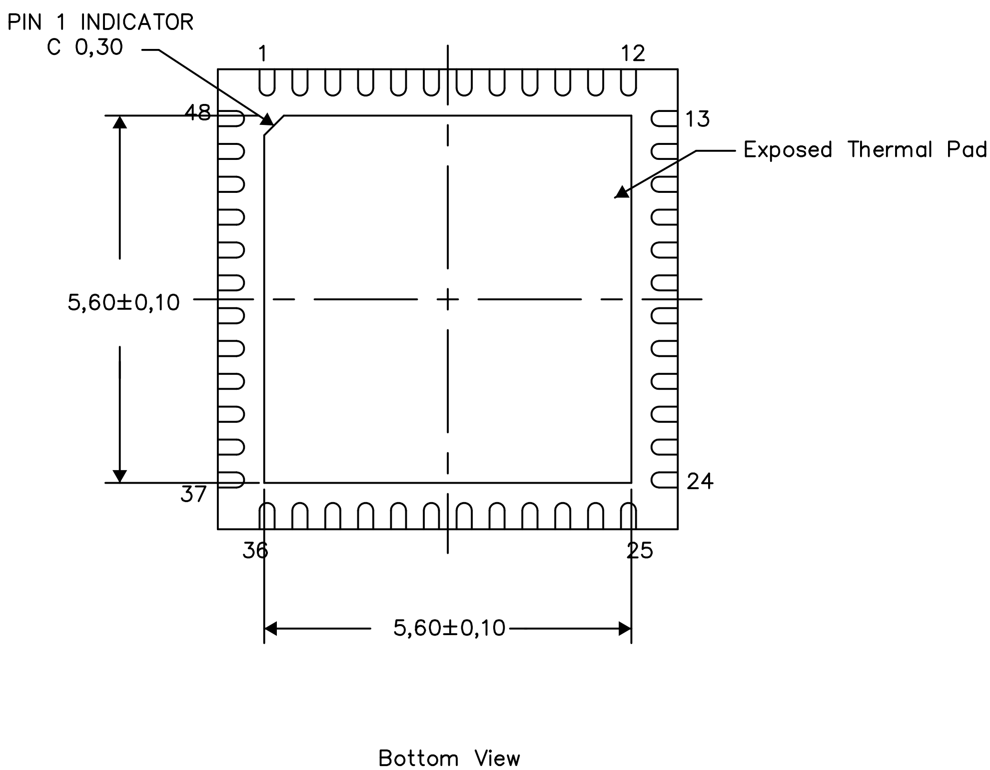
RGZ (S-PVQFN-N48) PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

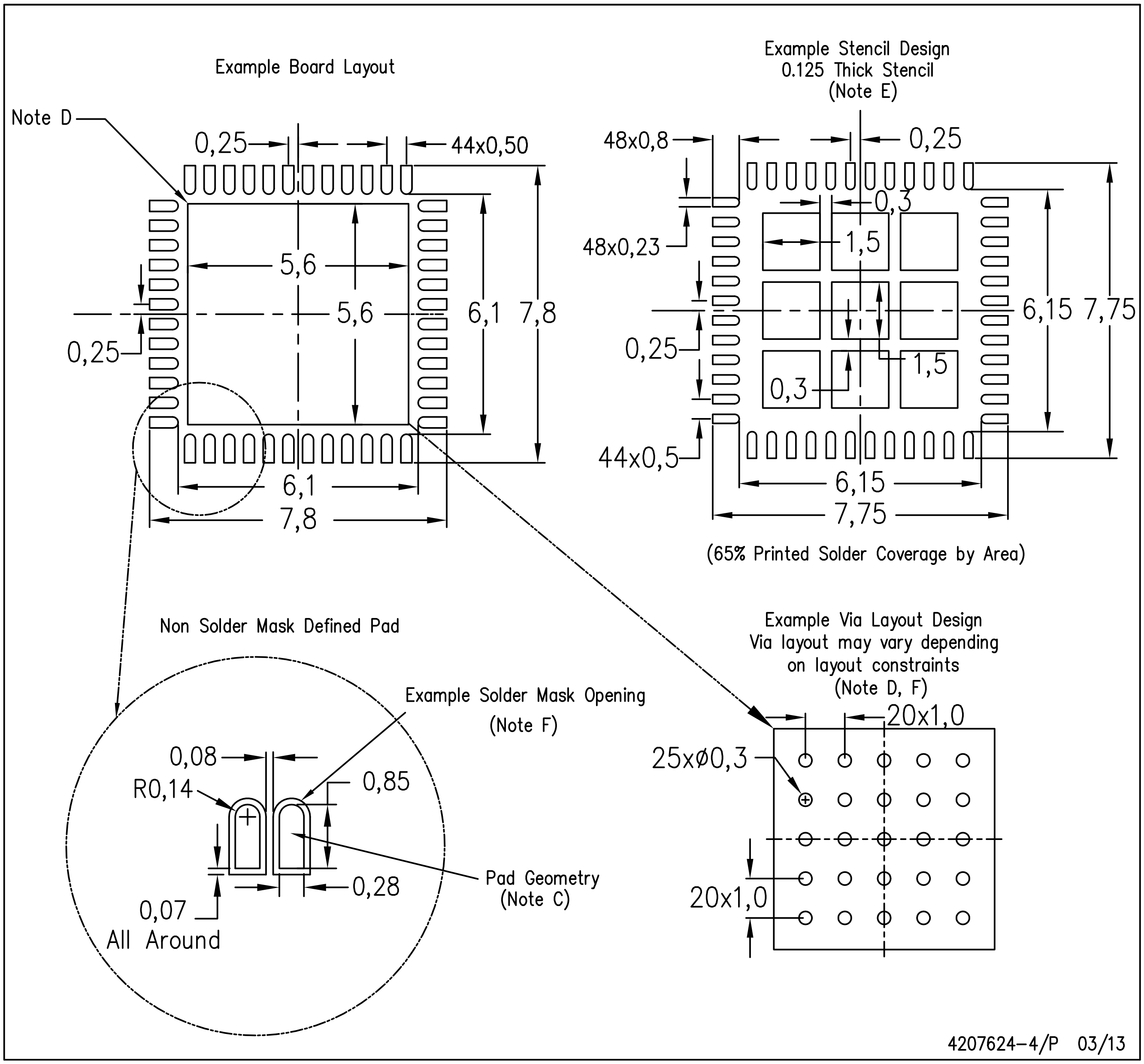


Exposed Thermal Pad Dimensions

4206354-5/T 03/13

NOTE: All linear dimensions are in millimeters

RGZ (S-PVQFN-N48) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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