TFS7701-7708
HiperTFS™-2 Family

Combined Two-Switch Forward and Flyback Power Supply Controllers with Integrated High-Voltage MOSFETs

Product Enhancements

- Selectable 132 kHz main switching frequency for lower cost and smaller magnetics
- Increased main peak power vs. HiperTFS-1
- Self-biased high-side driver eliminates high-side bias winding and diode
- Package lead form and pinout modified for easier insertion and PC-board layout
- Tighter $UV_{(ON)}$ standby threshold tolerance
- Improved standby no-load performance

Key Benefits

- Single IC solution for two-switch forward main (66 kHz/132 kHz) and flyback (132 kHz) standby
- High integration allows smaller form factor and higher power density designs, with reduced component count
- Incorporates control, gate drivers, and three power MOSFETs
- Level shift technology eliminates need for pulse transformer
- Protection features include: UV, OV, OTP, OVP, standby OPC, SCP, and I_{LIMIT}
- Transformer reset control, prevents saturation under all conditions
- Main duty cycle operation above 50% for reduced rms currents and lower output diode voltage rating
- Less than 10% variation in standby overload power over input voltage range
- Up to 586 W peak output power in a highly compact package
- >90% efficiency at full load
- Simple clip mounting to heat sink without need for insulation pad
- Halogen free and RoHS compliant

Typical Applications

- PC (80 PLUS® Bronze and 80 PLUS Silver)
- Printer
- LCD TV
- Video game consoles
- High-power adapters
- Industrial and appliance

Output Power Table

Product[3]	Two-Switch Forward 380 V		Flyback 100 V - 400 V
	Continuous[1] (50 °C)	Peak[2]	Continuous (50 °C)
TFS7701H	148 W	187 W	20 W
TFS7702H	190 W	297 W	20 W
TFS7703H	229 W	375 W	20 W
TFS7704H	251 W	419 W	20 W
TFS7705H	269 W	466 W	20 W
TFS7706H	298 W	513 W	20 W
TFS7707H	322 W	553 W	20 W
TFS7708H	343 W	586 W	20 W

Table 1. Output Power Table.

Notes:
1. Maximum practical continuous power in an open frame design with adequate heat sinking to maintain a heat sink temperature ≤95 °C (see Key Applications Considerations for more information) measured at specified ambient temperature.
2. Peak load less than 10 seconds and average power less than maximum continuous load.
3. Package: eSIP-16F. (Note: Direct attach to heat sink, does not require insulation SIL pad).

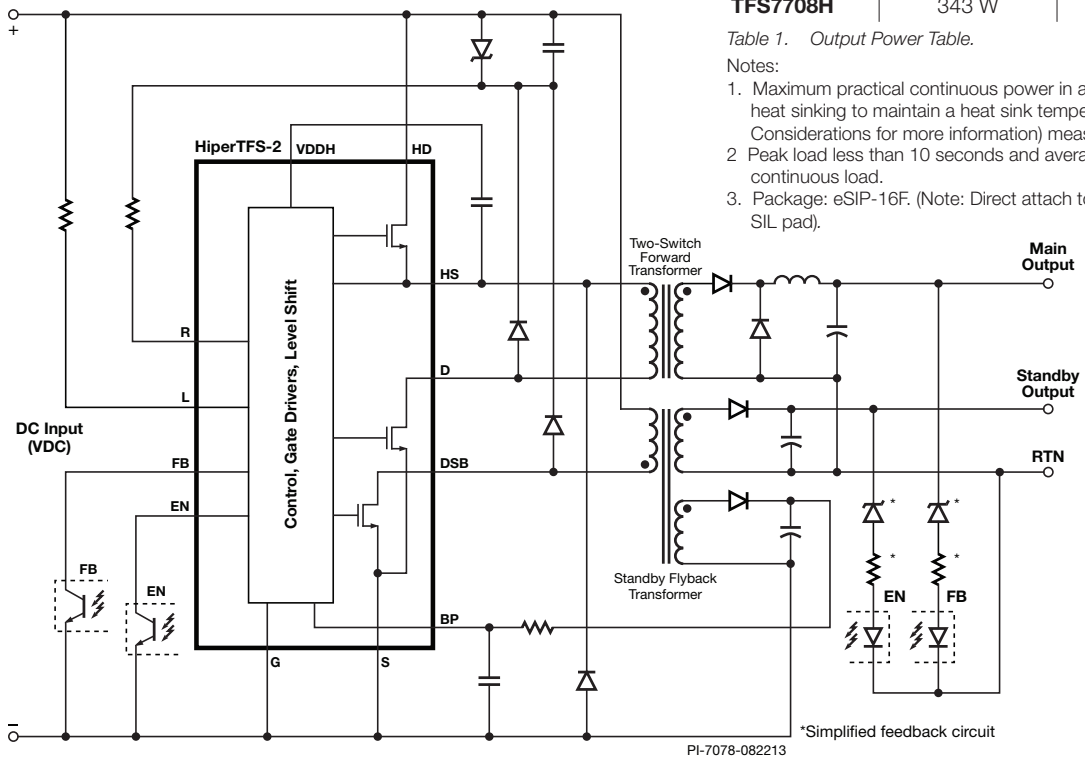
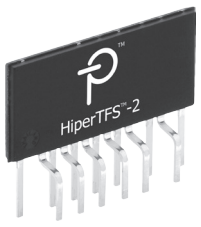


Figure 1. Schematic of Two-Switch Forward and Flyback Converter.



eSIP-16F (H Package)

Figure 2. Package Option.

Section List

Description

The HiperTFS-2 device family members incorporate both a high-power two-switch-forward converter and a mid-power flyback (standby) converter into a single, low-profile eSIP™ power package. The single chip solution provides the controllers for the two-switch-forward and flyback converters, high- and low-side drivers, all three of the high-voltage power MOSFETs, and eliminates the converter's need for costly external pulse transformers. The device is ideal for high power applications that require both a main power converter (two-switch forward) up to 586 W peak, and standby converter (flyback) up to 20 W. HiperTFS-2 includes Power Integrations' standard set of comprehensive protection features, such as integrated soft-start, fault and overload protection, and hysteretic thermal shutdown. HiperTFS-2 utilizes advanced power packaging technology that simplifies the complexity of two-switch forward layout, mounting and thermal management, while providing very high power capabilities in a single compact package. The devices operate over a wide input voltage range, and can be used following a power-factor correction stage such as HiperPFS.

Two-switch-forward power converters are often selected for applications demanding cost-effective converters that have high efficiency, fast transient response, and high rejection to line voltage variation. The two-switch-forward controller incorporated into HiperTFS-2 devices improves on the classic topology by allowing operation considerably above 50% duty cycle. This improvement reduces RMS current conduction losses, minimizes the size and cost of the bulk capacitor, and minimizes output diode voltage ratings. The advanced design also includes transformer flux reset control (saturation protection) and charge-recovery switching of the high-side MOSFET, which reduces switching losses. This combination of innovations yields an extremely efficient power supply with smaller MOSFETs, fewer passives and discrete components, and a lower-cost smaller transformer.

HiperTFS-2's flyback standby controller and MOSFET solution is based on the highly popular TinySwitch™ technology used in billions of power converter ICs due to its simplicity of operation, light load efficiency, and rugged, reliable, performance. This flyback converter can provide up to 20 W of output power and the built-in overload power compensation reduces component design margin.

Product Highlights

Protected Two-Switch Forward and Flyback Combination Solution

- Incorporates three high-voltage power MOSFETs, main and standby controllers, and gate drivers
- Level shift technology eliminates need for pulse transformer
- Programmable line undervoltage (UV) detection prevents turn-off glitches
- Programmable line overvoltage (OV) detection; latching and non-latching
- Accurate hysteretic thermal shutdown (OTP)
- Accurate selectable cycle-by-cycle current limit (main and standby)
  - Line compensated standby MOSFET current limit for standby over power compensation (OPC)
- Fully integrated soft-start to minimize start-up stress
- Simple fast AC reset
- Reduced EMI
  - Synchronized 66/132 kHz forward and 132 kHz flyback converters
  - Frequency jitter
- Eliminates up to 30 discrete components for higher reliability and lower cost

Asymmetrical Two-Switch Forward Reduces Losses

- Allows >50% duty cycle operation
  - Reduces primary-side RMS currents and conduction losses
  - Minimizes the size and cost of the bulk capacitor
  - Allows reduced capacitance or longer hold-up time
  - Allows lower voltage output diodes for higher efficiency
- Transformer reset control
  - Prevents transformer saturation under all conditions
  - Extends duty cycle to satisfy AC cycle drop out ride through
- Duty cycle soft-start
  - Satisfies 2 ms ~ 20 ms start-up with large capacitance at output
- Self-biased high-side driver eliminates high-side bias winding (66 kHz)
- Remote-on/off function
- Voltage-mode controller with current limit

20 W Flyback with Selectable Power Limit

- TinySwitch-III based converter
- Selectable power limit (10 W, 12.5 W, 15 W, 20 W)
- Built-in overload power compensation (OPC)
  - Flat overload power vs. input voltage
  - Reduces component stress during overload conditions
  - Reduces required design margin for transformer and output diode
- Output overvoltage (OVP) protection with fast AC reset
  - Latching, non-latching, or auto-restart
- Output short-circuit protection (SCP) with auto-restart

Advanced Package for High Power Applications

- Up to 586 W peak output power capability in a highly compact package
- Simple clip mounting to heat sink
  - Can be directly connected to heat sink without insulation pad
  - Provides lower thermal resistance than a TO-220
  - Heat slug connected to ground potential for low EMI
- Two row lead form for easy insertion into PC-board
- Single power package for two power converters reduces assembly costs and layout size

Function	Typical Two-Switch Forward	HiperTFS-2	Advantages of HiperTFS-2
Nominal Duty Cycle	33%	45%	Wider duty cycle reduces RMS switch currents by 17%. Reduces $R_{DS(ON)}$ losses by 31%
Maximum Duty Cycle	<50%	63%	
Switch Current (RMS)	100%	83%	
Output Catch Diode Voltage Rating	100%	79%	Lower losses. Wider D_{MAX} lowers catch diode rating by $V_O + V_D/D_{MAX}$ reduction in catch diode voltage rating
Clamp Voltage	Reset diodes from zero to V_{IN}	Reset from zero to (V_{IN} + 130 V)	With fast/slow diode combination, allows charge recovery to limit high-side MOSFET C_{OSS} loss
Thermal Shutdown	---	118 °C Shutdown / 55 °C Hysteresis	HiperTFS-2 provides integrated OTP device protection
Current Sense Resistor	0.5 V drop (0.33 Ω at 300 W)	No sense resistor	Improved efficiency. MOSFET $R_{DS(ON)}$ sense eliminates need for sense resistor
High-Side Drive	Requires gate-drive transformer (high-cost)	Built-in high-side drive	Lower cost; component elimination. Removes high-cost gate-drive transformer (EE10 or toroid)
Component Count	Higher	Lower	Saves up to 30 components, depending on specification.
TinySwitch Overload Power Compensation vs. Input Voltage	---	Built-in compensation	Safer design; easier to design power supply. Flattens standby overload output power versus line voltages
Package PC Board Creepage	TO-220 = 1.17 mm	eSIP16/12 = 2.3 mm	HiperTFS-2 meets functional safety spacing at package pins
Package Assembly	2 × TO-220 package, 2 × SIL (insulation), 1 main controller, 1 standby controller	1 Package	No SIL (insulation) pad required

Table 2. Summary of Differences Between HiperTFS-2 and Other Typical High Power Supplies.

Pin Functional Description

MAIN DRAIN (D) Pin
Drain of the low-side MOSFET transistor forward converter.

STANDBY DRAIN (DSB) Pin
Drain of the MOSFET of standby power supply.

GROUND (G) Pin
This pin gives a signal current path to the substrate of the low-side controller. This pin is provided to allow a separate Kelvin connection to the substrate of the low-side controller to eliminate inductive voltages that might be developed by high switching currents in the SOURCE pin. The GROUND pin is not intended to carry high currents, it is intended as a voltage-reference connection only.

SOURCE (S) Pin
SOURCE pin that is common to both the standby and main supplies.

RESET (R) Pin
This pin provides information to limit the maximum duty cycle as a function of the current fed into the LINE-SENSE and RESET pins to prevent cycle-by-cycle saturation of main transformer. This pin can also be pulled up to bypass to signal remote-on/off of the main converter only.

ENABLE (EN) Pin
This is the ENABLE and CURRENT LIMIT SELECTION pin for the standby controller. Prior to start-up the resistor value connected from ENABLE to BYPASS, is detected to select one of several internal standby current limit values.

LINE-SENSE (L) Pin
This pin provides input bulk voltage line-sense function. This information is used by the undervoltage and overvoltage detection circuits for both main and standby. The pin can also be pulled up to BYPASS or be pulled down to SOURCE to implement a remote-on/off of both standby and main supplies simultaneously. The LINE-SENSE pin works in conjunction with the RESET pin to implement a duty cycle limit function. The LINE-SENSE pin compensates the value of standby current limit so as to flatten the output overload power characteristic as a function of input voltage.

FEEDBACK (FB) Pin
This pin provides feedback for the main two transistor forward converter. An increase in sink current from the FEEDBACK pin to ground, reduces the operating duty cycle. This pin also selects the main device current limit at start-up (in a similar manner to ENABLE pin).

BYPASS (BP) Pin
This is the decoupled operating voltage pin for the low-side controller. At start-up the capacitor connected to this pin is charged from an internal current source. During normal operation the capacitor voltage is maintained by drawing current from the low-side bias winding on the standby power supply. This pin is also used to implement remote-on/off for the main controller. This is done by driving extra current into the BYPASS pin when we want to turn-on the main controller. The BYPASS pin also implements a latch-off function to disable standby and main when the BYPASS pin current exceeds a threshold. The latch is reset when LINE-SENSE pin falls below UV (off) standby threshold. The BYPASS pin capacitor value selects for either 66 kHz (1 µF) or 132 kHz (10 µF) main switching frequency.

HIGH-SIDE OPERATING VOLTAGE (VDDH) Pin
This is the high-side bias (VDD) of approximately 11.5 V. This voltage is maintained with current from an internal high-voltage current source and/or from a bootstrap diode from the low-side standby bias supply.

HIGH-SIDE SOURCE (HS) Pin
SOURCE pin of the high-side MOSFET.

HIGH-SIDE DRAIN (HD) Pin
DRAIN pin of the high-side MOSFET. This MOSFET is floating with respect to low-side source and ground.

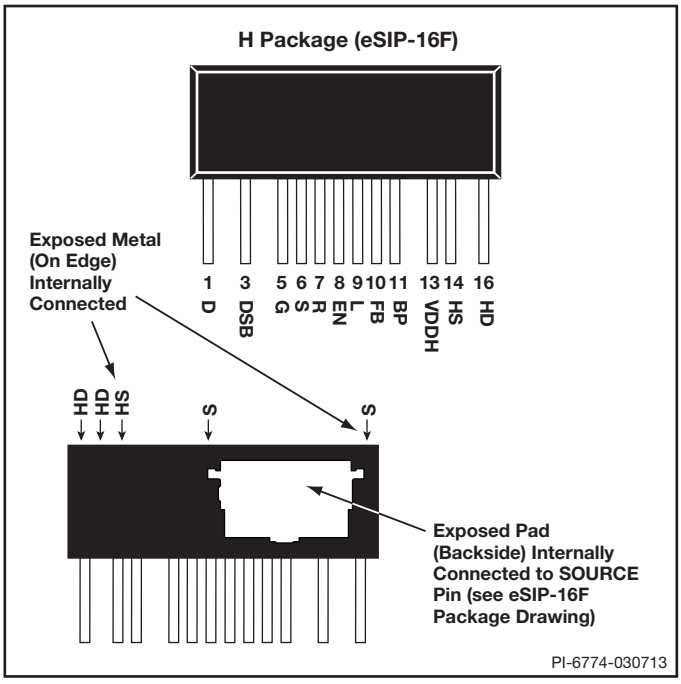


Figure 2. Pin Configuration.

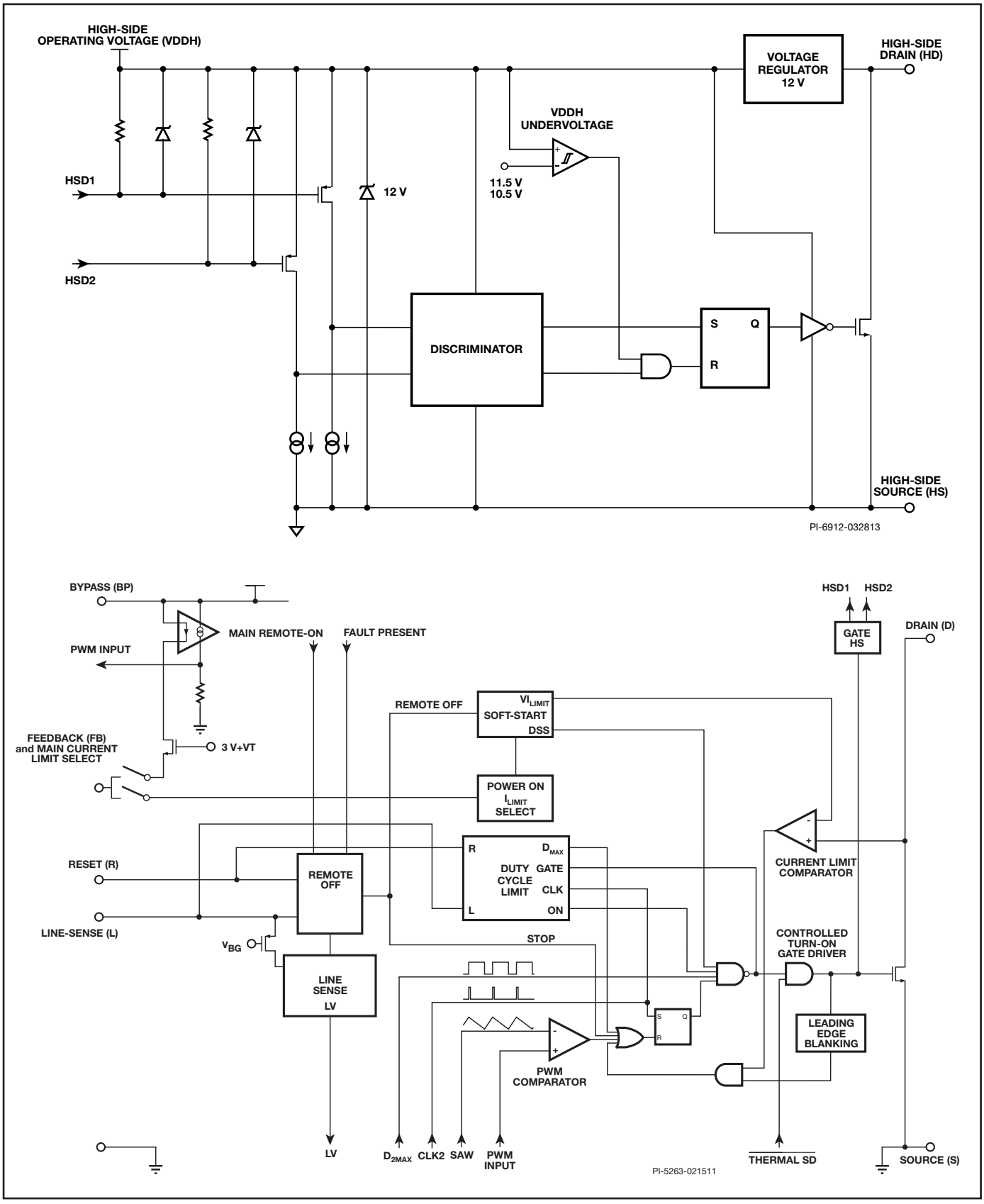


Figure 3. Functional Block Diagram for Two-Switch Forward Converter.

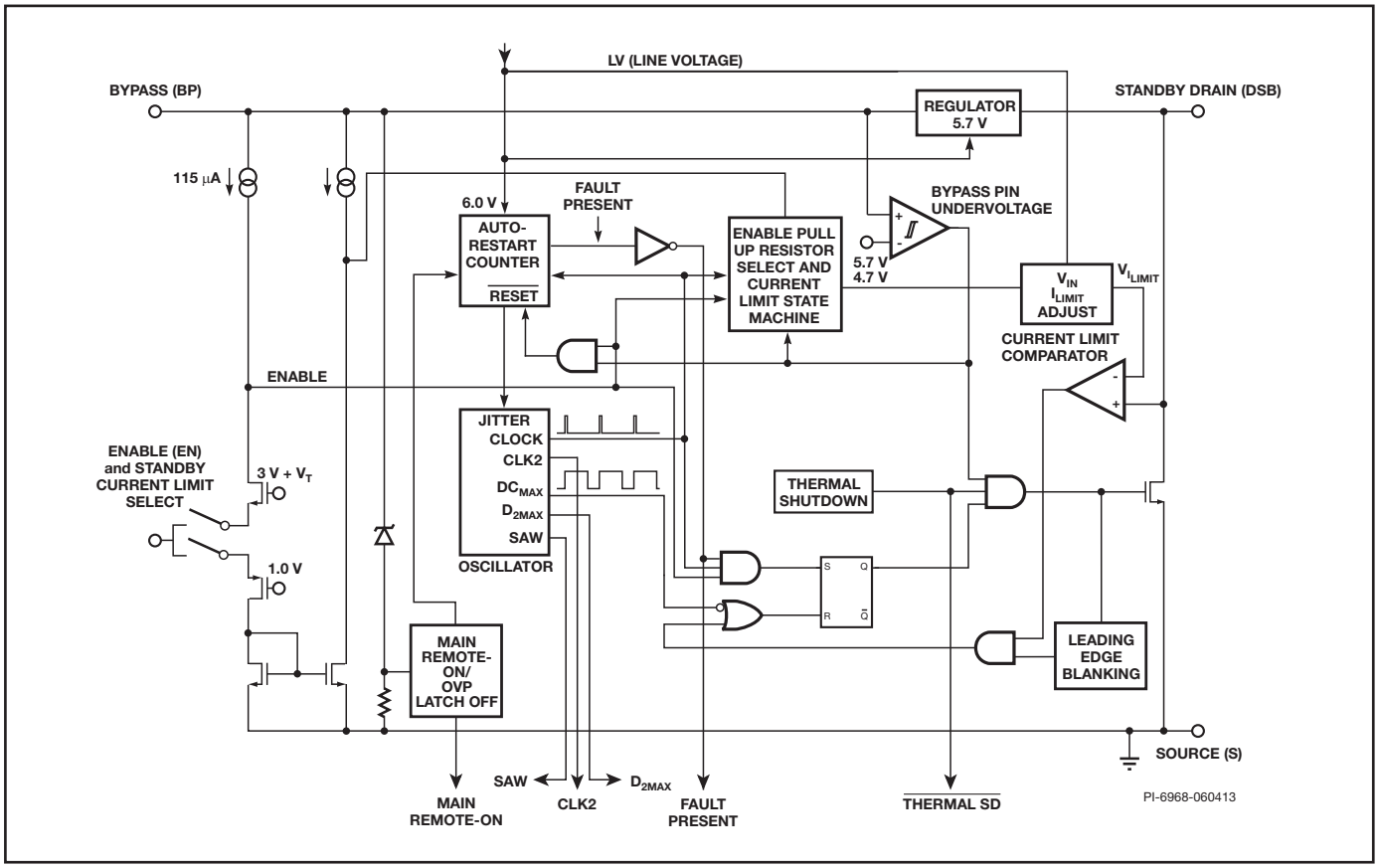


Figure 4. Functional Block Diagram for Flyback/Standby Converter.

Functional Description

The HiperTFS-2 contains two switch-mode power supply controllers and associated low-side MOSFET's along with high-side driver and high-side MOSFET.

- The HiperTFS-2 two-switch forward includes a controller along with low-side power MOSFET, high-side power MOSFET, high-side driver and selectable main switching frequency (synchronous with standby) of 66/132 kHz. The main converter operates in voltage-mode (linear duty cycle control) at fixed frequency (exactly half the operating frequency of the standby controller when is 66 kHz mode). The control converts a current input (FEEDBACK pin), to a duty cycle at the open drain MOSFET MAIN DRAIN pin decreasing duty cycle with increasing sourced current from the FEEDBACK pin.

- The HiperTFS-2 fixed frequency (132 kHz) standby flyback includes a controller and power MOSFET which is based on TinySwitch-4. This device operates in multi-level ON/OFF current limit control mode. The open drain MOSFET (STAND-BY DRAIN pin) is turned on when the sourced current from the ENABLE pin is below the threshold and switching is disabled when the ENABLE pin current is above the threshold.

In addition to the basic features, such as the high-voltage start-up, the cycle-by-cycle current limiting, loop compensation circuitry, auto-restart and thermal shutdown, the HiperTFS-2 main controller incorporates many additional functions that reduce system cost, increase power supply performance and design flexibility.

Main Converter General Introduction

The main converter for the HiperTFS-2, is a two-switch forward converter (although the HiperTFS-2 could be used with other two-switch topologies). This topology involves a low-side and high-side power MOSFET, both of which are switched at the same time. In the case of the HiperTFS-2, the low-side MOSFET is a 725 V MOSFET (with the substrate connected to the SOURCE pin). The high-side MOSFET is a 530 V MOSFET (with the substrate connected to the HIGH-SIDE DRAIN (HD) pin). As such the substrate of both low-side and high-side MOSFET's are tied to quiet circuit nodes (0 V and V_{IN} respectively), meaning that both MOSFETs have electrically quiet substrates – good for EMI.

The low-side MOSFET has a very low C_{OSS} capacitance and thus can be hard-switched without performance penalty. Due to the external clamp configuration it is possible to substantially soft-switch the high-side MOSFET at high-loads (thus eliminating a large proportion of high-side capacitive switching loss) and improving efficiency. The higher breakdown voltage on the low-side MOSFET allows the transformer reset voltage to exceed the input voltage, and thus allow operation at duty cycles greater than 50%. Higher duty cycle operation leads to lower RMS switch currents and also lower output diode voltage-rating, both of which contribute to improved efficiency.

The HiperTFS-2 also contains a high-side driver to control the high-side MOSFET. This external bootstrap diode (or internally self-biased) high-side driver eliminates the need for a gate-driver transformer, an expensive component that is required for many other two-switch forward circuits.

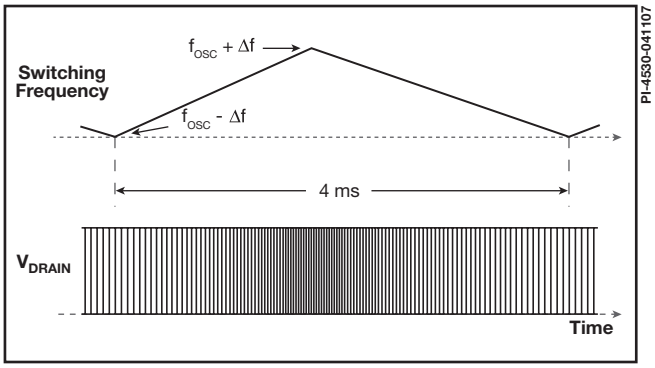


Figure 5. Switching Frequency Jitter (Idealized V_{DRAIN} Waveforms).

Main Start-Up Operation

Once the flyback (standby) converter is up and running, the main converter can be enabled by two functions. The first condition is that the BYPASS pin remote-on current must exceed the remote-on threshold ($I_{BP(ON)}$), provided by an external remote-on/off circuit. This current threshold has a hysteresis to prevent noise interference. Once the BYPASS remote-on has been achieved, the HiperTFS-2 also requires that the LINE-SENSE pin current exceeds the UV main-on ($I_{L(MA-UVON)}$), which corresponds to approximately 336 VDC input voltage when using a 4 MΩ LINE-SENSE pin resistor. Once this LINE-SENSE pin threshold has been achieved the HiperTFS-2 will enter a 60 ms pre-charge period ($t_{D(CH)}$) to allow the PFC-boost stage to reach

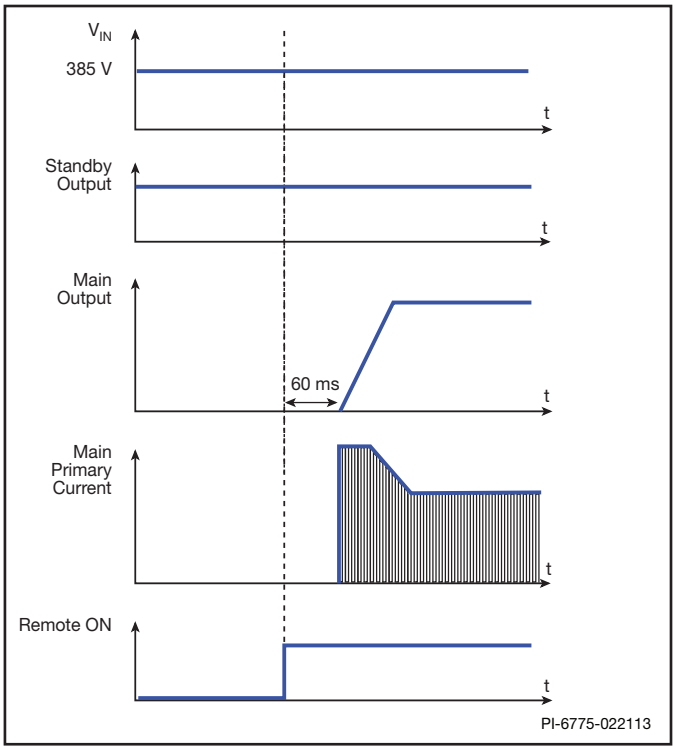


Figure 6. Supply Start-Up Sequence by Remote-On.

regulation before the main applies a load to the bulk-capacitor. Also during this pre-charge period the high-side driver is charged via the bootstrap diode (or self bias) from the low-side auxiliary voltage, and is charged when the main low-side MOSFET turns on, while the main high-side MOSFET is held off. By the end of the pre-charge period, the PFC-boost voltage should be at or above the nominal boost voltage. The HiperTFS-2 begins switching, going through the soft-start period (t_{SS}). During the soft-start period the maximum duty cycle starts at 30% and is ramped during a 12 ms period to the maximum. The ramped duty cycle controls the rise slew rate of the output during start-up, allowing well controlled start-up and also facilitates a smooth transition when the control loop takes over regulation towards the end of soft-start. This allows the main to start-up within the required period for the application (typically <20 ms for PC main applications), when there is a substantial capacitive load on the output.

Main Converter Control FEEDBACK (FB) Pin Operation

The FEEDBACK pin is the input for control loop feedback from the main control loop. During normal operation the FEEDBACK pin is used to provide duty cycle control for the main converter. The system output voltage is detected and converted into a feedback current. The main converter duty cycle will reduce as more current is sourced from the FEEDBACK pin, reaching zero duty cycle at approximately 2.1 mA. The nominal voltage of the FEEDBACK pin is maintained at approximately 3.5 V. An internal pole on the FEEDBACK pin is set to approximately 12 kHz, in order to facilitate optimal control loop response.

The maximum duty cycle of the main converter is defined by the LINE-SENSE pin and RESET pin behavior and is a dynamically calculated value according to cycle-by-cycle conditions on the LINE-SENSE pin and RESET pin.

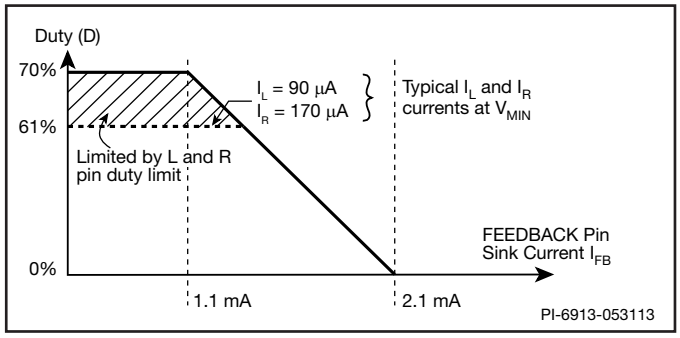


Figure 7. PWM Duty Cycle vs. Control Current.

Main High-Side Driver

The high-side driver is a device that is electrically floating at the potential of the HIGH-SIDE MOSFET SOURCE (HS) pin. This device provides gate-drive for the high-side main MOSFET. The low-side main and high-side main MOSFET's switch simultaneously. The high-side driver has a HIGH-SIDE OPERATING VOLTAGE supply pin. External circuitry or an internal source, provides operating current and provides HIGH-SIDE OPERATING VOLTAGE pin. The high-side operating voltage has an internal 12 V shunt-regulator. The device consumes approximately 2.3 mA when driving the high-side MOSFET.

The HIGH-SIDE OPERATING VOLTAGE pin has an undervoltage lock-out threshold, to prevent gate-drive when the supply voltage drops below a safe threshold. At power-up the high-side driver remains in the off-state, until the HIGH-SIDE OPERATING VOLTAGE pin is charged above 10.5 V, at which point the high-side driver becomes active. The high-side driver is initially charged via either a bootstrap diode connected to the HIGH-SIDE OPERATING VOLTAGE pin from the low-side standby auxiliary supply (approximately 12 V) or from an internal high-voltage current source. During start-up the high-side MOSFET remains off, but the low-side MOSFET is turned on for a period of 60 ms to allow pre-charge of the high-side operating voltage to 12 V. After this period, the high-side operating voltage is supplied by a bootstrap diode or internal current source.

Once the high-side driver is operating it receives level-shifted drive commands from the low-side device. These drive commands cause both turn-on and turn-off drive of the high-side main MOSFET simultaneously with that of the low-side main MOSFET.

The high-side driver also contains a thermal shutdown on-chip, but this is set to a temperature above the thermal shutdown temperature of the low-side device. Thus the low-side will always shutdown first.

Main Converter Maximum Duty Cycle

The LINE-SENSE pin resistor converts the input voltage into an LINE-SENSE pin current signal. The RESET pin resistor converts the reset voltage into an RESET pin current signal. The LINE-SENSE pin and RESET pin currents allow the HiperTFS-2 to determine a maximum duty cycle envelope on a cycle-by-cycle basis. This feature ensures sufficient time for transformer reset on a cycle-by-cycle basis and also protects against single-cycle transformer saturation and at high-input voltage by limiting the maximum duty cycle to prevent the transformer from reaching an unsafe flux density during the on-time period. Both of these features allow the optimal performance to be obtained from the main transformer. The duty cycle limit is trimmed during production.

The LINE-SENSE pin and RESET pin are sampled just before the turn-on of the next main cycle. This is done to sample at a point when there is minimal noise in the system. Due to the low current signal input to the LINE-SENSE pin and RESET pin, care should be taken to prevent noise injection on these pins (see Applications section layout guidelines for details).

Main On-Chip Current Limit with External Selection

During start-up, the FEEDBACK pin and ENABLE pin are both used to select internal current limits for the main and standby converters respectively. The detection period occurs at the initial start-up of the device, and before the main or standby MOSFETs start switching. This is done to minimize noise interference.

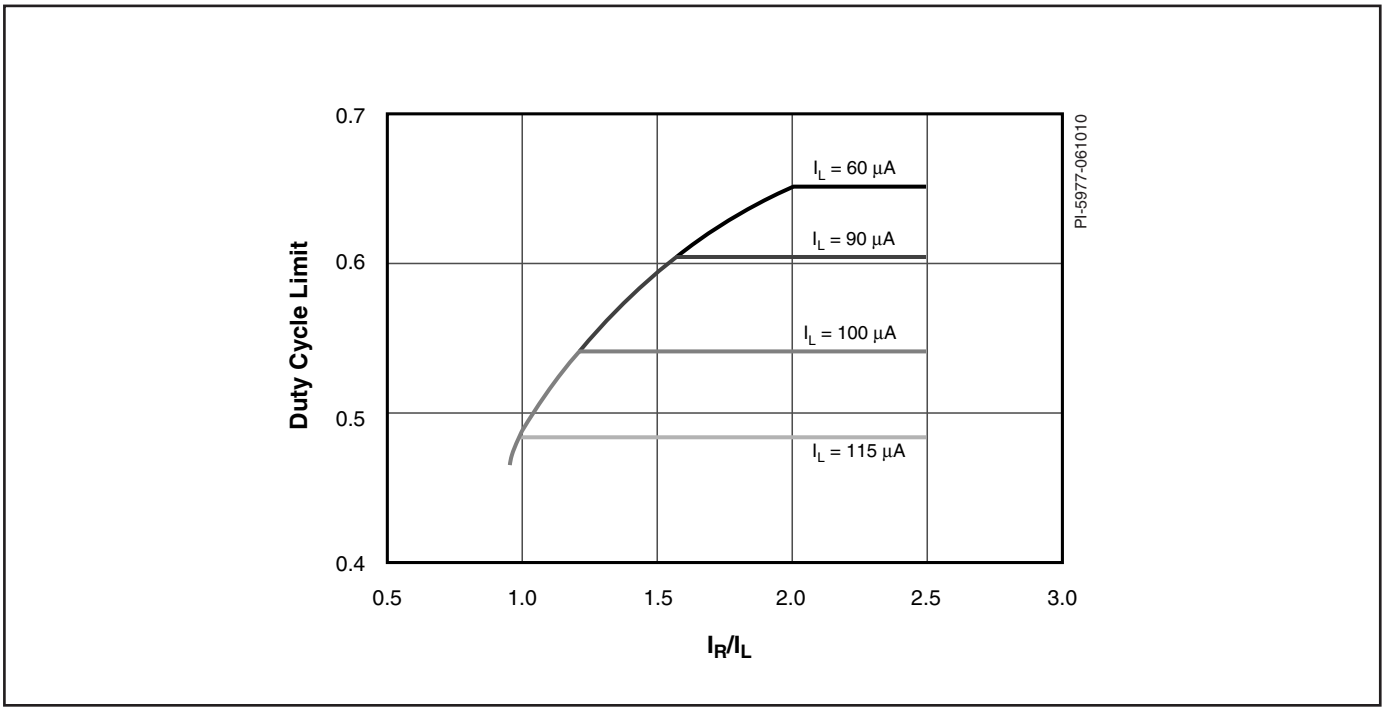


Figure 8. Duty Cycle Limit vs. Ratio of R Pin Current Over L Pin Current.

A resistor R_{FB} is connected from the BYPASS pin to the FEEDBACK pin. This resistor feeds current into the FEEDBACK pin (pin voltage is clamped to approximately 1 V during this detection period). The current into the FEEDBACK pin is determined by the value of the resistor, and thus the input current (and indirectly the resistor value), select an internal current limit according to the following table.

I_{FB} (Threshold)	I_{LIMIT} (Main)			$R_{FB(SELECT)}$ (1%)	
0.0 - 5.1 µA	L1	70%	mA	Open	kΩ
5.1 - 11.9 µA	L2	90%	mA	511.0	kΩ
11.9 - 23.8 µA	L3	100%	mA	232.0	kΩ

Table 3. FEEDBACK Pin Main Current Limit Selection.

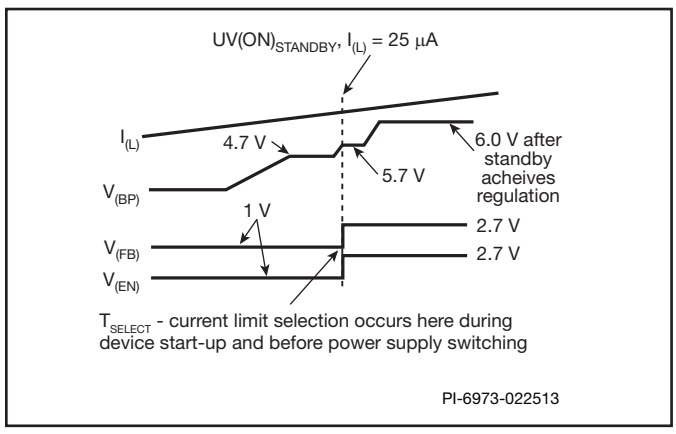


Figure 9. Current Limit Selection.

Main Line Undervoltage Detection (UV)

The LINE-SENSE pin resistor is connected to V_{IN} and generates a current signal proportional to V_{IN}. The LINE-SENSE pin voltage is held by the device at 1.2 V. The LINE-SENSE pin current signal is used to trigger under/overvoltage thresholds for both the standby and main converters. Assuming a LINE-SENSE pin resistor of 4 MΩ, the standby will begin operating when the LINE-SENSE pin current exceeds the ($I_{L(SB-UVON)}$) threshold, nominally approximately 100 V. However the main is still held in the off-state, until the LINE-SENSE pin current exceeds the ($I_{L(MA-UVON)}$) threshold, nominally 336 V for 4 MΩ. There is hysteresis for both main and standby undervoltage-off thresholds, to allow sufficient margin to avoid accidental triggering, and to provide sufficient margin to meet hold-up time requirements. Bear in mind that the main converter may start to loose regulation before it finally shuts down. This is because the dynamic duty cycle limit may clamp the duty cycle below that required for regulation at lower input voltages. Once the input voltage falls below the 215 V ($I_{L(MA\_UVOFF)}$) threshold, the main will shutdown but standby will continue to operate. The standby will turn off when the input voltage drops below approximately 40 V ($I_{L(SB-UVON)}$).

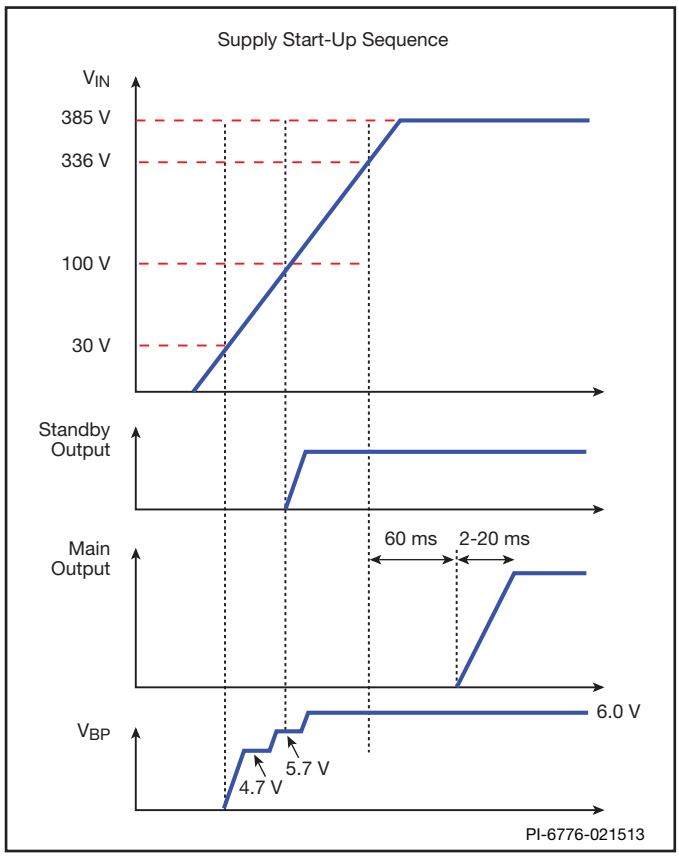


Figure 10. Main and Standby Start-Up.

Main Reset Overvoltage Detection

There is also an overvoltage threshold for the RESET pin. When triggered, the RESET overvoltage will shutdown only the main, leaving the standby in operation.

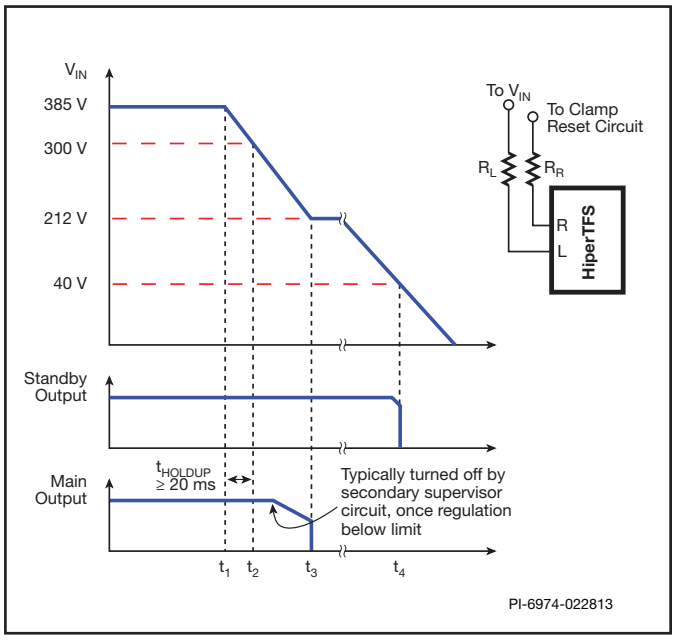


Figure 11. L and R Pin Duty Limit Mode.

Standby Power General Introduction

The standby is a wide range power supply, typically a flyback converter, operating over a wide input range (85-265 VAC) and delivering up to 20 W continuous output power. The standby power supply provides two functions in most high-power applications. It provides a direct secondary output but also provide bias power to other primary-side devices (in particular typically a PFC boost converter).

The HiperTFS-2 standby retains most features of the TinySwitch-III, such as auto-restart, thermal shutdown, multi-level current limit ON/OFF control, etc. The HiperTFS-2 standby controller has a few differences versus TinySwitch-III:

1. There are 4 current limits that are selected via the ENABLE pin (rather than by using different BYPASS pin capacitors as in TinySwitch-III). There are 4 user selectable current limits 500, 550, 650, 750 mA design for secondary standby output power of 10, 12.5, 15 and 20 W.
2. Secondary OVP latching shutdown. This is triggered via a current in excess of the BYPASS pin latching shutdown threshold ($I_{BP(SD)}$ = 15 mA).
3. Dedicated LINE-SENSE pin for line-voltage detection providing absolute UV and OV ON/OFF thresholds (unlike TinySwitch-4 which detects input voltage only during restart). Also higher accuracy for UV(ON) threshold.
4. Current limit is compensated as a function of input voltage to maintain a flat overload characteristic versus input voltage.

In a high-power system, the standby power supply is the first power supply to begin operating. The main converter cannot begin working until the standby is in operation. Likewise the main converter will shutdown at a higher-voltage than the standby and thus the standby is always the last power supply to shutdown.

Standby On-Chip Current Limit with External Selection

During start-up, the FEEDBACK pin and ENABLE pin are both used to select internal current limits for the main and standby converters respectively. The detection period occurs at the initial start-up of the device (just after BYPASS pin voltage of 4.7 V is achieved), and before the main or standby MOSFETs start switching. This is done to minimize noise interference.

I EN (Threshold)	I_{LIMIT} (Standby)			R EN (Select) (1%)	
0 - 5 µA	L1	500	mA	Open	kΩ
5 - 12 µA	L2	550	mA	511	kΩ
12 - 24 µA	L3	650	mA	232	KΩ
24 - 48 µA	L4	750	mA	107	kΩ

Table 4. ENABLE Pin Standby Current Limit Selection.

The ENABLE pin works in a similar way to the FEEDBACK pin selection. The ENABLE pin is clamped to 1 V during selection, during the detection period. Thus the selection resistor values are the same for the ENABLE pin and the FEEDBACK pin. The ENABLE pin internal current selection is chosen according to the above table.

The current limit selection for both FEEDBACK pin and ENABLE pin takes place when the BYPASS pin first reaches 4.7 V. Once the short detection period is complete, the BYPASS pin is ramped on up to 5.7 V, and the FEEDBACK pin is allowed to float to it's nominal voltage of 3.5 V.

Standby Line Compensated Current Limit to Flatten Output Overload Power

For many power supplies, the power output capability of the power supply increases dramatically as the input voltage increases. This means that most power supplies are able to deliver much more power (up to 30-40% more power), into a fault overload when operating at higher input voltage (versus operating at lower input voltage). This can cause a problem since many specifications require that the output overload power capability of the device is more tightly managed.

In the case of the HiperTFS-2, the standby current limit is adjusted as a function of line (input voltage), in such a ways as to always provide substantially the same maximum overload power capability. The input voltage is detected via the LINE-SENSE pin current and the internal standby current limit of the device is adjusted accordingly on a cycle-by-cycle basis. This means that the HiperTFS-2 standby will only deliver approximately 5% more overload power at high-line as it did at low-line. This feature provides a much safer design.

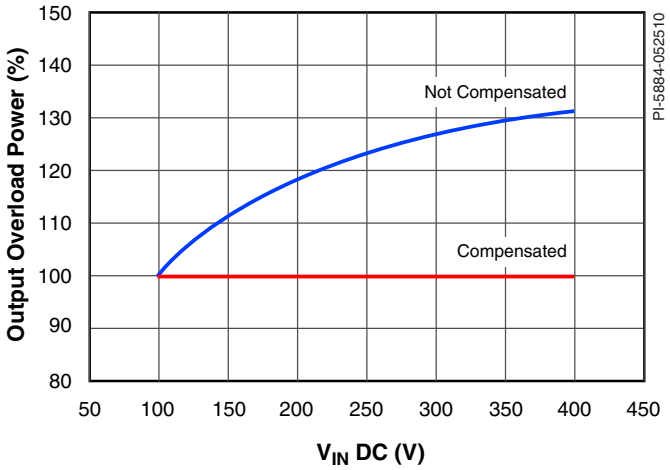


Figure 12. Shows Output Overload Power for Compensated (TFS-2) Standby and General Uncompensated Standby.

Standby Line Undervoltage Detection (UV)

The LINE-SENSE pin resistor is connected to V_{IN} and generates a current signal proportional to V_{IN}. The LINE-SENSE pin voltage is held by the device at 1.2 V. The LINE-SENSE pin current signal is used to trigger under/overvoltage thresholds for both the standby and main converters. Assuming a LINE-SENSE pin resistor of 4 MΩ, the standby will begin operating at approximately 100 V (as defined by $I_{L(SB\_UVON)}$). The standby will shutdown if regulation is lost when input voltage is below 100 V. However the standby will be forced to shutdown if this input voltage drops below approximately 40 V (as defined by $I_{L(SB-UVOFF)}$).

Main and Standby Oscillator and Switching Frequency

The standby converter operates at a frequency of 132 kHz. When in 66 kHz mode, main converter operates at exactly half that frequency. The two converters both include a common frequency jitter profile that varies the switching frequency ±4 kHz for the main (twice the jitter frequency range ±8 kHz for the standby), during a 4 ms jitter period. The frequency jitter helps reduce quasi-peak and average EMI emissions.

The HiperTFS-2 main switch frequency is selected at start-up for 66 kHz or 132 kHz based on the value of the BYPASS pin capacitor

It should be noted that when the HiperTFS-2 is running at 66 kHz there is a collision avoidance scheme in which the main converter is the master and the standby is the slave, which avoids the main and standby switching at exactly simultaneous moments. The most common condition would be close to 50% duty cycle, if the main (master) is about to switch (turn-off), then the standby (slave), waits for short instant (200 ns) before starting it's next cycle. The standby is used as the slave, since the ON/OFF control of the HiperTFS-2 standby is less easily disrupted by sudden delays in switching, versus the linear control loop of the main converter. This collision avoidance is not required when both standby and main run at 132 kHz.

Standby and Main Thermal Shutdown

The HiperTFS-2 provides a thermal shutdown function, (OTP) that protects the HiperTFS-2. This hysteretic thermal shutdown allows the device to automatically recover from any thermal fault event. The thermal shutdown is triggered at a die-temperature of approximately 118 °C and has a high hysteresis to ensure the average device temperature is within safe levels. In a well designed system the HiperTFS-2 thermal shutdown is not triggered during any normal operation and is only present as a safety feature to protect against abnormal or fault conditions.

BYPASS (BP) Pin Operation

The BYPASS (BP) pin is the supply pin for the entire HiperTFS-2 device. The BYPASS pin is internally connected to a high-voltage current source via the STANDBY DRAIN power MOSFET. This high-voltage source will charge the BYPASS pin to 4.7 V during initial power-up. Once the BYPASS pin reaches 4.7 V, the BYPASS pin will check the main and standby current limit selection (FEEDBACK pin and ENABLE pin resistors respectively). This selection takes a very short period, thereafter the BYPASS pin continues being charged until it reaches 5.7 V. During this change the value of the BYPASS pin capacitor is determined. The value selects for main switching frequency of (1 µF = 66 kHz) and 10 µF = 132 kHz) on completion of frequency selection, the standby power supply is ready to begin operation. Like the TinySwitch-4 the high-voltage current source will continue to charge the BYPASS pin if it drops below 5.7 V. However in most typical applications, a resistor (typically 7.5 kΩ) is connected from primary bias (12 V) to the BYPASS pin. This resistor provides the operating current to the BYPASS pin, preventing the need to draw power from the high-voltage current source. Like the TinySwitch, the BYPASS pin contains a

shunt regulator, which will be enabled if the BYPASS pin voltage is externally driven above 5.7 V. The BYPASS pin shunt current is used for two functions:

1. First, a 4 mA threshold ($I_{BP(ON)}$) for main remote-on. When the BYPASS pin current exceeds this threshold, the main is enabled.
2. Second a 15 mA threshold ($I_{BP(SD)}$)for standby secondary OVP latch-off. When the BYPASS pin current exceeds this threshold, the standby and main converters are latched-off. This latch can be reset by pulling the LINE-SENSE pin below the line undervoltage threshold ($I_{L(SB-UVOFF)}$), or by discharging the BYPASS pin below 4.7 V.

Main and Standby Line Overvoltage Detection (OV)

The overvoltage threshold is included in the device, and can be used to disable the device during overvoltage (with the use of an additional external signal Zener). The overvoltage threshold is set sufficiently high to prevent accidental triggering during boost PFC overshoot conditions. When the overvoltage condition is triggered, it will simultaneously shutdown both the main and standby. The overvoltage feature is intended for use with external components (circuitry), to program the overvoltage threshold independently of the undervoltage thresholds (see the Applications section for details).

High-Power eSIP Package

The HiperTFS-2 package is designed to minimize the physical size of the device, while maintaining a low thermal resistance and sufficient electrical spacing for the pins. The package has 12 functional pins with 4 pins removed for increased pin-to-pin spacing between high-voltage pins. The low-side two-switch forward and flyback MOSFETs have a thermal resistance of less than 1 °C/W to the exposed pad on the back of the package. Since this pad is referenced to the SOURCE pin (Source), it is at electrical ground potential and thus can be connected to the heat sink without need for electrical insulation. The high-side MOSFET is over-molded to achieve electrical isolation and thus also allows direct connection to the heat sink.

Design, Assembly and Layout Considerations

Power Table

The data sheet power table (Table 1, page 1) represents the maximum advised continuous power (thermally limited) based on the following conditions:

1. +12 V output PC main and +12 V standby.
2. A regulated DC input for main with a nominal voltage of 385 VDC and a minimum of 300 VDC.
3. HiperTFS-2 combined main and standby efficiency of 87% at full load.
4. Schottky high-efficiency output diodes.
5. DC input for Standby 115 VDC to 385 VDC.
6. Sufficient heat sinking and fan cooling to maintain heat sink temperature below 95 °C.
7. Transformer designed with nominal duty factor of 45%.

HiperTFS-2 Selection

Selecting the optimum HiperTFS-2 depends upon the continuous output power, peak power, thermal management, (heat sinking) and maximum ambient operating temperature. OEM applications typically specify 50 °C max ambient while clone PC supplies usually specify 25 °C ambient. Higher efficiency can be achieved by using a larger device and selecting a reduced device current limit. The maximum output power can be tailored for any given device by programming the device current limit for main and standby.

Main Frequency Selection

For single output applications 132 kHz operation is recommended for the main converter in order to reduce size and cost of the main transformer and output choke. With optimized magnetics design, the efficiency can match that of a 66 kHz design. For multiple output designs, 66 kHz operation is recommended to provide better voltage centering of the outputs.

Hold-Up Time

The input capacitor is a critical component to ensure meeting the specified minimum hold-up time. Proper design of the forward converter's nominal duty cycle and sufficient primary winding clamp voltage for sufficient magnetizing reset of the main transformer are also essential. PIXIs (PI Expert Design Spreadsheet) can compute these values, or refer to formula in AN-51.

Bias Support for High-Side Driver

The high-side MOSFET driver of HiperTFS-2 is internally biased by a high-voltage current source. For 66 kHz operation an external bias circuit is unnecessary. When using the internal bias, use 4.7 µF for C1. Using external bias support for 66 kHz operation may in some cases improve very light-load efficiency of the main converter.

External bias is required for 132 kHz operation. (D1, R1, and C2 in Figure 13) It is sourced from an ultrafast bootstrap diode (D1) from standby low-side primary bias (V_{AUX}) which should provide a typical minimum of 15 V at zero load on the standby converter to guarantee the 12 V bias required for the high-side driver. When using external bias, use a 0.1 µF VDDH bypass capacitor (C1). Note the value of R1 will be different for 66 kHz vs. 132 kHz operation.

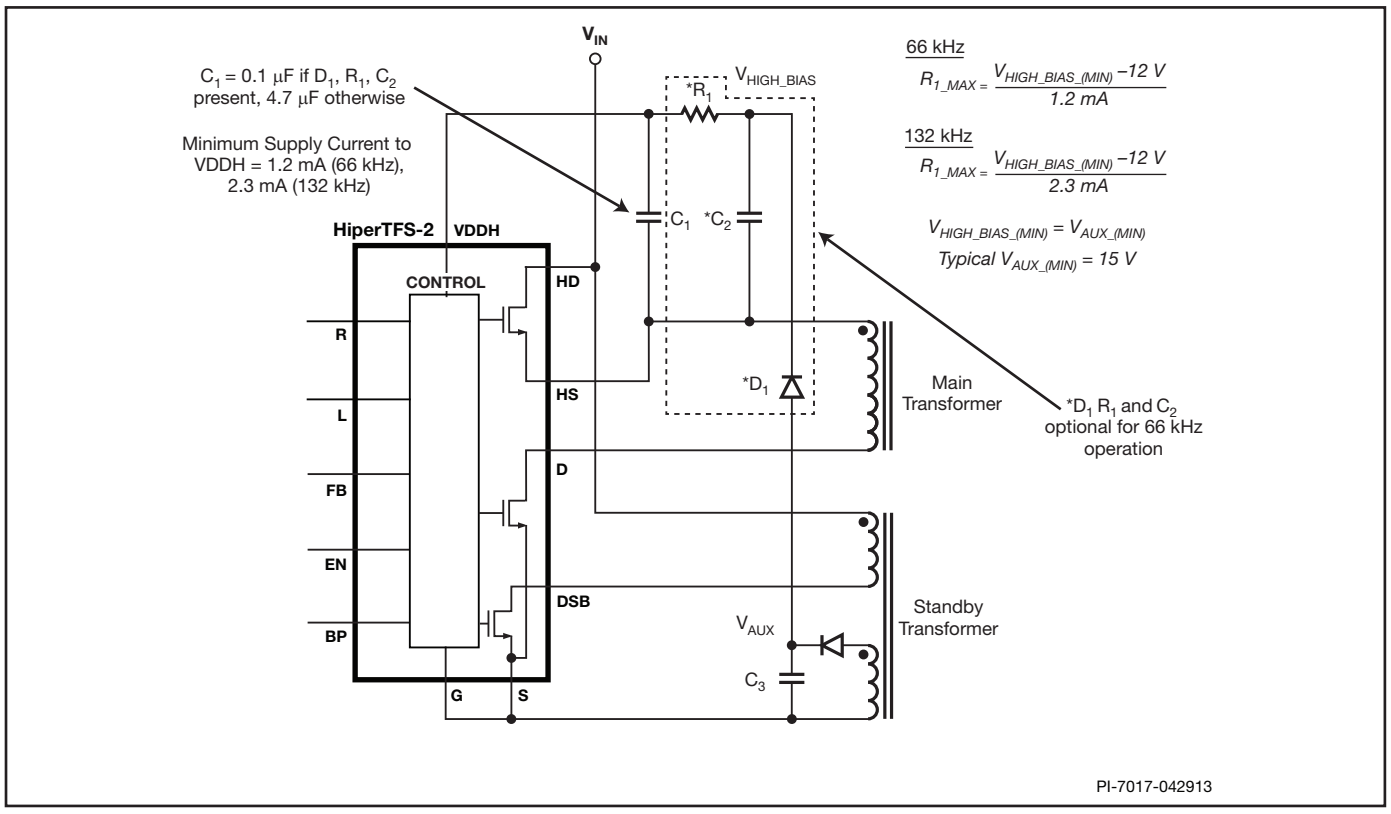


Figure 13. Bootstrap Supply for VDDH and Component Calculations. Typical V_{AUX_MIN} is 17 V. Typical Value is 1 kΩ for 132 kHz Operation, and 2 kΩ if the Bias Support Circuit is used for 66 kHz.

Primary Bias Support

The standby converter provides a minimum 15 V low-side bias output used to bias the BYPASS pin of HiperTFS-2 through a resistor to prevent the internal high-voltage bias current source from becoming active. The low-side bias output (V_{AUX}) is also the source for remote-on/off control circuitry and output OVP latching triggering circuitry. This output should be capable of delivering a minimum of 20 mA, plus any additional load from other primary-side circuitry such as PFC controllers. The primary V_{AUX} filter capacitor should be at least 330 µF to hold up the V_{AUX} during start-up and standby output load dump.

Soft-Start

Forward converters typically require a soft-start circuit on the main feedback loop to prevent output overshoot on start-up. This soft-start circuit closes the feedback loop while the output is still rising. However, this soft-start circuit by itself may not prevent a small output glitch during the output rise time, which can violate any output monotonicity specifications. To prevent this problem, the main feedback loop soft-start must work in conjunction with the HiperTFS-2 internal soft-start. The HiperTFS-2 main converter has two built-in soft-start mechanisms: the current limit, and a duty cycle limit, which starts at 30 % and opens to 78 % over 12 ms. The feedback loop soft-start (R11 and C5 in Figure 16) needs to close the feedback loop (opto needs to start conducting), and control the output rise while the HiperTFS-2 is still in the current limit startup phase.

EMI

The frequency jitter feature modulates the switching frequency over a small range as a means to reduce conducted EMI average and quasi-peak measurement associated with the harmonics of the fundamental switching frequency. This is particularly beneficial for average conduction mode where the sampling bandwidth is narrow. The modulation rate is nominally 250 Hz which is high enough to reduce EMI but low enough to have minimal effect on output ripple (rejected by the control loop).

Transformer Design

It is recommended that the transformer be designed for an AC p-p flux density of ~2900 Gauss during continuous operation at nominal input voltage and maximum output power, and a maximum peak-peak transient flux density no greater than 4000 Gauss. The turns ratio should be chosen for a nominal duty factor of 45% at 385 VDC input. This yields a good compromise between switching RMS currents, output diode voltage ratings, and minimum input voltage at the end of hold-up time.

Even though leakage inductance energy is partially recycled, low-leakage-inductance construction (e.g., split primary, secondary is sandwiched between series primary halves), is recommended.

For optimal main and standby transformer design refer to AN-51 and use PIXIs spreadsheet. Foil secondary windings are recommended for outputs above 10 A.

Primary Clamp Scheme

Figure 2 shows two primary clamp schemes. Clamp-to-rail offers higher efficiency, while clamp-to-ground allows regulation down to a lower input voltage, extending hold-up time or allowing use of a smaller input bulk capacitor. The HiperTFS-2 spreadsheet allows selection of either scheme.

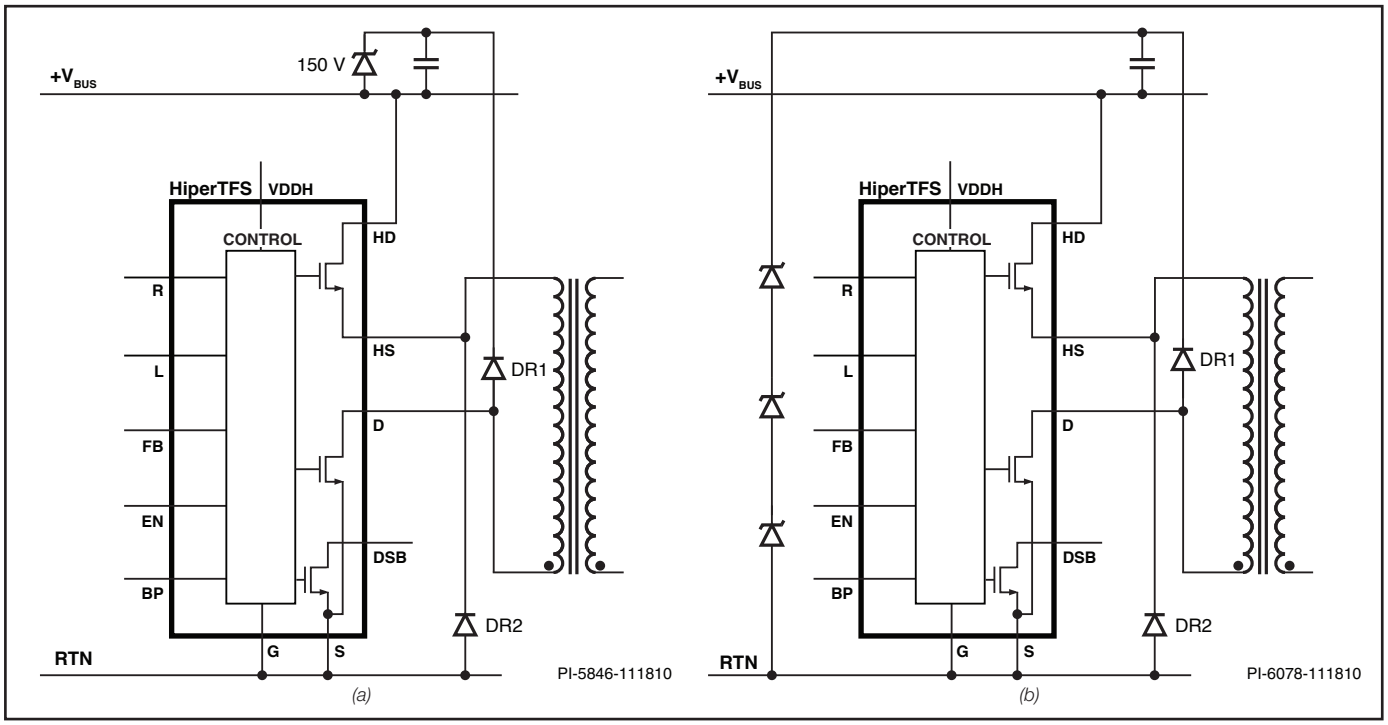


Figure 14. Two Primary Clamp Schemes, (a) Clamp-to-Rail (Higher Efficiency) and (b) Clamp-to-Ground (Enables Output to Stay in Regulation to a Lower Input Voltage).

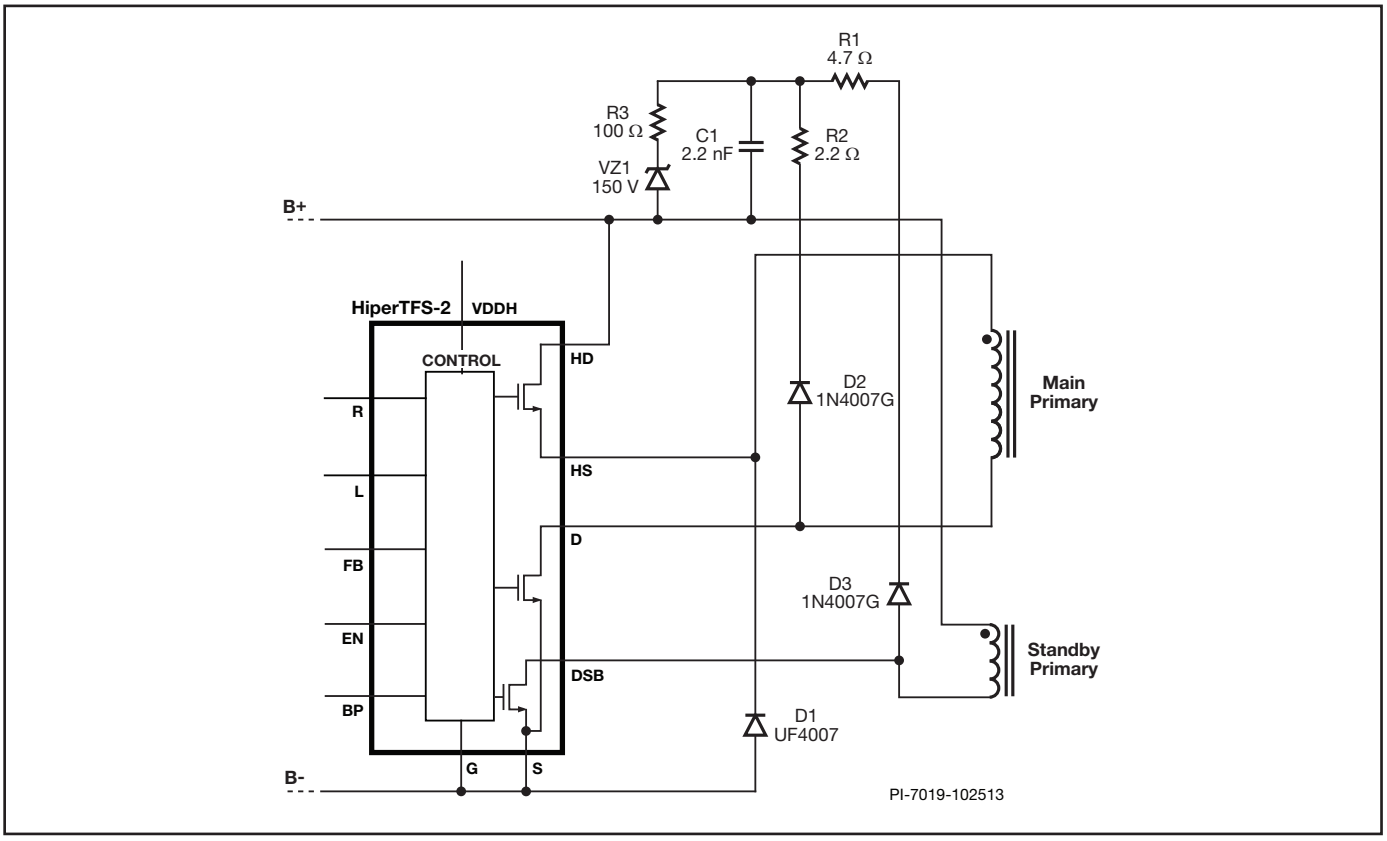


Figure 15. Standard Values for Clamp-to-Rail Scheme. These Work Well for all Power Ranges and both 66 and 132 kHz. Using Standard Recovery Diodes for CR2 and CR3 Allow for Partial Recycling of Leakage Inductance Energy and Improve Efficiency. R1 and R2 Limit Peak Reverse Current and Provide Some High Frequency Damping, and R3 Allows VZ1 to Work as a "Bleed" Instead of a Hard Clamp, to Improve Efficiency.

Output Choke

The use of iron powder (lower cost) or Sendust ("Kool-Mu", higher efficiency) core material is recommended. The inductance of a powdered iron or Sendust core varies significantly with load. At light load the inductance is much higher than at full load, which allows a forward converter to remain in continuous conduction mode (CCM), down to very light load.

For multiple outputs the inductor turns ratio should be the same as the main transformer secondary. Spreading the windings equally throughout the toroid improves coupling and cross-regulation.

Output Capacitors

The output capacitors in a forward converter do not see high AC ripple currents. Very-low ESR capacitors are not necessary. However the ESR of the capacitors have a direct effect on output ripple voltage (if no post-filter is used) and on fast load-transient response. The capacitance has an effect on medium-speed load-transient response. Polymer (solid electrolyte) capacitors are not necessary but can be used for output capacitors if very small size is required. However, their small capacitance may require an additional, low-cost (moderate ESR) electrolytic capacitor in parallel, to maintain sufficient capacitance for loop stabilization and transient response.

Standby Mode Consumption

To improve the standby converter's light load efficiency, a 7.5 kΩ bias resistor should be connected from V_{AUX} to the BYPASS pin. This will turn off the internal high-voltage current source that otherwise powers the BYPASS pin.

Heat Sinking

The HiperTFS-2 package is eSIP-16F. There is a metal exposed pad that provides a low thermal resistance path to the heat sink for the low-side main MOSFET and standby power MOSFET. There is also an over-molded, electrically isolated section on the back of the package that provides isolation between the heat sink and the internal high-side main MOSFET. The heat sink temperature behind the device should not exceed 95 °C to provide sufficient thermal margin to avoid activating over-temperature shutdown. The device does not require Insulation pad (SIL pad). See Power Integrations' website "Mounting with Plastic and Metal Clips". Clip to provide 20N of clamping force (15N min, 50N max). Thermal heat sink compound is required for optimal thermal performance.

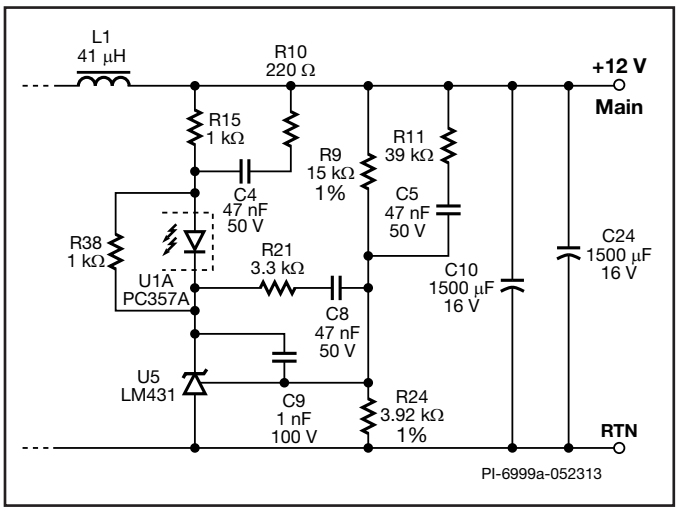


Figure 16. LM431 Feedback Loop Components.

Feedback Loop Design

The HiperTFS-II is a voltage-mode controller. The main forward plant feedback loop poles and zeros are:

- Output LC filter double pole – typically at 800 Hz, slightly underdamped.
- Output capacitor ESR zero – typically at 3-5 kHz.
- Optocoupler and FEEDBACK pin system pole – typically at 8-12 kHz. (The HiperTFS-2 has a low impedance FEEDBACK pin to improve optocoupler bandwidth)

See Figure 16, the compensator should have a:

- Pole at the origin (an integrator to minimize steady-state error). This is implemented by C9.
- A Zero near the LC double pole location. This is implemented by R21 in conjunction with C8.
- A phase-boost circuit, centered near the crossover frequency – implemented with R10 and C4. This will improve phase margin and increase the crossover frequency.

With the above compensation, and with the use of low ESR electrolytic capacitors, a gain crossover frequency of 7-9 kHz with a gain margin of >55° is achievable.

Resistor R11 and C5 are for soft-start. They do not contribute significantly to the gain-phase characteristic.

Resistor R15 should be sized to conduct approximately 10 mA when the TL431 is fully “ON” or saturated (2.5 V on the cathode). It is also an overall gain-setting resistor, affecting the entire frequency range. It, along with the phase-boost network (R10 + C4), are the main high-frequency gain setting components.

Resistor R38 is to provide the minimum bias current for the LM431. Capacitor C9 rolls off the LM431 gain at very high frequencies.

Overvoltage Protection

An overvoltage protection circuit can be implemented by sourcing >15 mA into the BYPASS pin to cause latching shut-off of both converters. Resetting requires the BYPASS pin voltage to fall below 4.8 V.

Layout Considerations

Source and Ground Pins

Connect SOURCE and GROUND pins together on the PCB. All high current traces (e.g., from bulk capacitor), should route to the SOURCE pin. All small signal traces, and low voltage bypass capacitors, should be connected to the GROUND pin. See Figure 17. If this rule is violated, the connection in question must be very close to the SOURCE or GROUND pin.

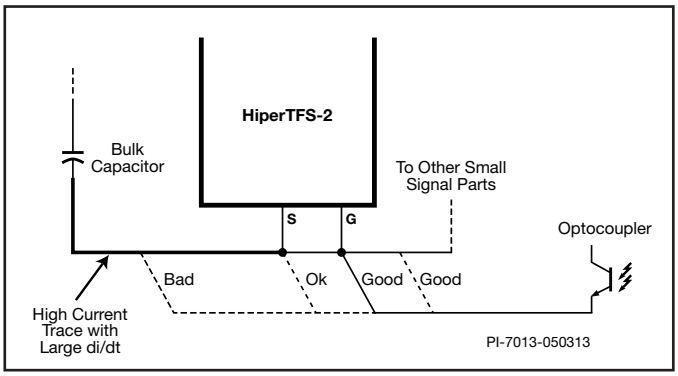


Figure 17. The PCB Trace from the Bulk Capacitor to the SOURCE Pin Contains Currents with Large di/dt. Do not Return any Small Signal Ground Connections to this Trace, Such as Small Signal Bypass Capacitors, or Optocouplers.

Bypass Capacitors

The BYPASS pin and ENABLE pin bypass capacitors must be connected with short traces to the GROUND pin. Likewise, the VDDH bypass capacitor must be connected with short traces to the HIGH-SIDE SOURCE pin.

Primary Return (B-) Routing for HiperTFS-2 and PFC MOSFET

When the HiperTFS-2 shares a heat sink with a HiperPFS or other PFC MOSFET, there is potential for noise coupling to cause misbehavior, due to the very high di/dt associated with the PFC diode reverse recovery. The metal in the backside of the HiperTFS-2 is internally connected to the SOURCE pin and thus the heat sink will be at SOURCE pin potential. The heat sink should not be used to conduct current. The HiperTFS-2 requires a dedicated PCB trace from the SOURCE pin to the bulk capacitor B- pin. The HiperPFS (or PFC MOSFET Source) requires a separate PCB trace to the bulk capacitor B- pin. The bulk capacitor is preferably placed between the HiperPFS and HiperTFS-2. The heat sink must have a single connection to the PFC SOURCE pin, which must be as close as possible to the PFC MOSFET. Because of the PFC’s higher di/dt, the bulk capacitor should be closer to the PFC than to the HiperTFS-2. See Figure 18.

Standby Primary Bias (V_{AUX}) Capacitor Ground Routing

The primary V_{AUX} output filter capacitor negative terminal should be routed to the bulk capacitor B- terminal. This is to prevent the large noise currents that flow during common-mode surge and ESD, from flowing in the HiperTFS-2 small-signal PCB ground traces and creating ground bounce issues.

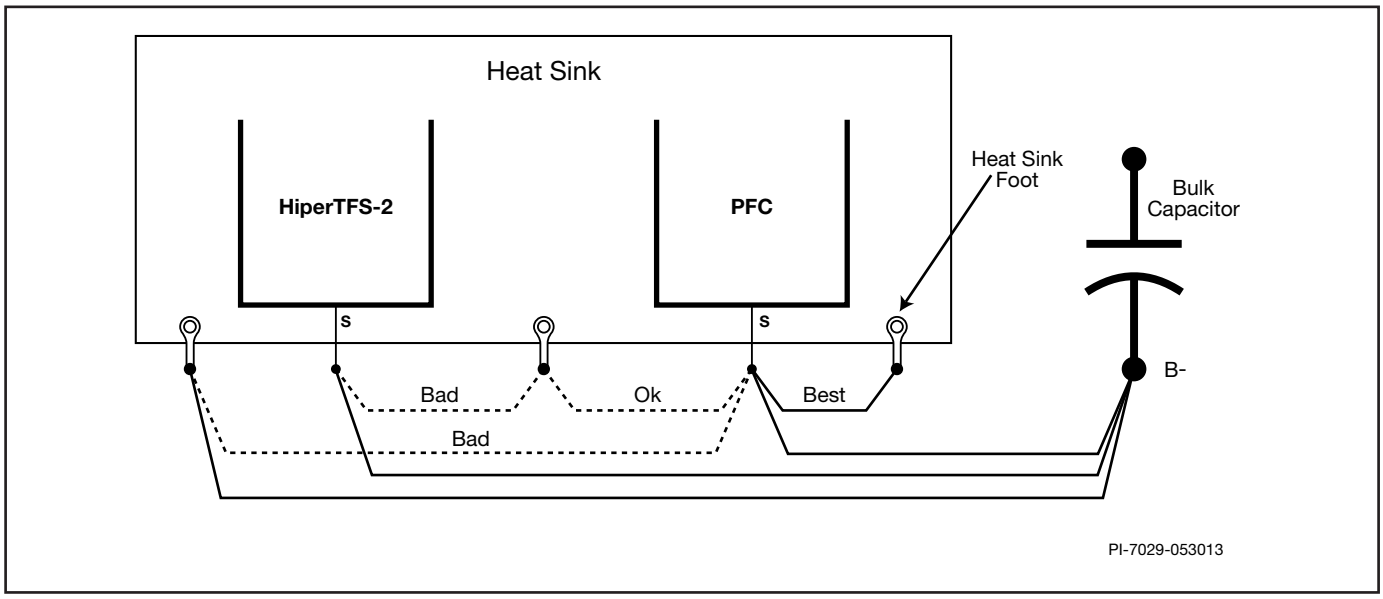


Figure 18. Proper Heat Sink, TFS-2, and PFC Connections to the Bulk Capacitor, are Necessary to Prevent Interference. PFC and HiperTFS-2 both need Dedicated Return Traces to Bulk Capacitor B-. Bulk Capacitor is PReferably Placed Between the PFC and HiperTFS-2.

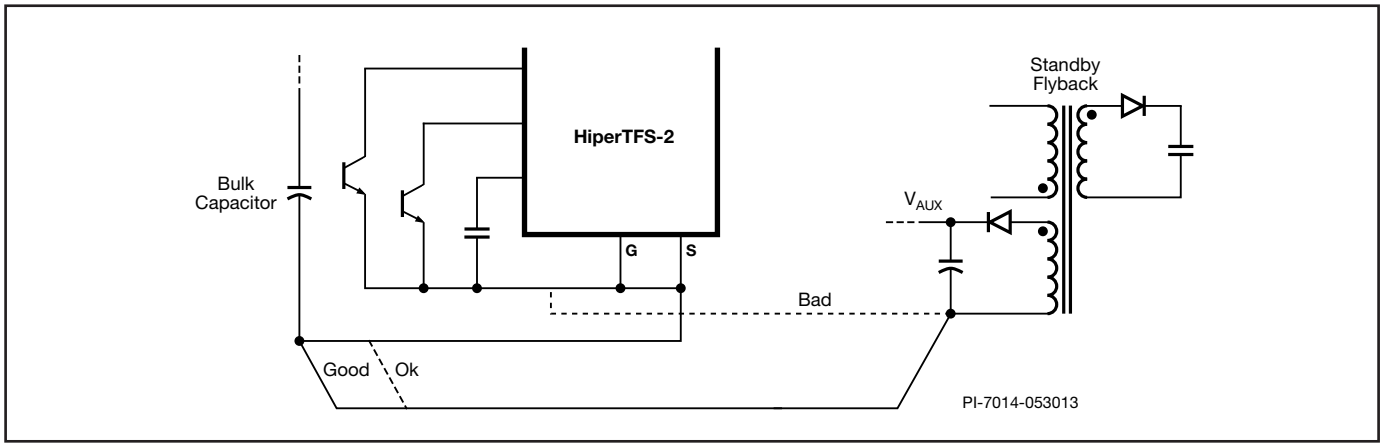


Figure 19. The (-) Terminal of the V_{AUX} Capacitor Should be Connected to B- of the Bulk Capacitor, and not to the Ground Traces. This will Improve Lightning Surge and ESD Immunity, due to Capacitive Displacement Currents Flowing Through the Primary-to-Secondary Capacitance in the Flyback Transformer.

Y Capacitor Connections

Y class safety capacitors connected across the isolation barrier, should be routed directly to the positive of the bulk capacitor, and preferably to B+ instead of B- to divert surge and ESD currents away from the HiperTFS-2 small signal components and PCB traces. See Figure 20.

This will also improve surge and ESD immunity. The secondary-side of the Y capacitor should be connected to the main transformer secondary return pin. This will reduce the height of thin “spikes” coincident with the main converter switching edges in the output ripple, which comes from common-mode switching noise. See Figure 21.

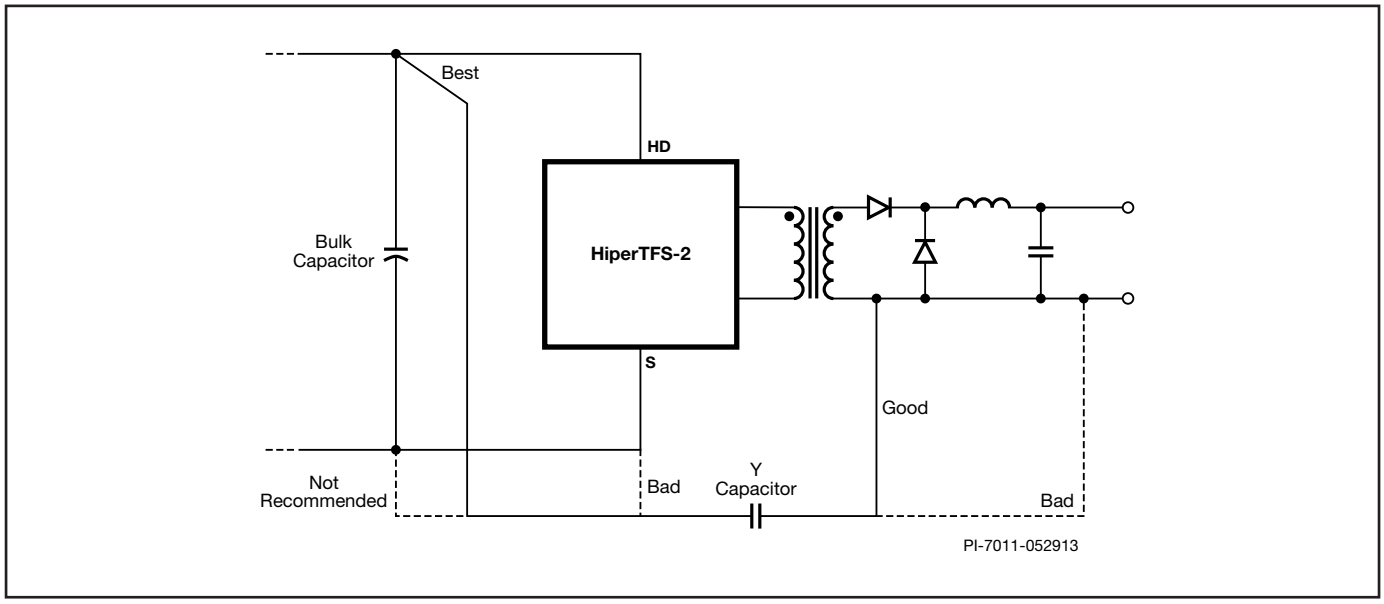


Figure 20. Recommended Y Capacitor Connections to Improve Surge and ESD Immunity and Output Ripple High-Frequency Noise.

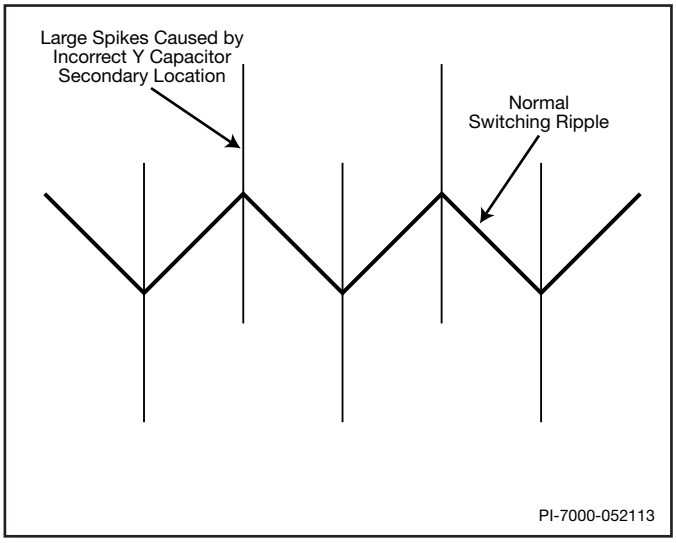


Figure 21. Close-up of Output Ripple Voltage Showing Large Spikes. These Spikes are Often Caused by Common-Mode Switching Noise Appearing in the Output. A Poor Secondary Layout or a Y Capacitor Connected to the Output Connector Instead of to the Transformer Secondary GROUND Pin, can Cause the Spikes.

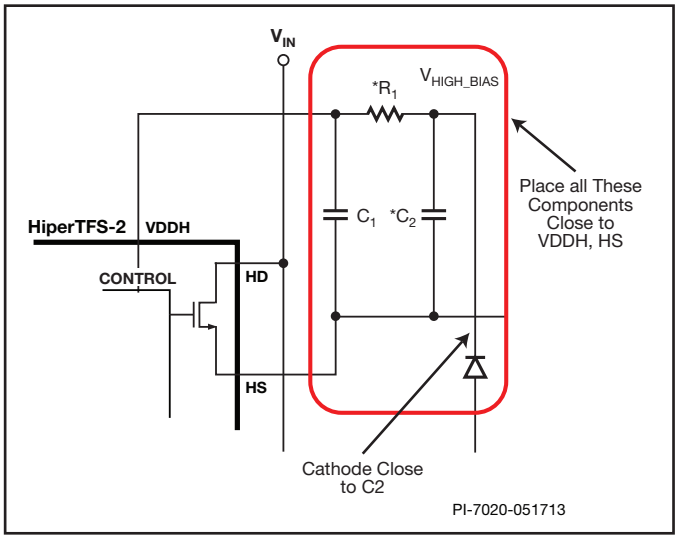


Figure 22. VDDH Components Exhibit Large dv/dt and Should be Mounted Close to the HIGH-SIDE SOURCE and VDDH pins. The Diode Should be Mounted Close to the VDDH Pin so that the Cathode Trace can be Made Short. The Anode Trace is Connected to V_{AUX} and is Quiet.

STANDBY DRAIN, MAIN DRAIN, HIGH-SIDE SOURCE, and HIGH-SIDE OPERATING VOLTAGE Pins

The STANDBY DRAIN, MAIN DRAIN, HIGH-SIDE SOURCE, and HIGH-SIDE OPERATING VOLTAGE pins are high-voltage switching nodes with high dv/dt and must be kept away from the traces connected to low voltage small signal pins (i.e., LINE-SENSE, RESET, FEEDBACK, ENABLE pins). Stray capacitance between them will cause capacitive noise injection. The small components connected to the HIGH-SIDE OPERATING VOLTAGE pin also have high dv/dt with respect to the other small signal traces. Place them close to the HIGH-SIDE OPERATING VOLTAGE pin and away from the other small signal traces. Also place the bootstrap diode (if used, required for 132 kHz), close to the HIGH-SIDE OPERATING VOLTAGE pin.

LINE-SENSE and RESET

Care must be taken to avoid noise injection into the LINE-SENSE and RESET pins. These pins have multiple series resistors in order to reduce the voltage stress per resistor. See Figure 23. The series resistors in each chain do not have to be the same type or value. If they have different maximum voltage ratings, they should have different values, proportional to their voltage ratings. If the resistors are different types with different withstand voltage ratings, (e.g., 0805 SMD for R25 and R36,

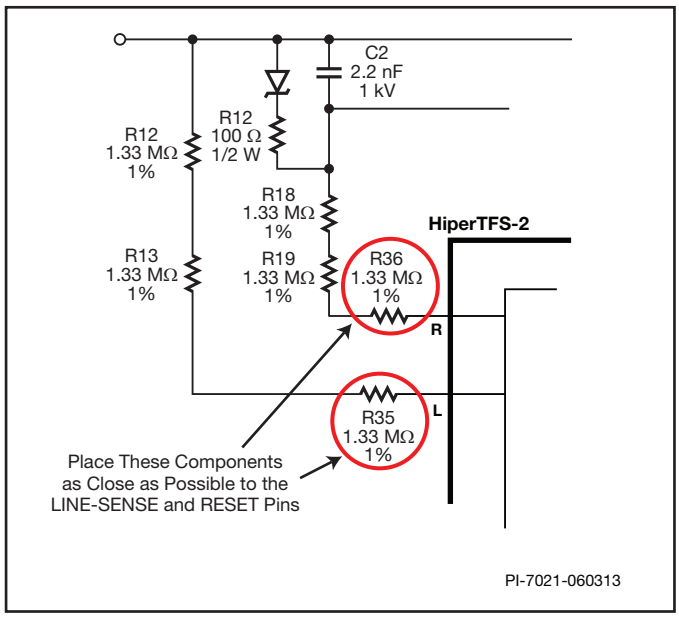


Figure 23. LINE-SENSE and RESET Pin Resistor Chain. The Highlighted Resistors Should be SMD Type and Placed as Close as Possible to Their Respective Pins.

and through-hole for the others), their values should be proportional to their voltage ratings (while maintaining the correct total series value).

The last resistor in the series chain, should be connected to the LINE-SENSE and RESET pins, (R35 and R36 in Figure 23) must be SMD type and placed very close to their associated pins.

The traces that feed these pins, and the additional series resistors, should not be placed close to any high dv/dt traces and areas with high-voltage switching. Noise on these pins may cause distortion of the various functions determined by the LINE-SENSE and RESET pins, such as LINE-SENSE pin UVLO, and LINSE-SENSE and RESET pin duty cycle limiting. For optimal performance, the LINSE-SENSE and RESET pins are located in between the BYPASS and GROUND pins which have DC voltages, so that the traces connecting to the DC voltages can act as Faraday shields for the traces connected to the LINSE-SENSE and RESET pins. See Figure 24.

Feedback and Enable Pins

The FEEDBACK and ENABLE pins should likewise be kept away from noisy, high-voltage switching areas. If it is unavoidable to have long traces connecting to FEEDBACK pins, then route these traces parallel to and close to, quiet, low impedance traces that act as Faraday shields, such as V_{AUX} or BP.

Transformer Secondary and Output Diodes

Flyback Layout

The diode and output capacitor should be mounted close to the secondary winding and routed with short traces. The standby primary bias (V_{AUX}) capacitor and diode should be mounted close to the winding.

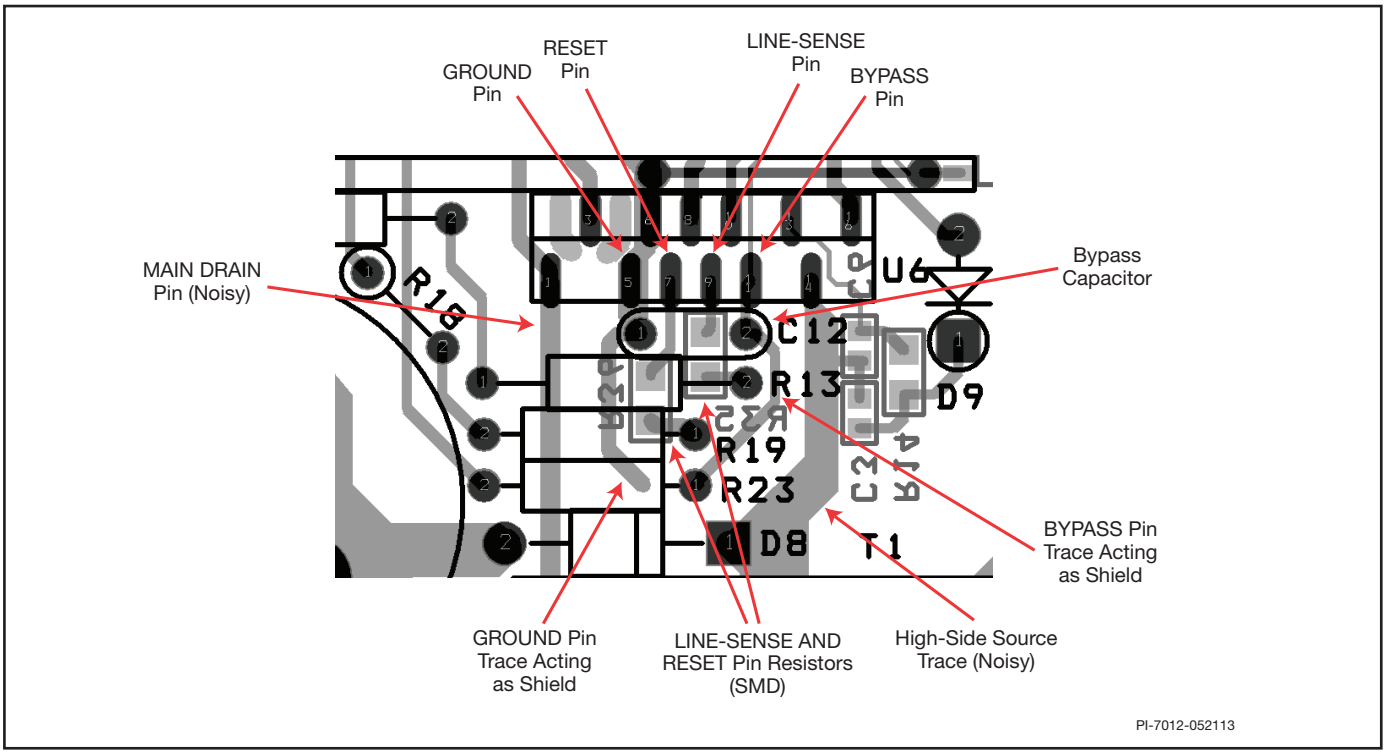


Figure 24. LINE-SENSE and RESET Pin Resistor Layout. The 2 Resistors Connected to LINSE-SENSE and RESET Pins Should be SMD, and the GROUND and BYPASS Pin Traces Provide Faraday Shielding Against the HIGH-SIDE SOURCE and MAIN-DRAIN Pin Traces. The Bypass Capacitor is Through-Hole Type so that the Traces Connecting to the Pins can be Very Short.

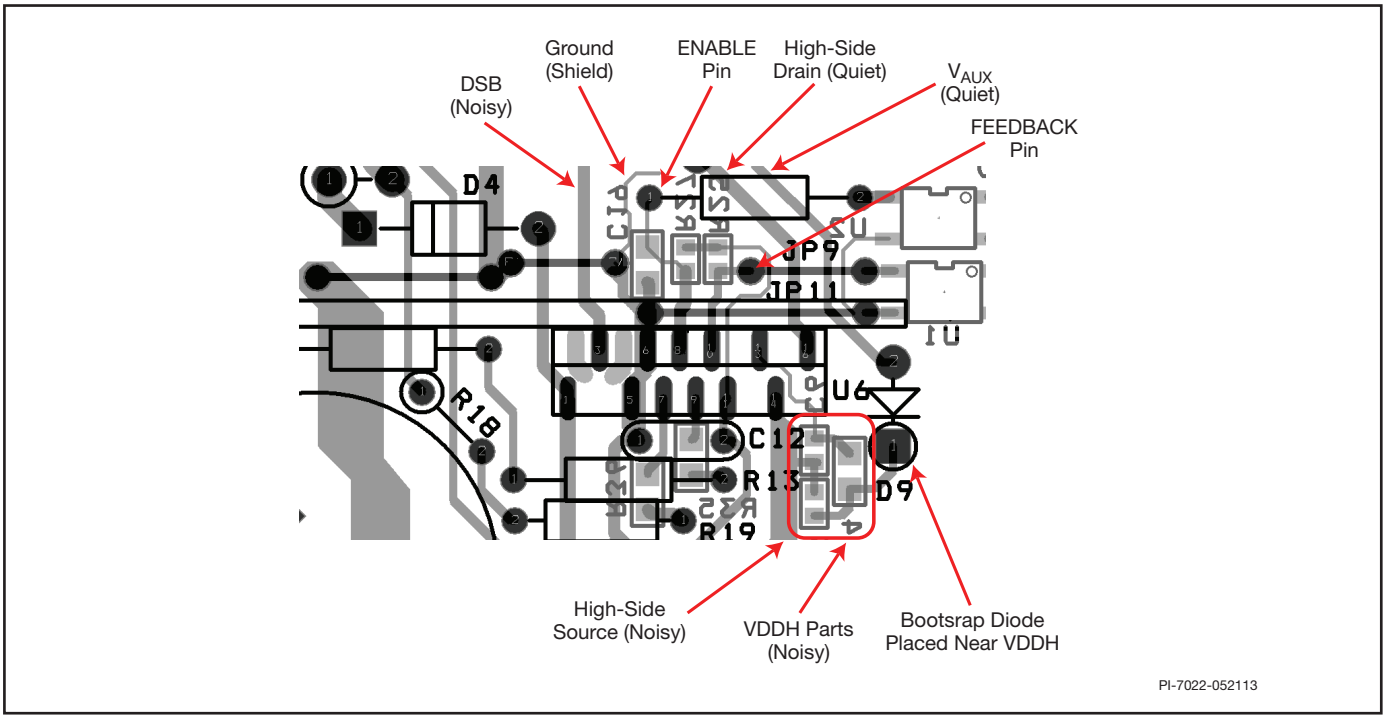


Figure 25. Layout Around ENABLE and FEEDBACK Pin. Use Quiet Traces as Faraday Shields from Noisy Traces, Especially if the Traces to the Optocouplers are Long.

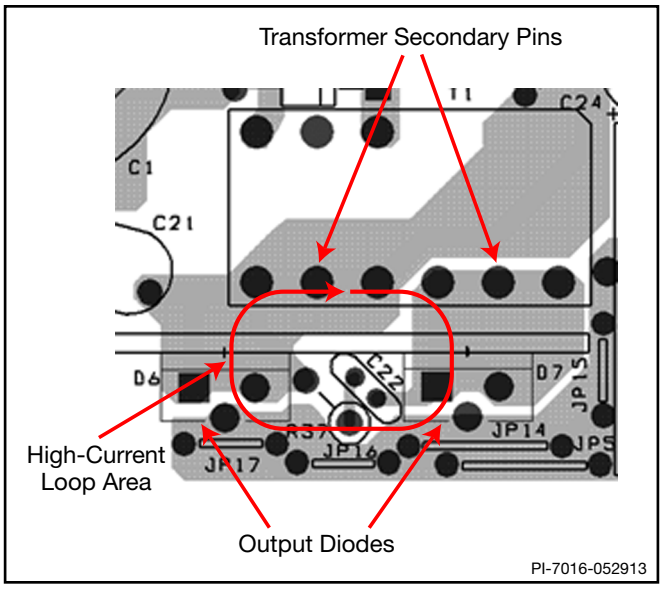


Figure 26. Layout of Forward Transformer Secondary and Output Diodes. The Diodes and Secondary Pins Should be Mounted Close Together, to Minimize the Loop Area They Form.

Main Converter Typical Waveforms

Main Transformer Primary Inductance and Resonant Frequency

At zero load, check the resonant frequency visible in the Drain voltage. This is the resonant frequency between the primary inductance and the total capacitance reflected to the primary (MOSFETs, transformer self-capacitance, output diode capacitances). See Figure 27. A low resonant frequency can prevent proper core reset at low-line and continuous-mode light load, and can lead to core staircase saturation. See Figure 29. Too much primary inductance causes the Drain rise time to be very slow, eroding core reset volt-seconds. If the measured resonant frequency is below 120 kHz (for 132 kHz operation), or below 60 kHz (for 66 kHz operation), reduce transformer primary inductance by increasing core gap. This initial test is a rule of thumb. The final test is to check for complete core reset at very low input voltage (just above the main UVLO threshold), at a light load that is just above borderline continuous operation. Reducing primary inductance below the value necessary for complete core reset, will reduce efficiency.

Full Load

Figure 16 shows the typical full-load waveform. Check high-side V_{COSS} at turn-on. It is typically below 40% of the input voltage. If it is greater, ensure that the low-side MOSFET clamp diode is a standard-recovery (slow) rectifier (1N4007) and the high-side MOSFET clamp diode (to ground) is an ultrafast type (e.g., UF4005). Reducing the primary inductance by 20-30% will also decrease this voltage, and in some cases may improve full load efficiency.

Flyback Standby Converter

The data sheet standby max power rating represents the minimum practical continuous output power level that can be obtained under the following assumed conditions:

1. The minimum DC input voltage is 115 V.

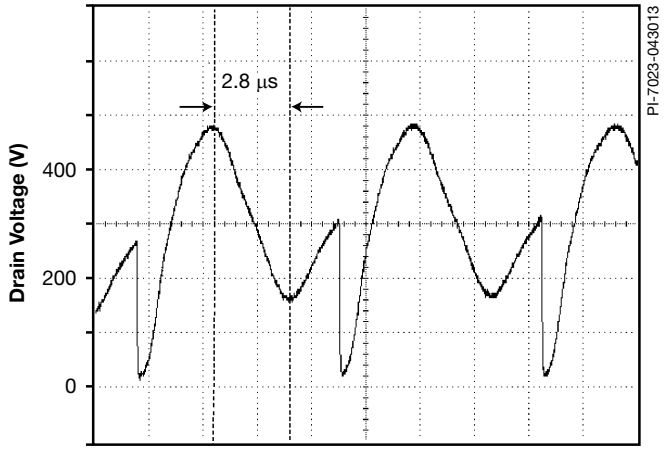


Figure 27. Drain Voltage at Zero Load, to Measure Magnetizing Resonant Frequency. In the Above Example, the Cursors Were Set to Measure a Half-Cycle. The Resonant Frequency calculates as f_O = 1/(2.8 µs × 2) = 177 kHz.

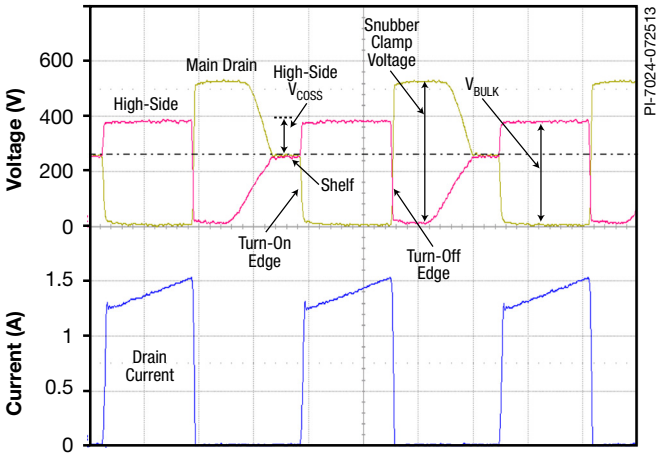


Figure 28. Typical Full Load Waveforms of the Main Drian. High-Side MOSFET Source, and Drain Current.

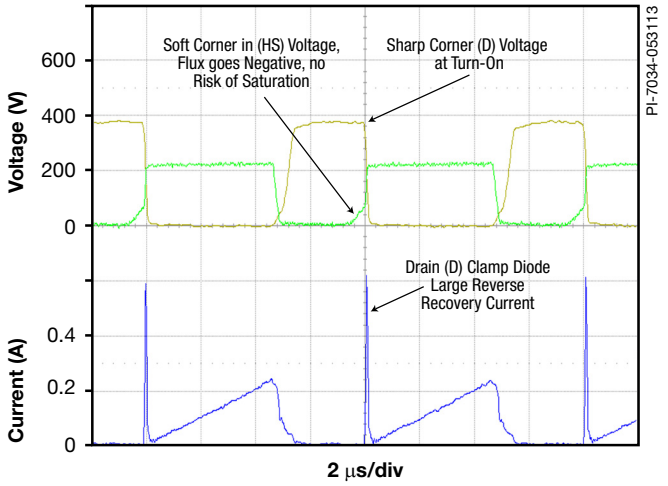


Figure 29. Low-Line Operation (Just Above Main UV-OFF Threshold), with Load in Borderline Continuous Mode. The Output will be out of Regulation. This is the Condition to test for Complete Core Reset. The Soft Corner in the (HS) Voltage at Turn-On Signifies Reversal of Magnetizing Current and thus Complete Core Reset. The Sharp Corner in the Drain (D) Waveform Signifies Hard-Reverse Recovery in the Drain (Standard-Recovery) Clamp Rectifier. This is Acceptable for Transient Conditions (e.g., Hold-Up Time)

2. Efficiency of 80% at full load, minimum nominal input.
3. Minimum data sheet value of I^2f.
4. Transformer primary inductance tolerance of ±10%.
5. Reflected output voltage (V_{OR}) of 100 V.
6. Voltage only output of 5 V with a Schottky diode.
7. Continuous conduction mode operation with transient K_P* value of 0.25.
8. Highest standby current limit selection.
9. Heat sink max temperature is 95 °C.

*Below a value of 1, K_P is the ratio of ripple to peak primary current. A transient K_P limit of ≥0.25 is recommended to prevent reduced power capability due to premature termination of switching cycles. Due to the initial current limit (I_{INIT}) being exceeded at MOSFET turn-on.

Reducing No-Load Consumption

The BYPASS pin can be powered from the internal high-voltage current source from the HIGH-SIDE DRAIN pin, but R16 (7.5 kΩ) in Figure 30 will reduce no-load consumption by providing the BYPASS pin current from a lower voltage and inhibiting the internal high-voltage current source.

Audible Noise

Standard dip varnishing on the standby transformer will prevent the possibility of audible noise in the standby converter. Additionally, the peak core flux density should be kept below 3000 Gauss (300 mT). Vacuum impregnation of the transformer is not recommended because it will increase standby no-load losses due to the increased primary capacitance. Higher flux densities are possible, however careful evaluation of the audible noise performance should be made using production transformer samples before approving the design. Ceramic capacitors that use dielectrics such as Z5U, when used in clamp circuits with high ripple voltage, may also generate audio noise. If this is the case, try replacing them with a capacitor having a different dielectric or construction, for example a film type.

Recommended First-Time Power-Up Procedure

Place a small, fast-blow low-capacity fuse between the bulk capacitor and the HiperTFS-2 circuitry. Use a current-limited bench power supply to power the HiperTFS-2 converter instead of using the PFC or the AC mains. Be careful using a programmable bench AC source in DC mode, because when they are loaded with a large bulk capacitor and their output is turned off, the output of the AC source can undershoot to a negative voltage and damage the HiperTFS-2. If a remote-on circuit is present, keep it OFF so that only the standby will run. Place a voltage and current probe on the STANDBY DRAIN pin. Raise the bulk capacitor voltage slowly until the standby turns on. Check for proper waveforms (peak voltage, and check for core saturation) and for output regulation. Check the VAUX voltage. Check for over-heating components. Slowly increase the load and the input voltage. Check for over-heating components again.

Place voltage probes on DRAIN and HIGH-SIDE SOURCE pins. Place current probe in DRAIN pin. If a remote-on circuit is present turn remote to ON. Keep input voltage below UV start threshold (typically 330 V). Slowly increase input voltage until main converter starts. Check for proper waveforms and for output regulation. Check for over-heating components, especially the Drain clamp diode, and associated snubber components. Slowly increase input voltage and load. Check for over-heating components again.

Quick Design Checklist

Flyback

1. Maximum standby drain voltage – Verify that DSB voltage does not exceed 675 V at highest input voltage and peak (overload) output power. This 50 V margin to the 725 V BVDSS specification gives margin for unit-to-unit variation.
2. Maximum DSB current – At maximum ambient temperature, maximum input voltage and peak output (overload) power, verify Standby Drain current waveforms for any signs of transformer saturation and excessive leading edge current spikes at start-up. Repeat under steady-state conditions and verify that the leading edge current spike event is below $I_{LIMIT(N)(MIN)}$ at the end of the $t_{LEB(MIN)}$. Under all conditions, the maximum Standby Drain current should be below the specified absolute maximum ratings.
3. Thermal check – With main converter off (and any system fans are also off), at specified maximum output power, minimum input voltage and maximum ambient temperature, verify that the temperature specifications are not exceeded for the HiperTFS-2, transformer, output diode, and output capacitors.

Main (Forward) Converter

Examine the voltage and current at 20% load and nominal input voltage. Measure and check the following:

- Switching frequency
- Duty cycle
- Peak voltage

Repeat the measurements at full load. Be cautious of over-heating the power supply and use a strong fan. Measure the source voltage (HS) of the high-side MOSFET at turn-on for each steady-state switch cycle (Figure 28). It should be < 40% of the bulk voltage. Calculate and verify the K_P from the current waveform and verify with the spreadsheet. Also check the peak current at peak load – do not dwell at peak load for more than several seconds to prevent over-heating.

Check for any oscillation visible in the Drain current envelope.

Start-Up

Examine the start-up voltage and current. The peak start-up current should be close to the I_{LIMIT} of the device. Examine the output voltage monotonicity. Check for the high-side misfiring during start-up. If the bootstrap diode is omitted (66 kHz only), the VDDH capacitor should be ≥4.7 µF to prevent misfiring. Start-up should be acceptable with either the remote-on/off switch, or by bringing up the HVDC supply with remote-on already asserted. Check startup at maximum expected input voltage.

Brown-Out

At full load, reduce input voltage until the output just falls out of regulation. Note the HVDC input voltage, measure the duty cycle, and check the waveforms for complete core reset. Reduce the input voltage further until the output just drops below regulation (it is now in “LR mode”) while checking for complete core reset further reduce input voltage to find the voltage at which the converter shuts off (main UVLO)

Temperatures

Use a thermal camera and check device hotspot temperature, and the temperatures of the snubber components, output diodes, and magnetics.

Light Load

Examine the high-side MOSFET Source waveform at very light load. As the load is reduced, the duty cycle will begin to reduce, and at light enough load the high-side Source voltage will not reach ground. Keep reducing the load and check for misfiring in the high-side MOSFET. At 132 kHz operation, some misfiring at very light load may occur, but it should occur at such low duty cycles that any audio noise in the main transformer will not be audible if the transformer is dip-varnished.

Loop Stability

As a first check, do a load step of 50% -> 100% load, and check for oscillation or excessive ringing. Also check from 100% to peak load (be careful to avoid over-heating when operating at peak load).

Check for cross-talk between the forward and flyback outputs. When a load transient is applied to one output, the other output should only show a very small perturbation, well below the output ripple specification.

Use a gain-phase analyzer and check gain and phase margin at full load. Also check the minimum phase at lower frequencies. Check minimum phase at reduced load (just enough for continuous mode operation).

Design Example

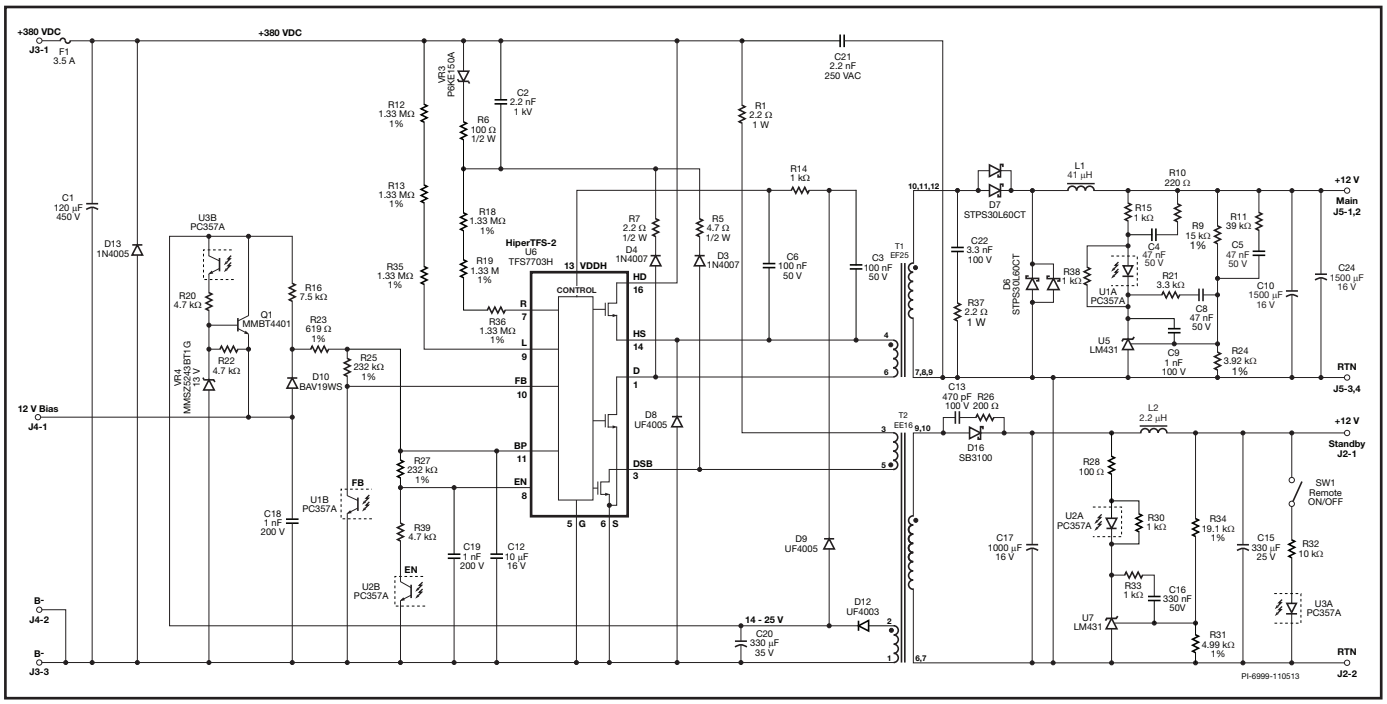


Figure 30. Design Example: 12 V / 15 A Main Output, 12 V, 0.83 A Standby.

High-Efficiency +12 V, 15 A Main Output and 12 V, 0.83 A

The circuit in Figure 30 is an example of a design using HiperTFS-2 providing a 180 W +12 V forward main converter and a 10 W, 12 V standby output from the flyback controller of HiperTFS-2. The very high integration of two full converters within a single package immediately shows the result of very low external parts count for the entire design. Both the main converter and the flyback section of HiperTFS-2 are designed to provide very high-efficiency.

The main converter takes advantage of the ability to operate above 50% duty factor which lowers RMS switch currents and allows using lower voltage more efficient Schottky diodes on the output. The flyback standby section uses Power Integrations' TinySwitch technology which is often used in designs that demand high-efficiency and low no-load input power consumption. The design in Figure 30 is intended to work with a PFC boost front end that nominally provides a 385 VDC input. The main converter will regulate to full load between 300 VDC and 385 VDC. This voltage range guarantees greater than 20 ms hold-up time with C1 (120 µF). R27 selects the 650 mA standby MOSFET current limit, and R25 selects the 3.24 A main converter current limit. The standby section is designed to operate whether the boost PFC stage is on or off. The standby therefore is designed to operate from 100 VDC to 385 VDC which covers the normal universal input of 90 VAC to 265 VAC.

The start-up sequence is initiated with HiperTFS-2 charging the BYPASS pin capacitor via the internal high-voltage current source. Current limit selection then follows via FEEDBACK pin and ENABLE pin resistors. The HiperTFS-2 then senses the input voltage via the LINE-SENSE pin resistor series chain R12, R13, R35. When the input voltage reaches 100 V VDC the LINE-SENSE pin UV standby threshold is reached and the standby converter turns on. After several milliseconds the standby output will reach regulation and the primary V_{AUX} 14-25 V bias will be stable. R16 (7.5 kΩ) will provide bias current for the operating current of the BYPASS pin to inhibit the internal high-voltage current source to reduce zero-load consumption.

When the input bulk voltage reaches 336 VDC which is the UV threshold for the main converter, the main converter will initiate a turn-on sequence once the remote-on command from secondary is activated. The remote-on switch (SW1) on the secondary-side for this particular design allows the user to manually activate that main converter by turning on the remote-on optocoupler. In actual PC designs the remote-on would be controlled by a computer start-up command.

This optocoupler sources 6 mA (set by R23) into the BYPASS pin of the HiperTFS-2 which is greater than the threshold current to start the turn-on sequence for the main converter. The main converter will first turn on the bottom switch to allow the high-side drive to receive the bootstrap bias. After 60 ms the main converter will start switching both high-side and low-side main switches at 132 kHz (set by the value of C12 which is 10 µF) and the main output voltage will rise. Once the regulator U5 becomes active, current will flow through the optocoupler U1. The collector of U1 will sink current out of the FEEDBACK pin to adjust for appropriate duty cycle to maintain regulation. The normal operating sink current is between 1 mA and 2 mA. D9 provides bootstrap charging for the high-side driver supply pin VDDH. R14 limits the current from the bootstrap.

During normal and brown-out operation the RESET pin senses the turn-off clamp voltage via the resistor chain R36, R18, R19 and the internal controller determines the maximum safe duty factor by comparing the RESET pin current with the LINE-SENSE pin current. This feature guarantees that saturation of the transformer is completely avoided in all conditions including brown-out and load transients.

The LINE-SENSE pin also has a UV low threshold which turns off the main converter when the input voltage is below 212 V. This design in particular is intended to operate with a forced air cooling at full load to maintain a heat sink temperature below 95 ºC at full load at worst-case ambient temperature. The standby uses auto-restart to protect the standby output from output overload. The main output is current limited by the selected internal primary current limit of the main switch path.

See PCB layout in Figure 31. HiperTFS-2 small signal pin decoupling capacitors are placed close to the HiperTFS-2. Small signal components and traces connected to the HiperTFS-2 are kept away or shielded from traces with large switching voltages. The optocouplers are placed to minimize capacitive coupling between their signal traces, and traces with high-voltage switching. Small signal ground return, and ground traces that conduct large switching currents, are segregated. Proper PCB clearance is observed between the high-voltage pins and traces, and low-voltage traces and components.

The Y capacitor (C21) is placed so that it has short direct connections to the bulk capacitor B+ pin (C1), and the transformer secondary pins (T1). The output rectifiers (D6 and D7) are placed close to the secondary pins. The main output capacitor (C10), is placed close to the main output connector. Jumpers are used to augment the PCB traces in the high-current secondary traces.

The primary bias diode (D12) and capacitor (C20), standby output diode (D16) and capacitor (C17), are placed close to the standby transformer (T2). C20 negative terminal is routed to the bulk capacitor B- pin instead of to the HiperTFS-2 SOURCE or GROUND pin. The 2nd standby output filter capacitor (C15) is placed close to the standby output connector (J2).

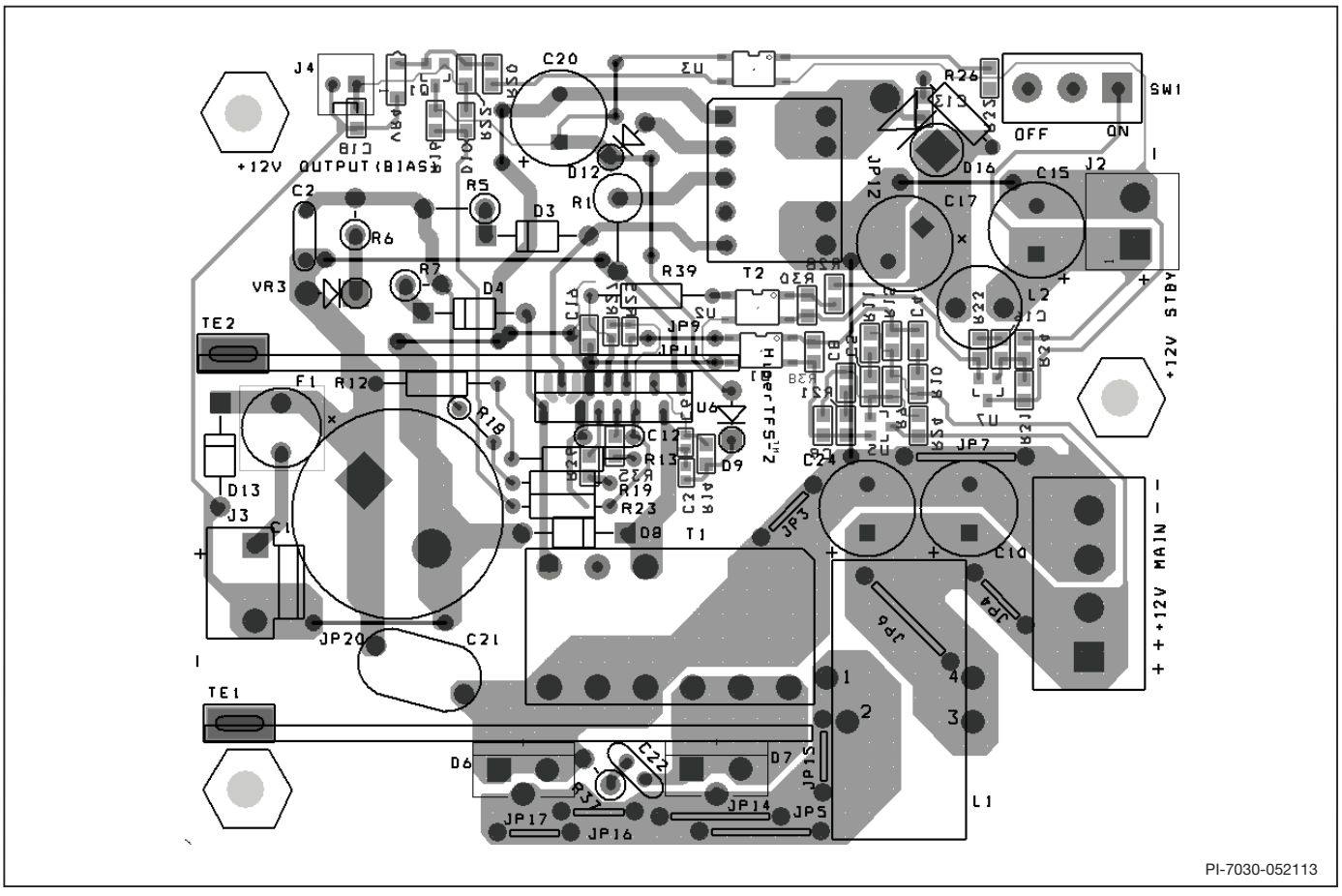


Figure 31. PCB Layout of Design Example Schematic in Figure 30.

Absolute Maximum Ratings[1,5]

DRAIN Voltage High-Side MOSFET ..... -0.3 V to 530 V
DRAIN Voltage Low-Side MOSFET ..... -0.3 V to 725 V
DRAIN Peak Current Low-Side
and High-Side: TFS7701 ..... 2.6 (5.0)[4] A
TFS7702 ..... 4.2 (8.0)[4] A
TFS7703 ..... 5.0 (9.3)[4] A
TFS7704 ..... 5.7 (10.7)[4] A
TFS7705 ..... 6.1 (11.4)[4] A
TFS7706 ..... 6.4 (12.1)[4] A
TFS7707 ..... 7.2 (13.4)[4] A
TFS7708 ..... 8.3 (15.5)[4] A
DRAIN Voltage Standby MOSFET ..... -0.3 V to 725 V
DRAIN Peak Current Standby MOSFET ..... 1.20 (2.25)[4] A
ENABLE (EN) Pin Voltage ..... -0.3 V to 9 V
ENABLE (EN) Pin Current ..... 100 mA
FEEDBACK (FB) Pin Voltage ..... -0.3 V to 9 V
FEEDBACK (FB) Current ..... 100 mA
LINE-SENSE (L) Pin Voltage ..... -0.3 V to 9 V
LINE-SENS (L) Pin Current ..... 100 mA
RESET (R) Pin Voltage ..... -0.3 V to 9 V
RESET (R) Pin Current ..... 100 mA
BYPASS Supply (BP) Pin Voltage ..... -0.3 V to 9 V
BYPASS Supply (BP) Pin Current ..... 100 mA
HIGHT-SIDE (VDDH) Supply Pin Voltage ..... -0.3 V to 13.4 V
HIGH-SIDE (VDDH) Supply Pin Current ..... 50 mA
Storage Temperature ..... -65 °C to 150 °C
Operating Junction Temperature[2] ..... -40 °C to 150 °C
Lead Temperature[3] ..... 260 °C

Notes:
1. All voltages referenced to SOURCE, T_J = 25 °C.
2. Normally limited by internal circuitry.
3. 1/16 in. (1.59 mm) from case for 5 seconds.
4. The higher peak DRAIN current is allowed while the DRAIN voltage is simultaneously less than 400 V.
5. Maximum ratings specified may be applied one at a time, without causing permanent damage to the product. Exposure to Absolute Rating conditions for extended periods of time may affect product reliability.

Thermal Resistance

High-Side MOSFET (θ_{JC}) TFS7701-7706 ..... 5 °C/W
TFS7707-7708 ..... 4 °C/W
Low-Side MOSFET (θ_{JC}) ..... 1 °C/W

Notes:
1. All voltages referenced to SOURCE, T_A = 25 °C.

Parameter	Symbol	Conditions SOURCE = 0 V; T_J = 0 °C to 100 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Control Functions							
Switching Frequency – PC Main	$f_{S1(MA)}$	T_J = 25 °C	Average	62	66	70	kHz
			Peak-to-Peak Jitter		4		
	$f_{S2(MA)}$	T_J = 25 °C	Average	124	132	140	
			Peak-to-Peak Jitter		8		
Frequency Jitter Modulation Rate	$f_{M1(MA)}$				250		Hz
	$f_{M2(MA)}$				250		
Remote-ON Main							
BYPASS Pin Remote-ON Current	$I_{BP(ON)}$	V_{EN} = Open		4.3	5.3	6.3	mA
BYPASS Pin Remote-OFF Current Hysteresis	$I_{BP(HYST)}$	66 kHz	TFS7701		3.8		mA
			TFS7702		3.7		
			TFS7703		3.6		
			TFS7704		3.6		
			TFS7705		3.5		
			TFS7706		3.4		
			TFS7707		3.4		
			TFS7708		3.4		
	$I_{BP(HYST)}$	132 kHz	TFS7701		3.6		
			TFS7702		3.5		
			TFS7703		3.3		
			TFS7704		3.2		
			TFS7705		3.1		
			TFS7706		2.9		
			TFS7707		2.8		
			TFS7708		2.7		

Parameter	Symbol	Conditions SOURCE = 0 V; T_J = 0 °C to 100 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Remote-ON Main (cont.)							
BYPASS Pin Latching Shutdown Threshold	$I_{BP(SD)}$				17		mA
Main/Standby Remote-ON Delay	$t_{R(ON)}$				2.5		µs
Main/Standby Remote-OFF Delay	$t_{R(OFF)}$				2.5		µs
Soft-Start							
High-Side Start-Up Charge Time	$t_{D(CH)}$				60		ms
Soft-Start Period	t_{SS}	See Note D			12		ms
FEEDBACK Pin							
PWM Gain	$DC_{REG(MA)}$	-1800 µA < I_{FB} < -1500 µA, I_L = 60 µA, I_R = 160 µA			-70		%/mA
PWM Gain Temperature Drift	TC_{DCREG}				0.05		%/°C
FEEDBACK Pin Feed-back Onset current	$I_{FB(ON)}$	I_L = 100 µA, I_R = 170 µA T_J = 25 °C			-1.2		mA
FEEDBACK Pin Current at Zero Duty Cycle	$I_{FB(OFF)}$				-2.1		mA
FEEDBACK Pin Internal Filter Pole	$f_{P(FB)}$				12		kHz
FEEDBACK Pin Voltage	V_{FB}	I_{FB} = $I_{FB(ON)}$			2.9		V
LINE-SENSE Pin (Line Voltage)							
Line Undervoltage Threshold – Standby	$I_{L(SB-UVON)}$	T_J = 25 °C	Threshold	23.75	25	26.25	µA
	$I_{L(SB-UVOFF)}$		Threshold	9.0	10.5	12	
Line Undervoltage Threshold – Main	$I_{L(MA-UVON)}$	T_J = 25 °C	Threshold	80	84	88	µA
	$I_{L(MA-UVOFF)}$		Threshold	47	54	58	
Line Overvoltage Threshold – Main and Standby	$I_{L(MA-OVON)}$	T_J = 25 °C	Threshold	119	130	146	µA
	$I_{L(MA-OVOFF)}$		Threshold	135	144	164	
LINE-SENSE Pin Voltage	V_L	T_J = 25 °C	I_L = 79 µA	0.75	1.27	1.55	V
			I_L = 149 µA	1.0	1.45	1.85	
LINE-SENSE Pin Short-Circuit	$I_{L(SC)}$	V_L = V_{BP}			3900		µA
RESET Pin (Duty Limit/Main Only Remote-OFF)							
Reset Overvoltage Threshold	$I_{R(MA-OVON)}$	T_J = 25 °C	Threshold	165	205	245	µA
	$I_{R(MA-OVOFF)}$		Threshold	175	215	255	
RESET Pin Voltage	V_R	I_R = 155 µA			1.55		V
RESET Pin Short-Circuit Current	$I_{R(SC)}$	V_R = V_{BP}			3750		µA
Duty Cycle – Programmable Limit	$DC_{LIMIT(MA)}$	I_L = 100 µA, I_R = 110 µA			50.5		%
		I_L = 115 µA, I_R = 170 µA			48.2		
	$DC_{MAX(MA)}$	I_L = 90 µA, I_R = 170 µA			61		

Parameter	Symbol	Conditions SOURCE = 0 V; T_J = 0 °C to 100 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Current Limit Programming							
FEEDBACK Pin Current Limit Detection Range #1	$I_{LIM(1)(MA)}$	Start-up See Note B			0-5		µA
FEEDBACK Pin Current Limit Detection Range #2	$I_{LIM(2)(MA)}$	Start-up See Note B			5-12		µA
FEEDBACK Pin Current Limit Detection Range #3	$I_{LIM(3)(MA)}$	Start-up See Note B			12-24		µA
Maximum Current Limit							
Current Limit	$I_{LIM(1)(MA)}$	TFS7701 T_J = 25 °C F_S = 66 kHz	di/dt = 175 mA/µs		1.19		A
	$I_{LIM(2)(MA)}$		di/dt = 224 mA/µs		1.53		
	$I_{LIM(3)(MA)}$		di/dt = 249 mA/µs	1.58	1.70	1.82	
	$I_{LIM(1)(MA)}$	TFS7702 T_J = 25 °C F_S = 66 kHz	di/dt = 267 mA/µs		1.82		
	$I_{LIM(2)(MA)}$		di/dt = 343 mA/µs		2.34		
	$I_{LIM(3)(MA)}$		di/dt = 381 mA/µs	2.40	2.60	2.78	
	$I_{LIM(1)(MA)}$	TFS7703 T_J = 25 °C F_S = 66 kHz	di/dt = 333 mA/µs		2.26		
	$I_{LIM(2)(MA)}$		di/dt = 428 mA/µs		2.91		
	$I_{LIM(3)(MA)}$		di/dt = 475 mA/µs	2.99	3.24	3.46	
	$I_{LIM(1)(MA)}$	TFS7704 T_J = 25 °C F_S = 66 kHz	di/dt = 370 mA/µs		2.52		
	$I_{LIM(2)(MA)}$		di/dt = 475 mA/µs		3.24		
	$I_{LIM(3)(MA)}$		di/dt = 528 mA/µs	3.33	3.60	3.85	
	$I_{LIM(1)(MA)}$	TFS7705 T_J = 25 °C F_S = 66 kHz	di/dt = 409 mA/µs		2.78		
	$I_{LIM(2)(MA)}$		di/dt = 525 mA/µs		3.58		
	$I_{LIM(3)(MA)}$		di/dt = 584 mA/µs	3.68	3.98	4.26	
	$I_{LIM(1)(MA)}$	TFS7706 T_J = 25 °C F_S = 66 kHz	di/dt = 448 mA/µs		3.05		
	$I_{LIM(2)(MA)}$		di/dt = 576 mA/µs		3.92		
	$I_{LIM(3)(MA)}$		di/dt = 639 mA/µs	4.03	4.36	4.66	
	$I_{LIM(1)(MA)}$	TFS7707 T_J = 25 °C F_S = 66 kHz	di/dt = 482 mA/µs		3.28		
	$I_{LIM(2)(MA)}$		di/dt = 619 mA/µs		4.22		
	$I_{LIM(3)(MA)}$		di/dt = 688 mA/µs	4.33	4.69	5.01	
	$I_{LIM(1)(MA)}$	TFS7708 T_J = 25 °C F_S = 66 kHz	di/dt = 509 mA/µs		3.47		
	$I_{LIM(2)(MA)}$		di/dt = 655 mA/µs		4.46		
	$I_{LIM(3)(MA)}$		di/dt = 727 mA/µs	4.58	4.96	5.30	
Low-Side Main MOSFET							
ON-State Resistance	$R_{DS(ON)}$	TFS7701 I_D = 10% $I_{LIM(3)(MA)}$	T_J = 25 °C		4.3	4.95	Ω
			T_J = 100 °C		6.5	7.48	
		TFS7702 I_D = 10% $I_{LIM(3)(MA)}$	T_J = 25 °C		2.7	3.10	
			T_J = 100 °C		4.1	4.70	
		TFS7703 I_D = 10% $I_{LIM(3)(MA)}$	T_J = 25 °C		2.0	2.30	
			T_J = 100 °C		3.0	3.45	
		TFS7704 I_D = 10% $I_{LIM(3)(MA)}$	T_J = 25 °C		1.55	1.78	
			T_J = 100 °C		2.35	2.70	

Parameter	Symbol	Conditions SOURCE = 0 V; T_J = 0 °C to 100 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Low-Side Main MOSFET (cont.)							
ON-State Resistance	$R_{DS(ON)}$	TFS7705 I_D = 10% $I_{LIM(3)(MA)}$	T_J = 25 °C		1.3	1.49	Ω
			T_J = 100 °C		1.95	2.24	
		TFS7706 I_D = 10% $I_{LIM(3)(MA)}$	T_J = 25 °C		1.1	1.26	
			T_J = 100 °C		1.65	1.90	
		TFS7707 I_D = 10% $I_{LIM(3)(MA)}$	T_J = 25 °C		1.0	1.15	
			T_J = 100 °C		1.45	1.67	
		TFS7708 I_D = 10% $I_{LIM(3)(MA)}$	T_J = 25 °C		0.9	1.03	
			T_J = 100 °C		1.3	1.50	
OFF-State Drain Leakage Current	$I_{DSS(D)}$	TFS7701	V_L, V_R = 0 V, I_{BP} = 6 mA, V_{DS} = 560 V, T_J = 100 °C			150	µA
		TFS7702				150	
		TFS7703				150	
		TFS7704				150	
		TFS7705				170	
		TFS7706				170	
		TFS7707				470	
		TFS7708				470	
Breakdown Voltage	$BV_{DSS(D)}$	V_L, V_R = 0 V, I_{BP} = 6 mA, T_J = 25 °C		725			V
Rise Time	$t_{R(D)}$				100		ns
Fall Time	$t_{F(D)}$				50		ns
High-Side Main MOSFET							
ON-State Resistance	$R_{DS(ON)(HD)}$	TFS7701 (V_{HD} - V_{HS}) = 1 V	T_J = 25 °C			1.90	Ω
			T_J = 100 °C		2.40		
		TFS7702 (V_{HD} - V_{HS}) = 1 V	T_J = 25 °C			1.90	
			T_J = 100 °C		2.40		
		TFS7703 (V_{HD} - V_{HS}) = 1 V	T_J = 25 °C			1.20	
			T_J = 100 °C		1.50		
		TFS7704 (V_{HD} - V_{HS}) = 1 V	T_J = 25 °C			1.20	
			T_J = 100 °C		1.50		
		TFS7705 (V_{HD} - V_{HS}) = 1 V	T_J = 25 °C			0.90	
			T_J = 100 °C		1.10		
		TFS7706 (V_{HD} - V_{HS}) = 1 V	T_J = 25 °C			0.90	
			T_J = 100 °C		1.10		
		TFS7707 (V_{HD} - V_{HS}) = 1 V	T_J = 25 °C			0.71	
			T_J = 100 °C		0.90		
		TFS7708 (V_{HD} - V_{HS}) = 1 V	T_J = 25 °C			0.71	
			T_J = 100 °C		0.90		
Effective Output Capacitance	$C_{OSS(EFF)(HD)}$	TFS7701	T_J = 25 °C, V_{GS} = 0 V V_{DS} = 0 V to 80% $V_{DSS(HD)}$		55		pF
		TFS7702			55		
		TFS7703			82		
		TFS7704			82		
		TFS7705			110		
		TFS7706			110		
		TFS7707			165		
		TFS7708			165		

Parameter	Symbol	Conditions SOURCE = 0 V; T_J = 0 °C to 100 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
High-Side Main MOSFET (cont.)							
Breakdown Voltage	$BV_{DSS(HD)}$	T_J = 25 °C		530			530
OFF-State Drain Current Leakage	$I_{DSS(HD)}$	TFS7701	V_D = 424 V, T_J = 100 °C			60	µA
		TFS7702				60	
		TFS7703				60	
		TFS7704				60	
		TFS7705				80	
		TFS7706				80	
		TFS7707				110	
		TFS7708				110	
Turn-On Voltage Rise Time	$t_{R(HD)}$				30		ns
Turn-Off Voltage Fall Time	$t_{F(HD)}$				25		ns
High-Side Bias Shunt Voltage	$V_{DDH(SHUNT)}$	I_{DDH} = 5 mA See Note A			12.2		V
High-Side Undervoltage ON-Threshold	$V_{DDH(UVON)}$	See Note A			11.5		V
High-Side Undervoltage OFF-Threshold	$V_{DDH(UVOFF)}$	See Note A			10.3		V
High-Side Shunt Hysteresis Voltage	$V_{DDH(HYST)}$	See Note A			1.1		V
Standby MOSFET							
ON-State Resistance	$R_{DS(ON)(DS)}$	I_{DSB} = 10% $I_{LIM(4)(DSB)}$	T_J = 25 °C		8.5	9.7	Ω
			T_J = 100 °C		12.8	14.6	
OFF-State Drain Leakage Current	$I_{DSS1(DS)}$	V_{BP} = 6.2 V V_{EN} = 0 V V_{DS} = 560 V T_J = 100 °C				200	µA
	$I_{DSS2(DS)}$	V_{BP} = 6.2 V V_{EN} = 0 V	V_{DS} = 375 V, T_J = 50 °C		15		
Breakdown Voltage	$BV_{DSS(DS)}$	V_{BP} = 6.2 V, V_{EN} = 0 V, T_J = 25 °C		725			V
DRAIN Supply Voltage	$V_{DSB(START)}$			50			V
Standby Controller							
Output Frequency in Standard Mode	$f_{S(SB)}$	T_J = 25 °C	Average	124	132	140	kHz
			Peak-to-Peak Jitter		8		
Maximum Duty Cycle	$DC_{MAX(DSB)}$	I_L = 40 µA		66	69	72	%
ENABLE Pin Upper Turnoff Threshold Current	I_{DIS}			-150	-105	-80	µA
ENABLE Pin Voltage	V_{EN}	I_{EN} = -25 µA		2.7	3.6	4.5	V

Parameter	Symbol	Conditions SOURCE = 0 V; T_J = 0 °C to 100 °C (Unless Otherwise Specified)	Min	Typ	Max	Units
Standby Controller (cont.)						
BYPASS Pin Charge Current	I_{CH1}	V_{BP} = 0 V, T_J = 25 °C	-5	-4.0	-2	mA
	I_{CH2}	V_{BP} = 4 V, T_J = 25 °C	-4	-2.1	0	
BYPASS Pin Voltage	V_{BP}	V_{DS} = 50 V	5.60	5.80	6.00	V
BYPASS Pin Voltage Hysteresis	$V_{BP(HYST)}$		0.80	1.1	1.3	V
BYPASS Pin Shunt Voltage	$V_{BP(SHUNT)}$	I_{BP} = 2 mA	5.8	6.15	6.4	V
Standby Circuit Protection						
ENABLE Pin Current Limit Selection Range #1	$I_{LIM(1)(DSB)}$	Start-up		0-5		µA
ENABLE Pin Current Limit Selection Range #2	$I_{LIM(2)(DSB)}$	Start-up		5-12		µA
ENABLE Pin Current Limit Selection Range #3	$I_{LIM(3)(DSB)}$	Start-up		12-24		µA
ENABLE Pin Current Limit Selection Range #4	$I_{LIM(4)(DSB)}$	Start-up		24-48		µA
Standby Current Limit	$I_{LIM(1)(DSB)}$	I_L = 20 µA, di/dt = 95 mA/µs, T_J = 25 °C	450	500	540	mA
	$I_{LIM(2)(DSB)}$	I_L = 20 µA, di/dt = 105 mA/µs, T_J = 25 °C	500	550	600	
	$I_{LIM(3)(DSB)}$	I_L = 20 µA, di/dt = 123 mA/µs, T_J = 25 °C	610	650	690	
	$I_{LIM(4)(DSB)}$	I_L = 20 µA, di/dt = 143 mA/µs, T_J = 25 °C	690	750	810	
	ΔI_{LIM}	I_{LIM} (I_L = 100 µA) / I_{LIM} (I_L = 20 µA) di/dt = 125 mA/µs		84		%
General Circuit Protection						
Power Coefficient	I^2f	$I^2f = I_{LIM(3)(DSB)(TYP)} \times f_{S(SB)(OSC)(TYP)}$ T_J = 25 °C	0.9 × I^2f	I^2f	1.12 × I^2f	A^2Hz
Initial Current Limit	I_{INIT}	T_J = 25 °C See Note D	0.75 × $I_{LIM(MIN)}$			
Leading Edge Blanking Time (Main)	$t_{LEB(D)}$	T_J = 25 °C		150		ns
Leading Edge Blanking Time (Standby)	$t_{LEB(DSB)}$	T_J = 25 °C See Note D	170	215		ns
Current Limit Delay (Main)	$t_{ILD(D)}$	T_J = 25 °C		150		ns

Parameter	Symbol	Conditions SOURCE = 0 V; T_J = 0 °C to 100 °C (Unless Otherwise Specified)	Min	Typ	Max	Units
General Circuit Protection (cont.)						
Current Limit Delay (Standby)	$t_{ILD(DSB)}$	T_J = 25 °C		150		ns
Thermal Shutdown Temperature	T_{SD}	See Note D		118		°C
Thermal Shutdown Hysteresis	$T_{SD(HYST)}$			55		°C
Auto-Restart ON-Time at f_{osc} Standby	t_{AR}	T_J = 25 °C		64		ms
Auto-Restart Duty Cycle Standby	DC_{AR}	T_J = 25 °C		2.2		%
Supply Current						
DRAIN Supply Current	I_{S1}	EN Current > I_{DIS} (No MOSFETs Switching)	200	550	800	µA
	I_{S2}	EN Open (Standby MOSFET Switching at f_{OSC})	360	710	960	

NOTES:
A. $V_{DDH(SHUNT)}$ minus $V_{DDH(UV\_ON)}$ is equal to 250 mV minimum.
B. Level 1 R_{FB} = open, Level 2 R_{FB} = 511 kΩ, Level 3 R_{FB} = 232 kΩ.
C. Level 1 R_{EN} = open, Level 2 R_{EN} = 511 kΩ, Level 3 R_{EN} = 232 kΩ, Level 4 R_{EN} = 107 kΩ.
D. Guaranteed by characterization. Not tested in production.

Typical Performance Characteristics

Note: Curves shown with $f_{S1(MA)}$ = 66 kHz and $f_{S(SB)}$ = 132 kHz.

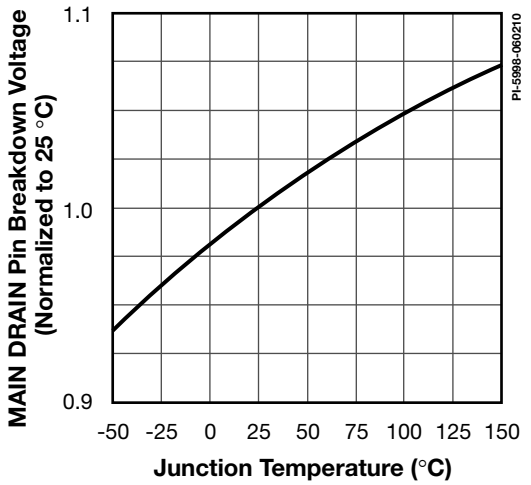


Figure 32. Main Supply. Breakdown Voltage vs. Temperature.

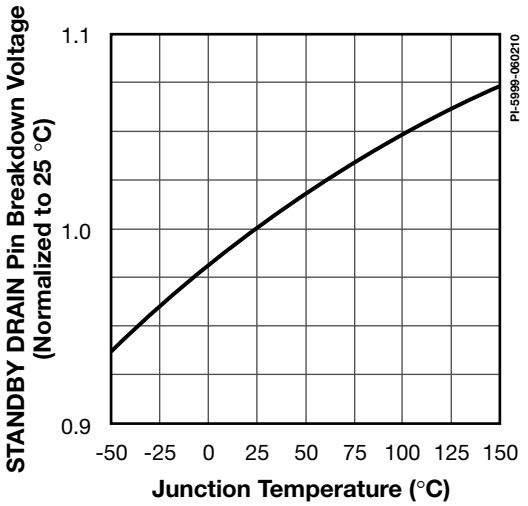


Figure 33. Standby Supply. Breakdown vs. Temperature.

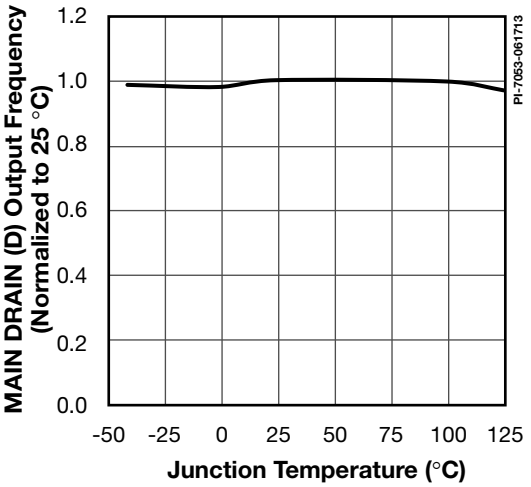


Figure 34. Main Switching Frequency vs. Temperature.

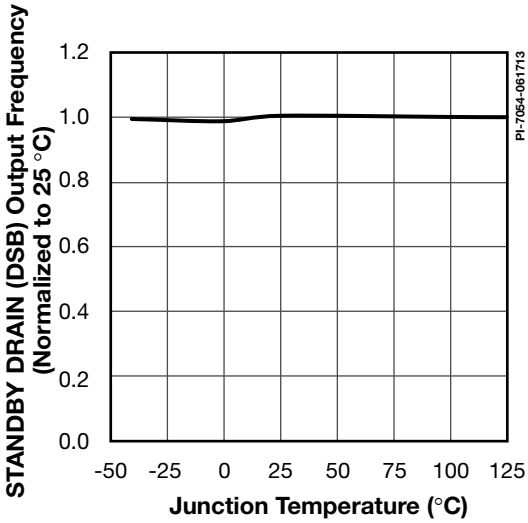


Figure 35. Standby Switching Frequency vs. Temperature.

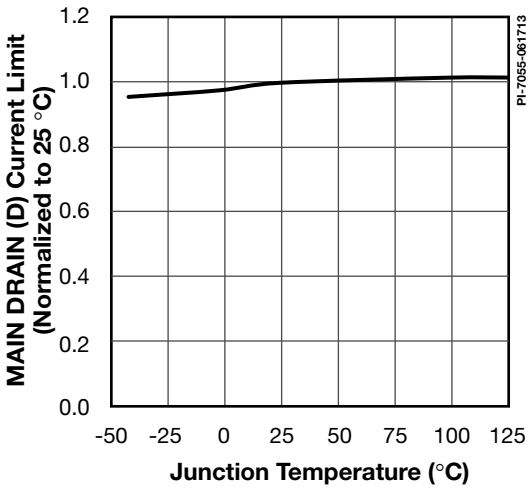


Figure 36. Main Drain (D) Current Limit vs. Temperature.

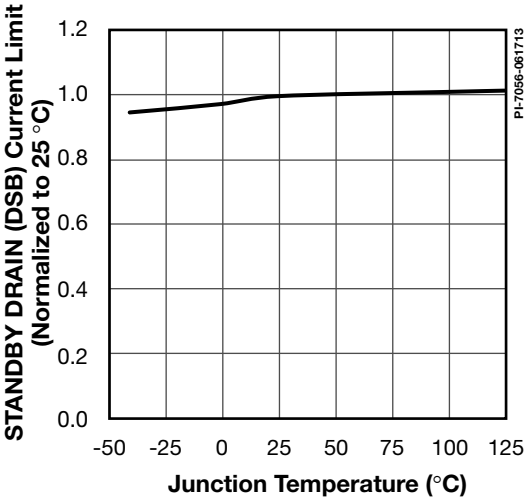


Figure 37. Standby Drain (DSB) Current Limit vs. Temperature.

Typical Performance Characteristics (cont.)

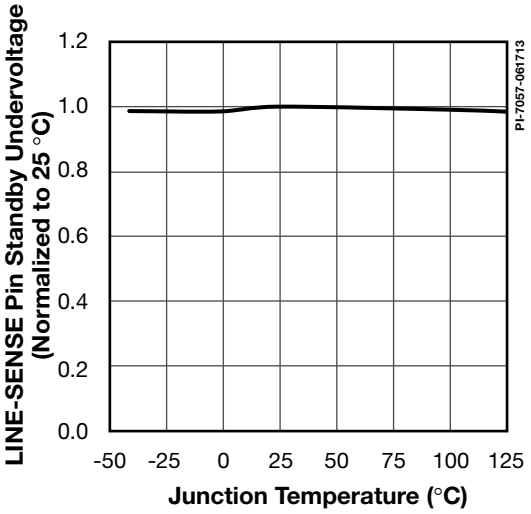


Figure 38. Standby Supply. Undervoltage Threshold vs. Junction Temperature.

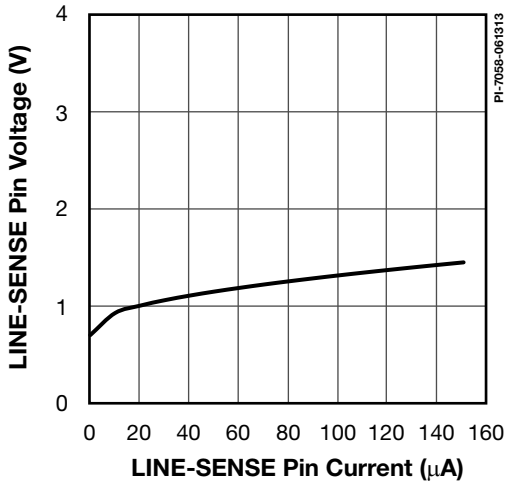


Figure 39. LINE-SENSE (L) Pin Voltage vs. Current.

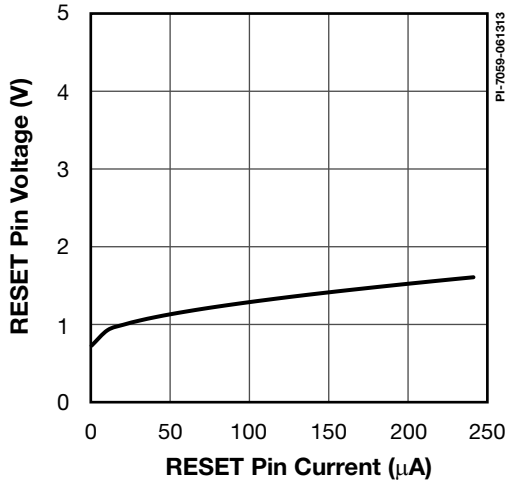


Figure 40. RESET (R) Pin Voltage vs. Current.

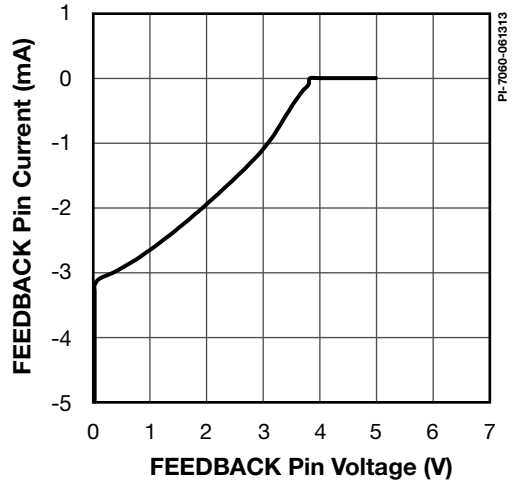


Figure 41. FEEDBACK (FB) Pin Current vs. Voltage.

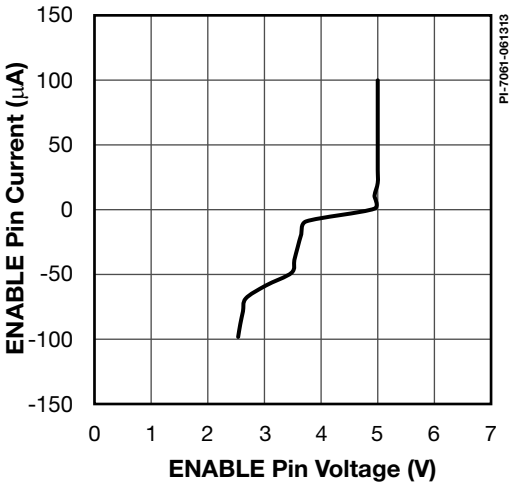


Figure 42. ENABLE (EN) Pin Current vs. Voltage.

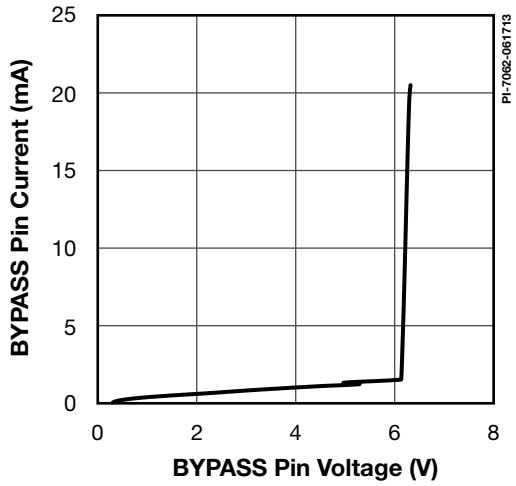


Figure 43. BYPASS (BP) Pin Current vs. Voltage.

Typical Performance Characteristics (cont.)

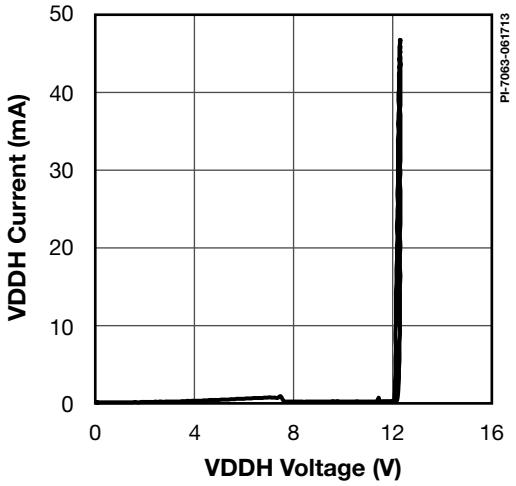


Figure 44. VDDH Pin Current vs. Voltage.

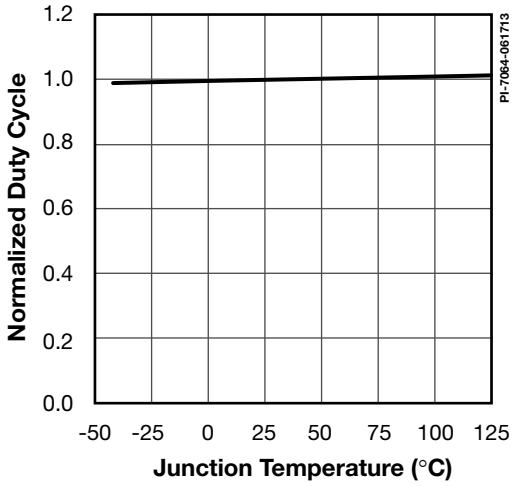


Figure 45. Duty Cycle vs. Temperature (I_L = 100 µA, I_R = 110 µA).

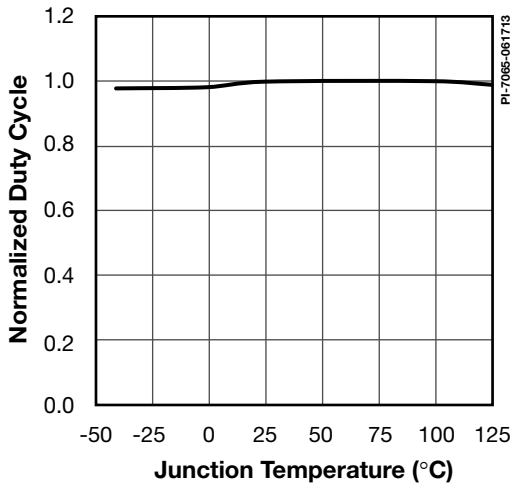


Figure 46. Duty Cycle vs. Temperature (I_L = 115 µA, I_R = 170 µA)

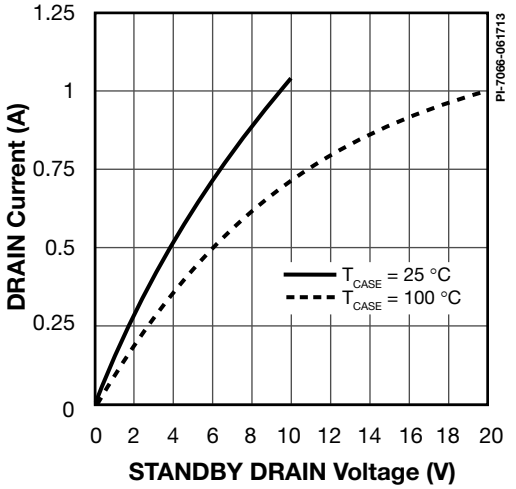


Figure 47. Standby Supply. Output Characteristics.

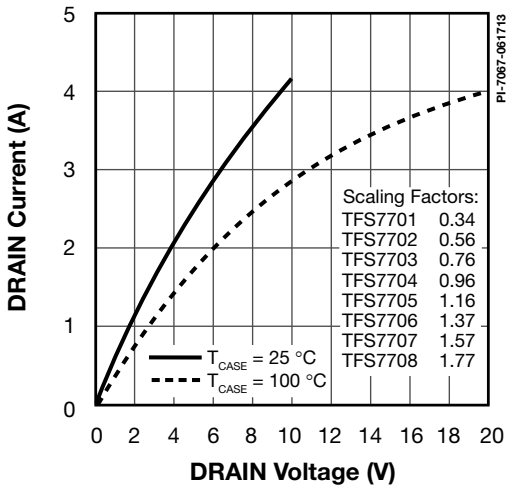


Figure 48. Drain Supply. Output Characteristics.

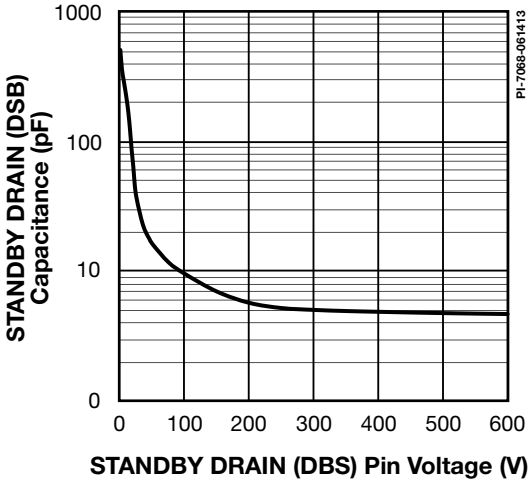


Figure 49. Standby Drain Capacitance vs. Drain Voltage.

Typical Performance Characteristics (cont.)

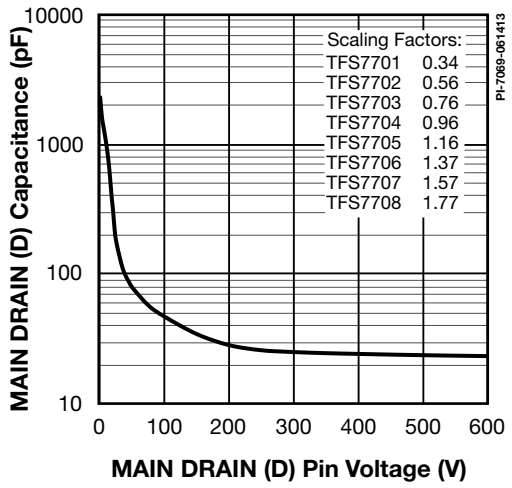


Figure 50. Main Drain Capacitance vs. Drain Voltage.

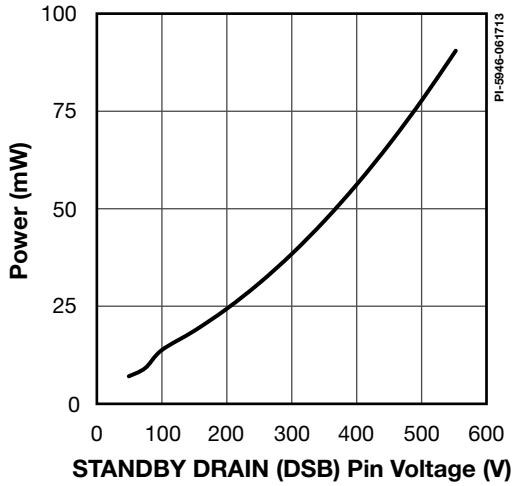


Figure 51. Standby Drain Switching Power vs. Drain Voltage.

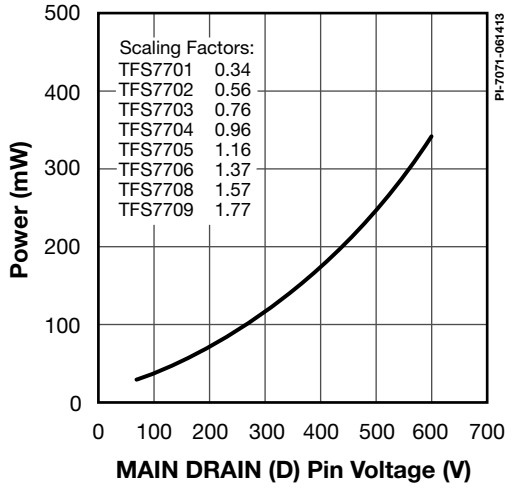


Figure 52. Main Drain Switching Power vs. Drain Voltage.

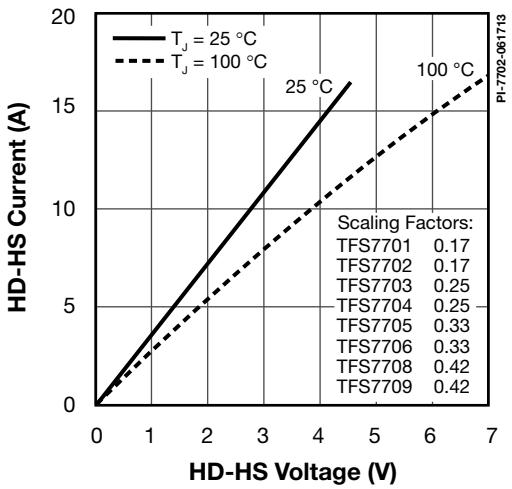


Figure 53. High-Side MOSFET (HD-HS) Drain Current vs. Drain Voltage.

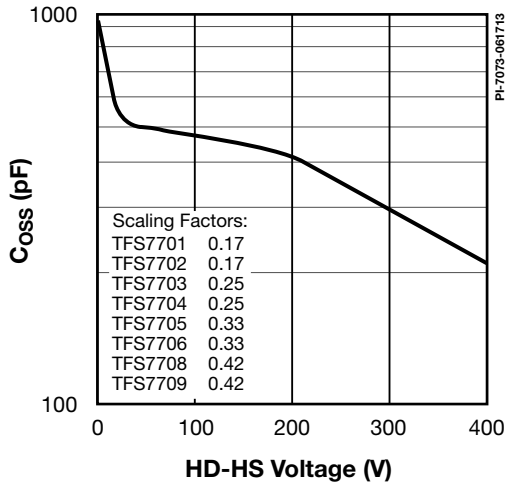


Figure 54. High-Side MOSFET (HD-HS) Drain Current vs. Drain Voltage.

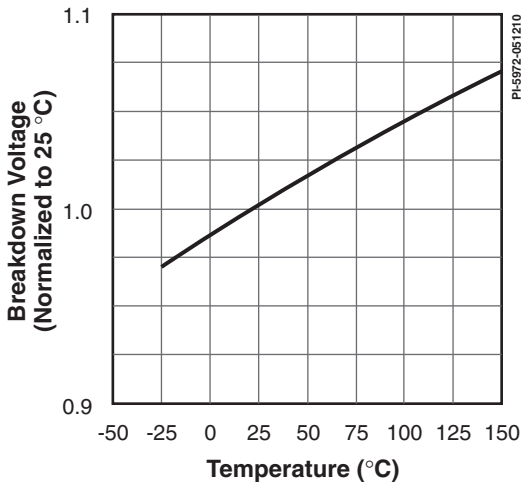


Figure 55. High-Side MOSFET Breakdown Voltage vs. Temperature.

Typical Performance Characteristics (cont.)

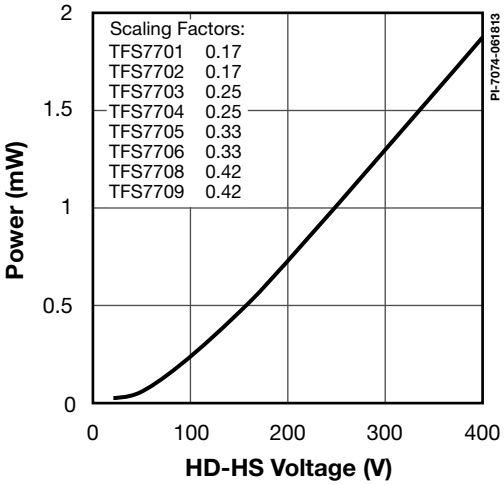


Figure 56. High-Side MOSFET (HD-HS) Power vs. Drain Voltage.

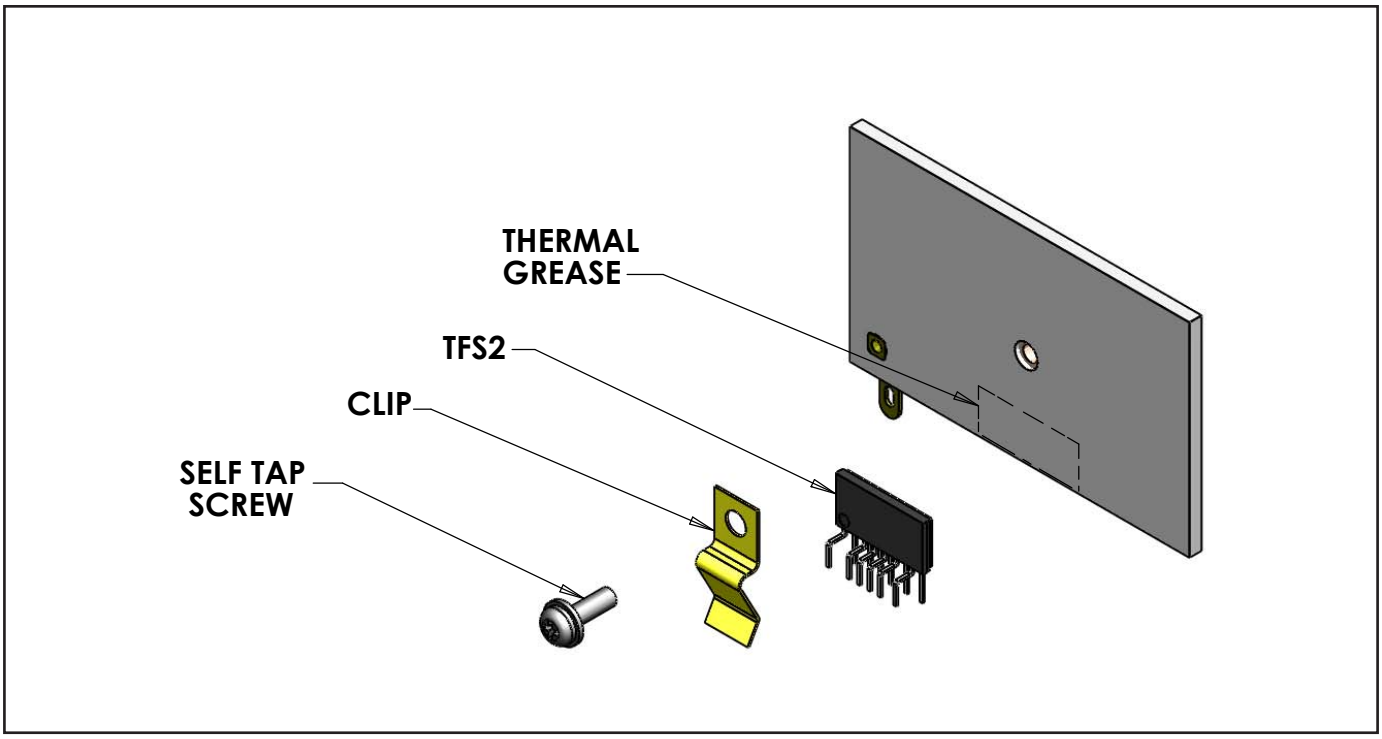
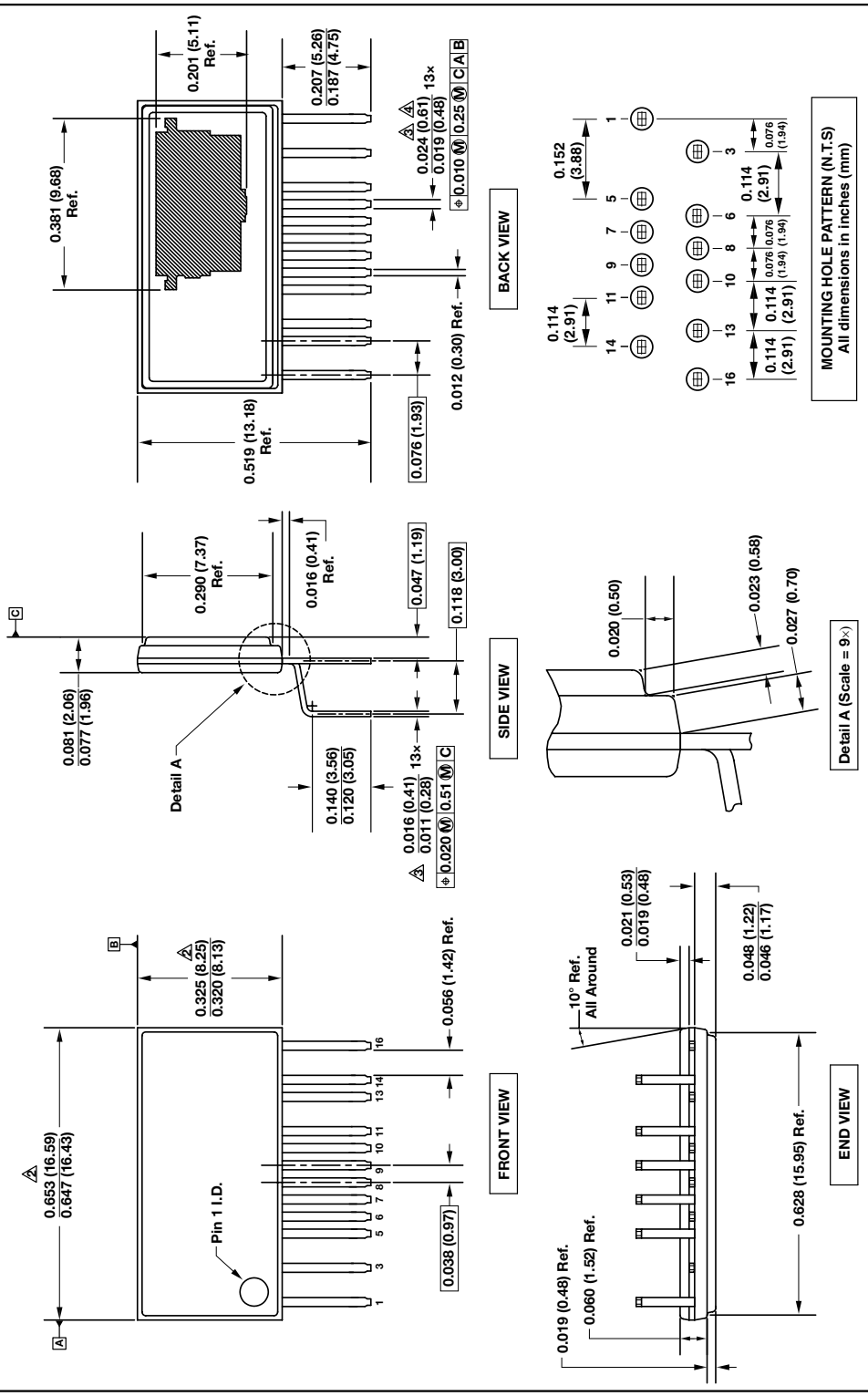


Figure 57. Heat Sink Assembly – using Thermally Conductive Silicone Grease.

eSIP-16F (H Package)



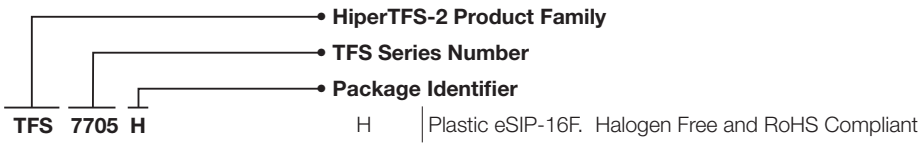
Notes:
1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions noted are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs, and interlead flash, but including any mismatch between the top and bottom of the plastic body. Maximum mold protrusion is 0.007 [0.18] per side.
3. Dimensions noted are inclusive of plating thickness.
4. Does not include interlead flash or protrusions.
5. Controlling dimensions in inches (mm).
6. 7. Tied to SOURCE (Pin 6).
8. Tied to HS (Pin 14).
9. 10. Tied to HD (Pin 16).

PI-7080-070813

Part Ordering Information

Part Number	Option	Quantity
TFS7701H	Tube	30
TFS7702H	Tube	30
TFS7703H	Tube	30
TFS7704H	Tube	30
TFS7705H	Tube	30
TFS7706H	Tube	30
TFS7707H	Tube	30
TFS7708H	Tube	30

Part Marking Information



Revision	Notes	Date
A	Code A.	11/13
B	Moved location of “output short-circuit protection (SCP)” bullet point on page 3.	04/15

For the latest updates, visit our website: www.power.com

Power Integrations reserves the right to make changes to its products at any time to improve reliability or manufacturability. Power Integrations does not assume any liability arising from the use of any device or circuit described herein. POWER INTEGRATIONS MAKES NO WARRANTY HEREIN AND SPECIFICALLY DISCLAIMS ALL WARRANTIES INCLUDING, WITHOUT LIMITATION, THE IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF THIRD PARTY RIGHTS.

Patent Information

The products and applications illustrated herein (including transformer construction and circuits external to the products) may be covered by one or more U.S. and foreign patents, or potentially by pending U.S. and foreign patent applications assigned to Power Integrations. A complete list of Power Integrations patents may be found at www.power.com. Power Integrations grants its customers a license under certain patent rights as set forth at http://www.power.com/ip.htm.

Life Support Policy

POWER INTEGRATIONS PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF POWER INTEGRATIONS. As used herein:

1. A Life support device or system is one which, (i) is intended for surgical implant into the body, or (ii) supports or sustains life, and (iii) whose failure to perform, when properly used in accordance with instructions for use, can be reasonably expected to result in significant injury or death to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

Power Integrations Worldwide Sales Support Locations

World Headquarters
5245 Hellyer Avenue
San Jose, CA 95138, USA.
Main: +1-408-414-9200
Customer Service:
Phone: +1-408-414-9665
Fax: +1-408-414-9765
e-mail: usasales@power.com

China (Shanghai)
Rm 1601/1610, Tower 1,
Kerry Everbright City
No. 218 Tianmu Road West,
Shanghai, P.R.C. 200070
Phone: +86-21-6354-6323
Fax: +86-21-6354-6325
e-mail: chinasales@power.com

China (Shenzhen)
17/F, Hivac Building, No. 2,
Keji Nan 8th Road, Nanshan
District, Shenzhen, China,
518057
Phone: +86-755-8672-8689
Fax: +86-755-8672-8690
e-mail: chinasales@power.com

Germany
Lindwurmstrasse 114
80337 Munich
Germany
Phone: +49-895-527-39110
Fax: +49-895-527-39200
e-mail: eurosales@power.com

India
#1, 14th Main Road
Vasanthanagar
Bangalore-560052 India
Phone: +91-80-4113-8020
Fax: +91-80-4113-8023
e-mail: indiasales@power.com

Italy
Via Milanese 20, 3rd. Fl.
20099 Sesto San Giovanni (MI)
Italy
Phone: +39-024-550-8701
Fax: +39-028-928-6009
e-mail: eurosales@power.com

Japan
Kosei Dai-3 Bldg.
2-12-11, Shin-Yokohama,
Kohoku-ku
Yokohama-shi Kanagwan
222-0033 Japan
Phone: +81-45-471-1021
Fax: +81-45-471-3717
e-mail: japansales@power.com

Korea
RM 602, 6FL
Korea City Air Terminal B/D, 159-6
Samsung-Dong, Kangnam-Gu,
Seoul, 135-728, Korea
Phone: +82-2-2016-6610
Fax: +82-2-2016-6630
e-mail: koreasales@power.com

Singapore
51 Newton Road
#19-01/05 Goldhill Plaza
Singapore, 308900
Phone: +65-6358-2160
Fax: +65-6358-2015
e-mail: singaporesales@power.com

Taiwan
5F, No. 318, Nei Hu Rd., Sec. 1
Nei Hu Dist.
Taipei 11493, Taiwan R.O.C.
Phone: +886-2-2659-4570
Fax: +886-2-2659-4550
e-mail: taiwansales@power.com

UK
First Floor, Unit 15, Meadway
Court, Rutherford Close,
Stevenage, Herts. SG1 2EF
United Kingdom
Phone: +44 (0) 1252-730-141
Fax: +44 (0) 1252-727-689
e-mail: eurosales@power.com

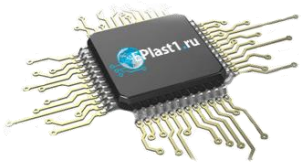
Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов;
- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits,General Dynamics и др.);

Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

Телефон: 8 (812) 309 58 32 (многоканальный)
Факс: 8 (812) 320-02-42
Электронная почта: org@eplast1.ru
Адрес: 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.