10 MHz to 10 GHz 67 dB TruPwr Detector

Data Sheet

ADL5906

FEATURES

- Accurate rms-to-dc conversion from 10 MHz to 10 GHz
- Single-ended ±1.0 dB dynamic range: 67 dB at 2.14 GHz
  - No balun or external input matching required
- Response independent of waveform types, such as
  - GSM-EDGE/CDMA/W-CDMA/TD-SCDMA/WiMAX/LTE
- Logarithmic slope: 55 mV/dB
- Temperature stability: <±1 dB from −40°C to +125°C
- Operating temperature: −55°C to +125°C
- Supply voltage: 4.75 V to 5.25 V
- Sleep current: 250 µA
- Pin compatible with ADL5902 and AD8363

APPLICATIONS

- Power amplifier linearization/control loops
- Transmitter signal strength indication (TSSI)
- RF instrumentation

FUNCTIONAL BLOCK DIAGRAM

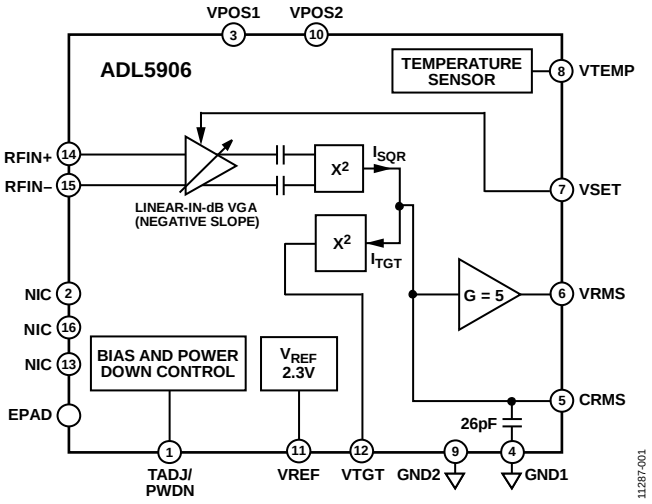

Figure 1.

GENERAL DESCRIPTION

The ADL5906 is a true rms responding power detector that has a 67 dB measurement range when driven with a single-ended 50 Ω source. The easy to use input makes the ADL5906 frequency versatile by eliminating the need for a balun or any other form of external input tuning for operation up to 10 GHz.

The ADL5906 provides a solution in a variety of high frequency systems requiring an accurate rms measurement of signal power. The ADL5906 can operate from 10 MHz to 10 GHz and can accept inputs from −65 dBm to +8 dBm with varying crest factors and bandwidths, such as GSM-EDGE, CDMA, W-CDMA, TD-SCDMA, WiMAX, and OFDM-based LTE carriers. In addition, its temperature stability over the broad temperature range of −55°C to +125°C makes it ideally suited for a wide array of communications, military, industrial, and instrumentation applications.

Used as a power measurement device, VRMS is connected to VSET. The output is then proportional to the logarithm of the rms value of the input. In other words, the reading is presented directly in decibels and is scaled 1.1 V per decade, or 55 mV/dB; other slopes are easily arranged. In controller mode, the voltage applied to VSET determines the power level required at the input to null the deviation from the setpoint. The output buffer can provide high load currents.

Requiring only a single supply of 5 V and a few capacitors, it is easy to use and capable of being driven single-ended or with a balun for differential input drive. The ADL5906 has a low 250 µA sleep current when powered down by a logic high applied to the PWDN pin. It powers up within approximately 1.4 µs to its nominal operating current of 68 mA at 25°C.

The ADL5906 is supplied in a 4 mm × 4 mm, 16-lead LFCSP, and it is pin compatible with the ADL5902 and the AD8363 TruPwr™ rms detectors. This feature allows the designer to create one circuit layout for projects requiring different dynamic ranges. A fully populated RoHS-compliant evaluation board is available.

Rev. A
Document Feedback

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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
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Technical Support
www.analog.com

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REVISION HISTORY

10/13—Rev. 0 to Rev. A

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3/13—Revision 0: Initial Version

SPECIFICATIONS

VPOS1 = VPOS2 = 5 V, T_A = 25°C, single-ended input drive, R_T = 60.4 Ω, VRMS connected to VSET, V_{TGT} = 0.8 V, C_{RMS} = 0.1 µF. Negative current values imply that the ADL5906 is sourcing current out of the indicated pin.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
OVERALL FUNCTION					
Frequency Range			10 to 10,000		MHz
RF INPUT INTERFACE	RFIN+, Pin RFIN– (Pin 14, Pin 15), ac-coupled				
Input Impedance	Single-ended drive, 50 MHz		2500		Ω
Common-Mode Voltage			2.5		V
100 MHz					
±1.0 dB Dynamic Range	Continuous wave (CW) input, T_A = 25°C		62		dB
Maximum Input Level, ±1.0 dB	Calibration at −55 dBm, −40 dBm, and 0 dBm		2		dBm
Minimum Input Level, ±1.0 dB	Calibration at −55 dBm, −40 dBm, and 0 dBm		−60		dBm
Deviation vs. Temperature	Deviation from output at 25°C, V_{TADJ} = 0.35 V				
	−40°C < T_A < +85°C; P_{IN} = 0 dBm		−0.8/+0.2		dB
	−40°C < T_A < +85°C; P_{IN} = −45 dBm		−0.8/+0.4		dB
	−55°C < T_A < +125°C; P_{IN} = 0 dBm		−1.3/+0.2		dB
	−55°C < T_A < +125°C; P_{IN} = −45 dBm		−1.2/+0.6		dB
Logarithmic Slope	−65 dBm < P_{IN} < +10 dBm; calibration at −40 dBm and 0 dBm		59		mV/dB
Logarithmic Intercept	−65 dBm < P_{IN} < +10 dBm; calibration at −40 dBm and 0 dBm		−64		dBm
700 MHz					
±1.0 dB Dynamic Range	CW input, T_A = 25°C		62		dB
Maximum Input Level, ±1.0 dB	Calibration at −55 dBm, −40 dBm, and 0 dBm		2		dBm
Minimum Input Level, ±1.0 dB	Calibration at −55 dBm, −40 dBm, and 0 dBm		−60		dBm
Deviation vs. Temperature	Deviation from output at 25°C, V_{TADJ} = 0.35 V				
	−40°C < T_A < +85°C; P_{IN} = 0 dBm		−0.9/+0.3		dB
	−40°C < T_A < +85°C; P_{IN} = −45 dBm		−0.9/+0.4		dB
	−55°C < T_A < +125°C; P_{IN} = 0 dBm		−1.5/+0.3		dB
	−55°C < T_A < +125°C; P_{IN} = −45 dBm		−1.3/+0.7		dB
Logarithmic Slope	−65 dBm < P_{IN} < +10 dBm; calibration at −40 dBm, and 0 dBm		59		mV/dB
Logarithmic Intercept	−65 dBm < P_{IN} < +10 dBm; calibration at −40 dBm and 0 dBm		−65		dBm
900 MHz					
±1.0 dB Dynamic Range	CW input, T_A = 25°C		63		dB
Maximum Input Level, ±1.0 dB	Calibration at −55 dBm, −40 dBm, and 0 dBm		3		dBm
Minimum Input Level, ±1.0 dB	Calibration at −55 dBm, −40 dBm, and 0 dBm		−60		dBm
Deviation vs. Temperature	Deviation from output at 25°C, V_{TADJ} = 0.35 V				
	−40°C < T_A < +85°C; P_{IN} = 0 dBm		−0.8/+0.3		dB
	−40°C < T_A < +85°C; P_{IN} = −45 dBm		−0.9/+0.4		dB
	−55°C < T_A < +125°C; P_{IN} = 0 dBm		−1.4/+0.3		dB
	−55°C < T_A < +125°C; P_{IN} = −45 dBm		−1.4/+0.8		dB
Logarithmic Slope	−65 dBm < P_{IN} < +10 dBm; calibration at −40 dBm and 0 dBm		59		mV/dB
Logarithmic Intercept	−65 dBm < P_{IN} < +10 dBm; calibration at −40 dBm and 0 dBm		−65		dBm
Deviation from CW Response (−45 dBm to −5 dBm)	12.16 dB peak-to-rms ratio (four-carrier W-CDMA)		−0.1		dB
	11.58 dB peak-to-rms ratio (LTE TM1, one-carrier, 20 MHz bandwidth)		−0.2		dB
	10.56 dB peak-to-rms ratio (W-CDMA)		0.05		dB
	7.4 dB peak-to-rms ratio (64 QAM)		−0.1		dB

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
1900 MHz					
±1.0 dB Dynamic Range	CW input, T_A = 25°C		66		dB
Maximum Input Level, ±1.0 dB	Calibration at −55 dBm, −40 dBm, and 0 dBm		6		dBm
Minimum Input Level, ±1.0 dB	Calibration at −55 dBm, −40 dBm, and 0 dBm		−60		dBm
Deviation vs. Temperature	Deviation from output at 25°C, V_{TADJ} = 0.35 V				
	−40°C < T_A < +85°C; P_{IN} = 0 dBm		−0.8/+0.2		dB
	−40°C < T_A < +85°C; P_{IN} = −45 dBm		−0.8/+0.5		dB
	−55°C < T_A < +125°C; P_{IN} = 0 dBm		−1.4/+0.2		dB
	−55°C < T_A < +125°C; P_{IN} = −45 dBm		−1.2/+0.9		dB
Logarithmic Slope	−65 dBm < P_{IN} < +10 dBm; calibration at −40 dBm and 0 dBm		57		mV/dB
Logarithmic Intercept	−65 dBm < P_{IN} < +10 dBm; calibration at −40 dBm and 0 dBm		−65		dBm
2140 MHz					
±1.0 dB Dynamic Range	CW input, T_A = 25°C		67		dB
Maximum Input Level, ±1.0 dB	Calibration at −55 dBm, −40 dBm, and 0 dBm		7		dBm
Minimum Input Level, ±1.0 dB	Calibration at −55 dBm, −40 dBm, and 0 dBm		−60		dBm
Deviation vs. Temperature	Deviation from output at 25°C, V_{TADJ} = 0.35 V				
	−40°C < T_A < +85°C; P_{IN} = 0 dBm		−0.8/+0.3		dB
	−40°C < T_A < +85°C; P_{IN} = −45 dBm		−0.8/+0.6		dB
	−55°C < T_A < +125°C; P_{IN} = 0 dBm		−1.3/+0.3		dB
	−55°C < T_A < +125°C; P_{IN} = −45 dBm		−1.2/+0.9		dB
Logarithmic Slope	−65 dBm < P_{IN} < +10 dBm; calibration at −40 dBm and 0 dBm		56		mV/dB
Logarithmic Intercept	−65 dBm < P_{IN} < +10 dBm; calibration at −40 dBm and 0 dBm		−65		dBm
Deviation from CW Response (−45 dBm to −5 dBm)	12.16 dB peak-to-rms ratio (four-carrier W-CDMA)		−0.1		dB
	11.58 dB peak-to-rms ratio (LTE TM1, one-carrier, 20 MHz bandwidth)		0.1		dB
	10.56 dB peak-to-rms ratio (one-carrier W-CDMA)		0.1		dB
	7.4 dB peak-to-rms ratio (64 QAM)		−0.1		dB
2600 MHz					
±1.0 dB Dynamic Range	CW input, T_A = 25°C		68		dB
Maximum Input Level, ±1.0 dB	Calibration at −55 dBm, −40 dBm, and 0 dBm		8		dBm
Minimum Input Level, ±1.0 dB	Calibration at −55 dBm, −40 dBm, and 0 dBm		−60		dBm
Deviation vs. Temperature	Deviation from output at 25°C, V_{TADJ} = 0.4 V				
	−40°C < T_A < +85°C; P_{IN} = 0 dBm		−0.9/+0.3		dB
	−40°C < T_A < +85°C; P_{IN} = −45 dBm		−1/+0.5		dB
	−55°C < T_A < +125°C; P_{IN} = 0 dBm		−1.4/+0.3		dB
	−55°C < T_A < +125°C; P_{IN} = −45 dBm		−1.4/+0.8		dB
Logarithmic Slope	−65 dBm < P_{IN} < +10 dBm; calibration at −40 dBm and 0 dBm		55		mV/dB
Logarithmic Intercept	−65 dBm < P_{IN} < +10 dBm; calibration at −40 dBm and 0 dBm		−65		dBm
3500 MHz					
±1.0 dB Dynamic Range	CW input, T_A = 25°C		65		dB
Maximum Input Level, ±1.0 dB	Calibration at −55 dBm, −40 dBm, and 0 dBm		5		dBm
Minimum Input Level, ±1.0 dB	Calibration at −55 dBm, −40 dBm, and 0 dBm		−60		dBm
Deviation vs. Temperature	Deviation from output at 25°C, V_{TADJ} = 0.45 V				
	−40°C < T_A < +85°C; P_{IN} = 0 dBm		−1.5/0		dB
	−40°C < T_A < +85°C; P_{IN} = −45 dBm		−1/+0.3		dB
	−55°C < T_A < +125°C; P_{IN} = 0 dBm		−1.5/0		dB
	−55°C < T_A < +125°C; P_{IN} = −45 dBm		−1.4/+0.4		dB
Logarithmic Slope	−65 dBm < P_{IN} < +10 dBm; calibration at −40 dBm and 0 dBm		52		mV/dB
Logarithmic Intercept	−65 dBm < P_{IN} < +10 dBm; calibration at −40 dBm and 0 dBm		−64		dBm

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
5800 MHz					
±1.0 dB Dynamic Range	CW input, T_A = 25°C		57		dB
Maximum Input Level, ±1.0 dB	Calibration at −50 dBm, −40 dBm, and 0 dBm		3		dBm
Minimum Input Level, ±1.0 dB	Calibration at −50 dBm, −40 dBm, and 0 dBm		−54		dBm
Deviation vs. Temperature	Deviation from output at 25°C, V_{TADJ} = 1 V				
	−40°C < T_A < +85°C; P_{IN} = 0 dBm		−2.4/+0		dB
	−40°C < T_A < +85°C; P_{IN} = −45 dBm		−1.4/-0.2		dB
	−55°C < T_A < +125°C; P_{IN} = 0 dBm		−3.6/+0		dB
	−55°C < T_A < +125°C; P_{IN} = −45 dBm		−2.1/-0.2		dB
Logarithmic Slope	−65 dBm < P_{IN} < +10 dBm; calibration at −40 dBm and 0 dBm		42		mV/dB
Logarithmic Intercept	−65 dBm < P_{IN} < +10 dBm; calibration at −40 dBm and 0 dBm		−60		dBm
OUTPUT INTERFACE	VRMS (Pin 6)				
Output Swing, Controller Mode	Swing range minimum, R_L ≥ 500 Ω to ground		0.05		V
	Swing range maximum, R_L ≥ 500 Ω to ground		3.92		V
Current Source/Sink Capability				10/10	mA
Rise Time	P_{IN} = off to −10 dBm, 10% to 90%, C_{RMS} = 1 nF		0.1		µs
Fall Time	P_{IN} = −10 dBm to off, 90% to 10%, C_{RMS} = 1 nF		14.6		µs
SETPOINT INPUT	VSET (Pin 7)				
Voltage Range	Log conformance error ≤ 1 dB, minimum 2.14 GHz		3.92		V
	Log conformance error ≤ 1 dB, maximum 2.14 GHz		0.4		V
Input Resistance			72		kΩ
Logarithmic Scale Factor	f = 2.14 GHz		56		mV/dB
Logarithmic Intercept	f = 2.14 GHz		−65		dBm
TEMPERATURE COMPENSATION	TADJ/PWDN (Pin 1)				
Input Voltage Range		0		V_{POS}	V
Input Bias Current	V_{TADJ} = 0.35 V		5		µA
Input Resistance	V_{TADJ} = 0.35 V		70		kΩ
VOLTAGE REFERENCE	VREF (Pin 11)				
Output Voltage	P_{IN} = −55 dBm		2.3		V
Temperature Sensitivity	25°C ≤ T_A ≤ 125°C		−0.12		mV/°C
	−55°C ≤ T_A ≤ +25°C		0.07		mV/°C
Short-Circuit Current Source/ Sink Capability	25°C ≤ T_A ≤ 125°C		4/0.05		mA
	−55°C ≤ T_A ≤ +25°C		3/0.05		mA
Voltage Regulation	T_A = 25°C, I_{LOAD} = 2 mA		−0.4		%
TEMPERATURE REFERENCE	VTEMP (Pin 8)				
Output Voltage	T_A = 25°C, R_L ≥ 10 kΩ		1.4		V
Temperature Coefficient	−40°C ≤ T_A ≤ +125°C, R_L ≥ 10 kΩ		4.8		mV/°C
Short-Circuit Current Source/ Sink Capability	25°C ≤ T_A ≤ 125°C		4/0.05		mA
	−55°C ≤ T_A ≤ +25°C		3/0.05		mA
Voltage Regulation	T_A = 25°C, I_{LOAD} = 1 mA		−2.8		%
RMS TARGET INTERFACE	VTGT (Pin 12)				
Input Voltage Range		0.2		2.5	V
Input Bias Current	V_{TGT} = 0.8 V		8		µA
Input Resistance			100		kΩ
POWER-DOWN INTERFACE	VTADJ/PWDN (Pin 1)				
Voltage Level to Enable	V_{PWDN} decreasing			1.3	V
Voltage Level to Disable	V_{PWDN} increasing	1.4			V
Input Bias Current	V_{PWDN} = 5 V		72		µA
	V_{PWDN} = 0 V		0.1		µA
Enable Time	V_{PWDN} low to V_{RMS}, 10% to 90%, C_{RMS} = 1 nF, P_{IN} = 0 dBm		1.4		µs
Disable Time	V_{PWDN} high to V_{RMS}, 90% to 10%, C_{RMS} = 1 nF, P_{IN} = 0 dBm		1.0		µs

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
POWER SUPPLY INTERFACE	VPOS1, VPOS2 (Pin 3, Pin 10)				
Supply Voltage		4.75	5	5.25	V
Quiescent Current	T_A = 25°C, P_{IN} < –60 dBm		68		mA
	T_A = 125°C, P_{IN} < –60 dBm		86		mA
Power-Down Current	V_{PWDN} > 1.4 V		250		µA

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage, VPOS1, VPOS2	5.25 V
Input Average RF Power[1]	21 dBm
Equivalent Voltage, Sine Wave Input	2.51 V p-p
Internal Power Dissipation	550 mW
θ_{JC}[2]	10.6°C/W
θ_{JB}[2]	35.3°C/W
θ_{JA}[2]	57.2°C/W
Ψ_{JT}[2]	1.0°C/W
Ψ_{JB}[2]	34°C/W
Maximum Junction Temperature	150°C
Operating Temperature Range (ADL5906ACPZN)	−40°C to +105°C
Operating Temperature Range (ADL5906SCPZN)	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

[1] This is for long durations. Excursions above this level, with durations much less than 1 second, are possible without damage.
[2] No airflow with the exposed pad soldered to a 4-layer JEDEC board.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

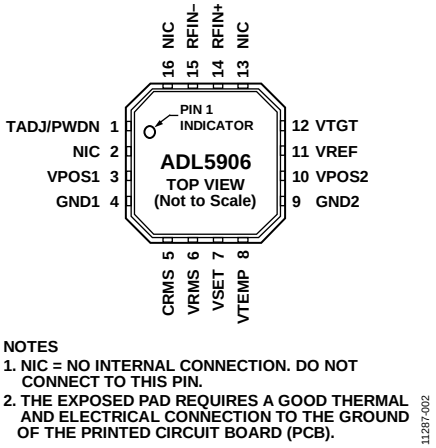

Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	TADJ/PWDN	Temperature Compensation/Shutdown. This is a dual function pin used for controlling temperature slope compensation at voltages <1.0 V and/or for shutting down the device at voltages >1.4 V. The temperature compensation voltage is generally set by connecting this pin to VREF through a resistive voltage divider (see the Setting V_{TADJ} section for additional information). See Figure 46 for an equivalent circuit.
2, 13, 16	NIC	No Internal Connection. Do not connect to these pins. These pins are not internally connected.
3, 10	VPOS1, VPOS2	Power Supply. Because these pins are internally shorted, they must be connected to the same 5 V power supply. The power supply to each pin must also be decoupled using 100 pF and 100 nF capacitors located as close as possible to the pins.
4, 9	GND1, GND2	Ground. Connect both GND1 and GND2 to system ground using a low impedance path.
5	CRMS	RMS Averaging Capacitor. Connect an rms averaging capacitor between CRMS and ground. See the Choosing a Value for C_{RMS} section for more information. See Figure 48 for an equivalent circuit.
6	VRMS	RMS Output. In measurement mode, this pin is connected to VSET either directly or through a resistor divider (when the slope is being increased). In controller mode, this pin is used to drive the gain control input of a voltage variable attenuator (VVA) or variable gain amplifier (VGA). See Figure 48 for an equivalent circuit.
7	VSET	Setpoint Input. In measurement mode, this pin is connected to VRMS either directly or through a resistor divider. In controller mode, the voltage applied to this pin sets the decibel value of the required RF input level to balance the automatic power control loop. See Figure 47 for an equivalent circuit.
8	VTEMP	Temperature Sensor Output of 1.4 V at 25°C with a Coefficient of 4.8 mV/°C. See Figure 43 for an equivalent circuit.
11	VREF	Reference Voltage Output. This voltage reference has a nominal value of 2.3 V. This reference output voltage can be used to set the voltage to the TADJ/PWDN and VTGT pins. See Figure 44 for an equivalent circuit.
12	VTGT	RMS Target Voltage. The voltage applied to this pin sets the target RF input at the output of the VGA that is also the rms squaring circuit. The recommended voltage for VTGT is 0.8 V. Increasing V_{TGT} above 0.8 V degrades the rms accuracy of the ADL5906. Reducing V_{TGT} below 0.8 V can improve the rms accuracy for signals with very high crest factors; however, it reduces the detection range of the ADL5906. See Figure 49 for an equivalent circuit.
14, 15	RFIN+, RFIN–	RF Inputs. The RF inputs are normally applied single-ended with the RF input signal ac-coupled to RFIN+ and RFIN– ac-coupled to ground. See Figure 42 for an equivalent circuit.
EPAD		The exposed pad on the underside of the device (EPAD) is also internally connected to ground and requires a good thermal and electrical connection to the ground of the printed circuit board (PCB).

TYPICAL PERFORMANCE CHARACTERISTICS

VPOS1 = VPOS2 = 5 V, single-ended input drive, VRMS connected to VSET, V_{TGT} = 0.8 V, C_{RMS} = 0.1 µF, T_A = +25°C (green), −55°C (light blue), −40°C (blue), +85°C (red), +105°C (orange), and +125°C (black), where appropriate. Error referred to slope and intercept at indicated calibration points. Input RF signal is a sine wave (CW), unless otherwise indicated.

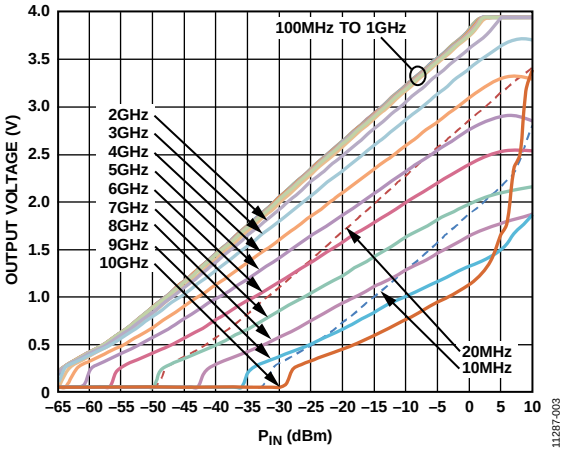

Figure 3. Typical V_{RMS} vs. Input Power (dBm) vs. Frequency (10 MHz to 10 GHz) at 25°C

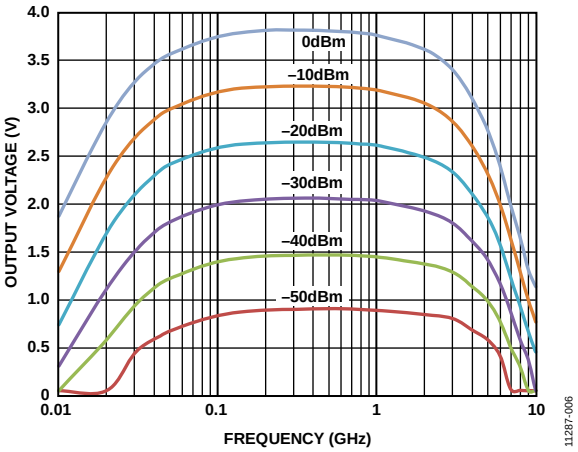

Figure 6. Typical V_{RMS} vs. Frequency for Six RF Input Levels

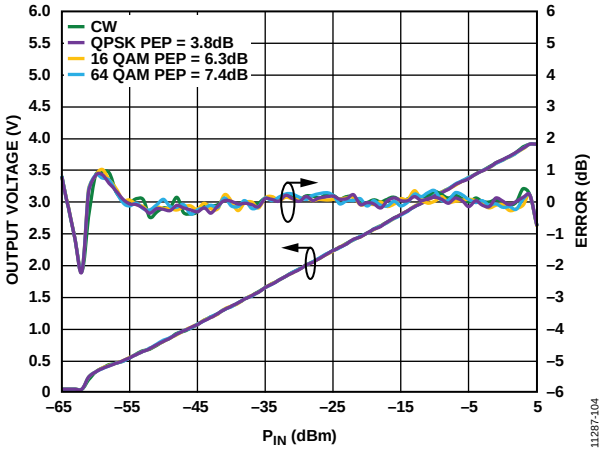

Figure 4. Error from CW Linear Reference vs. Signal Modulation (QPSK, 16 QAM, 64 QAM), Frequency = 900 MHz, C_{RMS} = 0.1 µF, Three Point Calibration at 0 dBm, −40 dBm, and −55 dBm

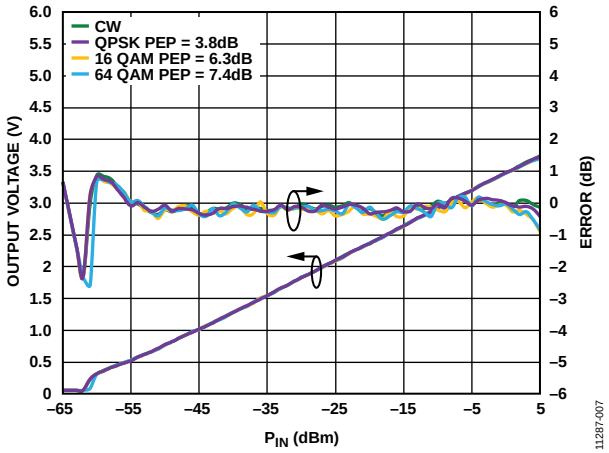

Figure 7. Error from CW Linear Reference vs. Signal Modulation (QPSK, 16 QAM, 64 QAM), Frequency = 2.14 GHz, C_{RMS} = 0.1 µF, Three Point Calibration at 0 dBm, −40 dBm, and −55 dBm

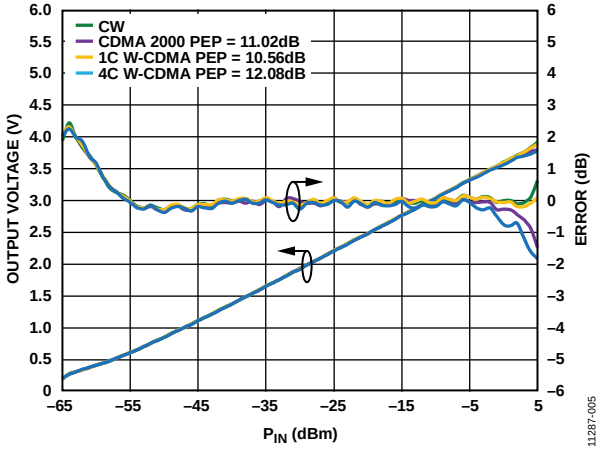

Figure 5. Error from CW Linear Reference vs. Signal Modulation (CDMA 2000, One-Carrier W-CDMA, Four-Carrier W-CDMA), Frequency = 2.14 GHz, C_{RMS} = 0.1 µF, Three Point Calibration at 0 dBm, −40 dBm, and −55 dBm

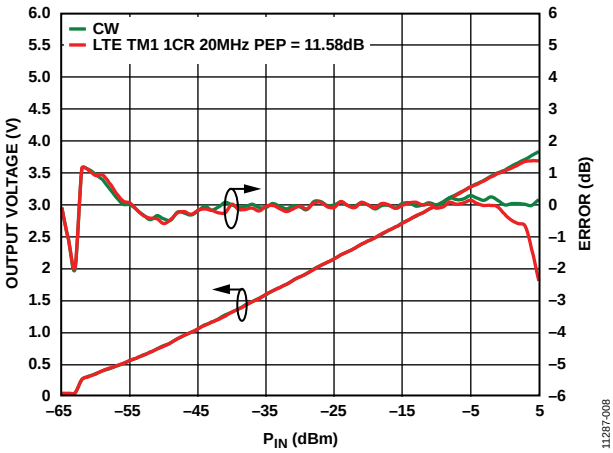

Figure 8. Error from CW Linear Reference vs. Signal Modulation (LTE TM1 One-Carrier, 20 MHz), Frequency = 2.14 GHz, C_{RMS} = 0.1 µF, Three Point Calibration at 0 dBm, −40 dBm, and −55 dBm

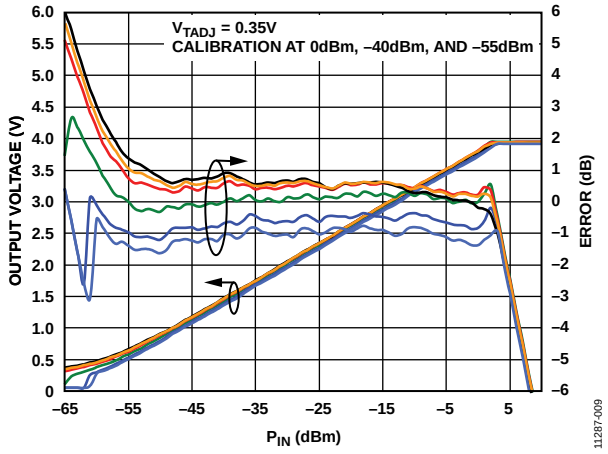

Figure 9. V_{RMS} and Log Conformance Error vs. Input Level and Temperature at 100 MHz

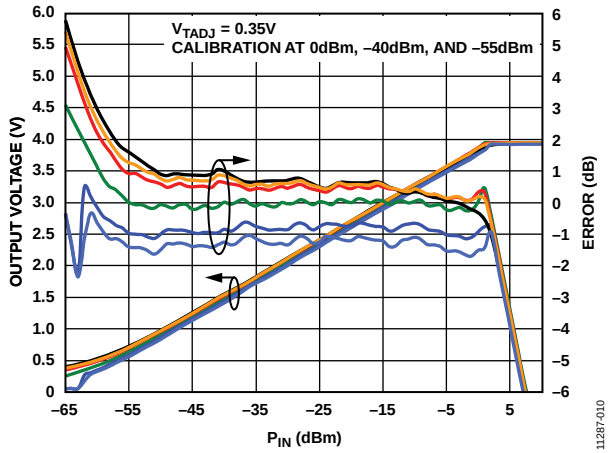

Figure 10. V_{RMS} and Log Conformance Error vs. Input Level and Temperature at 700 MHz

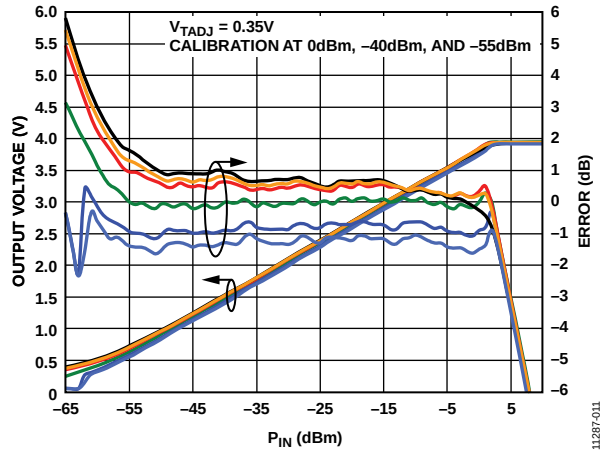

Figure 11. V_{RMS} and Log Conformance Error vs. Input Level and Temperature at 900 MHz

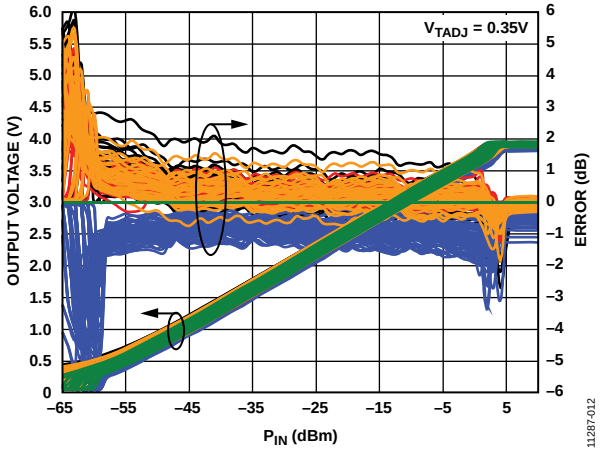

Figure 12. Distribution of Log Conformance Error with Respect to V_{RMS} at 25°C vs. Input Level and Temperature at 100 MHz

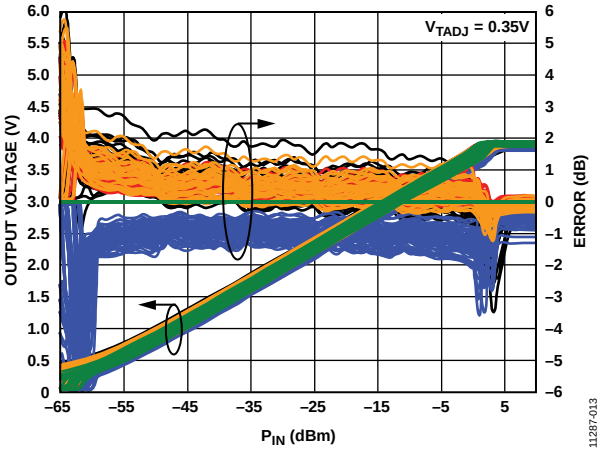

Figure 13. Distribution of Log Conformance Error with Respect to V_{RMS} at 25°C vs. Input Level and Temperature at 700 MHz

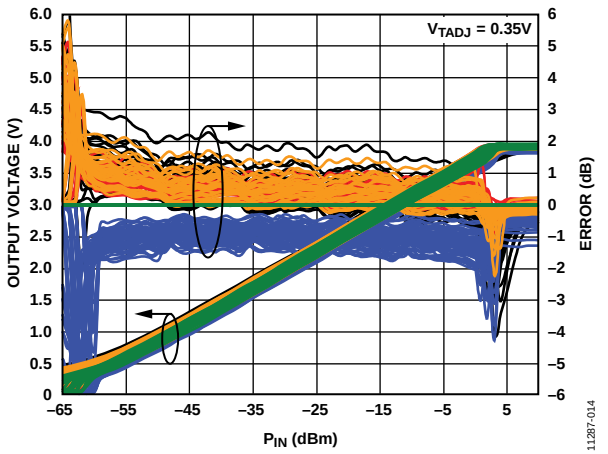

Figure 14. Distribution of Log Conformance Error with Respect to V_{RMS} at 25°C vs. Input Level and Temperature at 900 MHz

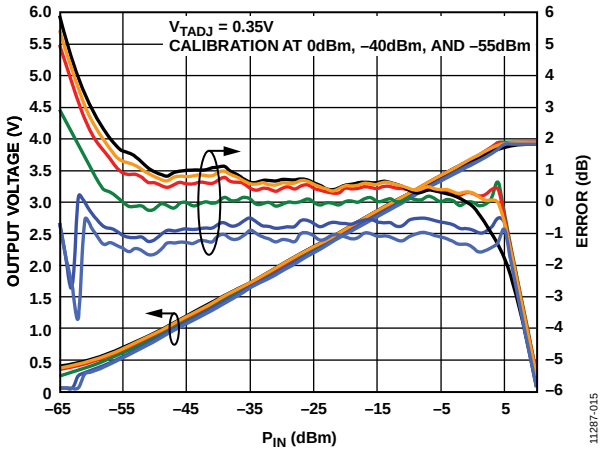

Figure 15. V_{RMS} and Log Conformance Error vs. Input Level and Temperature at 1.9 GHz

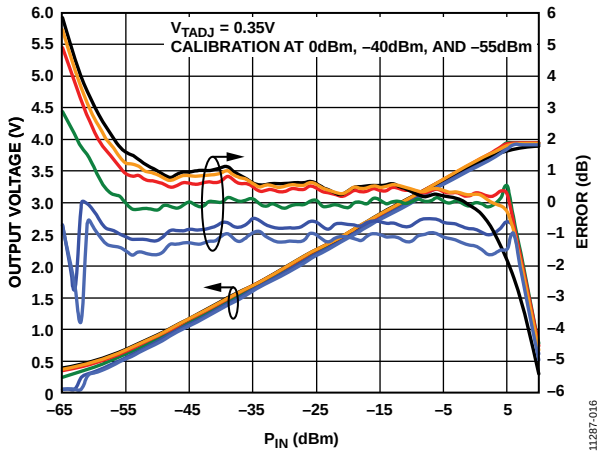

Figure 16. V_{RMS} and Log Conformance Error vs. Input Level and Temperature at 2.14 GHz

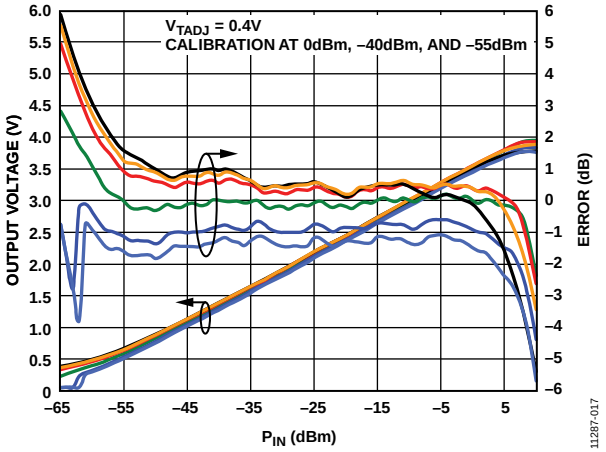

Figure 17. V_{RMS} and Log Conformance Error vs. Input Level and Temperature at 2.6 GHz

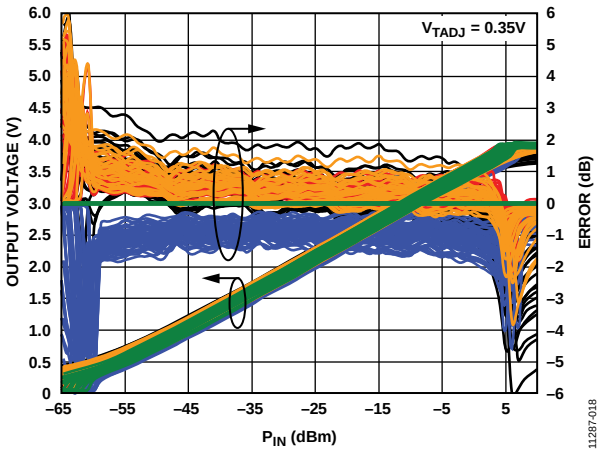

Figure 18. Distribution of Log Conformance Error with Respect to V_{RMS} at 25°C vs. Input Level and Temperature at 1.9 GHz

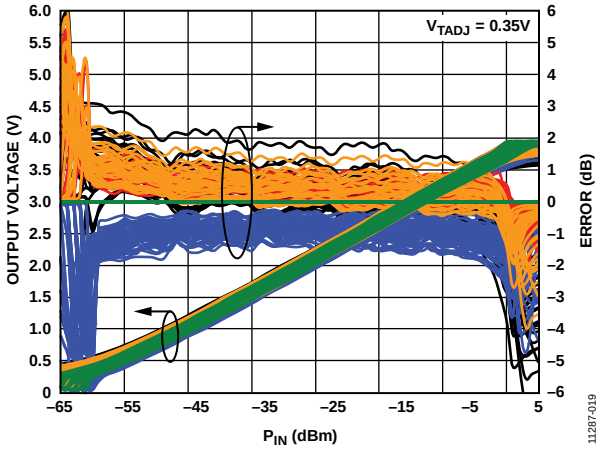

Figure 19. Distribution of Log Conformance Error with Respect to V_{RMS} at 25°C vs. Input Level and Temperature at 2.14 GHz

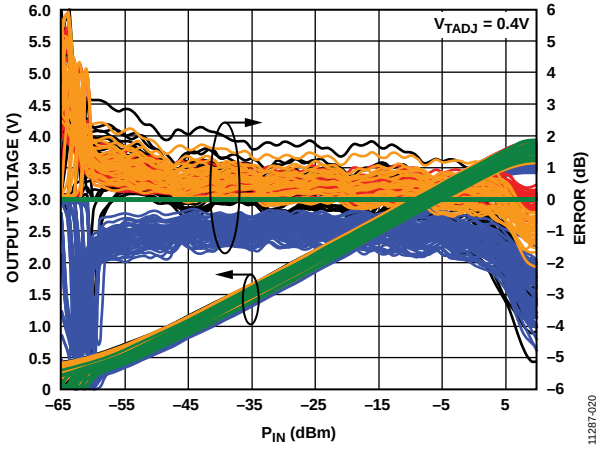

Figure 20. Distribution of Log Conformance Error with Respect to V_{RMS} at 25°C vs. Input Level and Temperature at 2.6 GHz

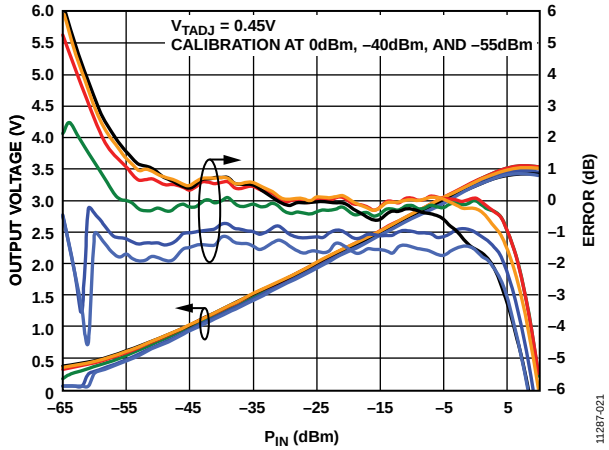

Figure 21. V_{RMS} and Log Conformance Error vs. Input Level and Temperature at 3.5 GHz

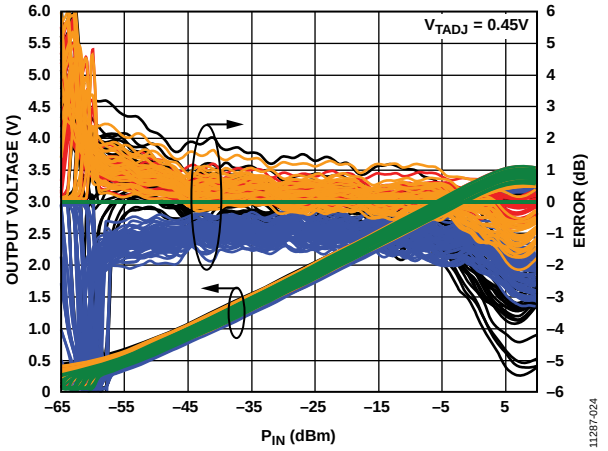

Figure 24. Distribution of Log Conformance Error with Respect to V_{RMS} at 25°C vs. Input Level and Temperature at 3.5 GHz

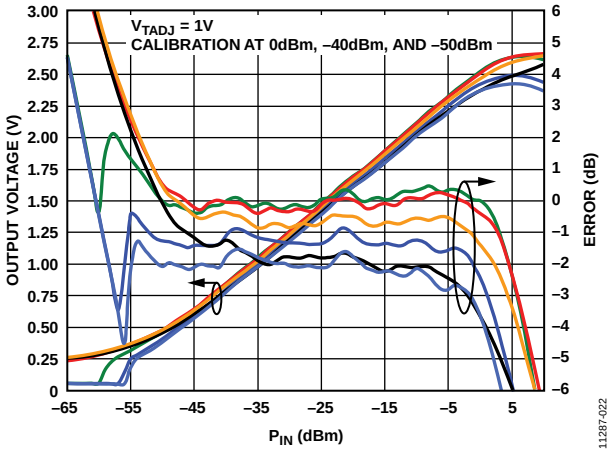

Figure 22. V_{RMS} and Log Conformance Error vs. Input Level and Temperature at 5.8 GHz

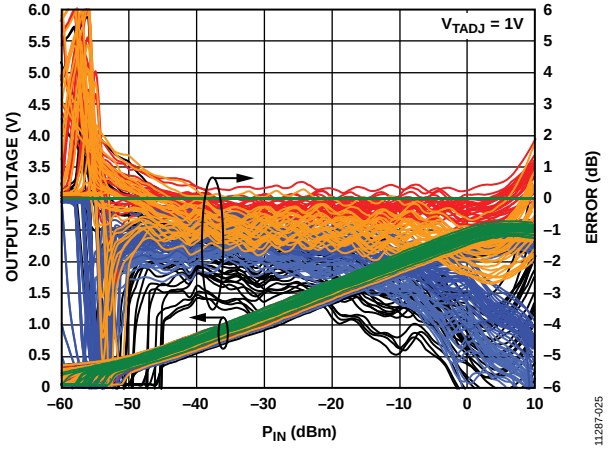

Figure 25. Distribution of Log Conformance Error with Respect to V_{RMS} at 25°C vs. Input Level and Temperature at 5.8 GHz

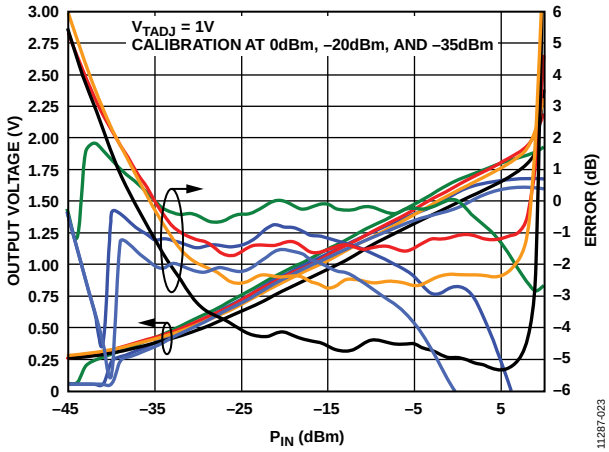

Figure 23. V_{RMS} and Log Conformance Error vs. Input Level and Temperature at 8 GHz

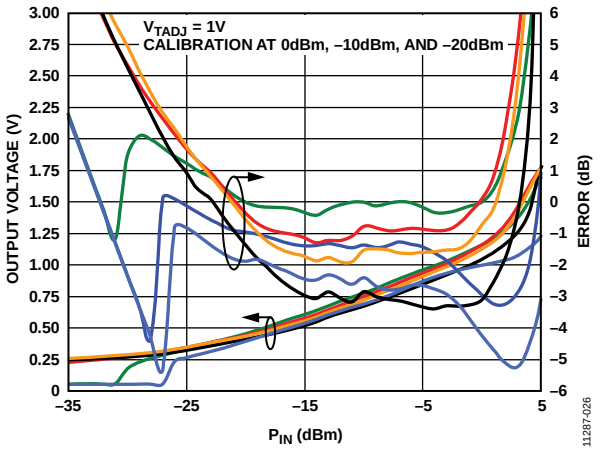

Figure 26. V_{RMS} and Log Conformance Error vs. Input Level and Temperature at 10 GHz

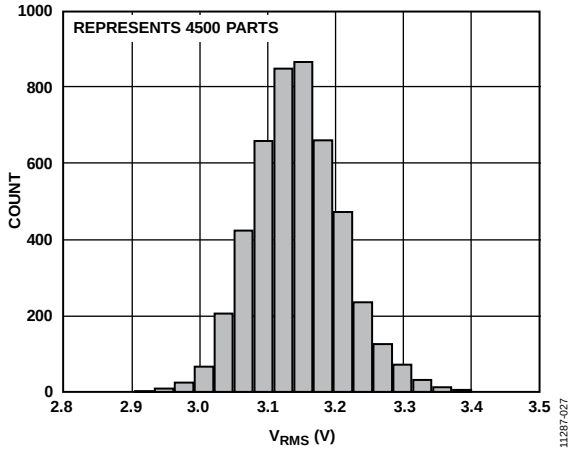

Figure 27. Distribution of V_{RMS}, P_{IN} = −10 dBm, 900 MHz

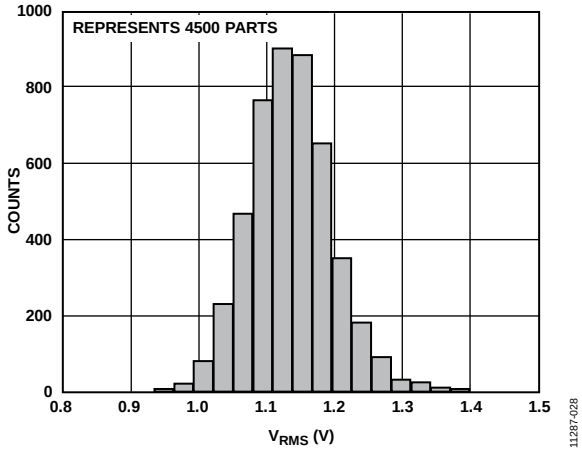

Figure 28. Distribution of V_{RMS}, P_{IN} = −45 dBm, 900 MHz

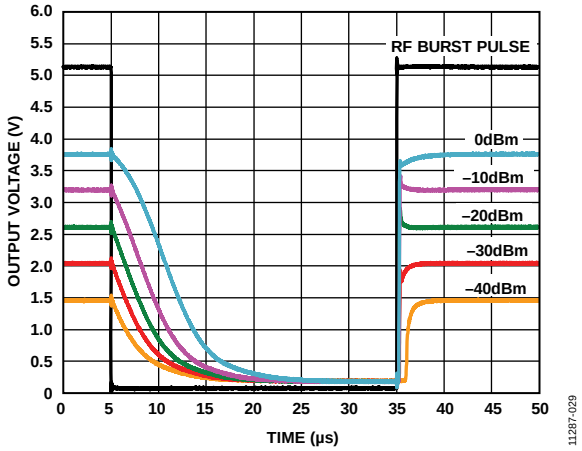

Figure 29. Output Response to RF Burst Input, Carrier Frequency = 2.14 GHz, C_{RMS} = 1 nF

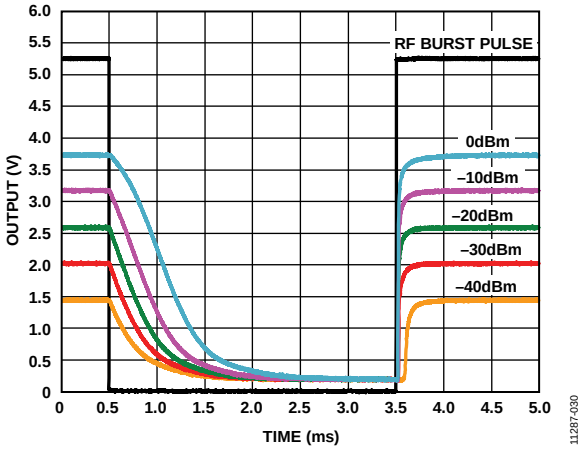

Figure 30. Output Response to RF Burst Input, Carrier Frequency = 2.14 GHz, C_{RMS} = 0.1 µF

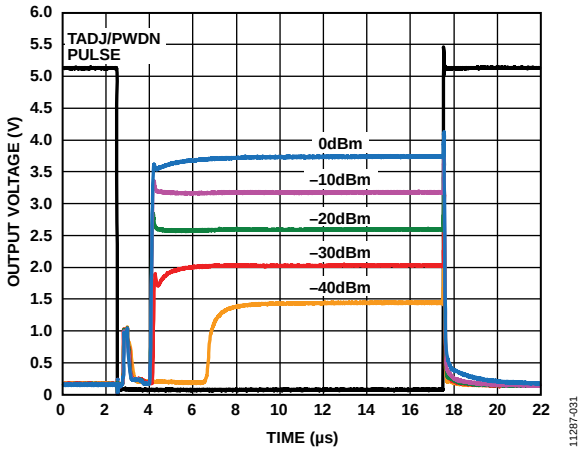

Figure 31. Output Response Using Power-Down Mode for Various RF Input Levels, Carrier Frequency = 2.14 GHz, C_{RMS} = 1 nF

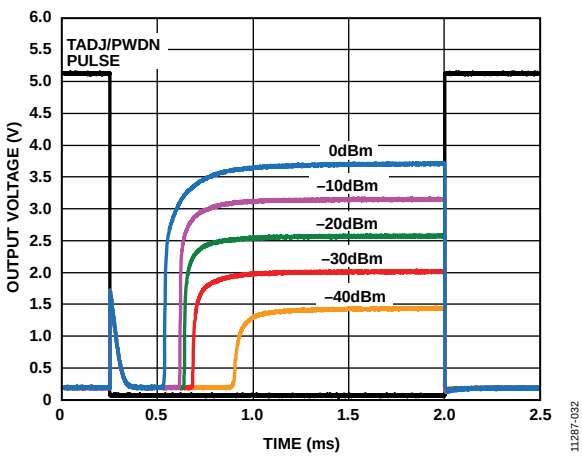

Figure 32. Output Response Using Power-Down Mode for Various RF Input Levels, Carrier Frequency = 2.14 GHz, C_{RMS} = 0.1 µF

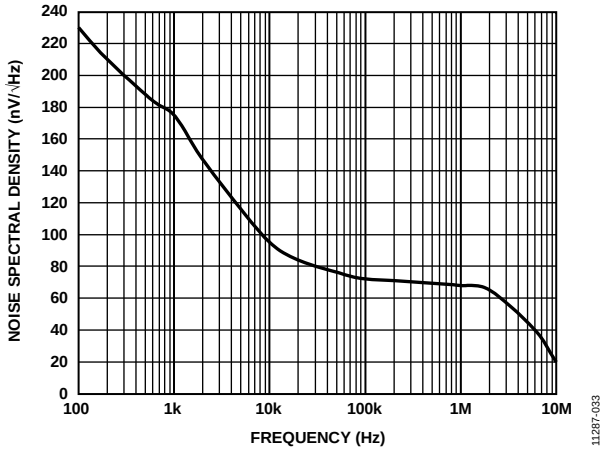

Figure 33. Noise Spectral Density of V_{RMS}, P_{IN} = −10 dBm, −35 dBm, and −60 dBm (No Change in NSD vs. P_{IN}), C_{RMS} = 0.1 µF

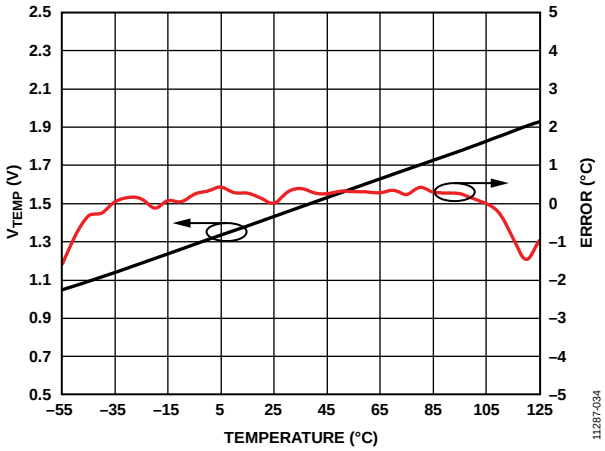

Figure 34. V_{TEMP} and Linearity Error with Respect to Straight Line vs. Temperature for Typical Device

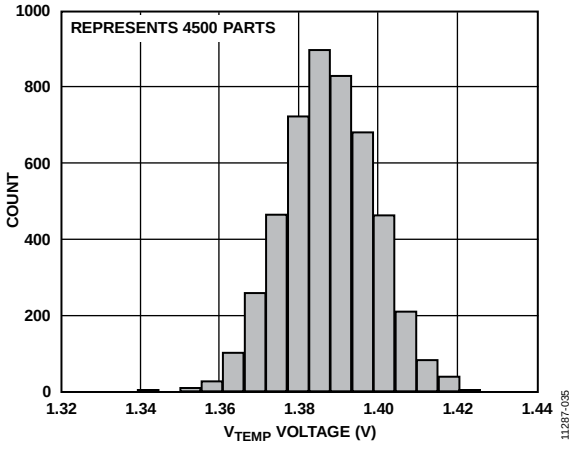

Figure 35. Distribution of V_{TEMP} at 25°C, No RF Input

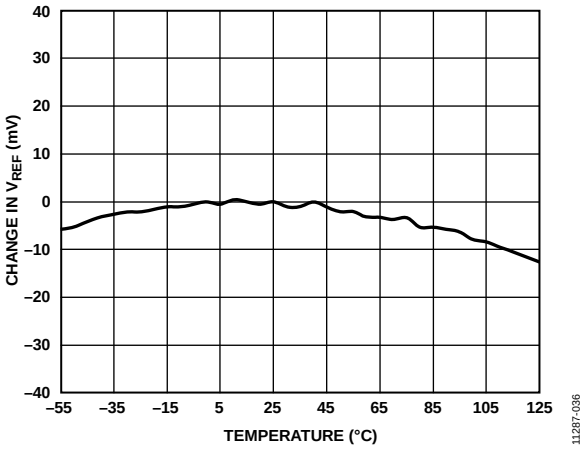

Figure 36. Change in V_{REF} vs. Temperature with Respect to 25°C, P_{IN} = −40 dBm

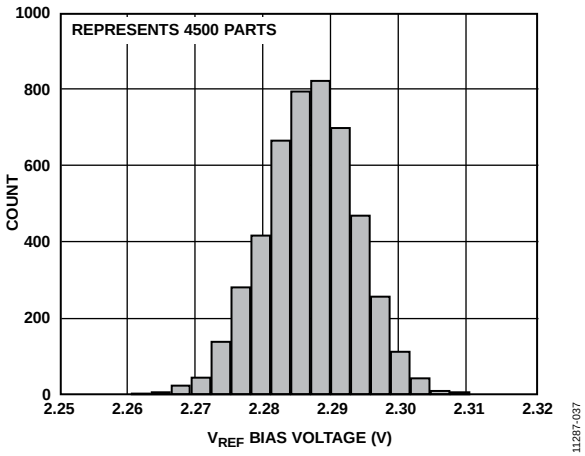

Figure 37. Distribution of V_{REF} at 25°C, No RF Input

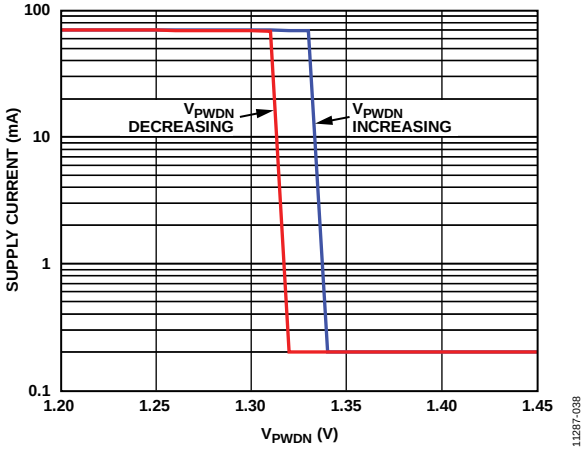

Figure 38. Supply Current vs. V_{PWDN}

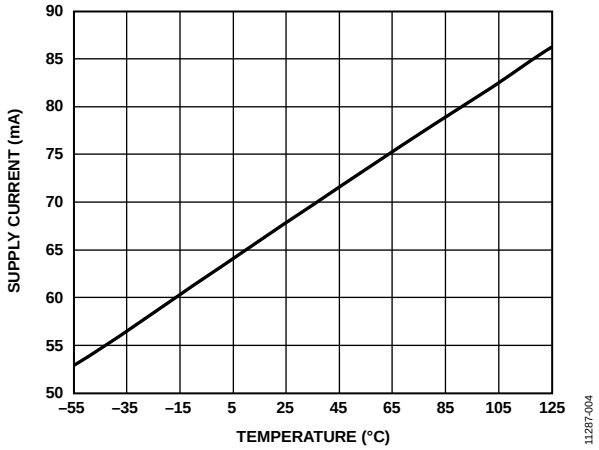

Figure 39. Supply Current vs. Temperature

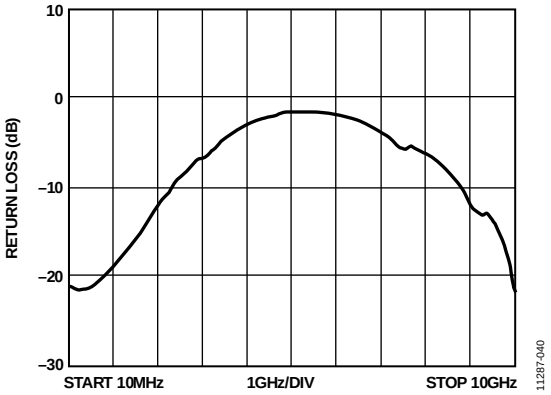

Figure 40. Return Loss at RF Input Port, 10 MHz to 10 GHz

THEORY OF OPERATION

The ADL5906 is functionally nearly identical to the ADL5902 but has a broader frequency range (10 MHz to 10 GHz). It is a true rms responding detector with a 67 dB measurement range at 2.14 GHz and a greater than 57 dB measurement range at frequencies up to 5.8 GHz. It is pin compatible with the ADL5902 and AD8363. Transfer function peak-to-peak ripple is <±0.3 dB over the entire dynamic range. Temperature stability of the rms output measurements provides <±1 dB error typical over the temperature range of −40°C to +125°C up to 3.5 GHz. The device accurately measures waveforms that have a high peak-to-rms ratio (crest factor).

The ADL5906 consists of a high performance automatic gain control (AGC) loop. As shown in Figure 41, the AGC loop comprises a wide bandwidth variable gain amplifier (VGA), square law detectors, an amplitude target circuit, and an output driver.

The nomenclature used in this data sheet to distinguish between a pin name and the signal on that pin is as follows:

- The pin name is all uppercase, for example, CRMS, VSET, and VRMS.
- The signal name or a value associated with that pin is the pin mnemonic with a partial subscript, for example, C_{RMS}, V_{SET}, and V_{RMS}.

SQUARE LAW DETECTOR AND AMPLITUDE TARGET

The VGA gain has the form

$$G_{SET} = G_O \, e^{-(V_{SET}/V_{GNS})} \quad (1)$$

where:
G_O is the basic fixed gain.
V_{GNS} is a scaling voltage that defines the gain slope (the decibel change per voltage). The gain decreases with increasing V_{SET}.

The VGA output is

$$V_{SIG} = G_{SET} \times RF_{IN} = G_O \times RF_{IN} \, e^{-(V_{SET}/V_{GNS})} \quad (2)$$

where RF_{IN} is the ac voltage applied to the input terminals of the ADL5906.

The output of the VGA, V_{SIG}, is applied to a wideband square law detector. The detector provides the true rms response of the RF input signal, independent of waveform. The detector output, I_{SQR}, is a fluctuating current with a positive mean value. The difference between I_{SQR} and an internally generated current, I_{TGT}, is integrated by the parallel combination of C_F and the external capacitor attached to the CRMS pin at the summing node. C_F is an on-chip 26 pF filter capacitor, and C_{RMS}, the external capacitance connected to the CRMS pin, can be used to arbitrarily increase the averaging time while trading off with the response time. When the AGC loop is at equilibrium

$$Mean(I_{SQR}) = I_{TGT} \quad (3)$$

This equilibrium occurs only when

$$Mean(V_{SIG}^2) = V_{TGT}^2 \quad (4)$$

where V_{TGT} is the voltage presented at the VTGT pin. This pin can conveniently be connected to the VREF pin through a voltage divider to establish a target rms voltage, V_{ATG}, of ~40 mV rms when V_{TGT} = 0.8 V.

Because the square law detectors are electrically identical and well matched, process and temperature dependent variations are effectively cancelled.

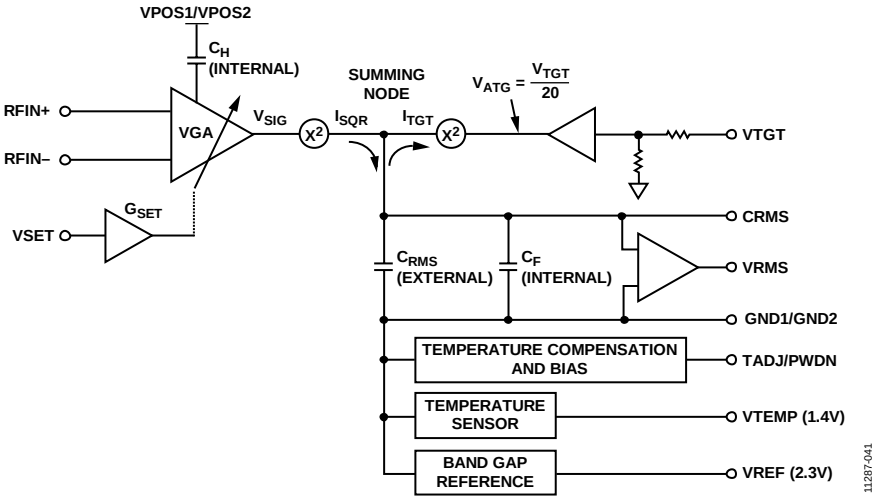

Figure 41. Simplified Architecture Details

When forcing the previous identity by varying the VGA setpoint, it is apparent that

$$RMS(V_{SIG}) = \sqrt{(Mean(V_{SIG}^2))} = \sqrt{(V_{ATG}^2)} = V_{ATG} \quad (5)$$

Substituting the value of V_{SIG} from Equation 2 results in

$$RMS(G_0 \times RF_{IN}\, e^{-(V_{SET}/V_{GNS})}) = V_{ATG} \quad (6)$$

When connected as a measurement device, $V_{SET} = V_{RMS}$. Solving for V_{RMS} as a function of RF_{IN},

$$V_{RMS} = V_{SLOPE} \times \log_{10}(RMS(RF_{IN})/V_Z) \quad (7)$$

where:
V_{SLOPE} = 1.12 V/decade (or 56 mV/dB) at 2.14 GHz.
V_Z is the intercept voltage.

When $RMS(RF_{IN}) = V_Z$, this implies that $V_{RMS} = 0$ V because $\log_{10}(1) = 0$. This makes the intercept the input that forces V_{RMS} = 0 V if the ADL5906 had no sensitivity limit.

In most applications, the AGC loop is closed through the setpoint interface and the VSET pin. In measurement mode, VRMS is directly connected to VSET (see the Measurement Mode Basic Connections section for more information). In controller mode, a control voltage is applied to VSET, and the VRMS pin typically drives the control input of an amplification or attenuation system. In this case, the voltage at the VSET pin forces a signal amplitude at the RF inputs of the ADL5906 that balances the system through feedback.

RF INPUT INTERFACE

Figure 42 shows the RF input connections within the ADL5906. Two internal 2.5 kΩ resistors connected between RFIN+ and RFIN− primarily set the input impedance. A dc level of approximately half the supply voltage on each pin is established internally at the center point of the bias resistors. Either the RFIN+ or the RFIN− pin can be used as the single-ended RF input pin. Connect signal coupling capacitors from the input signal to the RFIN+ and RFIN− pins. A single external 60.4 Ω resistor to ground from the desired input creates an equivalent 50 Ω impedance over a broad section of the operating frequency range. RF ac-couple the other input pin to common (ground). The input signal high-pass corner formed by the internal and external resistances of the input coupling capacitor is

$$f_{HIGHPASS} = 1/(2 \times \pi \times 50 \times C) \quad (8)$$

where C is the capacitance in farads, and $f_{HIGHPASS}$ is in hertz.

The input coupling capacitors must be large enough in value to pass the input signal frequency of interest and determine the low end of the frequency response. RFIN+ and RFIN− can also be driven differentially using a balun.

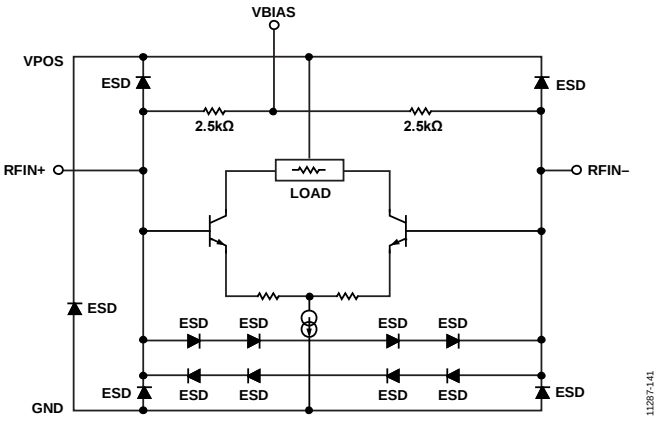

Figure 42. RF Inputs

Extensive ESD protection is employed on the RF inputs, and this protection limits the maximum possible input to the ADL5906.

TEMPERATURE SENSOR INTERFACE

The ADL5906 provides a temperature sensor output with a scaling factor of the output voltage of approximately 4.8 mV/°C. The output is capable of sourcing 4 mA and sinking 50 µA maximum at 25°C. An external resistor can be connected from VTEMP to GND to provide additional current sink capability. The typical output voltage at 25°C is approximately 1.4 V.

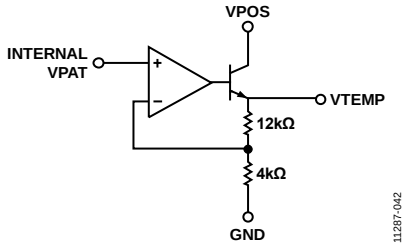

Figure 43. TEMP Interface Simplified Schematic

VREF INTERFACE

The VREF pin provides an internally generated voltage reference for the user. The VREF voltage is a temperature stable 2.3 V reference that is capable of sourcing 4 mA and sinking 50 µA maximum. An external resistor can be connected from VREF to GND to provide additional current sink capability. The voltage on this pin can be used to drive the TADJ/PWDN and VTGT pins.

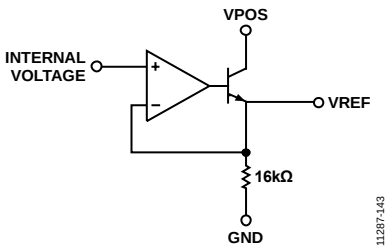

Figure 44. VREF Interface Simplified Schematic

TEMPERATURE COMPENSATION INTERFACE

The ADL5906 has a TADJ pin that provides the ability to optimize temperature performance using proprietary techniques as in the ADL5902. Just like the ADL5902, the ADL5906 has dual functionality on Pin 1, TADJ/PWDN; however, the PWDN function was redesigned to be driven by CMOS logic as low as 1.8 V. For more detail on the power-down interface, see the Power-Down Interface section.

For optimal performance, the output temperature drift must be compensated using the TADJ pin. The absolute value of compensation varies with frequency and VTGT. For recommended V_{TADJ} values at popular frequencies, see the Setting VTADJ section.

One difference in the temperature compensation of the ADL5906 compared to the ADL5902 is that V_{TADJ} adjusts the slope of the detector, and with the ADL5902, the intercept was adjusted. Adjusting the slope was found beneficial to locking in temperature drift and thereby producing parallel error curves over most frequencies. Any remaining intercept temperature drift can then be reduced in the digital domain after sampling V_{RMS} because the intercept drift is quite repeatable at frequencies up to approximately 5.8 GHz (see the Using VTEMP to Improve Intercept Temperature Drift section).

There is a trade-off in setting values, and optimizing for one area of the dynamic range may mean less than optimal drift performance at other input amplitudes. In addition, different voltages applied to the VTGT pin impact drift; all TADJ voltages shown in the performance curves were determined with a VTGT of 0.8 V. For VTGT values that do not deviate too far from the nominal 0.8 V, and for frequencies up to approximately 5 GHz, it is expected that the TADJ voltages are a good starting point for the best temperature drift compensation.

Compensating the device for temperature drift using V_{TADJ} allows for great flexibility. If the user requires minimum temperature drift at a given input power, a subset of the dynamic range, or even over a different temperature range than shown in this data sheet, the V_{TADJ} can be swept while monitoring V_{RMS} over the temperature at the frequency and amplitude of interest. The optimal V_{TADJ} to achieve minimum temperature drift at a given power and frequency is the value of V_{TADJ} where the output has minimum movement.

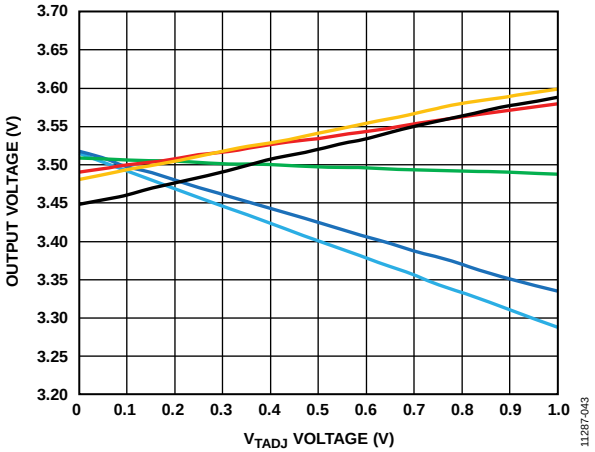

Figure 45. Effect of V_{TADJ} at Various Temperatures, 2.14 GHz, 0 dBm

Varying V_{TADJ} has only a very slight effect on VRMS at device temperatures near 25°C; however, the compensation circuit has increasing effect as the temperature departs farther from 25°C.

It is important to note that the slope is adjusted vs. temperature. The pivot point of this is at low input power levels and thereby moves the V_{RMS} output more at larger input signal levels; that is, near maximum input power, the temperature drift can be minimized the most. This is advantageous in most power measurement cases because errors at larger powers tend to have more of a negative effect.

The TADJ/PWDN pin has a nominal input resistance of 70 kΩ and can be conveniently driven from an external source or from an attenuated value of VREF using a resistor divider. The resistors are shown in the evaluation board schematic (see Figure 63). The voltage range for V_{TADJ} is from 0 V to approximately 1.0 V because approximately 1.3 V is the logic threshold for power down of the device.

POWER-DOWN INTERFACE

Figure 46 shows a simplified schematic representation of the TADJ/PWDN interface.

The quiescent and power-down currents for the ADL5906 at 25°C are approximately 68 mA and 250 µA, respectively. The dual function TADJ/PWDN pin is connected to the temperature compensation circuit as well as the power-down circuit. The temperature compensation circuit responds only to voltages between 0 V and 1 V. When the voltage on this pin is greater than ~1.4 V, the device is fully powered down. Figure 38 shows this characteristic as a function of V_{PWDN}. The TADJ/PWDN pin with an internal 70 kΩ resistor to ground sinks approximately 26 µA at 1.8 V, 47 µA at 3.3 V, and 72 µA at 5 V. The source used to disable the ADL5906 must have a sufficiently high current capability for this reason. Figure 31 shows the typical response times for various RF input levels. The output reaches within 1 dB of its steady state value in approximately 12 µs for C_{RMS} = 1 nF; however, the reference voltage is available to full accuracy in a much shorter time. This wake-up response varies depending on the input coupling and the value of C_{RMS}.

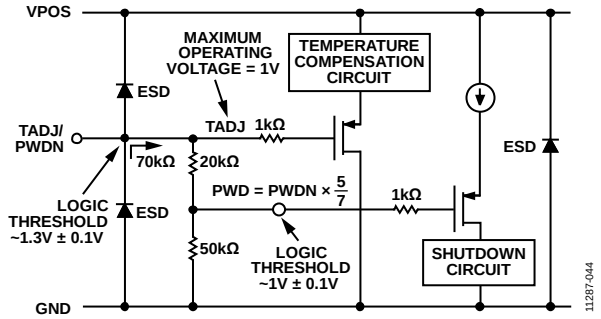

Figure 46. TADJ/PWDN Interface Simplified Schematic

VSET INTERFACE

The VSET interface has a high input impedance of 72 kΩ. The voltage at VSET is converted to an internal current used to set the internal VGA gain. The VGA attenuation control is approximately 18 dB/V.

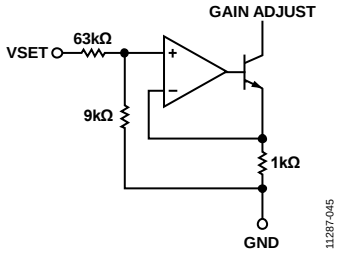

Figure 47. VSET Interface Simplified Schematic

OUTPUT INTERFACE

The ADL5906 incorporates rail-to-rail output drivers with pull-up and pull-down capabilities. The level shift circuitry and the output amplifier are very fast compared to the typical rms response required by a complex waveform. In essence, the output stage from the CRMS pin to the VRMS output is only a dc signal because by definition V_{RMS} is supposed to be a single rms value. The VRMS pin can source and sink up to 10 mA.

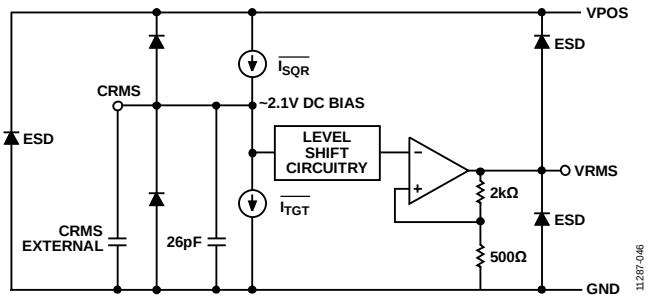

Figure 48. VRMS Interface Simplified Schematic

VTGT INTERFACE

The target voltage can be set with an external source or by connecting the VREF pin (nominally 2.3 V) to the VTGT pin through a resistive voltage divider. With 0.8 V on the VTGT pin, the rms voltage that must be provided by the VGA to balance the AGC feedback loop is 0.8 V × 0.05 = 40 mV rms. Most of the characterization information in this data sheet was collected at V_{TGT} = 0.8 V. Voltages higher and lower than this can be used; however, doing so increases or decreases the gain at the internal squaring cell, which results in a corresponding increase or decrease in intercept. This, in turn, affects the sensitivity and the usable measurement range, in addition to the sensitivity to different carrier modulation schemes. As V_{TGT} decreases, the squaring circuits produce more noise; this becomes noticeable in the output response at low input signal amplitudes. As V_{TGT} increases, measurement error due to modulation increases, and temperature drift tends to decrease. The chosen V_{TGT} value of 0.8 V represents a compromise between these characteristics.

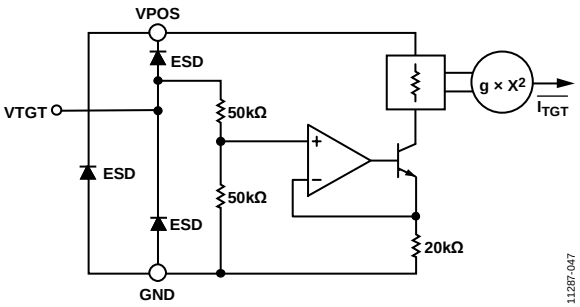

Figure 49. VTGT Interface

BASIS FOR ERROR CALCULATIONS

The slope and intercept used in the error plots are calculated using the coefficients of a linear regression performed on data collected in its central operating range. The error plots in the Typical Performance Characteristics section are shown in two formats: error from the ideal line and error with respect to the 25°C output voltage. The error from the ideal line is the decibel difference in V_{RMS} from the ideal straight-line fit of V_{RMS} calculated by the linear regression fit over the linear range of the detector, typically at 25°C. The error in decibels is calculated by

$$Error\ (dB) = (V_{RMS} - Slope \times (P_{IN} - P_Z))/Slope \quad (9)$$

where P_Z is the x-axis intercept expressed in decibels relative to 1 mW (the input amplitude that produces a 0 V output if such an output were possible).

The error from the ideal line is not a measure of absolute accuracy because it is calculated using the slope and intercept of each device. However, it verifies the linearity and the effect of temperature and modulation on the response of the device. An example of this type of plot is Figure 9. The slope and intercept that form the ideal line are those at 25°C with CW modulation. Figure 4, Figure 5, Figure 7, and Figure 8 show the error with various popular forms of modulation with respect to the ideal CW line. This method for calculating error is accurate, assuming that each device is calibrated at room temperature.

In the second plot format, the V_{RMS} voltage at a given input amplitude and temperature is subtracted from the corresponding V_{RMS} at 25°C and then divided by the 25°C slope to obtain an error in decibels. This type of plot does not provide any information on the linear-in-dB performance of the device; it merely shows the decibel equivalent of the deviation of V_{RMS} over temperature, given a calibration at 25°C. When calculating error from any one particular calibration point, this error format is accurate. It is accurate over the full range shown on the plot assuming that enough calibration points are used. Figure 12 shows this plot type.

The error calculations for Figure 34 are similar to those for the V_{RMS} plots. The slope and intercept of the V_{TEMP} function vs. temperature are determined and applied as follows:

$$Error\ (°C) = (V_{TEMP} - Slope \times (Temp - T_Z))/Slope \quad (10)$$

where:
V_{TEMP} is the voltage at the TEMP pin at that temperature.
Slope is, typically, 4.8 mV/°C.
Temp is the ambient temperature of the ADL5906 in degrees Celsius.
T_Z is the x-axis intercept expressed in degrees Celsius (the temperature that would result in a V_{TEMP} of 0 V if this were possible).

MEASUREMENT MODE BASIC CONNECTIONS

The basic connections circuit for ADL5906 is shown in Figure 51. The ADL5906 requires a single supply of nominally 5 V. The supply is connected to the VPOS1 and VPOS2 supply pins. Decouple each of these pins using two capacitors with values equal or similar to those shown in Figure 51. Place these capacitors as close as possible to the VPOS pins. The three no connect pins (NIC) are not internally connected. Leave these pins unconnected.

An external 60.4 Ω resistor combines with the relatively high RF input impedance of the ADL5906 to provide a broadband 50 Ω match. Place an ac coupling capacitor between this resistor and RFIN+. AC-couple the RFIN− input to ground using the same value capacitor. To operate down to 10 MHz, the coupling capacitors must be at least 100 pF.

The ADL5906 is placed in measurement mode by connecting the VRMS pin to the VSET pin. In measurement mode, the output voltage is proportional to the log of the rms input signal level.

SETTING V_{TADJ}

As described in the Theory of Operation section, the output temperature drift can be compensated by applying a voltage to the TADJ pin. The compensating voltage varies with frequency. The voltage for the TADJ pin can be easily derived from a resistor divider connected to the VREF pin. Table 4 shows the recommended V_{TADJ} voltages for operation from −55°C to +125°C, along with resistor divider values. Resistor values are chosen so that they neither pull too much current from the VREF pin (I_{OUTMAX} = 4 mA) nor are so large that the maximum bias current at a V_{TADJ} = 1 V (14 µA) affects the resulting voltage.

The V_{TADJ} function provides temperature compensation of theoutput slope of the ADL5906. The Using VTEMP to Improve Intercept Temperature Drift section describes how the temperature stability of the ADL5906 can be further improved.

Table 4. Recommended V_{TADJ} Voltages

Frequency	V_{TADJ} (V)	R9 (Ω)	R12 (Ω)
10 MHz to 2.14 GHz	0.35	1500	270
2.6 GHz	0.4	1500	316
3.5 GHz	0.45	1500	365
5.8 GHz	1.0	1540	1200
8 GHz	1.0	1540	1200
10 GHz	1.0	1540	1200

SETTING V_{TGT}

As described in the Theory of Operation section, setting the voltage on VTGT to 0.8 V represents a compromise between achieving excellent rms accuracy and maximizing dynamic range. The voltage on VTGT can be derived from the VREF pin using a resistor divider, as shown Figure 51. Like the resistors chosen to set the V_{TADJ} voltage, the resistors setting V_{TGT} must have reasonable values that do not pull too much current from VREF or cause bias current errors. In addition, note the combined current that VREF must deliver to generate the V_{TADJ} and V_{TGT} voltages. The values shown in Figure 51 and Table 4 result in a maximum VREF current of 1.7 mA. This current is well below the maximum specified VREF current of 4 mA.

CHOOSING A VALUE FOR C_{RMS}

C_{RMS} provides the averaging function for the internal rms computation. Using the minimum value for C_{RMS} allows the quickest response time to a pulsed waveform but leaves significant output noise on the output voltage signal. By the same token, a large filter capacitor reduces output noise but at the expense of response time.

In applications where response time is not critical, a relatively large capacitor can be placed on the CRMS pin. In Figure 51, a value of 0.1 µF is used. For most signal modulation schemes, this value ensures excellent rms measurement compliance and low residual output noise. There is no maximum capacitance limit for C_{RMS}.

Figure 50 shows how output noise varies with C_{RMS} when the ADL5906 is driven by a single-carrier W-CDMA signal (Test Model TM1-64, peak envelope power = 10.56 dB, bandwidth = 3.84 MHz).

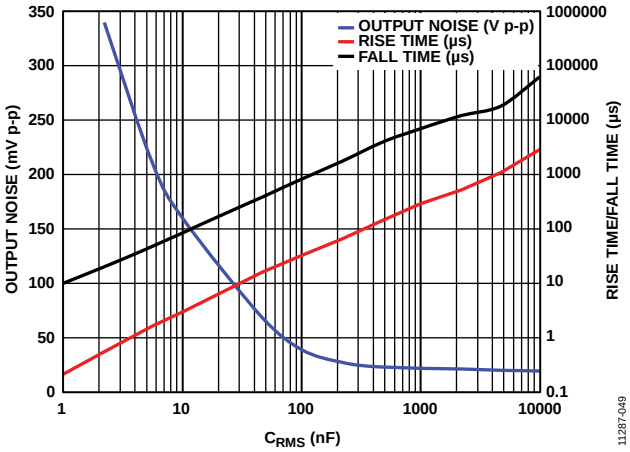

Figure 50. Output Noise, Rise and Fall Times vs. C_{RMS} Capacitance, Single-Carrier W-CDMA (TM1-64) at 2.14 GHz with P_{IN} = 0 dBm

Figure 50 also shows how the response time is affected by the value of C_{RMS}. To measure this, an RF burst at 2.14 GHz at 0 dBm was applied to the ADL5906. The 10% to 90% rise time and 90% to 10% fall time were then measured.

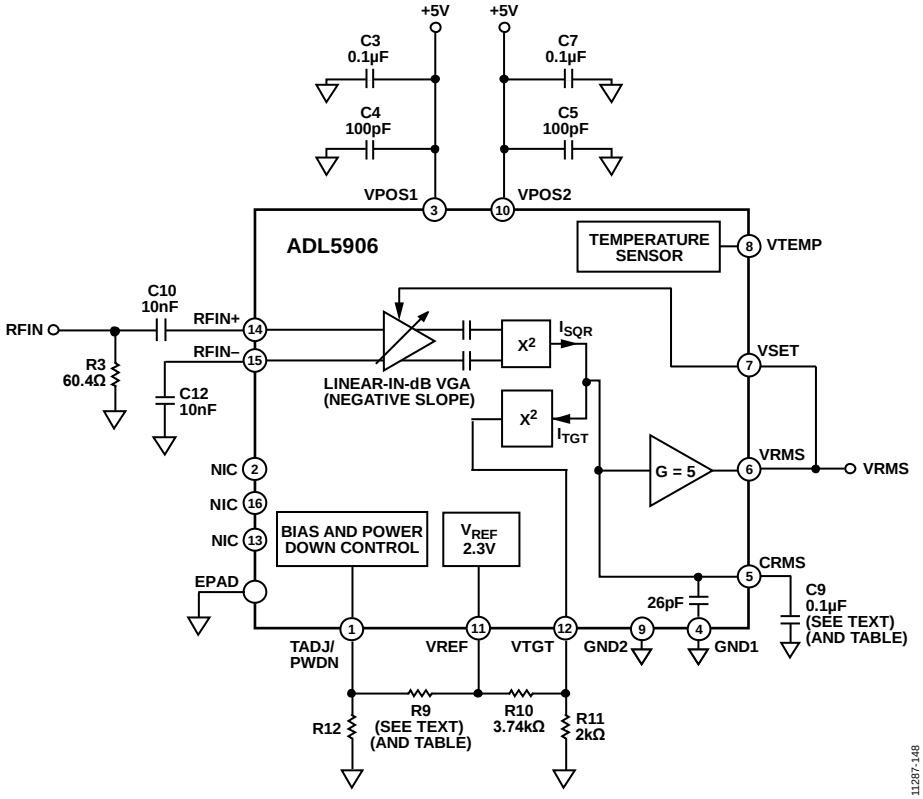

Figure 51. Basic Connections for Operation in Measurement Mode

Table 5. Recommended Minimum C_{RMS} Values for Various Modulation Schemes

Modulation/Standard	Peak Envelope Power Ratio (dB)	Carrier Bandwidth (MHz)	C_{RMSMIN} (nF)	Output Noise (mV p-p)	Rise/Fall Time (µs)
QPSK, 5 MSPS (SQR COS Filter, α = 0.35)	3.8	5	1	84	0.2/10
QPSK ,15 MSPS (SQR COS Filter, α = 0.35)	3.8	15	1	42	0.2/10
64 QAM, 1 MSPS (SQR COS Filter, α = 0.35)	7.4	1	10	265	3/85
64 QAM, 5 MSPS (SQR COS Filter, α = 0.35)	7.4	5	1	380	0.2/10
64 QAM, 13 MSPS (SQR COS Filter, α = 0.35)	7.4	13	1	205	0.2/10
W-CDMA, One-Carrier, TM1-64	10.56	3.84	1	820	0.2/10
W-CDMA Four-Carrier, TM1-64, TM1-32, TM1-16, TM1-8	12.08	18.84	1	640	0.2/10
LTE, TM1, One-Carrier, 20 MHz (2048 QPSK Subcarriers)	11.58	20	1	140	0.2/10

Table 5 shows the recommended minimum values of C_{RMS} for popular modulation schemes. Using lower capacitor values results in rms measurement errors. Output response time is also shown. If the output noise shown in Table 5 is unacceptably high, it can be reduced by

- Increasing C_{RMS}
- Implementing an averaging algorithm after the output voltage of the ADL5906 has been sampled by an analog-to-digital converter (ADC)

The values in Table 5 were experimentally determined to be the minimum capacitance that ensures good rms accuracy for that particular signal type. This test was carried out by starting out with a large capacitance value on the CRMS pin (for example, 10 µF). The value of V_{RMS} was noted for a fixed input power level (for example, −10 dBm). The value of C_{RMS} was then progressively reduced (this can be done with press-down capacitors) until the value of V_{RMS} started to deviate from its original value (this indicates that the accuracy of the rms computation is degrading and that C_{RMS} is becoming too small).

In general, the minimum required rms averaging capacitance increases as the peak-to-average ratio of the carrier increases. The minimum required C_{RMS} also tends to increase as the bandwidth of the carrier decreases. With narrow-band carriers, the noise spectrum of the V_{RMS} output tends to have a correspondingly narrow profile. The relatively narrow spectral profile demands a larger value of C_{RMS} that reduces the low-pass corner frequency of the averaging function and ensures a valid rms computation.

OUTPUT VOLTAGE SCALING

The linear output voltage range of the ADL5906 is nominally 0.3 V to 3.7 V. V_{RMS} is clamped to a maximum voltage of ~3.9 V; this helps improve falling edge settling speeds because the V_{RMS} output stays closer to the nominal linear-in-dB output range of 0.3 V to 3.7 V. Within the 0 V to 3.9 V maximum output range, the slope can be adjusted as needed via extra resistors, as shown in Figure 52.

If only a part of the RF input power range of the ADL5906 is being used (for example, −10 dBm to −60 dBm), increase the scaling so that this reduced input range fits into the available output swing (0 V to 3.9 V) of the ADL5906.

The output swing is reduced by simply adding a voltage divider on the output pin, as shown in the A side of Figure 52. Reducing the output scaling can be used when interfacing the ADL5906 to an ADC with a 0 V to 2.5 V input range.

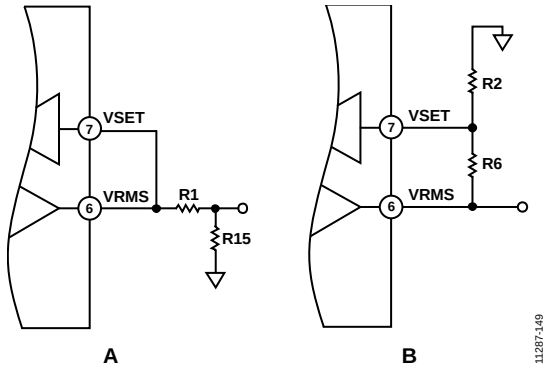

Figure 52. Decreasing and Increasing Slope

The output voltage swing can be increased using a technique that is analogous to setting the gain of an op amp in noninverting mode (see the B side of Figure 52) with the VSET pin being the equivalent of the inverting input of the op amp.

With VRMS connected to VSET, the nominal transfer function of the ADL5906 is given by

$$V_{RMS} = Slope \times (P_{IN} - Intercept)$$

For example at 3.5 GHz, with P_{IN} equal to 0 dBm, the nominal output voltage is equal to 0.052 V/dB × (0 dBm − (−64 dBm) = 3.328 V.

To scale this voltage downward using a resistor divider, choose a value for R15 and calculate R1 using the following equation:

$$R1 = R15 \times \left(\frac{V_{RMS}}{V_{RMS}'} - 1 \right) \quad (11)$$

To scale this voltage upward, choose a value for R2 and calculate R6 using the following equation:

$$R6 = (R2 \,||\, R_{IN})\left(\frac{V'_{RMS}}{V_{RMS}} - 1\right) \quad (12)$$

where:
R_{IN} is the input resistance of VSET (72 kΩ).
V'_{RMS} is the desired maximum output voltage.
V_{RMS} is the nominal maximum output voltage before scaling (see Figure 9 through Figure 26).

When choosing R1, R2, R6, and R15, notice the current drive capability of the VRMS pin and the input resistance of the VSET pin. The choice of resistors must not be too small because this results in excessive current drawn out of the VRMS pin (the VRMS pin can source a maximum current of 10 mA). However, choosing an R2 that is too large is also problematic. If the value of R2 chosen is compatible with the input resistance of the VSET pin (72 kΩ), this input resistance, which varies slightly from part to part, contributes to the resulting slope and output voltage. In general, ensure that the value of R2 is at least 10 times smaller than the input resistance of VSET. Therefore, the values for R6 and R2 must be in the 1 kΩ to 5 kΩ range. Similar values must be used for R1 and R15.

It is also important to take into account part-to-part and frequency variation in output swing along with the maximum output voltage (3.9 V) of the output stage of the ADL5906. The V_{RMS} part-to-part distribution is well characterized at major frequency bands in the Typical Performance Characteristics section (see Figure 12 through Figure 14, Figure 18 through Figure 20, Figure 24, and Figure 25). The resistor values in Table 6, which were calculated based on 3.5 GHz operation, have been conservatively chosen so that there is no chance that the desired output voltage swings exceed the output swing of the ADL5906 (when scaling upward) or the input range of a 0 V to 2.5 V ADC (when scaling downward). In each case, the nominal maximum voltage that results is 100 mV below the desired maximum to account for part-to-part variation and resistor tolerances.

Table 6. Output Voltage Range Scaling Examples at 3.5 GHz

	Slope Increase		Slope Decrease			
Desired Input Range (dBm)	R6 (Ω)	R2 (Ω)	R1 (Ω)	R15(Ω)	New Slope (mV/dB)	Nominal Maximum Output Voltage (V)
0 to −60	274	2000			59	3.8
−10 to −50	681	2000			70	3.8
0 to −60			787	2000	37	2.4
−10 to −50			348	2000	44	2.4

SYSTEM CALIBRATION AND ERROR CALCULATION

The measured transfer function of the ADL5906 at 2.14 GHz is shown in Figure 53, which contains plots of both output voltage vs. input level and linearity error vs. input level. As the input level varies from −65 dBm to +5 dBm, the output voltage varies from ~0.25 V to ~3.9 V.

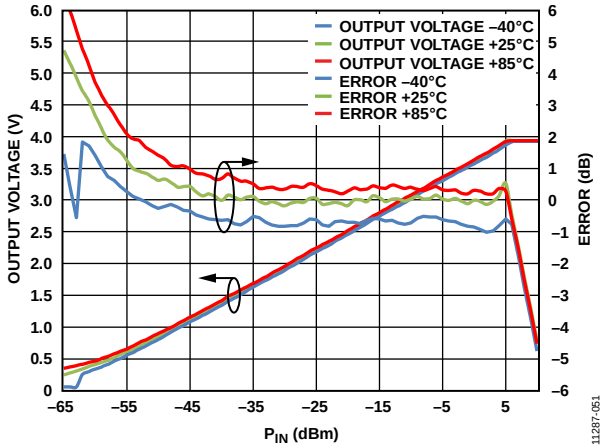

Figure 53. 2.14 GHz V_{RMS} and Log Conformance Error at +25°C, −40°C, and +85°C Using Two-Point Calibration at 0 dBm and −40 dBm

Because slope and intercept vary from device to device, board level calibration must be performed to achieve high accuracy. The equation for the idealized output voltage can be written as

$$V_{RMS(IDEAL)} = Slope \times (P_{IN} - Intercept) \quad (13)$$

where:
Slope is the change in output voltage divided by the change in input power (dB).
Intercept is the calculated input power level at which the output voltage is equal to 0 V (note that *Intercept* is an extrapolated theoretical value and not a measured value).

In general, calibration is performed during equipment manufacture by applying two or more known signal levels to the input of the ADL5906 and measuring the corresponding output voltages. The calibration points must be within the linear operating range of the device.

With a two-point calibration, the slope and intercept are calculated as follows:

$$Slope = (V_{RMS1} - V_{RMS2})/(P_{IN1} - P_{IN2}) \quad (14)$$

$$Intercept = P_{IN1} - (V_{RMS1}/Slope) \quad (15)$$

After the slope and intercept are calculated and stored in nonvolatile memory during equipment calibration, an equation can be used to calculate an unknown input power based on the output voltage of the detector.

$$P_{IN}\,(Unknown) = (V_{RMS(MEASURED)}/Slope) + Intercept \quad (16)$$

The log conformance error is the difference between this straight line and the actual performance of the detector.

$$Error\ (dB) = (V_{RMS(MEASURED)} - V_{RMS(IDEAL)})/Slope \quad (17)$$

Figure 53 includes a plot of this error at +25°C, −40°C, and +85°C when using a two-point calibration (calibration points are 0 dBm and −40 dBm). The error at the calibration points at 25°C (in this case, −40 dBm and 0 dBm) is equal to 0 dB by definition.

The residual nonlinearity of the transfer function that is apparent in the two-point calibration error plot can be reduced by increasing the number of calibration points. Figure 54 shows the post-calibration error plots for a three-point calibration. With a multipoint calibration, the transfer function is segmented, with each segment having its own slope and intercept. Multiple known power levels (three levels in this case) are applied, and multiple voltages are measured. When the equipment is in operation, the measured voltage from the detector is first used to determine which of the stored slope and intercept calibration coefficients are to be used. Then, the unknown power level is calculated by inserting the appropriate slope and intercept values into Equation 16.

When choosing calibration points, there is no requirement for, or value in, equal spacing between the points. There is also no limit to the number of calibration points used. However, when more calibration points are used, calibration time increases.

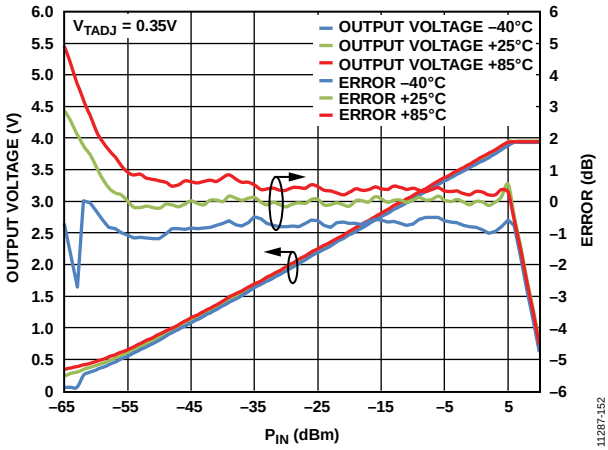

Figure 54. 2.14 GHz V_{RMS} and Log Conformance Error at +25°C, −40°C, and +85°C Using Three-Point Calibration at 0 dBm, −40 dBm, and −55 dBm

The −40°C and +85°C error plots in Figure 54 are generated using the +25°C slope and intercept values. This is consistent with equipment calibration in a mass production environment where calibration of multiple temperatures is not practical.

USING V_{TEMP} TO IMPROVE INTERCEPT TEMPERATURE DRIFT

In applications where V_{TEMP} and V_{RMS} are both being digitized by an ADC, the V_{TEMP} voltage can be used to further improve the temperature drift of the ADL5906.

As shown in Figure 54, whereas the slope is stable vs. the temperature at 2140 MHz, the intercept of the ADL5906 does vary slightly vs. temperature (approximately +0.3 dB at +85°C and −0.8 dB at −40°C). This variation in intercept is constant vs. input power level at most frequencies. Table 7 lists the average temperature coefficient of V_{RMS} in mV/°C at frequencies from 100 MHz to 5.8 GHz. This temperature coefficient is given by the following equation:

$$TC_{VRMS} = (DRIFT_{VRMS}/\Delta_{TEMP}) \times Slope \quad (18)$$

where:
$DRIFT_{VRMS}$ is the specified drift of V_{RMS} (scaled in dB) from ambient to either −40°C or +85°C at an input power level of 0 dBm (see Table 1).
Δ_{TEMP} is equal to either +65°C for cold drift (that is, +25°C − (−40°C)) or +60°C for hot drift (that is, +85°C − +25°C).
Slope is the specified slope of V_{RMS} (see Table 1).

For example, at 2.14 GHz, TC_{VRMS} for hot drift can be calculated as

$$TC_{VRMS} = (0.3 \text{ dB}/60°C) \times 56 \text{ mV/dB} = 0.28 \text{ mV}/°C$$

The value for slope that is used can also be the slope that is calculated during device calibration. This gives results that are slightly more accurate because there is slight variation in slope from device to device.

Table 7 also lists the typical temperature coefficient of the V_{TEMP} temperature sensor output. To calculate the appropriate amount of compensation required at a particular frequency, a V_{TEMP} weighting factor is calculated. This is simply the ratio of the temperature coefficients of VTEMP and VRMS. These weighting factors are also shown in Table 7.

Using the data shown in Table 7, an adjusted value for V_{RMS} (V_{RMS}′) can be calculated using the following equation:

$$V_{RMS}' = V_{RMS} - \left(\frac{V_{TEMP} - V_{TEMP25}}{Weighting\ Factor} \right) \quad (19)$$

where:
V_{TEMP25} is equal to the voltage measured on V_{TEMP} during system calibration at ambient temperature.
V_{TEMP} is equal to the voltage on V_{TEMP} during normal operation.

Figure 55 to Figure 62 show typical plots of V_{RMS}′ vs. input level and temperature at frequencies from 100 MHz to 5.8 GHz when this temperature compensation algorithm is applied.

From a system calibration and operation perspective, the only additional measurements that are required to implement this algorithm are measurement and storage of V_{TEMP} during calibration (that is, at ambient temperature) and measurement of V_{TEMP} during operation. All other information required to implement this algorithm (that is, nominal temperature drift of V_{RMS} and temperature coefficient of V_{TEMP}) is based on typical data sheet specifications.

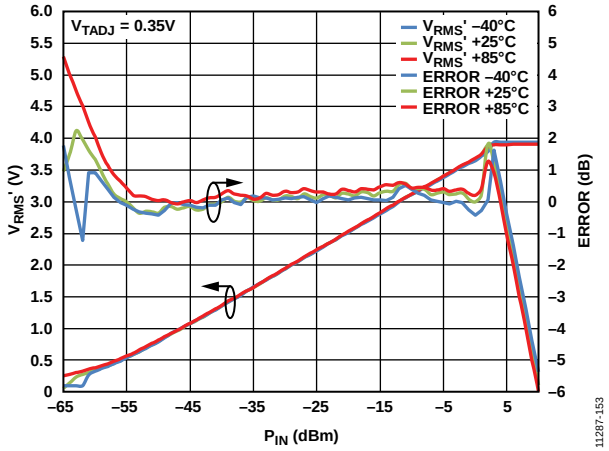

Figure 55. V_{RMS}′ and Log Conformance Error vs. Input Level and Temperature at 100 MHz Using V_{TEMP} Intercept Compensation

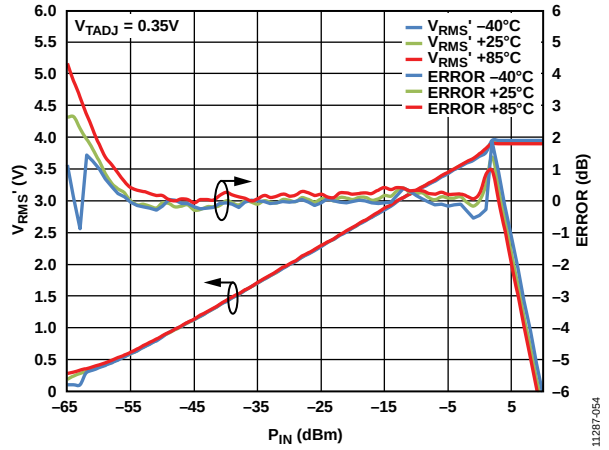

Figure 56. V_{RMS}′ and Log Conformance Error vs. Input Level and Temperature at 700 MHz Using V_{TEMP} Intercept Compensation

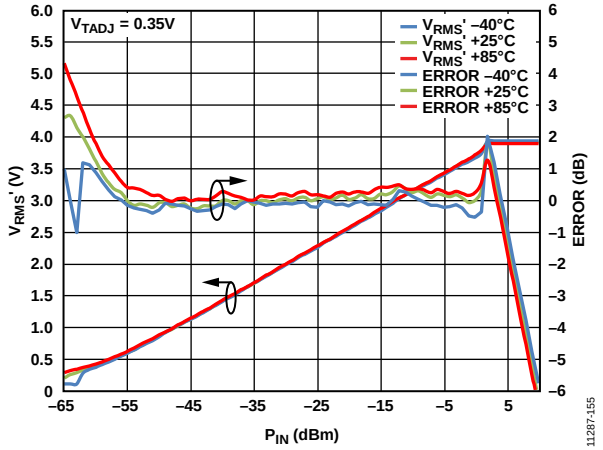

Figure 57. V_{RMS}' and Log Conformance Error vs. Input Level and Temperature at 900 MHz Using V_{TEMP} Intercept Compensation

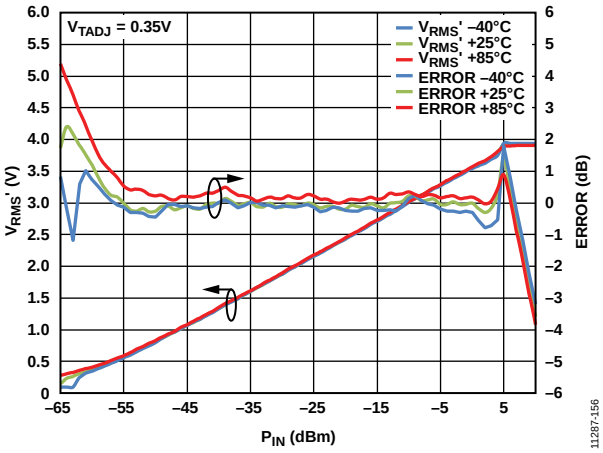

Figure 58. V_{RMS}' and Log Conformance Error vs. Input Level and Temperature at 1900 MHz Using V_{TEMP} Intercept Compensation

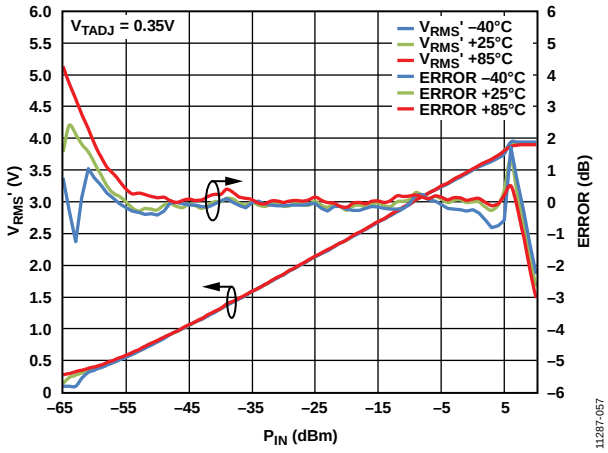

Figure 59. V_{RMS}' and Log Conformance Error vs. Input Level and Temperature at 2140 MHz using V_{TEMP} Intercept Compensation

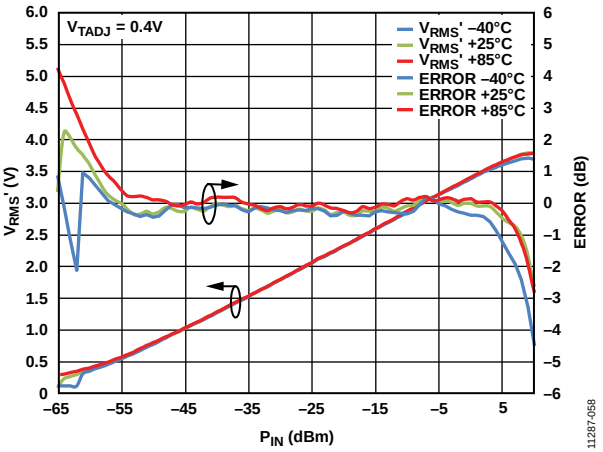

Figure 60. V_{RMS}' and Log Conformance Error vs. Input Level and Temperature at 2600 MHz Using V_{TEMP} Intercept Compensation

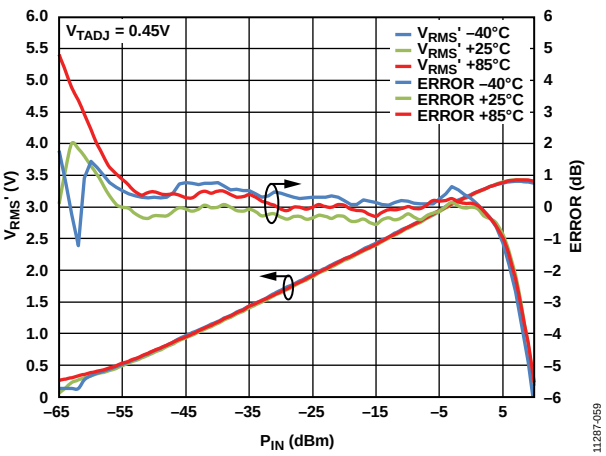

Figure 61. V_{RMS}' and Log Conformance Error vs. Input Level and Temperature at 3500 MHz Using V_{TEMP} Intercept Compensation

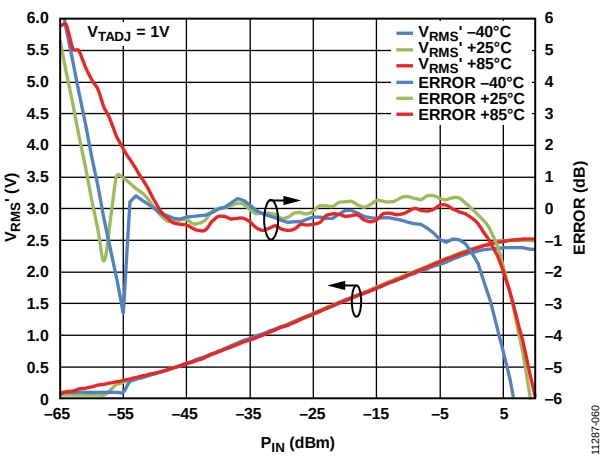

Figure 62. V_{RMS}' and Log Conformance Error vs. Input Level and Temperature at 5800 MHz Using V_{TEMP} Intercept Compensation

Table 7. Scaling Factors for Intercept Temperature Drift Compensation Using V_{TEMP}

Frequency (MHz)	TC_{VRMS}, −40°C to +25°C, P_{IN} = 0 dBm (mV/°C)	TC_{VRMS}, 25°C to 85°C, P_{IN} = 0 dBm (mV/°C)	TC_{VTEMP} (mV/°C)	V_{TEMP} Weighting Factor, −40°C to +25°C (TC_{VTEMP}/TC_{VRMS})	V_{TEMP} Weighting Factor, +25°C to +85°C (TC_{VTEMP}/TC_{VRMS})
100	0.72615	0.19667	4.8	6.61017	24.40678
700	0.81692	0.295	4.8	5.87571	16.27119
900	0.72615	0.295	4.8	6.61017	16.27119
1900	0.70154	0.19	4.8	6.84211	25.26316
2140	0.68923	0.28	4.8	6.96429	17.14286
2600	0.76154	0.275	4.8	6.30303	17.45455
3500	1.2	0	4.8	4	∞
5800	1.2393[1]	0.0804[1]	4.8	5.99417	85.287

[1] TC_{VRMS} based on temperature drift at P_{IN} = −10 dBm.

DESCRIPTION OF CHARACTERIZATION

For a description on how characterization was completed, see the ADL5902 data sheet.

EVALUATION BOARD

The ADL5906-EVALZ is a fully populated, 4-layer, FR4-based evaluation board. For normal operation, it requires a 5 V/100 mA power supply. The 5 V power supply must be connected to the VPOS and GND test loops. The RF input signal is applied to the SMA connector (RFIN). The output voltage is available on the SMA connector (VOUT1) or on the test loop (VOUT). Configuration options for the evaluation board are listed in Table 8.

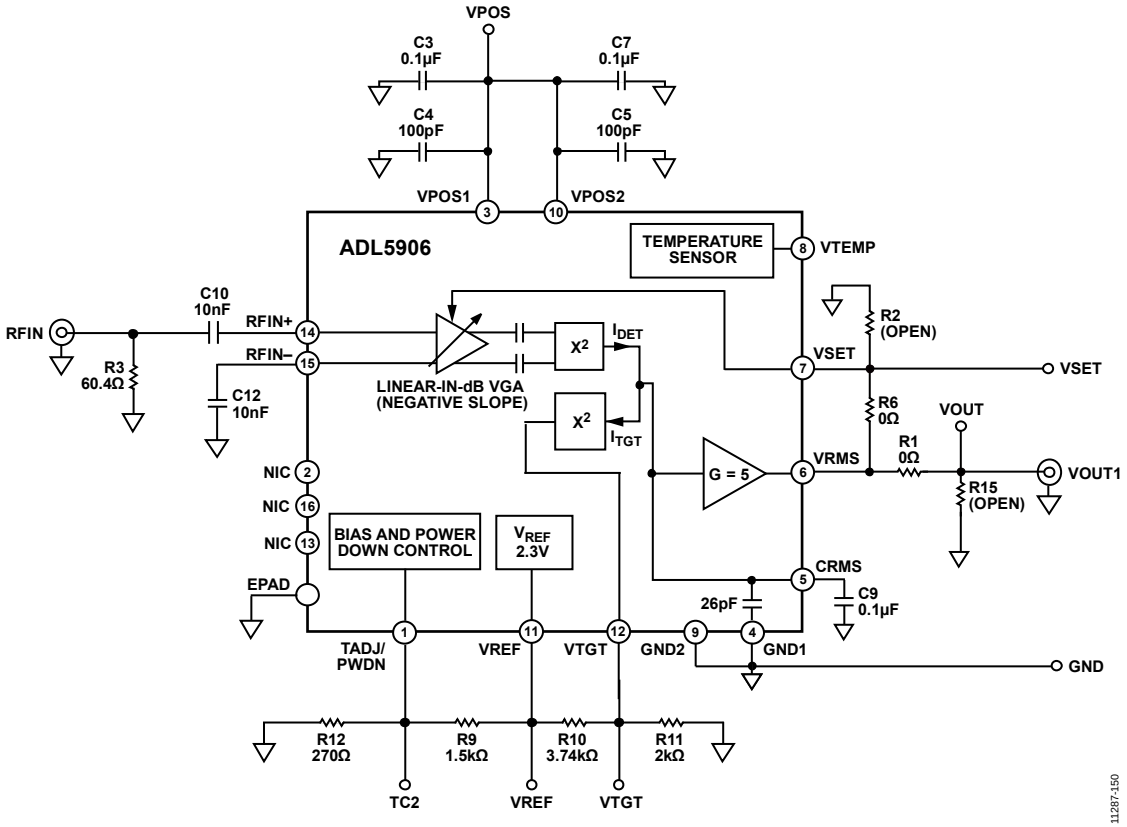

Figure 63. Evaluation Board Schematic

Table 8. Evaluation Board Configuration Options

Component	Function/Notes	Default Value
RFIN, R3, C10, C12	RF input. The evaluation board is configured for single-ended drive on the RFIN+ pin (Pin 14). Capacitors C10 and C12 have been set large enough so that the full frequency range of the device is covered. If operation down to 10 MHz is not required, the value of these capacitors can be reduced.	RFIN = SMA connector, C10 = C12 = 10 nF, R3 = 60.4 Ω
VTGT, R10, R11	VTGT interface. R10 and R11 are set up to provide 0.8 V to VTGT derived from VREF. If R10 and R11 are removed, an external voltage can be applied on the VTGT test point.	VTGT = black test loop, R10 = 3.74 kΩ, R11 = 2 kΩ, VTGT = 0.8 V
VPOS, GND, C3, C4, C5,C7	Power supply interface and decoupling. Apply the power supply for the evaluation board to the VPOS and GND test loops. The nominal supply decoupling consists of a 100 pF capacitor and a 0.1 µF capacitor on each power supply pin, with the 100 pF capacitor placed closer to the pin.	VPOS = red test loop, GND = black test loop, C3 = C7 = 0.1 µF, C4 = C5 = 100 pF

Component	Function/Notes	Default Value
VOUT, VOUT1, VSET, R1, R2, R6, R15	Output interface. In measurement mode, a portion of the voltage at the VRMS pin is fed back to the VSET pin via R6 (R6 is normally set to 0 Ω). Using the voltage divider created by R2 and R6, the magnitude of the slope of V_{RMS} is increased by reducing the portion of VRMS that is fed back to VSET. Resistors R1 and R15 can be used to reduce the output slope. In controller mode, R6 must be open. In this mode, the ADL5906 can control the gain of a variable gain amplifier (VGA) or voltage variable attenuator (VVA). A setpoint voltage is applied to the VSET test loop, and the VRMS test loop or SMA connector drives the gain control input of the VGA/VVA.	VOUT = black test loop, VOUT1 = SMA connector, VSET = black test loop, R1 = R6 = 0 Ω, R15 = R2 = open
C9	RMS averaging capacitor. The value of the rms averaging capacitor should be set based on the peak-to-average ratio of the input signal and based on the desired output response time and residual output noise.	C9 = 0.1 µF
TC2, R9, R12	TADJ/PWDN interface. The TADJ/PWDN pin controls the slope temperature compensation and/or shuts down the device. The evaluation board is configured with VTADJ connected to VREF through a resistor divider (R9, R12). This voltage divider can be removed (or simply overdriven) allowing for the external application of a voltage to the VTADJ pin by applying a voltage to the TC2 test point.	TC2 = black test loop, R9 = 1.5 kΩ, R12 = 270 Ω, VTADJ = 0.35 V

EVALUATION BOARD ASSEMBLY DRAWINGS

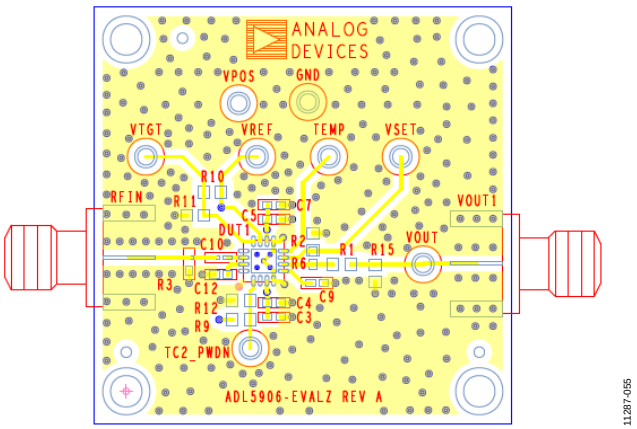

Figure 64. ADL5906 Evaluation Board Layout, Top Side

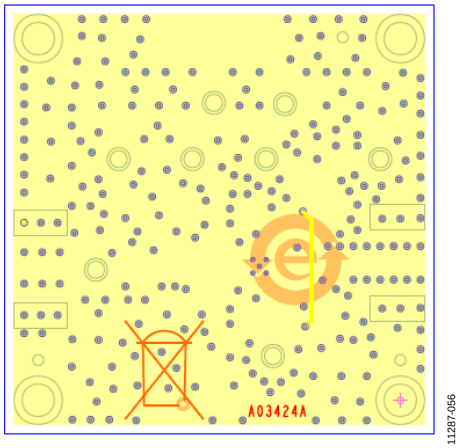

Figure 65. ADL5906 Evaluation Board Layout, Bottom Side

OUTLINE DIMENSIONS

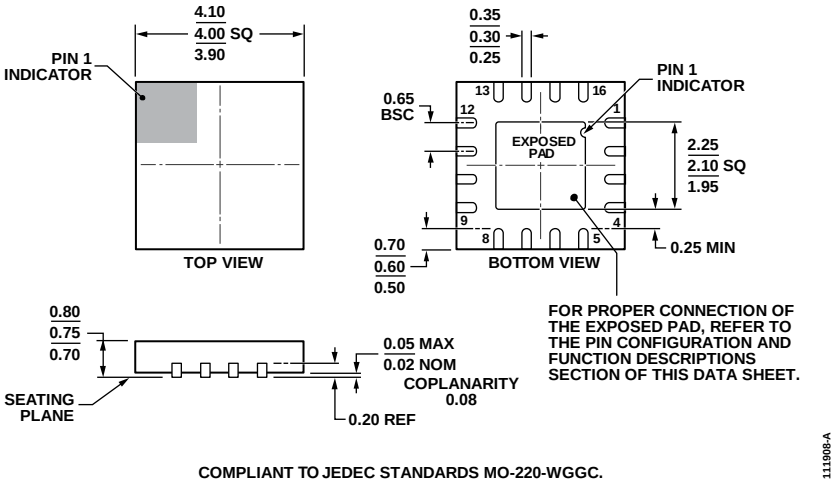

Figure 66. 16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
4 mm × 4 mm Body, Very Very Thin Quad
(CP-16-23)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Ordering Quantity
ADL5906ACPZN-R2	−40°C to +105°C	16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-16-23	250
ADL5906ACPZN-R7	−40°C to +105°C	16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-16-23	1,500
ADL5906SCPZN-R7	−55°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-16-23	1,500
ADL5906-EVALZ		Evaluation Board		

[1] Z = RoHS Compliant Part.

NOTES

NOTES

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D11287-0-10/13(A)

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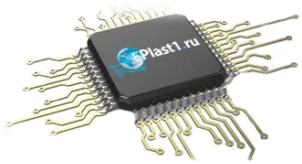
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

Телефон: 8 (812) 309 58 32 (многоканальный)
Факс: 8 (812) 320-02-42
Электронная почта: org@eplast1.ru
Адрес: 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.