

## TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS

### 262,144-WORD BY 16-BIT CMOS STATIC RAM

#### DESCRIPTION

The TC55VZM216AJJN/AFTN is a 4,194,304-bit high-speed static random access memory (SRAM) organized as 262,144 words by 16 bits. Fabricated using CMOS technology and advanced circuit techniques to provide high speed, it operates from a single 3.3 V power supply. Chip enable ( $\overline{CE}$ ) can be used to place the device in a low-power mode, and output enable ( $\overline{OE}$ ) provides fast memory access. Data byte control signals ( $\overline{LB}$ ,  $\overline{UB}$ ) provide lower and upper byte access. This device is well suited to cache memory applications where high-speed access and high-speed storage are required. All inputs and outputs are directly LVTTL compatible. The TC55VZM216AJJN/AFTN is available in plastic 44-pin SOJ and TSOP with 400mil width for high density surface assembly.

#### FEATURES

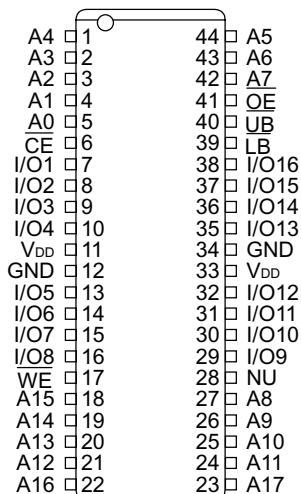
- Fast access time (the following are maximum values)
  - TC55VZM216AJJN/AFTN08:8 ns
  - TC55VZM216AJJN/AFTN10:10 ns
  - TC55VZM216AJJN/AFTN12:12 ns
- Low-power dissipation ( $I_{DD02}$ ) (the following are maximum values)
 

| Cycle Time      | 8   | 10  | 12  | ns |
|-----------------|-----|-----|-----|----|
| Operation (max) | 140 | 130 | 120 | mA |
- Single power supply voltage of 3.3 V  $\pm$  0.3 V
- Fully static operation
- All inputs and outputs are LVTTL compatible
- Output buffer control using  $\overline{OE}$
- Data byte control using  $\overline{LB}$  (I/O1 to I/O8) and  $\overline{UB}$  (I/O9 to I/O16)
- Package:
  - SOJ44-P-400-1.27 (AJJN) (Weight: 1.64 g typ)
  - TSOP II44-P-400-0.80 (AFTN) (Weight: 0.45 g typ)

Standby:4 mA (both devices)

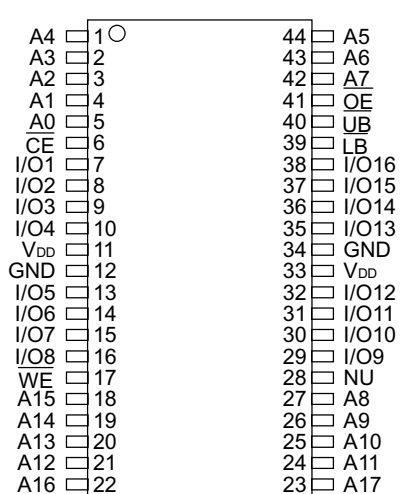
#### PIN ASSIGNMENT (TOP VIEW)

##### 44 PIN SOJ



(TC55VZM216AJJN)

##### 44 PIN TSOP

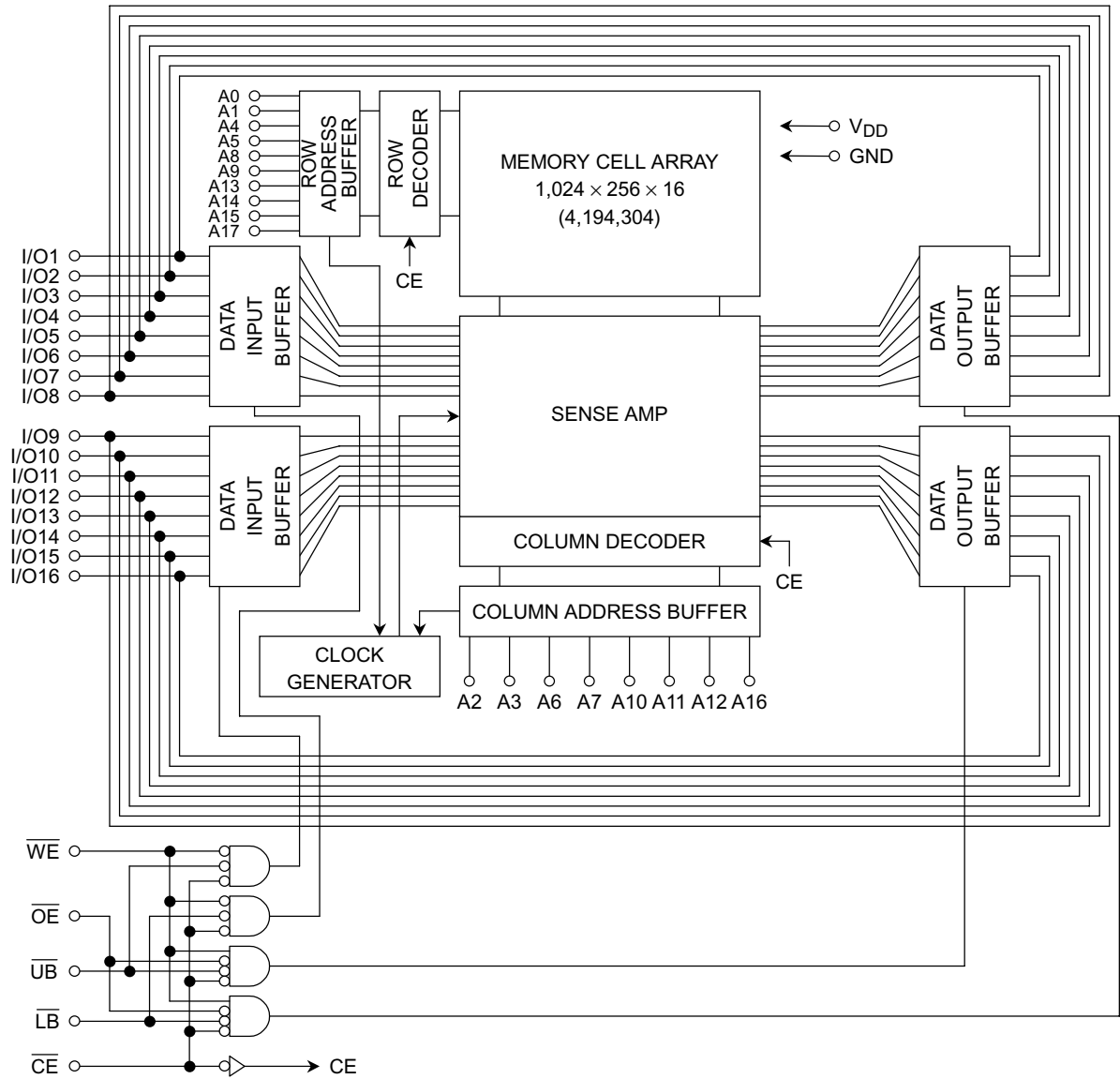


(TC55VZM216AFTN)

#### PIN NAMES

|                                   |                          |
|-----------------------------------|--------------------------|
| A0 to A17                         | Address Inputs           |
| I/O1 to I/O16                     | Data Inputs/Outputs      |
| $\overline{CE}$                   | Chip Enable Input        |
| $\overline{WE}$                   | Write Enable Input       |
| $\overline{OE}$                   | Output Enable Input      |
| $\overline{LB}$ , $\overline{UB}$ | Data Byte Control Inputs |
| $V_{DD}$                          | Power (+3.3 V)           |
| GND                               | Ground                   |
| NU                                | Not Usable (Input)       |

**BLOCK DIAGRAM**



**MAXIMUM RATINGS**

| SYMBOL              | RATING                        | VALUE                            | UNIT |
|---------------------|-------------------------------|----------------------------------|------|
| V <sub>DD</sub>     | Power Supply Voltage          | -0.5 to 4.6                      | V    |
| V <sub>IN</sub>     | Input Terminal Voltage        | -0.5* to 4.6                     | V    |
| V <sub>I/O</sub>    | Input/Output Terminal Voltage | -0.5* to V <sub>DD</sub> + 0.5** | V    |
| P <sub>D</sub>      | Power Dissipation             | 1.4                              | W    |
| T <sub>solder</sub> | Soldering Temperature (10s)   | 260                              | °C   |
| T <sub>stg</sub>    | Storage Temperature           | -65 to 150                       | °C   |
| T <sub>opr</sub>    | Operating Temperature         | -10 to 85                        | °C   |

\*: -1.5 V with a pulse width of 20% of t<sub>RC</sub> min (4 ns max)

\*\*: V<sub>DD</sub> + 1.5 V with a pulse width of 20% of t<sub>RC</sub> min (4 ns max)

## DC RECOMMENDED OPERATING CONDITIONS (Ta = 0° to 70°C)

| SYMBOL          | PARAMETER            | MIN   | TYP | MAX                     | UNIT |
|-----------------|----------------------|-------|-----|-------------------------|------|
| V <sub>DD</sub> | Power Supply Voltage | 3.0   | 3.3 | 3.6                     | V    |
| V <sub>IH</sub> | Input High Voltage   | 2.0   | —   | V <sub>DD</sub> + 0.3** | V    |
| V <sub>IL</sub> | Input Low Voltage    | -0.3* | —   | 0.8                     | V    |

\*: -1.0 V with a pulse width of 20% of t<sub>RC</sub> min (4 ns max)

\*\*: V<sub>DD</sub> + 1.0 V with a pulse width of 20% of t<sub>RC</sub> min (4 ns max)

## DC CHARACTERISTICS (Ta = 0° to 70°C, V<sub>DD</sub> = 3.3 V ± 0.3 V)

| SYMBOL              | PARAMETER                                | TEST CONDITION                                                                                                                        |                            | MIN                   | TYP | MAX | UNIT |
|---------------------|------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------|----------------------------|-----------------------|-----|-----|------|
| I <sub>IL</sub>     | Input Leakage Current<br>(Except NU pin) | V <sub>IN</sub> = 0 to V <sub>DD</sub>                                                                                                |                            | −1                    | —   | 1   | μA   |
| I <sub>LO</sub>     | Output Leakage<br>Current                | $\overline{CE} = V_{IH}$ or $\overline{WE} = V_{IL}$ or $\overline{OE} = V_{IH}$ ,<br>V <sub>OUT</sub> = 0 to V <sub>DD</sub>         |                            | −1                    | —   | 1   | μA   |
| I <sub>I</sub> (NU) | Input Leakage Current<br>(NU pin)        | V <sub>IN</sub> = 0 V                                                                                                                 |                            | −1                    | —   | 1   | μA   |
| V <sub>OH</sub>     | Output High Voltage                      | I <sub>OH</sub> = −2 mA                                                                                                               |                            | 2.4                   | —   | —   | V    |
|                     |                                          | I <sub>OH</sub> = −100 μA                                                                                                             |                            | V <sub>DD</sub> − 0.2 | —   | —   |      |
| V <sub>OL</sub>     | Output Low Voltage                       | I <sub>OL</sub> = 2 mA                                                                                                                |                            | —                     | —   | 0.4 |      |
|                     |                                          | I <sub>OL</sub> = 100 μA                                                                                                              |                            | —                     | —   | 0.2 |      |
| I <sub>DDO1</sub>   | Operating Current                        | $\overline{CE} = V_{IL}$ , I <sub>OUT</sub> = 0 mA,<br>$\overline{OE} = V_{IH}$ ,<br>Other Input = V <sub>IH</sub> /V <sub>IL</sub>   | t <sub>cycle</sub> = 8 ns  | —                     | —   | 170 | mA   |
|                     |                                          |                                                                                                                                       | t <sub>cycle</sub> = 10 ns | —                     | —   | 160 |      |
|                     |                                          |                                                                                                                                       | t <sub>cycle</sub> = 12 ns | —                     | —   | 150 |      |
| I <sub>DDO2</sub>   |                                          | $\overline{CE} = 0.2$ V, I <sub>OUT</sub> = 0 mA,<br>$\overline{OE} = V_{DD} - 0.2$ V,<br>Other Input = V <sub>DD</sub> − 0.2 V/0.2 V | t <sub>cycle</sub> = 8 ns  | —                     | —   | 140 |      |
|                     |                                          |                                                                                                                                       | t <sub>cycle</sub> = 10 ns | —                     | —   | 130 |      |
|                     |                                          |                                                                                                                                       | t <sub>cycle</sub> = 12 ns | —                     | —   | 120 |      |
| I <sub>DDS1</sub>   | Standby Current                          | $\overline{CE} = V_{IH}$ , Other Input = V <sub>IH</sub> or V <sub>IL</sub>                                                           |                            | —                     | —   | 55  | mA   |
| I <sub>DDS2</sub>   |                                          | $\overline{CE} = V_{DD} - 0.2$ V, Other Input = V <sub>DD</sub> − 0.2 V or 0.2 V                                                      |                            | —                     | —   | 4   |      |

## CAPACITANCE (Ta = 25°C, f = 1.0 MHz)

| SYMBOL           | PARAMETER                | TEST CONDITION         | MAX | UNIT |
|------------------|--------------------------|------------------------|-----|------|
| C <sub>IN</sub>  | Input Capacitance        | V <sub>IN</sub> = GND  | 6   | pF   |
| C <sub>I/O</sub> | Input/Output Capacitance | V <sub>I/O</sub> = GND | 8   | pF   |

Note: This parameter is periodically sampled and is not 100% tested.

**OPERATING MODE**

| MODE            | $\overline{\text{CE}}$ | $\overline{\text{OE}}$ | $\overline{\text{WE}}$ | $\overline{\text{LB}}$ | $\overline{\text{UB}}$ | I/O1 to I/O8   | I/O9 to I/O16  | POWER            |
|-----------------|------------------------|------------------------|------------------------|------------------------|------------------------|----------------|----------------|------------------|
| Read            | L                      | L                      | H                      | L                      | L                      | Output         | Output         | $I_{\text{DDO}}$ |
|                 |                        |                        |                        | H                      | L                      | High Impedance | Output         | $I_{\text{DDO}}$ |
|                 |                        |                        |                        | L                      | H                      | Output         | High Impedance | $I_{\text{DDO}}$ |
| Write           | L                      | *                      | L                      | L                      | L                      | Input          | Input          | $I_{\text{DDO}}$ |
|                 |                        |                        |                        | H                      | L                      | High Impedance | Input          | $I_{\text{DDO}}$ |
|                 |                        |                        |                        | L                      | H                      | Input          | High Impedance | $I_{\text{DDO}}$ |
| Outputs Disable | L                      | H                      | H                      | *                      | *                      | High Impedance | High Impedance | $I_{\text{DDO}}$ |
|                 | L                      | *                      | *                      | H                      | H                      |                |                |                  |
| Standby         | H                      | *                      | *                      | *                      | *                      | High Impedance | High Impedance | $I_{\text{DDS}}$ |

\* : Don't care

Note: The NU pin must be left unconnected or tied to GND.  
 You must not apply a voltage of more than 0.8 V to the NU.

## AC CHARACTERISTICS (Ta = 0° to 70°C (See Note 1), VDD = 3.3 V ± 0.3 V)

### READ CYCLE

| SYMBOL           | PARAMETER                                       | TC55VZM216AJJN/AFTN |     |     |     |     |     | UNIT |
|------------------|-------------------------------------------------|---------------------|-----|-----|-----|-----|-----|------|
|                  |                                                 | 08                  |     | 10  |     | 12  |     |      |
|                  |                                                 | MIN                 | MAX | MIN | MAX | MIN | MAX |      |
| t <sub>RC</sub>  | Read Cycle Time                                 | 8                   | —   | 10  | —   | 12  | —   | ns   |
| t <sub>ACC</sub> | Address Access Time                             | —                   | 8   | —   | 10  | —   | 12  |      |
| t <sub>CO</sub>  | Chip Enable Access Time                         | —                   | 8   | —   | 10  | —   | 12  |      |
| t <sub>OE</sub>  | Output Enable Access Time                       | —                   | 4   | —   | 5   | —   | 6   |      |
| t <sub>BA</sub>  | Upper Byte, Lower Byte Access Time              | —                   | 4   | —   | 5   | —   | 6   |      |
| t <sub>OH</sub>  | Output Data Hold Time from Address Change       | 3                   | —   | 3   | —   | 3   | —   |      |
| t <sub>COE</sub> | Output Enable Time from Chip Enable             | 3                   | —   | 3   | —   | 3   | —   |      |
| t <sub>OEE</sub> | Output Enable Time from Output Enable           | 0                   | —   | 0   | —   | 0   | —   |      |
| t <sub>BE</sub>  | Output Enable Time from Upper Byte, Lower Byte  | 0                   | —   | 0   | —   | 0   | —   |      |
| t <sub>COD</sub> | Output Disable Time from Chip Enable            | —                   | 4   | —   | 5   | —   | 6   |      |
| t <sub>ODO</sub> | Output Disable Time from Output Enable          | —                   | 4   | —   | 5   | —   | 6   |      |
| t <sub>BD</sub>  | Output Disable Time from Upper Byte, Lower Byte | —                   | 4   | —   | 5   | —   | 6   |      |

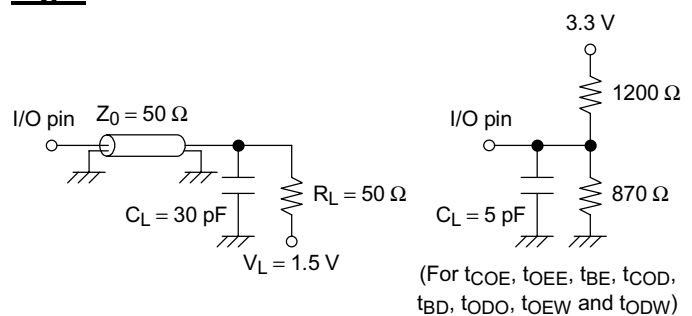
### WRITE CYCLE

| SYMBOL           | PARAMETER                                     | TC55VZM216AJJN/AFTN |     |     |     |     |     | UNIT |
|------------------|-----------------------------------------------|---------------------|-----|-----|-----|-----|-----|------|
|                  |                                               | 08                  |     | 10  |     | 12  |     |      |
|                  |                                               | MIN                 | MAX | MIN | MAX | MIN | MAX |      |
| t <sub>WC</sub>  | Write Cycle Time                              | 8                   | —   | 10  | —   | 12  | —   | ns   |
| t <sub>WP</sub>  | Write Pulse Width                             | 6                   | —   | 7   | —   | 8   | —   |      |
| t <sub>CW</sub>  | Chip Enable to End of Write                   | 6                   | —   | 7   | —   | 8   | —   |      |
| t <sub>BW</sub>  | Upper Byte, Lower Byte Enable to End of Write | 6                   | —   | 7   | —   | 8   | —   |      |
| t <sub>AW</sub>  | Address Valid to End of Write                 | 6                   | —   | 7   | —   | 8   | —   |      |
| t <sub>AS</sub>  | Address Setup Time                            | 0                   | —   | 0   | —   | 0   | —   |      |
| t <sub>WR</sub>  | Write Recovery Time                           | 0                   | —   | 0   | —   | 0   | —   |      |
| t <sub>DS</sub>  | Data Setup Time                               | 4                   | —   | 5   | —   | 6   | —   |      |
| t <sub>DH</sub>  | Data Hold Time                                | 0                   | —   | 0   | —   | 0   | —   |      |
| t <sub>OEW</sub> | Output Enable Time from Write Enable          | 3                   | —   | 3   | —   | 3   | —   |      |
| t <sub>ODW</sub> | Output Disable Time from Write Enable         | —                   | 4   | —   | 5   | —   | 6   |      |

## AC TEST CONDITIONS

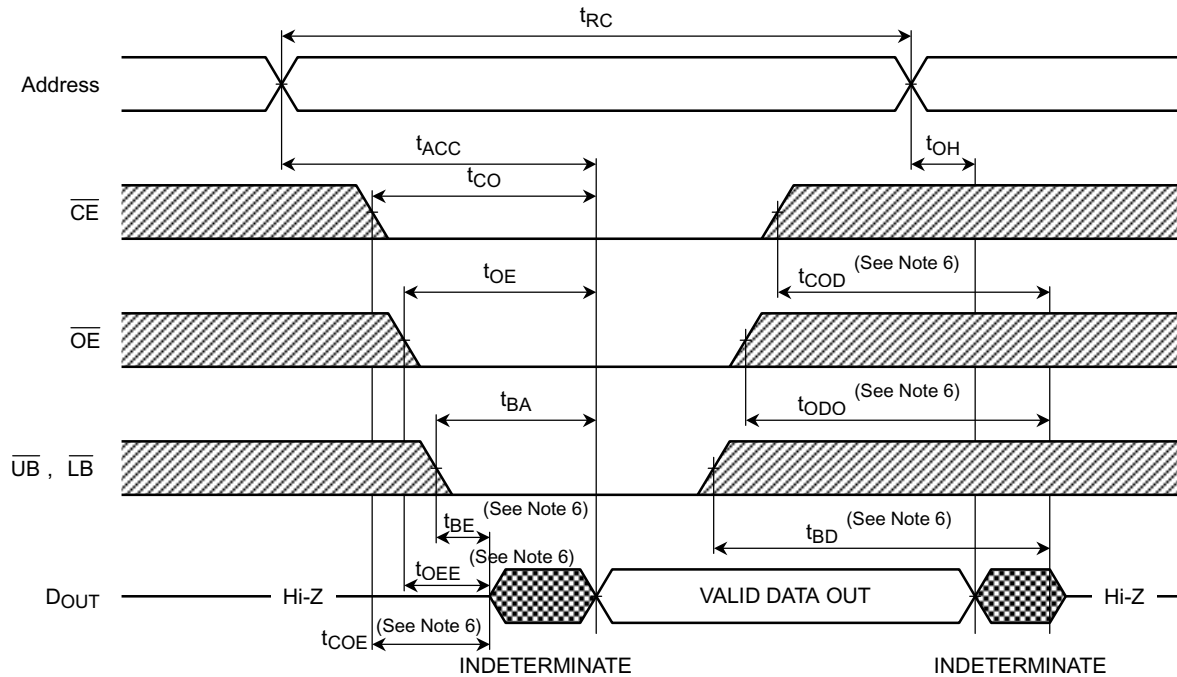
| PARAMETER                                 | TEST CONDITION |
|-------------------------------------------|----------------|
| Input Pulse Level                         | 3.0 V/ 0.0 V   |
| Input Pulse Rise and Fall Time            | 2 ns           |
| Input Timing Measurement Reference Level  | 1.5 V          |
| Output Timing Measurement Reference Level | 1.5 V          |
| Output Load                               | Fig.1          |

Fig.1

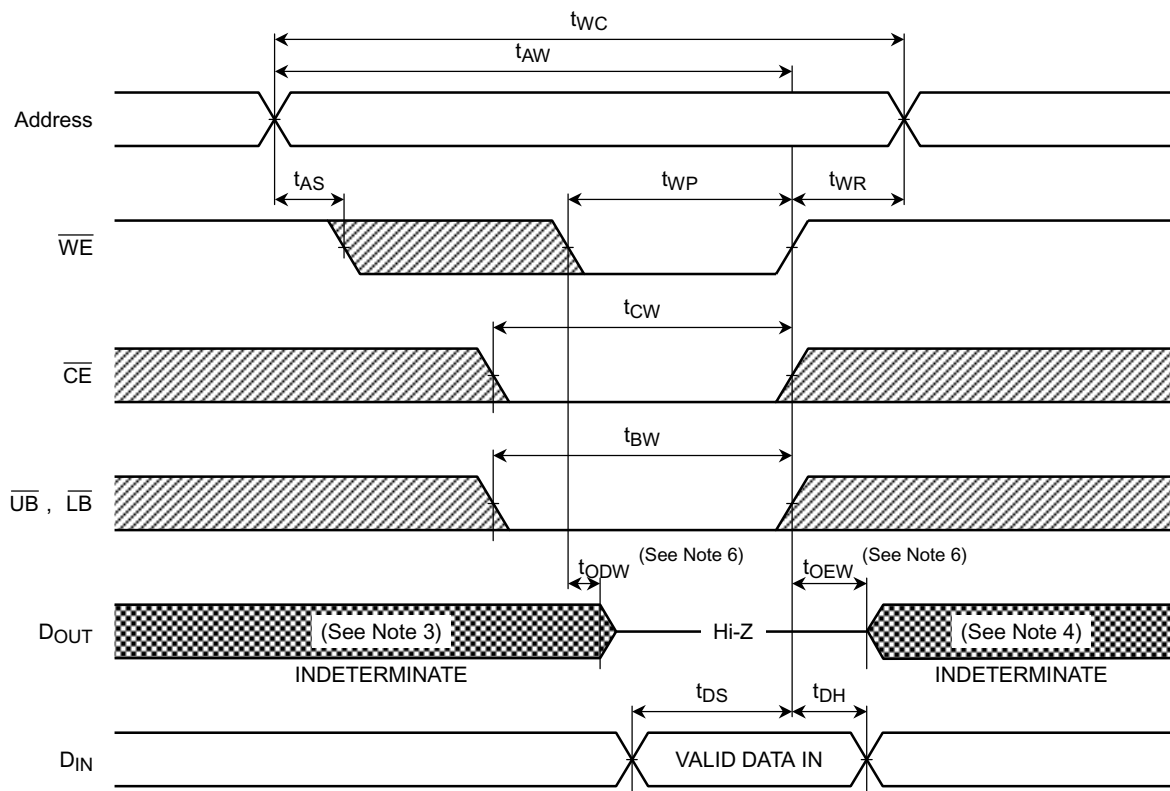


## TIMING DIAGRAMS

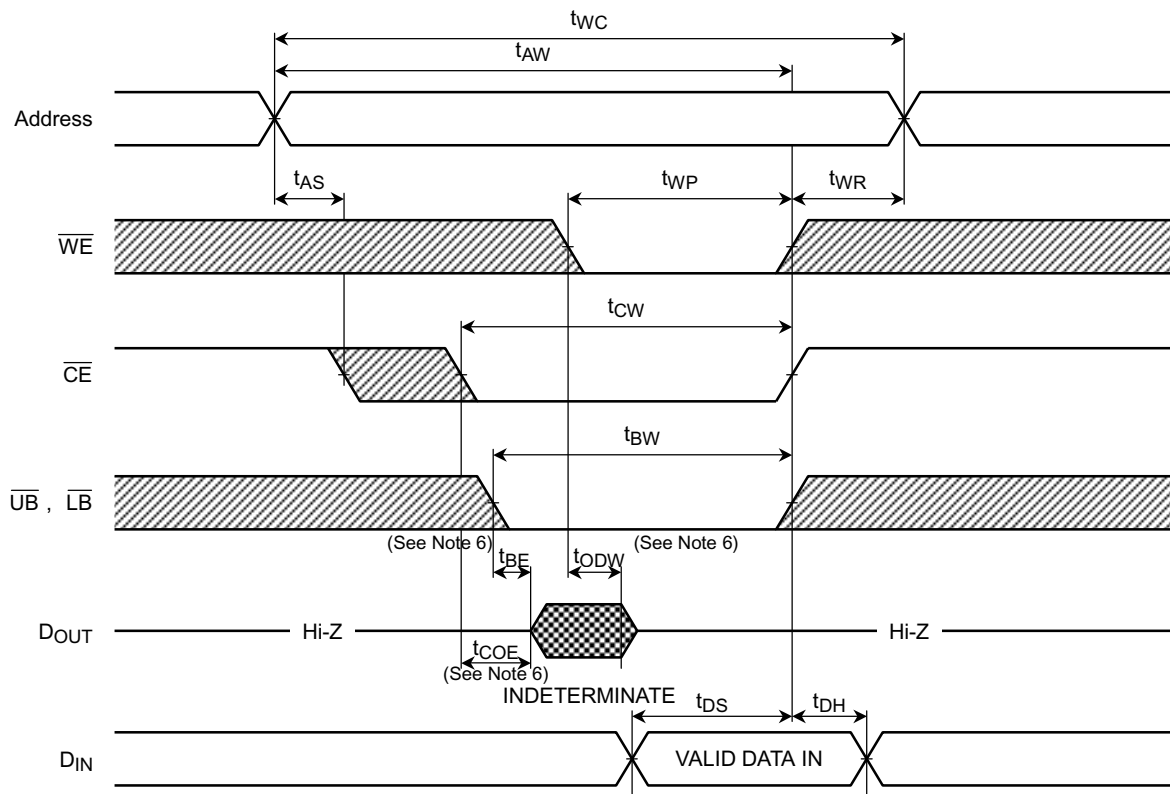
### READ CYCLE (See Note 2)



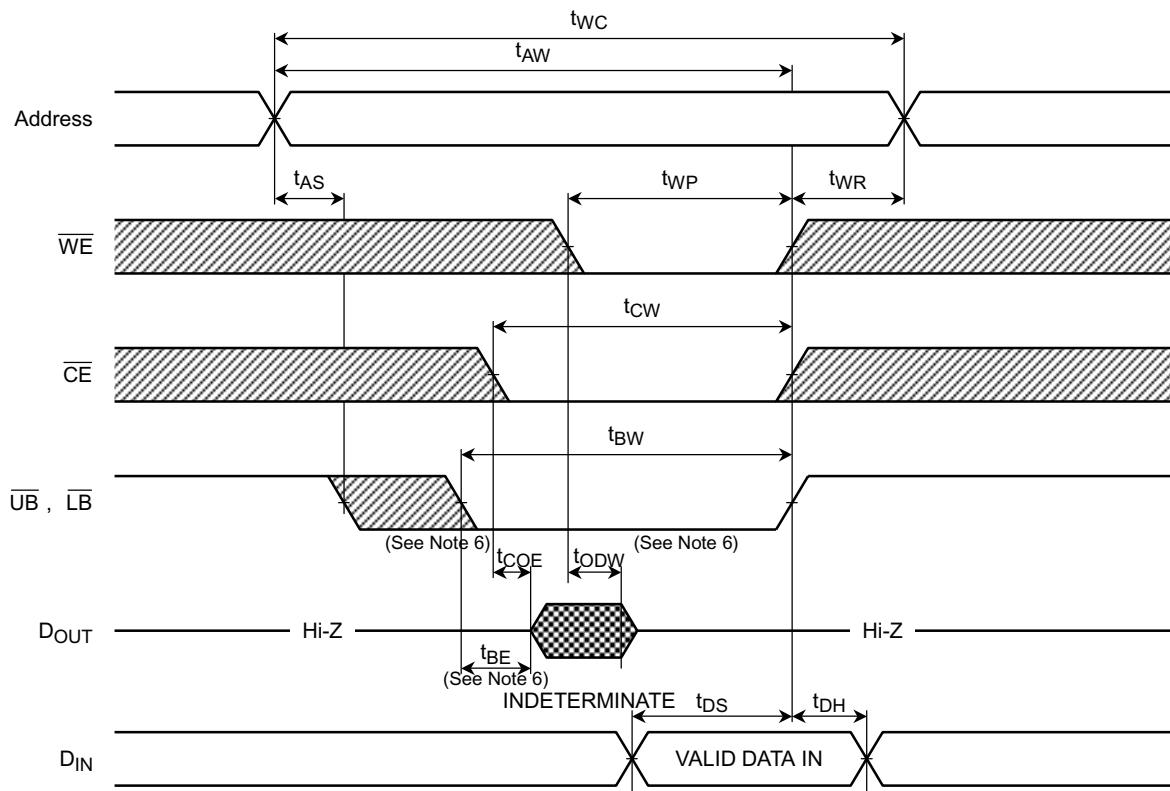
### WRITE CYCLE 1 ( $\overline{WE}$ CONTROLLED) (See Note 5)



WRITE CYCLE 2 ( $\overline{\text{CE}}$  CONTROLLED) (See Note 5)

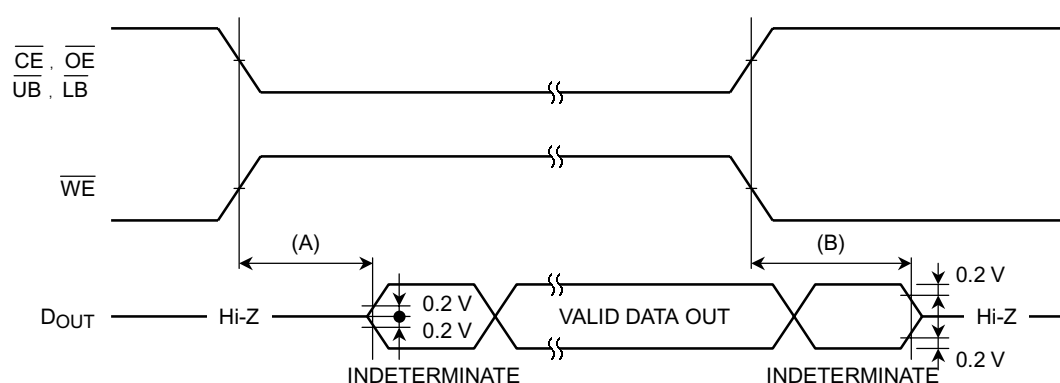


WRITE CYCLE 2 ( $\overline{\text{UB}}$ ,  $\overline{\text{LB}}$  CONTROLLED) (See Note 5)

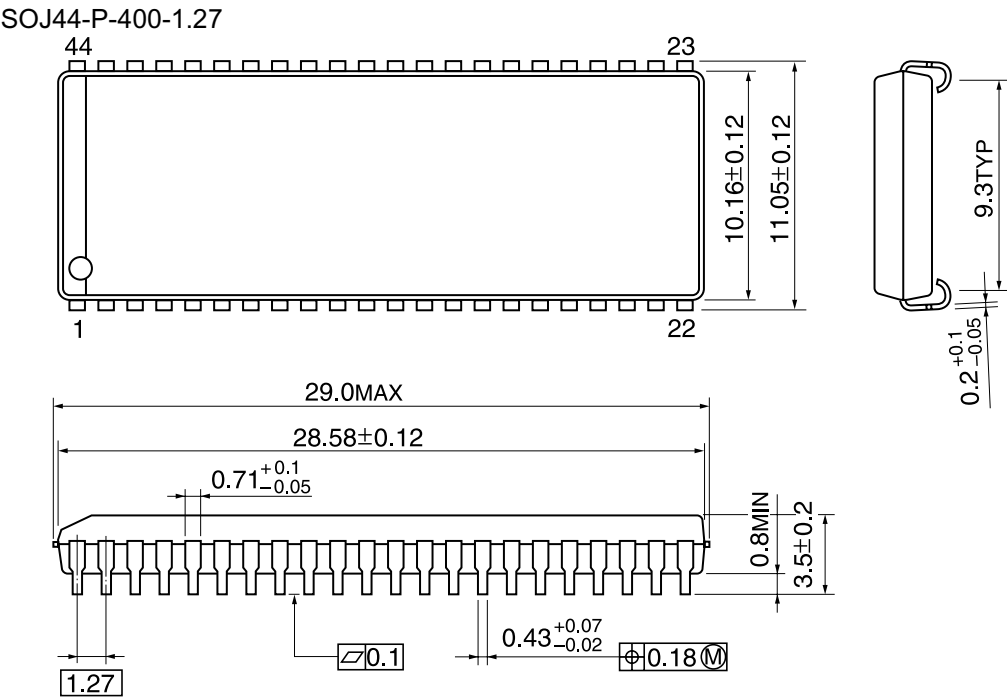


- (1) Operating temperature (Ta) is guaranteed for transverse air flow exceeding 400 linear feet per minute.
- (2)  $\overline{\text{WE}}$  remains HIGH for the Read Cycle.
- (3) If  $\overline{\text{CE}}$  goes LOW coincident with or after  $\overline{\text{WE}}$  goes LOW, the outputs will remain at high impedance.
- (4) If  $\overline{\text{CE}}$  goes HIGH coincident with or before  $\overline{\text{WE}}$  goes HIGH, the outputs will remain at high impedance.
- (5) If  $\overline{\text{OE}}$  is HIGH during the write cycle, the outputs will remain at high impedance.
- (6) The parameters specified below are measured using the load shown in Fig.1.

(B) tCOD, tODO, tBD, tODW..... Output Disable Time



PACKAGE DIMENSIONS

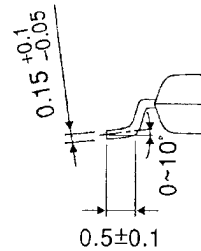
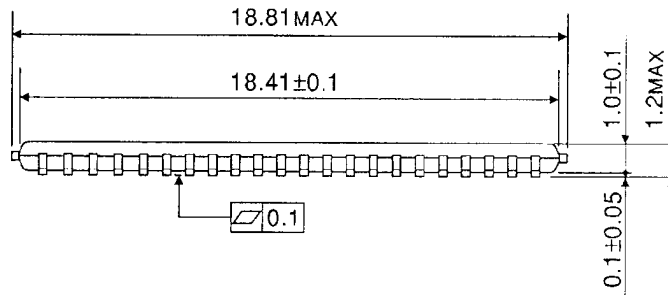
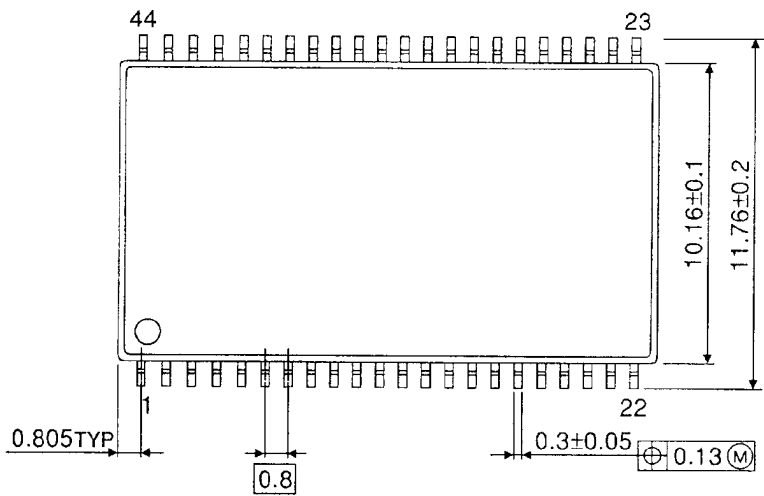


Weight: 1.64 g (typ)

PACKAGE DIMENSIONS

TSOPII 44-P-400-0.80

Unit : mm



Weight: 0.45 g (typ)

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000707EBA

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#### Как с нами связаться

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