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16-bit Microcontroller

CMOS

F²MC-16LX MB90920 Series

**MB90F922NC/F922NCS/922NCS/F923NC/F923NCS/
MB90F924NC/F924NCS/V920-101/V920-102**

■ DESCRIPTION

The MB90920 series is a family of general-purpose FUJITSU SEMICONDUCTOR 16-bit microcontrollers designed for applications such as vehicle instrument panel control.

The instruction set retains the AT architecture from the F²MC-8L and F²MC-16LX families, with further refinements including high-level language instructions, extended addressing modes, improved multiplication and division operations (signed), and bit processing. In addition, long word processing is made possible by the inclusion of a built-in 32-bit accumulator.

Note : F²MC is the abbreviation of FUJITSU Flexible Microcontroller.

■ FEATURES

- Clock
Built-in PLL clock frequency multiplication circuit.
Selection of machine clocks (PLL clocks) is allowed among frequency division by two on oscillation clock, and multiplication of 1 to 8 times of oscillation clock (for 4 MHz oscillation clock, 4 MHz to 32 MHz).
Operation by sub clock (up to 50 kHz : 100 kHz oscillation clock divided by two) is allowed.
- 16-bit input capture (8 channels)
Detects rising, falling, or both edges.
16-bit capture register × 8
The value of a 16-bit free-run timer counter is latched upon detection of an edge input to pin and an interrupt request is generated.

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For the information for microcontroller supports, see the following web site.

This web site includes the "**Customer Design Review Supplement**" which provides the latest cautions on system development and the minimal requirements to be checked to prevent problems before the system development.

<http://edevice.fujitsu.com/micom/en-support/>

MB90920 Series

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- 16-bit reload timer (4 channels)
16-bit reload timer operation (select toggle output or one-shot output)
Selectable event count function
- Real time watch timer (main clock)
Operates directly from oscillator clock.
Interrupt can be generated by second/minute/hour/date counter overflow.
- PPG timer (6 channels)
Output pins (3 channels), external trigger input pin (1 channel)
Operation clock frequencies : f_{CP} , $f_{CP}/2^2$, $f_{CP}/2^4$, $f_{CP}/2^6$
- Delay interrupt
Generates interrupt for task switching.
Interrupts to CPU can be generated/cleared by software setting.
- External interrupts (8 channels)
8-channel independent operation
Interrupt source setting available : “L” to “H” edge/ “H” to “L” edge/ “L” level/ “H” level.
- 8/10-bit A/D converter (8 channels)
Conversion time : 3 μ s (at $f_{CP} = 32$ MHz)
External trigger activation available (P50/INT0/ADTG)
Internal timer activation available (16-bit reload timer 1)
- UART(LIN/SCI) (4 channels)
Equipped with full duplex double buffer
Clock-asynchronous or clock-synchronous serial transfer is available
- CAN interface (4 channels : CAN0 and CAN2, and CAN1 and CAN3 share transmission and reception pins, and interrupt control registers).
Conforms to CAN specifications version 2.0 Part A and B.
Automatic resend in case of error.
Automatic transfer in response to remote frame.
16 prioritized message buffers for data and ID
Multiple message support
Flexible configuration for receive filter : Full bit compare/full bit mask/two partial bit masks
Supports up to 1 Mbps
CAN wakeup function (RX connected to INT0 internally)
- LCD controller/driver (32 segment x 4 common)
Segment driver and command driver with direct LCD panel (display) drive capability
- Reset on detection of low voltage/program loop
Automatic reset when low voltage is detected
Program looping detection function
- Stepping motor controller (4 channels)
High current output for each channel $\times 4$
Synchronized 8/10-bit PWM for each channel $\times 2$
- Sound generator (2 channels)
8-bit PWM signal mixed with tone frequency from 8-bit reload counter.
PWM frequencies : 125 kHz, 62.5 kHz, 31.2 kHz, 15.6 kHz (at $f_{CP} = 32$ MHz)
Tone frequencies : PWM frequency /2/ , divided by (reload frequency +1)
- Input/output ports
General-purpose input/output port (CMOS output) 93 ports
- Function for port input level selection
Automotive/CMOS-Schmitt
- Flash memory security function
Protects the contents of Flash memory (Flash memory product only)

MB90920 Series

■ PRODUCT LINEUP

| Part number Parameter | MB90 F922NC | MB90 F922NCS | MB90 F923NC | MB90 F923NCS | MB90 F924NC | MB90 F924NCS | MB90 922NCS | MB90 V920-101 | MB90 V920-102 |
|--|--|-----------------|----------------------------|-----------------|----------------------------|-----------------|------------------------|--------------------|------------------|
| Type | Flash memory product | | | | | | MASK ROM product | Evaluation product | |
| CPU | F ² MC-16LX CPU | | | | | | | | |
| System clock | PLL clock multiplier circuit (× 1, × 2, × 3, × 4, × 8, 1/2 when PLL stopped) Minimum instruction execution time 31.25 ns (with 4 MHz oscillation clock × 8) | | | | | | | | |
| Sub clock pins (X0A, X1A) | Yes | No | Yes | No | Yes | No | No | No | Yes |
| ROM | Flash memory 256 Kbytes | | Flash memory 384 Kbytes | | Flash memory 512 Kbytes | | 256 K bytes | External | |
| RAM | 10 Kbytes | | 16 Kbytes | | 24 Kbytes | | 10 K bytes | 30 Kbytes | |
| I/O port | 91 ports | 93 ports | 91 ports | 93 ports | 91 ports | 93 ports | 93 ports | 93 ports | 91 ports |
| LCD controller | 32 segment × 4 common | | | | | | | | |
| LIN-UART | UART (LIN/SCI) 4 channels | | | | | | | | |
| CAN interface | 4 channels | | | | | | | | |
| 16-bit input capture | 8 channels | | | | | | | | |
| 16-bit reload timer | 4 channels | | | | | | | | |
| 16-bit free-run timer | 1 channel | | | | | | | | |
| Real time watch timer | 1 channel | | | | | | | | |
| 16-bit PPG timer | 6 channels | | | | | | | | |
| External interrupt | 8 channels | | | | | | | | |
| 8/10-bit A/D converter | 8 channels | | | | | | | | |
| Low-voltage/ CPU operating detection reset | Yes | | | | | | No | | |
| Stepping motor controller | 4 channels | | | | | | | | |
| Sound generator | 2 channels | | | | | | | | |
| Flash memory security | Yes | | | | | | — | | |
| Operating voltage | 4.0 V to 5.5 V | | | | | | 4.5 V to 5.5 V | | |
| Package | LQFP-120 | | | | | | PGA-299 | | |

MB90920 Series

■ PIN ASSIGNMENT



■ PIN DESCRIPTIONS

| Pin no. | Pin name | I/O circuit type*1 | Function |
|---------|-------------------------|--------------------|--|
| 108 | X0 | A | High-speed oscillation input pin |
| 107 | X1 | | High-speed oscillation output pin |
| 13 | X0A | B | Low-speed oscillation input pin |
| | P92 | I | General-purpose I/O port |
| 14 | X1A | B | Low-speed oscillation output pin |
| | P93 | I | General-purpose I/O port |
| 90 | $\overline{\text{RST}}$ | C | Reset input pin |
| 93 | P00 | F | General-purpose I/O port |
| | SEG24 | | LCD controller/driver segment output pin |
| 94 | P01 | F | General-purpose I/O port |
| | SEG25 | | LCD controller/driver segment output pin |
| 95 | P02 | F | General-purpose I/O port |
| | SEG26 | | LCD controller/driver segment output pin |
| 96 | P03 | F | General-purpose I/O port |
| | SEG27 | | LCD controller/driver segment output pin |
| 97 | P04 | F | General-purpose I/O port |
| | SEG28 | | LCD controller/driver segment output pin |
| 98 | P05 | F | General-purpose I/O port |
| | SEG29 | | LCD controller/driver segment output pin |
| 99 | P06 | F | General-purpose I/O port |
| | SEG30 | | LCD controller/driver segment output pin |
| 100 | P07 | F | General-purpose I/O port |
| | SEG31 | | LCD controller/driver segment output pin |
| 101 | P10 | I | General-purpose I/O port |
| | PPG2 | | 16-bit PPG ch.2 output pin |
| | IN5 | | Input capture ch.5 trigger input pin |
| 102 | P11 | I | General-purpose I/O port |
| | TOT0 | | 16-bit reload timer ch.0 TOT output pin |
| | PPG3 | | 16-bit PPG ch.3 output pin |
| | IN4 | | Input capture ch.4 trigger input pin |
| 103 | P12 | I | General-purpose I/O port |
| | TIN0 | | 16-bit reload timer ch.0 TIN input pin |
| | PPG4 | | 16-bit PPG ch.4 output pin |

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MB90920 Series

| Pin no. | Pin name | I/O circuit type*1 | Function |
|---------|----------|--------------------|--|
| 104 | P13 | I | General-purpose I/O port |
| | PPG5 | | 16-bit PPG ch.5 output pin |
| 109 | P14 | I | General-purpose I/O port |
| | TIN2 | | 16-bit reload timer ch.2 TIN input pin |
| | IN1 | | Input capture ch.1 trigger input pin |
| 110 | P15 | I | General-purpose I/O port |
| | IN0 | | Input capture ch.0 trigger input pin |
| 111 | COM0 | P | LCD controller/driver common output pin |
| 112 | COM1 | P | LCD controller/driver common output pin |
| 113 | COM2 | P | LCD controller/driver common output pin |
| 114 | COM3 | P | LCD controller/driver common output pin |
| 115 | P22 | F | General-purpose I/O port |
| | SEG00 | | LCD controller/driver segment output pin |
| 116 | P23 | F | General-purpose I/O port |
| | SEG01 | | LCD controller/driver segment output pin |
| 117 | P24 | F | General-purpose I/O port |
| | SEG02 | | LCD controller/driver segment output pin |
| 118 | P25 | F | General-purpose I/O port |
| | SEG03 | | LCD controller/driver segment output pin |
| 119 | P26 | F | General-purpose I/O port |
| | SEG04 | | LCD controller/driver segment output pin |
| 120 | P27 | F | General-purpose I/O port |
| | SEG05 | | LCD controller/driver segment output pin |
| 1 | P30 | F | General-purpose I/O port |
| | SEG06 | | LCD controller/driver segment output pin |
| 2 | P31 | F | General-purpose I/O port |
| | SEG07 | | LCD controller/driver segment output pin |
| 3 | P32 | F | General-purpose I/O port |
| | SEG08 | | LCD controller/driver segment output pin |
| 4 | P33 | F | General-purpose I/O port |
| | SEG09 | | LCD controller/driver segment output pin |
| 5 | P34 | F | General-purpose I/O port |
| | SEG10 | | LCD controller/driver segment output pin |
| 6 | P35 | F | General-purpose I/O port |
| | SEG11 | | LCD controller/driver segment output pin |

(Continued)

MB90920 Series

| Pin no. | Pin name | I/O circuit type*1 | Function |
|---------|----------|--------------------|--|
| 7 | P36 | F | General-purpose I/O port |
| | SEG12 | | LCD controller/driver segment output pin |
| 8 | P37 | F | General-purpose I/O port |
| | SEG13 | | LCD controller/driver segment output pin |
| 9 | P40 | F | General-purpose I/O port |
| | SEG14 | | LCD controller/driver segment output pin |
| 10 | P41 | F | General-purpose I/O port |
| | SEG15 | | LCD controller/driver segment output pin |
| 11 | P42 | F | General-purpose I/O port |
| | SEG16 | | LCD controller/driver segment output pin |
| 12 | P43 | F | General-purpose I/O port |
| | SEG17 | | LCD controller/driver segment output pin |
| 18 | P44 | F | General-purpose I/O port |
| | SEG18 | | LCD controller/driver segment output pin |
| 19 | P45 | F | General-purpose I/O port |
| | SEG19 | | LCD controller/driver segment output pin |
| 20 | P46 | F | General-purpose I/O port |
| | SEG20 | | LCD controller/driver segment output pin |
| 21 | P47 | F | General-purpose I/O port |
| | SEG21 | | LCD controller/driver segment output pin |
| 37 | P50 | I | General-purpose I/O port |
| | INT0 | | INT0 external interrupt input pin |
| | ADTG | | A/D converter external trigger input pin |
| 58 | P51 | I | General-purpose I/O port |
| | INT1 | | INT1 external interrupt input pin |
| | RX1 | | CAN interface 1 RX input pin |
| | RX3 | | CAN interface 3 RX input pin |
| 59 | P52 | I | General-purpose I/O port |
| | TX1 | | CAN interface 1 TX output pin |
| | TX3 | | CAN interface 3 TX output pin |
| 60 | P53 | I | General-purpose I/O port |
| | INT3 | | INT3 external interrupt input pin |

(Continued)

MB90920 Series

| Pin no. | Pin name | I/O circuit type*1 | Function |
|---------|----------|--------------------|---|
| 61 | P54 | I | General-purpose I/O port |
| | TX0 | | CAN interface 0 TX output pin |
| | TX2 | | CAN interface 2 TX output pin |
| | SGA1 | | Sound generator ch.1 SGA output pin |
| 63 | P55 | I | General-purpose I/O port |
| | RX0 | | CAN interface 0 RX input pin |
| | RX2 | | CAN interface 2 RX input pin |
| | INT2 | | INT2 external interrupt input pin |
| 91 | P56 | I | General-purpose I/O port |
| | SGO0 | | Sound generator ch.0 SGO output pin |
| | FRCK | | Free-run timer clock input pin |
| 92 | P57 | I | General-purpose I/O port |
| | SGA0 | | Sound generator ch.0 SGA output pin |
| 39 | P60 | H | General-purpose I/O port |
| | AN0 | | A/D converter input pin |
| 40 | P61 | H | General-purpose I/O port |
| | AN1 | | A/D converter input pin |
| 41 | P62 | H | General-purpose I/O port |
| | AN2 | | A/D converter input pin |
| 42 | P63 | H | General-purpose I/O port |
| | AN3 | | A/D converter input pin |
| 43 | P64 | H | General-purpose I/O port |
| | AN4 | | A/D converter input pin |
| 44 | P65 | H | General-purpose I/O port |
| | AN5 | | A/D converter input pin |
| 45 | P66 | H | General-purpose I/O port |
| | AN6 | | A/D converter input pin |
| 46 | P67 | H | General-purpose I/O port |
| | AN7 | | A/D converter input pin |
| 67 | P70 | L | General-purpose output-only port |
| | PWM1P0 | | Stepping motor controller ch.0 output pin |
| 68 | P71 | L | General-purpose output-only port |
| | PWM1M0 | | Stepping motor controller ch.0 output pin |
| 69 | P72 | L | General-purpose output-only port |
| | PWM2P0 | | Stepping motor controller ch.0 output pin |

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| Pin no. | Pin name | I/O circuit type*1 | Function |
|---------|----------|--------------------|--|
| 70 | P73 | L | General-purpose output-only port |
| | PWM2M0 | | Stepping motor controller ch.0 output pin |
| 71 | P74 | L | General-purpose output-only port |
| | PWM1P1 | | Stepping motor controller ch.1 output pin |
| 72 | P75 | L | General-purpose output-only port |
| | PWM1M1 | | Stepping motor controller ch.1 output pin |
| 73 | P76 | L | General-purpose output-only port |
| | PWM2P1 | | Stepping motor controller ch.1 output pin |
| 74 | P77 | L | General-purpose output-only port |
| | PWM2M1 | | Stepping motor controller ch.1 output pin |
| 77 | P80 | L | General-purpose output-only port |
| | PWM1P2 | | Stepping motor controller ch.2 output pin |
| 78 | P81 | L | General-purpose output-only port |
| | PWM1M2 | | Stepping motor controller ch.2 output pin |
| 79 | P82 | L | General-purpose output-only port |
| | PWM2P2 | | Stepping motor controller ch.2 output pin |
| 80 | P83 | L | General-purpose output-only port |
| | PWM2M2 | | Stepping motor controller ch.2 output pin |
| 81 | P84 | L | General-purpose output-only port |
| | PWM1P3 | | Stepping motor controller ch.3 output pin |
| 82 | P85 | L | General-purpose output-only port |
| | PWM1M3 | | Stepping motor controller ch.3 output pin |
| 83 | P86 | L | General-purpose output-only port |
| | PWM2P3 | | Stepping motor controller ch.3 output pin |
| 84 | P87 | L | General-purpose output-only port |
| | PWM2M3 | | Stepping motor controller ch.3 output pin |
| 22 | P90 | F | General-purpose I/O port |
| | SEG22 | | LCD controller/driver segment output pin |
| 23 | P91 | F | General-purpose I/O port |
| | SEG23 | | LCD controller/driver segment output pin |
| 31 | P94 | G | General-purpose I/O port |
| | V0 | | LCD controller/driver reference power supply pin |
| 32 | P95 | G | General-purpose I/O port |
| | V1 | | LCD controller/driver reference power supply pin |

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MB90920 Series

| Pin no. | Pin name | I/O circuit type*1 | Function |
|---------|----------|--------------------|--|
| 33 | P96 | G | General-purpose I/O port |
| | V2 | | LCD controller/driver reference power supply pin |
| 34 | V3 | — | LCD controller/driver reference power supply pin |
| 48 | PC0 | J | General-purpose I/O port |
| | SIN0 | | UART ch.0 serial data input pin |
| | INT4 | | INT4 external interrupt input pin |
| 49 | PC1 | I | General-purpose I/O port |
| | SOT0 | | UART ch.0 serial data output pin |
| | INT5 | | INT5 external interrupt input pin |
| | IN3 | | Input capture ch.3 trigger input pin |
| 50 | PC2 | I | General-purpose I/O port |
| | SCK0 | | UART ch.0 serial clock I/O pin |
| | INT6 | | INT6 external interrupt input pin |
| | IN2 | | Input capture ch.2 trigger input pin |
| 51 | PC3 | J | General-purpose I/O port |
| | SIN1 | | UART ch.1 serial data input pin |
| | INT7 | | INT7 external interrupt input pin |
| 52 | PC4 | I | General-purpose I/O port |
| | SOT1 | | UART ch.1 serial data output pin |
| 53 | PC5 | I | General-purpose I/O port |
| | SCK1 | | UART ch.1 serial clock I/O pin |
| | TRG | | 16-bit PPG ch.0 to ch.5 external trigger input pin |
| 54 | PC6 | I | General-purpose I/O port |
| | PPG0 | | 16-bit PPG ch.0 output pin |
| | TOT1 | | 16-bit reload timer ch.1 TOT output pin |
| | IN7 | | Input capture ch.7 trigger input pin |
| 55 | PC7 | I | General-purpose I/O port |
| | PPG1 | | 16-bit PPG ch.1 output pin |
| | TIN1 | | 16-bit reload timer ch.1 TIN input pin |
| | IN6 | | Input capture ch.6 trigger input pin |
| 24 | PD0 | J | General-purpose I/O port |
| | SIN2 | | UART ch.2 serial data input pin |
| 25 | PD1 | I | General-purpose I/O port |
| | SOT2 | | UART ch.2 serial data output pin |

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| Pin no. | Pin name | I/O circuit type*1 | Function |
|-------------|----------|--------------------|---|
| 26 | PD2 | I | General-purpose I/O port |
| | SCK2 | | UART ch.2 serial clock I/O pin |
| 27 | PD3 | J | General-purpose I/O port |
| | SIN3 | | UART ch.3 serial data input pin |
| 28 | PD4 | I | General-purpose I/O port |
| | SOT3 | | UART ch.3 serial data output pin |
| 29 | PD5 | I | General-purpose I/O port |
| | SCK3 | | UART ch.3 serial clock I/O pin |
| 30 | PD6 | I | General-purpose I/O port |
| | TOT2 | | 16-bit reload timer ch.2 TOT output pin |
| 56 | PE0 | I | General-purpose I/O port |
| | TOT3 | | 16-bit reload timer ch.3 TOT output pin |
| 57 | PE1 | I | General-purpose I/O port |
| | TIN3 | | 16-bit reload timer ch.3 TIN input pin |
| 64 | PE2 | I | General-purpose I/O port |
| | SGO1 | | Sound generator ch.1 SGO output pin |
| 62 | RSTO | N | Internal reset signal output pin |
| 65, 75, 85 | DVCC | — | Power supply input pins dedicated for high current output buffer |
| 66, 76, 86 | DVSS | — | Power supply GND pins dedicated for high current output buffer |
| 35 | AVCC | — | A/D converter dedicated power supply input pin |
| 38 | AVSS | — | A/D converter dedicated power supply GND pin |
| 36 | AVRH | — | A/D converter Vref+ input pin. Vref- is fixed to AVSS. |
| 89 | MD0 | D | Mode setting input pin. Connect to VCC pin. |
| 88 | MD1 | D | Mode setting input pin. Connect to VCC pin. |
| 87 | MD2 | D/E*2 | Mode setting input pin. Connect to VSS pin. |
| 17 | C | — | External capacitor pin. Connect a 0.1 μF capacitor between this pin and the VSS pin. |
| 15, 105 | VCC | — | Power supply input pins |
| 16, 47, 106 | VSS | — | GND power supply pins |

*1 : For I/O circuit type, refer to “■ I/O CIRCUIT TYPES”.

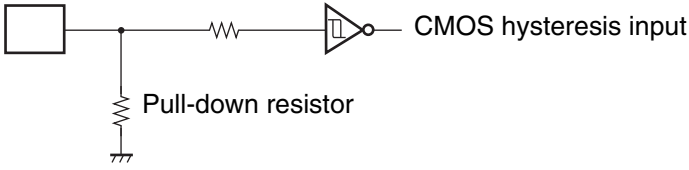
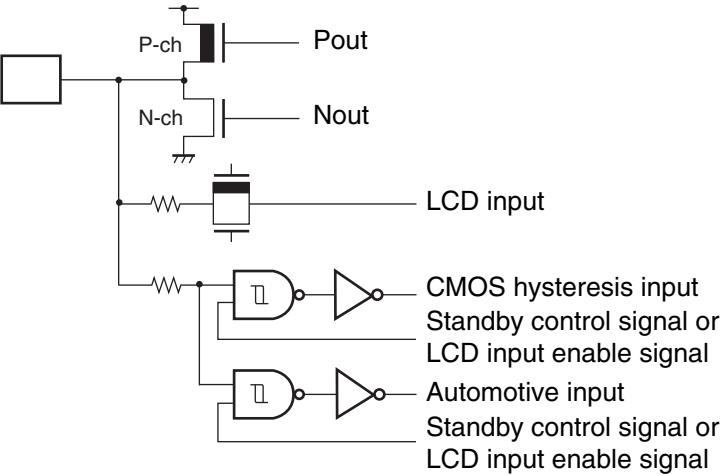
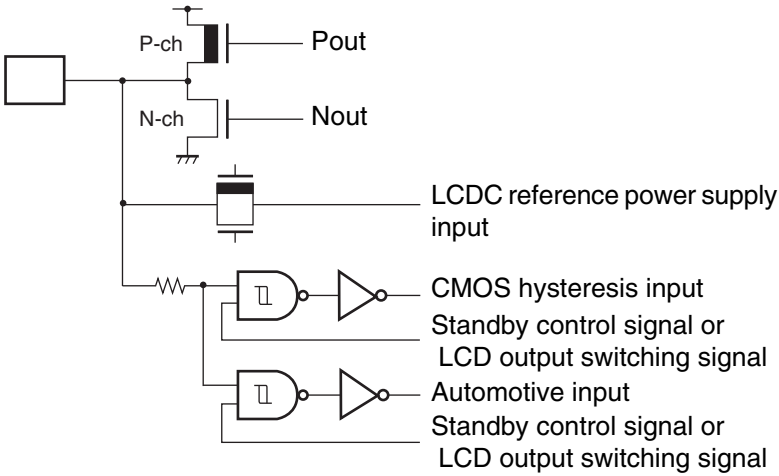
*2 : The I/O circuit type is D for Flash memory products and E for evaluation products.

MB90920 Series

■ I/O CIRCUIT TYPE

| Type | Circuit | Remarks |
|------|---------|--|
| A | | Oscillation circuit High-speed oscillation feedback resistance : approx. 1 M Ω (Flash memory product/MASK ROM product/Evaluation product) |
| B | | Oscillation circuit Low-speed oscillation feedback resistance : approx. 10 M Ω |
| C | | Input-only pin (with pull-up resistance) <ul style="list-style-type: none"> Attached pull-up resistor : approx. 50 kΩ CMOS hysteresis input ($V_{IH}/V_{IL} = 0.8 V_{CC}/0.2 V_{CC}$) |
| D | | Input-only pin <ul style="list-style-type: none"> CMOS hysteresis input ($V_{IH}/V_{IL} = 0.8 V_{CC}/0.2 V_{CC}$) Note: The MD2 pin of the Flash memory products uses this circuit type. |

(Continued)

| Type | Circuit | Remarks |
|------|---|--|
| E |  <p>Pull-down resistor</p> <p>CMOS hysteresis input</p> | <p>Input-only pin (with pull-down resistance)</p> <ul style="list-style-type: none"> Attached pull-down resistance: approx. 50 kΩ CMOS hysteresis input ($V_{IH}/V_{IL} = 0.8 V_{CC}/0.2 V_{CC}$) <p>Note: The MD2 pin of the evaluation products uses this circuit type.</p> |
| F |  <p>P-ch Pout</p> <p>N-ch Nout</p> <p>LCD input</p> <p>CMOS hysteresis input Standby control signal or LCD input enable signal</p> <p>Automotive input Standby control signal or LCD input enable signal</p> | <p>LCD output common general-purpose port</p> <ul style="list-style-type: none"> CMOS output ($I_{OH}/I_{OL} = \pm 4 \text{ mA}$) Hysteresis input ($V_{IH}/V_{IL} = 0.8 V_{CC}/0.2 V_{CC}$) Automotive input ($V_{IH}/V_{IL} = 0.8 V_{CC}/0.5 V_{CC}$) |
| G |  <p>P-ch Pout</p> <p>N-ch Nout</p> <p>LDC reference power supply input</p> <p>CMOS hysteresis input Standby control signal or LCD output switching signal</p> <p>Automotive input Standby control signal or LCD output switching signal</p> | <p>LDC reference power supply common general-purpose port</p> <ul style="list-style-type: none"> CMOS output ($I_{OH}/I_{OL} = \pm 4 \text{ mA}$) CMOS hysteresis input ($V_{IH}/V_{IL} = 0.8 V_{CC}/0.2 V_{CC}$) Automotive input ($V_{IH}/V_{IL} = 0.8 V_{CC}/0.5 V_{CC}$) |

(Continued)

MB90920 Series

| Type | Circuit | Remarks |
|------|---------|--|
| H | | <p>A/D converter input common general-purpose port</p> <ul style="list-style-type: none"> • CMOS output ($I_{OH}/I_{OL} = \pm 4 \text{ mA}$) • CMOS hysteresis input ($V_{IH}/V_{IL} = 0.8 V_{CC}/0.2 V_{CC}$) • Automotive input ($V_{IH}/V_{IL} = 0.8 V_{CC}/0.5 V_{CC}$) |
| I | | <p>General-purpose port</p> <ul style="list-style-type: none"> • CMOS output ($I_{OH}/I_{OL} = \pm 4 \text{ mA}$) • CMOS hysteresis input ($V_{IH}/V_{IL} = 0.8 V_{CC}/0.2 V_{CC}$) • Automotive input ($V_{IH}/V_{IL} = 0.8 V_{CC}/0.5 V_{CC}$) |
| J | | <p>General-purpose port (serial input)</p> <ul style="list-style-type: none"> • CMOS output ($I_{OH}/I_{OL} = \pm 4 \text{ mA}$) • CMOS hysteresis input ($V_{IH}/V_{IL} = 0.8 V_{CC}/0.2 V_{CC}$) • CMOS input (SIN) ($V_{IH}/V_{IL} = 0.7 V_{CC}/0.3 V_{CC}$) • Automotive input ($V_{IH}/V_{IL} = 0.8 V_{CC}/0.5 V_{CC}$) |

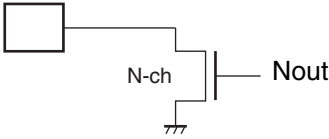
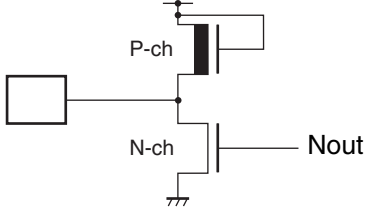

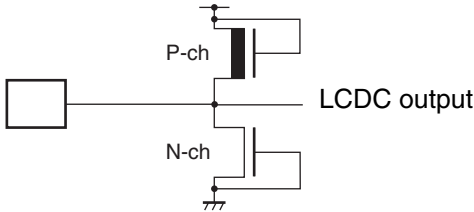
(Continued)

| Type | Circuit | Remarks |
|------|--|---|
| K |  <p>P-ch MOSFET (Pout) N-ch MOSFET (Nout) Analog output CMOS hysteresis input Standby control signal or analog input enable signal Automotive input Standby control signal or analog input enable signal CMOS input (SIN) Standby control signal or analog input enable signal</p> | <p>A/D converter input common general-purpose port (serial input)</p> <ul style="list-style-type: none"> • CMOS output ($I_{OH}/I_{OL} = \pm 4 \text{ mA}$) • CMOS hysteresis input ($V_{IH}/V_{IL} = 0.8 V_{CC}/0.2 V_{CC}$) • CMOS input (SIN) ($V_{IH}/V_{IL} = 0.7 V_{CC}/0.3 V_{CC}$) • Automotive input ($V_{IH}/V_{IL} = 0.8 V_{CC}/0.5 V_{CC}$) |
| L |  <p>P-ch MOSFET (Pout) N-ch MOSFET (Nout) High current</p> | <p>High current output port (SMC pin) CMOS output ($I_{OH}/I_{OL} = \pm 30 \text{ mA}$)</p> |
| M |  <p>P-ch MOSFET (Pout) N-ch MOSFET (Nout) LCDC output CMOS hysteresis input Standby control signal or LCDC output switching signal Automotive input Standby control signal or LCDC output switching signal CMOS input (SIN) Standby control signal or LCDC output switching signal</p> | <p>LCDC output common general-purpose port (serial input)</p> <ul style="list-style-type: none"> • CMOS output ($I_{OH}/I_{OL} = \pm 4 \text{ mA}$) • CMOS hysteresis input ($V_{IH}/V_{IL} = 0.8 V_{CC}/0.2 V_{CC}$) • CMOS input (SIN) ($V_{IH}/V_{IL} = 0.7 V_{CC}/0.3 V_{CC}$) • Automotive input ($V_{IH}/V_{IL} = 0.8 V_{CC}/0.5 V_{CC}$) |

(Continued)

MB90920 Series

(Continued)

| Type | Circuit | Remarks |
|------|--|---|
| N | <div style="display: flex; justify-content: space-around;"> <div style="text-align: center;"> <p>Evaluation product</p>  </div> <div style="text-align: center;"> <p>Flash memory product</p>  </div> </div> | <p>N-ch open-drain pin $I_{OL} = 4 \text{ mA}$</p> |
| O |  | <p>Input-only pin Automotive input $(V_{IH}/V_{IL} = 0.8 V_{CC}/0.5 V_{CC})$</p> |
| P |  | <p>LCDC output pin (COM pin)</p> |

■ HANDLING DEVICES

- **Strictly observe maximum rated voltages (preventing latch-up)**

In CMOS IC devices, a condition known as latch-up may occur if voltages higher than V_{CC} or lower than V_{SS} are applied to input or output pins other than medium or high withstand voltage pins, or if the voltage applied between V_{CC} and V_{SS} pins exceeds the rated voltage level. If a latch-up occurs, the power supply current may increase dramatically and may destroy semiconductor elements. When using semiconductor devices, always take sufficient care to avoid exceeding maximum ratings.

When the analog system power supply is switched on or off, be careful not to apply the analog power supply (AV_{CC} , AV_{RH}), the analog input voltages and the power supply voltage for the high current output buffer pins (DV_{CC}) in excess of the digital power supply voltage (V_{CC}).

Once the digital power supply voltage (V_{CC}) has been disconnected, the analog power supply (AV_{CC} , AV_{RH}) and the power supply voltage for the high current output buffer pins (DV_{CC}) may be turned on in any sequence.

- **Supply voltage stabilization**

Rapid fluctuations in the power supply voltage can cause malfunctions even if the V_{CC} power supply voltage remains within the warranted operating range. It is recommended that the power supply be stabilized such that ripple fluctuations (P-P value) at commercial frequencies (50 Hz/60 Hz) be limited to within 10% of the standard V_{CC} value, and that transient fluctuations due to power supply switching, etc. be limited to a rate of 0.1 V/ms or less.

- **Precautions when turning the power on**

In order to prevent the built-in step-down circuits from malfunctioning, the time taken for the voltage to rise (0.2 V to 2.7 V) during power-on should be less than 50 μ s.

- **Handling unused pins**

If unused input pins are left open, they may cause malfunctions or latch-up which may lead to permanent damage to the semiconductor. Unused input pins should therefore be pulled up or pulled down through a resistor of at least 2 k Ω .

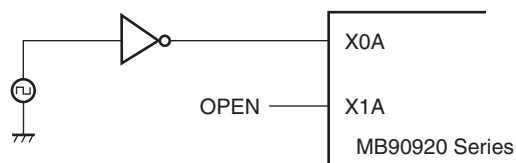
Unused input/output pins may be set to the output state and left open, or set to the input state and connected to a pull-up or pull-down resistance of 2 k Ω or more.

- **Handling A/D converter power supply pins**

Even if the A/D converter is not used, the power supply pins should be connected such as $AV_{CC} = V_{CC}$, and $AV_{SS} = AVR_{H} = V_{SS}$.

- **Notes on using an external clock**

Even when an external clock is used, an oscillation stabilization wait time is required following power-on reset or release from sub clock mode or stop mode. Furthermore, only the X0A pin should be driven when an external clock is used, with the X1A pin open as shown in the following diagram. Do not use high-speed oscillation pins (X0 and X1) for external clock input.



Sample external clock connection

• Notes on operating in PLL clock mode

On this microcontroller, if in case the crystal oscillator breaks off or an external reference clock input stops while the PLL clock mode is selected, a self-oscillator circuit contained in the PLL may continue its operation at its self-running frequency. However, FUJITSU SEMICONDUCTOR will not guarantee results of operations if such failure occurs.

• Crystal oscillator circuit

Noise around the X0/X1, or X0A/X1A pins may cause this device to operate abnormally. In the interest of stable operation it is strongly recommended that printed circuit artwork places ground bypass capacitors as close as possible to the X0/X1, X0A/X1A and crystal oscillator (or ceramic oscillator) and that oscillator lines do not cross the lines of other circuits.

Please ask each crystal maker to evaluate the oscillational characteristics of the crystal and this device.

• Power supply pins

Devices including multiple VCC or VSS pins are designed such that pins that need to be at the same potential are interconnected internally to prevent malfunctions such as latch-up. To reduce unnecessary radiation, prevent malfunctioning of the strobe signal due to the rise of ground level, and observe the standard for total output current, be sure to connect the VCC and VSS pins to the power supply and ground externally.

Always connect all of the VCC pins to the same potential and all of the VSS pins to ground as shown in the following diagram. The device will not operate correctly if multiple VCC or VSS pins are connected to different voltages, even if those voltages are within the guaranteed operating ranges.



In addition, care must be given to connecting the VCC and VSS pins of this device to the current supply source with as low impedance as possible. It is recommended that a 1.0 μF bypass capacitor be connected between the VCC and VSS pins as close to the pins as possible.

• Sequence for connecting the A/D converter power supply and analog inputs

The A/D converter power supply (AV_{CC} , $AVRH$) and analog inputs (AN0 to AN7) must be applied after the digital power supply (V_{CC}) is switched on. When turning the power off, the A/D converter power supply and analog inputs must be disconnected before the digital power supply is switched off (V_{CC}). Ensure that $AVRH$ does not exceed AV_{CC} during either power-on or power-off. Even when pins which double as analog input pins are used as input ports, be sure that the input voltage does not exceed AV_{CC} (turning on/off the analog and digital power supplies simultaneously is acceptable).

- **Handling the power supply for high-current output buffer pins (DV_{CC} , DV_{SS})**

- **Flash memory products and MASK ROM products (MB90F922NC/F922NCS/922NCS/F923NC/F923NCS/F924NC/F924NCS)**

In the Flash memory products and MASK ROM products, the power supply for the high-current output buffer pins (DV_{CC} , DV_{SS}) is isolated from the digital power supply (V_{CC}).

Therefore, DV_{CC} can therefore be set to a higher voltage than V_{CC} . If the power supply for the high-current output buffer pins (DV_{CC} , DV_{SS}) is supplied before the digital power supply (V_{CC}), however, care needs to be taken because it is possible that the port 7 or port 8 stepping motor outputs may momentarily output an “H” or “L” level. In order to prevent this, connect the digital power supply (V_{CC}) prior to connecting the power supply for the high-current output buffer pins. Even when the high-current output buffer pins are used as general-purpose ports, power should be supplied to the power supply pins for the high-current output buffer pins (DV_{CC} , DV_{SS}).

- **Evaluation product (MB90V920-101/MB90V920-102)**

In the evaluation products, the power supply for the high-current output buffer pins (DV_{CC} , DV_{SS}) is not isolated from the digital power supply (V_{CC}). Therefore, DV_{CC} must therefore be set to a lower voltage than V_{CC} . The power supply for the high-current output buffer pins (DV_{CC} , DV_{SS}) must always be applied after the digital power supply (V_{CC}) has been connected, and disconnected before the digital power supply (V_{CC}) is disconnected (the power supply for the high-current output buffer pins may also be connected and disconnected simultaneously with the digital power supply).

Even when the high-current output buffer pins are used as general-purpose ports, power should be supplied to the power supply pins for the high-current output buffer pins (DV_{CC} , DV_{SS}).

- **Pull-up/pull-down resistors**

MB90920 series does not support internal pull-up/pull-down resistors. Use external components as necessary.

- **Precautions when not using a sub clock signal**

If the X0A and X1A pins are not connected to an oscillator, apply a pull-down resistance to the X0A pin and leave the X1A pin open.

- **Notes on operating when the external clock is stopped**

The MB90920 series is not guaranteed to operate correctly using the internal oscillator circuit when there is no external oscillator or the external clock input is stopped.

- **Flash memory security function**

A security bit is located within the Flash memory region. The security function is activated by writing the protection code 01_H to the security bit.

Do not write the value 01_H to this address if you are not using the security function.

Please refer to following table for the address of the security bit.

| | Flash memory size | Address for security bit |
|---------------------------|-------------------------------|--------------------------|
| MB90F922NC MB90F922NCS | Built-in 2 Mbits Flash Memory | FC0001 _H |
| MB90F923NCS | Built-in 3 Mbits Flash Memory | F80001 _H |
| MB90F924NCS | Built-in 4 Mbits Flash Memory | F80001 _H |

- **Serial communication**

In serial communication, reception of wrong data may occur due to noise or other causes. Therefore, design a printed circuit board to prevent noise from occurring. Taking account of the reception of wrong data, detect errors by measures such as adding a checksum to the end of data. If an error is detected, retransmit the data.

- **Characteristic difference between flash device and MASK ROM device**

In the flash device and the MASK ROM device, the electrical characteristic including current consumption, ESD, latch-up, the noise characteristic, and oscillation characteristic, etc. is different according to the difference between the chip layout and the memory structure.

Reconfirm the electrical characteristic when the product is replaced by another product of the same series.

■ BLOCK DIAGRAM



MB90920 Series

MEMORY MAP



| Parts No. | ROM (Flash) capacitance | RAM capacitance | Address #1 | Address #2 | Address #3 |
|---------------------------|-------------------------|-----------------|------------|------------|------------|
| MB90F922NC/F922NCS/922NCS | 256 Kbytes | 10 Kbytes | FC000H | 004A00H | 002900H |
| MB90F923NC/F923NCS | 384 Kbytes | 16 Kbytes | FA0000H | 004A00H | 003700H |
| MB90F924NC/F924NCS | 512 Kbytes | 24 Kbytes | F80000H | 006A00H | 003700H |

* : Evaluation products do not contain internal ROM. Treat this address as the ROM decode area used by the tools.

Note: To select models without the ROM mirror function, refer to the “ROM Mirror Function Selection Module” in Hardware Manual. The image of the ROM data in the FF bank appears at the top of the 00 bank, in order to enable efficient use of small C compiler models. The lower 16-bits of the FF bank addresses are allocated to the same addresses as the lower 16-bits of the 00 bank, making it possible to reference tables in ROM without declaring the “far” modifier with the pointers. For example, when an access is made to the address 00C000H, the actual address to be accessed is FFC000H in ROM. Because the size of the FF bank ROM area exceeds 32 Kbytes, it is not possible to view the entire region in the 00 bank image. Therefore because the ROM data from FF8000H to FFFFFFFH appears in the image from 008000H to 00FFFFFFH, it is recommended that ROM data tables be stored in the area from FF8000H to FFFFFFFH.

■ I/O MAP

| Address | Register name | Symbol | Read/write | Resource name | Initial value |
|-------------------|------------------------------------|--------|------------|---------------|-----------------------|
| 00000H | Port 0 data register | PDR0 | R/W | Port 0 | XXXXXXXX _B |
| 00001H | Port 1 data register | PDR1 | R/W | Port 1 | XXXXXXXX _B |
| 00002H | Port 2 data register | PDR2 | R/W | Port 2 | XXXXXXXX _B |
| 00003H | Port 3 data register | PDR3 | R/W | Port 3 | XXXXXXXX _B |
| 00004H | Port 4 data register | PDR4 | R/W | Port 4 | XXXXXXXX _B |
| 00005H | Port 5 data register | PDR5 | R/W | Port 5 | XXXXXXXX _B |
| 00006H | Port 6 data register | PDR6 | R/W | Port 6 | XXXXXXXX _B |
| 00007H | Port 7 data register | PDR7 | R/W | Port 7 | XXXXXXXX _B |
| 00008H | Port 8 data register | PDR8 | R/W | Port 8 | XXXXXXXX _B |
| 00009H | Port 9 data register | PDR9 | R/W | Port 9 | XXXXXXXX _B |
| 0000AH, 0000BH | (Disabled) | | | | |
| 0000CH | Port C data register | PDRC | R/W | Port C | XXXXXXXX _B |
| 0000DH | Port D data register | PDRD | R/W | Port D | XXXXXXXX _B |
| 0000EH | Port E data register | PDRE | R/W | Port E | XXXXXXXX _B |
| 0000FH | (Disabled) | | | | |
| 00010H | Port 0 direction register | DDR0 | R/W | Port 0 | 00000000 _B |
| 00011H | Port 1 direction register | DDR1 | R/W | Port 1 | XX000000 _B |
| 00012H | Port 2 direction register | DDR2 | R/W | Port 2 | 000000XX _B |
| 00013H | Port 3 direction register | DDR3 | R/W | Port 3 | 00000000 _B |
| 00014H | Port 4 direction register | DDR4 | R/W | Port 4 | 00000000 _B |
| 00015H | Port 5 direction register | DDR5 | R/W | Port 5 | 00000000 _B |
| 00016H | Port 6 direction register | DDR6 | R/W | Port 6 | 00000000 _B |
| 00017H | Port 7 direction register | DDR7 | R/W | Port 7 | 00000000 _B |
| 00018H | Port 8 direction register | DDR8 | R/W | Port 8 | 00000000 _B |
| 00019H | Port 9 direction register | DDR9 | R/W | Port 9 | X0000000 _B |
| 0001AH | Analog input enable | ADER6 | R/W | Port 6, A/D | 11111111 _B |
| 0001BH | (Disabled) | | | | |
| 0001CH | Port C direction register | DDRC | R/W | Port C | 00000000 _B |
| 0001DH | Port D direction register | DDRD | R/W | Port D | X0000000 _B |
| 0001EH | Port E direction register | DDRE | R/W | Port E | XXXXX000 _B |
| 0001FH | (Disabled) | | | | |
| 00020H | Lower A/D control status register | ADCS0 | R/W | A/D converter | 00XXXX00 _B |
| 00021H | Higher A/D control status register | ADCS1 | R/W | | 0000000X _B |
| 00022H | Lower A/D control status register | ADCR0 | R | | 00000000 _B |
| 00023H | Higher A/D data register | ADCR1 | R | | XXXXXX00 _B |

(Continued)

MB90920 Series

| Address | Register name | Symbol | Read/write | Resource name | Initial value |
|--|--|-----------------|------------|--------------------------|-----------------------|
| 000024 _H | Compare clear register | CPCLR | R/W | 16-bit free-run timer | XXXXXXXX _B |
| 000025 _H | | | R/W | | XXXXXXXX _B |
| 000026 _H | Timer data register | TCDT | R/W | | 00000000 _B |
| 000027 _H | | | R/W | | 00000000 _B |
| 000028 _H | Lower timer control status register | TCCSL | R/W | | 00000000 _B |
| 000029 _H | Higher timer control status register | TCCSH | R/W | | 01-00000 _B |
| 00002A _H | Lower PPG0 control status register | PCNTL0 | R/W | 16-bit PPG0 | 00000000 _B |
| 00002B _H | Higher PPG0 control status register | PCNTH0 | R/W | | 00000001 _B |
| 00002C _H | Lower PPG1 control status register | PCNTL1 | R/W | 16-bit PPG1 | 00000000 _B |
| 00002D _H | Higher PPG1 control status register | PCNTH1 | R/W | | 00000001 _B |
| 00002E _H | Lower PPG2 control status register | PCNTL2 | R/W | 16-bit PPG2 | 00000000 _B |
| 00002F _H | Higher PPG2 control status register | PCNTH2 | R/W | | 00000001 _B |
| 000030 _H | External interrupt enable | ENIR | R/W | External interrupt | 00000000 _B |
| 000031 _H | External interrupt request | EIRR | R/W | | 00000000 _B |
| 000032 _H | Lower external interrupt level | ELVRL | R/W | | 00000000 _B |
| 000033 _H | Higher external interrupt level | ELVRH | R/W | | 00000000 _B |
| 000034 _H | Serial mode register 0 | SMR0 | R/W, W | UART (LIN/SCI) 0 | 00000000 _B |
| 000035 _H | Serial control register 0 | SCR0 | R/W, W | | 00000000 _B |
| 000036 _H | Reception/transmission data register 1 | RDR0/ TDR0 | R/W | | 00000000 _B |
| 000037 _H | Serial status register 0 | SSR0 | R/W, R | | 00001000 _B |
| 000038 _H | Extended communication control register 0 | ECCR0 | R/W, R | | 000000XX _B |
| 000039 _H | Extended status control register 0 | ESCR0 | R/W | | 00000100 _B |
| 00003A _H | Baud rate generator register 00 | BGR00 | R/W | | 00000000 _B |
| 00003B _H | Baud rate generator register 01 | BGR01 | R/W, R | | 00000000 _B |
| 00003C _H to 00003F _H | (Disabled) | | | | |
| 000040 _H to 00004F _H | Area reserved for CAN Controller 0. Refer to "■ CAN CONTROLLERS" | | | | |
| 000050 _H | Lower timer control status register 0 | TMCSR0L | R/W | 16-bit reload timer 0 | 00000000 _B |
| 000051 _H | Higher timer control status register 0 | TMCSR0H | R/W | | XXX10000 _B |
| 000052 _H | Timer register 0/reload register 0 | TMR0/ TMRLR0 | R/W | | XXXXXXXX _B |
| 000053 _H | | | | | XXXXXXXX _B |

(Continued)

MB90920 Series

| Address | Register name | Symbol | Read/write | Resource name | Initial value |
|--|--|-----------------------|------------|---|------------------------|
| 000054 _H | Lower timer control status register 1 | TMCSR1L | R/W | 16-bit reload timer 1 | 00000000 _B |
| 000055 _H | Higher timer control status register 1 | TMCSR1H | R/W | | XXX10000 _B |
| 000056 _H | Timer register 1/reload register 1 | TMR1/ TMRLR1 | R/W | | XXXXXXXX _B |
| 000057 _H | | XXXXXXXX _B | | | |
| 000058 _H | LCD output control register 1 | LOCR1 | R/W | LCDC | 11111111 _B |
| 000059 _H | LCD output control register 2 | LOCR2 | R/W | | 00000000 _B |
| 00005A _H | Lower sound control register 0 | SGCRL0 | R/W | Sound generator 0 | 00000000 _B |
| 00005B _H | Higher sound control register 0 | SGCRH0 | R/W | | 0XXXX100 _B |
| 00005C _H | Frequency data register 0 | SGFR0 | R/W | | XXXXXXXX _B |
| 00005D _H | Amplitude data register 0 | SGAR0 | R/W | | 00000000 _B |
| 00005E _H | Decrement grade register 0 | SGDR0 | R/W | | XXXXXXXX _B |
| 00005F _H | Tone count register 0 | SGTR0 | R/W | | XXXXXXXX _B |
| 000060 _H | Input capture register 0 | IPCP0 | R | Input capture 0/1 | XXXXXXXX _B |
| 000061 _H | | | | | XXXXXXXX _B |
| 000062 _H | Input capture register 1 | IPCP1 | R | | XXXXXXXX _B |
| 000063 _H | | | | | XXXXXXXX _B |
| 000064 _H | Input capture register 2 | IPCP2 | R | Input capture 2/3 | XXXXXXXX _B |
| 000065 _H | | | | | XXXXXXXX _B |
| 000066 _H | Input capture register 3 | IPCP3 | R | | XXXXXXXX _B |
| 000067 _H | | | | | XXXXXXXX _B |
| 000068 _H | Input capture control status 0/1 | ICS01 | R/W | Input capture 0/1 | 00000000 _B |
| 000069 _H | Input capture edge register 0/1 | ICE01 | R/W | | XXX0X0XX _B |
| 00006A _H | Input capture control status 2/3 | ICS23 | R/W | Input capture 2/3 | 00000000 _B |
| 00006B _H | Input capture edge register 2/3 | ICE23 | R/W | | XXXXXXXX _B |
| 00006C _H | Lower LCD control register | LCRL | R/W | LCD controller/ driver | 00010000 _B |
| 00006D _H | Higher LCD control register | LCRH | R/W | | 00000000 _B |
| 00006E _H | Low voltage/CPU operation detection reset control register | LVRC | R/W | Low voltage/CPU operation detection reset | 00111000 _B |
| 00006F _H | ROM mirror | ROMM | W | ROM mirror | XXXXXXXX1 _B |
| 000070 _H to 00007F _H | Area reserved for CAN Controller 1. Refer to "■ CAN CONTROLLERS" | | | | |
| 000080 _H | PWM control register 0 | PWC0 | R/W | Stepping motor controller 0 | 000000X0 _B |
| 000081 _H | (Disabled) | | | | |
| 000082 _H | PWM control register 1 | PWC1 | R/W | Stepping motor controller 1 | 000000X0 _B |

(Continued)

MB90920 Series

| Address | Register name | Symbol | Read/write | Resource name | Initial value |
|--|--|--------|------------|------------------------------|------------------------|
| 000083 _H | (Disabled) | | | | |
| 000084 _H | PWM control register 2 | PWC2 | R/W | Stepping motor controller 2 | 000000X0 _B |
| 000085 _H | (Disabled) | | | | |
| 000086 _H | PWM control register 3 | PWC3 | R/W | Stepping motor controller 3 | 000000X0 _B |
| 000087 _H | (Disabled) | | | | |
| 000088 _H | LCD output control register 3 | LOCR3 | R/W | LCDC | XXXXX111 _B |
| 000089 _H | (Disabled) | | | | |
| 00008A _H | A/D setting register 0 | ADSR0 | R/W | A/D converter | 00000000 _B |
| 00008B _H | A/D setting register 1 | ADSR1 | R/W | | 00000000 _B |
| 00008C _H | Port input level select 0 | PIL0 | R/W | Port input level select | 00000000 _B |
| 00008D _H | Port input level select 1 | PIL1 | R/W | | XXXX0000 _B |
| 00008E _H | Port input level select 2 | PIL2 | R/W | | XXXX0000 _B |
| 00008F _H to 00009D _H | (Disabled) | | | | |
| 00009E _H | Program address detection control register | PACSR | R/W | Address match detection | XXXX0X0X _B |
| 00009F _H | Delayed Interrupt/Release Register | DIRR | R/W | Delay interrupt | XXXXXXXX0 _B |
| 0000A0 _H | Power saving mode control register | LPMCR | R/W | Power saving control circuit | 00011000 _B |
| 0000A1 _H | Clock select register | CKSCR | R/W, R | | 11111100 _B |
| 0000A2 _H to 0000A7 _H | (Disabled) | | | | |
| 0000A8 _H | Watchdog timer control register | WDTC | R, W | Watchdog timer | XXXXX111 _B |
| 0000A9 _H | Time-base timer control register | TBTC | R/W, W | Time-base timer | 1XX00100 _B |
| 0000AA _H | Watch timer control register | WTC | R/W, W, R | Watch timer (sub clock) | 10001000 _B |
| 0000AB _H to 0000AD _H | (Disabled) | | | | |
| 0000AE _H | Flash memory control status register | FMCS | R/W | Flash interface | 000X0000 _B |
| 0000AF _H | (Disabled) | | | | |

(Continued)

MB90920 Series

| Address | Register name | Symbol | Read/write | Resource name | Initial value |
|--|--|---------------|------------|--------------------------|-----------------------|
| 0000B0 _H | Interrupt control register 00 | ICR00 | R/W | Interrupt controller | 00000111 _B |
| 0000B1 _H | Interrupt control register 01 | ICR01 | R/W | | 00000111 _B |
| 0000B2 _H | Interrupt control register 02 | ICR02 | R/W | | 00000111 _B |
| 0000B3 _H | Interrupt control register 03 | ICR03 | R/W | | 00000111 _B |
| 0000B4 _H | Interrupt control register 04 | ICR04 | R/W | | 00000111 _B |
| 0000B5 _H | Interrupt control register 05 | ICR05 | R/W | | 00000111 _B |
| 0000B6 _H | Interrupt control register 06 | ICR06 | R/W | | 00000111 _B |
| 0000B7 _H | Interrupt control register 07 | ICR07 | R/W | | 00000111 _B |
| 0000B8 _H | Interrupt control register 08 | ICR08 | R/W | | 00000111 _B |
| 0000B9 _H | Interrupt control register 09 | ICR09 | R/W | | 00000111 _B |
| 0000BA _H | Interrupt control register 10 | ICR10 | R/W | | 00000111 _B |
| 0000BB _H | Interrupt control register 11 | ICR11 | R/W | | 00000111 _B |
| 0000BC _H | Interrupt control register 12 | ICR12 | R/W | | 00000111 _B |
| 0000BD _H | Interrupt control register 13 | ICR13 | R/W | | 00000111 _B |
| 0000BE _H | Interrupt control register 14 | ICR14 | R/W | | 00000111 _B |
| 0000BF _H | Interrupt control register 15 | ICR15 | R/W | | 00000111 _B |
| 0000C0 _H to 0000C3 _H | (Disabled) | | | | |
| 0000C4 _H | Serial mode register 1 | SMR1 | R/W, W | UART (LIN/SCI) 1 | 00000000 _B |
| 0000C5 _H | Serial control register 1 | SCR1 | R/W, W | | 00000000 _B |
| 0000C6 _H | Reception/transmission data register 1 | RDR1/ TDR1 | R/W | | 00000000 _B |
| 0000C7 _H | Serial status register 1 | SSR1 | R/W, R | | 00001000 _B |
| 0000C8 _H | Extended communication control register 1 | ECCR1 | R/W, R | | 000000XX _B |
| 0000C9 _H | Extended status control register 1 | ESCR1 | R/W | | 00000100 _B |
| 0000CA _H | Baud rate generator register 10 | BGR10 | R/W | | 00000000 _B |
| 0000CB _H | Baud rate generator register 11 | BGR11 | R/W, R | | 00000000 _B |
| 0000CC _H | Lower watch timer control register | WTCRL | R/W | Real-time watch timer | 000XXXX0 _B |
| 0000CD _H | Middle watch timer control register | WTCRM | R/W | | 00000000 _B |
| 0000CE _H | Higher watch timer control register | WTCRH | R/W | | XXXXXX00 _B |
| 0000CF _H | Sub clock control register | PSCCR | W | Sub clock | XXXX0000 _B |
| 0000D0 _H | Input capture control status 4/5 | ICS45 | R/W | Input capture 4/5 | 00000000 _B |
| 0000D1 _H | Input capture edge register 4/5 | ICE45 | R/W, R | | XXXXXXXX _B |
| 0000D2 _H | Input capture control status 6/7 | ICS67 | R/W | Input capture 6/7 | 00000000 _B |
| 0000D3 _H | Input capture edge register 6/7 | ICE67 | R/W, R | | XXX0X0XX _B |

(Continued)

MB90920 Series

| Address | Register name | Symbol | Read/write | Resource name | Initial value |
|---------------------|---|---------------|------------|----------------------------|-----------------------|
| 0000D4 _H | Lower timer control status register 2 | TMCSR2L | R/W | 16-bit reload timer 2 | 00000000 _B |
| 0000D5 _H | Higher timer control status register 2 | TMCSR2H | R/W | | XXX10000 _B |
| 0000D6 _H | Lower timer control status register 3 | TMCSR3L | R/W | 16-bit reload timer 3 | 00000000 _B |
| 0000D7 _H | Higher timer control status register 3 | TMCSR3H | R/W | | XXX10000 _B |
| 0000D8 _H | Lower sound control register 1 | SGCRL1 | R/W | Sound generator 1 | 00000000 _B |
| 0000D9 _H | Higher sound control register 1 | SGCRH1 | R/W | | 0XXXX100 _B |
| 0000DA _H | Lower PPG3 control status register | PCNTL3 | R/W | 16-bit PPG3 | 00000000 _B |
| 0000DB _H | Higher PPG3 control status register | PCNTH3 | R/W | | 00000001 _B |
| 0000DC _H | Lower PPG4 control status register | PCNTL4 | R/W | 16-bit PPG4 | 00000000 _B |
| 0000DD _H | Higher PPG4 control status register | PCNTH4 | R/W | | 00000001 _B |
| 0000DE _H | Lower PPG5 control status register | PCNTL5 | R/W | 16-bit PPG5 | 00000000 _B |
| 0000DF _H | Higher PPG5 control status register | PCNTH5 | R/W | | 00000001 _B |
| 0000E0 _H | Serial mode register 2 | SMR2 | R/W, W | UART (LIN/SCI) 2 | 00000000 _B |
| 0000E1 _H | Serial control register 2 | SCR2 | R/W, W | | 00000000 _B |
| 0000E2 _H | Reception/transmission data register 2 | RDR2/ TDR2 | R/W | | 00000000 _B |
| 0000E3 _H | Serial status register 2 | SSR2 | R/W, R | | 00001000 _B |
| 0000E4 _H | Extended communication control register 2 | ECCR2 | R/W, R | | 000000XX _B |
| 0000E5 _H | Extended status control register 2 | ESCR2 | R/W | | 00000100 _B |
| 0000E6 _H | Baud rate generator register 20 | BGR20 | R/W | | 00000000 _B |
| 0000E7 _H | Baud rate generator register 21 | BGR21 | R/W, R | | 00000000 _B |
| 0000E8 _H | Serial mode register 3 | SMR3 | R/W, W | | 00000000 _B |
| 0000E9 _H | Serial control register 3 | SCR3 | R/W, W | | 00000000 _B |
| 0000EA _H | Reception/transmission data register 3 | RDR3/ TDR3 | R/W | 00000000 _B | |
| 0000EB _H | Serial status register 3 | SSR3 | R/W, R | 00001000 _B | |
| 0000EC _H | Extended communication control register 3 | ECCR3 | R/W, R | 000000XX _B | |
| 0000ED _H | Extended status control register 3 | ESCR3 | R/W | 00000100 _B | |
| 0000EE _H | Baud rate generator register 30 | BGR30 | R/W | 00000000 _B | |
| 0000EF _H | Baud rate generator register 31 | BGR31 | R/W, R | 00000000 _B | |
| 001FF0 _H | Program address detection register 0 | PADR0 | R/W | Address match detection | XXXXXXXX _B |
| 001FF1 _H | Program address detection register 1 | PADR0 | R/W | | XXXXXXXX _B |
| 001FF2 _H | Program address detection register 2 | PADR0 | R/W | | XXXXXXXX _B |
| 001FF3 _H | Program address detection register 3 | PADR1 | R/W | | XXXXXXXX _B |
| 001FF4 _H | Program address detection register 4 | PADR1 | R/W | | XXXXXXXX _B |
| 001FF5 _H | Program address detection register 5 | PADR1 | R/W | | XXXXXXXX _B |

(Continued)

MB90920 Series

| Address | Register name | Symbol | Read/write | Resource name | Initial value |
|--|--|---------|------------|-----------------------|-----------------------|
| 003700 _H to 0037FF _H | Area reserved for CAN Controller 2. Refer to "■ CAN CONTROLLERS" | | | | |
| 003800 _H to 0038FF _H | Area reserved for CAN Controller 3. Refer to "■ CAN CONTROLLERS" | | | | |
| 003900 _H to 00391F _H | (Disabled) | | | | |
| 003920 _H | PPG0 down counter register | PDCR0 | R | 16-bit PPG0 | 11111111 _B |
| 003921 _H | | | | | 11111111 _B |
| 003922 _H | PPG0 cycle setting register | PCSR0 | W | | 11111111 _B |
| 003923 _H | | | | | 11111111 _B |
| 003924 _H | PPG0 duty setting register | PDUT0 | W | 16-bit PPG0 | 00000000 _B |
| 003925 _H | | | | | 00000000 _B |
| 003926 _H | PPG0 output division setting register | PPGDIV0 | R/W, R | | 11111100 _B |
| 003927 _H | (Disabled) | | | | |
| 003928 _H | PPG1 down counter register | PDCR1 | R | 16-bit PPG1 | 11111111 _B |
| 003929 _H | | | | | 11111111 _B |
| 00392A _H | PPG1 cycle setting register | PCSR1 | W | | 11111111 _B |
| 00392B _H | | | | | 11111111 _B |
| 00392C _H | PPG1 duty setting register | PDUT1 | W | | 00000000 _B |
| 00392D _H | | | | | 00000000 _B |
| 00392E _H | PPG1 output division setting register | PPGDIV1 | R/W, R | 11111100 _B | |
| 00392F _H | (Disabled) | | | | |
| 003930 _H | PPG2 down counter register | PDCR2 | R | 16-bit PPG2 | 11111111 _B |
| 003931 _H | | | | | 11111111 _B |
| 003932 _H | PPG2 cycle setting register | PCSR2 | W | | 11111111 _B |
| 003933 _H | | | | | 11111111 _B |
| 003934 _H | PPG2 duty setting register | PDUT2 | W | | 00000000 _B |
| 003935 _H | | | | | 00000000 _B |
| 003936 _H | PPG2 output division setting register | PPGDIV2 | R/W, R | 11111100 _B | |
| 003937 _H to 00393F _H | (Disabled) | | | | |
| 003940 _H | Input capture register 4 | IPCP4 | R | Input capture 4/5 | XXXXXXXX _B |
| 003941 _H | | | | | XXXXXXXX _B |
| 003942 _H | Input capture register 5 | IPCP5 | R | | XXXXXXXX _B |
| 003943 _H | | | | | XXXXXXXX _B |

(Continued)

MB90920 Series

| Address | Register name | Symbol | Read/write | Resource name | Initial value |
|--|--|-----------------|------------|------------------------------|-----------------------|
| 003944 _H | Input capture register 6 | IPCP6 | R | Input capture 6/7 | XXXXXXXX _B |
| 003945 _H | | | | | XXXXXXXX _B |
| 003946 _H | Input capture register 7 | IPCP7 | R | | XXXXXXXX _B |
| 003947 _H | | | | | XXXXXXXX _B |
| 003948 _H to 00394F _H | (Disabled) | | | | |
| 003950 _H | Minute data register 2/Reload register 2 | TMR2/ TMRLR2 | R/W | 16-bit reload timer 2 | XXXXXXXX _B |
| 003951 _H | | | | | XXXXXXXX _B |
| 003952 _H | Minute data register 3/Reload register 3 | TMR3/ TMRLR3 | R/W | 16-bit reload timer 3 | XXXXXXXX _B |
| 003953 _H | | | | | XXXXXXXX _B |
| 003954 _H to 003957 _H | (Disabled) | | | | |
| 003958 _H | Sub second data register | WTBR | R/W | Real time watch timer | XXXXXXXX _B |
| 003959 _H | | | | | XXXXXXXX _B |
| 00395A _H | | | | | XXXXXXXX _B |
| 00395B _H | Second data register | WTSR | R/W | | XX000000 _B |
| 00395C _H | Minute data register | WTMR | R/W | | XX000000 _B |
| 00395D _H | Hour data register | WTHR | R/W | | XXX00000 _B |
| 00395E _H | Day data register | WTDR | R/W | 00X00001 _B | |
| 00395F _H | (Disabled) | | | | |
| 003960 _H | LCD display RAM | VRAM | R/W | LCD controller/ driver | XXXXXXXX _B |
| 003961 _H | | | | | XXXXXXXX _B |
| 003962 _H | | | | | XXXXXXXX _B |
| 003963 _H | | | | | XXXXXXXX _B |
| 003964 _H | | | | | XXXXXXXX _B |
| 003965 _H | | | | | XXXXXXXX _B |
| 003966 _H | | | | | XXXXXXXX _B |
| 003967 _H | | | | | XXXXXXXX _B |
| 003968 _H | | | | | XXXXXXXX _B |
| 003969 _H | | | | | XXXXXXXX _B |
| 00396A _H | | | | | XXXXXXXX _B |
| 00396B _H | | | | | XXXXXXXX _B |
| 00396C _H | | | | | XXXXXXXX _B |
| 00396D _H | | | | | XXXXXXXX _B |
| 00396E _H | | | | | XXXXXXXX _B |
| 00396F _H | XXXXXXXX _B | | | | |

(Continued)

MB90920 Series

| Address | Register name | Symbol | Read/write | Resource name | Initial value |
|--|----------------------------|--------|------------|-----------------------------|-----------------------|
| 003970 _H to 003973 _H | (Disabled) | | | | |
| 003974 _H | Frequency data register 1 | SGFR1 | R/W | Sound generator 1 | XXXXXXXX _B |
| 003975 _H | Amplitude data register 1 | SGAR1 | R/W | | 0000000 _B |
| 003976 _H | Decrement grade register 1 | SGDR1 | R/W | | XXXXXXXX _B |
| 003977 _H | Tone count register 1 | SGTR1 | R/W | | XXXXXXXX _B |
| 003978 _H to 00397F _H | (Disabled) | | | | |
| 003980 _H | PWM1 compare register 0 | PWC10 | R/W | Stepping motor controller 0 | XXXXXXXX _B |
| 003981 _H | | | | | XXXXXXXX _B |
| 003982 _H | PWM2 compare register 0 | PWC20 | R/W | | XXXXXXXX _B |
| 003983 _H | | | | | XXXXXXXX _B |
| 003984 _H | PWM1 select register 0 | PWS10 | R/W | | 0000000 _B |
| 003985 _H | PWM2 select register 0 | PWS20 | R/W | | X000000 _B |
| 003986 _H , 003987 _H | (Disabled) | | | | |
| 003988 _H | PWM1 compare register 1 | PWC11 | R/W | Stepping motor controller 1 | XXXXXXXX _B |
| 003989 _H | | | | | XXXXXXXX _B |
| 00398A _H | PWM2 compare register 1 | PWC21 | R/W | | XXXXXXXX _B |
| 00398B _H | | | | | XXXXXXXX _B |
| 00398C _H | PWM1 select register 1 | PWS11 | R/W | | 0000000 _B |
| 00398D _H | PWM2 select register 1 | PWS21 | R/W | | X000000 _B |
| 00398E _H , 00398F _H | (Disabled) | | | | |
| 003990 _H | PWM1 compare register 2 | PWC12 | R/W | Stepping motor controller 2 | XXXXXXXX _B |
| 003991 _H | | | | | XXXXXXXX _B |
| 003992 _H | PWM2 compare register 2 | PWC22 | R/W | | XXXXXXXX _B |
| 003993 _H | | | | | XXXXXXXX _B |
| 003994 _H | PWM1 select register 2 | PWS12 | R/W | | 0000000 _B |
| 003995 _H | PWM2 select register 2 | PWS22 | R/W | | X000000 _B |
| 003996 _H , 003997 _H | (Disabled) | | | | |

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MB90920 Series

(Continued)

| Address | Register name | Symbol | Read/write | Resource name | Initial value |
|--|--|--------|------------|-----------------------------|-----------------------|
| 003998 _H | PWM1 compare register 3 | PWC13 | R/W | Stepping motor controller 3 | XXXXXXXX _B |
| 003999 _H | | | | | XXXXXXXX _B |
| 00399A _H | PWM2 compare register 3 | PWC23 | R/W | | XXXXXXXX _B |
| 00399B _H | | | | | XXXXXXXX _B |
| 00399C _H | PWM1 select register 3 | PWS13 | R/W | | 00000000 _B |
| 00399D _H | PWM2 select register 3 | PWS23 | R/W | | X0000000 _B |
| 00399E _H to 0039A5 _H | (Disabled) | | | | |
| 0039A6 _H | Flash write control register 0 | FWR0 | R/W | Flash I/F | 00000000 _B |
| 0039A7 _H | Flash write control register 1 | FWR1 | | | 00000000 _B |
| 0039A8 _H to 0039BF _H | (Disabled) | | | | |
| 0039C0 _H to 0039DF _H | Area reserved for CAN Controller 2. Refer to “■ CAN CONTROLLERS” | | | | |
| 0039E0 _H to 0039FF _H | Area reserved for CAN Controller 3. Refer to “■ CAN CONTROLLERS” | | | | |
| 003A00 _H to 003AFF _H | Area reserved for CAN Controller 0. Refer to “■ CAN CONTROLLERS” | | | | |
| 003B00 _H to 003BFF _H | Area reserved for CAN Controller 1. Refer to “■ CAN CONTROLLERS” | | | | |
| 003C00 _H to 003CFF _H | Area reserved for CAN Controller 0. Refer to “■ CAN CONTROLLERS” | | | | |
| 003D00 _H to 003DFF _H | Area reserved for CAN Controller 1. Refer to “■ CAN CONTROLLERS” | | | | |
| 003E00 _H to 003EFF _H | Area reserved for CAN Controller 2. Refer to “■ CAN CONTROLLERS” | | | | |
| 003F00 _H to 003FFF _H | Area reserved for CAN Controller 3. Refer to “■ CAN CONTROLLERS” | | | | |

■ CAN CONTROLLERS

The CAN controller has the following features :

- Conforms to CAN Specification Version 2.0 Part A and B
 - Supports transmission/reception in standard frame and extended frame formats
- Supports transmission of data frames by receiving remote frames
- 16 transmission/reception message buffers
 - 29-bit ID and 8-byte data
 - Multi-level message buffer configuration
- Provides full-bit comparison, full-bit mask, acceptance register 0/acceptance register 1 for each message buffer as ID acceptance mask
 - 2 acceptance mask registers in either standard frame format or extended frame formats
- Bit rate programmable from 10 kbps to 2 Mbps (when input clock is at 16 MHz)

List of Control Registers(1)

| Address | | | | Register | Abbreviation | Access | Initial Value |
|---------------------|---------------------|---------------------|---------------------|-------------------------------|--------------|--------|--|
| CAN0 | CAN1 | CAN2 | CAN3 | | | | |
| 003C00 _H | 003D00 _H | 003E00 _H | 003F00 _H | Control status register | CSR | R/W, R | 00---000 _B 0----0-1 _B |
| 003C01 _H | 003D01 _H | 003E01 _H | 003F01 _H | | | | |
| 003C02 _H | 003D02 _H | 003E02 _H | 003F02 _H | Last event indicator register | LEIR | R/W | ----- _B 000-0000 _B |
| 003C03 _H | 003D03 _H | 003E03 _H | 003F03 _H | | | | |
| 003C04 _H | 003D04 _H | 003E04 _H | 003F04 _H | RX/TX error counter | RTEC | R | 00000000 _B 00000000 _B |
| 003C05 _H | 003D05 _H | 003E05 _H | 003F05 _H | | | | |
| 003C06 _H | 003D06 _H | 003E06 _H | 003F06 _H | Bit timing register | BTR | R/W | -1111111 _B 11111111 _B |
| 003C07 _H | 003D07 _H | 003E07 _H | 003F07 _H | | | | |

MB90920 Series

List of Control Registers(2)

| Address | | | | Register | Abbreviation | Access | Initial Value |
|---------------------|---------------------|---------------------|---------------------|------------------------------------|--------------|--------|--|
| CAN0 | CAN1 | CAN2 | CAN3 | | | | |
| 000040 _H | 000070 _H | 0039C0 _H | 0039D0 _H | Message buffer valid register | BVALR | R/W | 00000000 _B 00000000 _B |
| 000041 _H | 000071 _H | 0039C1 _H | 0039D1 _H | | | | |
| 000042 _H | 000072 _H | 0039C2 _H | 0039D2 _H | Transmit request register | TREQR | R/W | 00000000 _B 00000000 _B |
| 000043 _H | 000073 _H | 0039C3 _H | 0039D3 _H | | | | |
| 000044 _H | 000074 _H | 0039C4 _H | 0039D4 _H | Transmit cancel register | TCANR | W | 00000000 _B 00000000 _B |
| 000045 _H | 000075 _H | 0039C5 _H | 0039D5 _H | | | | |
| 000046 _H | 000076 _H | 0039C6 _H | 0039D6 _H | Transmit complete register | TCR | R/W | 00000000 _B 00000000 _B |
| 000047 _H | 000077 _H | 0039C7 _H | 0039D7 _H | | | | |
| 000048 _H | 000078 _H | 0039C8 _H | 0039D8 _H | Receive complete register | RCR | R/W | 00000000 _B 00000000 _B |
| 000049 _H | 000079 _H | 0039C9 _H | 0039D9 _H | | | | |
| 00004A _H | 00007A _H | 0039CA _H | 0039DA _H | Remote request receive register | RRTRR | R/W | 00000000 _B 00000000 _B |
| 00004B _H | 00007B _H | 0039CB _H | 0039DB _H | | | | |
| 00004C _H | 00007C _H | 0039CC _H | 0039DC _H | Receive overrun register | ROVRR | R/W | 00000000 _B 00000000 _B |
| 00004D _H | 00007D _H | 0039CD _H | 0039DD _H | | | | |
| 00004E _H | 00007E _H | 0039CE _H | 0039DE _H | Receive interrupt enable register | RIER | R/W | 00000000 _B 00000000 _B |
| 00004F _H | 00007F _H | 0039CF _H | 0039DF _H | | | | |
| 003C08 _H | 003D08 _H | 003E08 _H | 003F08 _H | IDE register | IDER | R/W | XXXXXXXX _B |
| 003C09 _H | 003D09 _H | 003E09 _H | 003F09 _H | | | | XXXXXXXX _B |
| 003C0A _H | 003D0A _H | 003E0A _H | 003F0A _H | Transmit RTR register | TRTRR | R/W | 00000000 _B |
| 003C0B _H | 003D0B _H | 003E0B _H | 003F0B _H | | | | 00000000 _B |
| 003C0C _H | 003D0C _H | 003E0C _H | 003F0C _H | Remote frame receive wait register | RFWTR | R/W | XXXXXXXX _B |
| 003C0D _H | 003D0D _H | 003E0D _H | 003F0D _H | | | | XXXXXXXX _B |
| 003C0E _H | 003D0E _H | 003E0E _H | 003F0E _H | Transmit interrupt enable register | TIER | R/W | 00000000 _B |
| 003C0F _H | 003D0F _H | 003E0F _H | 003F0F _H | | | | 00000000 _B |
| 003C10 _H | 003D10 _H | 003E10 _H | 003F10 _H | Acceptance mask select register | AMSR | R/W | XXXXXXXX _B |
| 003C11 _H | 003D11 _H | 003E11 _H | 003F11 _H | | | | XXXXXXXX _B |
| 003C12 _H | 003D12 _H | 003E12 _H | 003F12 _H | | | | XXXXXXXX _B |
| 003C13 _H | 003D13 _H | 003E13 _H | 003F13 _H | | | | XXXXXXXX _B |
| 003C14 _H | 003D14 _H | 003E14 _H | 003F14 _H | Acceptance mask register 0 | AMR0 | R/W | XXXXXXXX _B |
| 003C15 _H | 003D15 _H | 003E15 _H | 003F15 _H | | | | XXXXXXXX _B |
| 003C16 _H | 003D16 _H | 003E16 _H | 003F16 _H | | | | XXXXXX--- _B |
| 003C17 _H | 003D17 _H | 003E17 _H | 003F17 _H | | | | XXXXXXXX _B |
| 003C18 _H | 003D18 _H | 003E18 _H | 003F18 _H | Acceptance mask register 1 | AMR1 | R/W | XXXXXXXX _B |
| 003C19 _H | 003D19 _H | 003E19 _H | 003F19 _H | | | | XXXXXXXX _B |
| 003C1A _H | 003D1A _H | 003E1A _H | 003F1A _H | | | | XXXXXX--- _B |
| 003C1B _H | 003D1B _H | 003E1B _H | 003F1B _H | | | | XXXXXXXX _B |

List of Message Buffers (ID Registers)

| Address | | | | Register | Abbreviation | Access | Initial Value |
|--|--|--|--|---------------------|--------------|--------|--|
| CAN0 | CAN1 | CAN2 | CAN3 | | | | |
| 003A00 _H to 003A1F _H | 003B00 _H to 003B1F _H | 003700 _H to 00371F _H | 003800 _H to 00381F _H | General-purpose RAM | — | R/W | XXXXXXXX _B to XXXXXXXX _B |
| 003A20 _H | 003B20 _H | 003720 _H | 003820 _H | ID register 0 | IDR0 | R/W | XXXXXXXX _B XXXXXXXX _B |
| 003A21 _H | 003B21 _H | 003721 _H | 003821 _H | | | | XXXXX--- _B XXXXXXXX _B |
| 003A22 _H | 003B22 _H | 003722 _H | 003822 _H | | | | |
| 003A23 _H | 003B23 _H | 003723 _H | 003823 _H | | | | |
| 003A24 _H | 003B24 _H | 003724 _H | 003824 _H | ID register 1 | IDR1 | R/W | XXXXXXXX _B XXXXXXXX _B |
| 003A25 _H | 003B25 _H | 003725 _H | 003825 _H | | | | XXXXX--- _B XXXXXXXX _B |
| 003A26 _H | 003B26 _H | 003726 _H | 003826 _H | | | | |
| 003A27 _H | 003B27 _H | 003727 _H | 003827 _H | | | | |
| 003A28 _H | 003B28 _H | 003728 _H | 003828 _H | ID register 2 | IDR2 | R/W | XXXXXXXX _B XXXXXXXX _B |
| 003A29 _H | 003B29 _H | 003729 _H | 003829 _H | | | | XXXXX--- _B XXXXXXXX _B |
| 003A2A _H | 003B2A _H | 00372A _H | 00382A _H | | | | |
| 003A2B _H | 003B2B _H | 00372B _H | 00382B _H | | | | |
| 003A2C _H | 003B2C _H | 00372C _H | 00382C _H | ID register 3 | IDR3 | R/W | XXXXXXXX _B XXXXXXXX _B |
| 003A2D _H | 003B2D _H | 00372D _H | 00382D _H | | | | XXXXX--- _B XXXXXXXX _B |
| 003A2E _H | 003B2E _H | 00372E _H | 00382E _H | | | | |
| 003A2F _H | 003B2F _H | 00372F _H | 00382F _H | | | | |
| 003A30 _H | 003B30 _H | 003730 _H | 003830 _H | ID register 4 | IDR4 | R/W | XXXXXXXX _B XXXXXXXX _B |
| 003A31 _H | 003B31 _H | 003731 _H | 003831 _H | | | | XXXXX--- _B XXXXXXXX _B |
| 003A32 _H | 003B32 _H | 003732 _H | 003832 _H | | | | |
| 003A33 _H | 003B33 _H | 003733 _H | 003833 _H | | | | |
| 003A34 _H | 003B34 _H | 003734 _H | 003834 _H | ID register 5 | IDR5 | R/W | XXXXXXXX _B XXXXXXXX _B |
| 003A35 _H | 003B35 _H | 003735 _H | 003835 _H | | | | XXXXX--- _B XXXXXXXX _B |
| 003A36 _H | 003B36 _H | 003736 _H | 003836 _H | | | | |
| 003A37 _H | 003B37 _H | 003737 _H | 003837 _H | | | | |
| 003A38 _H | 003B38 _H | 003738 _H | 003838 _H | ID register 6 | IDR6 | R/W | XXXXXXXX _B XXXXXXXX _B |
| 003A39 _H | 003B39 _H | 003739 _H | 003839 _H | | | | XXXXX--- _B XXXXXXXX _B |
| 003A3A _H | 003B3A _H | 00373A _H | 00383A _H | | | | |
| 003A3B _H | 003B3B _H | 00373B _H | 00383B _H | | | | |
| 003A3C _H | 003B3C _H | 00373C _H | 00383C _H | ID register 7 | IDR7 | R/W | XXXXXXXX _B XXXXXXXX _B |
| 003A3D _H | 003B3D _H | 00373D _H | 00383D _H | | | | XXXXX--- _B XXXXXXXX _B |
| 003A3E _H | 003B3E _H | 00373E _H | 00383E _H | | | | |
| 003A3F _H | 003B3F _H | 00373F _H | 00383F _H | | | | |

(Continued)

MB90920 Series

(Continued)

| Address | | | | Register | Abbreviation | Access | Initial Value |
|---------------------|---------------------|---------------------|---------------------|----------------|--------------|--------|--|
| CAN0 | CAN1 | CAN2 | CAN3 | | | | |
| 003A40 _H | 003B40 _H | 003740 _H | 003840 _H | ID register 8 | IDR8 | R/W | XXXXXXXX _B XXXXXXXX _B |
| 003A41 _H | 003B41 _H | 003741 _H | 003841 _H | | | | |
| 003A42 _H | 003B42 _H | 003742 _H | 003842 _H | | | | |
| 003A43 _H | 003B43 _H | 003743 _H | 003843 _H | | | | |
| 003A44 _H | 003B44 _H | 003744 _H | 003844 _H | ID register 9 | IDR9 | R/W | XXXXXXXX _B XXXXXXXX _B |
| 003A45 _H | 003B45 _H | 003745 _H | 003845 _H | | | | |
| 003A46 _H | 003B46 _H | 003746 _H | 003846 _H | | | | |
| 003A47 _H | 003B47 _H | 003747 _H | 003847 _H | | | | |
| 003A48 _H | 003B48 _H | 003748 _H | 003848 _H | ID register 10 | IDR10 | R/W | XXXXXXXX _B XXXXXXXX _B |
| 003A49 _H | 003B49 _H | 003749 _H | 003849 _H | | | | |
| 003A4A _H | 003B4A _H | 00374A _H | 00384A _H | | | | |
| 003A4B _H | 003B4B _H | 00374B _H | 00384B _H | | | | |
| 003A4C _H | 003B4C _H | 00374C _H | 00384C _H | ID register 11 | IDR11 | R/W | XXXXXXXX _B XXXXXXXX _B |
| 003A4D _H | 003B4D _H | 00374D _H | 00384D _H | | | | |
| 003A4E _H | 003B4E _H | 00374E _H | 00384E _H | | | | |
| 003A4F _H | 003B4F _H | 00374F _H | 00384F _H | | | | |
| 003A50 _H | 003B50 _H | 003750 _H | 003850 _H | ID register 12 | IDR12 | R/W | XXXXXXXX _B XXXXXXXX _B |
| 003A51 _H | 003B51 _H | 003751 _H | 003851 _H | | | | |
| 003A52 _H | 003B52 _H | 003752 _H | 003852 _H | | | | |
| 003A53 _H | 003B53 _H | 003753 _H | 003853 _H | | | | |
| 003A54 _H | 003B54 _H | 003754 _H | 003854 _H | ID register 13 | IDR13 | R/W | XXXXXXXX _B XXXXXXXX _B |
| 003A55 _H | 003B55 _H | 003755 _H | 003855 _H | | | | |
| 003A56 _H | 003B56 _H | 003756 _H | 003856 _H | | | | |
| 003A57 _H | 003B57 _H | 003757 _H | 003857 _H | | | | |
| 003A58 _H | 003B58 _H | 003758 _H | 003858 _H | ID register 14 | IDR14 | R/W | XXXXXXXX _B XXXXXXXX _B |
| 003A59 _H | 003B59 _H | 003759 _H | 003859 _H | | | | |
| 003A5A _H | 003B5A _H | 00375A _H | 00385A _H | | | | |
| 003A5B _H | 003B5B _H | 00375B _H | 00385B _H | | | | |
| 003A5C _H | 003B5C _H | 00375C _H | 00385C _H | ID register 15 | IDR15 | R/W | XXXXXXXX _B XXXXXXXX _B |
| 003A5D _H | 003B5D _H | 00375D _H | 00385D _H | | | | |
| 003A5E _H | 003B5E _H | 00375E _H | 00385E _H | | | | |
| 003A5F _H | 003B5F _H | 00375F _H | 00385F _H | | | | |

List of Message Buffers (DLC Registers)

| Address | | | | Register | Abbrevia- tion | Access | Initial Value |
|---------------------|---------------------|---------------------|---------------------|-----------------|-------------------|--------|-----------------------|
| CAN0 | CAN1 | CAN2 | CAN3 | | | | |
| 003A60 _H | 003B60 _H | 003760 _H | 003860 _H | DLC register 0 | DLCR0 | R/W | ----XXXX _B |
| 003A61 _H | 003B61 _H | 003761 _H | 003861 _H | | | | |
| 003A62 _H | 003B62 _H | 003762 _H | 003862 _H | DLC register 1 | DLCR1 | R/W | ----XXXX _B |
| 003A63 _H | 003B63 _H | 003763 _H | 003863 _H | | | | |
| 003A64 _H | 003B64 _H | 003764 _H | 003864 _H | DLC register 2 | DLCR2 | R/W | ----XXXX _B |
| 003A65 _H | 003B65 _H | 003765 _H | 003865 _H | | | | |
| 003A66 _H | 003B66 _H | 003766 _H | 003866 _H | DLC register 3 | DLCR3 | R/W | ----XXXX _B |
| 003A67 _H | 003B67 _H | 003767 _H | 003867 _H | | | | |
| 003A68 _H | 003B68 _H | 003768 _H | 003868 _H | DLC register 4 | DLCR4 | R/W | ----XXXX _B |
| 003A69 _H | 003B69 _H | 003769 _H | 003869 _H | | | | |
| 003A6A _H | 003B6A _H | 00376A _H | 00386A _H | DLC register 5 | DLCR5 | R/W | ----XXXX _B |
| 003A6B _H | 003B6B _H | 00376B _H | 00386B _H | | | | |
| 003A6C _H | 003B6C _H | 00376C _H | 00386C _H | DLC register 6 | DLCR6 | R/W | ----XXXX _B |
| 003A6D _H | 003B6D _H | 00376D _H | 00386D _H | | | | |
| 003A6E _H | 003B6E _H | 00376E _H | 00386E _H | DLC register 7 | DLCR7 | R/W | ----XXXX _B |
| 003A6F _H | 003B6F _H | 00376F _H | 00386F _H | | | | |
| 003A70 _H | 003B70 _H | 003770 _H | 003870 _H | DLC register 8 | DLCR8 | R/W | ----XXXX _B |
| 003A71 _H | 003B71 _H | 003771 _H | 003871 _H | | | | |
| 003A72 _H | 003B72 _H | 003772 _H | 003872 _H | DLC register 9 | DLCR9 | R/W | ----XXXX _B |
| 003A73 _H | 003B73 _H | 003773 _H | 003873 _H | | | | |
| 003A74 _H | 003B74 _H | 003774 _H | 003874 _H | DLC register 10 | DLCR10 | R/W | ----XXXX _B |
| 003A75 _H | 003B75 _H | 003775 _H | 003875 _H | | | | |
| 003A76 _H | 003B76 _H | 003776 _H | 003876 _H | DLC register 11 | DLCR11 | R/W | ----XXXX _B |
| 003A77 _H | 003B77 _H | 003777 _H | 003877 _H | | | | |
| 003A78 _H | 003B78 _H | 003778 _H | 003878 _H | DLC register 12 | DLCR12 | R/W | ----XXXX _B |
| 003A79 _H | 003B79 _H | 003779 _H | 003879 _H | | | | |
| 003A7A _H | 003B7A _H | 00377A _H | 00387A _H | DLC register 13 | DLCR13 | R/W | ----XXXX _B |
| 003A7B _H | 003B7B _H | 00377B _H | 00387B _H | | | | |
| 003A7C _H | 003B7C _H | 00377C _H | 00387C _H | DLC register 14 | DLCR14 | R/W | ----XXXX _B |
| 003A7D _H | 003B7D _H | 00377D _H | 00387D _H | | | | |
| 003A7E _H | 003B7E _H | 00377E _H | 00387E _H | DLC register 15 | DLCR15 | R/W | ----XXXX _B |
| 003A7F _H | 003B7F _H | 00377F _H | 00387F _H | | | | |

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List of Message Buffers (Data register)

| Address | | | | Register | Abbreviation | Access | Initial Value |
|--|--|--|--|----------------------------|--------------|--------|--|
| CAN0 | CAN1 | CAN2 | CAN3 | | | | |
| 003A80 _H to 003A87 _H | 003B80 _H to 003B87 _H | 003780 _H to 003787 _H | 003880 _H to 003887 _H | Data register 0 (8 bytes) | DTR0 | R/W | XXXXXXXX _B to XXXXXXXX _B |
| 003A88 _H to 003A8F _H | 003B88 _H to 003B8F _H | 003788 _H to 00378F _H | 003888 _H to 00388F _H | Data register 1 (8 bytes) | DTR1 | R/W | XXXXXXXX _B to XXXXXXXX _B |
| 003A90 _H to 003A97 _H | 003B90 _H to 003B97 _H | 003790 _H to 003797 _H | 003890 _H to 003897 _H | Data register 2 (8 bytes) | DTR2 | R/W | XXXXXXXX _B to XXXXXXXX _B |
| 003A98 _H to 003A9F _H | 003B98 _H to 003B9F _H | 003798 _H to 00379F _H | 003898 _H to 00389F _H | Data register 3 (8 bytes) | DTR3 | R/W | XXXXXXXX _B to XXXXXXXX _B |
| 003AA0 _H to 003AA7 _H | 003BA0 _H to 003BA7 _H | 0037A0 _H to 0037A7 _H | 0038A0 _H to 0038A7 _H | Data register 4 (8 bytes) | DTR4 | R/W | XXXXXXXX _B to XXXXXXXX _B |
| 003AA8 _H to 003AAF _H | 003BA8 _H to 003BAF _H | 0037A8 _H to 0037AF _H | 0038A8 _H to 0038AF _H | Data register 5 (8 bytes) | DTR5 | R/W | XXXXXXXX _B to XXXXXXXX _B |
| 003AB0 _H to 003AB7 _H | 003BB0 _H to 003BB7 _H | 0037B0 _H to 0037B7 _H | 0038B0 _H to 0038B7 _H | Data register 6 (8 bytes) | DTR6 | R/W | XXXXXXXX _B to XXXXXXXX _B |
| 003AB8 _H to 003ABF _H | 003BB8 _H to 003BBF _H | 0037B8 _H to 0037BF _H | 0038B8 _H to 0038BF _H | Data register 7 (8 bytes) | DTR7 | R/W | XXXXXXXX _B to XXXXXXXX _B |
| 003AC0 _H to 003AC7 _H | 003BC0 _H to 003BC7 _H | 0037C0 _H to 0037C7 _H | 0038C0 _H to 0038C7 _H | Data register 8 (8 bytes) | DTR8 | R/W | XXXXXXXX _B to XXXXXXXX _B |
| 003AC8 _H to 003ACF _H | 003BC8 _H to 003BCF _H | 0037C8 _H to 0037CF _H | 0038C8 _H to 0038CF _H | Data register 9 (8 bytes) | DTR9 | R/W | XXXXXXXX _B to XXXXXXXX _B |
| 003AD0 _H to 003AD7 _H | 003BD0 _H to 003BD7 _H | 0037D0 _H to 0037D7 _H | 0038D0 _H to 0038D7 _H | Data register 10 (8 bytes) | DTR10 | R/W | XXXXXXXX _B to XXXXXXXX _B |
| 003AD8 _H to 003ADF _H | 003BD8 _H to 003BDF _H | 0037D8 _H to 0037DF _H | 0038D8 _H to 0038DF _H | Data register 11 (8 bytes) | DTR11 | R/W | XXXXXXXX _B to XXXXXXXX _B |
| 003AE0 _H to 003AE7 _H | 003BE0 _H to 003BE7 _H | 0037E0 _H to 0037E7 _H | 0038E0 _H to 0038E7 _H | Data register 12 (8 bytes) | DTR12 | R/W | XXXXXXXX _B to XXXXXXXX _B |
| 003AE8 _H to 003AEF _H | 003BE8 _H to 003BEF _H | 0037E8 _H to 0037EF _H | 0038E8 _H to 0038EF _H | Data register 13 (8 bytes) | DTR13 | R/W | XXXXXXXX _B to XXXXXXXX _B |
| 003AF0 _H to 003AF7 _H | 003BF0 _H to 003BF7 _H | 0037F0 _H to 0037F7 _H | 0038F0 _H to 0038F7 _H | Data register 14 (8 bytes) | DTR14 | R/W | XXXXXXXX _B to XXXXXXXX _B |
| 003AF8 _H to 003AFF _H | 003BF8 _H to 003BFF _H | 0037F8 _H to 0037FF _H | 0038F8 _H to 0038FF _H | Data register 15 (8 bytes) | DTR15 | R/W | XXXXXXXX _B to XXXXXXXX _B |

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| Interrupt source | EI ² OS corresponding | Interrupt vector | | | Interrupt control register | | Priority ^{*2} |
|----------------------------------|----------------------------------|------------------|-----------------|---------------------|----------------------------|-----------------------------------|------------------------|
| | | Number | Address | Address | ICR | Address | |
| UART 1 RX | ◎ | #37 | 25 _H | FFFF68 _H | ICR13 | 0000BD _H ^{*1} | High ↑ ↓ Low |
| UART 1 TX | △ | #38 | 26 _H | FFFF64 _H | | | |
| UART 0 RX | ◎ | #39 | 27 _H | FFFF60 _H | ICR14 | 0000BE _H ^{*1} | |
| UART 0 TX | △ | #40 | 28 _H | FFFF5C _H | | | |
| Flash memory status | × | #41 | 29 _H | FFFF58 _H | ICR15 | 0000BF _H ^{*1} | |
| Delay interrupt generator module | × | #42 | 2A _H | FFFF54 _H | | | |

◎ : Usable, and has expanded intelligent I/O services (EI²OS) stop function

○ : Usable

△ : Usable when interrupt sources sharing ICR are not in use

×

*1 : • Peripheral functions that share the ICR register have the same interrupt level.

• If the expanded intelligent I/O service (EI²OS) is used with peripheral functions that share the ICR register, only one of the peripheral functions that share the register can be used.

• When the expanded intelligent I/O service (EI²OS) is specified for one of the peripheral functions that shares the ICR register, interrupts cannot be used from the other peripheral functions that share the register.

*2 : Priority applies when interrupts of the same level are generated.

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

| Parameter | Symbol | Rating | | Unit | Remarks |
|--|------------------------|-----------------------|-----------------------|------|---------------------------------------|
| | | Min | Max | | |
| Power supply voltage*1 | V _{CC} | V _{SS} - 0.3 | V _{SS} + 6.0 | V | |
| | AV _{CC} | V _{SS} - 0.3 | V _{SS} + 6.0 | V | AV _{CC} = V _{CC} *2 |
| | AVRH | V _{SS} - 0.3 | V _{SS} + 6.0 | V | AV _{CC} ≥ AVRH*2 |
| | DV _{CC} | V _{SS} - 0.3 | V _{SS} + 6.0 | V | DV _{CC} = V _{CC} *2 |
| Input voltage*1 | V _I | V _{SS} - 0.3 | V _{CC} + 0.3 | V | *3 |
| Output voltage*1 | V _O | V _{SS} - 0.3 | V _{CC} + 0.3 | V | |
| Maximum clamp current | I _{CLAMP} | - 4 | + 4 | mA | *7 |
| Total maximum clamp current | Σ I _{CLAMP} | — | 40 | mA | *7 |
| “L” level maximum output current*4 | I _{OL1} | — | 15 | mA | Except P70 to P77 and P80 to P87 |
| | I _{OL2} | — | 40 | mA | P70 to P77 and P80 to P87 |
| “L” level average output current*5 | I _{OLAV1} | — | 4 | mA | Except P70 to P77 and P80 to P87 |
| | I _{OLAV2} | — | 30 | mA | P70 to P77 and P80 to P87 |
| “L” level maximum total output current | ΣI _{OL1} | — | 100 | mA | Except P70 to P77 and P80 to P87 |
| | ΣI _{OL2} | — | 330 | mA | P70 to P77 and P80 to P87 |
| “L” level average total output current | ΣI _{OLAV1} | — | 50 | mA | Except P70 to P77 and P80 to P87 |
| | ΣI _{OLAV2} | — | 250 | mA | P70 to P77 and P80 to P87 |
| “H” level maximum output current | I _{OH1} *4 | — | -15 | mA | Except P70 to P77 and P80 to P87 |
| | I _{OH2} *4 | — | -40 | mA | P70 to P77 and P80 to P87 |
| “H” level average output current | I _{OHAV1} *5 | — | -4 | mA | Except P70 to P77 and P80 to P87 |
| | I _{OHAV2} *5 | — | -30 | mA | P70 to P77 and P80 to P87 |
| “H” level maximum total output current | ΣI _{OH1} | — | -100 | mA | Except P70 to P77 and P80 to P87 |
| | ΣI _{OH2} | — | -330 | mA | P70 to P77 and P80 to P87 |
| “H” level average total output current | ΣI _{OHAV1} *6 | — | -50 | mA | Except P70 to P77 and P80 to P87 |
| | ΣI _{OHAV2} *6 | — | -250 | mA | P70 to P77 and P80 to P87 |
| Power consumption | P _D | — | 625 | mW | |
| Operating temperature | T _A | - 40 | + 105 | °C | |
| Storage temperature | T _{STG} | - 55 | + 150 | °C | |

*1 : The parameter is based on V_{SS} = AV_{SS} = DV_{SS} = 0.0 V.

*2 : AV_{CC}, AVRH must not exceed V_{CC}, and AVRH must not exceed AV_{CC}.

When using an evaluation product, DV_{CC} must not exceed V_{CC} (however, DV_{CC} can be set to a higher voltage than V_{CC} when using a Flash memory product).

*3 : If the input current or the maximum input current is limited using external components, I_{CLAMP} is the applicable rating instead of V_I.

*4 : Maximum output current is defined as the peak value of current through any one of the corresponding pins.

(Continued)

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(Continued)

- *5 : Average output current is defined as the average value of the current flowing through any one of the corresponding pins within a period of 100 ms. The “average value” can be calculated by multiplying the “operating current” by the “operating factor”.
- *6 : Average total output current is defined as the average value of the current flowing through all of the corresponding pins within a period of 100 ms. The “average value” can be calculated by multiplying the “operating current” by the “operating factor”.
- *7 :
 - Applicable to pins: P10 to P15, P50 to P57, P60 to P67, P70 to P77, P80 to P87, PC0 to PC7, PD0 to PD6, PE0 to PE2
 - Use within recommended operating conditions.
 - Use at DC voltage (current) .
 - The +B signal should always be applied with a limiting resistance placed between the +B signal and the microcontroller.
 - The value of the limiting resistance should be set so that when the +B signal is applied, the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
 - Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the V_{CC} pin, and this may affect other devices.
 - Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0 V) , the microcontroller may partially malfunction on power supplied through the +B signal pin.
 - Note that if the +B input is applied during power-on, the power supply voltage may reach a level such that the power-on reset does not function due to the power supplied from the +B signal.
 - Care must be taken not to leave +B input pins open.
 - Note that analog system input/output pins (LCD drive pins, comparator input pins, etc.) cannot accept +B signal inputs.
 - Sample recommended circuit :



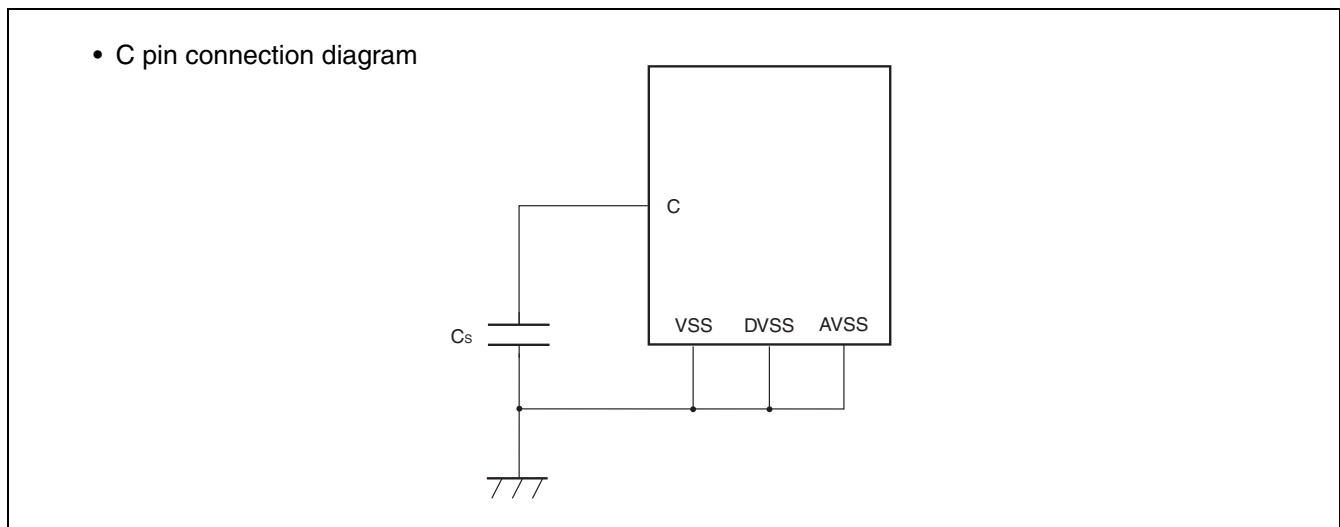
WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended Operating Conditions

($V_{SS} = DV_{SS} = AV_{SS} = 0.0\text{ V}$)

| Parameter | Symbol | Value | | Unit | Remarks |
|-----------------------|------------------------|-------|------|--------------------|--|
| | | Min | Max | | |
| Power supply voltage | V_{CC} | 4.0 | 5.5 | V | The low voltage detection reset operates when the power supply voltage reaches $4.2\text{ V} \pm 0.2\text{ V}$. |
| | AV_{CC} DV_{CC} | 4.4 | 5.5 | V | Maintain stop operation status The low voltage detection reset operates when the power supply voltage reaches $4.2\text{ V} \pm 0.2\text{ V}$. |
| Smoothing capacitor* | C_s | 0.1 | 1.0 | μF | Use a ceramic capacitor or other capacitor of equivalent frequency characteristics. Use a capacitor with a capacitance greater than this capacitor as the bypass capacitor for the V_{CC} pin. |
| Operating temperature | T_A | -40 | +105 | $^{\circ}\text{C}$ | |

* : Refer to the following diagram for details on the connection of the smoothing capacitor C_s .



WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

MB90920 Series

3. DC Characteristics

($V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = DV_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^\circ\text{C}$ to $+105\text{ }^\circ\text{C}$)

| Parameter | Symbol | Pin name | Conditions | Value | | | Unit | Remarks |
|-------------------------|--------------|----------|---|--------------|-----|--------------|---------------|---|
| | | | | Min | Typ | Max | | |
| “H” level input voltage | V_{IHA} | — | — | $0.8 V_{CC}$ | — | — | V | Pin inputs if Automotive input levels are selected |
| | V_{IHS} | — | — | $0.8 V_{CC}$ | — | — | V | Pin inputs if CMOS hysteresis input levels are selected |
| | V_{IHC} | — | — | $0.7 V_{CC}$ | — | — | V | $\overline{\text{RST}}$ input pin (CMOS hysteresis) |
| “L” level input voltage | V_{ILA} | — | — | — | — | $0.5 V_{CC}$ | V | Pin inputs if Automotive input levels are selected |
| | V_{ILS} | — | — | — | — | $0.2 V_{CC}$ | V | Pin inputs if CMOS hysteresis input levels are selected |
| | V_{ILR} | — | — | — | — | $0.3 V_{CC}$ | V | $\overline{\text{RST}}$ input pin (CMOS hysteresis) |
| Powersupply current* | I_{CC} | V_{CC} | Maximum operating frequency $F_{CP} = 32\text{ MHz}$, normal operation | — | 35 | 45 | mA | |
| | | | Maximum operating frequency $F_{CP} = 32\text{ MHz}$, writing Flash memory | — | 55 | 65 | mA | |
| | I_{CCS} | | Operating frequency $F_{CP} = 32\text{ MHz}$, sleep mode | — | 13 | 20 | mA | |
| | I_{CTS} | | Operating frequency $F_{CP} = 2\text{ MHz}$, time-base timer mode | — | 0.6 | 1.0 | mA | |
| | I_{CTSPLL} | | Operating frequency $F_{CP} = 32\text{ MHz}$, PLL timer mode, External frequency = 4 MHz | — | 2.5 | 4 | mA | |
| | I_{CCL} | | Operating frequency $F_{CP} = 8\text{ kHz}$, $T_A = +25\text{ }^\circ\text{C}$, sub clock operation | — | 120 | 270 | μA | |
| | I_{CCLS} | | Operating frequency $F_{CP} = 8\text{ kHz}$, $T_A = +25\text{ }^\circ\text{C}$, sub sleep operation | — | 100 | 200 | μA | |
| | I_{CCT} | | Operating frequency $F_{CP} = 8\text{ kHz}$, $T_A = +25\text{ }^\circ\text{C}$, watch mode | — | 90 | 180 | μA | |
| | I_{CCH} | | $T_A = +25\text{ }^\circ\text{C}$, stop mode | — | 80 | 170 | μA | |

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MB90920 Series

($V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = DV_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^\circ\text{C}$ to $+105\text{ }^\circ\text{C}$)

| Parameter | Symbol | Pin name | Conditions | Value | | | Unit | Remarks |
|---|-----------------|---|--|----------------|------|------|---------------|--------------------------------|
| | | | | Min | Typ | Max | | |
| Input leakage current | I_{IL} | All input pins | $V_{CC} = DV_{CC} = AV_{CC} = 5.5\text{ V}$, $V_{SS} < V_I < V_{CC}$ | — | — | 10 | μA | |
| Input capacitance 1 | C_{IN1} | All pins except VCC, VSS, DVCC, DVSS, AVCC, AVSS, C, P70 to P77, P80 to P87 | — | — | — | 15 | pF | |
| Input capacitance 2 | C_{IN2} | P70 to P77, P80 to P87 | — | — | — | 45 | pF | |
| Pull-up resistance | R_{UP} | \overline{RST} | — | 25 | 50 | 100 | k Ω | |
| Pull-down resistance | R_{DOWN} | MD2 | — | — | — | 100 | k Ω | Excluding Flash memory product |
| General-purpose output "H" voltage | V_{OH1} | All pins except P70 to P77, P80 to P87 | $V_{CC} = 4.5\text{ V}$, $I_{OH} = -4.0\text{ mA}$ | $V_{CC} - 0.5$ | — | — | V | |
| Stepping motor output "H" voltage | V_{OH2} | P70 to P77, P80 to P87 | $V_{CC} = 4.5\text{ V}$, $I_{OH} = -30.0\text{ mA}$ | $V_{CC} - 0.5$ | — | — | V | |
| General-purpose output "L" voltage | V_{OL1} | All pins except P70 to P77, P80 to P87 | $V_{CC} = 4.5\text{ V}$, $I_{OL} = 4.0\text{ mA}$ | — | — | 0.4 | V | |
| Stepping motor output "L" voltage | V_{OL2} | P70 to P77, P80 to P87 | $V_{CC} = 4.5\text{ V}$, $I_{OL} = 30.0\text{ mA}$ | — | — | 0.55 | V | |
| Stepping motor output phase variation "H" | ΔV_{OH} | PWM1Pn, PWM1Mn, PWM2Pn, PWM2Mn, n = 0 to 3 | $V_{CC} = 4.5\text{ V}$, $I_{OH} = -30.0\text{ mA}$, maximum deviation V_{OH2} | — | — | 90 | mV | |
| Stepping motor output phase variation "L" | ΔV_{OL} | PWM1Pn, PWM1Mn, PWM2Pn, PWM2Mn, n = 0 to 3 | $V_{CC} = 4.5\text{ V}$, $I_{OL} = 30.0\text{ mA}$, maximum deviation V_{OH2} | — | — | 90 | mV | |
| LCD internal divider resistance | R_{LCD} | Between V0 and V1, Between V1 and V2, Between V2 and V3 | — | 50 | 100 | 200 | k Ω | Evaluation product |
| | | | | 8.75 | 12.5 | 17.0 | k Ω | Flash memory product |

(Continued)

MB90920 Series

(Continued)

($V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = DV_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^\circ\text{C}$ to $+105\text{ }^\circ\text{C}$)

| Parameter | Symbol | Pin name | Conditions | Value | | | Unit | Remarks |
|----------------------|------------|--|------------|-------|-----|-----|------------------|---------|
| | | | | Min | Typ | Max | | |
| LCDC leakage current | I_{LCDC} | V0 to V3, COMm (m = 0 to 3) , SEgn, (n = 00 to 31) | — | — | — | 5.0 | μA | |
| LCD output impedance | R_{vcom} | COMn (n = 0 to 3) | — | — | — | 4.5 | $\text{k}\Omega$ | |
| | R_{vseg} | SEgn (n = 00 to 31) | — | — | — | 17 | $\text{k}\Omega$ | |

* : Power supply current values assume an external clock supplied to the X1 pin and X1A pin. Users must be aware that power supply current levels differ depending on whether an external clock or oscillator is used.

4. AC Characteristics

(1) Clock timing

($V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = DV_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^\circ\text{C}$ to $+105\text{ }^\circ\text{C}$)

| Parameter | Symbol | Pin name | Condi- tions | Value | | | Unit | Remarks |
|-------------------------------------|-------------------------------------|----------|-----------------|--------|-------|---------------------|------|--|
| | | | | Min | Typ | Max | | |
| Clock frequency | F _C | X0, X1 | — | 3 | — | 16 | MHz | 1/2 (PLL stopped) When using the oscillator circuit |
| | | | | 3 | — | 32 | MHz | 1/2 (PLL stopped) When using an external clock |
| | | | | 4 | — | 32 | MHz | PLL multiplied by 1 |
| | | | | 3 | — | 16 | MHz | PLL multiplied by 2 |
| | | | | 3 | — | 10.7 | MHz | PLL multiplied by 3 |
| | | | | 3 | — | 8 | MHz | PLL multiplied by 4 |
| | | | | 3 | — | 5.33 | MHz | PLL multiplied by 6 |
| | 3 | — | | 4 | MHz | PLL multiplied by 8 | | |
| | F _{LC} | X0A, X1A | — | 32.768 | — | kHz | | |
| Clock cycle time | t _{CYL} | X0, X1 | — | 62.5 | — | 333 | ns | When using an oscillator |
| | | | — | 31.25 | — | 333 | ns | External clock input |
| | t _{LCYL} | X0A, X1A | — | 30.5 | — | — | μs | |
| Input clock pulse width | P _{WH} , P _{WL} | X0 | — | 5 | — | — | ns | Use duty ratio of 50% ± 3% as a guideline |
| | P _{WLH} , P _{WLL} | X0A | — | — | 15.2 | — | μs | |
| Input clock rise and fall time | t _{cr} , t _{cf} | X0 | — | — | 5 | — | ns | When using an external clock signal |
| Internal operating clock frequency | F _{CP} | — | — | 1.5 | — | 32 | MHz | Using main clock (PLL clock) |
| | F _{LCP} | — | — | — | 8.192 | — | kHz | Using sub clock |
| Internal operating clock cycle time | t _{CP} | — | — | 31.25 | — | 666 | ns | Using main clock (PLL clock) |
| | t _{LCP} | — | — | — | 122.1 | — | μs | Using sub clock |

MB90920 Series

- X0, X1 clock timing



- X0A, X1A clock timing



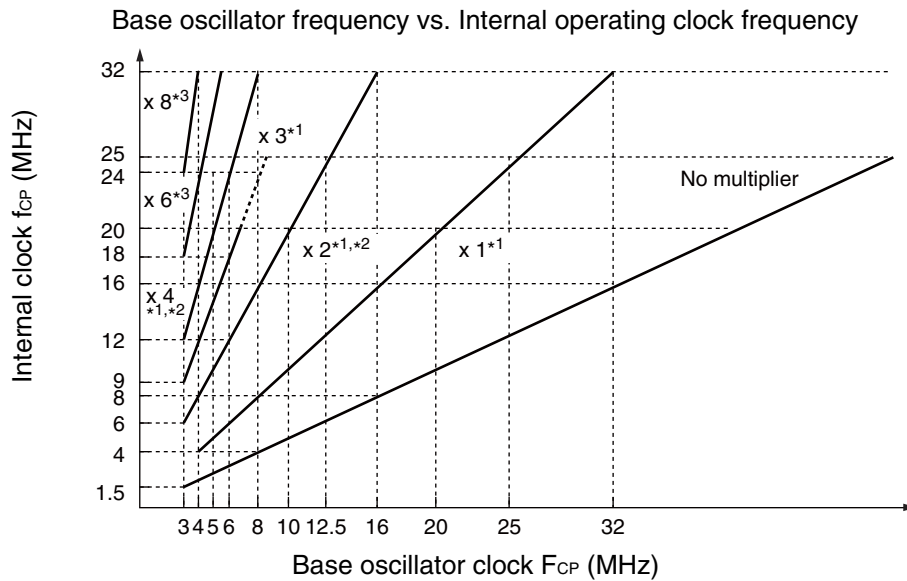
• Guaranteed PLL Operation Range



- Notes :
- For PLL 1 \times only, use with $t_{cp} = 4$ MHz or greater.
 - Refer to "5. A/D Converter (1) Electrical Characteristics" for details on the A/D converter operating frequency.

(Continued)

(Continued)



*1 : When the PLL multiplier is $\times 1$, $\times 2$, $\times 3$ or $\times 4$ and the internal clock is $20 \text{ MHz} < f_{CP} \leq 32 \text{ MHz}$, set DIV2 bit = "1"*4, CS2 bit = "1" in the PSCCR register.

[Example] When using a base oscillator frequency of 24 MHz at PLL $\times 1$:

CKSCR register : CS1 bit = "0", CS0 bit = "0"

PSCCR register : DIV2 bit = "1"*4, CS2 bit = "1"

[Example] When using a base oscillator frequency of 6 MHz at PLL $\times 3$:

CKSCR register : CS1 bit = "1", CS0 bit = "0"

PSCCR register : DIV2 bit = "1"*4, CS2 bit = "1"

*2 : When the PLL multiplier is $\times 2$ or $\times 4$ and the internal clock is $20 \text{ MHz} < f_{CP} \leq 32 \text{ MHz}$, the following settings are also supported.

PLL $\times 2$: CKSCR register : CS1 bit = "0", CS0 bit = "0"

PSCCR register : DIV2 bit = "0"*4, CS2 bit = "0"

PLL $\times 4$: CKSCR register : CS1 bit = "0", CS0 bit = "1"

PSCCR register : DIV2 bit = "0"*4, CS2 bit = "0"

*3 : When the PLL multiplier is set to $\times 6$ or $\times 8$ set "DIV2 bit = "0"*4 CS2 bit = "1" and "PLL2 bit = 1" in the PSCCR register.

[Example] When using a base oscillator frequency of 4 MHz at PLL $\times 6$:

CKSCR register : CS1 bit = "1", CS0 bit = "0"

PLLOS register : DIV2 bit = "0"*4, CS2 bit = "1"

[Example] When using a base oscillator frequency of 3 MHz at PLL $\times 8$:

CKSCR register : CS1 bit = "1", CS0 bit = "1"

PLLOS register : DIV2 bit = "0"*4, CS2 bit = "1"

*4 : The DIV2 bit is assigned to bit 9 of the PSCCR register and the CS2 bit is assigned to bit 8 of the PSCCR register. Both bits have a default value of "0".

(2) Reset input

($V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^\circ\text{C}$ to $+105\text{ }^\circ\text{C}$)

| Parameter | Symbol | Pin name | Value | | Unit | Remarks |
|------------------|------------|------------------|--|-----|---------------|--|
| | | | Min | Max | | |
| Reset input time | t_{RSTL} | \overline{RST} | 500 | — | ns | During normal operation |
| | | | Oscillator oscillation time* + 16 t_{CP} | — | ms | In stop mode, sub clock mode, sub sleep mode, and watch mode |
| | | | 100 | — | μs | In time-base timer mode |

*: The oscillation time of the oscillator is the time taken to reach 90% of the amplitude. The oscillation time of a crystal oscillator is between several ms and tens of ms. The oscillation time of a ceramic oscillator is between hundreds of μs and several ms. The oscillation time of an external clock is 0 ms.

Note : t_{CP} is the internal operating clock cycle time. (Unit : ns)

- During normal operation



- In stop mode, sub clock mode, sub sleep mode, watch mode, and power-on



MB90920 Series

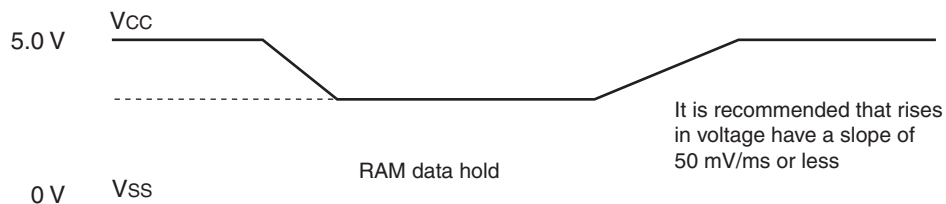
(3) Power-on reset

($V_{CC} = 2.7\text{ V to }3.6\text{ V}$, $V_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^\circ\text{C to }+105\text{ }^\circ\text{C}$)

| Parameter | Symbol | Pin name | Conditions | Value | | Unit | Remarks |
|------------------------|-----------|----------|------------|-------|-----|------|-----------------------------|
| | | | | Min | Max | | |
| Power supply rise time | t_R | VCC | — | 0.05 | 30 | ms | |
| Power off time | t_{OFF} | | | 1 | — | ms | Waiting time until power-on |



Note : Extreme variations in power supply voltage may trigger a power-on reset. When the power supply voltage is changed during operation, it is recommended that increases in the voltage smoothed out as shown in the following diagram. The PLL clock of the device should not be in use when varying the voltage. However, the PLL clock may continue to be used if the rate of the voltage drop is 1 V/s or less.



(4) UART0/1/2/3 (LIN/SCI)

- Bit setting: ESCR0/1/2/3:SCES=0, ECCR0/1/2/3:SCDE=0

($V_{CC} = 5.0 V \pm 10\%$, $V_{SS} = AV_{SS} = 0.0 V$, $T_A = -40\text{ }^\circ\text{C}$ to $+105\text{ }^\circ\text{C}$)

| Parameter | Symbol | Pin name | Conditions | Value | | Unit |
|------------------------------|-------------|-------------------------------|--|------------------|-----------------|------|
| | | | | Min | Max | |
| Serial clock cycle time | t_{SCYC} | SCK0 to SCK3 | Internal shift clock mode output pin $C_L = 80\text{ pF} + 1\text{TTL}$ | $5 t_{CP}$ | — | ns |
| SCK ↓ → SOT delay time | t_{SLOVI} | SCK0 to SCK3, SOT0 to SOT3 | | - 50 | + 50 | ns |
| Valid SIN → SCK ↑ | t_{IVSHI} | SCK0 to SCK3, SIN0 to SIN3 | | $t_{CP} + 80$ | — | ns |
| SCK ↑ → valid SIN hold time | t_{SHIXI} | | | 0 | — | ns |
| Serial clock "L" pulse width | t_{SLSH} | SCK0 to SCK3 | External shift clock mode output pin $C_L = 80\text{ pF} + 1\text{TTL}$ | $3 t_{CP} - t_R$ | — | ns |
| Serial clock "H" pulse width | t_{SHSL} | | | $t_{CP} + 10$ | — | ns |
| SCK ↓ → SOT delay time | t_{SLOVE} | SCK0 to SCK3, SOT0 to SOT3 | | — | $2 t_{CP} + 60$ | ns |
| Valid SIN → SCK ↑ | t_{IVSHE} | SCK0 to SCK3, SIN0 to SIN3 | | 30 | — | ns |
| SCK ↑ → valid SIN hold time | t_{SHIXE} | | | $t_{CP} + 30$ | — | ns |
| SCK ↓ time | t_F | SCK0 to SCK3 | | — | 10 | ns |
| SCK ↑ time | t_R | | | — | 10 | ns |

Notes : • Depending on the machine clock frequency to be used, the maximum baud rate may be limited by some parameters. These parameters are shown in "MB90920 series hardware manual".

- C_L is the load capacitance connected to the pin during testing.
- t_{CP} is the internal operating clock cycle time. Refer to "(1) Clock timing".

- Internal shift clock mode



- External shift clock mode



MB90920 Series

• Bit setting: ESCR0/1/2/3:SCES=1, ECCR0/1/2/3:SCDE=0

($V_{CC} = 5.0 V \pm 10\%$, $V_{SS} = AV_{SS} = 0.0 V$, $T_A = -40\text{ }^\circ\text{C}$ to $+105\text{ }^\circ\text{C}$)

| Parameter | Symbol | Pin name | Conditions | Value | | Unit |
|--|-------------|-------------------------------|--|------------------|-----------------|------|
| | | | | Min | Max | |
| Serial clock cycle time | t_{SCYC} | SCK0 to SCK3 | Internal shift clock mode output pin $C_L = 80\text{ pF} + 1\text{TTL}$ | $5 t_{CP}$ | — | ns |
| SCK \uparrow \rightarrow SOT delay time | t_{SHOVI} | SCK0 to SCK3, SOT0 to SOT3 | | - 50 | + 50 | ns |
| Valid SIN \rightarrow SCK \downarrow | t_{IVSLI} | SCK0 to SCK3, SIN0 to SIN3 | | $t_{CP} + 80$ | — | ns |
| SCK \downarrow \rightarrow valid SIN hold time | t_{SLIXI} | | | 0 | — | ns |
| Serial clock "H" pulse width | t_{SHSL} | SCK0 to SCK3 | External shift clock mode output pin $C_L = 80\text{ pF} + 1\text{TTL}$ | $3 t_{CP} - t_R$ | — | ns |
| Serial clock "L" pulse width | t_{SLSH} | | | $t_{CP} + 10$ | — | ns |
| SCK \uparrow \rightarrow SOT delay time | t_{SHOVE} | SCK0 to SCK3, SOT0 to SOT3 | | — | $2 t_{CP} + 60$ | ns |
| Valid SIN \rightarrow SCK \downarrow | t_{IVSLE} | SCK0 to SCK3, SIN0 to SIN3 | | 30 | — | ns |
| SCK \downarrow \rightarrow valid SIN hold time | t_{SLIXE} | | | $t_{CP} + 30$ | — | ns |
| SCK \downarrow time | t_F | SCK0 to SCK3 | | — | 10 | ns |
| SCK \uparrow time | t_R | | | — | 10 | ns |

Notes : • Depending on the machine clock frequency to be used, the maximum baud rate may be limited by some parameters. These parameters are shown in "MB90920 series hardware manual".

- C_L is the load capacitance connected to the pin during testing.
- t_{CP} is the internal operating clock cycle time. Refer to "(1) Clock timing".

- Internal shift clock mode



- External shift clock mode



MB90920 Series

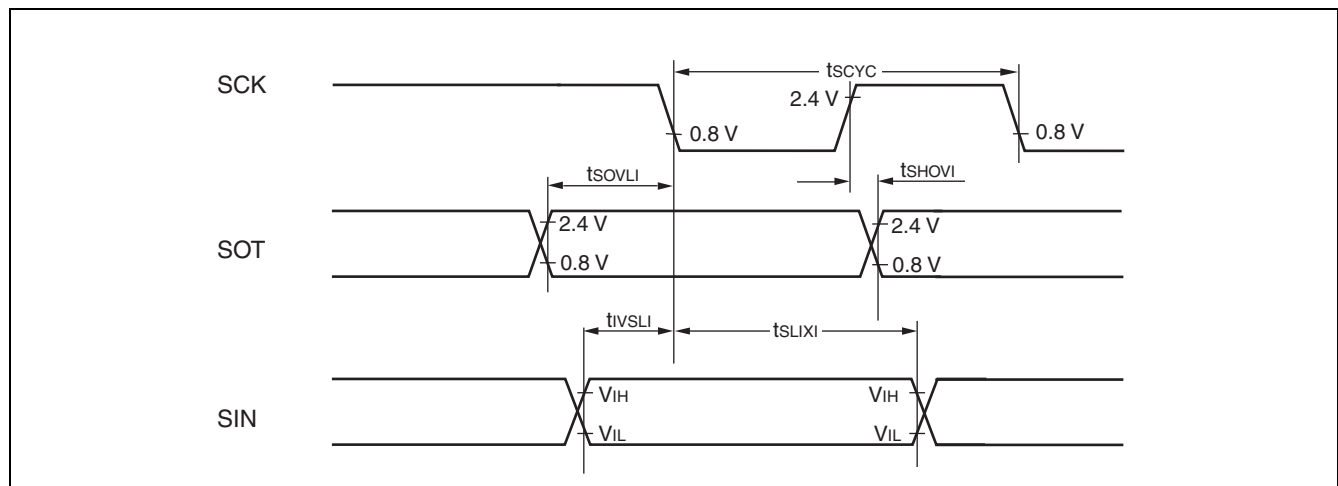
- Bit setting: ESCR0/1/2/3:SCES=0, ECCR0/1/2/3:SCDE=1

($V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^\circ\text{C}$ to $+105\text{ }^\circ\text{C}$)

| Parameter | Symbol | Pin name | Conditions | Value | | Unit |
|--|-------------|-------------------------------|---|-----------------|------|------|
| | | | | Min | Max | |
| Serial clock cycle time | t_{SCYC} | SCK0 to SCK3 | Internal shift clock mode output pin $C_L = 80\text{ pF} + 1\text{ TTL}$ | $5 t_{CP}$ | — | ns |
| SCK \uparrow \rightarrow SOT delay time | t_{SHOVI} | SCK0 to SCK3, SOT0 to SOT3 | | - 50 | + 50 | ns |
| Valid SIN \rightarrow SCK \downarrow | t_{IVSLI} | SCK0 to SCK3, SIN0 to SIN3 | | $t_{CP} + 80$ | — | ns |
| SCK \downarrow \rightarrow valid SIN hold time | t_{SLIXI} | | | 0 | — | ns |
| SOT \rightarrow SCK \downarrow delay time | t_{SOVLI} | SCK0 to SCK3, SOT0 to SOT3 | | $3 t_{CP} - 70$ | — | ns |

Notes : • Depending on the machine clock frequency to be used, the maximum baud rate may be limited by some parameters. These parameters are shown in “MB90920 series hardware manual”.

- C_L is the load capacitance connected to the pin during testing.
- t_{CP} is the internal operating clock cycle time. Refer to “(1) Clock timing”.



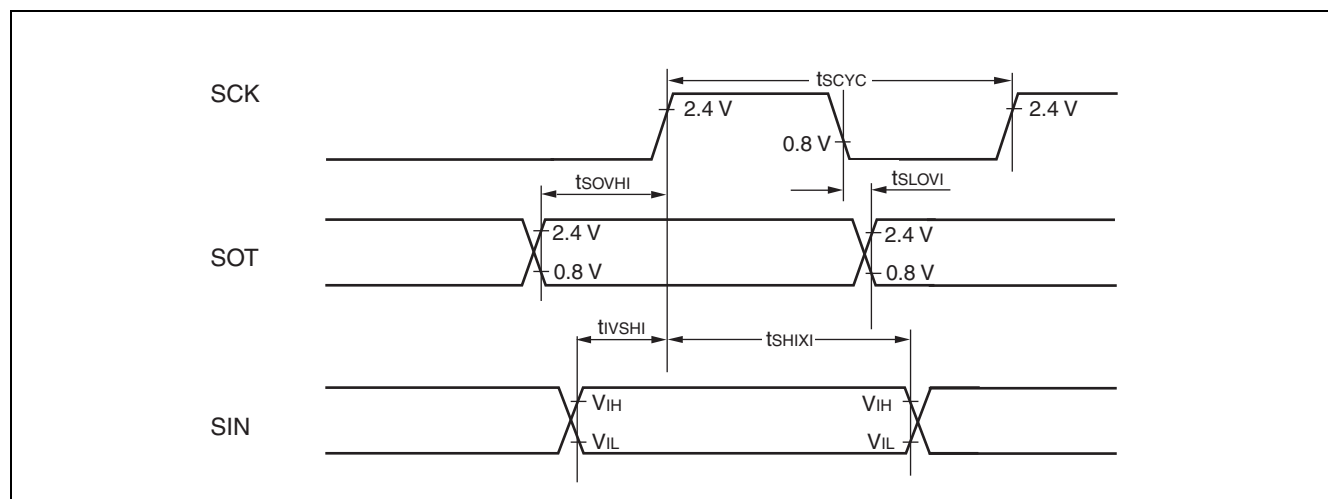
MB90920 Series

- Bit setting: ESCR0/1/2/3:SCES=1, ECCR0/1/2/3:SCDE=1

($V_{CC} = 5.0 \text{ V} \pm 10\%$, $V_{SS} = AV_{SS} = 0.0 \text{ V}$, $T_A = -40 \text{ }^\circ\text{C}$ to $+105 \text{ }^\circ\text{C}$)

| Parameter | Symbol | Pin name | Conditions | Value | | Unit |
|-----------------------------|-------------|-------------------------------|---|-----------------|------|------|
| | | | | Min | Max | |
| Serial clock cycle time | t_{SCYC} | SCK0 to SCK3 | Internal shift clock mode output pin $C_L = 80 \text{ pF} + 1\text{TTL}$ | $5 t_{CP}$ | — | ns |
| SCK ↓ → SOT delay time | t_{SLOVI} | SCK0 to SCK3, SOT0 to SOT3 | | - 50 | + 50 | ns |
| Valid SIN → SCK ↓ | t_{IVSHI} | SCK0 to SCK3, SIN0 to SIN3 | | $t_{CP} + 80$ | — | ns |
| SCK ↑ → valid SIN hold time | t_{SHIXI} | SCK0 to SCK3, SIN0 to SIN3 | | 0 | — | ns |
| SOT → SCK ↑ delay time | t_{SOVHI} | SCK0 to SCK3, SOT0 to SOT3 | | $3 t_{CP} - 70$ | — | ns |

- Notes :
- Depending on the machine clock frequency to be used, the maximum baud rate may be limited by some parameters. These parameters are shown in “MB90920 series hardware manual”.
 - C_L is the load capacitance connected to the pin during testing.
 - t_{CP} is the internal operating clock cycle time. Refer to “(1) Clock timing”.



(5) Timer input timing

($V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^\circ\text{C}$ to $+105\text{ }^\circ\text{C}$)

| Parameter | Symbol | Pin name | Conditions | Value | | Unit |
|-------------------|--------------------------|---------------------------|------------|------------|-----|------|
| | | | | Min | Max | |
| Input pulse width | t_{TIWH} t_{TIWL} | TIN0, TIN1, IN0 to IN3 | — | 4 t_{CP} | — | ns |

Note : t_{CP} is the internal operating clock cycle time. Refer to “(1) Clock timing”.

- Timer input timing



MB90920 Series

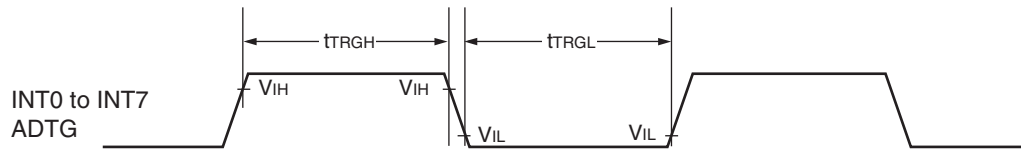
(6) Trigger input timing

($V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^\circ\text{C}$ to $+105\text{ }^\circ\text{C}$)

| Parameter | Symbol | Pin name | Conditions | Value | | Unit | Remarks |
|-------------------|----------------------------|--------------|------------|----------------|-----|------|-------------------------|
| | | | | Min | Max | | |
| Input pulse width | t_{TRGH} , t_{TRGL} | INT0 to INT7 | — | 200 | — | ns | During normal operation |
| | | ADTG | — | $t_{CP} + 200$ | — | ns | |

Note : t_{CP} is the internal operating clock cycle time. Refer to “(1) Clock timing”.

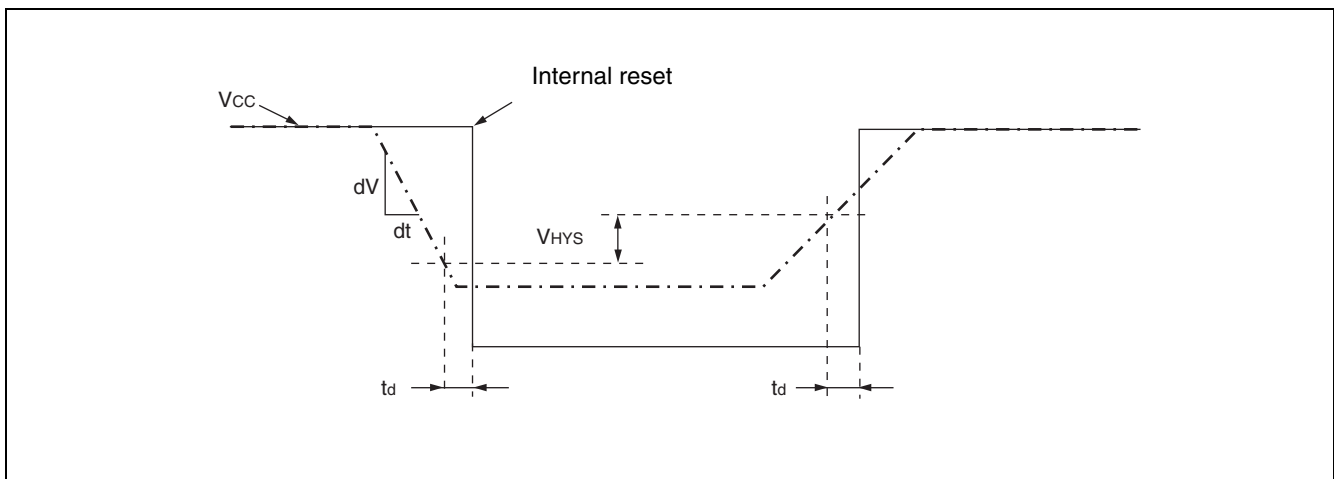
- Trigger input timing



(7) Low voltage detection

($V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^\circ\text{C}$ to $+105\text{ }^\circ\text{C}$)

| Parameter | Symbol | Pin name | Conditions | Value | | | Unit | Remarks |
|----------------------------------|-----------|----------|------------|--------|-----|--------|------------------|--|
| | | | | Min | Typ | Max | | |
| Detection voltage | V_{DL} | VCC | — | 4.0 | 4.2 | 4.4 | V | Flash memory product, during voltage drop |
| | | | | 3.7 | 4.0 | 4.3 | V | Evaluation product, during voltage drop |
| Hysteresis width | V_{HYS} | VCC | — | 190 | — | — | mV | Flash memory product, during voltage rise |
| | | | | 0.1 | — | — | V | Evaluation product, during voltage rise |
| Power supply voltage change rate | dV/dt | VCC | — | -0.1 | — | +0.1 | V/ μs | Flash memory product, dV/dt at low voltage reset |
| | | | | -0.004 | — | +0.004 | V/ μs | Flash memory product, dV/dt at standard value of low voltage detection/release voltage |
| | | | | -0.1 | — | +0.02 | V/ μs | Evaluation product |
| Detection delay time | t_d | — | — | — | — | 3.2 | μs | Flash memory product, when $dV/dt \leq 0.004\text{ V}/\mu\text{s}$ |
| | | | | — | — | 35 | μs | Evaluation product |



MB90920 Series

5. A/D Converter

(1) Electrical Characteristics

($V_{CC} = AV_{CC} = AVRH = 4.0\text{ V to }5.5\text{ V}$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C to }+105\text{ }^{\circ}\text{C}$)

| Parameter | Symbol | Pin name | Value | | | Unit | Remarks |
|----------------------------------|-----------|------------|----------------------------|----------------------------|----------------------------|---------------|---|
| | | | Min | Typ | Max | | |
| Resolution | — | — | — | — | 10 | bit | |
| Total error | — | — | - 3.0 | — | + 3.0 | LSB | |
| Non-linear error | — | — | - 2.5 | — | + 2.5 | LSB | |
| Differential linear error | — | — | - 1.9 | — | + 1.9 | LSB | |
| Zero transition voltage | V_{OT} | AN0 to AN7 | $AV_{SS} - 1.5\text{ LSB}$ | $AV_{SS} + 0.5\text{ LSB}$ | $AV_{SS} + 2.5\text{ LSB}$ | V | 1 LSB = ($AVRH - AV_{SS}$) / 1024 |
| Full scale transition voltage | V_{FST} | AN0 to AN7 | $AVRH - 3.5\text{ LSB}$ | $AVRH - 1.5\text{ LSB}$ | $AVRH + 0.5\text{ LSB}$ | V | |
| Sampling time | t_{SMP} | — | 0.4 | — | 16500 | μs | 4.5 V \leq $AV_{CC} \leq$ 5.5 V |
| | | | 1.0 | | | | 4.0 V \leq $AV_{CC} \leq$ 4.5 V |
| Compare time | t_{CMP} | — | 0.66 | — | — | μs | 4.5 V \leq $AV_{CC} \leq$ 5.5 V |
| | | | 2.2 | | | | 4.0 V \leq $AV_{CC} \leq$ 4.5 V |
| A/D conversion time | t_{CNV} | — | 1.44 | — | — | μs | *1 |
| Analog port input current | I_{AIN} | AN0 to AN7 | - 0.3 | — | + 10 | μA | |
| Analog input voltage | V_{AIN} | AN0 to AN7 | 0 | — | $AVRH$ | V | |
| Reference voltage | $AV+$ | $AVRH$ | $AV_{SS} + 2.7$ | — | AV_{CC} | V | |
| Power supply current | I_A | AV_{CC} | — | 2.3 | 6.0 | mA | |
| | I_{AH} | | — | — | 5 | μA | *2 |
| Reference voltage supply current | I_R | $AVRH$ | — | 520 | 900 | μA | $V_{AVRH} = 5.0\text{ V}$ |
| | I_{RH} | | — | — | 5 | μA | *2 |
| Inter-channel variation | — | AN0 to AN7 | — | — | 4 | LSB | |

*1 : The time per channel (4.5 V \leq $AV_{CC} \leq$ 5.5 V, and internal operating frequency = 32 MHz) .

*2 : Defined as supply current (when $V_{CC} = AV_{CC} = AVRH = 5.0\text{ V}$) with A/D converter not operating, and CPU in stop mode.

- **Notes on the external impedance and sampling time of analog inputs**

A/D converter with sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the internal sample and hold capacitor is insufficient, adversely affecting A/D conversion precision. Therefore, to satisfy the A/D conversion precision standard, consider the relationship between the external impedance and minimum sampling time and either adjust the register value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value. If the sampling time is still not sufficient, connect a capacitor of about 0.1 μF to the analog input pin.

- Analog input equivalent circuit



MB90F922NC/F922NCS/ F923NC/F923NCS/F924NC/F924NCS
MB90922NCS

| | R | C |
|--|-------------------------|--------------|
| $4.5 \text{ V} \leq AV_{\text{cc}} \leq 5.5 \text{ V}$ | : 2.6 k Ω (Max) | 8.5 pF (Max) |
| $4.0 \text{ V} \leq AV_{\text{cc}} \leq 4.5 \text{ V}$ | : 12.1 k Ω (Max) | 8.5 pF (Max) |

MB90V920-101/102

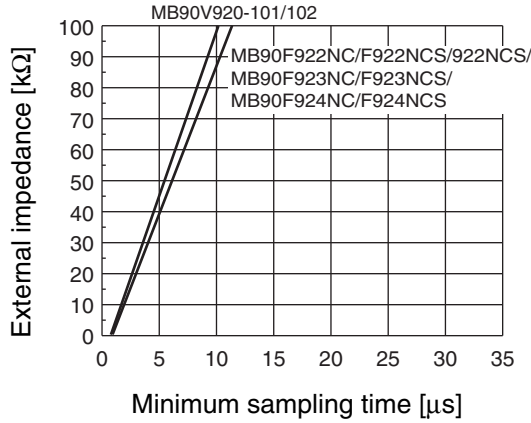
| | | |
|--|------------------------|---------------|
| $4.5 \text{ V} \leq AV_{\text{cc}} \leq 5.5 \text{ V}$ | : 2.0 k Ω (Max) | 14.4 pF (Max) |
| $4.0 \text{ V} \leq AV_{\text{cc}} \leq 4.5 \text{ V}$ | : 8.2 k Ω (Max) | 14.4 pF (Max) |

Note : The values are reference values.

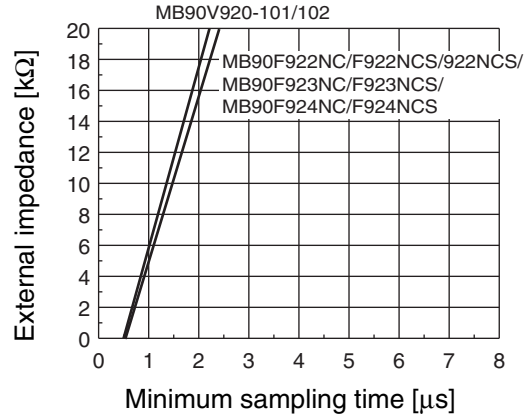
MB90920 Series

- The relationship between the external impedance and minimum sampling time
- At $4.5\text{ V} \leq AV_{CC} \leq 5.5\text{ V}$

(External impedance = 0 kΩ to 100 kΩ)

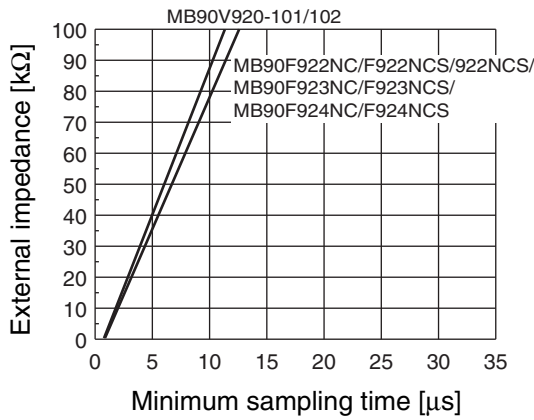


(External impedance = 0 kΩ to 20 kΩ)



- At $4.0\text{ V} \leq AV_{CC} \leq 4.5\text{ V}$

(External impedance = 0 kΩ to 100 kΩ)



(External impedance = 0 kΩ to 20 kΩ)



- About errors
As $|AV_{RH} - AV_{SS}|$ becomes smaller, the relative errors grow larger.

(2) Definition of terms

- Resolution : Analog changes that are identifiable by the A/D converter.
- Non-Linear error : The deviation of the straight line connecting the zero transition point (“00 0000 0000” ↔ “00 0000 0001”) with the full-scale transition point (“11 1111 1110” ↔ “11 1111 1111”) from actual conversion characteristics.
- Differential linear error : The deviation from the ideal value of the input voltage needed to change the output code by 1 LSB.
- Total error : The total error is the difference between the actual value and the theoretical value, and includes zero-transition error/full-scale transition error and linear error.



$$\text{Total error for digital output } N = \frac{V_{NT} - \{1 \text{ LSB} \times (N - 1) + 0.5 \text{ LSB}\}}{1 \text{ LSB}} \quad [\text{LSB}]$$

$$1 \text{ LSB (Ideal)} = \frac{AV_{RH} - AV_{SS}}{1024} \quad [\text{V}]$$

N : A/D converter digital output value

$$V_{OT} \text{ (Ideal)} = AV_{SS} + 0.5 \text{ LSB} \quad [\text{V}]$$

$$V_{FST} \text{ (Ideal)} = AV_{RH} - 1.5 \text{ LSB} \quad [\text{V}]$$

V_{NT} : Voltage when the digital output changes from (N - 1) to N

(Continued)

(Continued)



$$\text{Non-linear error of digital output } N = \frac{V_{NT} - \{1 \text{ LSB} \times (N - 1) + V_{OT}\}}{1 \text{ LSB}} \text{ [LSB]}$$

$$\text{Differential linear error of digital output } N = \frac{V_{(N+1)T} - V_{NT}}{1 \text{ LSB}} - 1 \text{ [LSB]}$$

$$1 \text{ LSB} = \frac{V_{FST} - V_{OT}}{1022} \text{ [V]}$$

N : A/D converter digital output value

V_{OT} : Voltage when digital output changes from 000_H to 001_H

V_{FST} : Voltage when digital output changes from 3FE_H to 3FF_H

6. Flash Memory Program/Erase Characteristics

| Parameter | Conditions | Value | | | Unit | Remarks |
|--------------------------------------|--|-------|-----|-----|-------|---------------------------------------|
| | | Min | Typ | Max | | |
| Sector erase time | T _A = + 25 °C V _{CC} = 5.0 V | — | 0.9 | 3.6 | s | Excludes pre-programming before erase |
| Word (16-bit width) programming time | | — | 23 | 370 | μs | Excludes system-level overhead |
| Chip programming time | T _A = + 25 °C, V _{CC} = 5.0 V | — | 3.4 | 55 | s | |
| Erase/program cycle | — | 10000 | — | — | cycle | |
| Flash memory data retention time | Average T _A = + 85 °C | 20 | — | — | year | * |

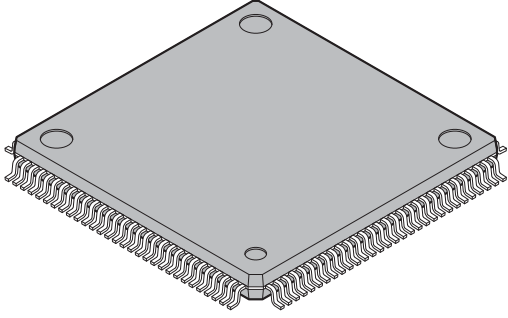
* : This value is calculated from the results of evaluating the reliability of the technology (using Arrhenius equation to translate high temperature measurements into normalized value at + 85 °C) .

MB90920 Series

■ ORDERING INFORMATION

| Part number | Package | Remarks |
|--|--|----------------|
| MB90F922NCPMC MB90F922NCSPMC MB90922NCSPMC MB90F923NCPMC MB90F923NCSPMC MB90F924NCPMC MB90F924NCSPMC | 120-pin plastic LQFP (FPT-120P-M21) | |
| MB90V920-101CR MB90V920-102CR | 299-pin ceramic PGA (PGA-299C-A01) | For evaluation |

PACKAGE DIMENSION

| | | |
|---|--------------------------------|-----------------------|
|  <p>120-pin plastic LQFP</p> <p>(FPT-120P-M21)</p> | Lead pitch | 0.50 mm |
| | Package width × package length | 16.0 × 16.0 mm |
| | Lead shape | Gullwing |
| | Sealing method | Plastic mold |
| | Mounting height | 1.70 mm MAX |
| | Weight | 0.88 g |
| | Code (Reference) | P-LFQFP120-16×16-0.50 |



Please check the latest package dimension at the following URL.
<http://edevic.fujitsu.com/package/en-search/>

MB90920 Series

■ MAJOR CHANGES IN THIS EDITION

| Page | Section | Change Results |
|------|---|--|
| 12 | ■ I/O CIRCUIT TYPE | Corrected the circuit type B. |
| 20 | ■ HANDLING DEVICES | Added the following items; <ul style="list-style-type: none">• Serial communication• Characteristic difference between flash device and MASK ROM device |
| 31 | ■ I/O MAP | Corrected "Address: 003970H". Clock supervisor control register → (Disabled) |
| 46 | ■ ELECTRICAL CHARACTERISTICS 3. DC Characteristics | Added the item for "LCD output impedance". |
| 68 | ■ ORDERING INFORMATION | Corrected the part numbers; MB90V920-101 → MB90V920-101CR MB90V920-102 → MB90V920-102CR |

The vertical lines marked in the left side of the page show the changes.

MEMO

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