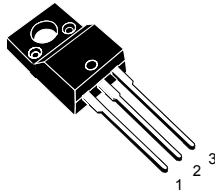
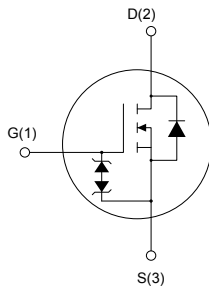


N-channel 900 V, 0.72 Ω typ., 7 A, MDmesh™ K5 Power MOSFET in a TO-220FP package



TO-220FP



AM01476v1_No_tab

Features

| Order code | V_{DS} | $R_{DS(on)}$ max. | I_D |
|------------|----------|-------------------|-------|
| STF7N90K5 | 900 V | 0.81 Ω | 7 A |

- Industry's lowest $R_{DS(on)}$ x area
- Industry's best FoM (figure of merit)
- Ultra-low gate charge
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

This very high voltage N-channel Power MOSFET is designed using MDmesh™ K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.

Product status

STF7N90K5

Product summary

| | |
|-------------------|-----------|
| Order code | STF7N90K5 |
| Marking | 7N90K5 |
| Package | TO-220FP |
| Packing | Tube |

1 Electrical ratings

Table 1. Absolute maximum ratings

| Symbol | Parameter | Value | Unit |
|---------------|---|------------|------------------|
| V_{GS} | Gate-source voltage | ± 30 | V |
| I_D | Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$ | 7 | A |
| I_D | Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$ | 4.4 | A |
| $I_D^{(1)}$ | Drain current (pulsed) | 28 | A |
| P_{TOT} | Total dissipation at $T_C = 25\text{ }^\circ\text{C}$ | 25 | W |
| V_{ISO} | Insulation withstand voltage (RMS) from all three leads to external heat sink ($t = 1\text{ s}$, $T_C = 25\text{ }^\circ\text{C}$) | 2500 | V |
| $dv/dt^{(2)}$ | Peak diode recovery voltage slope | 4.5 | V/ns |
| $dv/dt^{(3)}$ | MOSFET dv/dt ruggedness | 50 | |
| T_j | Operating junction temperature range | -55 to 150 | $^\circ\text{C}$ |
| T_{stg} | Storage temperature range | | |

1. Pulse width limited by safe operating area
2. $I_{SD} \leq 7\text{ A}$, $di/dt \leq 100\text{ A}/\mu\text{s}$, $V_{DS\text{ peak}} < V_{(BR)DSS}$, $V_{DD} = 450\text{ V}$
3. $V_{DS} \leq 720\text{ V}$

Table 2. Thermal data

| Symbol | Parameter | Value | Unit |
|----------------|-------------------------------------|-------|---------------------------|
| $R_{thj-case}$ | Thermal resistance junction-case | 5 | $^\circ\text{C}/\text{W}$ |
| $R_{thj-amb}$ | Thermal resistance junction-ambient | 62.5 | $^\circ\text{C}/\text{W}$ |

Table 3. Avalanche characteristics

| Symbol | Parameter | Value | Unit |
|----------|--|-------|------|
| I_{AR} | Avalanche current, repetitive or not repetitive (pulse width limited by T_{jmax}) | 2.4 | A |
| E_{AS} | Single pulse avalanche energy (starting $T_j = 25\text{ }^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$) | 230 | mJ |

2 Electrical characteristics

$T_C = 25\text{ °C}$ unless otherwise specified

Table 4. On-/off-state

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---------------|-----------------------------------|---|------|------|----------|---------------|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage | $V_{GS} = 0\text{ V}, I_D = 1\text{ mA}$ | 900 | | | V |
| I_{DSS} | Zero gate voltage drain current | $V_{GS} = 0\text{ V}, V_{DS} = 900\text{ V}$ | | | 1 | μA |
| | | $V_{GS} = 0\text{ V}, V_{DS} = 900\text{ V}$ $T_C = 125\text{ °C}^{(1)}$ | | | 50 | μA |
| I_{GSS} | Gate body leakage current | $V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$ | | | ± 10 | μA |
| $V_{GS(th)}$ | Gate threshold voltage | $V_{DD} = V_{GS}, I_D = 100\text{ }\mu\text{A}$ | 3 | 4 | 5 | V |
| $R_{DS(on)}$ | Static drain-source on-resistance | $V_{GS} = 10\text{ V}, I_D = 3.5\text{ A}$ | | 0.72 | 0.81 | Ω |

1. Defined by design, not subject to production test.

Table 5. Dynamic

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-------------------|---------------------------------------|---|------|------|------|----------|
| C_{iss} | Input capacitance | $V_{DS} = 100\text{ V}, f = 1\text{ MHz},$ $V_{GS} = 0\text{ V}$ | - | 425 | - | pF |
| C_{oss} | Output capacitance | | - | 41 | - | pF |
| C_{rss} | Reverse transfer capacitance | | - | 1.2 | - | pF |
| $C_{o(tr)}^{(1)}$ | Time-related equivalent capacitance | $V_{GS} = 0, V_{DS} = 0\text{ to }720\text{ V}$ | - | 64 | - | pF |
| $C_{o(er)}^{(2)}$ | Energy-related equivalent capacitance | | - | 24 | - | pF |
| R_g | Intrinsic gate resistance | $f = 1\text{ MHz}, I_D = 0\text{ A}$ | - | 6.7 | - | Ω |
| Q_g | Total gate charge | $V_{DD} = 720\text{ V}, I_D = 7\text{ A}$ | - | 12 | - | nC |
| Q_{gs} | Gate-source charge | $V_{GS} = 0\text{ to }10\text{ V}$ | - | 3.5 | - | nC |
| Q_{gd} | Gate-drain charge | (see Figure 14. Test circuit for gate charge behavior) | - | 6.5 | - | nC |

1. $C_{o(tr)}$ is a constant capacitance value that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .

2. $C_{o(er)}$ is a constant capacitance value that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .

Table 6. Switching times

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|--------------|---------------------|---|------|------|------|------|
| $t_{d(on)}$ | Turn-on delay time | $V_{DD} = 450\text{ V}, I_D = 3.5\text{ A},$ $R_G = 4.7\text{ }\Omega, V_{GS} = 10\text{ V}$ | - | 13.2 | - | ns |
| t_r | Rise time | | - | 14.2 | - | ns |
| $t_{d(off)}$ | Turn-off delay time | (see Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform) | - | 31.6 | - | ns |
| t_f | Fall time | | - | 14.7 | - | ns |

Table 7. Source-drain diode

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-----------------|-------------------------------|--|---|------|------|---------------|
| I_{SD} | Source-drain current | | - | | 7 | A |
| $I_{SDM}^{(1)}$ | Source-drain current (pulsed) | | - | | 28 | A |
| $V_{SD}^{(2)}$ | Forward on voltage | $I_{SD} = 7\text{ A}$, $V_{GS} = 0\text{ V}$ | - | | 1.5 | V |
| t_{rr} | Reverse recovery time | $I_{SD} = 7\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$ | - | 352 | | ns |
| Q_{rr} | Reverse recovery charge | | - | 3.63 | | μC |
| I_{RRM} | Reverse recovery current | (see Figure 15. Test circuit for inductive load switching and diode recovery times) | - | 20.6 | | A |
| t_{rr} | Reverse recovery time | $I_{SD} = 7\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$ | - | 525 | | ns |
| Q_{rr} | Reverse recovery charge | | - | 4.94 | | μC |
| I_{RRM} | Reverse recovery current | | (see Figure 15. Test circuit for inductive load switching and diode recovery times) | - | 18.8 | |

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

Table 8. Gate-source Zener diode

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---------------|-------------------------------|---|----------|------|------|------|
| $V_{(BR)GSO}$ | Gate-source breakdown voltage | $I_{GS} = \pm 1\text{ mA}$, $I_D = 0\text{ A}$ | ± 30 | - | - | V |

The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection, thus eliminating the need for additional external componentry.

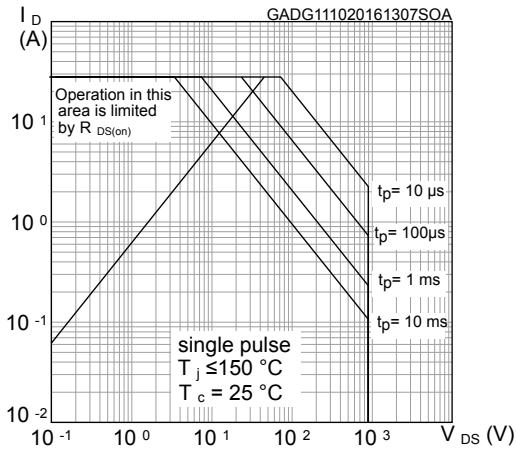
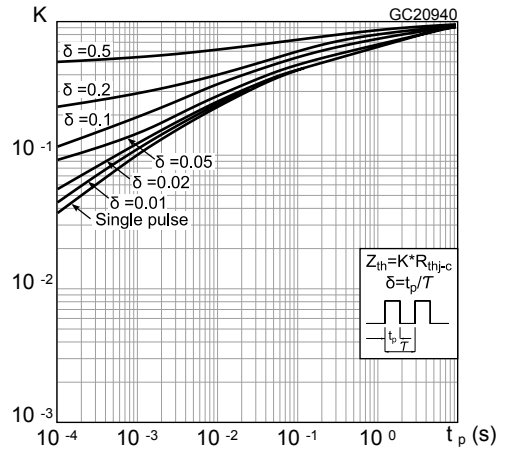
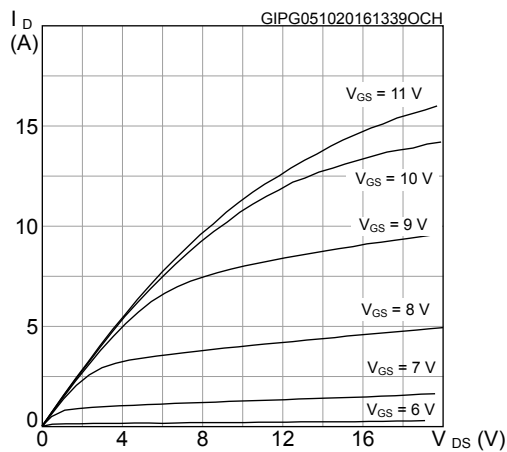
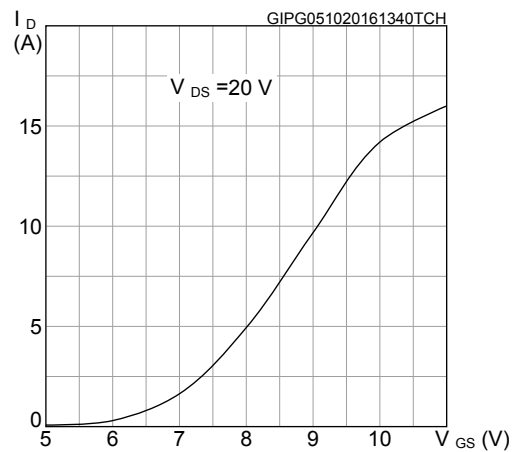
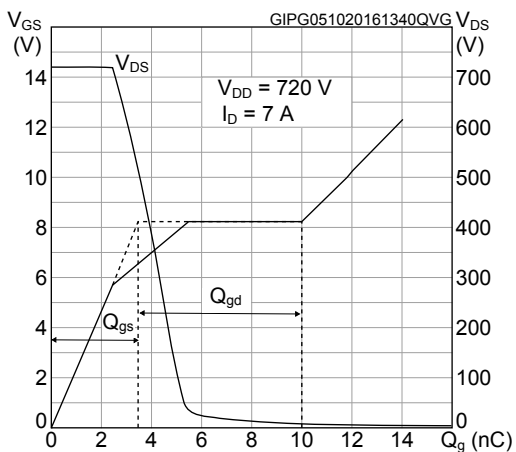
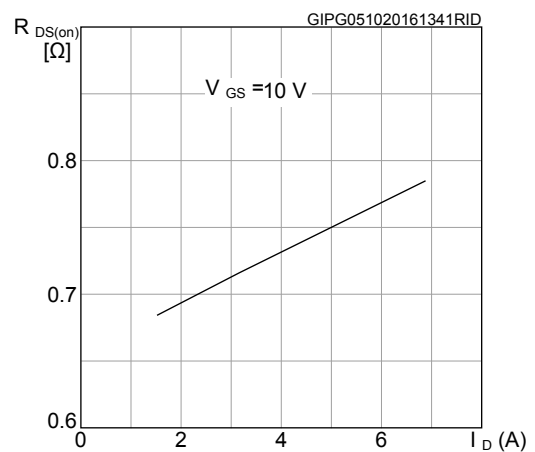
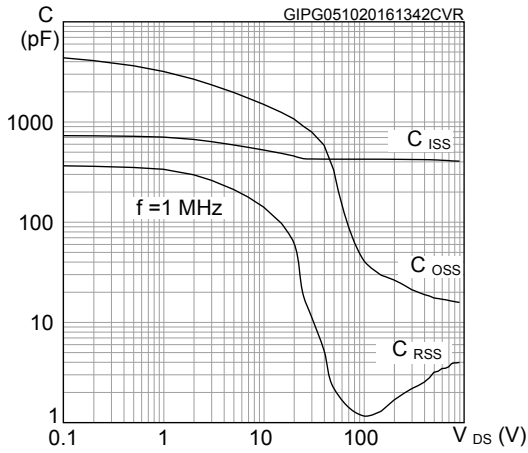
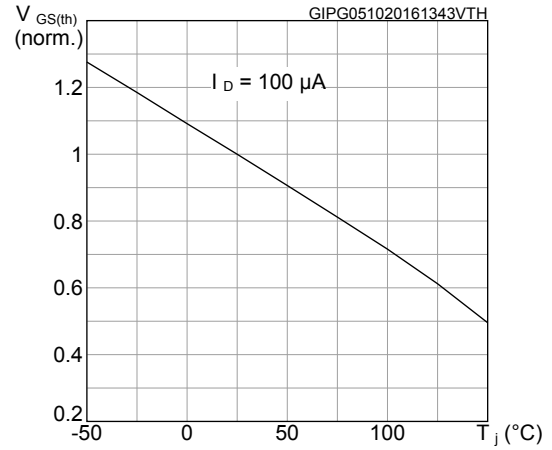
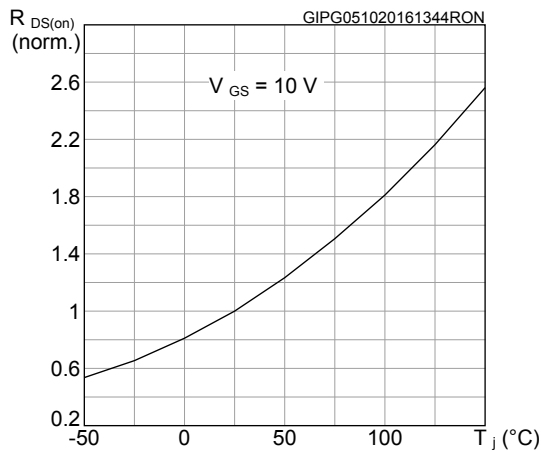
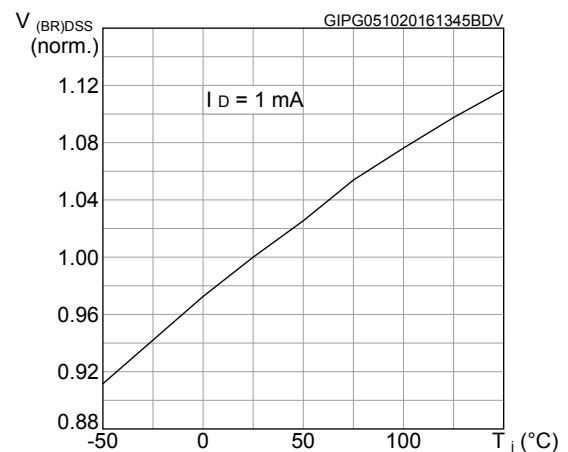
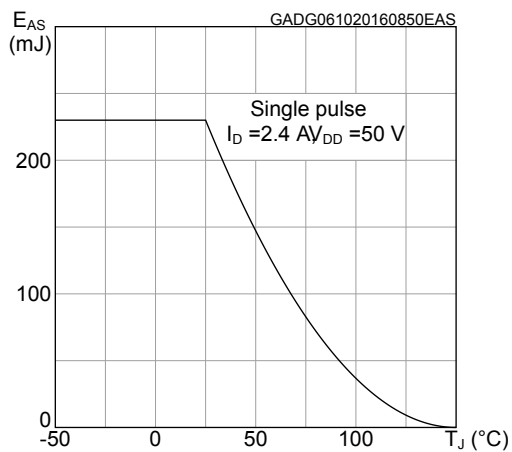
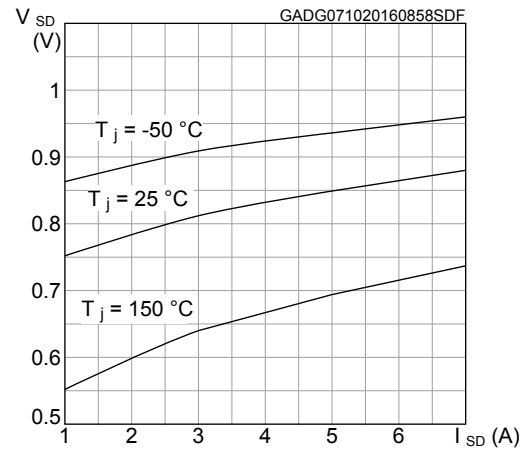
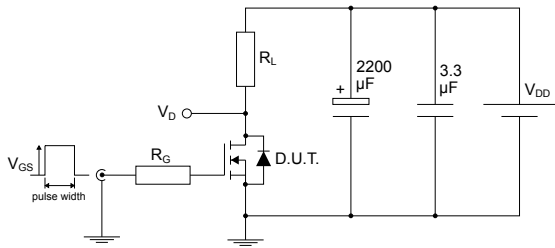
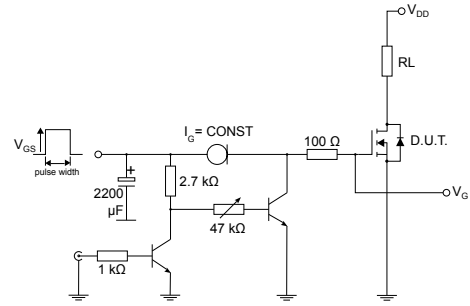
2.1 Electrical characteristics (curves)
Figure 1. Safe operating area

Figure 2. Thermal impedance

Figure 3. Output characteristics

Figure 4. Transfer characteristics

Figure 5. Gate charge vs gate-source voltage

Figure 6. Static drain-source on-resistance


Figure 7. Capacitance variations

Figure 8. Normalized gate threshold voltage vs temperature

Figure 9. Normalized on-resistance vs temperature

Figure 10. Normalized $V_{(BR)DSS}$ vs temperature

Figure 11. Maximum avalanche energy vs starting T_J

Figure 12. Source-drain diode forward characteristics


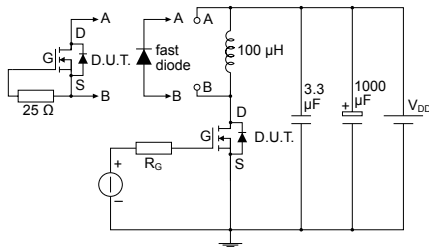
3 Test circuits

Figure 13. Test circuit for resistive load switching times


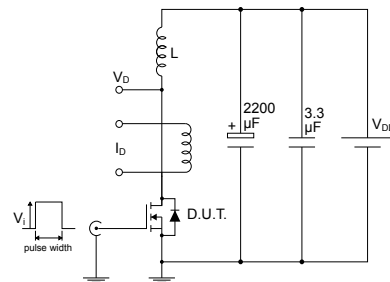
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Figure 14. Test circuit for gate charge behavior


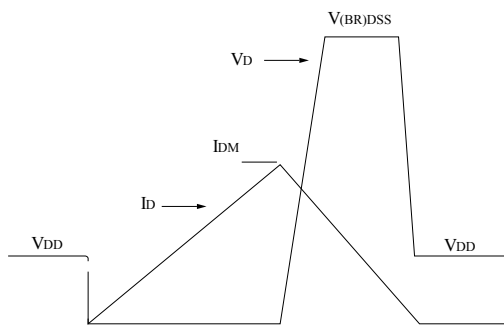
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Figure 15. Test circuit for inductive load switching and diode recovery times


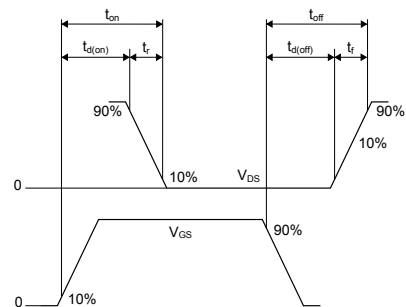
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Figure 16. Unclamped inductive load test circuit


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Figure 17. Unclamped inductive waveform


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Figure 18. Switching time waveform


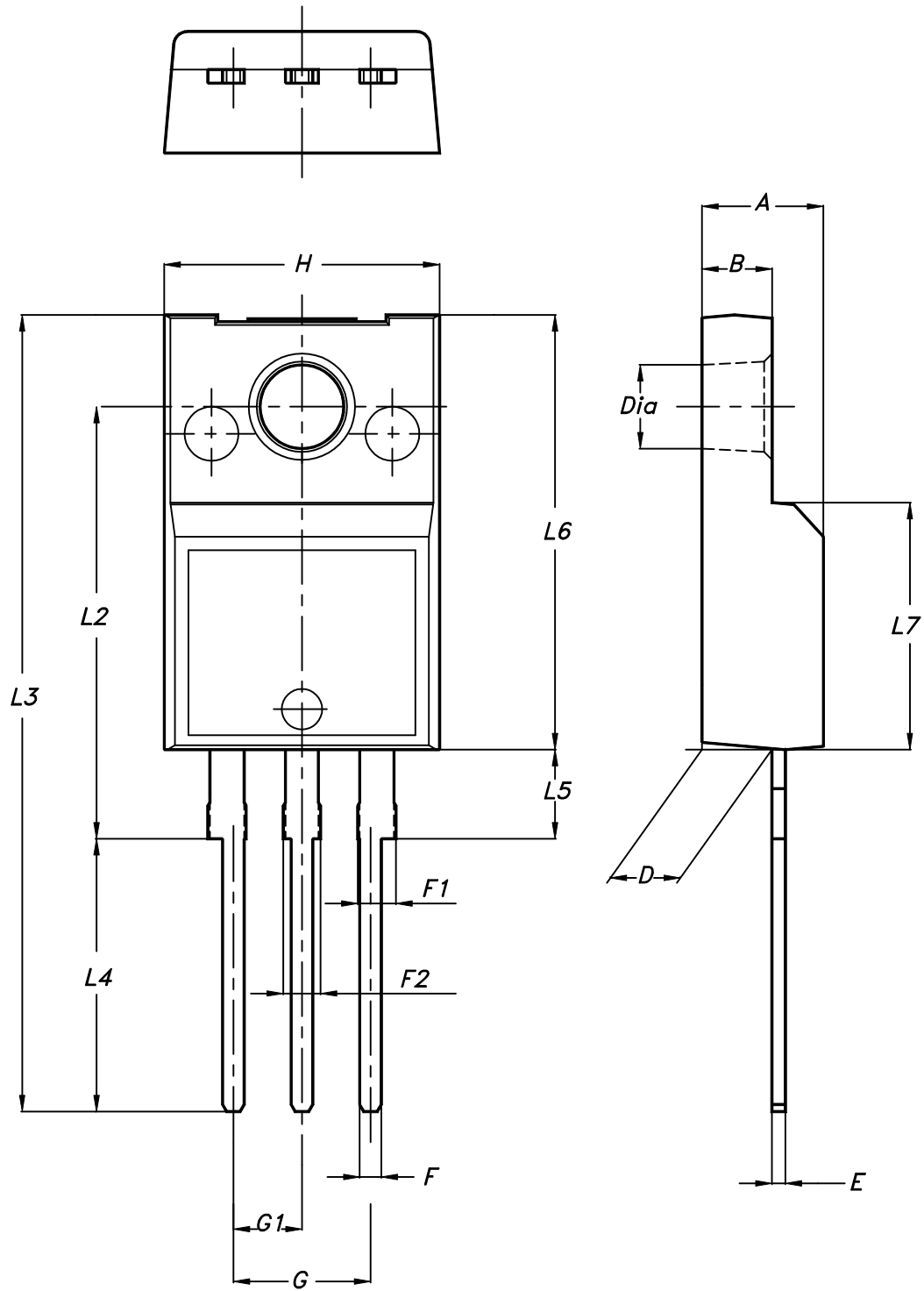
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4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 TO-220FP package information

Figure 19. TO-220FP package outline



7012510_Rev_12_B

Table 9. TO-220FP package mechanical data

| Dim. | mm | | |
|------|------|------|------|
| | Min. | Typ. | Max. |
| A | 4.4 | | 4.6 |
| B | 2.5 | | 2.7 |
| D | 2.5 | | 2.75 |
| E | 0.45 | | 0.7 |
| F | 0.75 | | 1 |
| F1 | 1.15 | | 1.70 |
| F2 | 1.15 | | 1.70 |
| G | 4.95 | | 5.2 |
| G1 | 2.4 | | 2.7 |
| H | 10 | | 10.4 |
| L2 | | 16 | |
| L3 | 28.6 | | 30.6 |
| L4 | 9.8 | | 10.6 |
| L5 | 2.9 | | 3.6 |
| L6 | 15.9 | | 16.4 |
| L7 | 9 | | 9.3 |
| Dia | 3 | | 3.2 |

Revision history

Table 10. Document revision history

| Date | Revision | Changes |
|-------------|----------|---|
| 11-Oct-2016 | 1 | First release. |
| 21-Feb-2018 | 2 | Removed maturity status indication from cover page. The document status is production data. Updated Table 5. Dynamic . Updated Figure 5. Gate charge vs gate-source voltage . Updated Section 4.1 TO-220FP package information . Minor text changes |

Contents

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