

Product Summary

BV _{DSS}	R _{DS(ON)} Max	I _D Max T _C = +25°C
100V	8mΩ @ V _{GS} = 10V	90A
	12.5mΩ @ V _{GS} = 4.5V	74A

Description

This new generation N-Channel Enhancement Mode MOSFET is designed to minimize R_{DS(ON)}, yet maintain superior switching performance. This device is ideal for use in notebook battery power management and load switch.

Applications

- Motor Control
- DC-DC Converters
- Power Management

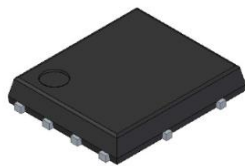
Features

- Thermally Efficient Package-Cooler Running Applications
- High Conversion Efficiency
- 100% Unclamped Inductive Switching (UIS) Test in Production – Ensures More Reliable and Robust End Application
- Low R_{DS(ON)} – Minimizes On-State Losses
- Low Input Capacitance
- Fast Switching Speed
- <1.1mm Package Profile – Ideal for Thin Applications
- **Lead-Free Finish; RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**

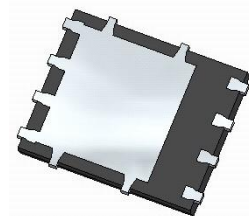
Mechanical Data

- Case: PowerDI[®] 5060-8
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections: See Diagram Below
- Terminal Finish - Matte Tin Annealed over Copper Leadframe. Solderable per MIL-STD-202, Method 208 ⁽³⁾
- Weight: 0.097 grams (Approximate)

PowerDI5060-8

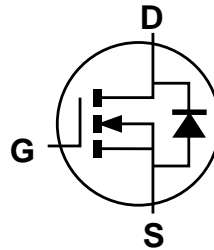


Top View

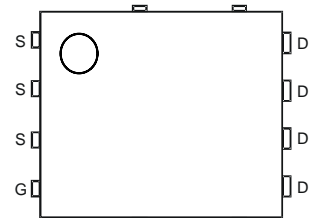


Bottom View

Pin1



Internal Schematic

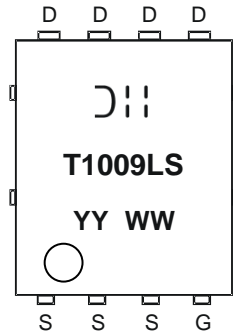

 Top View
Pin Configuration

Ordering Information (Note 4)

Part Number	Case	Packaging
DMT10H009LPS-13	PowerDI5060-8	2,500 / Tape & Reel

- Notes:
1. EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant. All applicable RoHS exemptions applied.
 2. See http://www.diodes.com/quality/lead_free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
 4. For packaging details, go to our website at <https://www.diodes.com/design/support/packaging/diodes-packaging/>.

Marking Information



= Manufacturer's Marking
 T1009LS = Product Type Marking Code
 YYWW = Date Code Marking
 YY = Last Two Digits of Year (ex: 19 = 2019)
 WW = Week Code (01 to 53)

Maximum Ratings (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic			Symbol	Value	Unit
Drain-Source Voltage			V_{DSS}	100	V
Gate-Source Voltage			V_{GSS}	± 20	V
Continuous Drain Current $V_{GS} = 10\text{V}$ (Note 6)	Steady State	$T_A = +25^\circ\text{C}$	I_D	10	A
		$T_A = +70^\circ\text{C}$		8	
Continuous Drain Current $V_{GS} = 10\text{V}$ (Note 7)	Steady State	$T_C = +25^\circ\text{C}$	I_D	90	A
		$T_C = +70^\circ\text{C}$		72	
Pulsed Drain Current (10 μs Pulse, $T_C = +25^\circ\text{C}$, Package Limited)			I_{DM}	360	A
Maximum Continuous Body Diode Forward Current			I_S	85	A
Pulsed Body Diode Current (10 μs Pulse, $T_C = +25^\circ\text{C}$, Package Limited)			I_{SM}	360	A
Avalanche Current (Note 8), $L = 0.3\text{mH}$			I_{AS}	21	A
Avalanche Energy (Note 8), $L = 0.3\text{mH}$			E_{AS}	66	mJ
V_{DS} Spike, $L = 0.1\text{mH}$		$t = 10\mu\text{s}$	V_{SPIKE}	110	V

Thermal Characteristics

Characteristic		Symbol	Value	Unit
Total Power Dissipation (Note 5)	$T_A = +25^\circ\text{C}$	P_D	1.3	W
Thermal Resistance, Junction to Ambient (Note 5)	Steady State	$R_{\theta JA}$	98	$^\circ\text{C/W}$
Total Power Dissipation (Note 6)	$T_A = +25^\circ\text{C}$	P_D	2.9	W
Thermal Resistance, Junction to Ambient (Note 6)	Steady State	$R_{\theta JA}$	43	$^\circ\text{C/W}$
Total Power Dissipation (Note 7)	$T_C = +25^\circ\text{C}$	P_D	104	W
Thermal Resistance, Junction to Case (Note 7)		$R_{\theta JC}$	1.2	$^\circ\text{C/W}$
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to +150	$^\circ\text{C}$

- Notes:
- Device mounted on FR-4 PC board, with minimum recommended pad layout, single sided.
 - Device mounted on FR-4 substrate PC board, 2oz copper, with thermal bias to bottom layer 1inch square copper plate.
 - Thermal resistance from junction to soldering point (on the exposed drain pad).
 - I_{AS} and E_{AS} ratings are based on low frequency and duty cycles to keep $T_J = +25^\circ\text{C}$.

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 9)						
Drain-Source Breakdown Voltage	BV _{DSS}	100	—	—	V	V _{GS} = 0V, I _D = 1mA
Zero Gate Voltage Drain Current	I _{DSS}	—	—	1	μA	V _{DS} = 80V, V _{GS} = 0V
Gate-Source Leakage	I _{GSS}	—	—	±100	nA	V _{GS} = ±20V, V _{DS} = 0V
ON CHARACTERISTICS (Note 9)						
Gate Threshold Voltage	V _{GS(TH)}	1.2	—	2.5	V	V _{DS} = V _{GS} , I _D = 250μA
Static Drain-Source On-Resistance	R _{DS(ON)}	—	6	8	mΩ	V _{GS} = 10V, I _D = 20A
		—	9	12.5		V _{GS} = 4.5V, I _D = 5A
Diode Forward Voltage	V _{SD}	—	0.8	1.2	V	V _{GS} = 0V, I _S = 13A
DYNAMIC CHARACTERISTICS (Note 10)						
Input Capacitance	C _{iSS}	—	2309	—	pF	V _{DS} = 50V, V _{GS} = 0V f = 1MHz
Output Capacitance	C _{oss}	—	536	—		
Reverse Transfer Capacitance	C _{rSS}	—	13.7	—		
Gate Resistance	R _g	—	1.9	—	Ω	V _{DS} = 0V, V _{GS} = 0V, f = 1MHz
Total Gate Charge (V _{GS} = 10V)	Q _g	—	40.2	—	nC	V _{DD} = 50V, I _D = 20A,
Total Gate Charge (V _{GS} = 4.5V)	Q _g	—	20.2	—		
Gate-Source Charge	Q _{gs}	—	7.0	—		
Gate-Drain Charge	Q _{gd}	—	8.5	—		
Turn-On Delay Time	t _{D(ON)}	—	5.4	—	ns	V _{DD} = 50V, V _{GS} = 10V, I _D = 20A, R _g = 3Ω
Turn-On Rise Time	t _r	—	10.6	—		
Turn-Off Delay Time	t _{D(OFF)}	—	28.3	—		
Turn-Off Fall Time	t _f	—	14.9	—		
Reverse Recovery Time	t _{RR}	—	44.3	—	ns	I _F = 20A, di/dt = 100A/μs
Reverse Recovery Charge	Q _{RR}	—	65.5	—	nC	

Notes: 9. Short duration pulse test used to minimize self-heating effect.
10. Guaranteed by design. Not subject to product testing.

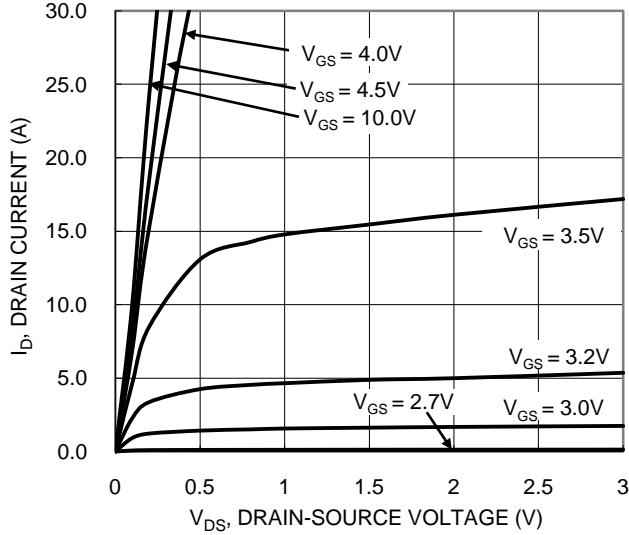


Figure 1. Typical Output Characteristic

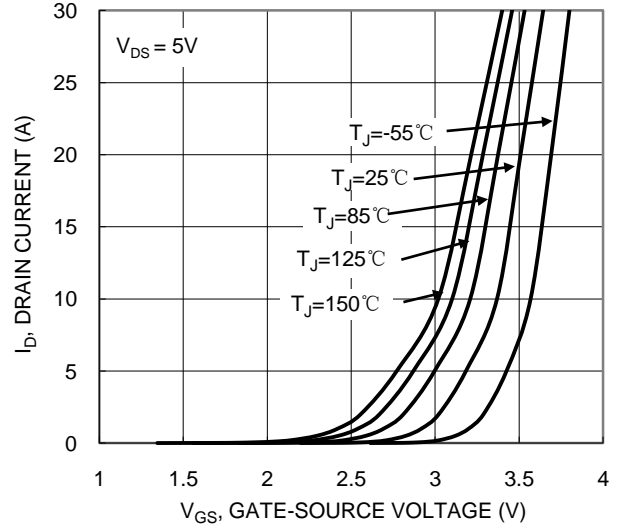


Figure 2. Typical Transfer Characteristic

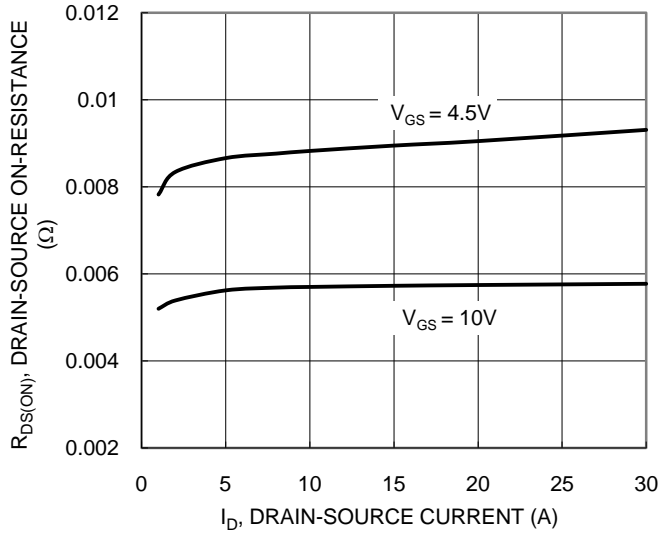


Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage

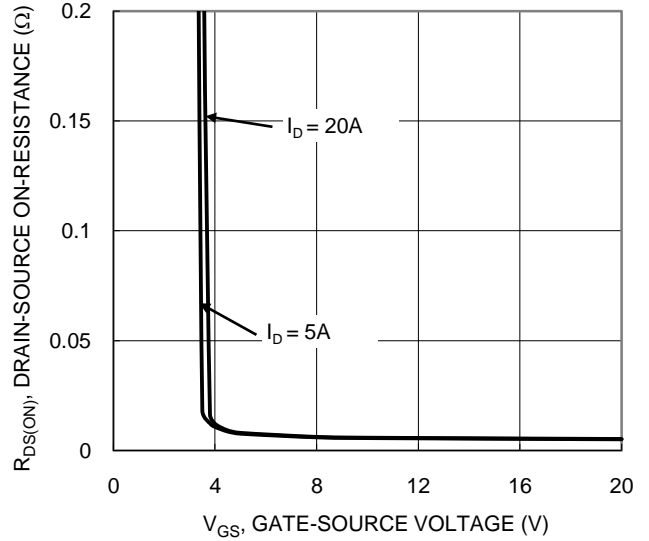


Figure 4. Typical Transfer Characteristic

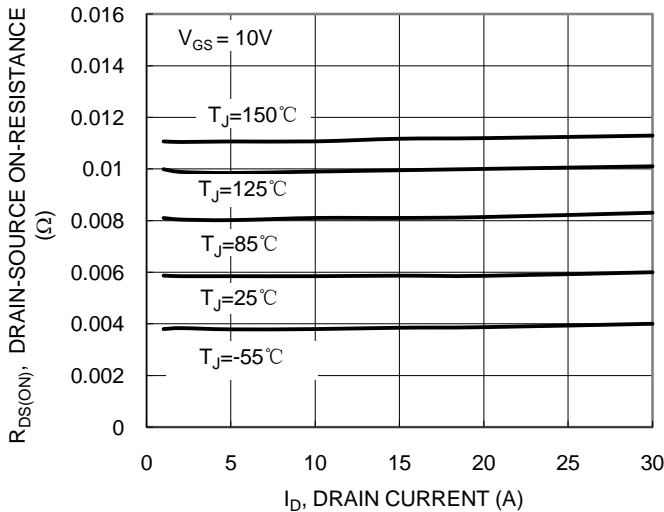


Figure 5. Typical On-Resistance vs. Drain Current and Junction Temperature

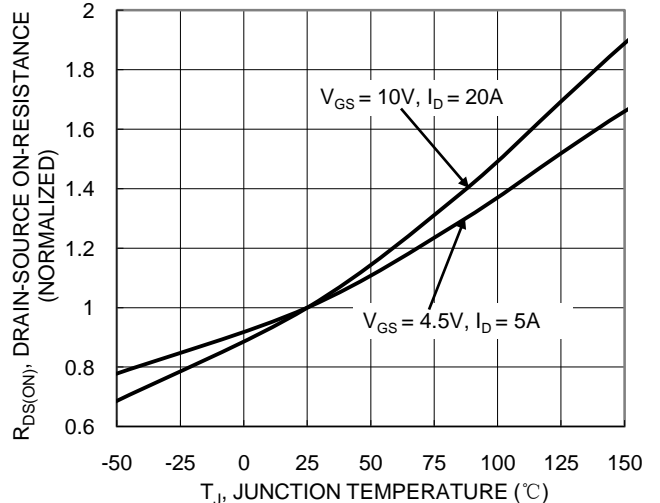


Figure 6. On-Resistance Variation with Junction Temperature

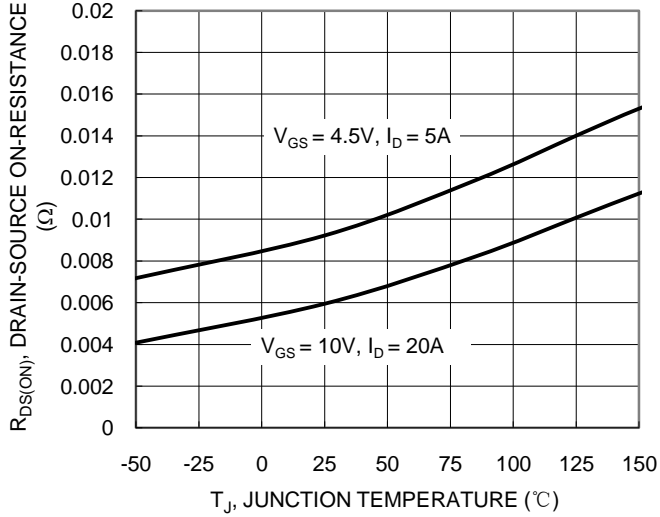


Figure 7. On-Resistance Variation with Junction Temperature

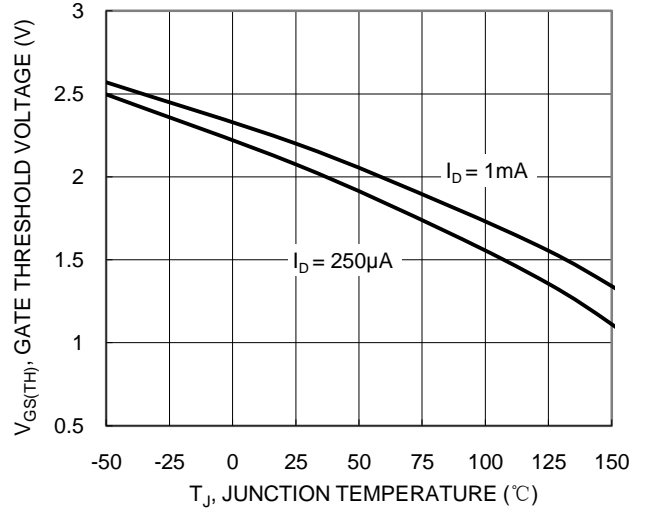


Figure 8. Gate Threshold Variation vs. Junction Temperature

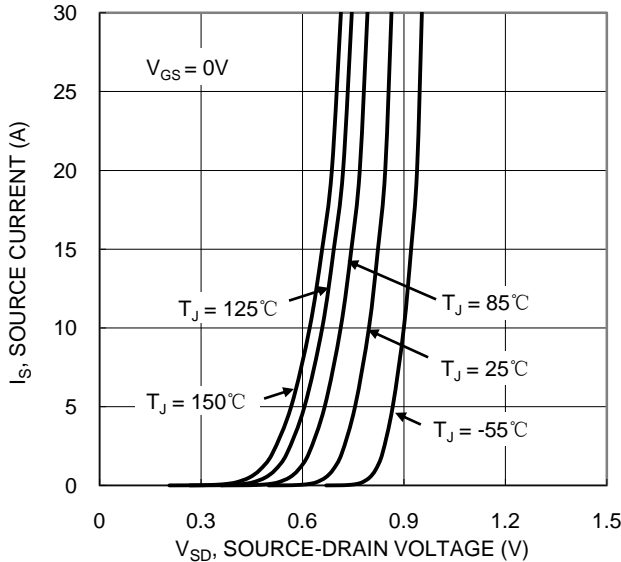


Figure 9. Diode Forward Voltage vs. Current

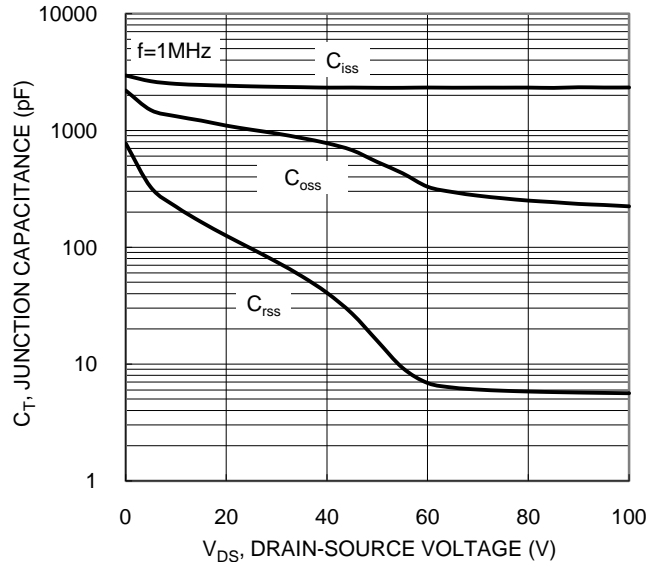


Figure 10. Typical Junction Capacitance

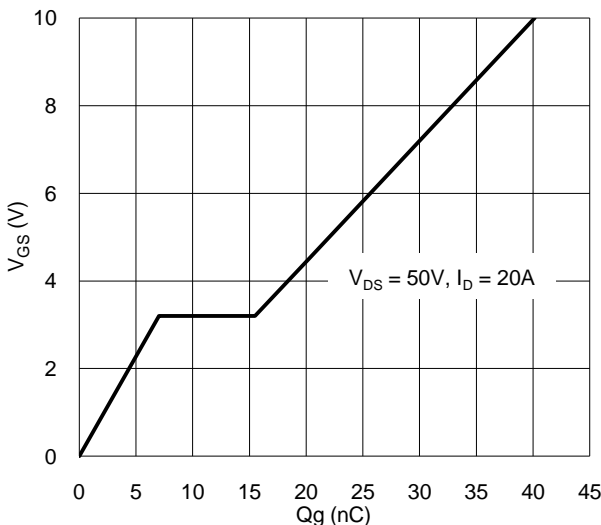


Figure 11. Gate Charge

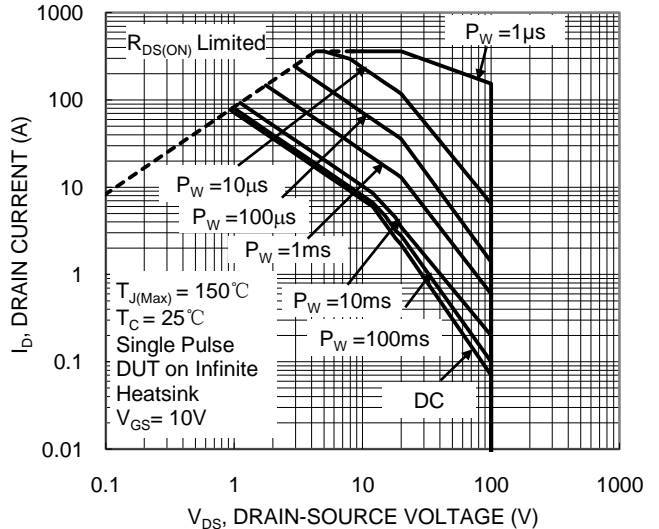


Figure 12. SOA, Safe Operation Area

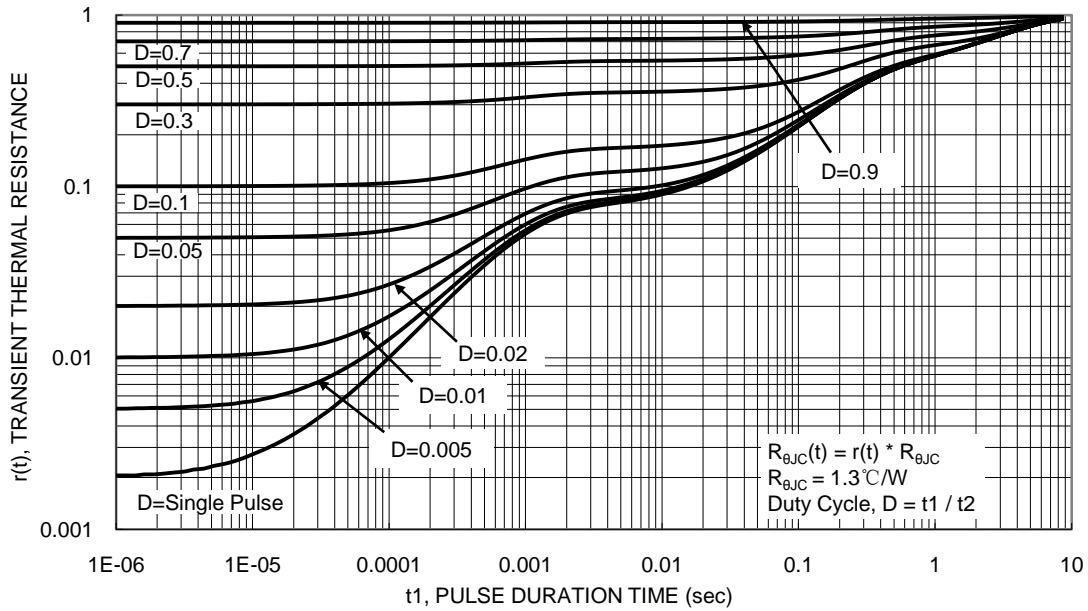
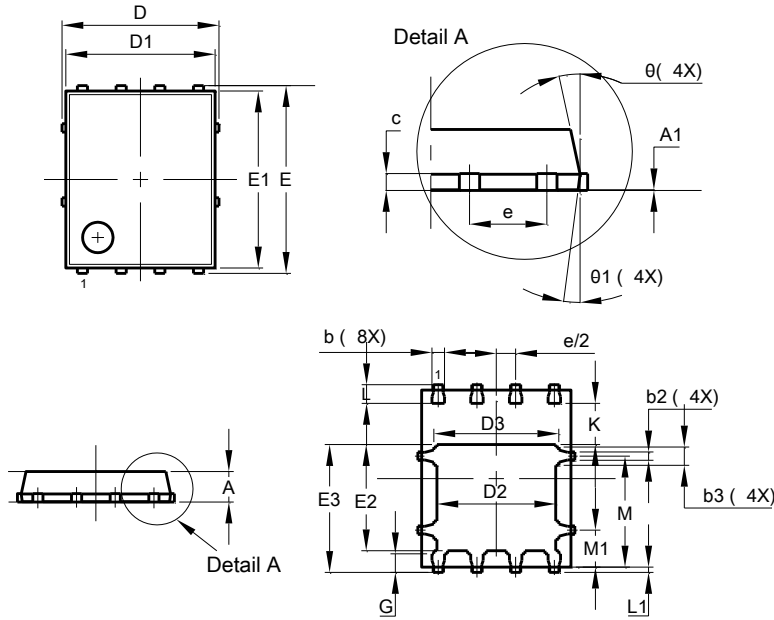


Figure 13. Transient Thermal Resistance

Package Outline Dimensions

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

PowerDI5060-8

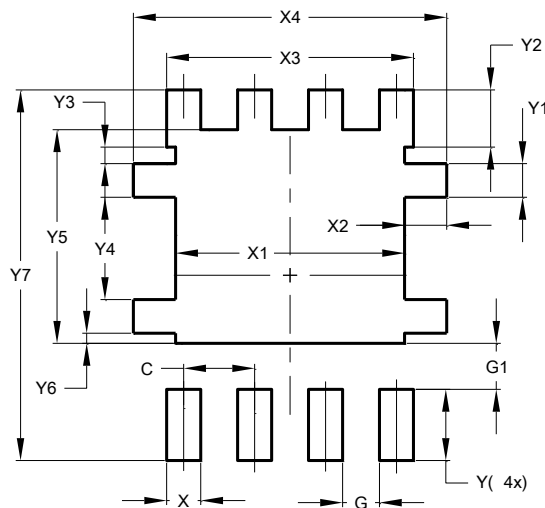


PowerDI5060-8			
Dim	Min	Max	Typ
A	0.90	1.10	1.00
A1	0.00	0.05	-
b	0.33	0.51	0.41
b2	0.200	0.350	0.273
b3	0.40	0.80	0.60
c	0.230	0.330	0.277
D	5.15 BSC		
D1	4.70	5.10	4.90
D2	3.70	4.10	3.90
D3	3.90	4.30	4.10
E	6.15 BSC		
E1	5.60	6.00	5.80
E2	3.28	3.68	3.48
E3	3.99	4.39	4.19
e	1.27 BSC		
G	0.51	0.71	0.61
K	0.51	-	-
L	0.51	0.71	0.61
L1	0.100	0.200	0.175
M	3.235	4.035	3.635
M1	1.00	1.40	1.21
θ	10°	12°	11°
$\theta 1$	6°	8°	7°
All Dimensions in mm			

Suggested Pad Layout

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

PowerDI5060-8



Dimensions	Value (in mm)
C	1.270
G	0.660
G1	0.820
X	0.610
X1	4.100
X2	0.755
X3	4.420
X4	5.610
Y	1.270
Y1	0.600
Y2	1.020
Y3	0.295
Y4	1.825
Y5	3.810
Y6	0.180
Y7	6.610

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Как с нами связаться

Телефон: 8 (812) 309 58 32 (многоканальный)

Факс: 8 (812) 320-02-42

Электронная почта: org@eplast1.ru

Адрес: 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.