



CMOS ASYNCHRONOUS FIFO
2,048 x 9, 4,096 x 9
8,192 x 9, 16,384 x 9
32,768 x 9 and 65,536 x 9

IDT7203
IDT7204
IDT7205
IDT7206
IDT7207
IDT7208

FEATURES:

- First-In/First-Out Dual-Port memory
- 2,048 x 9 organization (IDT7203)
- 4,096 x 9 organization (IDT7204)
- 8,192 x 9 organization (IDT7205)
- 16,384 x 9 organization (IDT7206)
- 32,768 x 9 organization (IDT7207)
- 65,536 x 9 organization (IDT7208)
- High-speed: 12ns access time
- Low power consumption
 - Active: 660mW (max.)
 - Power-down: 44mW (max.)
- Asynchronous and simultaneous read and write
- Fully expandable in both word depth and width
- 720x family is pin and functionally compatible from 256 x 9 to 64k x 9
- Status Flags: Empty, Half-Full, Full
- Retransmit capability
- High-performance CMOS technology
- Military product compliant to MIL-STD-883, Class B
- Standard Military Drawing for #5962-88669 (IDT7203), 5962-89567 (IDT7203), and 5962-89568 (IDT7204) are listed on this function

- Industrial temperature range (-40°C to $+85^{\circ}\text{C}$) is available (plastic packages only)
- Green parts available, see ordering information

DESCRIPTION:

The IDT7203/7204/7205/7206/7207/7208 are dual-port memory buffers with internal pointers that load and empty data on a first-in/first-out basis. The device uses Full and Empty flags to prevent data overflow and underflow and expansion logic to allow for unlimited expansion capability in both word size and depth.

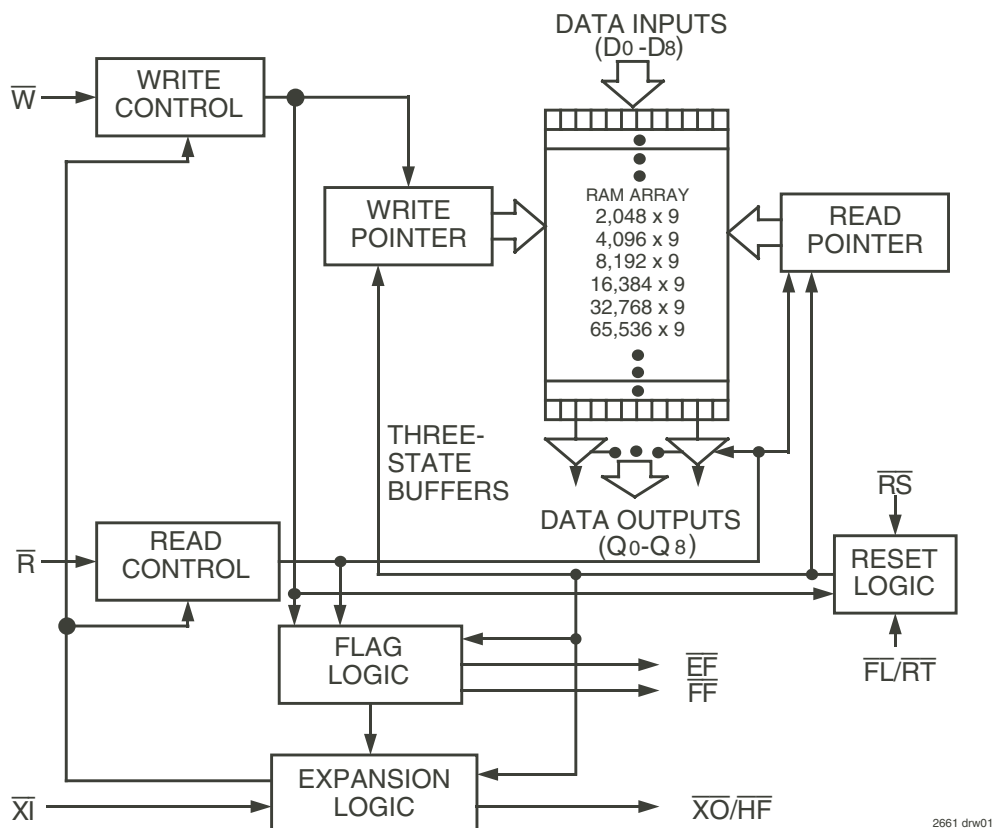
Data is toggled in and out of the device through the use of the Write ($\overline{W}$) and Read ($\overline{R}$) pins.

The device's 9-bit width provides a bit for a control or parity at the user's option. It also features a Retransmit ($\overline{RT}$) capability that allows the read pointer to be reset to its initial position when $\overline{RT}$ is pulsed LOW. A Half-Full Flag is available in the single device and width expansion modes.

These FIFOs are fabricated using high-speed CMOS technology. They are designed for applications requiring asynchronous and simultaneous read/writes in multiprocessing, rate buffering and other applications.

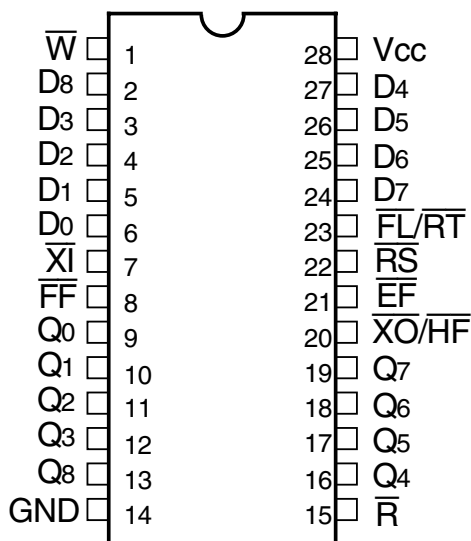
Military grade product is manufactured in compliance with MIL-STD-883, Class B.

FUNCTIONAL BLOCK DIAGRAM



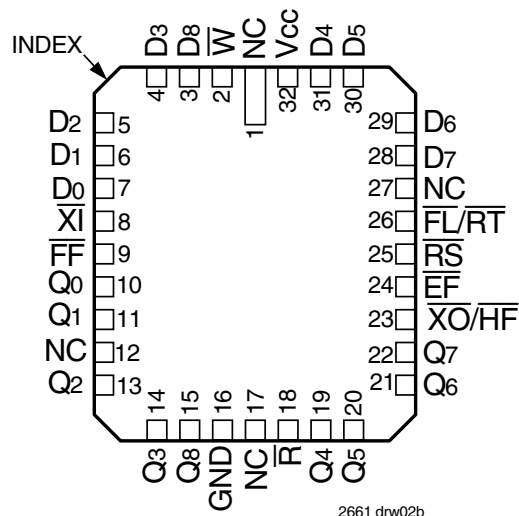
2661 dnw01

PIN CONFIGURATIONS



2661 drw02a

TOP VIEW



2661 drw02b

TOP VIEW

DC ELECTRICAL CHARACTERISTICS

(Commercial: $V_{CC} = 5V \pm 10\%$, $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$; Industrial: $V_{CC} = 5V \pm 10\%$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$; Military: $V_{CC} = 5V \pm 10\%$, $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$)

Symbol	Parameter	IDT7203 ⁽¹⁾ IDT7204 ⁽¹⁾ Commercial and Industrial $t_A = 12, 15, 20, 25, 35, 50 \text{ ns}$			IDT7203 IDT7204 Military ⁽³⁾ $t_A = 20, 30, 40 \text{ ns}$			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
$I_{LI}^{(6)}$	Input Leakage Current (Any Input)	-1	—	1	-1	—	1	μA
$I_{LO}^{(7)}$	Output Leakage Current	-10	—	10	-10	—	10	μA
V_{OH}	Output Logic "1" Voltage $I_{OH} = -2\text{mA}$	2.4	—	—	2.4	—	—	V
V_{OL}	Output Logic "0" Voltage $I_{OL} = 8\text{mA}$	—	—	0.4	—	—	0.4	V
$I_{CC1}^{(8,9,10)}$	Active Power Supply Current	—	—	120	—	—	150	mA
$I_{CC2}^{(8,10,11)}$	Standby Current ($\bar{R}=\bar{W}=\bar{RS}=\bar{FL}/\bar{RT}=V_{IH}$)	—	—	12	—	—	25	mA
$I_{CC3}^{(8,10,12)}$	Power Down Current	—	—	2	—	—	4	mA

Symbol	Parameter	IDT7205 ⁽¹⁾ IDT7206 ^(2,4) IDT7207 ^(2,4) IDT7208 ^(2,5) Commercial and Industrial $t_A = 12, 15, 20, 25, 35, 50 \text{ ns}$			IDT7205 IDT7206 IDT7207 Military $t_A = 20, 30 \text{ ns}$			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
$I_{LI}^{(6)}$	Input Leakage Current (Any Input)	-1	—	1	-1			

AC ELECTRICAL CHARACTERISTICS⁽¹⁾

(Commercial: VCC = 5V ± 10%, TA = 0°C to +70°C; Industrial: VCC = 5V ± 10%, TA = -40°C to +85°C; Military: VCC = 5V ± 10%, TA = -55°C to +125°C)

Symbol	Parameters	Commercial		Com'I & Ind'I		Com'I & Military		Commercial		Com'I & Ind'I		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
fS	Shift Frequency	—	50	—	40	—	33.3	—	33.3	—	28.5	MHz
tRC	Read Cycle Time	20	—	25	—	30	—	30	—	35	—	ns
tA	Access Time	—	12	—	15	—	20	—	20	—	25	ns
tRR	Read Recovery Time	8	—	10	—	10	—	10	—	10	—	ns
tRPW	Read Pulse Width ⁽⁴⁾	12	—	15	—	20	—	20	—	25	—	ns
tRLZ	Read LOW to Data Bus LOW ⁽⁵⁾	3	—	5	—	5	—	5	—	5	—	ns
tWLZ	Write HIGH to Data Bus Low-Z ^(5,6)	3	—	5	—	5	—	5	—	5	—	ns
tDV	Data Valid from Read HIGH	5	—	5	—	5	—	5	—	5	—	ns
tRHZ	Read HIGH to Data Bus High-Z ⁽⁵⁾	—	12	—	15	—	15	—	15	—	18	ns
tWC	Write Cycle Time	20	—	25	—	30	—	30	—	35	—	ns
tWPW	Write Pulse Width ⁽⁴⁾	12	—	15	—	20	—	20	—	25	—	ns
tWR	Write Recovery Time	8	—	10	—	10						

AC ELECTRICAL CHARACTERISTICS⁽¹⁾ (CONTINUED)

(Commercial: VCC = 5V ± 10%, TA = 0°C to +70°C; Industrial: VCC = 5V ± 10%, TA = -40°C to +85°C; Military: VCC = 5V ± 10%, TA = -55°C to +125°C)

Symbol	Parameters	Military		Commercial		Military		Commercial		Unit
		IDT7203L30 IDT7204L30 IDT7205L30 IDT7206L30 IDT7207L30		IDT7203L35 IDT7204L35 IDT7205L35 IDT7206L35 IDT7207L35 IDT7208L35		IDT7203L40		IDT7203L50 IDT7204L50 IDT7205L50 IDT7206L50 IDT7207L50		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t _S	Shift Frequency	—	25	—	22.22	—	20	—	15	MHz
t _{RC}	Read Cycle Time	40	—	45	—	50	—	65	—	ns
t _A	Access Time	—	30	—	35	—	40	—	50	ns
t _{RR}	Read Recovery Time	10	—	10	—	10	—	15	—	ns
t _{RPW}	Read Pulse Width ⁽²⁾	30	—	35	—	40	—	50	—	ns
t _{RLZ}	Read LOW to Data Bus LOW ⁽³⁾	5	—	5	—	5	—	10	—	ns
t _{WLZ}	Write HIGH to Data Bus Low-Z ^(3,4)	5	—	10	—	10	—	15	—	ns
t _{DV}	Data Valid from Read HIGH	5	—	5	—	5	—	5	—	ns
t _{RHZ}	Read HIGH to Data Bus High-Z ⁽³⁾	—	20	—	20	—	25	—	30	ns
t _{WC}	Write Cycle Time	40								

SIGNAL DESCRIPTIONS

INPUTS:

DATA IN (D₀–D₈) — Data inputs for 9-bit wide data.

CONTROLS:

RESET ($\overline{RS}$) — Reset is accomplished whenever the Reset ($\overline{RS}$) input is taken to a LOW state. During reset, both internal read and write pointers are set to the first location. A reset is required after power-up before a write operation can take place. **Both the Read Enable ($\overline{R}$) and Write Enable ($\overline{W}$) inputs must be in the HIGH state during the window shown in Figure 2 (i.e. t_{RSS} before the rising edge of $\overline{RS}$) and should not change until t_{RSR} after the rising edge of $\overline{RS}$.**

WRITE ENABLE ($\overline{W}$) — A write cycle is initiated on the falling edge of this input if the Full Flag ($\overline{FF}$) is not set. Data set-up and hold times must be adhered to, with respect to the rising edge of the Write Enable ($\overline{W}$). Data is stored in the RAM array sequentially and independently of any on-going read operation.

After half of the memory is filled, and at the falling edge of the next write operation, the Half-Full Flag ($\overline{HF}$) will be set to LOW, and will remain set until the difference between the write pointer and read pointer is less than or equal to one-half of the total memory of the device. The Half-Full Flag ($\overline{HF}$) is then reset by the rising edge of the read operation.

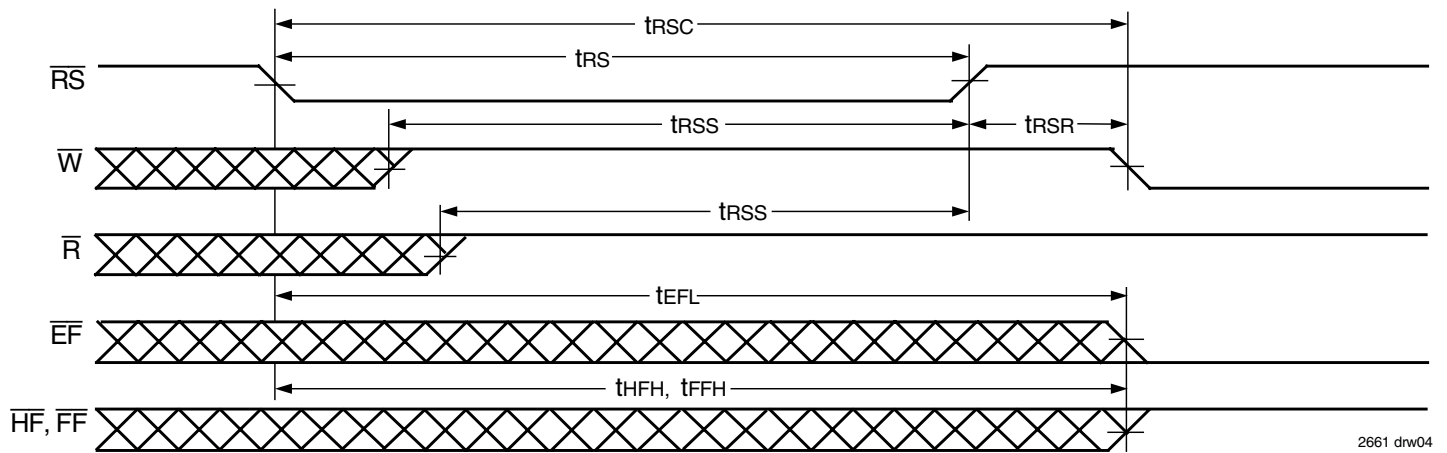
To prevent data overflow, the Full Flag ($\overline{FF}$) will go LOW on the falling edge of the last write signal, which inhibits further write operations. Upon the completion of a valid read operation, the Full Flag ($\overline{FF}$) will go HIGH after t_{RFF} , allowing a new valid write to begin. When the FIFO is full, the internal write pointer is blocked from $\overline{W}$, so external changes in $\overline{W}$ will not affect the FIFO when it is full.

READ ENABLE ($\overline{R}$) — A read cycle is initiated on the falling edge of the Read Enable ($\overline{R}$), provided the Empty Flag ($\overline{EF}$) is not set. The data is accessed on a First-In/First-Out basis, independent of any ongoing write operations. After Read Enable ($\overline{R}$) goes HIGH, the Data Outputs (Q₀ through Q₈) will return to a high-impedance condition until the next Read operation. When all the data has been read from the FIFO, the Empty Flag ($\overline{EF}$) will go LOW, allowing the “final” read cycle but inhibiting further read operations, with the data outputs remaining in a high-impedance state. Once a valid write operation has been accomplished, the Empty Flag ($\overline{EF}$) will go HIGH after t_{WEF} and a valid Read can then begin. When the FIFO is empty, the internal read pointer is blocked from $\overline{R}$ so external changes will not affect the FIFO when it is empty.

FIRST LOAD/RETRANSMIT ($\overline{FL/RT}$) — This is a dual-purpose input. In the Depth Expansion Mode, this pin is grounded to indicate that it is the first device

loaded (see Operating Modes). The Single Device Mode is initiated by grounding the Expansion In ($\overline{XI}$).

The IDT7203/7204/7205/7206/7207/7208 can be made to retransmit data when the Retransmit Enable Control ($\overline{RT}$) input is pulsed LOW. A retransmit operation will set the internal read pointer to the first location and will not affect the write pointer. The status of the Flags will change depending on the relative locations of the read and write pointers. Read Enable ($\overline{R}$

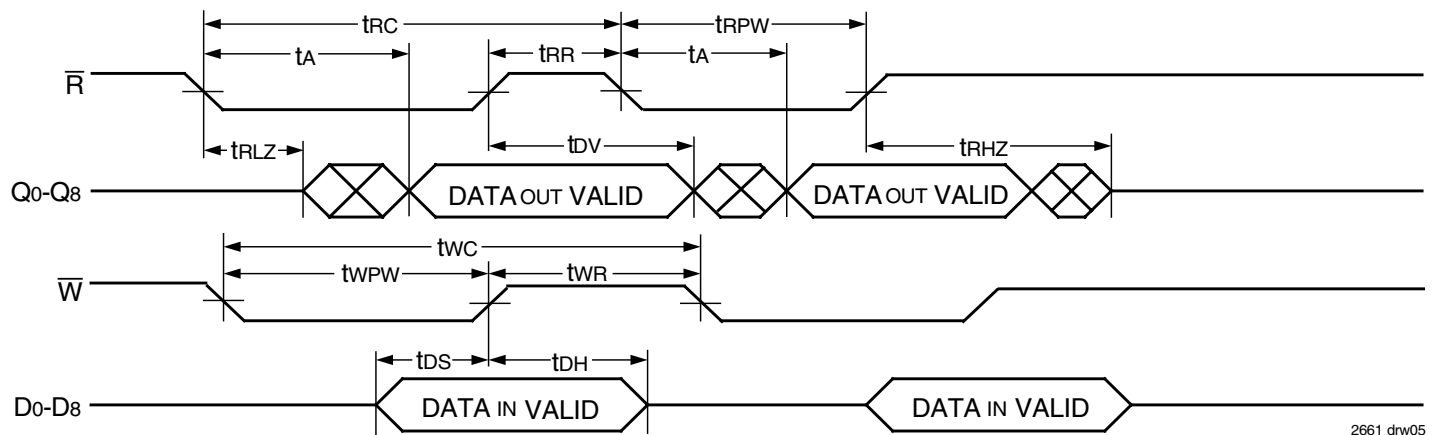


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NOTE:

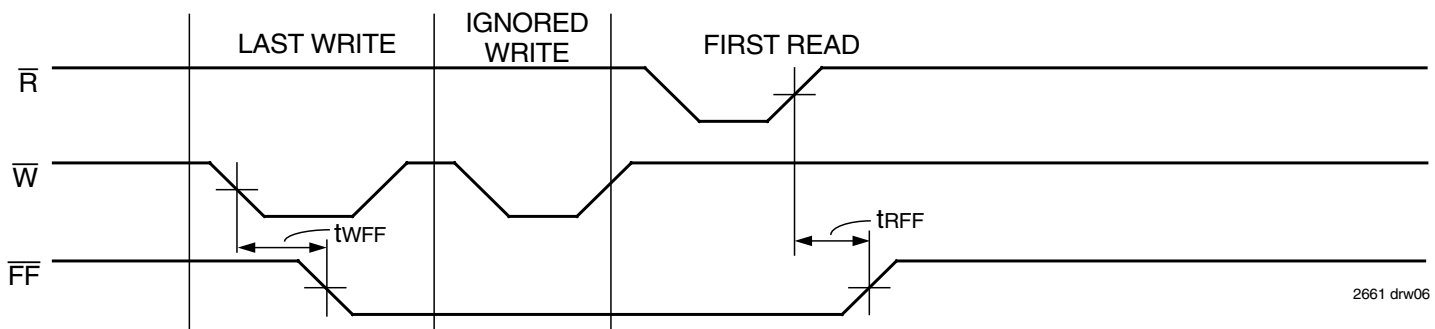
1. $\bar{W}$ and $\bar{R} = V_{IH}$ around the rising edge of $\bar{RS}$.

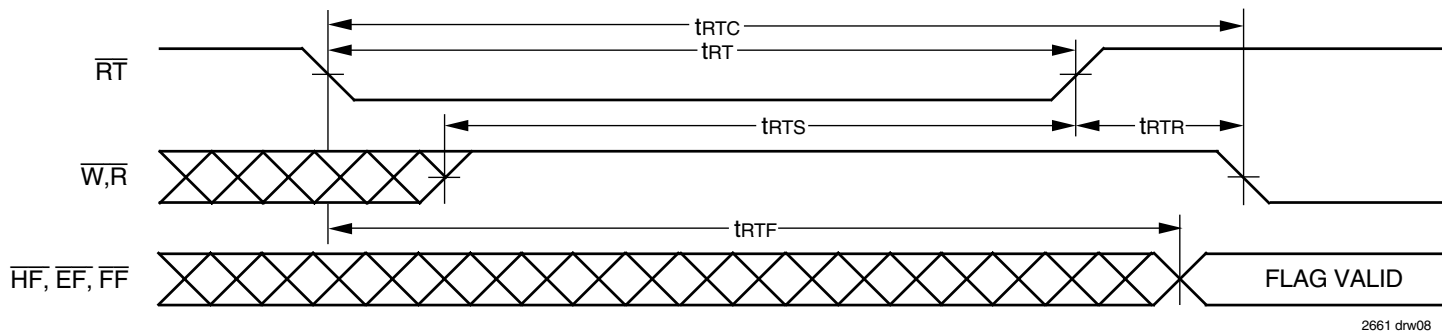
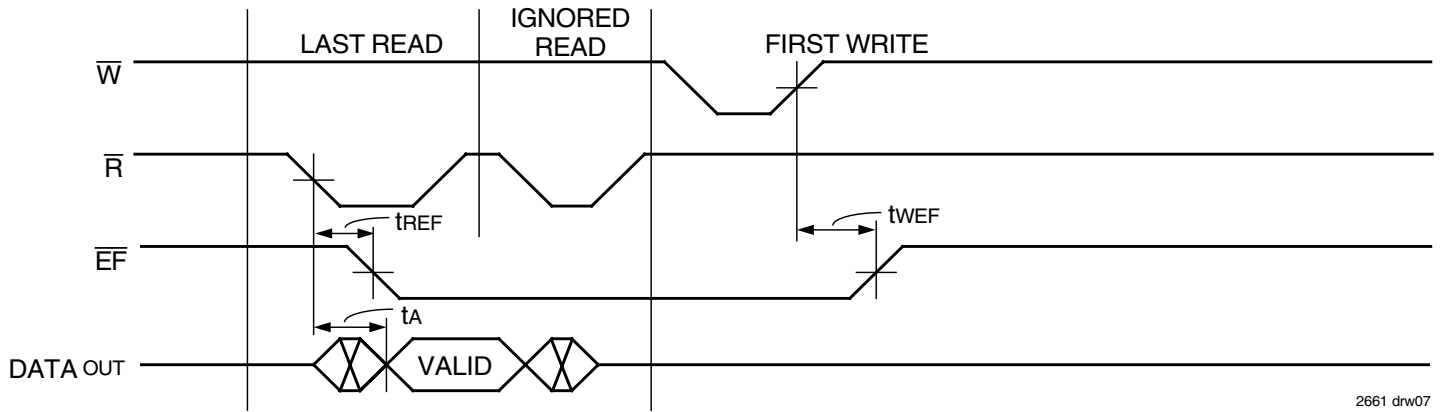
Figure 2. Reset



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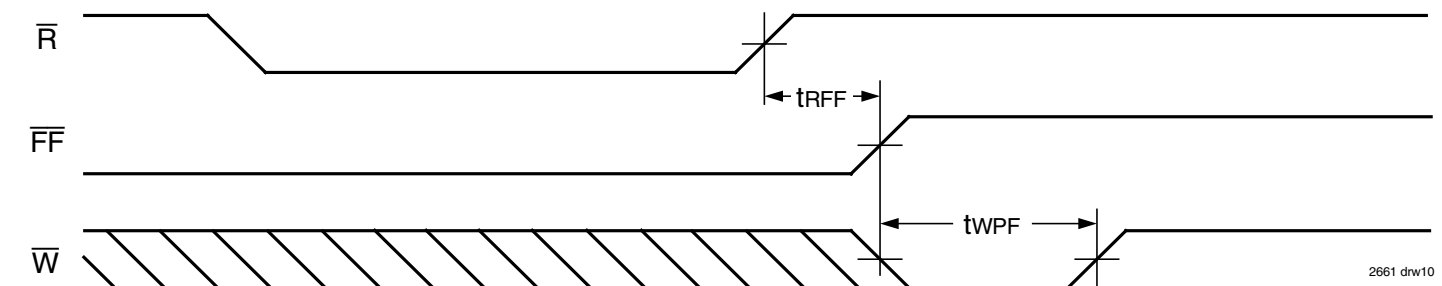
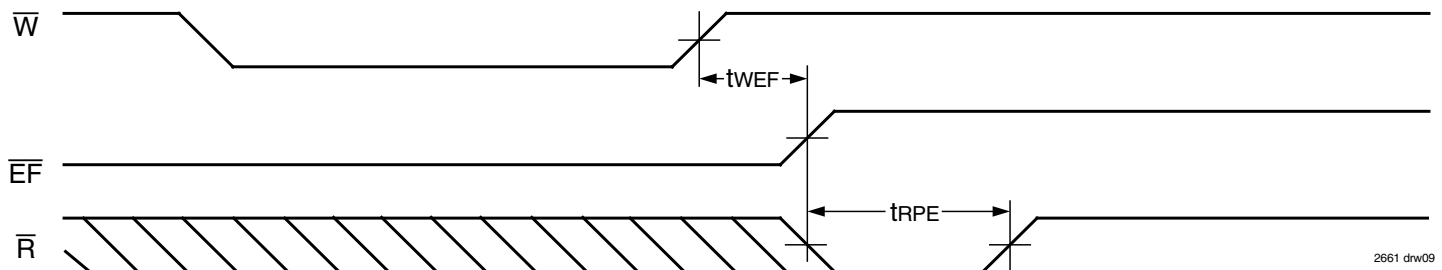
Figure 3. Asynchronous Write and Read Operation





NOTE:
1. EF, FF and HF may change status during Retransmit, but flags will be valid at tRTC.

Figure 6. Retransmit



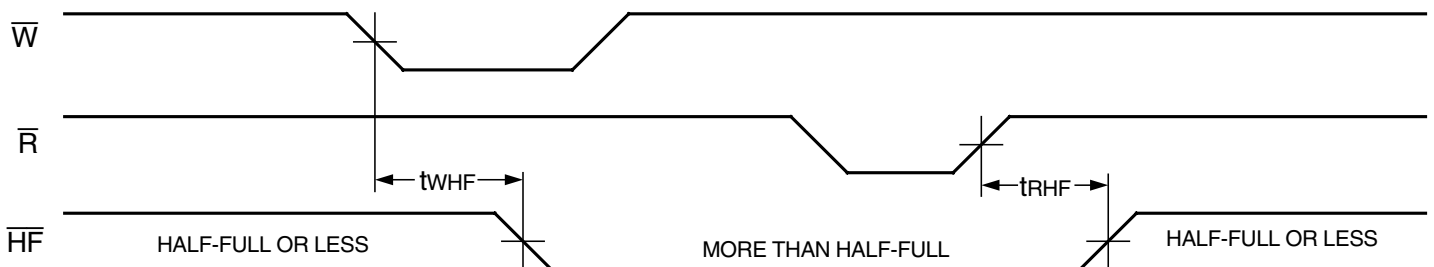


Figure 9. Half-Full Flag Timing

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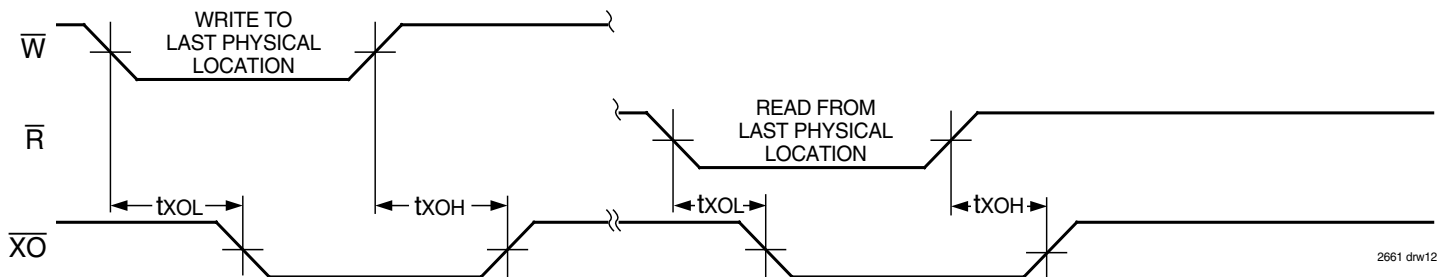


Figure 10. Expansion Out

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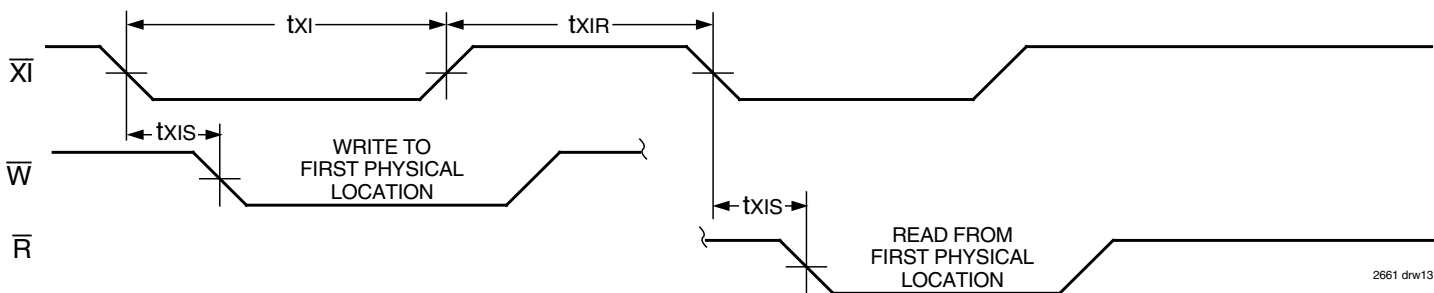


Figure 11. Expansion In

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OPERATING MODES:

Care must be taken to assure that the appropriate flag is monitored by each system (i.e. $\overline{FF}$ is monitored on the device where $\overline{W}$ is used; $\overline{EF}$ is monitored on the device where $\overline{R}$ is used). For additional information on the IDT7203/7204/7205/7206/7207, refer to Tech Note 8: *Operating FIFOs on Full and Empty Boundary Conditions* and Tech Note 6: *Designing with FIFOs*.

Single Device Mode

A single IDT7203/7204/7205/7206/7207/7208 may be used when the application requirements are for 2,048/4,096/8,192/16,384/32,768/65,536 words or less. These FIFOs are in a Single Device Configuration when the Expansion In ($\overline{XI}$) control input is grounded (see Figure 12).

Depth Expansion

These FIFOs can easily be adapted to applications when the requirements are for greater than 2,048/4,096/8,192/16,384/32,768/65,536 words. Figure 14 demonstrates Depth Expansion using three IDT7203/7204/7205/7206/7207/7208s. Any depth can be attained by adding additional IDT7203/

7204/7205/7206/7207/7208s. These devices operate in the Depth Expansion mode when the following conditions are met:</

USAGE MODES:

Width Expansion

Word width may be increased simply by connecting the corresponding input control signals of multiple devices. Status flags ($\overline{EF}$, $\overline{FF}$ and $\overline{HF}$) can be detected from any one device. Figure 13 demonstrates an 18-bit word width by using two IDT7203/7204/7205/7206/7207/7208s. Any word width can be attained by adding additional IDT7203/7204/7205/7206/7207/7208s (Figure 13).

Bidirectional Operation

Applications which require data buffering between two systems (each system capable of Read and Write operations) can be achieved by pairing IDT7203/7204/7205/7206/7207/7208s as shown in Figure 16. Both Depth Expansion and Width Expansion may be used in this mode.

Data Flow-Through

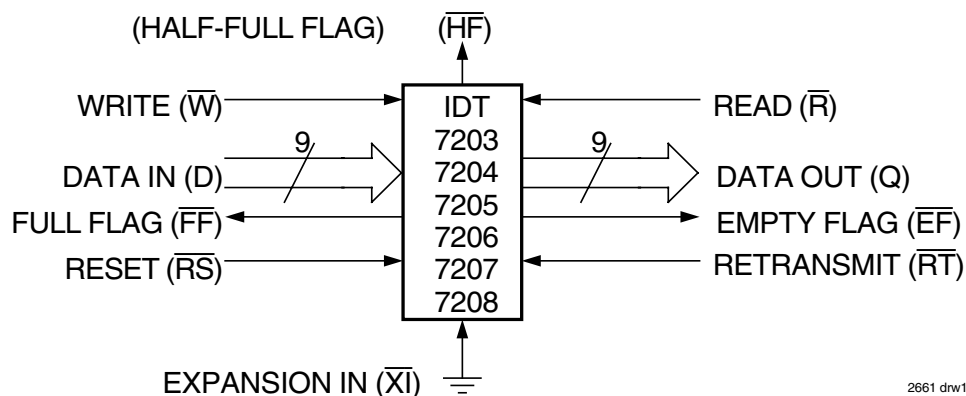
Two types of flow-through modes are permitted, a read flow-through and write flow-through mode. For the read flow-through mode (Figure 17), the

FIFO permits a reading of a single word after writing one word of data into an empty FIFO. The data is enabled on the bus in ($t_{WEF} + t_A$) ns after the rising edge of $\overline{W}$, called the first write edge, and it remains on the bus until the $\overline{R}$ line is raised from LOW-to-HIGH, after which the bus would go into a three-state mode after t_{RHZ} ns. The $\overline{EF}$ line would have a pulse showing temporary deassertion and then would be asserted.

In the write flow-through mode (Figure 18), the FIFO permits the writing of a single word of data immediately after reading one word of data from a full FIFO. The $\overline{R}$ line causes the $\overline{FF}$ to be deasserted but the $\overline{W}$ line being LOW causes it to be asserted again in anticipation of a new data word. On the rising edge of $\overline{W}$, the new word is loaded in the FIFO. The $\overline{W}$ line must be toggled when $\overline{FF}$ is not asserted to write new data in the FIFO and to increment the write pointer.

Compound Expansion

The two expansion techniques described above can be applied together in a straightforward manner to achieve large FIFO arrays (see Figure 15).



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Figure 12. Block Diagram of 2,048 x 9, 4,096 x 9, 8,192 x 9, 16,384 x 9, 32,768 x 9, 65,536 x 9 FIFO Used in Single Device Mode

TRUTH TABLES

TABLE 1 – RESET AND RETRANSMIT

SINGLE DEVICE CONFIGURATION/WIDTH EXPANSION MODE

Mode	Inputs			Internal Status		Outputs		
	$\overline{RS}$	$\overline{FL/RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$	$\overline{HF}$
Reset	0	X	0	Location Zero	Location Zero	0	1	1
Retransmit	1	0	0	Location Zero	Unchanged	X	X	X
Read/Write	1	1	0	Increment ⁽¹⁾	Increment ⁽¹⁾	X	X	X

NOTE:

1. Pointer will Increment if flag is HIGH.

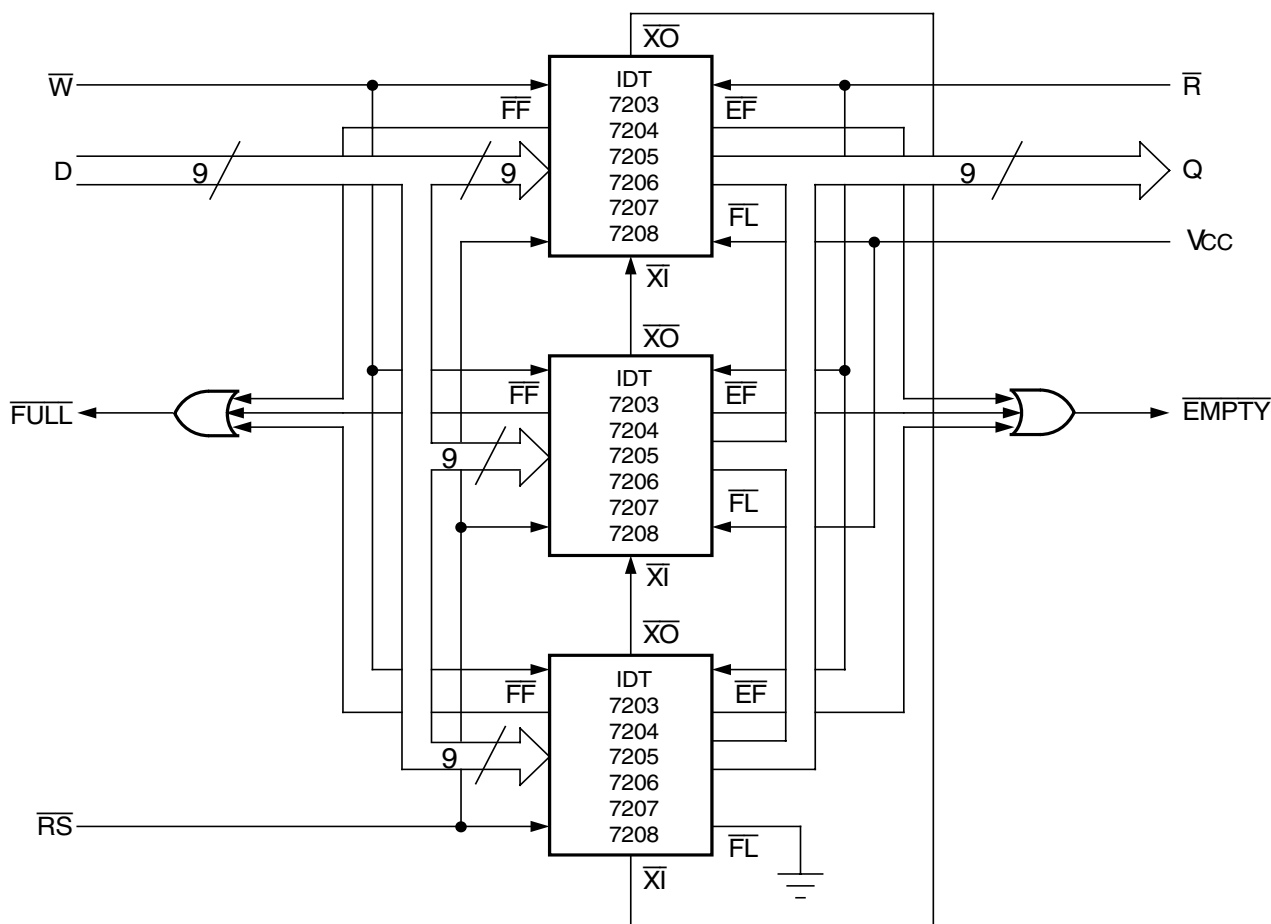
TABLE 2 – RESET AND FIRST LOAD

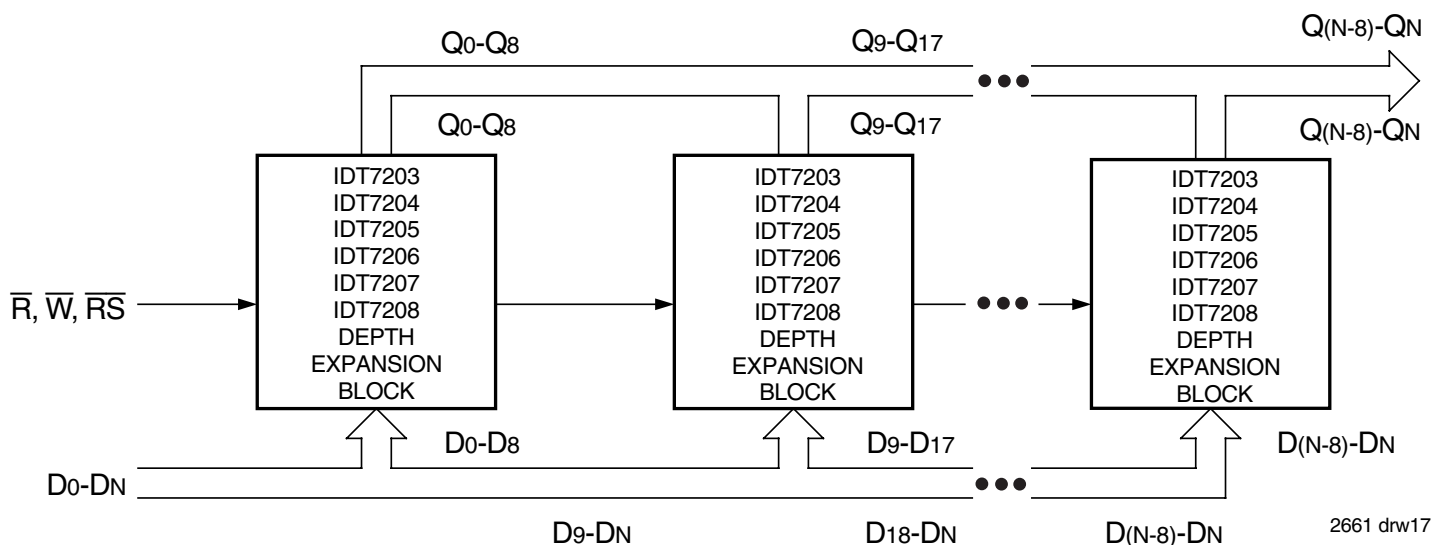
DEPTH EXPANSION/COMPOUND EXPANSION MODE

Mode	Inputs			Internal Status		Outputs	
	$\overline{RS}$	$\overline{FL/RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$
Reset First Device	0	0	(1)	Location Zero	Location Zero	0	1
Reset All Other Devices	0	1	(1)	Location Zero	Location Zero	0	1
Read/Write	1	X	(1)	X	X	X	X

NOTES:

1. $\overline{XI}$ is connected to $\overline{XO}$ of previous device. See Figure 14.
2. $\overline{RS}$ = Reset Input, $\overline{FL/RT}$ = First Load/Retransmit, $\overline{EF}$ = Empty Flag Output, $\overline{FF}$ = Full Flag Output, $\overline{XI}$ = Expansion Input, $\overline{HF}$ = Half-Full Flag Output





NOTES:

1. For depth expansion block see section on Depth Expansion and Figure 14.
2. For Flag detection see section on Width Expansion and Figure 13..

Figure 15. Compound FIFO Expansion

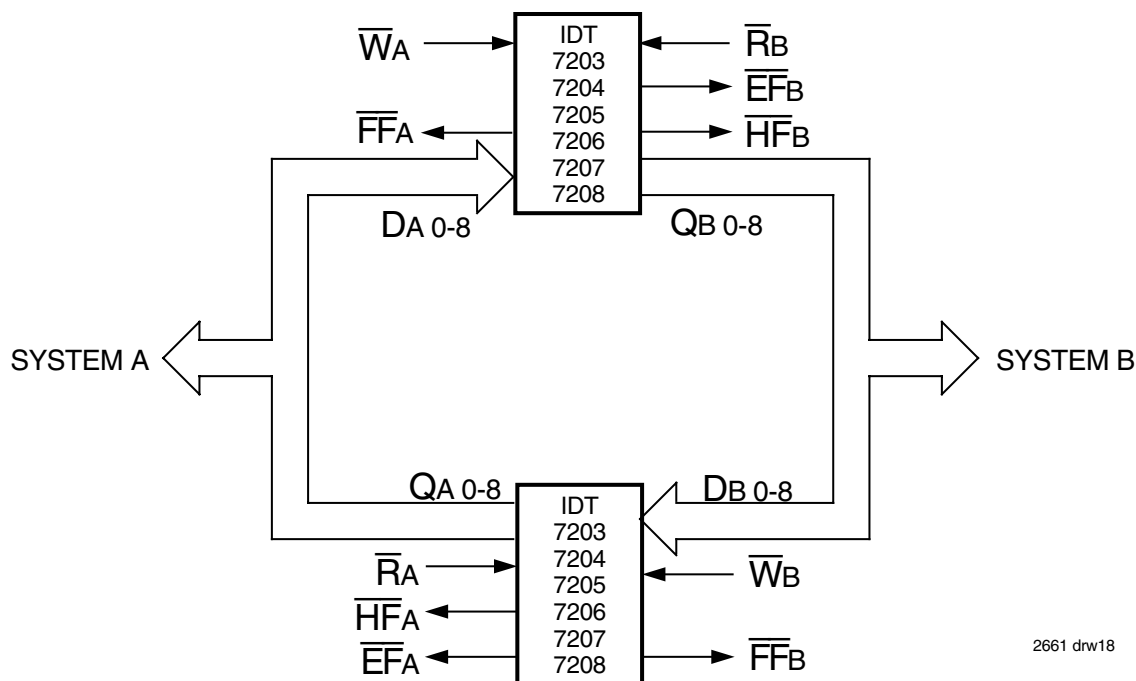


Figure 16. Bidirectional FIFO Operation

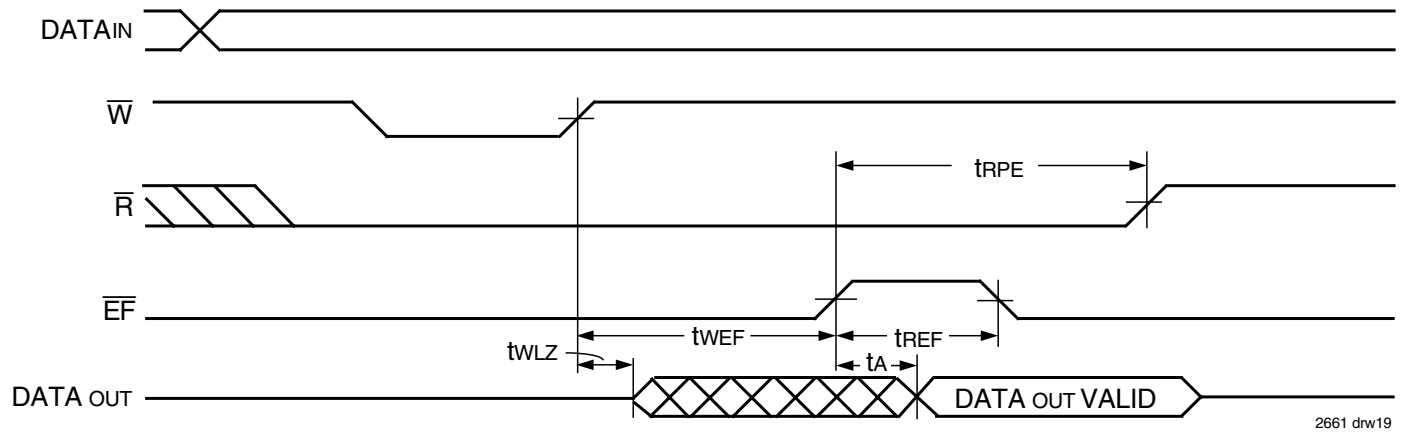


Figure 17. Read Data Flow-Through Mode

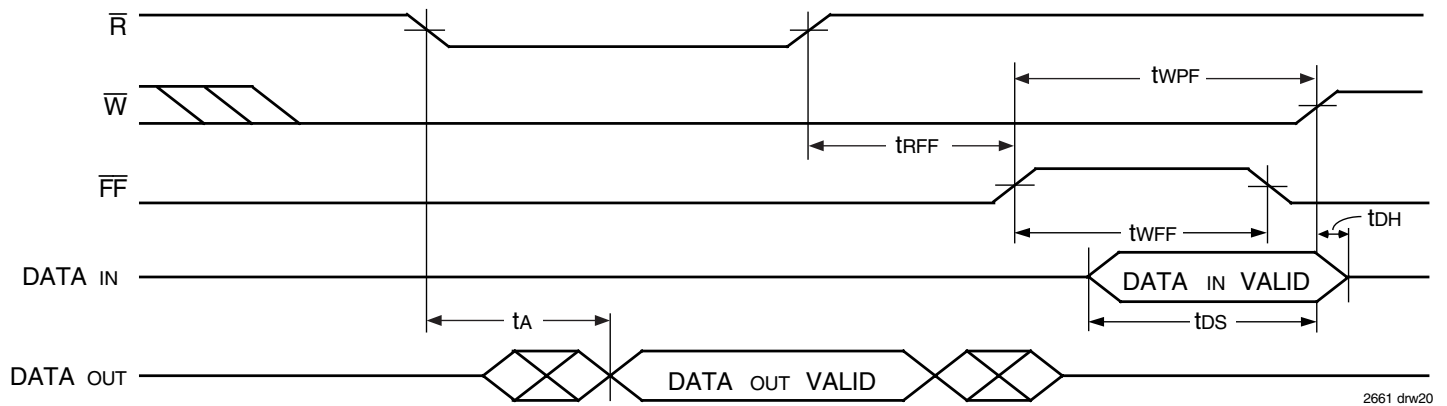
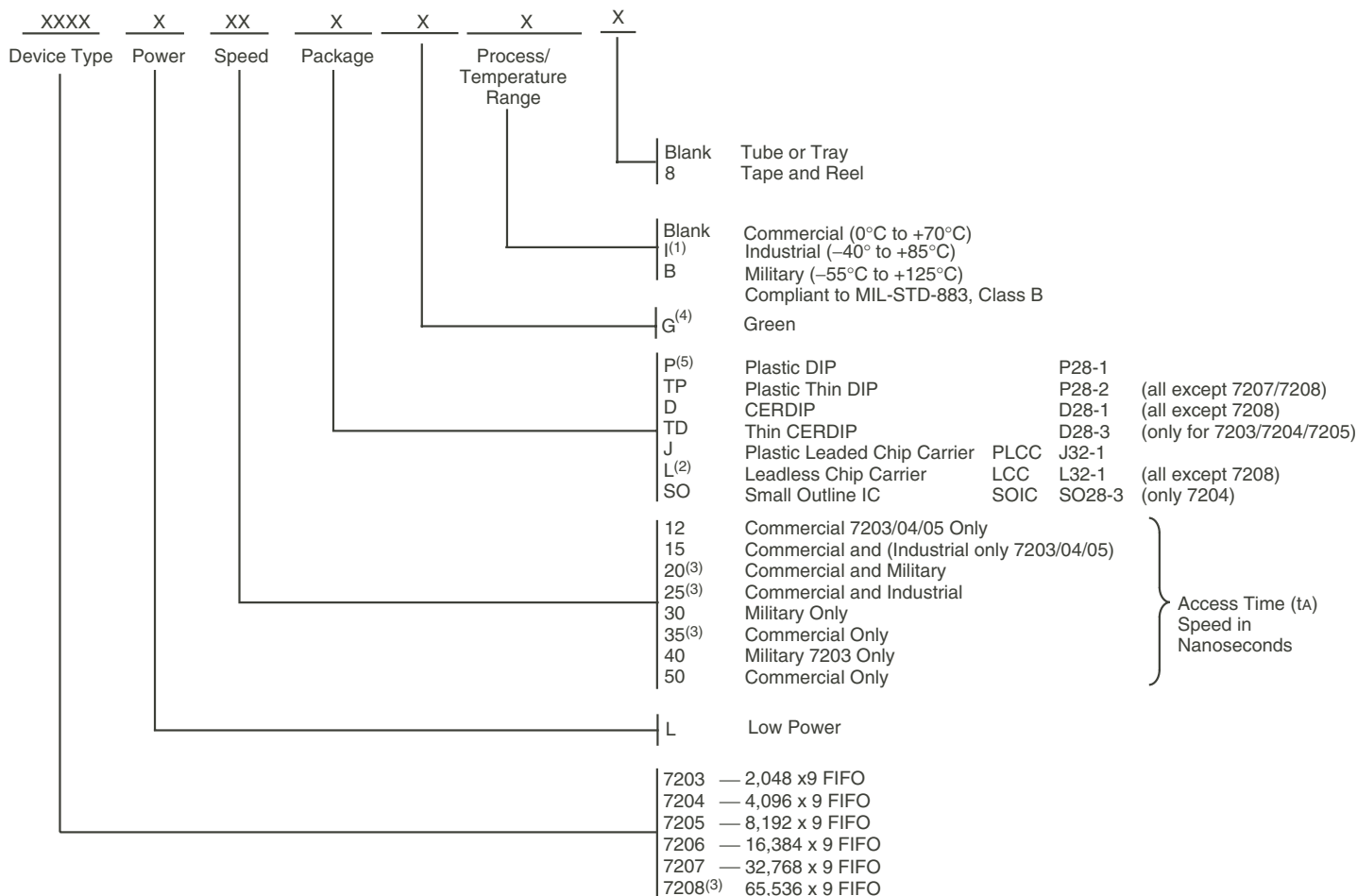


Figure 18. Write Data Flow-Through Mode

ORDERING INFORMATION



2661 drw21

NOTES:

- Industrial temperature range product for 15ns and 25ns speed grades are available as a standard device for IDT7203/7204/7205, and 25ns speed grade only is available as a standard device for IDT7206/7207/7208. All other speed grades are available by special order.
- The LCC is only available in the military temperature range.
- The IDT7208 is only available in commercial speed grades of 20, 25 and 35 ns.
- Green parts are available. For specific speeds and packages contact your local sales office.
- For "P", Plastic Dip, when ordering green package, the suffix is "PDG".

DATA SHEET HISTORY

05/10/2001	pgs. 2, 3, 4, 5, 11 and 14.
05/30/2001	pg. 2.
04/03/2006	pgs. 1 and 14.
10/22/2008	pg. 14.



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- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

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