

# PMF370XN

# N-channel TrenchMOS extremely low level FET

**Product data sheet** 

### 1. General description

Extremely low level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product is designed and qualified for use in computing, communications, consumer and industrial applications only.

### 2. Features and benefits

- Low conduction losses due to low on-state resistance
- · Low threshold voltage
- Saves PCB space due to small footprint (40 % smaller than SOT23)
- · Suitable for low gate drive sources
- · Surface-mounted package

### 3. Applications

- · Driver circuits
- Switching in portable appliances

### 4. Quick reference data

#### Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Тур	Max	Unit	
$V_{DS}$	drain-source voltage	25 °C ≤ T <sub>j</sub> ≤ 150 °C		-	-	30	V	
I <sub>D</sub>	drain current	V <sub>GS</sub> = 4.5 V; T <sub>sp</sub> = 25 °C		-	-	0.87	Α	
P <sub>tot</sub>	total power dissipation	T <sub>sp</sub> = 25 °C		-	-	0.56	W	
Static characte	Static characteristics							
R <sub>DSon</sub>	drain-source on-state resistance	$V_{GS} = 4.5 \text{ V}; I_D = 0.2 \text{ A}; T_j = 25 \text{ °C}$		-	370	440	mΩ	



### N-channel TrenchMOS extremely low level FET

# 5. Pinning information

#### **Table 2. Pinning information**

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	<u></u> 3	D
2	S	source		
3	D	drain		G—(FA)
				mbb076 S
			SC-70 (SOT323)	

# 6. Ordering information

#### **Table 3. Ordering information**

Type number	Package					
	Name	Description	Version			
PMF370XN	SC-70	plastic surface-mounted package; 3 leads	SOT323			

# 7. Marking

#### Table 4. Marking codes

Type number	Marking code[1]
PMF370XN	F6%

[1] % = placeholder for manufacturing site code

### N-channel TrenchMOS extremely low level FET

# 8. Limiting values

#### **Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134)

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>DS</sub>	drain-source voltage	25 °C ≤ T <sub>j</sub> ≤ 150 °C	-	30	V
$V_{DGR}$	drain-gate voltage	$25 \degree C ≤ Tj ≤ 150 \degree C; RGS = 20 kΩ$	-	30	V
V <sub>GS</sub>	gate-source voltage		-12	12	V
I <sub>D</sub>	drain current	V <sub>GS</sub> = 4.5 V; T <sub>sp</sub> = 25 °C	-	0.87	Α
		V <sub>GS</sub> = 4.5 V; T <sub>sp</sub> = 100 °C	-	0.55	Α
I <sub>DM</sub>	peak drain current	$T_{sp}$ = 25 °C; pulsed; $t_p \le 10 \mu s$	-	1.74	Α
P <sub>tot</sub>	total power dissipation	T <sub>sp</sub> = 25 °C	-	0.56	W
Tj	junction temperature		-55	150	°C
T <sub>stg</sub>	storage temperature		-55	150	°C
I <sub>S</sub>	source current	T <sub>sp</sub> = 25 °C	-	0.47	Α
I <sub>SM</sub>	peak source current	pulsed; t <sub>p</sub> ≤ 10 μs; T <sub>sp</sub> = 25 °C	-	0.94	Α

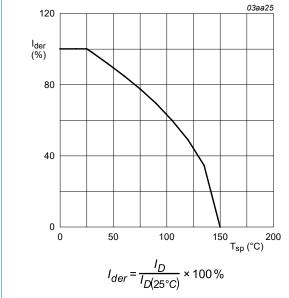


Fig. 1. Normalized continuous drain current as a function of solder point temperature

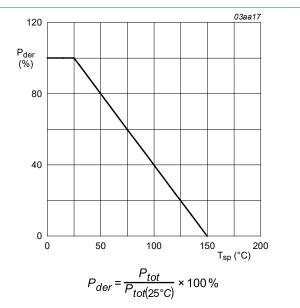
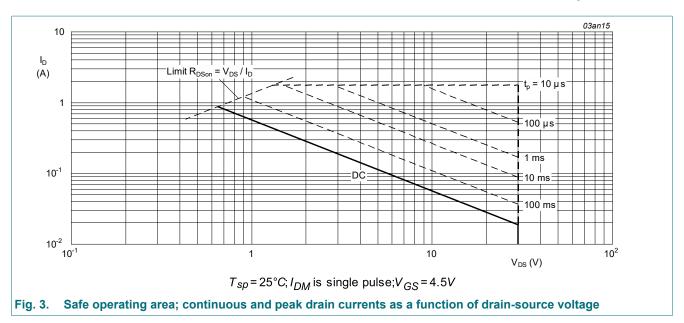


Fig. 2. Normalized total power dissipation as a function of solder point temperature

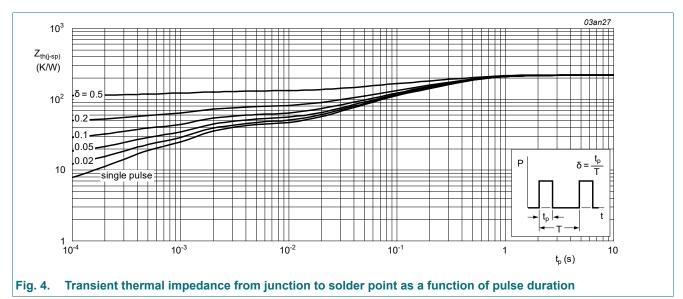


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### 9. Thermal characteristics

**Table 6. Thermal characteristics** 

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
11(J-3P)	thermal resistance from junction to solder point		-	-	220	K/W
	junction to solder point					



### N-channel TrenchMOS extremely low level FET

# 10. Characteristics

### **Table 7. Characteristics**

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static chara	acteristics					
V <sub>(BR)DSS</sub>	drain-source	I <sub>D</sub> = 250 μA; V <sub>GS</sub> = 0 V; T <sub>j</sub> = -55 °C	27	-	-	V
	breakdown voltage	I <sub>D</sub> = 250 μA; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C	30	-	-	V
$V_{GSth}$	gate-source threshold	I <sub>D</sub> = 250 μA; V <sub>DS</sub> = V <sub>GS</sub> ; T <sub>j</sub> = -55 °C	-	-	1.8	V
	voltage	I <sub>D</sub> = 250 μA; V <sub>DS</sub> = V <sub>GS</sub> ; T <sub>j</sub> = 150 °C	0.35	-	-	V
		I <sub>D</sub> = 250 μA; V <sub>DS</sub> = V <sub>GS</sub> ; T <sub>j</sub> = 25 °C	0.5	1	1.5	V
I <sub>DSS</sub>	drain leakage current	V <sub>DS</sub> = 30 V; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	-	1	μΑ
		V <sub>DS</sub> = 30 V; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 70 °C	-	-	2	μA
		V <sub>DS</sub> = 30 V; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 150 °C	-	-	10	μΑ
I <sub>GSS</sub>	gate leakage current	V <sub>GS</sub> = 12 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	10	100	nA
		V <sub>GS</sub> = -12 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	10	100	nA
R <sub>DSon</sub>	drain-source on-state resistance	$V_{GS} = 2.5 \text{ V}; I_D = 0.1 \text{ A}; T_j = 25 ^{\circ}\text{C}$	-	550	650	mΩ
		V <sub>GS</sub> = 4.5 V; I <sub>D</sub> = 0.2 A; T <sub>j</sub> = 150 °C	-	629	748	mΩ
		$V_{GS} = 4.5 \text{ V}; I_D = 0.2 \text{ A}; T_j = 25 ^{\circ}\text{C}$	-	370	440	mΩ
Dynamic ch	aracteristics					
Q <sub>G(tot)</sub>	total gate charge	V <sub>DS</sub> = 15 V; I <sub>D</sub> = 1 A; V <sub>GS</sub> = 4.5 V;	-	0.65	-	nC
Q <sub>GS</sub>	gate-source charge	T <sub>j</sub> = 25 °C	-	0.14	-	nC
Q <sub>GD</sub>	gate-drain charge	1	-	0.18	-	nC
C <sub>iss</sub>	input capacitance	V <sub>DS</sub> = 25 V; f = 1 MHz; V <sub>GS</sub> = 0 V;	-	37	-	pF
C <sub>oss</sub>	output capacitance	T <sub>j</sub> = 25 °C	-	8.5	-	pF
C <sub>rss</sub>	reverse transfer capacitance		-	5.5	-	pF
t <sub>d(on)</sub>	turn-on delay time	$V_{DS}$ = 15 V; $R_L$ = 15 $\Omega$ ; $V_{GS}$ = 4.5 V;	-	6.5	-	ns
t <sub>r</sub>	rise time	$R_{G(ext)} = 6 \Omega; T_j = 25 °C$	-	9.5	-	ns
t <sub>d(off)</sub>	turn-off delay time	]	-	14	-	ns
t <sub>f</sub>	fall time	1	-	5.5	-	ns
Source-drai	in diode		1			
$V_{SD}$	source-drain voltage	I <sub>S</sub> = 0.3 A; V <sub>GS</sub> = 0 V; T <sub>i</sub> = 25 °C	-	0.81	1.2	V

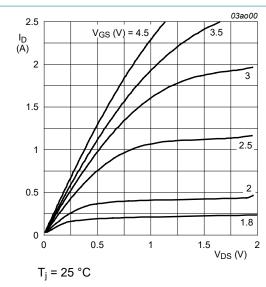


Fig. 5. Output characteristics: drain current as a function of drain-source voltage; typical values

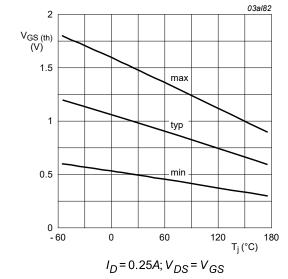


Fig. 7. Gate-source threshold voltage as a function of junction temperature

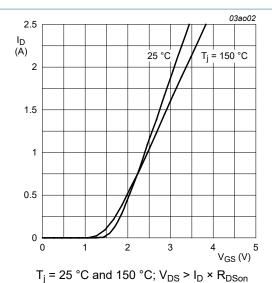


Fig. 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values

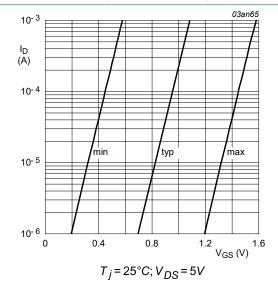


Fig. 8. Subthreshold drain current as a function of gate-source voltage

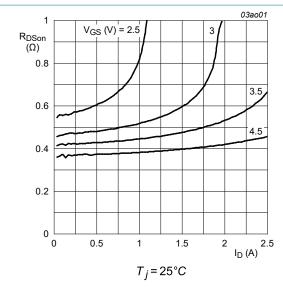


Fig. 9. Drain-source on-state resistance as a function of drain current; typical values

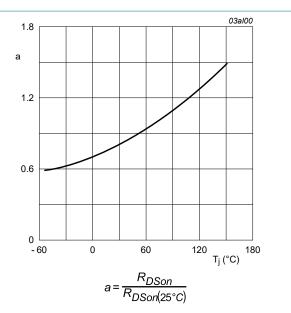


Fig. 10. Normalized drain-source on-state resistance factor as a function of junction temperature

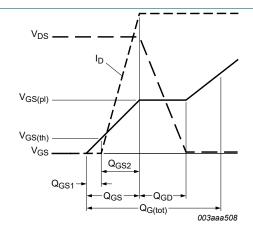


Fig. 11. Gate charge waveform definitions

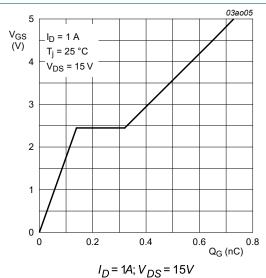


Fig. 12. Gate-source voltage as a function of gate charge; typical values

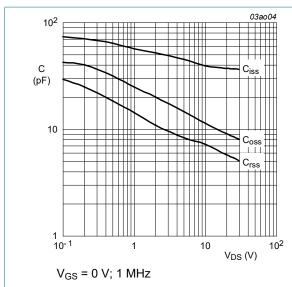
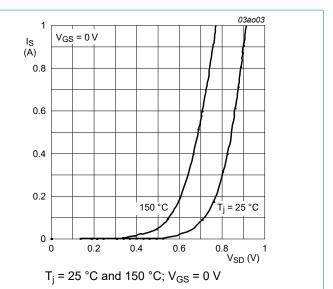


Fig. 13. Input, output and reverse transfer capacitances | Fig. 14. Source current as a function of source-drain as a function of drain-source voltage; typical values



voltage; typical values

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# 11. Package outline

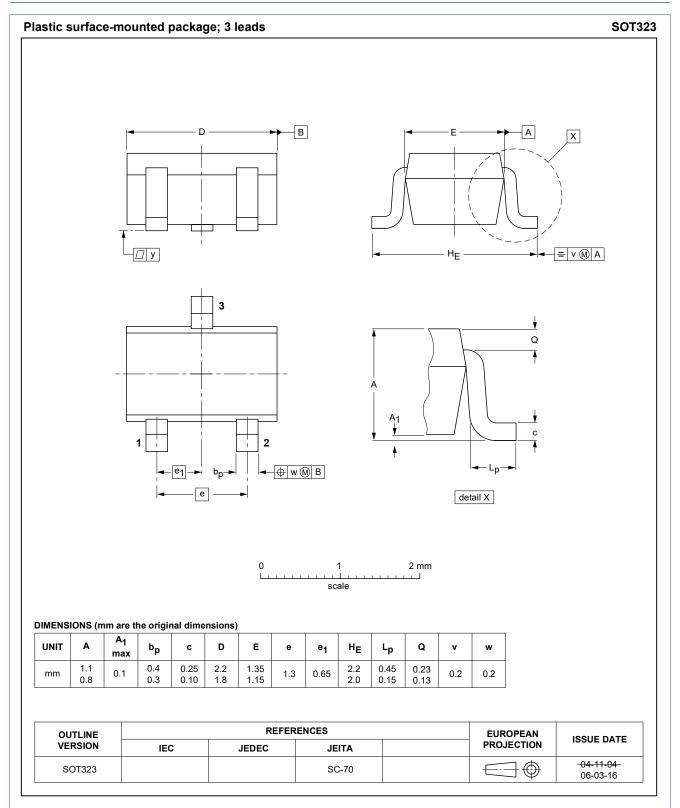
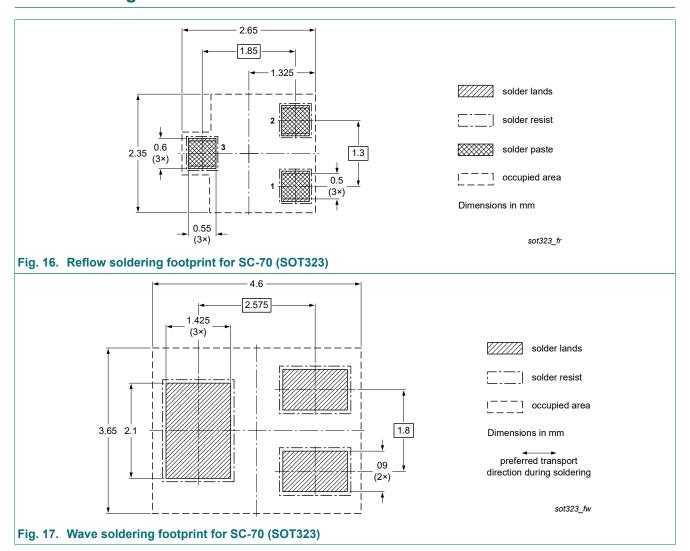


Fig. 15. Package outline SC-70 (SOT323)

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# 12. Soldering



# N-channel TrenchMOS extremely low level FET

# 13. Revision history

#### **Table 8. Revision history**

Table 0. INEVISION II	istory			
Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PMF370XN v.4	20190705	Product data sheet	-	PMF370XN v.3
Modifications:	<ul> <li>Legal texts ha</li> </ul>	conditions for V <sub>(BR)DSS</sub> revise we been adapted to the new o this data sheet has been rede	company name where a	• • •
PMF370XN v.3	20080620	Product data sheet	-	PMF370XN v.2
PMF370XN v.2	20051206	Product data sheet	-	PMF370XN v.1
PMF370XN v.1	20040211	Product data sheet	-	-

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#### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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