Low-Noise, 8-Channel, 24-Bit Analog Front-End for Biopotential Measurements

Check for Samples: ADS1299

FEATURES

- **Eight Low-Noise PGAs and Eight High-Resolution Simultaneous-Sampling ADCs**
- **Very Low Input-Referred Noise: 1.0 μV_{PP} (70-Hz BW)**
- **Low Power: 5 mW/channel**
- **Input Bias Current: 300 pA**
- **Data Rate: 250 SPS to 16 kSPS**
- **CMRR: –110 dB**
- **Programmable Gain: 1, 2, 4, 6, 8, 12, or 24**
- **Unipolar or Bipolar Supplies:**
  - **Analog: 4.75 V to 5.25 V**
  - **Digital: 1.8 V to 3.6 V**
- **Built-In Bias Drive Amplifier, Lead-Off Detection, Test Signals**
- **Built-In Oscillator**
- **Internal or External Reference**
- **Flexible Power-Down, Standby Mode**
- **Pin-Compatible with the ADS1298IPAG**
- **SPI™-Compatible Serial Interface**
- **Operating Temperature Range: –40°C to +85°C**

APPLICATIONS

- **Medical Instrumentation (EEG and ECG) Including:**
  - **EEG, Bispectral index (BIS), Evoked audio potential (EAP), Sleep study monitor**
- **High-Precision, Simultaneous, Multichannel Signal Acquisition**

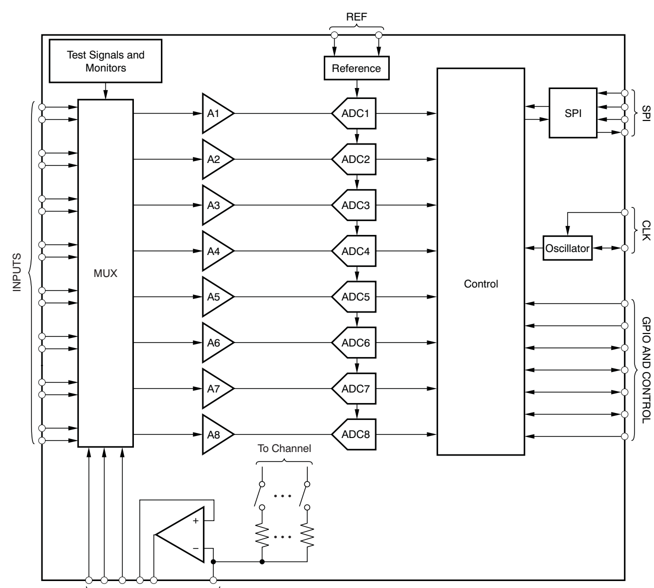
DESCRIPTION

The ADS1299 is a low-noise, multichannel, simultaneous-sampling, 24-bit, delta-sigma (ΔΣ) analog-to-digital converter (ADC) with a built-in programmable gain amplifier (PGA), internal reference, and an onboard oscillator. The ADS1299 incorporates all commonly-required features for electroencephalogram (EEG) applications.

With its high levels of integration and exceptional performance, the ADS1299 enables the creation of scalable medical instrumentation systems at significantly reduced size, power, and overall cost.

The ADS1299 has a flexible input multiplexer per channel that can be independently connected to the internally-generated signals for test, temperature, and lead-off detection. Additionally, any configuration of input channels can be selected for derivation of the patient bias output signal. The ADS1299 operates at data rates from 250 SPS to 16 kSPS. Lead-off detection can be implemented internal to the device, either with an external pull-up or pull-down resistor or an excitation current sink or source.

Multiple ADS1299 devices can be cascaded in high channel count systems in a daisy-chain configuration. The ADS1299 is offered in a TQFP-64 package specified from –40°C to +85°C.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

FAMILY AND ORDERING INFORMATION(1)

PRODUCT	PACKAGE OPTION	NUMBER OF CHANNELS	ADC RESOLUTION	MAXIMUM SAMPLE RATE (kSPS)	OPERATING TEMPERATURE RANGE
ADS1299IPAG	TQFP	8	24	16	–40°C to +85°C

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

		VALUE	UNIT
AVDD to AVSS		–0.3 to +5.5	V
DVDD to DGND		–0.3 to +3.9	V
AVSS to DGND		–3 to +0.2	V
V_{REF} input to AVSS		AVSS – 0.3 to AVDD + 0.3	V
Analog input to AVSS		AVSS – 0.3 to AVDD + 0.3	V
Digital input voltage to DGND		–0.3 to DVDD + 0.3	V
Digital output voltage to DGND		–0.3 to DVDD + 0.3	V
Input current	Momentary	100	mA
	Continuous	10	mA
Temperature	Operating range, T_A	–40 to +85	°C
	Storage range, T_{stg}	–60 to +150	°C
	Maximum junction, T_J	+150	°C
Electrostatic discharge (ESD) ratings	Human body model (HBM) JEDEC standard 22, test method A114-C.01, all pins	±1000	V
	Charged device model (CDM) JEDEC standard 22, test method C101, all pins	±500	V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

ELECTRICAL CHARACTERISTICS

Minimum and maximum specifications apply from –40°C to +85°C. Typical specifications are at +25°C. All specifications are at DVDD = 3.3 V, AVDD – AVSS = 5 V, V_{REF} = 4.5 V, external f_{CLK} = 2.048 MHz, data rate = 250 SPS, and gain = 12, unless otherwise noted.

PARAMETER		TEST CONDITIONS	ADS1299 MIN	ADS1299 TYP	ADS1299 MAX	UNIT
ANALOG INPUTS						
	Full-scale differential input voltage (AINP – AINN)			±V_{REF} / gain		V
	Input common-mode range			See the *Input Common-Mode Range* subsection of the *PGA Settings and Input Range* section		
C_i	Input capacitance			20		pF
I_{IB}	Input bias current	T_A = +25°C, input = 2.5 V			±300	pA
		T_A = –40°C to +85°C, input = 2.5 V		±300		pA
	DC input impedance	No lead-off	1000			MΩ
		Current source lead-off detection ($I_{LEADOFF}$ = 6 nA)		500		MΩ
PGA PERFORMANCE						
	Gain settings			1, 2, 4, 6, 8, 12, 24		
BW	Bandwidth			See Table 5		
ADC PERFORMANCE						
	Resolution		24			Bits
DR	Data rate	f_{CLK} = 2.048 MHz	250		16000	SPS
CHANNEL PERFORMANCE (DC Performance)						
	Input-referred noise (0.01 Hz to 70 Hz)	10 seconds of data, gain = 24[1]		1.0		μV_{PP}
		250 points, 1 second of data, gain = 24, T_A = +25°C		1.0	1.35	μV_{PP}
		250 points, 1 second of data, gain = 24, T_A = –40°C to +85°C		1.0	1.6	μV_{PP}
		All other sample rates and gain settings		See *Noise Measurements* section		
INL	Integral nonlinearity	Full-scale with gain = 12, best fit		8		ppm
E_O	Offset error			60		µV
	Offset error drift			80		nV/°C
E_G	Gain error	Excluding voltage reference error		0.1	±0.5	% of FS
	Gain drift	Excluding voltage reference drift		3		ppm/°C
	Gain match between channels			0.2		% of FS
CHANNEL PERFORMANCE (AC Performance)						
CMRR	Common-mode rejection ratio	f_{CM} = 50 Hz and 60 Hz[2]	–110	–120		dB
PSRR	Power-supply rejection ratio	f_{PS} = 50 Hz and 60 Hz		96		dB
	Crosstalk	f_{IN} = 50 Hz and 60 Hz		–110		dB
SNR	Signal-to-noise ratio	V_{IN} = –2 dBFs, f_{IN} = 10-Hz input, gain = 12		121		dB
THD	Total harmonic distortion	V_{IN} = –0.5 dBFs, f_{IN} = 10 Hz		–99		dB

(1) Noise data measured in a 10-second interval. Test not performed in production. Input-referred noise is calculated with the input shorted (without electrode resistance) over a 10-second interval.
(2) CMRR is measured with a common-mode signal of AVSS + 0.3 V to AVDD – 0.3 V. The values indicated are the minimum of the eight channels.

ELECTRICAL CHARACTERISTICS (continued)

Minimum and maximum specifications apply from –40°C to +85°C. Typical specifications are at +25°C. All specifications are at DVDD = 3.3 V, AVDD – AVSS = 5 V, V_{REF} = 4.5 V, external f_{CLK} = 2.048 MHz, data rate = 250 SPS, and gain = 12, unless otherwise noted.

PARAMETER			TEST CONDITIONS	ADS1299 MIN	ADS1299 TYP	ADS1299 MAX	UNIT
PATIENT BIAS AMPLIFIER							
	Integrated noise		BW = 150 Hz		2		μV_{RMS}
GBP	Gain bandwidth product		50 kΩ || 10 pF load, gain = 1		100		kHz
SR	Slew rate		50 kΩ || 10 pF load, gain = 1		0.07		V/µs
THD	Total harmonic distortion		f_{IN} = 10 Hz, gain = 1		–80		dB
CMIR	Common-mode input range			AVSS + 0.3		AVDD – 0.3	V
I_{SC}	Short-circuit current				1.1		mA
	Quiescent power consumption				20		µA
LEAD-OFF DETECT							
	Frequency		Continuous		0, f_{DR} / 4 See *Register Map* section for settings		Hz
	Frequency		One time or periodic		7.8, 31.2		Hz
	Current		ILEAD_OFF[1:0] = 00		6		nA
	Current		ILEAD_OFF[1:0] = 01		24		nA
	Current		ILEAD_OFF[1:0] = 10		6		µA
	Current		ILEAD_OFF[1:0] = 11		24		µA
	Current accuracy				±20		%
	Comparator threshold accuracy				±30		mV
EXTERNAL REFERENCE							
$V_{I(ref)}$	Reference input voltage		5-V supply, V_{REF} = (VREFP – VREFN)		4.5		V
VREFN	Negative input				AVSS		V
VREFP	Positive input				AVSS + 4.5		V
	Input impedance				5.6		kΩ
INTERNAL REFERENCE							
V_O	Output voltage				4.5		V
	V_{REF} accuracy				±0.2		%
	Drift		T_A = –40°C to +85°C		35		ppm
	Start-up time				150		ms
SYSTEM MONITORS							
	Reading error	Analog supply			2		%
	Reading error	Digital supply			2		%
	Device wake up		From power-up to $\overline{DRDY}$ low		150		ms
	Device wake up		STANDBY mode		31.25		µs
	Temperature sensor reading	Voltage	T_A = +25°C		145		mV
	Temperature sensor reading	Coefficient			490		µV/°C
	Test signal	Signal frequency	See *Register Map* section for settings		f_{CLK} / 2^{21}, f_{CLK} / 2^{20}		Hz
	Test signal	Signal voltage	See *Register Map* section for settings		±1, ±2		mV
	Test signal	Accuracy			±2		%

ELECTRICAL CHARACTERISTICS (continued)

Minimum and maximum specifications apply from –40°C to +85°C. Typical specifications are at +25°C. All specifications are at DVDD = 3.3 V, AVDD – AVSS = 5 V, V_{REF} = 4.5 V, external f_{CLK} = 2.048 MHz, data rate = 250 SPS, and gain = 12, unless otherwise noted.

PARAMETER			TEST CONDITIONS	ADS1299 MIN	ADS1299 TYP	ADS1299 MAX	UNIT
CLOCK							
	Internal oscillator clock frequency		Nominal frequency		2.048		MHz
	Internal clock accuracy		T_A = +25°C			±0.5	%
			–40°C ≤ T_A ≤ +85°C			±2.5	%
	Internal oscillator start-up time				20		µs
	Internal oscillator power consumption				120		µW
	External clock input frequency		CLKSEL pin = 0	1.5	2.048	2.25	MHz
DIGITAL INPUT/OUTPUT (DVDD = 1.8 V to 3.6 V)							
V_{IH}	Logic level, input voltage	High		0.8 DVDD		DVDD + 0.1	V
V_{IL}		Low		–0.1		0.2 DVDD	V
V_{OH}	Logic level, output voltage	High	I_{OH} = –500 µA	0.9 DVDD			V
V_{OL}		Low	I_{OL} = +500 µA			0.1 DVDD	V
I_{IN}	Input current		0 V < $V_{DigitalInput}$ < DVDD	–10		+10	µA
POWER-SUPPLY REQUIREMENTS							
	Analog supply (AVDD – AVSS)			4.75	5	5.25	V
DVDD	Digital supply			1.8	1.8	3.6	V
	AVDD – DVDD			–2.1		3.6	V
SUPPLY CURRENT (Bias Turned Off)							
I_{AVDD}	Normal mode		AVDD – AVSS = 5 V		7.14		mA
I_{DVDD}			DVDD = 3.3 V		1		mA
			DVDD = 1.8 V		0.5		mA
POWER DISSIPATION (Analog Supply = 5 V, Bias Amplifiers Turned Off)							
	Quiescent power dissipation		Normal mode		39	42	mW
			Power-down		10		µW
			Standby mode, internal reference		5.1		mW
	Quiescent power dissipation, per channel		Normal mode		4.3		mW
TEMPERATURE							
	Temperature range	Specified		–40		+85	°C
		Operating		–40		+85	°C
		Storage		–60		+150	°C

THERMAL INFORMATION

THERMAL METRIC(1)		ADS1299 PAG 64 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	43.3	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	36.5	
θ_{JB}	Junction-to-board thermal resistance	60.6	
ψ_{JT}	Junction-to-top characterization parameter	0.1	
ψ_{JB}	Junction-to-board characterization parameter	19.5	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

PARAMETRIC MEASUREMENT INFORMATION

NOISE MEASUREMENTS

The ADS1299 noise performance can be optimized by adjusting the data rate and PGA setting. When averaging is increased by reducing the data rate, the noise drops correspondingly. Increasing the PGA value reduces the input-referred noise, which is particularly useful when measuring low-level biopotential signals. Table 1 to Table 4 summarize the ADS1299 noise performance with a 5-V analog power supply. The data are representative of typical noise performance at T_A = +25°C. The data shown are the result of averaging the readings from multiple devices and are measured with the inputs shorted together. A minimum of 1000 consecutive readings are used to calculate the RMS and peak-to-peak noise for each reading. For the lower data rates, the ratio is approximately 6.6.

Table 1 shows measurements taken with an internal reference. The data are also representative of the ADS1299 noise performance when using a low-noise external reference such as the REF5025.

Table 1. Input-Referred Noise (μV_{RMS} / μV_{PP}) in Normal Mode 5-V Analog Supply and 4.5-V Reference(1)

DR BITS OF CONFIG1 REGISTER	OUTPUT DATA RATE (SPS)	–3-dB BANDWIDTH (Hz)	PGA GAIN = 1					PGA GAIN = 2				
			μV_{RMS}	μV_{PP}	SNR (dB)	NOISE-FREE BITS	ENOB	μV_{RMS}	μV_{PP}	SNR (dB)	NOISE-FREE BITS	ENOB
000	16000	4193	21.70	151.89	103.3	15.85	17.16	10.85	75.94	103.3	15.85	17.16
001	8000	2096	6.93	48.53	113.2	17.50	18.81	3.65	25.52	112.8	17.43	18.74
010	4000	1048	4.33	30.34	117.3	18.18	19.49	2.28	15.95	116.9	18.11	19.41
011	2000	524	3.06	21.45	120.3	18.68	19.99	1.61	11.29	119.9	18.60	19.91
100	1000	262	2.17	15.17	123.3	19.18	20.49	1.14	7.98	122.9	19.10	20.41
101	500	131	1.53	10.73	126.3	19.68	20.99	0.81	5.65	125.9	19.60	20.91
110	250	65	1.08	7.59	129.3	20.18	21.48	0.57	3.99	128.9	20.10	21.41
111	n/a	n/a	—	—	—	—	—	—	—	—	—	—

(1) At least 1000 consecutive readings were used to calculate the RMS and peak-to-peak noise values in this table.

Table 2. Input-Referred Noise (μV_{RMS} / μV_{PP}) in Normal Mode 5-V Analog Supply and 4.5-V Reference(1)

DR BITS OF CONFIG1 REGISTER	OUTPUT DATA RATE (SPS)	–3-dB BANDWIDTH (Hz)	PGA GAIN = 4					PGA GAIN = 6				
			μV_{RMS}	μV_{PP}	SNR (dB)	NOISE-FREE BITS	ENOB	μV_{RMS}	μV_{PP}	SNR (dB)	NOISE-FREE BITS	ENOB
000	16000	4193	5.60	39.23	103.0	15.81	17.12	3.87	27.10	102.7	15.76	17.06
001	8000	2096	1.98	13.87	112.1	17.31	18.62	1.31	9.19	112.1	17.32	18.62
010	4000	1048	1.24	8.66	116.1	17.99	19.29	0.93	6.50	115.1	17.82	19.12
011	2000	524	0.88	6.13	119.2	18.49	19.79	0.66	4.60	118.1	18.32	19.62
100	1000	262	0.62	4.34	122.2	18.99	20.29	0.46	3.25	121.1	18.81	20.12
101	500	131	0.44	3.07	125.2	19.49	20.79	0.33	2.30	124.1	19.31	20.62
110	250	65	0.31	2.16	128.2	19.99	21.30	0.23	1.62	127.2	19.82	21.13
111	n/a	n/a	—	—	—	—	—	—	—	—	—	—

(1) At least 1000 consecutive readings were used to calculate the RMS and peak-to-peak noise values in this table.

Table 3. Input-Referred Noise (μV_{RMS} / μV_{PP}) in Normal Mode 5-V Analog Supply and 4.5-V Reference(1)

DR BITS OF CONFIG1 REGISTER	OUTPUT DATA RATE (SPS)	–3-dB BANDWIDTH (Hz)	PGA GAIN = 8					PGA GAIN = 12				
			μV_{RMS}	μV_{PP}	SNR (dB)	NOISE-FREE BITS	ENOB	μV_{RMS}	μV_{PP}	SNR (dB)	NOISE-FREE BITS	ENOB
000	16000	4193	3.05	21.32	102.3	15.69	16.99	2.27	15.89	101.3	15.53	16.83
001	8000	2096	1.11	7.80	111.0	17.14	18.45	0.92	6.41	109.2	16.84	18.14
010	4000	1048	0.79	5.52	114.0	17.64	18.95	0.65	4.53	112.2	17.34	18.64
011	2000	524	0.56	3.90	117.1	18.14	19.44	0.46	3.20	115.2	17.84	19.14
100	1000	262	0.39	2.76	120.1	18.64	19.94	0.32	2.26	118.3	18.34	19.65
101	500	131	0.28	1.95	123.1	19.14	20.44	0.23	1.61	121.2	18.83	20.14
110	250	65	0.20	1.38	126.1	19.64	20.95	0.16	1.13	124.3	19.34	20.65
111	n/a	n/a	—	—	—	—	—	—	—	—	—	—

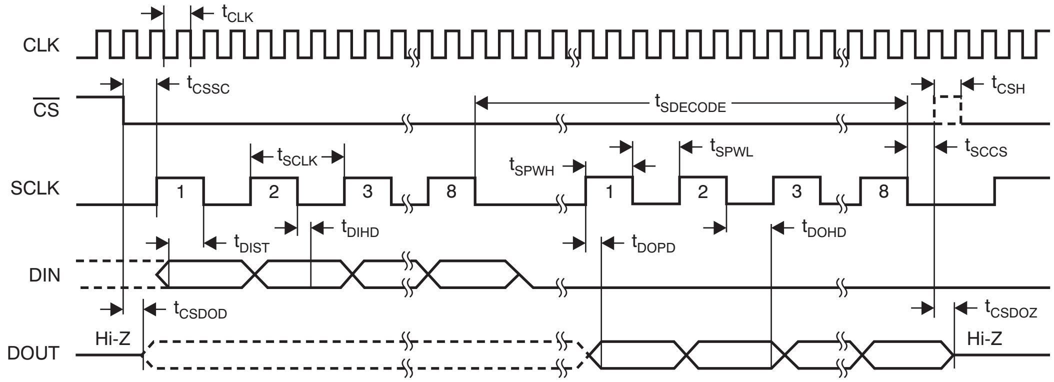
(1) At least 1000 consecutive readings were used to calculate the RMS and peak-to-peak noise values in this table.

Table 4. Input-Referred Noise (μV_{RMS} / μV_{PP}) in Normal Mode 5-V Analog Supply and 4.5-V Reference(1)

DR BITS OF CONFIG1 REGISTER	OUTPUT DATA RATE (SPS)	–3-dB BANDWIDTH (Hz)	PGA GAIN = 24				
			μV_{RMS}	μV_{PP}	SNR (dB)	NOISE-FREE BITS	ENOB
000	16000	4193	1.66	11.64	98.0	14.98	16.28
001	8000	2096	0.80	5.57	104.4	16.04	17.35
010	4000	1048	0.56	3.94	107.4	16.54	17.84
011	2000	524	0.40	2.79	110.4	17.04	18.35
100	1000	262	0.28	1.97	113.5	17.54	18.85
101	500	131	0.20	1.39	116.5	18.04	19.35
110	250	65	0.14	0.98	119.5	18.54	19.85
111	n/a	n/a	—	—	—	—	—

(1) At least 1000 consecutive readings were used to calculate the RMS and peak-to-peak noise values in this table.

TIMING CHARACTERISTICS



NOTE: SPI settings are CPOL = 0 and CPHA = 1.

Figure 1. Serial Interface Timing

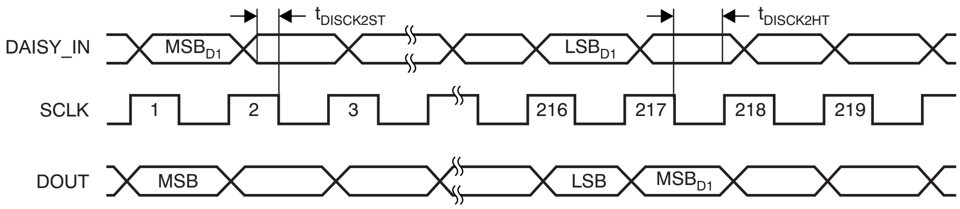


Figure 2. Daisy-Chain Interface Timing

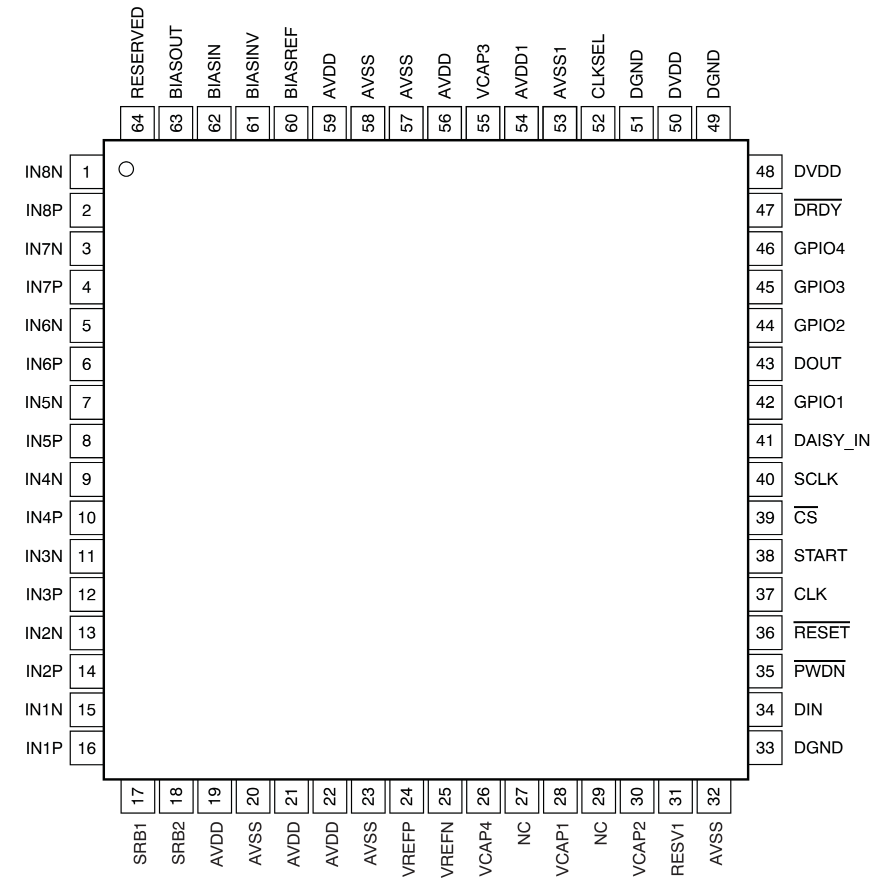
Timing Requirements For Figure 1 and Figure 2(1)

PARAMETER	DESCRIPTION	2.7 V ≤ DVDD ≤ 3.6 V MIN	TYP	MAX	1.8 V ≤ DVDD ≤ 2 V MIN	TYP	MAX	UNIT
t_{CLK}	Master clock period	444		666	444		666	ns
t_{CSSC}	$\overline{CS}$ low to first SCLK, setup time	6			17			ns
t_{SCLK}	SCLK period	50			66.6			ns
$t_{SPWH, L}$	SCLK pulse width, high and low	15			25			ns
t_{DIST}	DIN valid to SCLK falling edge: setup time	10			10			ns
t_{DIHD}	Valid DIN after SCLK falling edge: hold time	10			11			ns
t_{DOHD}	SCLK falling edge to invalid DOUT: hold time	10			10			ns
t_{DOPD}	SCLK rising edge to DOUT valid: setup time			17			32	ns
t_{CSH}	$\overline{CS}$ high pulse	2			2			t_{CLK}s
t_{CSDOD}	$\overline{CS}$ low to DOUT driven	10			20			ns
t_{SCCS}	Eighth SCLK falling edge to $\overline{CS}$ high	4			4			t_{CLK}s
$t_{SDECODE}$	Command decode time	4			4			t_{CLK}s
t_{CSDOZ}	$\overline{CS}$ high to DOUT Hi-Z			10			20	ns
$t_{DISCK2ST}$	Valid DAISY_IN to SCLK rising edge: setup time	10			10			ns
$t_{DISCK2HT}$	Valid DAISY_IN after SCLK rising edge: hold time	10			10			ns

(1) Specifications apply from –40°C to +85°C. Load on D_{OUT} = 20 pF || 100 kΩ.

PIN CONFIGURATION

PAG PACKAGE
TQFP-64
(TOP VIEW)



PIN ASSIGNMENTS

NAME	TERMINAL	FUNCTION	DESCRIPTION
AVDD	19, 21, 22, 56	Supply	Analog supply
AVDD	59	Supply	Charge pump analog supply
AVDD1	54	Supply	Analog supply
AVSS	20, 23, 32, 57	Supply	Analog ground
AVSS	58	Supply	Charge pump analog ground
AVSS1	53	Supply	Analog ground
BIASIN	62	Analog input	Bias drive input to MUX
BIASINV	61	Analog input/output	Bias drive inverting input
BIASOUT	63	Analog output	Bias drive output
BIASREF	60	Analog input	Bias drive noninverting input
$\overline{\text{CS}}$	39	Digital input	SPI chip select; active low
CLK	37	Digital input	Master clock input
CLKSEL	52	Digital input	Master clock select
DAISY_IN	41	Digital input	Daisy-chain input
DGND	33, 49, 51	Supply	Digital ground
DIN	34	Digital input	SPI data in
DOUT	43	Digital output	SPI data out
$\overline{\text{DRDY}}$	47	Digital output	Data ready; active low

PIN ASSIGNMENTS (continued)

NAME	TERMINAL	FUNCTION	DESCRIPTION
DVDD	48, 50	Supply	Digital power supply
GPIO1	42	Digital input/output	General-purpose input/output pin
GPIO2	44	Digital input/output	General-purpose input/output pin
GPIO3	45	Digital input/output	GPIO3 in normal mode
GPIO4	46	Digital input/output	GPIO4 in normal mode
IN1N(1)	15	Analog input	Differential analog negative input 1
IN1P	16	Analog input	Differential analog positive input 1
IN2N	13	Analog input	Differential analog negative input 2
IN2P	14	Analog input	Differential analog positive input 2
IN3N	11	Analog input	Differential analog negative input 3
IN3P	12	Analog input	Differential analog positive input 3
IN4N	9	Analog input	Differential analog negative input 4
IN4P	10	Analog input	Differential analog positive input 4
IN5N	7	Analog input	Differential analog negative input 5
IN5P	8	Analog input	Differential analog positive input 5
IN6N	5	Analog input	Differential analog negative input 6
IN6P	6	Analog input	Differential analog positive input 6
IN7N	3	Analog input	Differential analog negative input 7
IN7P	4	Analog input	Differential analog positive input 7
IN8N	1	Analog input	Differential analog negative input 8
IN8P	2	Analog input	Differential analog positive input 8
NC	27, 29	—	No connection
Reserved	64	Analog output	Leave as open circuit
$\overline{\text{RESET}}$	36	Digital input	System reset; active low
RESV1	31	Digital input	Reserved for future use. Must tie to logic low (DGND)
SCLK	40	Digital input	SPI clock
SRB1	17	Analog input/output	Patient stimulus, reference, and bias signal 1
SRB2	18	Analog input/output	Patient stimulus, reference, and bias signal 2
START	38	Digital input	Start conversion
$\overline{\text{PWDN}}$	35	Digital input	Power-down; active low
VCAP1	28	—	Analog bypass capacitor
VCAP2	30	—	Analog bypass capacitor
VCAP3	55	Analog	Analog bypass capacitor
VCAP4	26	Analog output	Analog bypass capacitor
VREFN	25	Analog input	Negative reference voltage
VREFP	24	Analog input/output	Positive reference voltage

(1) Connect unused analog inputs IN1x to IN8x to AVDD.

TYPICAL CHARACTERISTICS

All plots are at T_A = +25°C, AVDD = 5 V, AVSS = 0 V, DVDD = 3.3 V, internal VREFP = 4.5 V, VREFN = AVSS, external clock = 2.048 MHz, data rate = 250 SPS, and gain = 12, unless otherwise noted.

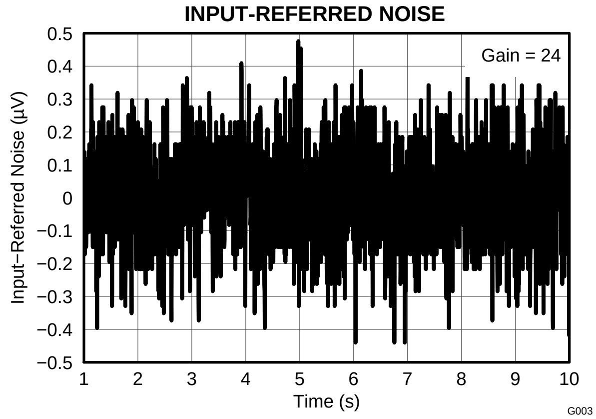


Figure 3.

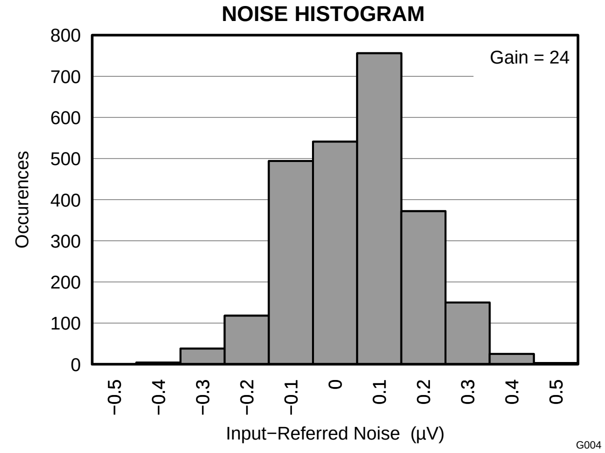


Figure 4.

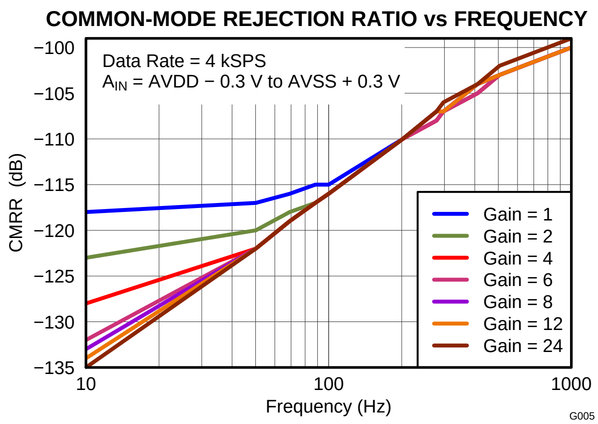


Figure 5.

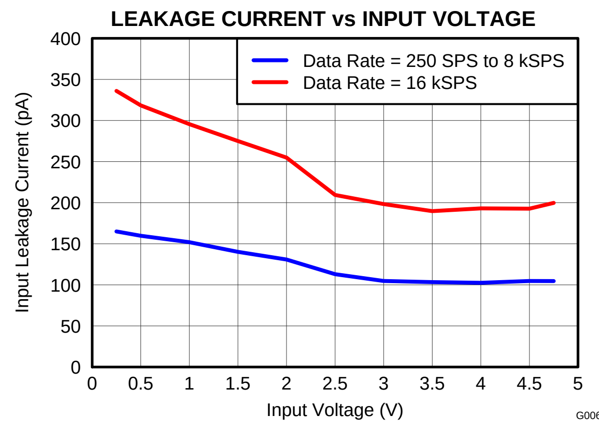


Figure 6.

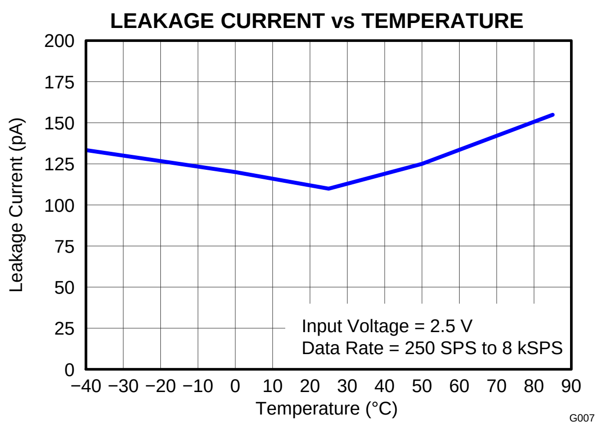


Figure 7.

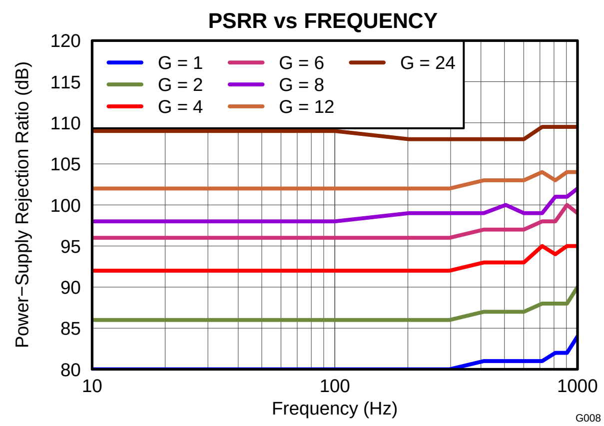


Figure 8.

TYPICAL CHARACTERISTICS (continued)

All plots are at T_A = +25°C, AVDD = 5 V, AVSS = 0 V, DVDD = 3.3 V, internal VREFP = 4.5 V, VREFN = AVSS, external clock = 2.048 MHz, data rate = 250 SPS, and gain = 12, unless otherwise noted.

THD vs FREQUENCY

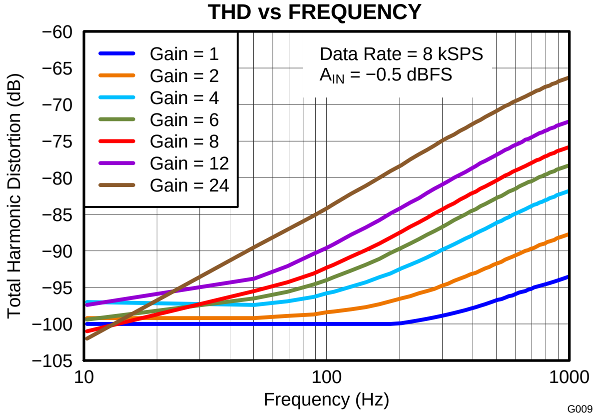


Figure 9.

INL vs PGA GAIN

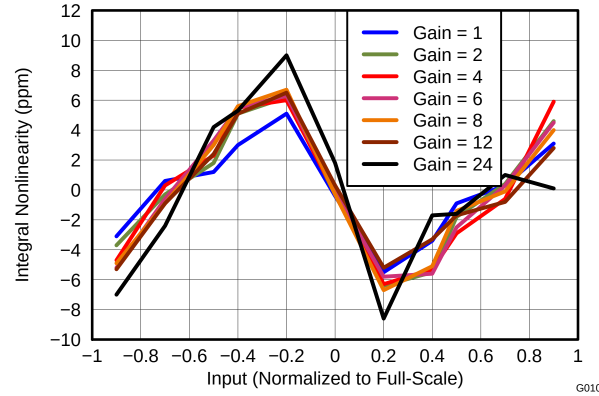


Figure 10.

INL vs TEMPERATURE

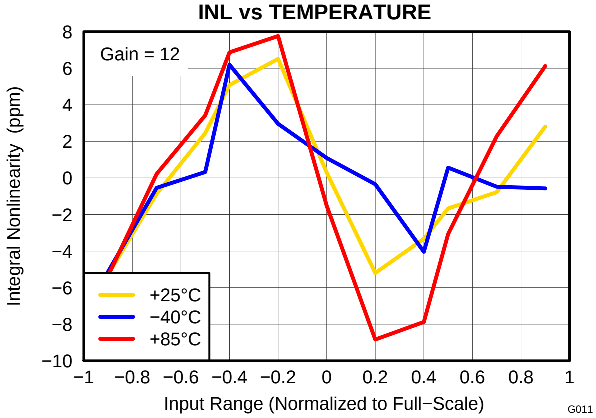


Figure 11.

THD FFT PLOT (60-Hz Signal)

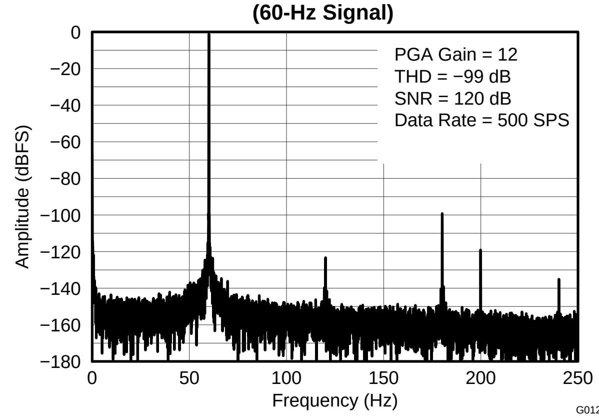


Figure 12.

FFT PLOT (60-Hz Signal)

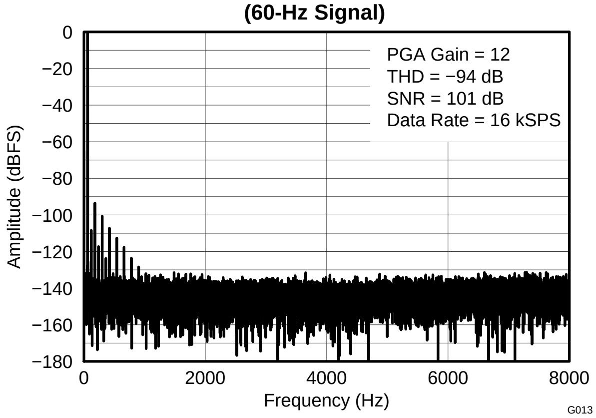


Figure 13.

OFFSET vs PGA GAIN (Absolute Value)

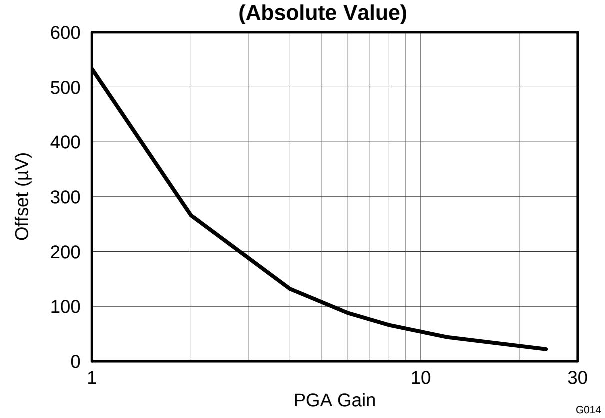


Figure 14.

TYPICAL CHARACTERISTICS (continued)

All plots are at T_A = +25°C, AVDD = 5 V, AVSS = 0 V, DVDD = 3.3 V, internal VREFP = 4.5 V, VREFN = AVSS, external clock = 2.048 MHz, data rate = 250 SPS, and gain = 12, unless otherwise noted.

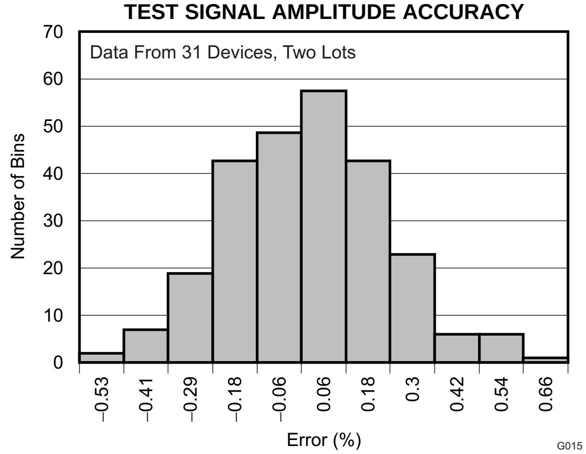


Figure 15.

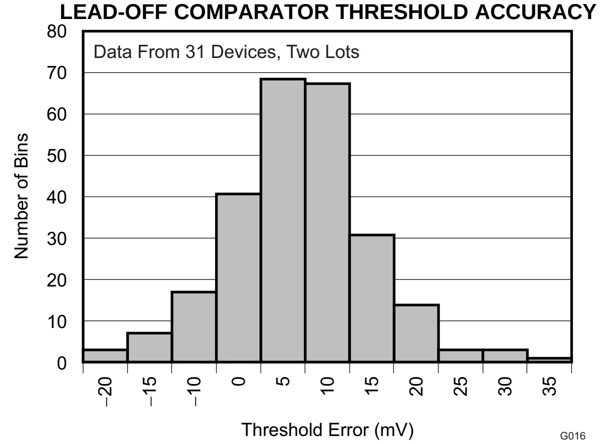


Figure 16.

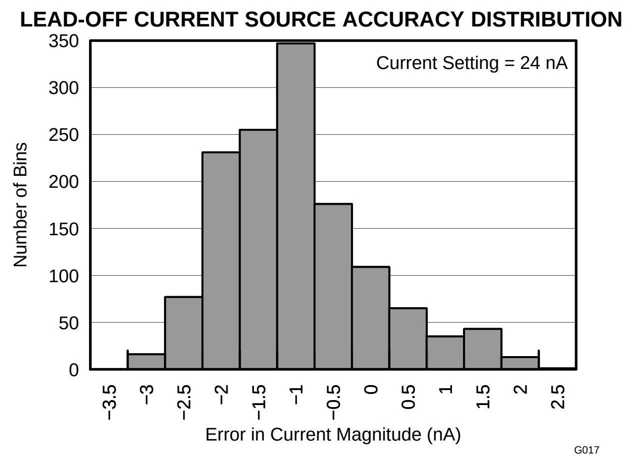


Figure 17.

OVERVIEW

The ADS1299 is a low-noise, low-power, multichannel, simultaneously-sampling, 24-bit, delta-sigma (ΔΣ) analog-to-digital converter (ADC) with an integrated programmable gain amplifier (PGA). This device integrates various EEG-specific functions that makes it well-suited for scalable electroencephalography (EEG) applications. The device can also be used in high-performance, multichannel, data acquisition systems by powering down the EEG-specific circuitry.

The ADS1299 has a highly-programmable multiplexer that allows for temperature, supply, input short, and bias measurements. Additionally, the multiplexer allows any input electrodes to be programmed as the patient reference drive. The PGA gain can be chosen from one of seven settings (1, 2, 4, 6, 8, 12, and 24). The ADCs in the device offer data rates from 250 SPS to 16 kSPS. Communication to the device is accomplished using an SPI-compatible interface. The device provides four general-purpose input/output (GPIO) pins for general use. Multiple devices can be synchronized using the START pin.

The internal reference can be programmed to 4.5 V. The internal oscillator generates a 2.048-MHz clock. The versatile patient bias drive block allows the average of any electrode combination to be chosen in order to generate the patient drive signal. Lead-off detection can be accomplished by using a current source or sink. A one-time, in-band, lead-off option and a continuous, out-of-band, internal lead-off option are available. Refer to Figure 18 for a block diagram.

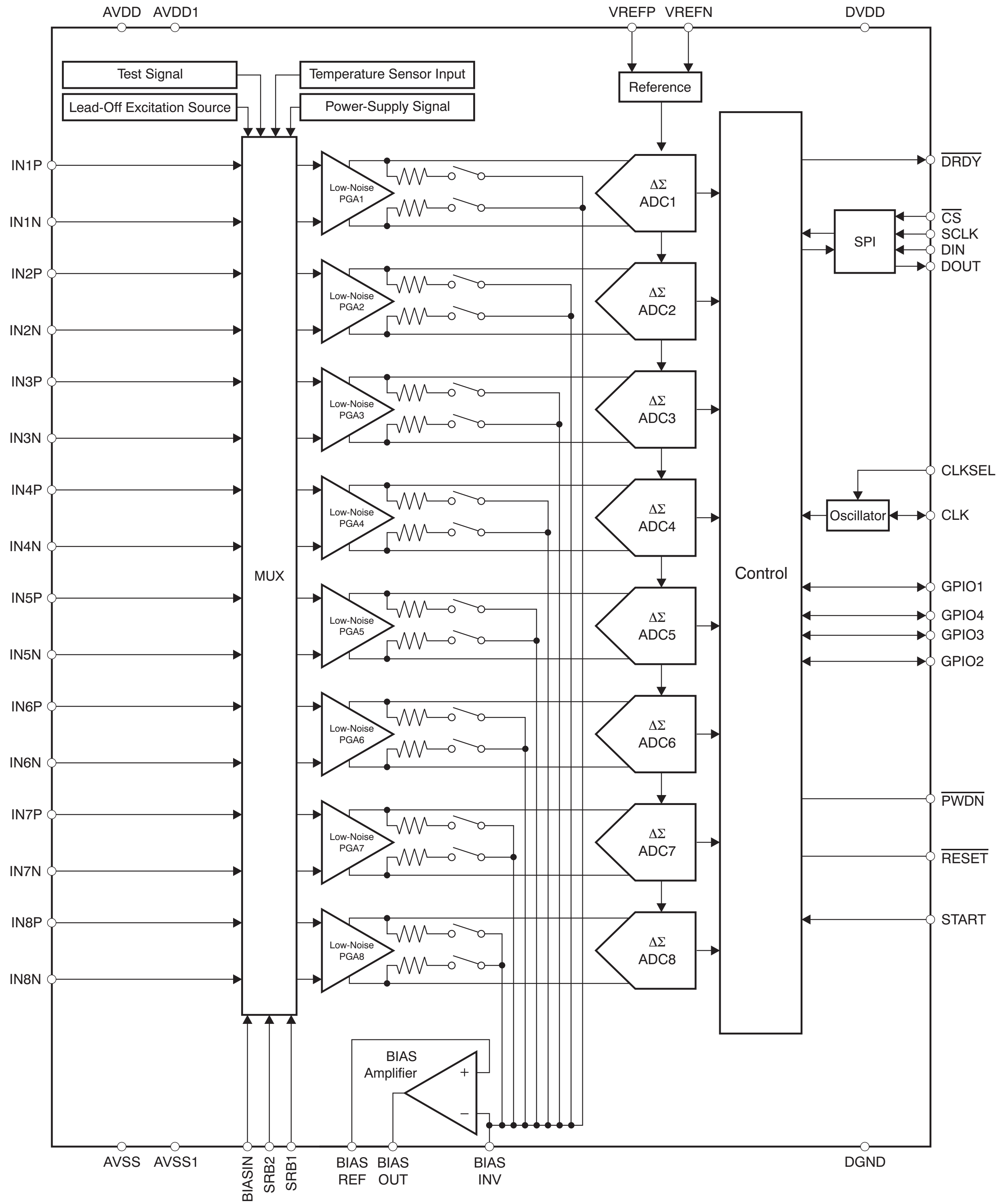


Figure 18. Functional Block Diagram

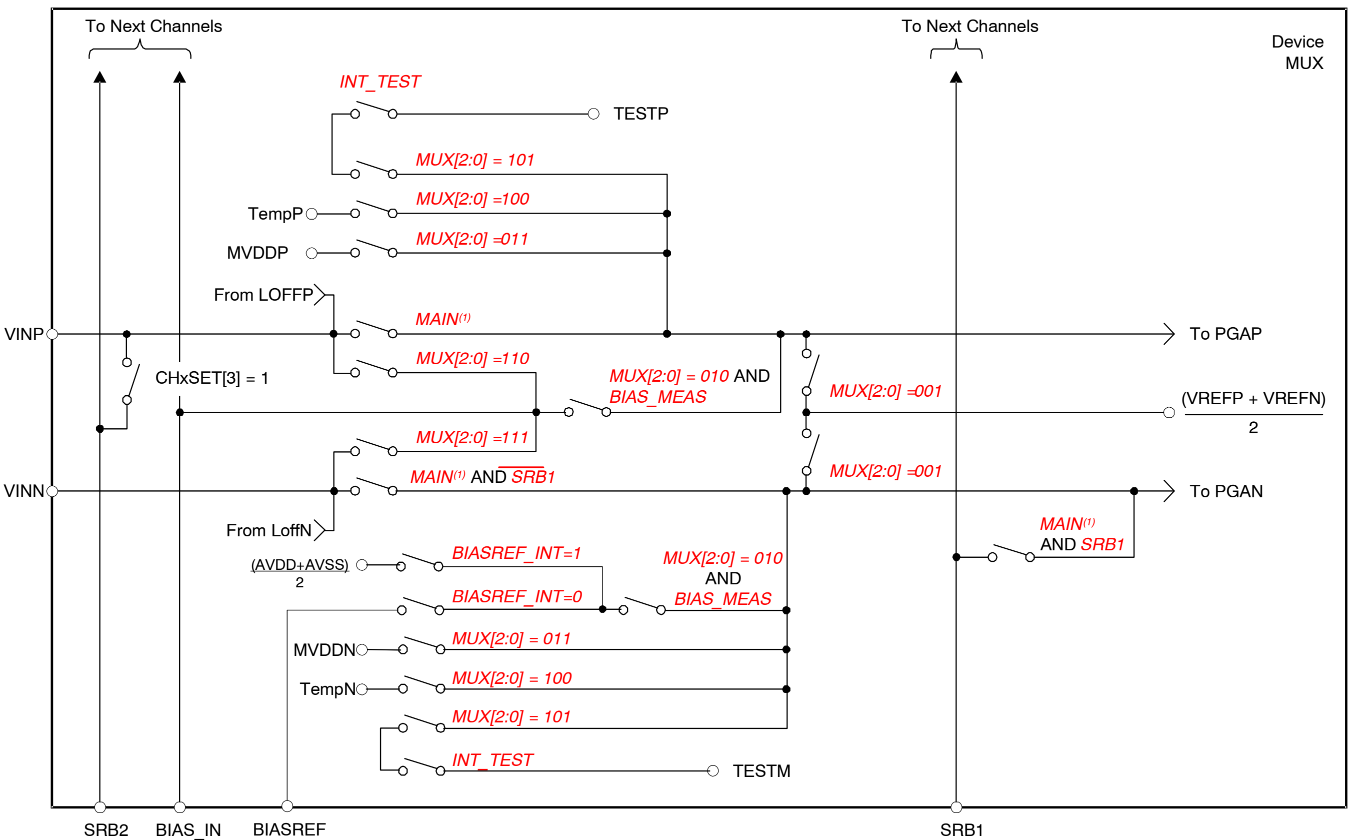
THEORY OF OPERATION

This section contains details of the ADS1299 internal functional elements. The analog blocks are discussed first, followed by the digital interface. Blocks implementing EEG-specific functions are covered at the end of this document.

Throughout this document, f_{CLK} denotes the CLK pin signal frequency, t_{CLK} denotes the CLK pin signal period, f_{DR} denotes the output data rate, t_{DR} denotes the output data time period, and f_{MOD} denotes the frequency at which the modulator samples the input.

INPUT MULTIPLEXER

The ADS1299 input multiplexers are very flexible and provide many configurable signal-switching options. Figure 19 shows the multiplexer on a single channel of the device. Note that the device has eight such blocks, one for each channel. SRB1, SRB2, and BIASIN are common to all eight blocks. VINP and VINN are separate for each of the eight blocks. This flexibility allows for significant device and sub-system diagnostics, calibration, and configuration. Switch setting selections for each channel are made by writing the appropriate values to the CHnSET[3:0] register (see the *CHnSET: Individual Channel Settings* section for details) by writing the BIAS_MEAS bit in the CONFIG3 register and the SRB1 bit in the MISC1 register (see the *CONFIG3: Configuration Register 3* subsection of the *Register Map* section for details). Refer to the *Input Multiplexer* subsection of the *EEG-Specifc Functions* section for further information regarding the EEG-specific features of the multiplexer.



(1) MAIN is equal to either MUX[2:0] = 000, MUX[2:0] = 110, or MUX[2:0] = 111.

Figure 19. Input Multiplexer Block for One Channel

Device Noise Measurements

Setting CHnSET[2:0] = 001 sets the common-mode voltage of [(VREFP + VREFN) / 2] to both channel inputs. This setting can be used to test inherent device noise in the user system.

Test Signals (TestP and TestN)

Setting CHnSET[2:0] = 101 provides internally-generated test signals for use in sub-system verification at power-up. This functionality allows the device internal signal chain to be tested out.

Test signals are controlled through register settings (see the *CONFIG2: Configuration Register 2* subsection in the *Register Map* section for details). TEST_AMP controls the signal amplitude and TEST_FREQ controls switching at the required frequency.

Temperature Sensor (TempP, TempN)

The ADS1299 contains an on-chip temperature sensor. This sensor uses two internal diodes with one diode having a current density 16x that of the other, as shown in Figure 20. The difference in diode current densities yields a voltage difference proportional to absolute temperature.

As a result of the low thermal resistance of the package to the printed circuit board (PCB), the internal device temperature tracks PCB temperature closely. Note that self-heating of the ADS1299 causes a higher reading than the temperature of the surrounding PCB.

The scale factor of Equation 1 converts the temperature reading to degrees Celsius. Before using this equation, the temperature reading code must first be scaled to microvolts.

$$\text{Temperature } (°\text{C}) = \left[\frac{\text{Temperature Reading } (\mu\text{V}) - 145{,}300\ \mu\text{V}}{490\ \mu\text{V}/°\text{C}}\right] + 25°\text{C} \tag{1}$$

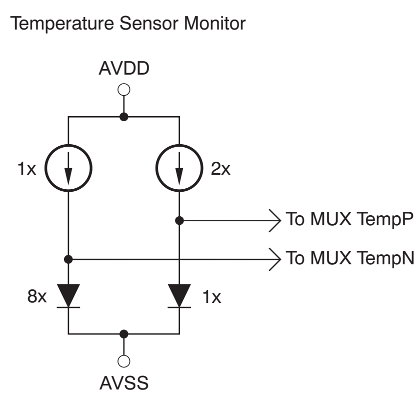


Figure 20. Temperature Sensor Measurement in the Input

Supply Measurements (MVDDP, MVDDN)

Setting CHnSET[2:0] = 011 sets the channel inputs to different supply voltages of the device. For channels 1, 2, 5, 6, 7, and 8, (MVDDP – MVDDN) is [0.5 × (AVDD + AVSS)]; for channels 3 and 4, (MVDDP – MVDDN) is DVDD / 4. Note that to avoid saturating the PGA while measuring power supplies, the gain must be set to '1'.

Lead-Off Excitation Signals (LoffP, LoffN)

The lead-off excitation signals are fed into the multiplexer before the switches. The comparators that detect the lead-off condition are also connected to the multiplexer block before the switches. For a detailed description of the lead-off block, refer to the *Lead-Off Detection* subsection in the *EEG-Specific Functions* section.

Auxiliary Single-Ended Input

The BIASIN pin is primarily used for routing the bias signal to any electrodes in case the bias electrode falls off. However, the BIASIN pin can be used as a multiple single-ended input channel. The signal at the BIASIN pin can be measured with respect to the voltage at the BIASREF pin using any of the eight channels. This measurement is done by setting the channel multiplexer setting to '010' and the BIAS_MEAS bit of the CONFIG3 register to '1'.

ANALOG INPUT

The ADS1299 analog input is fully differential. Assuming PGA = 1, the input (INP – INN) can span between $–V_{REF}$ to $+V_{REF}$. Refer to Table 7 for an explanation of the correlation between the analog input and digital codes. There are two general methods of driving the ADS1299 analog input: single-ended or differential (as shown in Figure 21 and Figure 22, respectively). Note that INP and INN are 180°C out-of-phase in the differential input method. When the input is single-ended, the INN input is held at the common-mode voltage, preferably at mid-supply. The INP input swings around the same common voltage and the peak-to-peak amplitude is (common-mode + 1/2 V_{REF}) and (common-mode – 1/2 V_{REF}). When the input is differential, the common-mode is given by [(INP + INN) / 2]. Both INP and INN inputs swing from (common-mode + 1/2 V_{REF}) to (common-mode – 1/2 V_{REF}). For optimal performance, the ADS1299 is recommended to be used in a differential configuration.

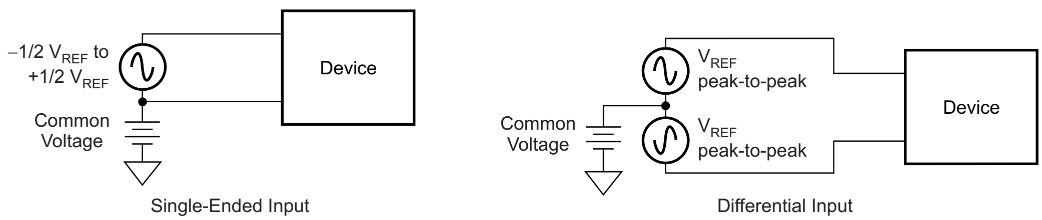
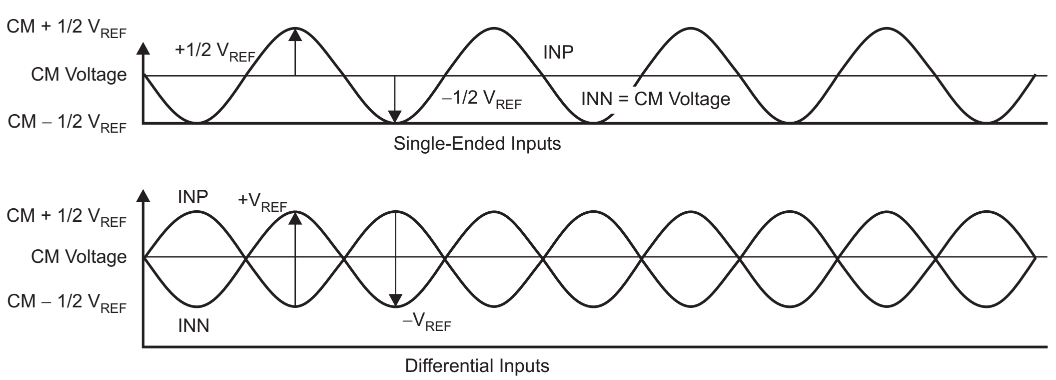


Figure 21. Methods of Driving the ADS1299: Single-Ended or Differential



Common-Mode Voltage (Differential Mode) = $\frac{(INP) + (INN)}{2}$, Common-Mode Voltage (Single-Ended Mode) = INN.

Input Range (Differential Mode) = (AINP – AINN) = V_{REF} – ($–V_{REF}$) = 2 V_{REF}.

Figure 22. Using the ADS1299 in Single-Ended and Differential Input Modes

PGA SETTINGS AND INPUT RANGE

The low-noise PGA is a differential input and output amplifier, as shown in Figure 23. The PGA has seven gain settings (1, 2, 4, 6, 8, 12, and 24) that can be set by writing to the CHnSET register (see the *CHnSET: Individual Channel Settings* subsection of the *Register Map* section for details). The ADS1299 has CMOS inputs and therefore has negligible current noise. Table 5 shows the typical bandwidth values for various gain settings. Note that Table 5 shows small-signal bandwidth. For large signals, performance is limited by PGA slew rate.

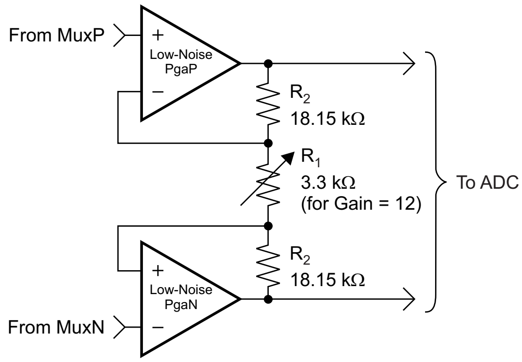


Figure 23. PGA Implementation

Table 5. PGA Gain versus Bandwidth

GAIN	NOMINAL BANDWIDTH AT ROOM TEMPERATURE (kHz)
1	662
2	332
4	165
6	110
8	83
12	55
24	27

The PGA resistor string that implements the gain has 39.6 kΩ of resistance for a gain of 12. This resistance provides a current path across the PGA outputs in the presence of a differential input signal. This current is in addition to the quiescent current specified for the device in the presence of a differential signal at the input.

Input Common-Mode Range

The usable input common-mode range of the front-end depends on various parameters, including the maximum differential input signal, supply voltage, PGA gain, and so forth. This range is described in Equation 2:

$$AVDD - 0.2 - \left(\frac{\text{Gain } V_{MAX\_DIFF}}{2}\right) > CM > AVSS + 0.2 + \left(\frac{\text{Gain } V_{MAX\_DIFF}}{2}\right)$$

where:

V_{MAX_DIFF} = maximum differential signal at the PGA input

CM = common-mode range (2)

For example:

If V_{DD} = 5 V, gain = 12, and V_{MAX_DIFF} = 350 mV
Then 2.3 V < CM < 2.7 V

Input Differential Dynamic Range

The differential (INP – INN) signal range depends on the analog supply and reference used in the system. This range is shown in Equation 3.

$$\text{Max (INP} - \text{INN)} < \frac{V_{REF}}{\text{Gain}} \quad ; \qquad \text{Full-Scale Range} = \frac{\pm V_{REF}}{\text{Gain}} = \frac{2\ V_{REF}}{\text{Gain}} \tag{3}$$

The 5-V supply, with a reference of 4.5 V and a gain of 12 for EEGs, is optimized for power with a differential input signal of approximately 300 mV.

ADC ΔΣ Modulator

Each ADS1299 channel has a 24-bit, ΔΣ ADC. This converter uses a second-order modulator optimized for low-noise applications. The modulator samples the input signal at the rate of ($f_{MOD} = f_{CLK}$ / 2). As in the case of any ΔΣ modulator, the ADS1299 noise is shaped until f_{MOD} / 2, as shown in Figure 24. The on-chip digital decimation filters explained in the next section can be used to filter out the noise at higher frequencies. These on-chip decimation filters also provide antialias filtering. This ΔΣ converter feature drastically reduces the complexity of the analog antialiasing filters typically required with nyquist ADCs.

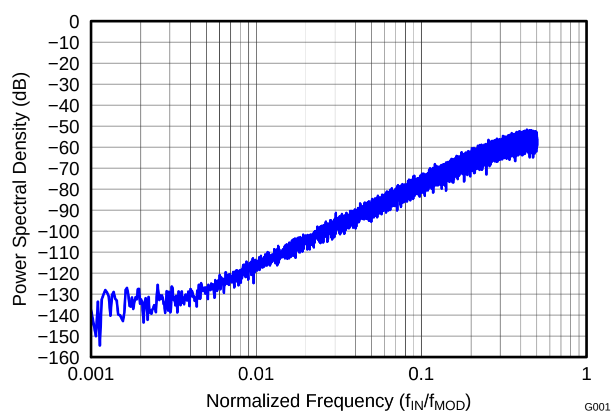


Figure 24. Modulator Noise Spectrum Up To 0.5 × f_{MOD}

DIGITAL DECIMATION FILTER

The digital filter receives the modulator output and decimates the data stream. By adjusting the amount of filtering, tradeoffs can be made between resolution and data rate: filter more for higher resolution, filter less for higher data rates. Higher data rates are typically used in EEG applications for ac lead-off detection.

The digital filter on each channel consists of a third-order sinc filter. The sinc filter decimation ratio can be adjusted by the DR bits in the CONFIG1 register (see the *Register Map* section for details). This setting is a global setting that affects all channels and, therefore, all channels operate at the same data rate in a device.

Sinc Filter Stage (sinx / x)

The sinc filter is a variable decimation rate, third-order, low-pass filter. Data are supplied to this section of the filter from the modulator at the rate of f_{MOD}. The sinc filter attenuates the modulator high-frequency noise, then decimates the data stream into parallel data. The decimation rate affects the overall converter data rate.

Equation 4 shows the scaled Z-domain transfer function of the sinc filter.

$$\left|H(z)\right| = \left|\frac{1 - Z^{-N}}{1 - Z^{-1}}\right|^3 \quad (4)$$

The frequency domain transfer function of the sinc filter is shown in Equation 5.

$$H(f)\left| = \right|\frac{\sin\left(\frac{N\pi f}{f_{MOD}}\right)}{N \times \sin\left(\frac{\pi f}{f_{MOD}}\right)}\right|^3$$

where:

N = decimation ratio (5)

The sinc filter has notches (or zeroes) that occur at the output data rate and multiples thereof. At these frequencies, the filter has infinite attenuation. Figure 25 shows the sinc filter frequency response and Figure 26 shows the sinc filter roll-off. With a step change at input, the filter takes 3 × t_{DR} to settle. After a rising edge of the START signal, the filter takes t_{SETTLE} time to give the first data output. The settling time of the filters at various data rates are discussed in the *START* subsection of the *SPI Interface* section. Figure 27 and Figure 28 show the filter transfer function until f_{MOD} / 2 and f_{MOD} / 16, respectively, at different data rates. Figure 29 shows the transfer function extended until 4 × f_{MOD}. The ADS1299 pass band repeats itself at every f_{MOD}. The input R-C antialiasing filters in the system should be chosen such that any interference in frequencies around multiples of f_{MOD} are attenuated sufficiently.

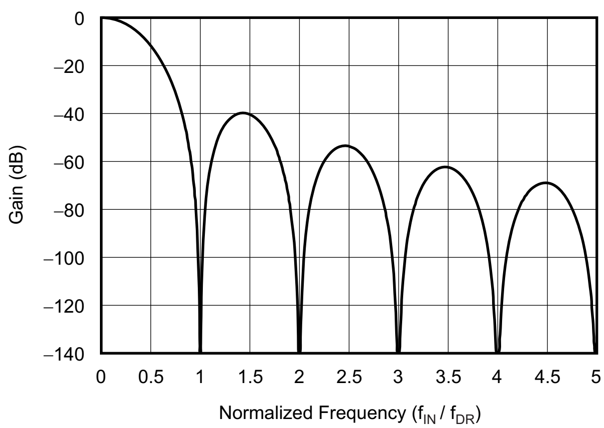


Figure 25. Sinc Filter Frequency Response

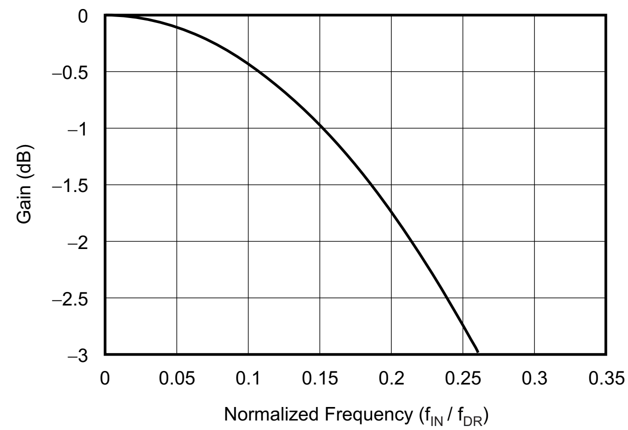


Figure 26. Sinc Filter Roll-Off

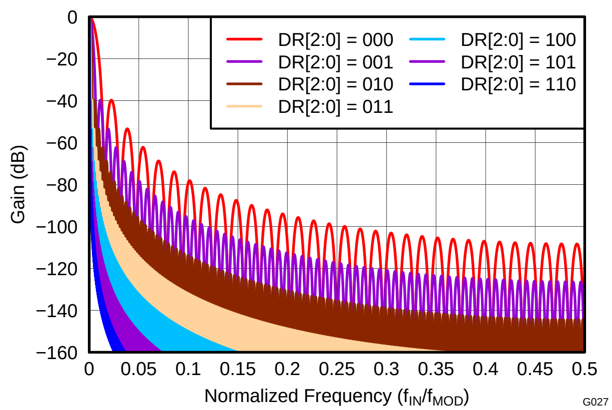


Figure 27. Transfer Function of On-Chip Decimation Filters Until f_{MOD} / 2

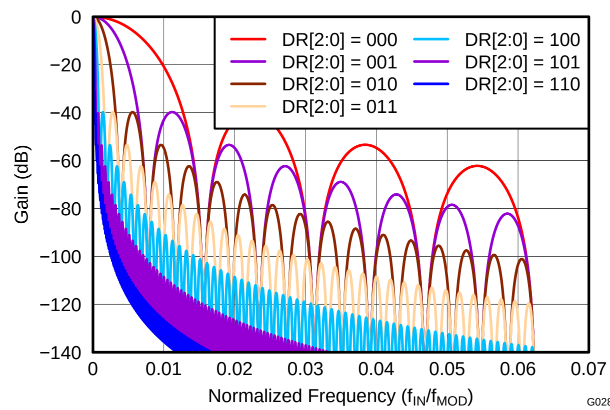


Figure 28. Transfer Function of On-Chip Decimation Filters Until f_{MOD} / 16

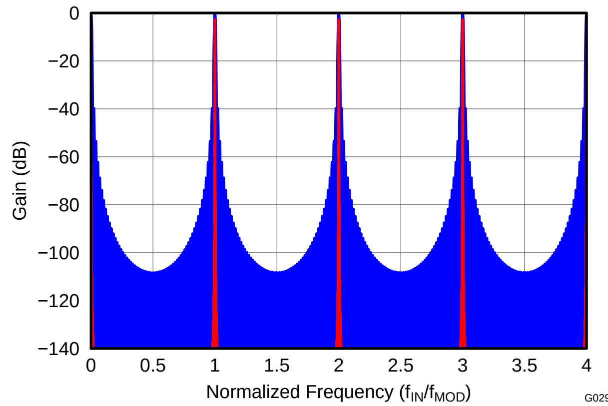
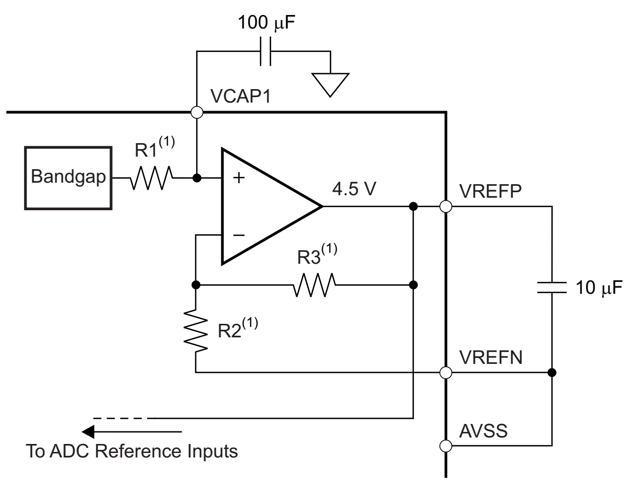


Figure 29. Transfer Function of On-Chip Decimation Filters Until 4 f_{MOD} for DR[2:0] = 000 and DR[2:0] = 110

REFERENCE

Figure 30 shows a simplified block diagram of the ADS1299 internal reference. The 4.5-V reference voltage is generated with respect to AVSS. When using the internal voltage reference, connect VREFN to AVSS.



(1) For V_{REF} = 4.5 V: R1 = 9.8 kΩ, R2 = 13.4 kΩ, and R3 = 36.85 kΩ.

Figure 30. Internal Reference

The external band-limiting capacitors determine the amount of reference noise contribution. For high-end EEG systems, the capacitor values should be chosen such that the bandwidth is limited to less than 10 Hz so that the reference noise does not dominate system noise.

Alternatively, the internal reference buffer can be powered down and VREFP can be applied externally. Figure 31 shows a typical external reference drive circuitry. Power-down is controlled by the PD_REFBUF bit in the CONFIG3 register. This power-down is also used to share internal references when two devices are cascaded. By default, the device wakes up in external reference mode.

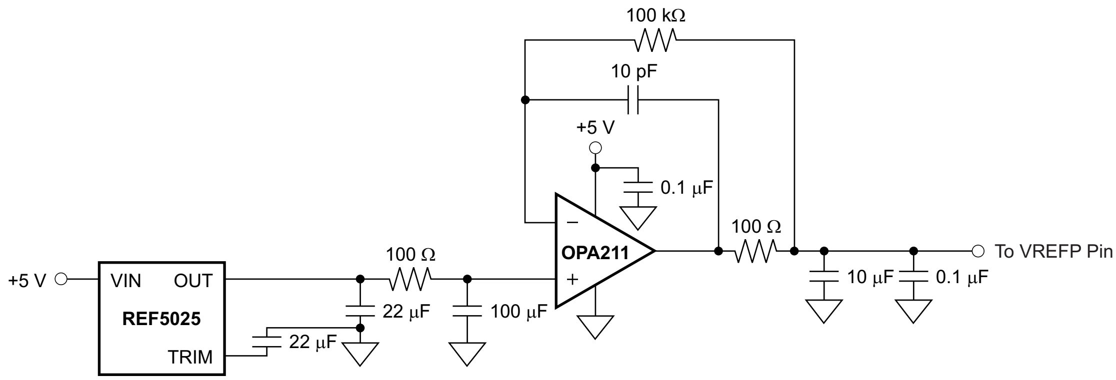


Figure 31. External Reference Driver

CLOCK

The ADS1299 provides two methods for device clocking: internal and external. Internal clocking is ideally suited for low-power, battery-powered systems. The internal oscillator is trimmed for accuracy at room temperature. Accuracy varies over the specified temperature range; see the Electrical Characteristics. Clock selection is controlled by the CLKSEL pin and the CLK_EN register bit.

The CLKSEL pin selects either the internal or external clock. The CLK_EN bit in the CONFIG1 register enables and disables the oscillator clock to be output in the CLK pin. A truth table for these two pins is shown in Table 6. The CLK_EN bit is useful when multiple devices are used in a daisy-chain configuration. During power-down, the external clock is recommended be shut down to save power.

Table 6. CLKSEL Pin and CLK_EN Bit

CLKSEL PIN	CONFIG1.CLK_EN BIT	CLOCK SOURCE	CLK PIN STATUS
0	X	External clock	Input: external clock
1	0	Internal clock oscillator	3-state
1	1	Internal clock oscillator	Output: internal clock oscillator

DATA FORMAT

The ADS1299 outputs 24 bits of data per channel in binary twos complement format, MSB first. The LSB has a weight of $[V_{REF} / (2^{23} – 1)]$. A positive full-scale input produces an output code of 7FFFFFh and the negative full-scale input produces an output code of 800000h. The output clips at these codes for signals exceeding full-scale. Table 7 summarizes the ideal output codes for different input signals. All 24 bits toggle when the analog input is at positive or negative full-scale.

Table 7. Ideal Output Code versus Input Signal(1)

INPUT SIGNAL, V_{IN} (AINP – AINN)	IDEAL OUTPUT CODE(2)
$\geq V_{REF}$	7FFFFFh
$+V_{REF} / (2^{23} – 1)$	000001h
0	000000h
$–V_{REF} / (2^{23} – 1)$	FFFFFFh
$\leq –V_{REF} (2^{23} / 2^{23} – 1)$	800000h

(1) Only valid for 24-bit resolution data rates.
(2) Excludes effects of noise, linearity, offset, and gain error.

SPI INTERFACE

The SPI-compatible serial interface consists of four signals: $\overline{CS}$, SCLK, DIN, and DOUT. The interface reads conversion data, reads and writes registers, and controls ADS1299 operation. The $\overline{DRDY}$ output is used as a status signal to indicate when data are ready. $\overline{DRDY}$ goes low when new data are available.

Chip Select ($\overline{CS}$)

Chip select ($\overline{CS}$) selects the ADS1299 for SPI communication. $\overline{CS}$ must remain low for the entire serial communication duration. After the serial communication is finished, always wait four or more t_{CLK} cycles before taking $\overline{CS}$ high. When $\overline{CS}$ is taken high, the serial interface is reset, SCLK and DIN are ignored, and DOUT enters a high-impedance state. $\overline{DRDY}$ asserts when data conversion is complete, regardless of whether $\overline{CS}$ is high or low.

Serial Clock (SCLK)

SCLK is the serial peripheral interface (SPI) serial clock. SCLK shifts in commands and shifts out data from the device. SCLK features a Schmitt-triggered input and clocks data on the DIN and DOUT pins into and out of the ADS1299. Even though the input has hysteresis, it is recommended to keep SCLK as clean as possible to prevent glitches from accidentally forcing a clock event. The absolute maximum SCLK limit is specified in the *Serial Interface Timing* table. When shifting in commands with SCLK, make sure that the entire set of SCLKs is issued to the device. Failure to do so can result in the device serial interface being placed into an unknown state, thus requiring $\overline{CS}$ to be taken high to recover.

For a single device, the minimum speed required for SCLK depends on the number of channels, number of bits of resolution, and output data rate. (For multiple cascaded devices, see the *Standard Mode* subsection of the *Multiple Device Configuration* section.)

For example, if the ADS1299 is used in a 500-SPS mode (8 channels, 24-bit resolution), the minimum SCLK speed is 110 kHz.

Data retrieval can be accomplished either by placing the device in RDATAC mode or by issuing an RDATA command for data on demand. The SCLK rate limitation in Equation 6 applies to RDATAC. For the RDATA command, the limitation applies if data must be read in between two consecutive $\overline{DRDY}$ signals. Equation 6 assumes that there are no other commands issued in between data captures.

$$t_{SCLK} < \frac{t_{DR} - 4\ t_{CLK}}{N_{BITS} \times N_{CHANNELS} + 24} \quad (6)$$

Data Input (DIN)

The data input pin (DIN) is used along with SCLK to communicate with the ADS1299 (opcode commands and register data). The device latches data on DIN on the SCLK falling edge.

Data Output (DOUT)

The data output pin (DOUT) is used with SCLK to read conversion and register data from the ADS1299. Data on DOUT are shifted out on the SCLK rising edge. DOUT goes to a high-impedance state when $\overline{CS}$ is high. In read data continuous mode (see the *SPI Command Definitions* section for more details), the DOUT output line also indicates when new data are available. This feature can be used to minimize the number of connections between the device and system controller.

Figure 32 shows the ADS1299 data output protocol.

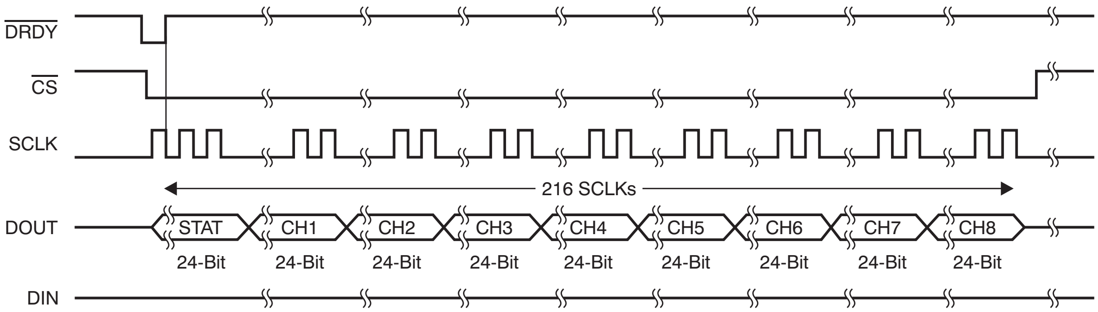


Figure 32. SPI Bus Data Output

Data Retrieval

Data retrieval can be accomplished in one of two methods. The read data continuous command (see the *RDATAC: Read Data Continuous* section) can be used to set the device in a mode to read data continuously without sending opcodes. The read data command (see the *RDATA: Read Data* section) can be used to read just one data output from the device (see the *SPI Command Definitions* section for more details). Conversion data are read by shifting data out on DOUT. The MSB of the data on DOUT is clocked out on the first SCLK rising edge. $\overline{DRDY}$ returns to high on the first SCLK falling edge. DIN should remain low for the entire read operation.

The number of bits in the data output depends on the number of channels and the number of bits per channel. For the ADS1299, the number of data outputs is [(24 status bits + 24 bits × 8 channels) = 216 bits]. The format of the 24 status bits is: (1100 + LOFF_STATP + LOFF_STATN + bits[4:7] of the GPIO register). The data format for each channel data are twos complement and MSB first. When channels are powered down using the user register setting, the corresponding channel output is set to '0'. However, the channel output sequence remains the same.

The ADS1299 also provides a multiple readback feature. Data can be read out multiple times by simply giving more SCLKs, in which case the MSB data byte repeats after reading the last byte. The DAISY_EN bit in the CONFIG1 register must be set to '1' for multiple readbacks.

Data Ready ($\overline{DRDY}$)

$\overline{DRDY}$ is an output. When $\overline{DRDY}$ transitions low, new conversion data are ready. The $\overline{CS}$ signal has no effect on the data ready signal. $\overline{DRDY}$ behavior is determined by whether the device is in RDATAC mode or the RDATA command is used to read data on demand. (See the *RDATAC: Read Data Continuous* and *RDATA: Read Data* subsections of the *SPI Command Definitions* section for further details).

When reading data with the RDATA command, the read operation can overlap the next $\overline{DRDY}$ occurrence without data corruption.

The START pin or the START command places the device either in normal data capture mode or pulse data capture mode.

Figure 33 shows the relationship between $\overline{\text{DRDY}}$, DOUT, and SCLK during data retrieval (in case of an ADS1299 with a selected data rate that gives 24-bit resolution). DOUT is latched out at the SCLK rising edge. $\overline{\text{DRDY}}$ is pulled high at the SCLK falling edge. Note that $\overline{\text{DRDY}}$ goes high on the first SCLK falling edge, regardless of whether data are being retrieved from the device or a command is being sent through the DIN pin.

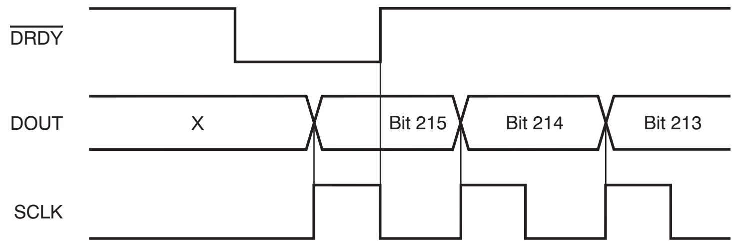


Figure 33. $\overline{\text{DRDY}}$ with Data Retrieval ($\overline{\text{CS}}$ = 0)

GPIO

The ADS1299 has a total of four general-purpose digital I/O (GPIO) pins available in normal mode of operation. The digital I/O pins are individually configurable as either inputs or outputs through the GPIOC bits register. The GPIOD bits in the GPIO register control the pin level. When reading the GPIOD bits, the data returned are the logic level of the pins, whether they are programmed as inputs or outputs. When the GPIO pin is configured as an input, a write to the corresponding GPIOD bit has no effect. When configured as an output, a write to the GPIOD bit sets the output value.

If configured as inputs, these pins must be driven (do not float). The GPIO pins are set as inputs after power-on or after a reset. Figure 34 shows the GPIO port structure. The pins should be shorted to DGND if not used.

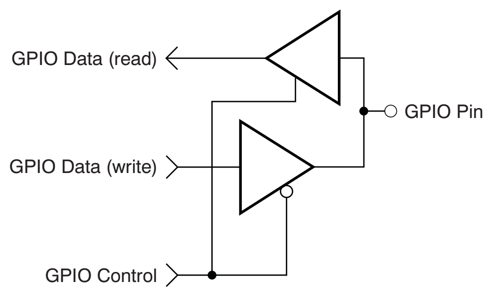


Figure 34. GPIO Port Pin

Power-Down ($\overline{\text{PWDN}}$)

When $\overline{\text{PWDN}}$ is pulled low, all on-chip circuitry is powered down. To exit power-down mode, take the $\overline{\text{PWDN}}$ pin high. Upon exiting from power-down mode, the internal oscillator and the reference require time to wake up. During power-down, the external clock is recommended to be shut down to save power.

Reset ($\overline{\text{RESET}}$)

There are two methods to reset the ADS1299: pull the $\overline{\text{RESET}}$ pin low, or send the RESET opcode command. When using the $\overline{\text{RESET}}$ pin, take the pin low to force a reset. Make sure to follow the minimum pulse width timing specifications before taking the $\overline{\text{RESET}}$ pin back high. The RESET command takes effect on the eighth SCLK falling edge of the opcode command. On reset, 18 t_{CLK} cycles are required to complete initialization of the configuration registers to default states and start the conversion cycle. Note that an internal RESET is automatically issued to the digital filter whenever the CONFIG1 register is set to a new value with a WREG command.

START

The START pin must be set high or the START command sent to begin conversions. When START is low or if the START command has not been sent, the device does not issue a $\overline{\text{DRDY}}$ signal (conversions are halted).

When using the START opcode to control conversions, hold the START pin low. The ADS1299 features two modes to control conversions: continuous mode and single-shot mode. The mode is selected by SINGLE_SHOT (bit 3 of the CONFIG4 register). In multiple device configurations, the START pin is used to synchronize devices (see the *Multiple Device Configuration* subsection of the *SPI Interface* section for more details).

Settling Time

The settling time (t_{SETTLE}) is the time required for the converter to output fully-settled data when the START signal is pulled high. When START is pulled high, $\overline{\text{DRDY}}$ is also pulled high. The next $\overline{\text{DRDY}}$ falling edge indicates that data are ready. Figure 35 shows the timing diagram and Table 8 shows the settling time for different data rates. The settling time depends on f_{CLK} and the decimation ratio (controlled by the DR[2:0] bits in the CONFIG1 register). Table 7 shows the settling time as a function of t_{CLK}. Note that when START is held high and there is a step change in the input signal, 3 × t_{DR} is required for the filter to settle to the new value. Settled data are available on the fourth $\overline{\text{DRDY}}$ pulse.

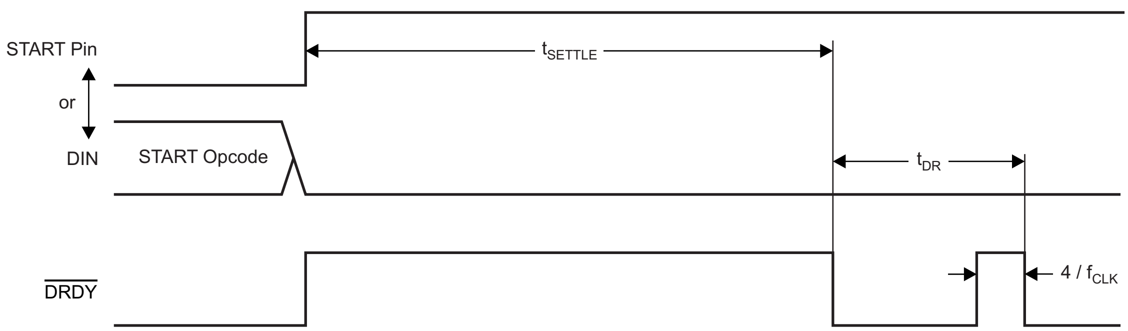


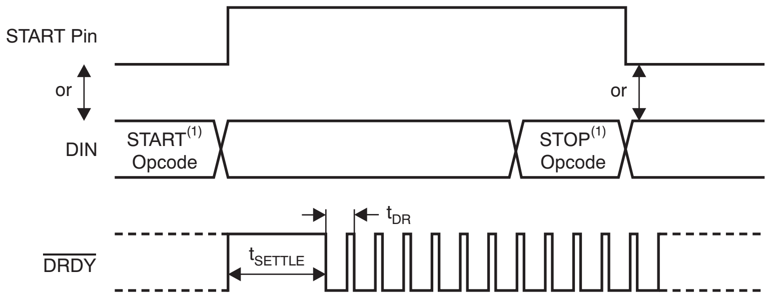
Figure 35. Settling Time

Table 8. Settling Time for Different Data Rates

DR[2:0]	NORMAL MODE	UNIT
000	521	t_{CLK}
001	1033	t_{CLK}
010	2057	t_{CLK}
011	4105	t_{CLK}
100	8201	t_{CLK}
101	16393	t_{CLK}
110	32777	t_{CLK}

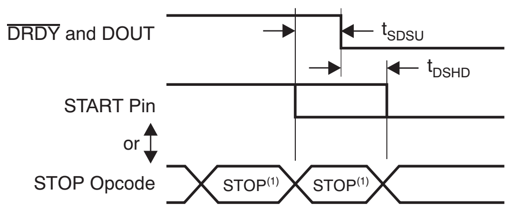
Continuous Mode

Conversions begin when the START pin is taken high or when the START opcode command is sent. As seen in Figure 36, the DRDY output goes high when conversions are started and goes low when data are ready. Conversions continue indefinitely until the START pin is taken low or the STOP opcode command is transmitted. When the START pin is pulled low or the stop command is issued, the conversion in progress is allowed to complete. Figure 37 and Table 9 show the required DRDY timing to the START pin and the START and STOP opcode commands when controlling conversions in this mode. To keep the converter running continuously, the START pin can be permanently tied high. Note that when switching from pulse mode to continuous mode, the START signal is pulsed or a STOP command must be issued followed by a START command. This conversion mode is ideal for applications that require a fixed continuous stream of conversions results.



(1) START and STOP opcode commands take effect on the seventh SCLK falling edge.

Figure 36. Continuous Conversion Mode



(1) START and STOP commands take effect on the seventh SCLK falling edge at the end of the opcode transmission.

Figure 37. START to DRDY Timing

Table 9. Timing Characteristics for Figure 37[(1)]

SYMBOL	DESCRIPTION	MIN	UNIT
t_{SDSU}	START pin low or STOP opcode to DRDY setup time to halt further conversions	16	$1/f_{CLK}$
t_{DSHD}	START pin low or STOP opcode to complete current conversion	16	$1/f_{CLK}$

(1) START and STOP commands take effect on the seventh SCLK falling edge at the end of the opcode transmission.

Single-Shot Mode

Single-shot mode is enabled by setting the SINGLE_SHOT bit in the CONFIG4 register to '1'. In single-shot mode, the ADS1299 performs a single conversion when the START pin is taken high or when the START opcode command is sent. As seen in Figure 38, when a conversion is complete, $\overline{\text{DRDY}}$ goes low and further conversions are stopped. Regardless of whether the conversion data are read or not, $\overline{\text{DRDY}}$ remains low. To begin a new conversion, take the START pin low and then back high, or transmit the START opcode again. Note that when switching from continuous mode to pulse mode, make sure the START signal is pulsed or issue a STOP command followed by a START command.

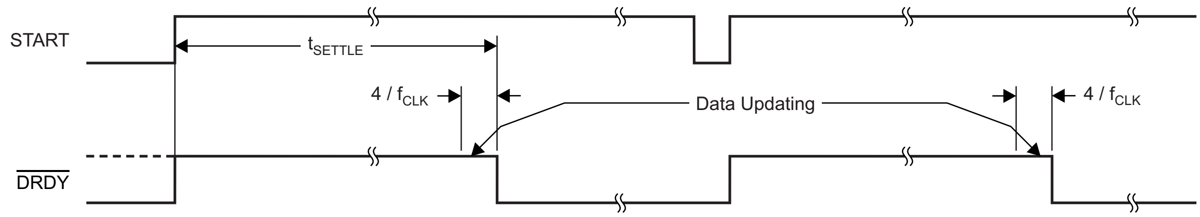


Figure 38. $\overline{\text{DRDY}}$ with No Data Retrieval in Single-Shot Mode

This conversion mode is provided for applications that require non-standard or non-continuous data rates. Issuing a START command or toggling the START pin high resets the digital filter, effectively dropping the data rate by a factor of four. This mode leaves the system more susceptible to aliasing effects, requiring more complex analog or digital filtering. Loading on the host processor increases because the processor must toggle the START pin or send a START command to initiate a new conversion cycle.

MULTIPLE DEVICE CONFIGURATION

The ADS1299 is designed to provide configuration flexibility when multiple devices are used in a system. The serial interface typically needs four signals: DIN, DOUT, SCLK, and $\overline{\text{CS}}$. With one additional chip select signal per device, multiple devices can be connected together. The number of signals needed to interface *n* devices is 3 + *n*.

The bias drive amplifiers can be daisy-chained, as explained in the *Bias Configuration with Multiple Devices* subsection of the *EEG-Specific Functions* section. To use the internal oscillator in a daisy-chain configuration, one device must be set as the master for the clock source with the internal oscillator enabled (CLKSEL pin = 1) and the internal oscillator clock brought out of the device by setting the CLK_EN register bit to '1'. This master device clock is used as the external clock source for other devices.

When using multiple devices, the devices can be synchronized with the START signal. The delay from START to the $\overline{\text{DRDY}}$ signal is fixed for a fixed data rate (see the *START* subsection of the *SPI Interface* section for more details on the settling times). Figure 39 shows the behavior of two devices when synchronized with the START signal.

There are two ways to connect multiple devices with a optimal number of interface pins: cascade mode and daisy-chain mode.

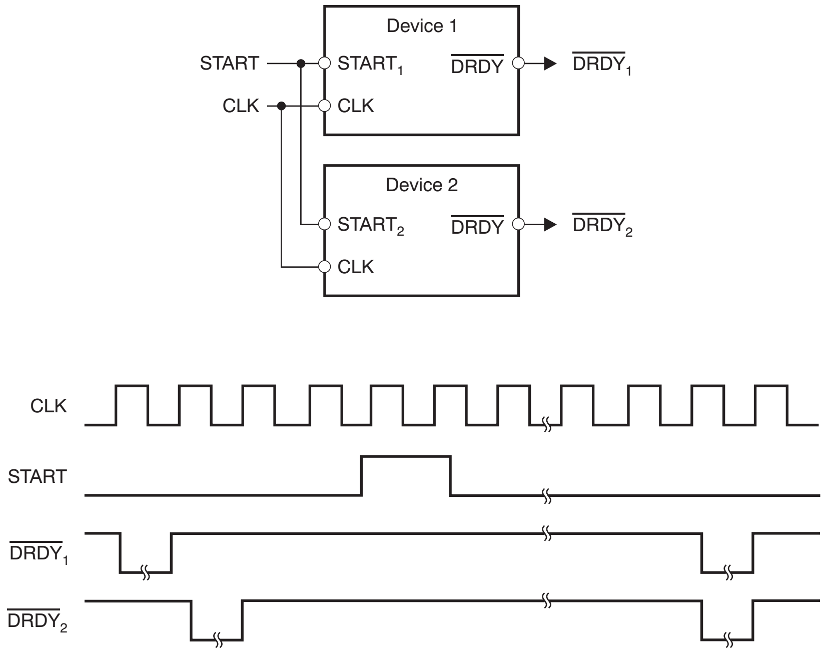


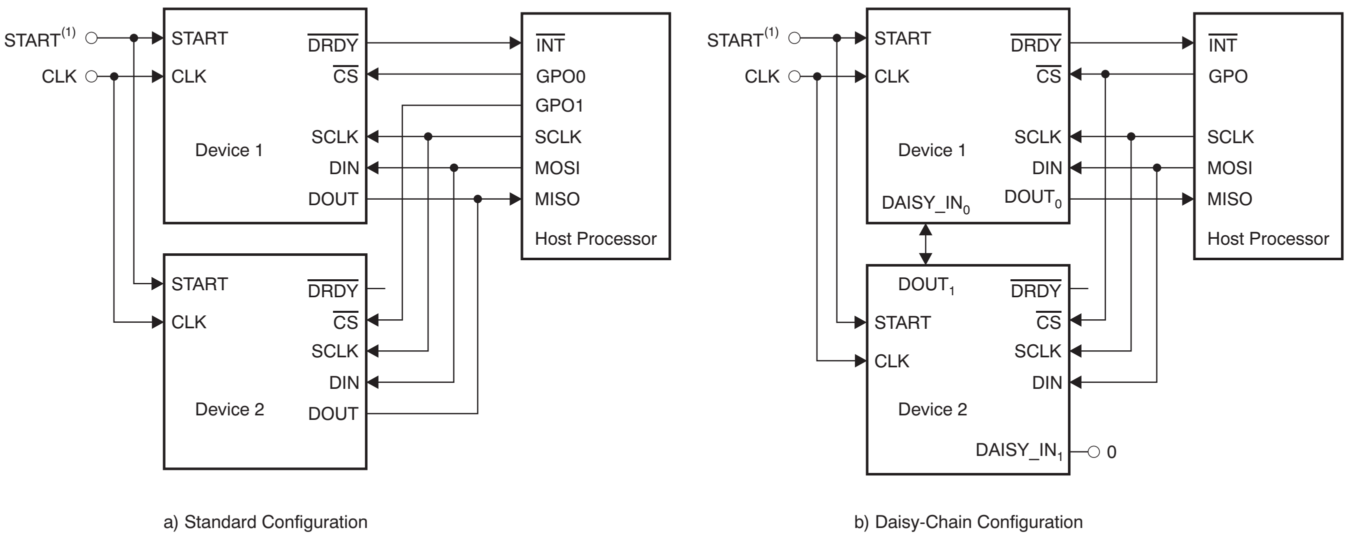
Figure 39. Synchronizing Multiple Converters

Standard Mode

Figure 40a shows a configuration with two devices cascaded together. Together, the devices create a system with 16 channels. DOUT, SCLK, and DIN are shared. Each device has its own chip select. When a device is not selected by the corresponding $\overline{CS}$ being driven to logic 1, the DOUT of this device is high-impedance. This structure allows the other device to take control of the DOUT bus. This configuration method is suitable for the majority of applications.

Daisy-Chain Mode

Daisy-chain mode is enabled by setting the $\overline{DAISY\_EN}$ bit in the CONFIG1 register. Figure 40b shows the daisy-chain configuration. In this mode SCLK, DIN, and $\overline{CS}$ are shared across multiple devices. The DOUT of one device is hooked up to the DAISY_IN of the other device, thereby creating a chain. Also, when using daisy-chain mode, the multiple readback feature is not available. Short the DAISY_IN pin to digital ground if not used. Figure 2 describes the required timing for the device shown in the configurations of Figure 40. Data from the ADS1299 appear first on DOUT, followed by the status and data words.



(1) To reduce pin count, set the START pin low and use the START serial command to synchronize and start conversions.

Figure 40. Multiple Device Configurations

When all devices in the chain operate in the same register setting, DIN can be shared as well. This configuration reduces the SPI communication signals to four, regardless of the number of devices. However, because the individual devices cannot be programmed, the BIAS driver cannot be shared among the multiple devices. Furthermore, an external clock must be used.

Note that from Figure 2, the SCLK rising edge shifts data out of the ADS1299 on DOUT. The SCLK rising edge is also used to latch data into the device DAISY_IN pin down the chain. This architecture allows for a faster SCLK rate speed, but also makes the interface sensitive to board-level signal delays. The more devices in the chain, the more challenging it could become to adhere to setup and hold times. A star-pattern connection of SCLK to all devices, minimizing DOUT length, and other printed circuit board (PCB) layout techniques helps. Placing delay circuits (such as buffers) between DOUT and DAISY_IN are ways to mitigate this challenge. One other option is to insert a *D* flip-flop between DOUT and DAISY_IN clocked on an inverted SCLK. Note also that daisy-chain mode requires some software overhead to recombine data bits spread across byte boundaries. Figure 41 shows a timing diagram for this mode.

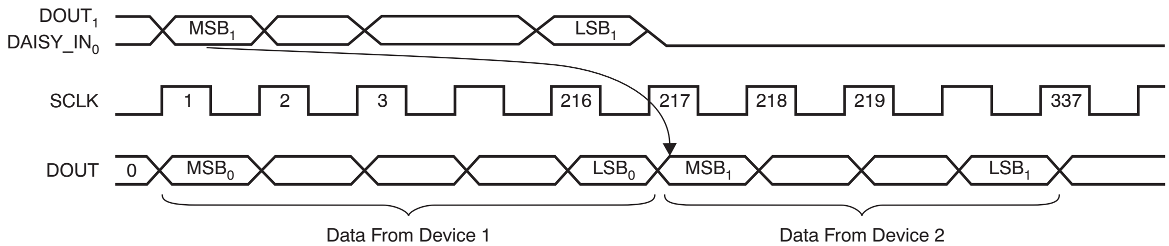


Figure 41. Daisy-Chain Timing

The maximum number of devices that can be daisy-chained depends on the data rate at which the device is operated at. The maximum number of devices can be approximately calculated with Equation 7.

$$N_{DEVICES} = \frac{f_{SCLK}}{f_{DR}\,(N_{BITS})(N_{CHANNELS}) + 24}$$

where:

N_{BITS} = device resolution (depending on data rate), and

$N_{CHANNELS}$ = number of channels in the device. (7)

For example, when the ADS1299 is operated at a 2-kSPS data rate with a 4-MHz f_{SCLK}, 10 devices can be daisy-chained.

SPI COMMAND DEFINITIONS

The ADS1299 provides flexible configuration control. The opcode commands, summarized in Table 10, control and configure device operation. The opcode commands are stand-alone, except for the register read and write operations that require a second command byte plus data. $\overline{CS}$ can be taken high or held low between opcode commands but must stay low for the entire command operation (especially for multi-byte commands). System opcode commands and the RDATA command are decoded by the ADS1299 on the seventh SCLK falling edge. The register read and write opcodes are decoded on the eighth SCLK falling edge. Be sure to follow SPI timing requirements when pulling $\overline{CS}$ high after issuing a command.

Table 10. Command Definitions

COMMAND	DESCRIPTION	FIRST BYTE	SECOND BYTE
System Commands			
WAKEUP	Wake-up from standby mode	0000 0010 (02h)	
STANDBY	Enter standby mode	0000 0100 (04h)	
RESET	Reset the device	0000 0110 (06h)	
START	Start and restart (synchronize) conversions	0000 1000 (08h)	
STOP	Stop conversion	0000 1010 (0Ah)	
Data Read Commands			
RDATAC	Enable Read Data Continuous mode. This mode is the default mode at power-up.(1)	0001 0000 (10h)	
SDATAC	Stop Read Data Continuously mode	0001 0001 (11h)	
RDATA	Read data by command; supports multiple read back.	0001 0010 (12h)	
Register Read Commands			
RREG	Read *n nnnn* registers starting at address *r rrrr*	001*r rrrr* (2xh)(2)	000*n nnnn*(2)
WREG	Write *n nnnn* registers starting at address *r rrrr*	010*r rrrr* (4xh)(2)	000*n nnnn*(2)

(1) When in RDATAC mode, the RREG command is ignored.
(2) *n nnnn* = number of registers to be read or written – 1. For example, to read or write three registers, set *n nnnn* = 0 (0010). *r rrrr* = starting register address for read or write opcodes.

WAKEUP: Exit STANDBY Mode

This opcode exits low-power standby mode; see the *STANDBY: Enter STANDBY Mode* subsection of the *SPI Command Definitions* section. Time is required when exiting standby mode (see the Electrical Characteristics for details). **There are no SCLK rate restrictions for this command and it can be issued at any time.** Any following commands must be sent after a delay of 4 t_{CLK} cycles.

STANDBY: Enter STANDBY Mode

This opcode command enters low-power standby mode. All parts of the circuit are shut down except for the reference section. The standby mode power consumption is specified in the Electrical Characteristics. **There are no SCLK rate restrictions for this command and it can be issued at any time.** Do not send any other commands other than the wakeup command after the device enters standby mode.

RESET: Reset Registers to Default Values

This command resets the digital filter cycle and returns all register settings to default values. See the *Reset (RESET)* subsection of the *SPI Interface* section for more details. **There are no SCLK rate restrictions for this command and it can be issued at any time.** 18 t_{CLK} cycles are required to execute the RESET command. Avoid sending any commands during this time.

START: Start Conversions

This opcode starts data conversions. Tie the START pin low to control conversions by command. If conversions are in progress, this command has no effect. The STOP opcode command stops conversions. If the START command is immediately followed by a STOP command, then there must be a 4-t_{CLK} cycle delay between them. When the START opcode is sent to the device, keep the START pin low until the STOP command is issued. (See the *START* subsection of the *SPI Interface* section for more details.) **There are no SCLK rate restrictions for this command and it can be issued at any time.**

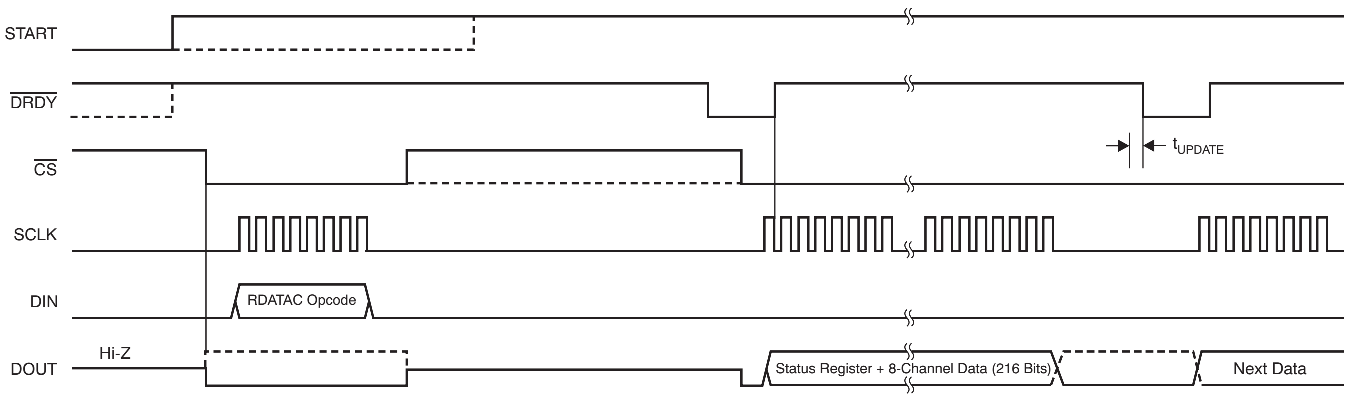
STOP: Stop Conversions

This opcode stops conversions. Tie the START pin low to control conversions by command. When the STOP command is sent, the conversion in progress completes and further conversions are stopped. If conversions are already stopped, this command has no effect. **There are no SCLK rate restrictions for this command and it can be issued at any time.**

RDATAC: Read Data Continuous

This opcode enables conversion data output on each $\overline{\text{DRDY}}$ without the need to issue subsequent read data opcodes. This mode places the conversion data in the output register and may be shifted out directly. The read data continuous mode is the device default mode; the ADS1299 defaults to this mode on power-up.

RDATAC mode is cancelled by the Stop Read Data Continuous command. If the device is in RDATAC mode, a SDATAC command must be issued before any other commands can be sent to the device. **There are no SCLK rate restrictions for this command.** However, subsequent data retrieval SCLKs or the SDATAC opcode command should wait at least 4 t_{CLK} cycles. RDATAC timing is shown in Figure 42. As Figure 42 shows, there is a *keep out* zone of 4 t_{CLK} cycles around the $\overline{\text{DRDY}}$ pulse where this command cannot be issued in. If no data are retrieved from the device, DOUT and $\overline{\text{DRDY}}$ behave similarly in this mode. To retrieve data from the device after the RDATAC command is issued, make sure either the START pin is high or the START command is issued. Figure 42 shows the recommended way to use the RDATAC command. RDATAC is ideally-suited for applications such as data loggers or recorders, where registers are set one time and do not need to be reconfigured.



(1) $t_{UPDATE} = 4 / f_{CLK}$. Do not read data during this time.

Figure 42. RDATAC Usage

SDATAC: Stop Read Data Continuous

This opcode cancels the Read Data Continuous mode. There are no SCLK rate restrictions for this command, but the next command must wait for 4 t_{CLK} cycles.

RDATA: Read Data

Issue this command after $\overline{DRDY}$ goes low to read the conversion result (in Stop Read Data Continuous mode). There are no SCLK rate restrictions for this command, and there is no wait time needed for the subsequent commands or data retrieval SCLKs. To retrieve data from the device after the RDATA command is issued, make sure either the START pin is high or the START command is issued. When reading data with the RDATA command, the read operation can overlap the next $\overline{DRDY}$ occurrence without data corruption. Figure 43 shows the recommended way to use the RDATA command. RDATA is best suited for ECG- and EEG-type systems, where register settings must be read or changed often between conversion cycles.

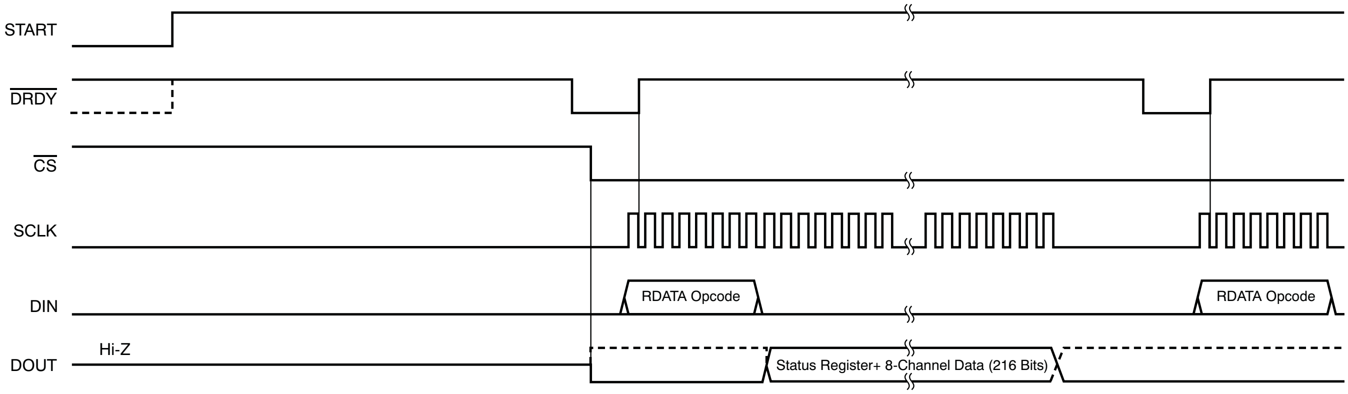


Figure 43. RDATA Usage

Sending Multi-Byte Commands

The ADS1299 serial interface decodes commands in bytes and requires 4 t_{CLK} cycles to decode and execute. Therefore, when sending multi-byte commands, a 4 t_{CLK} period must separate the end of one byte (or opcode) and the next.

Assuming CLK is 2.048 MHz, then $t_{SDECODE}$ (4 t_{CLK}) is 1.96 µs. When SCLK is 16 MHz, one byte can be transferred in 500 ns. This byte transfer time does not meet the $t_{SDECODE}$ specification; therefore, a delay must be inserted so the end of the second byte arrives 1.46 µs later. If SCLK is 4 MHz, one byte is transferred in 2 µs. Because this transfer time exceeds the $t_{SDECODE}$ specification, the processor can send subsequent bytes without delay. In this later scenario, the serial port can be programmed to move from single-byte transfers per cycle to multiple bytes.

RREG: Read From Register

This opcode reads register data. The Register Read command is a two-byte opcode followed by the register data output. The first byte contains the command opcode and register address. The second opcode byte specifies the number of registers to read – 1.

First opcode byte: 001*r rrrr*, where *r rrrr* is the starting register address.

Second opcode byte: 000*n nnnn*, where *n nnnn* is the number of registers to read – 1.

The 17th SCLK rising edge of the operation clocks out the MSB of the first register, as shown in Figure 44. When the device is in read data continuous mode, an SDATAC command must be issued before the RREG command can be issued. The RREG command can be issued any time. However, because this command is a multi-byte command, there are SCLK rate restrictions depending on how the SCLKs are issued. See the *Serial Clock (SCLK)* subsection of the *SPI Interface* section for more details. Note that $\overline{CS}$ must be low for the entire command.

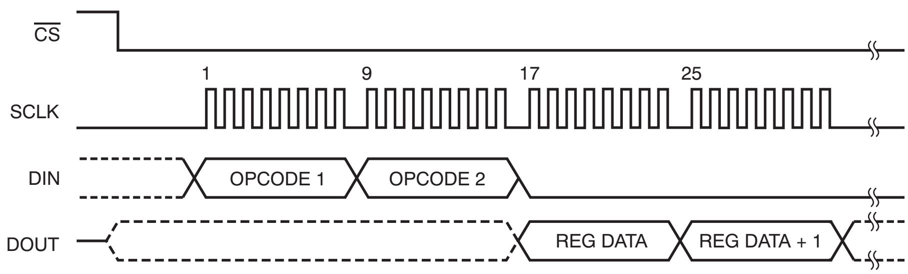


Figure 44. RREG Command Example: Read Two Registers Starting from Register 00h (ID Register) (OPCODE 1 = 0010 0000, OPCODE 2 = 0000 0001)

WREG: Write to Register

This opcode writes register data. The Register Write command is a two-byte opcode followed by the register data input. The first byte contains the command opcode and register address. The second opcode byte specifies the number of registers to write – 1.

First opcode byte: 010*r rrrr*, where *r rrrr* is the starting register address.

Second opcode byte: 000*n nnnn*, where *n nnnn* is the number of registers to write – 1.

After the opcode bytes, the register data follows (in MSB-first format), as shown in Figure 45. The WREG command can be issued any time. However, because this command is a multi-byte command, there are SCLK rate restrictions depending on how the SCLKs are issued. See the *Serial Clock (SCLK)* subsection of the *SPI Interface* section for more details. Note that $\overline{CS}$ must be low for the entire command.

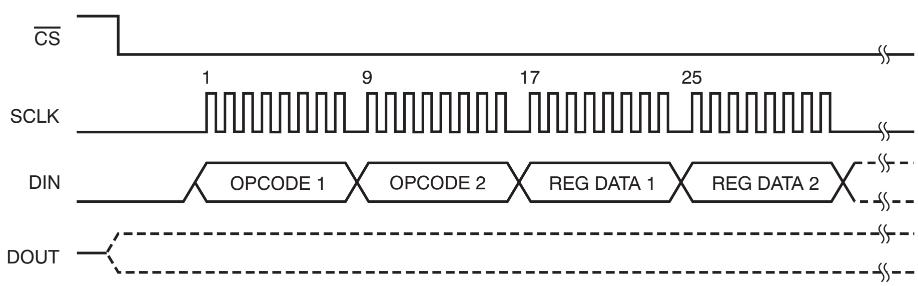


Figure 45. WREG Command Example: Write Two Registers Starting from 00h (ID Register) (OPCODE 1 = 0100 0000, OPCODE 2 = 0000 0001)

REGISTER MAP

Table 11 describes the various ADS1299 registers.

Table 11. Register Assignments

ADDRESS	REGISTER	RESET VALUE (Hex)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Device Settings (Read-Only Registers)										
00h	ID	00	REV_ID3	REV_ID2	REV_ID1	1	DEV_ID2	DEV_ID1	NU_CH2	NU_CH1
Global Settings Across Channels										
01h	CONFIG1	96	1	$\overline{\text{DAISY\_EN}}$	CLK_EN	1	0	DR2	DR1	DR0
02h	CONFIG2	C0	1	1	0	INT_CAL	0	CAL_AMP0	CAL_FREQ1	CAL_FREQ0
03h	CONFIG3	60	$\overline{\text{PD\_REFBUF}}$	1	1	BIAS_MEAS	BIASREF_INT	$\overline{\text{PD\_BIAS}}$	BIAS_LOFF_SENS	BIAS_STAT
04h	LOFF	00	COMP_TH2	COMP_TH1	COMP_TH0	0	ILEAD_OFF1	ILEAD_OFF0	FLEAD_OFF1	FLEAD_OFF0
Channel-Specific Settings										
05h	CH1SET	61	PD1	GAIN12	GAIN11	GAIN10	SRB2	MUX12	MUX11	MUX10
06h	CH2SET	61	PD2	GAIN22	GAIN21	GAIN20	SRB2	MUX22	MUX21	MUX20
07h	CH3SET	61	PD3	GAIN32	GAIN31	GAIN30	SRB2	MUX32	MUX31	MUX30
08h	CH4SET	61	PD4	GAIN42	GAIN41	GAIN40	SRB2	MUX42	MUX41	MUX40
09h	CH5SET	61	PD5	GAIN52	GAIN51	GAIN50	SRB2	MUX52	MUX51	MUX50
0Ah	CH6SET	61	PD6	GAIN62	GAIN61	GAIN60	SRB2	MUX62	MUX61	MUX60
0Bh	CH7SET	61	PD7	GAIN72	GAIN71	GAIN70	SRB2	MUX72	MUX71	MUX70
0Ch	CH8SET	61	PD8	GAIN82	GAIN81	GAIN80	SRB2	MUX82	MUX81	MUX80
0Dh	BIAS_SENSP	00	BIASP8	BIASP7	BIASP6	BIASP5	BIASP4	BIASP3	BIASP2	BIASP1
0Eh	BIAS_SENSN	00	BIASN8	BIASN7	BIASN6	BIASN5	BIASN4	BIASN3	BIASN2	BIASN1
0Fh	LOFF_SENSP	00	LOFFP8	LOFFP7	LOFFP6	LOFFP5	LOFFP4	LOFFP3	LOFFP2	LOFFP1
10h	LOFF_SENSN	00	LOFFM8	LOFFM7	LOFFM6	LOFFM5	LOFFM4	LOFFM3	LOFFM2	LOFFM1
11h	LOFF_FLIP	00	LOFF_FLIP8	LOFF_FLIP7	LOFF_FLIP6	LOFF_FLIP5	LOFF_FLIP4	LOFF_FLIP3	LOFF_FLIP2	LOFF_FLIP1
Lead-Off Status Registers (Read-Only Registers)										
12h	LOFF_STATP	00	IN8P_OFF	IN7P_OFF	IN6P_OFF	IN5P_OFF	IN4P_OFF	IN3P_OFF	IN2P_OFF	IN1P_OFF
13h	LOFF_STATN	00	IN8M_OFF	IN7M_OFF	IN6M_OFF	IN5M_OFF	IN4M_OFF	IN3M_OFF	IN2M_OFF	IN1M_OFF
GPIO and OTHER Registers										
14h	GPIO	0F	GPIOD4	GPIOD3	GPIOD2	GPIOD1	GPIOC4	GPIOC3	GPIOC2	GPIOC1
15h	MISC1	00	0	0	SRB1	0	0	0	0	0
16h	MISC2	00	0	0	0	0	0	0	0	0
17h	CONFIG4	00	0	0	0	0	SINGLE_SHOT	0	$\overline{\text{PD\_LOFF\_COMP}}$	0

User Register Description

ID: ID Control Register (Factory-Programmed, Read-Only)

Address = 00h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
REV_ID3	REV_ID2	REV_ID1	1	DEV_ID2	DEV_ID1	NU_CH2	NU_CH1

This register is programmed during device manufacture to indicate device characteristics.

Bits[7:5] **Not used**

Bit 4 **Must be set to '1'**

Bits[3:0] **Factory-programmed device identification bits**

1110 = ADS1299

CONFIG1: Configuration Register 1

Address = 01h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
1	$\overline{\text{DAISY\_EN}}$	CLK_EN	1	0	DR2	DR1	DR0

This register configures the $\overline{\text{DAISY\_EN}}$ bit, clock, and data rate.

Bit 7 **Must be set to '1'**

Bit 6 **$\overline{\text{DAISY\_EN}}$: Daisy-chain and multiple readback mode**

This bit determines which mode is enabled.
0 = Daisy-chain mode (default)
1 = Multiple readback mode

Bit 5 **CLK_EN: CLK connection[(1)]**

This bit determines if the internal oscillator signal is connected to the CLK pin when the CLKSEL pin = 1.
0 = Oscillator clock output disabled (default)
1 = Oscillator clock output enabled

Bits[4:3] **Must always be set to '10'**

Bits[2:0] **DR[2:0]: Output data rate**

$f_{MOD} = f_{CLK} / 2$.
These bits determine the output data rate of the device.

(1) Additional power is consumed when driving external devices.

BIT	DATA RATE	SAMPLE RATE[(1)]
000	f_{MOD} / 64	16 kSPS
001	f_{MOD} / 128	8 kSPS
010	f_{MOD} / 256	4 kSPS
011	f_{MOD} / 512	2 kSPS
100	f_{MOD} / 1024	1 kSPS
101	f_{MOD} / 2048	500 SPS
110 (default)	f_{MOD} / 4096	250 SPS
111	Do not use	n/a

(1) f_{CLK} = 2.048 MHz.

CONFIG2: Configuration Register 2

Address = 02h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
1	1	0	INT_CAL	0	CAL_AMP0	CAL_FREQ1	CAL_FREQ0

This register configures the test signal generation. See the *Input Multiplexer* section for more details.

Bits[7:5] **Must always be set to '110'**

Bit 4 **INT_CAL: TEST source**

This bit determines the source for the Test signal.
0 = Test signals are driven externally (default)
1 = Test signals are generated internally

Bit 3 **Must always be set to '0'**

Bit 2 **CAL_AMP0: Test signal amplitude**

This bit determines the calibration signal amplitude.
0 = 1 × (VREFP – VREFN) / 2.4 mV (default)
1 = 2 × (VREFP – VREFN) / 2.4 mV

Bits[1:0] **CAL_FREQ[1:0]: Test signal frequency**

These bits determine the calibration signal frequency.
00 = Pulsed at $f_{CLK} / 2^{21}$ (default)
01 = Pulsed at $f_{CLK} / 2^{20}$
10 = Not used
11 = At dc

CONFIG3: Configuration Register 3

Address = 03h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
$\overline{\text{PD\_REFBUF}}$	1	1	BIAS_MEAS	BIASREF_INT	$\overline{\text{PD\_BIAS}}$	BIAS_LOFF_SENS	BIAS_STAT

This register configures multi-reference and bias operations.

Bit 7 **$\overline{\text{PD\_REFBUF}}$: Power-down reference buffer**

This bit determines the power-down reference buffer state.
0 = Power-down internal reference buffer (default)
1 = Internal reference buffer enabled

Bits[6:5] **Must always be set to '1'**

Bit 4 **BIAS_MEAS: BIAS measurement**

This bit enables BIAS measurement. The BIAS signal may be measured with any channel.
0 = Open (default)
1 = BIASIN signal is routed to the channel that has the MUX_Setting *010* (V_{REF})

Bit 3 **BIASREF_INT: BIASREF signal**

This bit determines the BIASREF signal source.
0 = BIASREF signal fed externally (default)
1 = BIASREF signal (AVDD – AVSS) / 2 generated internally

Bit 2 **$\overline{\text{PD\_BIAS}}$: BIAS buffer power**

This bit determines the BIAS buffer power state.
0 = BIAS buffer is powered down (default)
1 = BIAS buffer is enabled

Bit 1 **BIAS_LOFF_SENS: BIAS sense function**

This bit enables the BIAS sense function.
0 = BIAS sense is disabled (default)
1 = BIAS sense is enabled

Bit 0 **BIAS_STAT: BIAS lead-off status**

This bit determines the BIAS status.
0 = BIAS is connected (default)
1 = BIAS is not connected

LOFF: Lead-Off Control Register

Address = 04h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
COMP_TH2	COMP_TH1	COMP_TH0	0	ILEAD_OFF1	ILEAD_OFF0	FLEAD_OFF1	FLEAD_OFF0

This register configures the lead-off detection operation.

Bits[7:5] **COMP_TH[2:0]: Lead-off comparator threshold**

These bits determine the lead-off comparator threshold level setting. See the *Lead-Off Detection* subsection of the *EEG-Specific Functions* section for a detailed description.

Comparator positive side

000 = 95% (default)
001 = 92.5%
010 = 90%
011 = 87.5%
100 = 85%
101 = 80%
110 = 75%
111 = 70%

Comparator negative side

000 = 5% (default)
001 = 7.5%
010 = 10%
011 = 12.5%
100 = 15%
101 = 20%
110 = 25%
111 = 30%

Bit 4 **Must always be set to '0'**

Bits[3:2] **ILEAD_OFF[1:0]: Lead-off current magnitude**

These bits determine the magnitude of current for the current lead-off mode.
00 = 6 nA (default)
01 = 24 nA
10 = 6 µA
11 = 24 µA

Bits[1:0] **FLEAD_OFF[1:0]: Lead-off frequency**

These bits determine the frequency of lead-off detect for each channel.
00 = DC lead-off detection (default)
01 = AC lead-off detection at 7.8 Hz (SYS_CLK / 2^{18})
10 = AC lead-off detection at 31.2 Hz (SYS_CLK / 2^{16})
11 = AC lead-off detection at f_{DR} / 4

CHnSET: Individual Channel Settings (n = 1:8)

Address = 05h to 0Ch

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PD1	GAIN12	GAIN11	GAIN10	SRB2	MUX12	MUX11	MUX10

This register configures the power mode, PGA gain, and multiplexer settings channels. See the *Input Multiplexer* section for details. CH[2:8]SET are similar to CH1SET, corresponding to the respective channels.

Bit 7 **PD: Power-down**

This bit determines the channel power mode for the corresponding channel.
0 = Normal operation (default)
1 = Channel power-down

Bits[6:4] **GAIN[2:0]: PGA gain**

These bits determine the PGA gain setting.

000 = 1
001 = 2
010 = 4
011 = 6
100 = 8
101 = 12
110 = 24 (default)
111 = n/a

Bit 3 **SRB2: Source, reference bias channel**

This bit determines the SRB2 connection for the corresponding channel.
0 = Open (off) (default)
1 = Closed (on)

Bits[2:0] **MUXn[2:0]: Channel input**

These bits determine the channel input selection.

000 = Normal electrode input (default)
001 = Input shorted (for offset or noise measurements)
010 = Used in conjunction with BIAS_MEAS bit for BIAS measurements. See the *Bias Drive (DC Bias Circuit)* subsection of the *EEG-Specific Functions* section for more details.
011 = MVDD for supply measurement
100 = Temperature sensor
101 = Test signal
110 = BIAS_DRP (positive electrode is the driver)
111 = BIAS_DRN (negative electrode is the driver)

BIAS_SENSP: Bias Drive Positive Sense Selection

Address = 0Dh

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
BIASP8	BIASP7	BIASP6	BIASP5	BIASP4	BIASP3	BIASP2	BIASP1

This register controls the selection of positive signals from each channel for bias drive derivation. See the *Bias Drive (DC Bias Circuit)* subsection of the *EEG-Specific Functions* section for details.

BIAS_SENSN: Bias Drive Negative Sense Selection

Address = 0Eh

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
BIASN8	BIASN7	BIASN6	BIASN5	BIASN4	BIASN3	BIASN2	BIASN1

This register controls the selection of negative signals from each channel for bias drive derivation. See the *Bias Drive (DC Bias Circuit)* subsection of the *EEG-Specific Functions* section for details.

LOFF_SENSP: Lead Off Positive Sense Selection

Address = 0Fh

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
LOFFP8	LOFFP7	LOFFP6	LOFFP5	LOFFP4	LOFFP3	LOFFP2	LOFFP1

This register selects the positive side from each channel for lead-off detection. See the *Lead-Off Detection* subsection of the *EEG-Specific Functions* section for details. Note that the LOFF_STATP register bits are only valid if the corresponding LOFF_SENSP bits are set to '1'.

LOFF_SENSN: Lead Off Negative Sense Selection

Address = 10h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
LOFFM8	LOFFM7	LOFFM6	LOFFM5	LOFFM4	LOFFM3	LOFFM2	LOFFM1

This register selects the negative side from each channel for lead-off detection. See the *Lead-Off Detection* subsection of the *EEG-Specific Functions* section for details. Note that the LOFF_STATN register bits are only valid if the corresponding LOFF_SENSN bits are set to '1'.

LOFF_FLIP: Lead Off Current Direction Control

Address = 11h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
LOFF_FLIP8	LOFF_FLIP7	LOFF_FLIP6	LOFF_FLIP5	LOFF_FLIP4	LOFF_FLIP3	LOFF_FLIP2	LOFF_FLIP1

This register controls the current direction used for lead-off derivation. See the *Lead-Off Detection* subsection of the *EEG-Specific Functions* section for details.

LOFF_STATP: Lead-Off Positive Input Status

Address = 12h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IN8P_OFF	IN7P_OFF	IN6P_OFF	IN5P_OFF	IN4P_OFF	IN3P_OFF	IN2P_OFF	IN1P_OFF

This register stores the status of whether the positive electrode on each channel is on or off. See the *Lead-Off Detection* subsection of the *EEG-Specific Functions* section for details. Ignore the LOFF_STATP values if the corresponding LOFF_SENSP bits are not set to '1'.

'0' is lead-on (default) and '1' is lead-off. When the LOFF_SENSP bits are '0', the LOFF_STATP bits should be ignored.

LOFF_STATN: Lead-Off Negative Input Status

Address = 13h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IN8M_OFF	IN7M_OFF	IN6M_OFF	IN5M_OFF	IN4M_OFF	IN3M_OFF	IN2M_OFF	IN1M_OFF

This register stores the status of whether the negative electrode on each channel is on or off. See the *Lead-Off Detection* subsection of the *EEG-Specific Functions* section for details. Ignore the LOFF_STATN values if the corresponding LOFF_SENSN bits are not set to '1'.

'0' is lead-on (default) and '1' is lead-off. When the LOFF_SENSN bits are '0', the LOFF_STATP bits should be ignored.

GPIO: General-Purpose I/O Register

Address = 14h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
GPIOD4	GPIOD3	GPIOD2	GPIOD1	GPIOC4	GPIOC3	GPIOC2	GPIOC1

This register controls the action of the four GPIO pins.

Bits[7:4] **GPIOD[4:1]: GPIO data**

These bits are used to read and write data to the GPIO ports.
When reading the register, the data returned correspond to the state of the GPIO external pins, whether they are programmed as inputs or as outputs. As outputs, a write to the GPIOD sets the output value. As inputs, a write to the GPIOD has no effect.

Bits[3:0] **GPIOC[4:1]: GPIO control (corresponding GPIOD)**

These bits determine if the corresponding GPIOD pin is an input or output.
0 = Output
1 = Input (default)

MISC1: Miscellaneous 1

Address = 15h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	0	SRB1	0	0	0	0	0

This register is for miscellaneous use.

Bits[7:6] **Must always be set to '0'**

Bit 5 **SRB1: Stimulus, reference, and bias 1**

This bit connects the SRB1 to all eight channels inverting inputs.
0 = Switches open (default)
1 = Switches closed

Bits[4:0] **Must always be set to '0'**

MISC2: Miscellaneous 2

Address = 16h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	0	0	0	0	0	0	0

This register is for miscellaneous use.

Bits[7:0] **Must always be set to '0'**

CONFIG4: Configuration Register 4

Address = 17h

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	0	0	0	SINGLE_SHOT	0	$\overline{\text{PD\_LOFF\_COMP}}$	0

Bits[7:4] **Must always be set to '0'**

Bit 3 **SINGLE_SHOT: Single-shot conversion**

This bit sets the conversion mode.
0 = Continuous conversion mode (default)
1 = Single-shot mode

Bit 2 **Must always be set to '0'**

Bit 1 **$\overline{\text{PD\_LOFF\_COMP}}$: Lead-off comparator power-down**

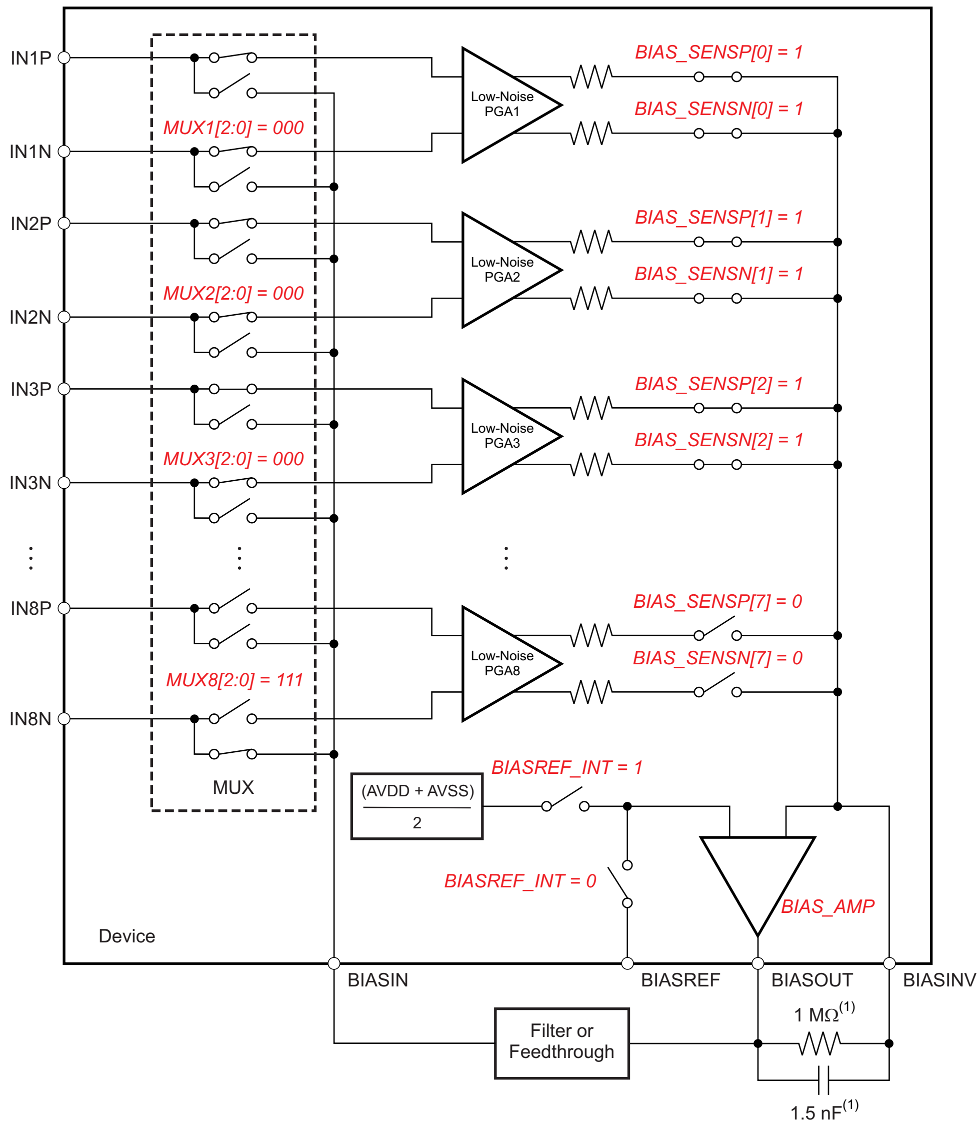
This bit powers down the lead-off comparators.
0 = Lead-off comparators disabled (default)
1 = Lead-off comparators enabled

Bit 0 **Must always be set to '0'**

EEG-SPECIFIC FUNCTIONS

INPUT MULTIPLEXER (Rerouting the BIAS Drive Signal)

The input multiplexer has EEG-specific functions for the bias drive signal. The BIAS signal is available at the BIASOUT pin when the appropriate channels are selected for BIAS derivation, feedback elements are installed external to the chip, and the loop is closed. This signal can either be fed after filtering or fed directly into the BIASIN pin, as shown in Figure 46. This BIASIN signal can be multiplexed into any input electrode by setting the MUX bits of the appropriate channel set registers to '110' for P-side or '111' for N-side. Figure 46 shows the BIAS signal generated from channels 1, 2, and 3 and routed to the N-side of channel 8. This feature can be used to dynamically change the electrode that is used as the reference signal to drive the patient body.

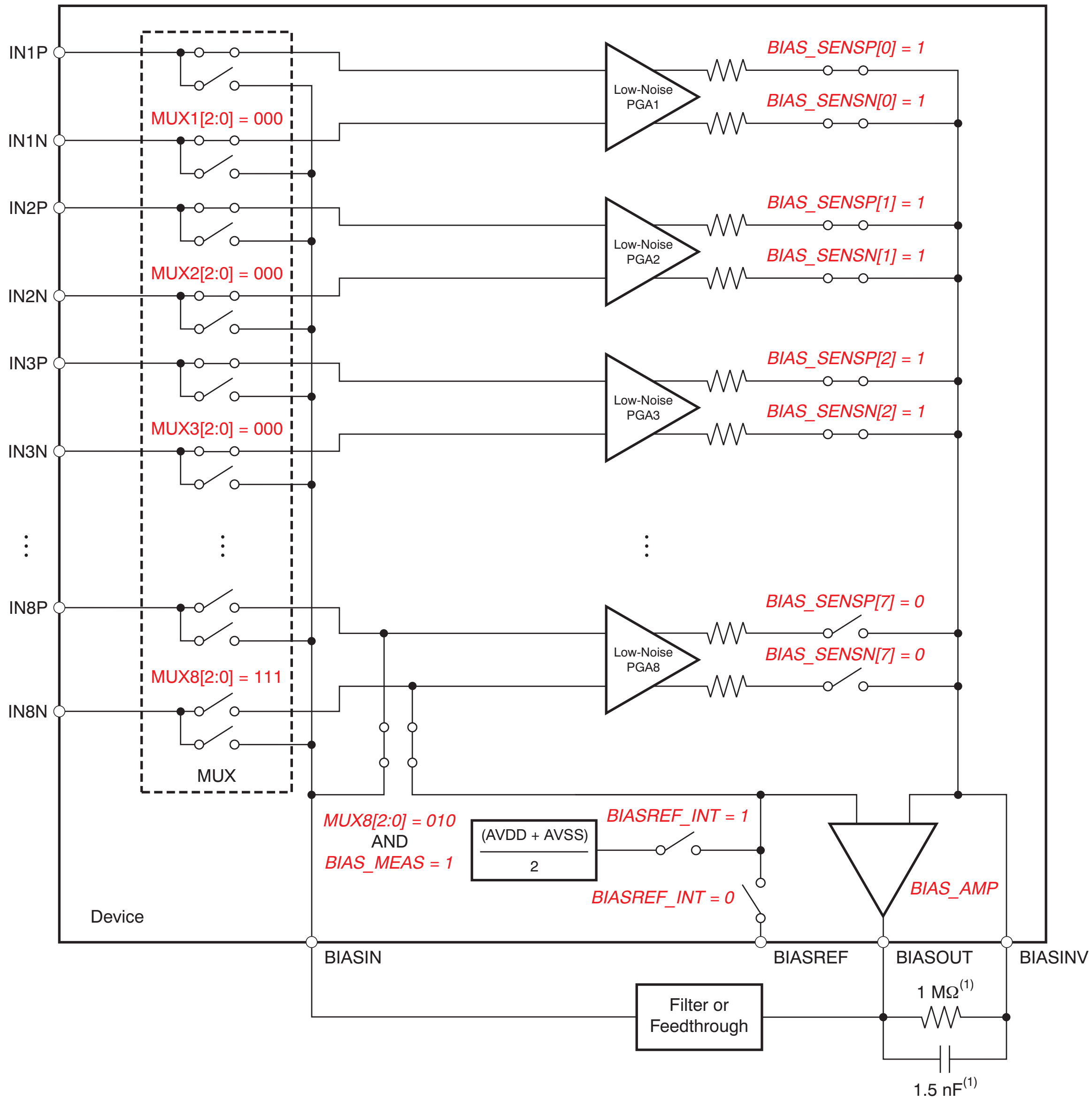


(1) Typical values for example only.

Figure 46. Example of BIASOUT Signal Configured to be Routed to IN8N

INPUT MULTIPLEXER (Measuring the BIAS Drive Signal)

Also, the BIASOUT signal can be routed to a channel (that is not used for the calculation of BIAS) for measurement. Figure 47 shows the register settings to route the BIASIN signal to channel 8. The measurement is done with respect to the voltage on the BIASREF pin. If BIASREF is chosen to be internal, it would be at [(AVDD + AVSS) / 2]. This feature is useful for debugging purposes during product development.



(1) Typical values for example only.

Figure 47. BIASOUT Signal Configured to be Read Back by Channel 8

LEAD-OFF DETECTION

Patient electrode impedances are known to decay over time. These electrode connections must be continuously monitored to verify that a suitable connection is present. The ADS1299 lead-off detection functional block provides significant flexibility to the user to choose from various lead-off detection strategies. Though called lead-off detection, this is in fact an *electrode-off* detection.

The basic principle is to inject an excitation signal and measure the response to determine if the electrode is off. As shown in the lead-off detection functional block diagram in Figure 48, this circuit provides two different methods of determining the state of the patient electrode. The methods differ in the frequency content of the excitation signal. Lead-off can be selectively done on a per channel basis using the LOFF_SENSP and LOFF_SENSN registers. Also, the internal excitation circuitry can be disabled and just the sensing circuitry can be enabled.

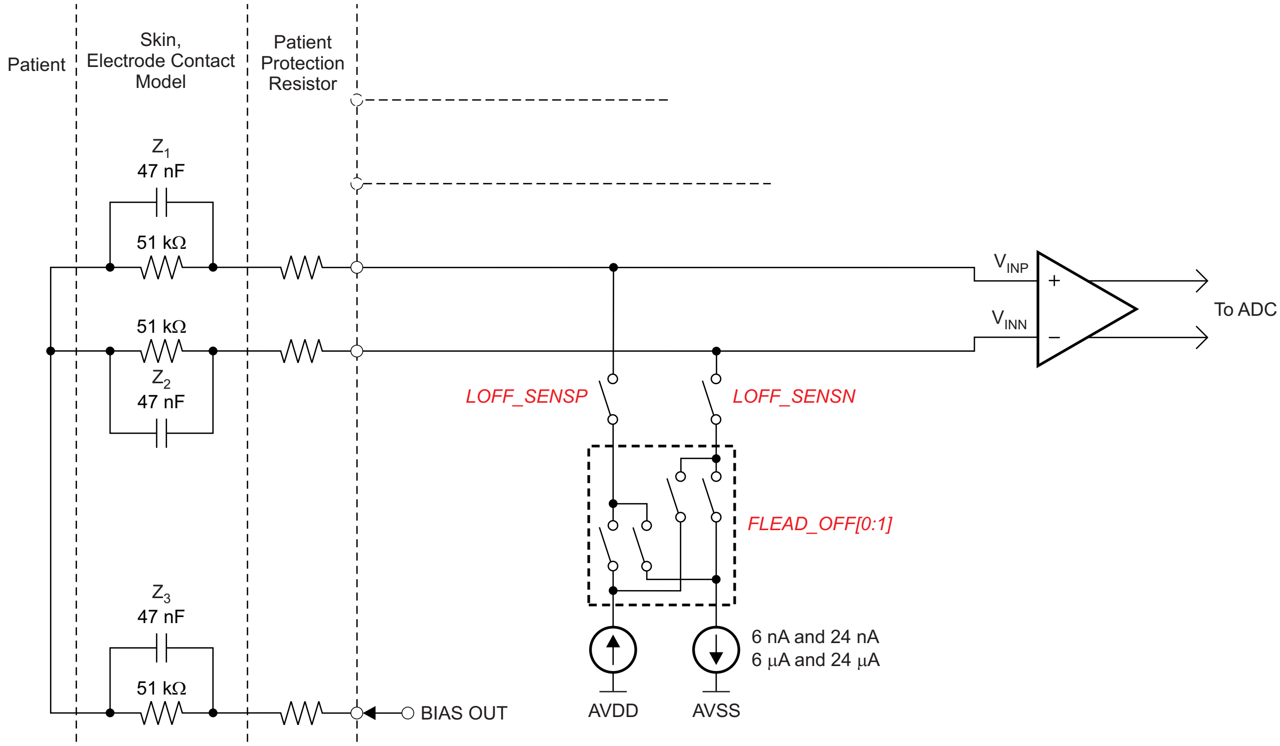


Figure 48. Lead-Off Detection

DC Lead-Off

In this method, the lead-off excitation is with a dc signal. The dc excitation signal can be chosen from either an external pull-up or pull-down resistor or an internal current source or sink, as shown in Figure 49. One side of the channel is pulled to supply and the other side is pulled to ground. The pull-up and pull-down current can be swapped (as shown in Figure 49b and Figure 49c) by setting the bits in the LOFF_FLIP register. In case of a current source or sink, the magnitude of the current can be set by using the ILEAD_OFF[1:0] bits in the LOFF register. The current source or sink gives larger input impedance compared to the 10-MΩ pull-up or pull-down resistor.

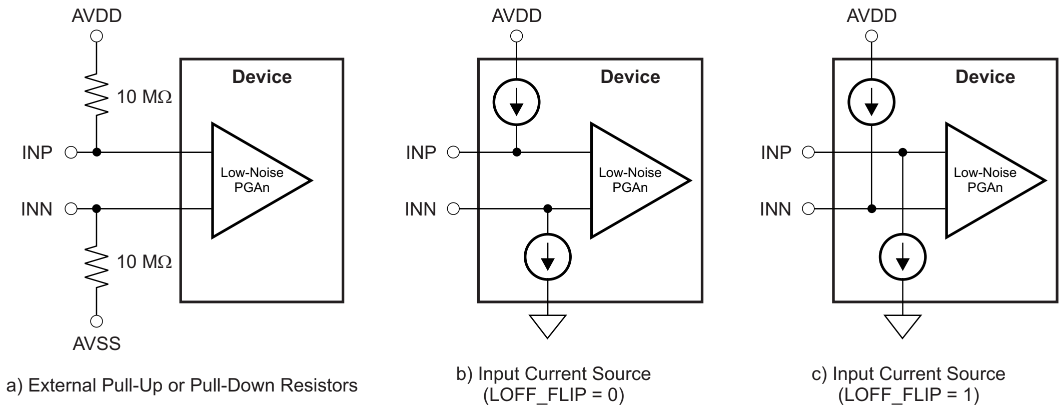


Figure 49. DC Lead-Off Excitation Options

Sensing of the response can be done either by searching the digital output code from the device or by monitoring the input voltages with an on-chip comparator. If either electrode is off, the pull-up and pull-down resistors saturate the channel. Searching the output code determines if either the P-side or the N-side is off. To pinpoint which one is off, the comparators must be used. The input voltage is also monitored using a comparator and a 3-bit DAC whose levels are set by the COMP_TH[2:0] bits in the LOFF register. The output of the comparators are stored in the LOFF_STATP and LOFF_STATN registers. These registers are available as a part of the output data stream. (See the *Data Output (DOUT)* subsection of the *SPI Interface* section.) If dc lead-off is not used, the lead-off comparators can be powered down by setting the PD_LOFF_COMP bit in the CONFIG4 register.

An example procedure to turn on dc lead-off is given in the *Lead-Off* subsection of the *Quick-Start Guide* section.

AC Lead-Off (One Time or Periodic)

In this method, an in-band ac signal is used for excitation. The ac signal is generated by alternatively providing a current source and sink at the input with a fixed frequency. The frequency can be chosen by the FLEAD_OFF[1:0] bits in the LOFF register. The excitation frequency is chosen to be one of the two in-band frequency selections (7.8 Hz or 31.2 Hz). This in-band excitation signal is passed through the channel and measured at the output.

Sensing of the ac signal is done by passing the signal through the channel to digitize it and measure at the output. The ac excitation signals are introduced at a frequency that is in the band of interest. The signal can be filtered out separately and processed. By measuring the magnitude of the excitation signal at the output spectrum, the electrode impedance can be calculated.

For continuous lead-off, an out-of-band ac current source or sink must be externally applied to the inputs. This signal can then be digitally post processed to determine the electrode impedance.

BIAS LEAD-OFF

The ADS1299 provides two modes for determining whether the BIAS is correctly connected:

- BIAS lead-off detection during normal operation
- BIAS lead-off detection during power-up

The following sections provide details of the two modes of operation.

BIAS Lead-Off Detection During Normal Operation

During normal operation, the ADS1299 BIAS lead-off at power-up function cannot be used because it is necessary to power off the BIAS amplifier.

BIAS Lead Off Detection At Power-Up

This feature is included in the ADS1299 for use in determining whether the bias electrode is suitably connected. At power-up, the ADS1299 provides two measurement procedures to determine the BIAS electrode connection status using either a current or an external pull-down resistor, as shown in Figure 50. The reference level of the comparator is set to determine the acceptable BIAS impedance threshold.

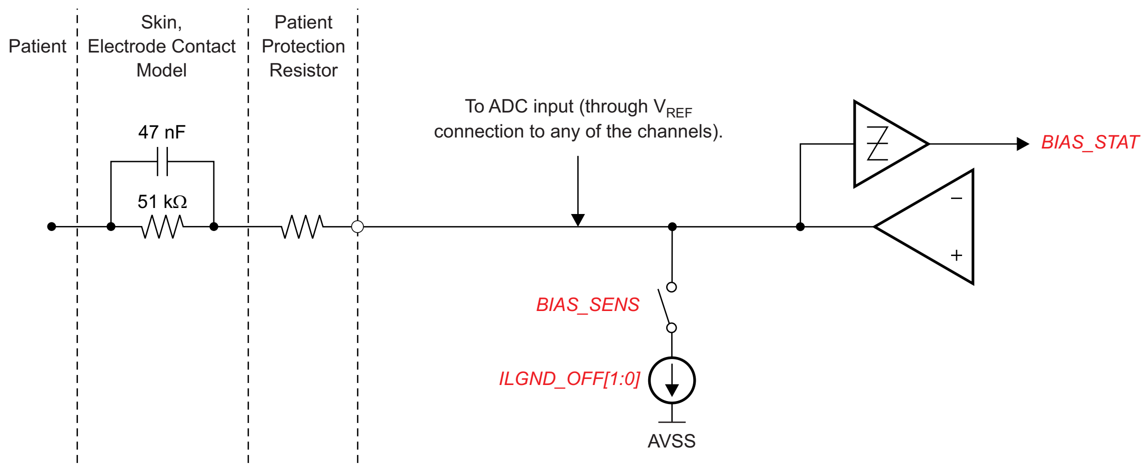


Figure 50. BIAS Lead-Off Detection at Power-Up

When the BIAS amplifier is powered on, the current source has no function. Only the comparator can be used to sense the voltage at the output of the BIAS amplifier. The comparator thresholds are set by the same LOFF[7:5] bits used to set the thresholds for other negative inputs.

BIAS DRIVE (DC BIAS CIRCUIT)

The bias circuitry is used as a means to counter the common-mode interference in a EEG system as a result of power lines and other sources, including fluorescent lights. The bias circuit senses the common-mode of a selected set of electrodes and creates a negative feedback loop by driving the body with an inverted common-mode signal. The negative feedback loop restricts the common-mode movement to a narrow range, depending on the loop gain. Stabilizing the entire loop is specific to the individual user system based on the various poles in the loop. The ADS1299 integrates the muxes to select the channel and an operational amplifier. All amplifier terminals are available at the pins, allowing the user to choose the components for the feedback loop. The circuit in Figure 52 illustrates the overall functional connectivity for the bias circuit.

The reference voltage for the bias drive can be chosen to be internally generated [(AVDD + AVSS) / 2] or it can be provided externally with a resistive divider. The selection of an internal versus external reference voltage for the bias loop is defined by writing the appropriate value to the BIASREF_INT bit in the CONFIG2 register.

If the bias function is not used, the amplifier can be powered down using the PD_BIAS bit (see the *CONFIG3: Configuration Register 3* subsection of the *Register Map* section for details). This bit is also used in daisy-chain mode to power-down all but one of the bias amplifiers.

The BIASIN pin functionality is explained in the *Input Multiplexer* section. An example procedure to use the bias amplifier is shown in the *Bias Drive* subsection of the *Quick-Start Guide* section.

Bias Configuration with Multiple Devices

Figure 51 shows multiple devices connected to the bias drive.

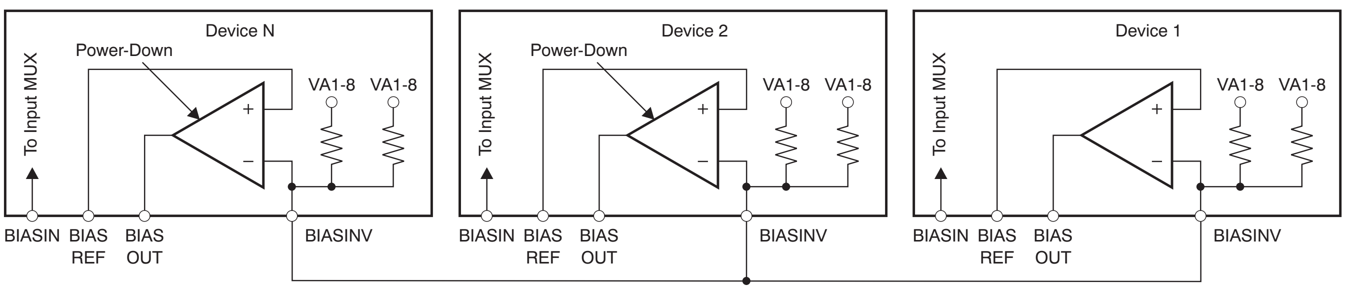
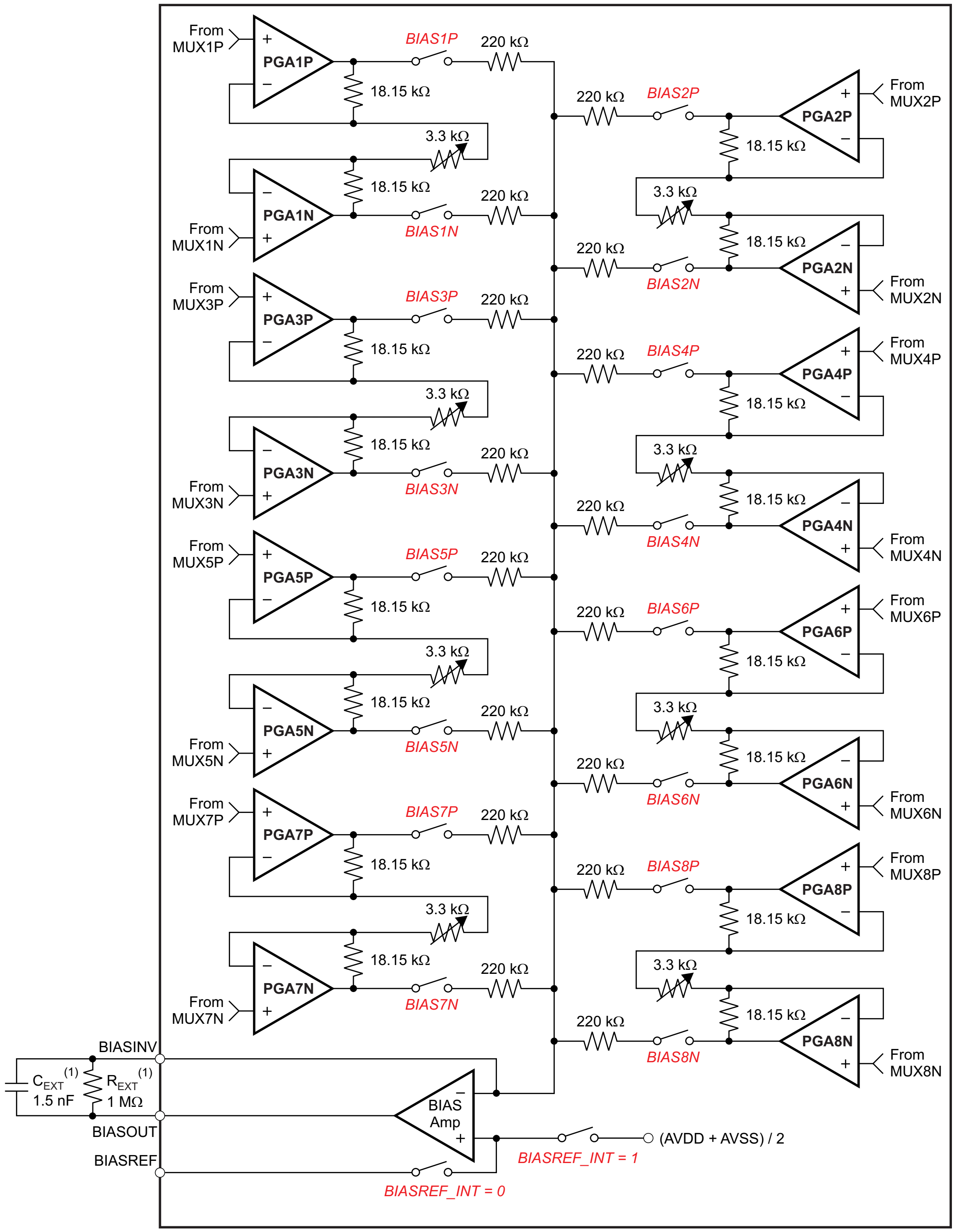


Figure 51. Bias Drive Connection for Multiple Devices



(1) Typical values.

Figure 52. Bias Channel Selection

QUICK-START GUIDE

PCB LAYOUT

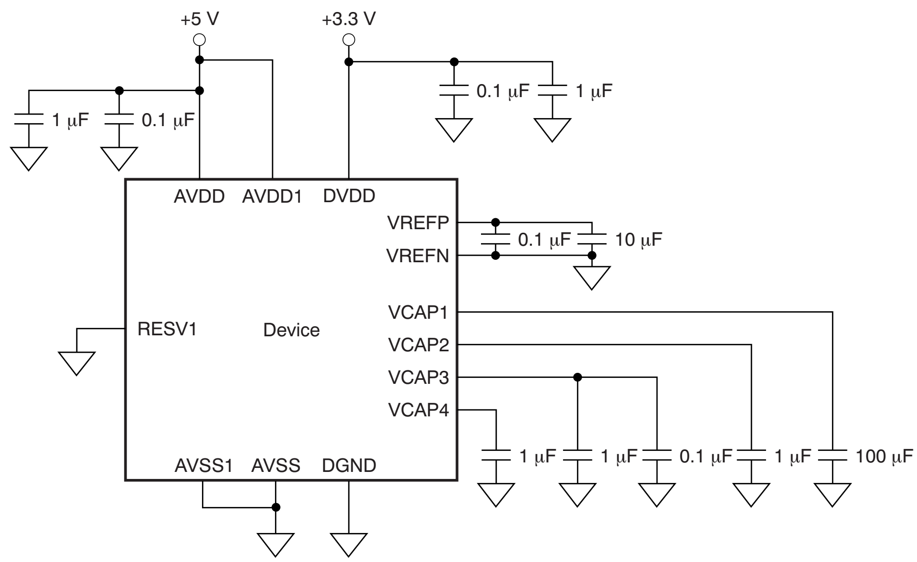
Power Supplies and Grounding

The ADS1299 has three supplies: AVDD, AVDD1, and DVDD. Both AVDD and AVDD1 should be as quiet as possible. AVDD1 provides the supply to the charge pump block and has transients at f_{CLK}. Therefore, AVDD1 and AVSS1 are recommended to be star-connected to AVDD and AVSS. It is important to eliminate noise from AVDD and AVDD1 that is non-synchronous with the ADS1299 operation. Each ADS1299 supply should be bypassed with 10-µF and a 0.1-µF solid ceramic capacitors. Placement of the digital circuits [(such as digital signal processors (DSPs), microcontrollers, and field-programmable gate arrays (FPGAs)] in the system is recommenced to done such that the return currents on those devices do not cross the analog return path of the ADS1299. The ADS1299 can be powered from unipolar or bipolar supplies.

The capacitors used for decoupling can be surface-mount, low-cost, low-profile multi-layer ceramic capacitors. In most cases, the VCAP1 capacitor can also be a multi-layer ceramic, but in systems where the board is subjected to high- or low-frequency vibration, it is recommend that a non-ferroelectric capacitor such as a tantalum or class 1 capacitor (for example, C0G or NPO) be installed. EIA class 2 and class 3 dielectrics (such as X7R, X5R, and X8R) are ferroelectric. The piezoelectric property of these capacitors can appear as electrical noise coming from the capacitor. When using internal reference, noise on the VCAP1 node results in performance degradation.

Connecting the Device to Unipolar (+5 V and +3.3 V) Supplies

Figure 53 illustrates the ADS1299 connected to a unipolar supply. In this example, analog supply (AVDD) is referenced to analog ground (AVSS) and digital supply (DVDD) is referenced to digital ground (DGND).

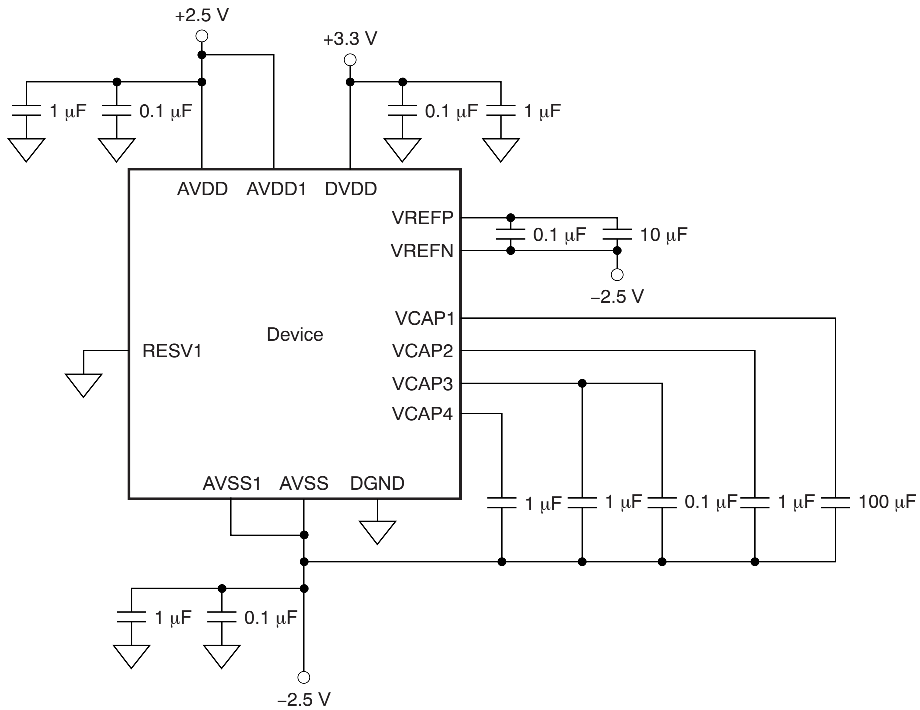


NOTE: Place the capacitors for supply, reference, and VCAP1 to VCAP4 as close to the package as possible.

Figure 53. Single-Supply Operation

Connecting the Device to Bipolar (±2.5 V and 3.3 V) Supplies

Figure 54 illustrates the ADS1299 connected to a bipolar supply. In this example, the analog supplies connect to the device analog supply (AVDD). This supply is referenced to the device analog return (AVSS), and the digital supply (DVDD) is referenced to the device digital ground return (DGND).



NOTE: Place the capacitors for supply, reference, and VCAP1 to VCAP4 as close to the package as possible.

Figure 54. Bipolar Supply Operation

Shielding Analog Signal Paths

As with any precision circuit, careful PCB layout ensures the best performance. It is essential to make short, direct interconnections and avoid stray wiring capacitance—particularly at the analog input pins and AVSS. These analog input pins are high-impedance and extremely sensitive to extraneous noise. The AVSS pin should be treated as a sensitive analog signal and connected directly to the supply ground with proper shielding. Leakage currents between the PCB traces can exceed the input bias current of the ADS1299 if shielding is not implemented. Digital signals should be kept as far as possible from the analog input signals on the PCB.

POWER-UP SEQUENCING

Before device power-up, all digital and analog inputs must be low. At the time of power-up, all of these signals should remain low until the power supplies have stabilized, as shown in Figure 55. At this time, begin supplying the master clock signal to the CLK pin. Wait for time t_{POR}, then transmit a RESET pulse. After releasing RESET, the configuration register must be programmed; see the *CONFIG1: Configuration Register 1* subsection of the *Register Map* section for details. The power-up sequence timing is shown in Table 12.

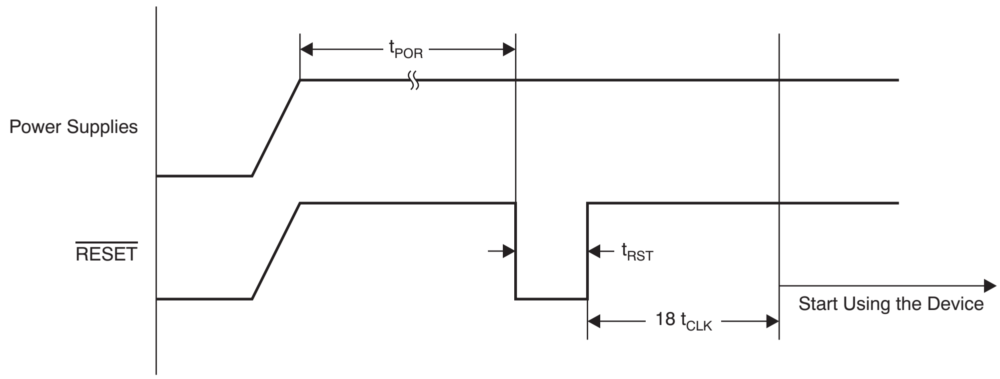


Figure 55. Power-Up Timing Diagram

Table 12. Power-Up Sequence Timing

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
t_{POR}	Wait after power-up until reset	2^{16}			t_{CLK}
t_{RST}	Reset low width	2			t_{CLK}

SETTING THE DEVICE FOR BASIC DATA CAPTURE

This section outlines the procedure to configure the device in a basic state and capture data. This procedure is intended to put the device in a data sheet condition to check if the device is working properly in the user system. This procedure is recommended to be followed initially to get familiar with the device settings. When this procedure is verified, the device can be configured as needed. For details on the timings for commands, refer to the appropriate sections in the data sheet. Also, some sample programming codes are added for the EEG-specific functions.

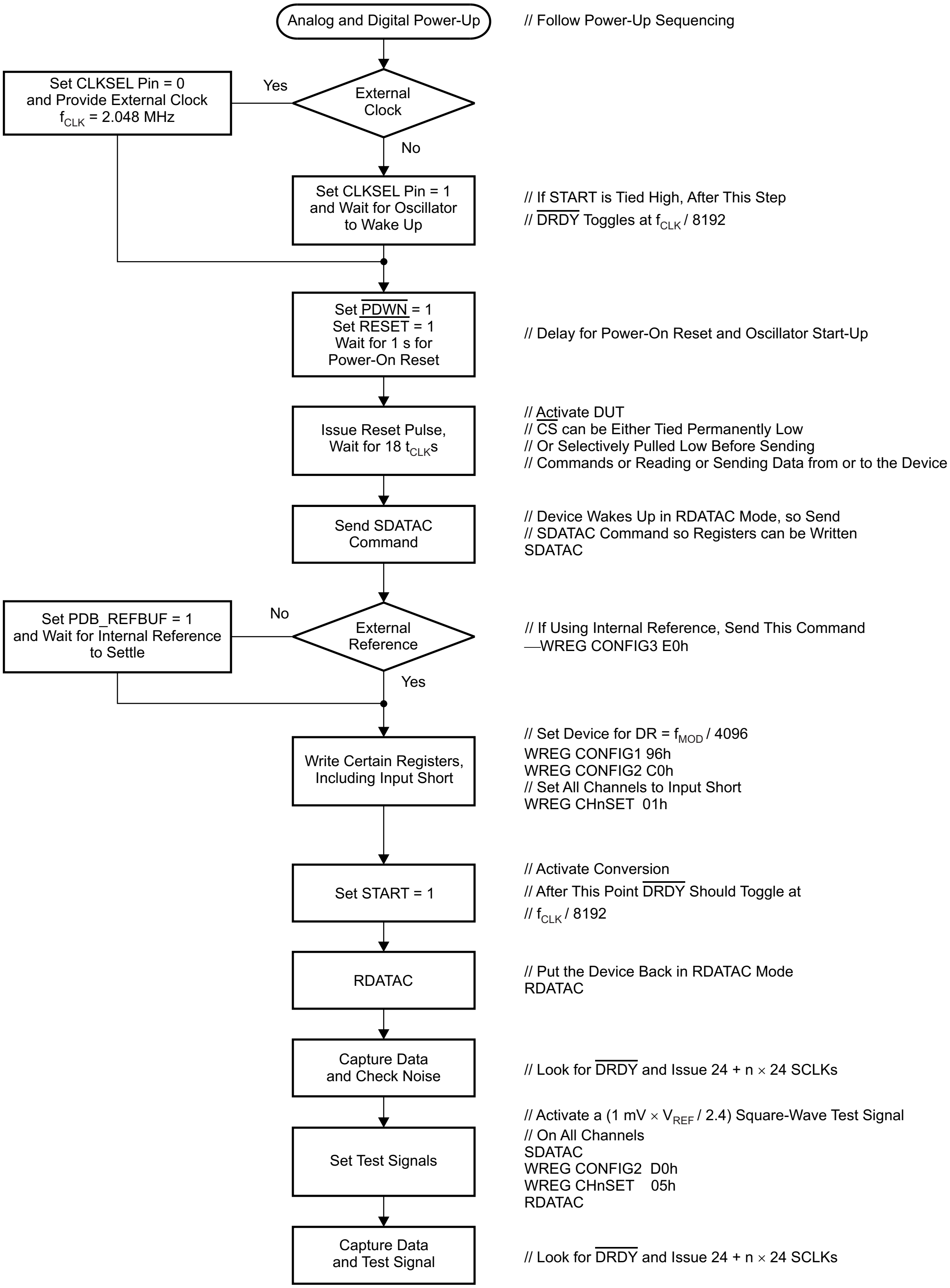


Figure 56. Initial Flow at Power-Up

Lead-Off

Sample code to set dc lead-off with pull-up and pull-down resistors on all channels.

WREG LOFF 00h // Comparator threshold at 95% and 5%, pull-up or pull-down current source // DC lead-off

WREG CONFIG4 02h // Turn-on dc lead-off comparators

WREG LOFF_SENSP FFh // Turn on the P-side of all channels for lead-off sensing

WREG LOFF_SENSN FFh // Turn on the N-side of all channels for lead-off sensing

Observe the status bits of the output data stream to monitor lead-off status.

Bias Drive

Sample code to choose bias as an average of the first three channels.

WREG BIAS_SENSP 07h // Select channel 1—3 P-side for bias sensing

WREG BIAS_SENSN 07h // Select channel 1—3 N-side for bias sensing

WREG CONFIG3 b'x11x 1100 // Turn on bias amplifier, set internal BIASREF voltage

Sample code to route the BIASOUT signal through channel 4 N-side and measure bias with channel 5. Make sure the external side to the chip BIASOUT is connected to BIASIN.

WREG CONFIG3 b'x111 1100 // Turn on bias amplifier, set internal BIASREF voltage, set bias measurement bit

WREG CH4SET b'xxxx 0111 // Route BIASIN to channel 4 N-side

WREG CH5SET b'xxxx 0010 // Route BIASIN to be measured at channel 5 w.r.t BIASREF

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (July 2012) to Revision A	Page
• Changed product column of Family and Ordering Information table	2

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
ADS1299IPAG	ACTIVE	TQFP	PAG	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
ADS1299IPAGR	ACTIVE	TQFP	PAG	64	1500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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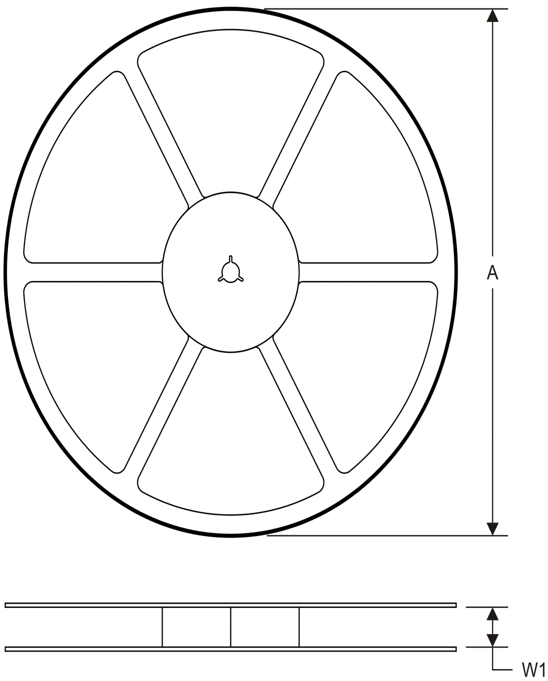
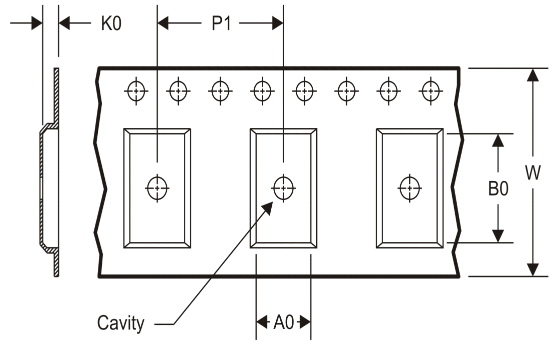
TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



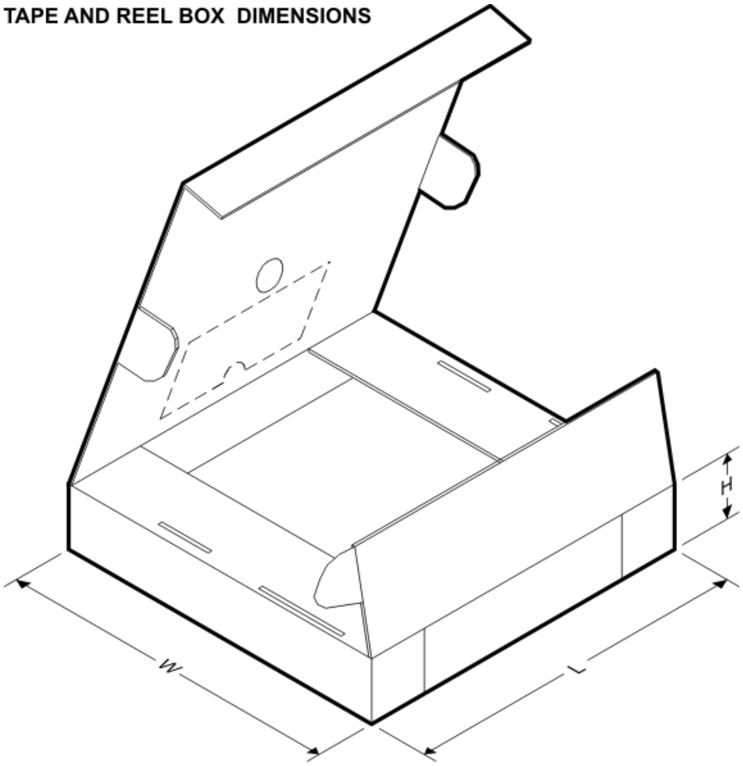
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS1299IPAGR	TQFP	PAG	64	1500	330.0	24.4	13.0	13.0	1.5	16.0	24.0	Q2

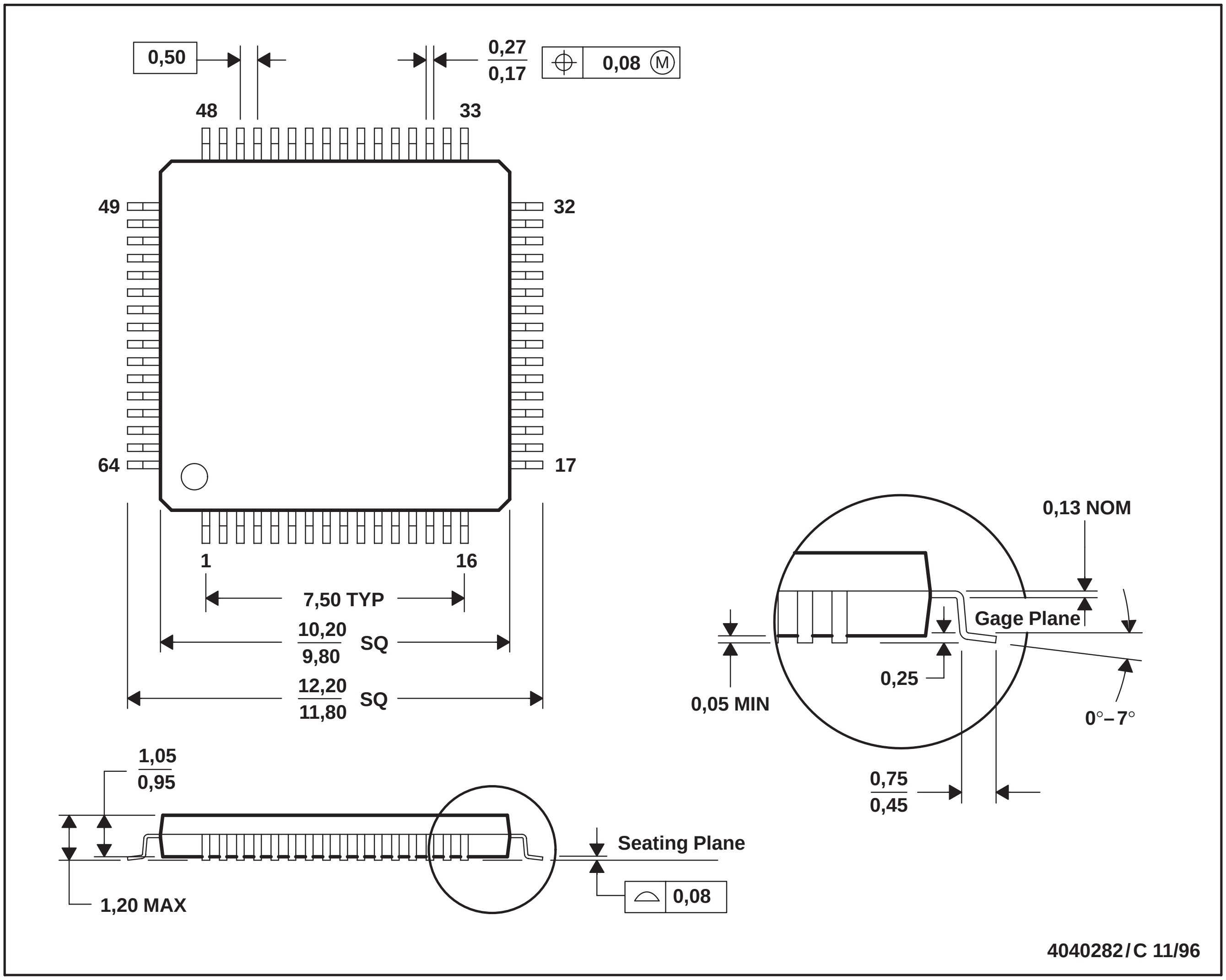
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS1299IPAGR	TQFP	PAG	64	1500	367.0	367.0	45.0

PAG (S-PQFP-G64) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

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- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.

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