

LOW-POWER DUAL C-MOS OPERATIONAL AMPLIFIER

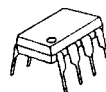
■ GENERAL DESCRIPTION

The NJU7014/7015/7016 are single supply dual C-MOS operational amplifiers featuring a low operating voltage from 1V and low operating current of 15 μ A/circuit (7014 typ.), 80 μ A/circuit (7015 typ.), 200 μ A/circuit (7016 typ.).

They also have a low input bias current of 1pA (typ.) and input voltage range from ground, which can provide a ground sensing, and rail-to-rail output swing in both rails.

The NJU7014/7015/7016 are available in a wide variety of 8-lead packages, dual-in-line DIP8, surface-mount SOP8 (DMP8), SSOP8, MSOP8 (VSP8), MSOP8 (TVSP8). The combination of these specifications makes them ideal for a variety of portable devices.

■ PACKAGE OUTLINE



NJU7015D
NJU7016D
(DIP8)



NJU7014M
NJU7015M
NJU7016M
(DMP8)



NJU7014V
NJU7015V
NJU7016V
(SSOP8)



NJU7014R
NJU7015R
NJU7016R
(MSOP8(VSP8))



NJU7014RB1
NJU7015RB1
NJU7016RB1
(MSOP8(TVSP8))

■ FEATURES

- Single Power Supply
- Wide Operating Voltage $V_{DD}=1\sim 5.5V$
- Wide Output Swing Range $V_{OM}=2.9V$ min. (@ $V_{DD}=3.0V$)
- Low Operating Current
- Low Bias Current $I_B=1pA$ typ.
- Compensation Capacitor Incorporated
- C-MOS Technology
- Package Outline

NJU7015D, NJU7016D : DIP8

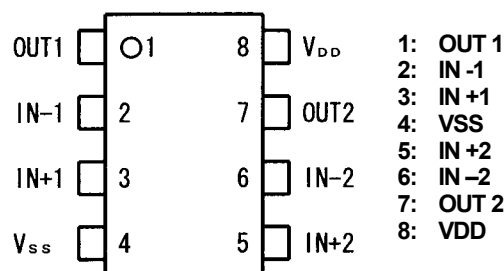
NJU7014M, NJU7015M, NJM7016M : DMP8

NJU7014V, NJU7015V, NJM7016V : SSOP8

NJU7014R, NJU7015R, NJM7016R : MSOP8(VSP8) MEET JEDEC MO-187-DA

NJU7014RB1, NJU7015RB1, NJM7016RB1 : MSOP8(VSP8) MEET JEDEC MO-187-DA / THIN TYPE

■ PIN CONFIGURATION



■ LINE-UP

($T_a=25^{\circ}C, V_{DD}=3.0V$, Per Circuit)

PARAMETER	NJU7014	NJU7015	NJU7016	UNIT
Operating Current	15	80	200	μ A (typ)
Slew Rate	0.1	1.0	2.4	V/ μ s (typ)
Unity Gain Bandwidth	0.2	1.0	1.0	MHz (typ)

NJU7014/15/16

■ EQUIVALENT CIRCUIT



■ ABSOLUTE MAXIMUM RATINGS

(Ta=25°C)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{DD}	7	V
Differential Input Voltage	V_{ID}	± 7 (note1)	V
Common Mode Input Voltage	V_{IC}	-0.3~7	V
Power Dissipation	P_D	(DIP8) 500 (DMP8) 300 (SSOP8) 250 (MSOP8(VSP8)) 320 (MSOP8(TVSP8)) 320	mW
Operating Temperature Range	T_{opr}	-40~+85	°C
Storage Temperature Range	T_{stg}	-55~+125	°C

(note1) If the supply voltage (V_{DD}) is less than 7V, the input voltage must not over the V_{DD} level though 7V is limit specified.

(note2) Decoupling capacitor should be connected between V_{DD} and V_{SS} due to the stabilized operation for the circuit.

■ ELECTRICAL CHARACTERISTICS

NJU7014

(Ta=25°C, $V_{DD}=3.0V, R_L=\infty$)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input Offset Voltage	V_{IO}	$V_{IN}=1/2V_{DD}$	-	-	10	mV
Input Offset Current	I_{IO}		-	1	-	pA
Input Bias Current	I_{IB}		-	1	-	pA
Input Impedance	R_{IN}		-	1	-	TΩ
Large Signal Voltage Gain	A_{VD}		60	70	-	dB
Input Common Mode Voltage Range	V_{ICM}		0~2.5	-	-	V
Maximum Output Swing Voltage	V_{OM1}	$R_L=1M\Omega$	$V_{DD}-0.1$	-	-	V
	V_{OM2}	$R_L=1M\Omega$	-	-	$V_{SS}+0.1$	V
Common Mode Rejection Ratio	CMR	$V_{IN}=1/2V_{DD}$	55	65	-	dB
Supply Voltage Rejection Ratio	SVR	$V_{DD}=1.5\sim 5.5V$	60	70	-	dB
Operating Current	I_{DD}	Per Circuit	-	15	25	μA
Slew Rate	SR		-	0.1	-	V/ μs
Unity Gain Bandwidth	F_t	$A_V=40dB, C_L=10pF$	-	0.2	-	MHz

(note3) The source current is less than 2.9 μA (at $V_{OM}/R_L=2.9V/1M\Omega$).

NJU7015

(Ta=25°C, V_{DD}=3.0V, R_L=∞)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input Offset Voltage	V _{IO}	V _{IN} =1/2V _{DD}	-	-	10	mV
Input Offset Current	I _{IO}		-	1	-	pA
Input Bias Current	I _{IB}		-	1	-	pA
Input Impedance	R _{IN}		-	1	-	TΩ
Large Signal Voltage Gain	A _{VD}		60	70	-	dB
Input Common Mode Voltage Range	V _{ICM}		0~2.5	-	-	V
Maximum Output Swing Voltage	V _{OM1}	R _L =100kΩ	V _{DD} -0.1	-	-	V
	V _{OM2}	R _L =100kΩ	-	-	V _{SS} +0.1	V
Common Mode Rejection Ratio	CMR	V _{IN} =1/2V _{DD}	55	65	-	dB
Supply Voltage Rejection Ratio	SVR	V _{DD} =1.5~5.5V	60	70	-	dB
Operating Current	I _{DD}	Per Circuit	-	80	160	μA
Slew Rate	SR		-	1.0	-	V/μs
Unity Gain Bandwidth	F _t	A _v =40dB, C _L =10pF	-	1.0	-	MHz

(note4) The source current is less than 29μA (at V_{OM}/R_L=2.9V/100kΩ).

NJU7016

(Ta=25°C, V_{DD}=3.0V, R_L=∞)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input Offset Voltage	V _{IO}	V _{IN} =1/2V _{DD}	-	-	10	mV
Input Offset Current	I _{IO}		-	1	-	pA
Input Bias Current	I _{IB}		-	1	-	pA
Input Impedance	R _{IN}		-	1	-	TΩ
Large Signal Voltage Gain	A _{VD}		60	70	-	dB
Input Common Mode Voltage Range	V _{ICM}		0~2.5	-	-	V
Maximum Output Swing Voltage	V _{OM1}	R _L =50kΩ	V _{DD} -0.1	-	-	V
	V _{OM2}	R _L =50kΩ	-	-	V _{SS} +0.1	V
Common Mode Rejection Ratio	CMR	V _{IN} =1/2V _{DD}	55	65	-	dB
Supply Voltage Rejection Ratio	SVR	V _{DD} =1.5~5.5V	60	70	-	dB
Operating Current	I _{DD}	Per Circuit	-	200	400	μA
Slew Rate	SR		-	1.0	-	V/μs
Unity Gain Bandwidth	F _t	A _v =40dB, C _L =10pF	-	1.0	-	MHz

(note5) The source current is less than 58μA (at V_{OM}/R_L=2.9V/50kΩ).

■ TYPICAL CHARACTERISTICS

(1) NJU7014

Output Voltage vs. Output Current (SOURCE)



Output Voltage vs. Output Current (SINK)



Operating Current vs. Operating Voltage

V_{IN}=0.1V



Output Current vs. Operating Voltage

V_{IN}=0.1V



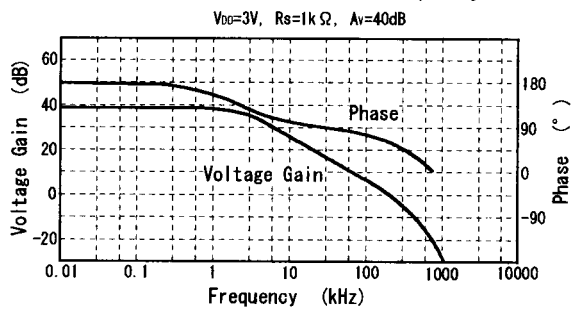
Maximum Output Swing Voltage vs. Load Resistance



Maximum Output Swing Voltage vs. Frequency

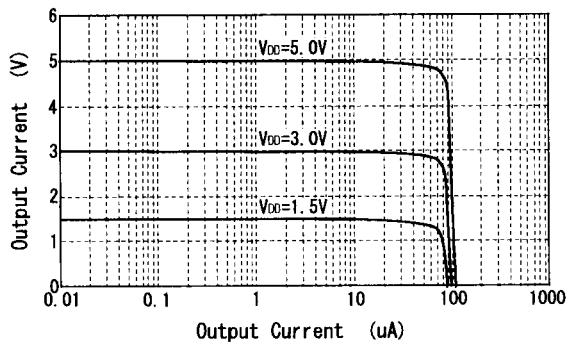


Voltage Gain-Phase vs. Frequency

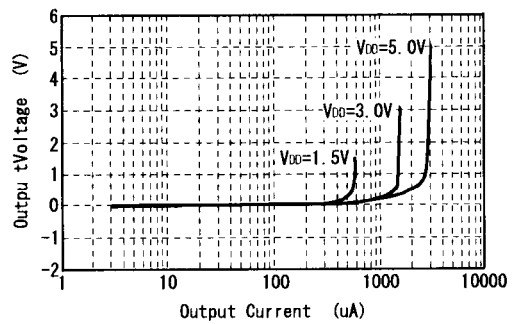


(2) NJU7015

Output Voltage vs. Output Current (SOURCE)

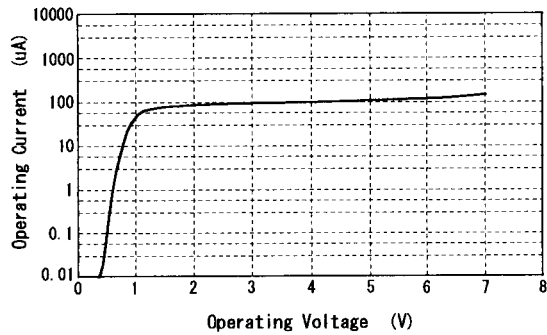


Output Voltage vs. Output Current (SINK)



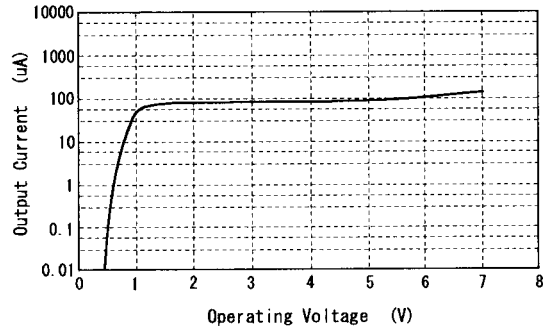
Operating Current vs. Operating Voltage

V_{IN}=0.1V



Output Current vs. Operating Voltage

V_{IN}=0.1V



Maximum Output Swing Voltage vs. Load Resistance



Maximum Output Swing Voltage vs. Frequency



Voltage Gain-Phase vs. Frequency

V_{DD}=3V, R_s=1kΩ, A_v=40dB



(3) NJU7016

Output Voltage vs. Output Current (SOURCE)

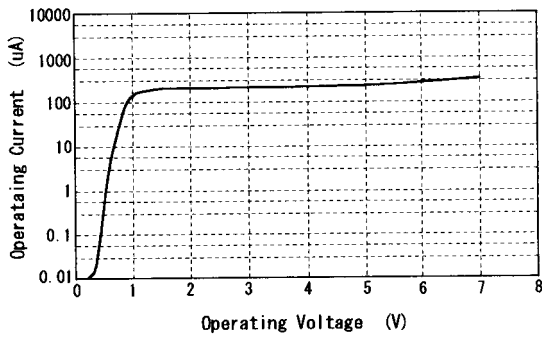


Output Voltage vs. Output Current (SINK)



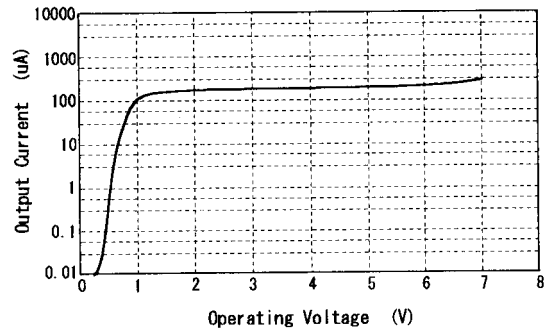
Operating Current vs. Operating Voltage

V_{IN} = 0.1V



Output Current vs. Operating Voltage

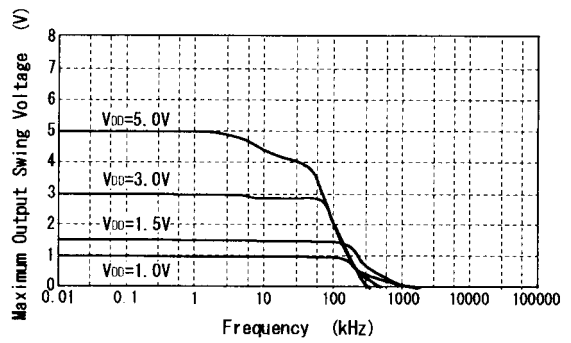
V_{IN} = 0.1V



Maximum Output Swing Voltage vs. Load Resistance



Maximum Output Swing Voltage vs. Frequency



Voltage Gain·Phase vs. Frequency



[CAUTION]

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- Техническая поддержка проекта;
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