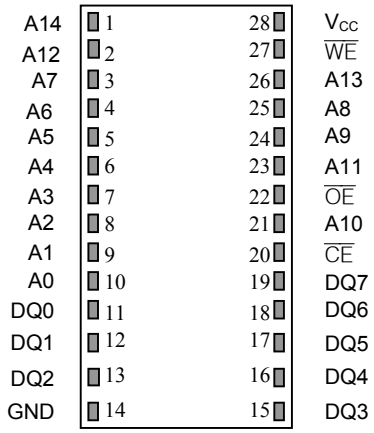
# DS1644/DS1644P
# Nonvolatile Timekeeping RAM

www.maxim-ic.com

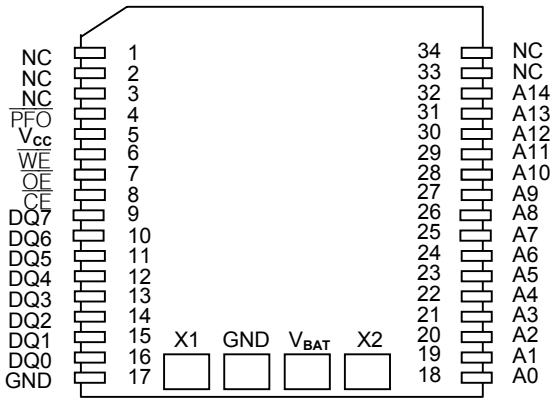
## FEATURES

- Integrated NV SRAM, Real-Time Clock, Crystal, Power-Fail Control Circuit and Lithium Energy Source
- Clock Registers are Accessed Identically to the Static RAM. These Registers are Resident in the Eight Top RAM Locations.
- Totally Nonvolatile with Over 10 Years of Operation in the Absence of Power
- BCD-Coded Year, Month, Date, Day, Hours, Minutes, and Seconds with Leap Year Compensation Valid Up to 2100
- Power-Fail Write Protection Allows for ±10% $V_{CC}$ Power Supply Tolerance
- DS1644 Only (DIP Module)
  - Upward Compatible with the DS1643 Timekeeping RAM to Achieve Higher RAM Density
  - Standard JEDEC Bytewide 32k x 8 Static RAM Pinout
- DS1644P Only (PowerCap® Module Board)
  - Surface Mountable Package for Direct Connection to PowerCap Containing Battery and crystal
  - Replaceable Battery (PowerCap)
  - Power-Fail Output
  - Pin-for-Pin Compatible with Other Densities of DS164XP Timekeeping RAM
  - Underwriters Laboratory (UL) Recognized

## PIN CONFIGURATIONS




28-Pin Encapsulated Package
(720-mil Extended)




34-Pin PowerCap Module Board
(Uses DS9034PCX PowerCap)

*PowerCap is a registered trademark of Dallas Semiconductor.*

## ORDERING INFORMATION

| PART | VOLTAGE RANGE (V) | TEMP RANGE | PIN-PACKAGE | TOP MARK |
|---|---|---|---|---|
| **DS1644**0120+ | 5.0 | 0°C to +70°C | 32 EDIP (0.740a) | DS1644+120 |
| DS16440-120 | 5.0 | 0°C to +70°C | 32 EDIP (0.740a) | DS1644-120 |
| **DS1644P**120+ | 5.0 | 0°C to +70°C | 34 PowerCap* | DS1644P+120 |
| DS1644P-120 | 5.0 | 0°C to +70°C | 34 PowerCap* | DS1644P-120 |

**DS9034-PCX, DS9034I-PCX, DS9034-PCX+ required (must be ordered separately).*

*A "+" indicates a lead-free product. The top mark will include a "+" symbol on lead-free devices.*

## PIN DESCRIPTION

| PIN | | NAME | FUNCTION |
|---|---|---|---|
| PDIP | PowerCap | | |
| 1 | 32 | A14 | Address Input |
| 2 | 30 | A12 | |
| 3 | 25 | A7 | |
| 4 | 24 | A6 | |
| 5 | 23 | A5 | |
| 6 | 22 | A4 | |
| 7 | 21 | A3 | |
| 8 | 20 | A2 | |
| 9 | 19 | A1 | |
| 10 | 18 | A0 | |
| 11 | 16 | DQ0 | Data Input/Output |
| 12 | 15 | DQ1 | |
| 13 | 14 | DQ2 | |
| 14 | 17 | GND | Ground |
| 15 | 13 | DQ3 | Data Input/Output |
| 16 | 12 | DQ4 | |
| 17 | 11 | DQ5 | |
| 18 | 10 | DQ6 | |
| 19 | 9 | DQ7 | |
| 20 | 8 | CE | Active Low Chip-Enable Input |
| 21 | 28 | A10 | Address Input |
| 22 | 7 | OE | Active Low Output-Enable Input |
| 23 | 29 | A11 | Address Input |
| 24 | 27 | A9 | |
| 25 | 26 | A8 | |
| 26 | 31 | A13 | |
| 27 | 6 | $\overline{WE}$ | Active-Low Write-Enable Input |
| 28 | 5 | $V_{CC}$ | Power-Supply Input |
| - | 4 | $\overline{RST}$ | Active-Low Reset Output, Open Drain. Requires a pullup resistor for proper operation. |
| - | 1-3,33,34 | NC | No Connection |
| - | | X1, X2, $V_{BAT}$ | Crystal Connection $V_{BAT}$ Battery Connection |

## DESCRIPTION

The DS1644 is a 32k x 8 nonvolatile static RAM with a full function real time clock, which are both accessible in a byte-wide format. The nonvolatile timekeeping RAM is functionally equivalent to any JEDEC standard 32k x 8 SRAM. The device can also be easily substituted for ROM, EPROM and EEPROM, providing read/write nonvolatility and the addition of the real time clock function. The real time clock information resides in the eight uppermost RAM locations. The RTC registers contain year, month, date, day, hours, minutes, and seconds data in 24-hour BCD format. Corrections for the day of the month and leap year are made automatically. The RTC clock registers are double-buffered to avoid access of incorrect data that can occur during clock update cycles. The double-buffered system also prevents time loss as the timekeeping countdown continues unabated by access to time register data. The DS1644 also contains its own power-fail circuitry, which deselects the device when the $V_{CC}$ supply is in an out-of-tolerance condition. This feature prevents loss of data from unpredictable system operation brought on by low $V_{CC}$ as errant access and update cycles are avoided.

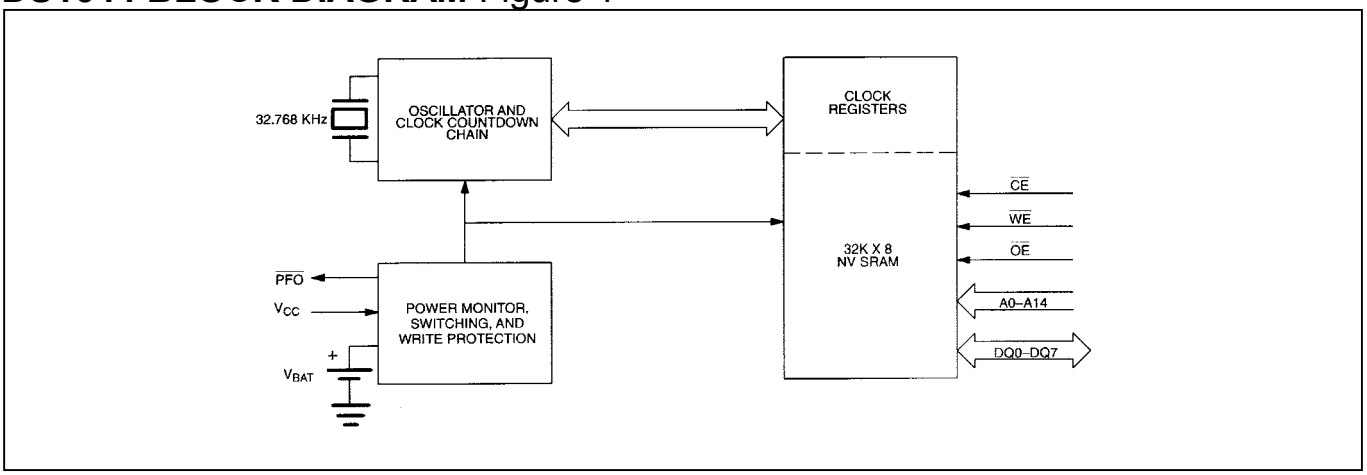
## PACKAGES

The DS1644 is available in two packages (28-pin DIP and 34-pin PowerCap module). The 28-pin DIP style module integrates the crystal, lithium energy source, and silicon all in one package. The 34-pin PowerCap Module Board is designed with contacts for connection to a separate PowerCap (DS9034PCX) that contains the crystal and battery. This design allows the PowerCap to be mounted on top of the DS1644P after the completion of the surface-mount process. Mounting the PowerCap after the surface mount process prevents damage to the crystal and battery due to the high temperatures required for solder reflow. The PowerCap is keyed to prevent reverse insertion. The PowerCap Module Board and PowerCap are ordered separately and shipped in separate containers. The part number for the PowerCap is DS9034PCX.

## CLOCK OPERATIONS—READING THE CLOCK

While the double-buffered register structure reduces the chance of reading incorrect data, internal updates to the DS1644 clock registers should be halted before clock data is read to prevent reading of data in transition. However, halting the internal clock register updating process does not affect clock accuracy. Updating is halted when a 1 is written into the read bit, the 7th most significant bit in the control register. As long as a 1 remains in that position, updating is halted. After a halt is issued, the registers reflect the count, that is day, date, and time that was present at the moment the halt command was issued. However, the internal clock registers of the double-buffered system continue to update so that the clock accuracy is not affected by the access of data. All of the DS1644 registers are updated simultaneously after the clock status is reset. Updating is within a second after the read bit is written to 0.

## DS1644 BLOCK DIAGRAM Figure 1




## DS1644 TRUTH TABLE Table 1

| $V_{CC}$ | $\overline{CE}$ | $\overline{OE}$ | $\overline{WE}$ | MODE | DQ | POWER |
|---|---|---|---|---|---|---|
| 5V ± 10% | $V_{IH}$ | X | X | DESELECT | HIGH-Z | STANDBY |
| | X | X | X | DESELECT | HIGH-Z | STANDBY |
| | $V_{IL}$ | X | $V_{IL}$ | WRITE | DATA IN | ACTIVE |
| | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | READ | DATA OUT | ACTIVE |
| | $V_{IL}$ | $V_{IH}$ | $V_{IH}$ | READ | HIGH-Z | ACTIVE |
| <4.5V >$V_{BAT}$ | X | X | X | DESELECT | HIGH-Z | CMOS STANDBY |
| <$V_{BAT}$ | X | X | X | DESELECT | HIGH-Z | DATA RETENTION MODE |

## SETTING THE CLOCK

The MSB Bit, (B7) of the control register is the write bit. Setting the write bit to a 1, like the read bit, halts updates to the DS1644 registers. The user can then load them with the correct day, date and time data in 24-hour BCD format. Resetting the write bit to a 0 then transfers those values to the actual clock counters and allows normal operation to resume.

## STOPPING AND STARTING THE CLOCK OSCILLATOR

The clock oscillator may be stopped at any time. To increase the shelf life, the oscillator can be turned off to minimize current drain from the battery. The $\overline{OSC}$ bit is the MSB for the seconds registers. Setting it to a 1 stops the oscillator.

## FREQUENCY TEST BIT

Bit 6 of the day byte is the frequency test bit. When the frequency test bit is set to logic 1 and the oscillator is running, the LSB of the seconds register will toggle at 512 Hz. When the seconds register is being read, the DQ0 line will toggle at the 512 Hz frequency as long as conditions for access remain valid (i.e., $\overline{CE}$ low, $\overline{OE}$ low, and address for seconds register remain valid and stable).

## CLOCK ACCURACY (DIP MODULE)

The DS1644 is guaranteed to keep time accuracy to within ±1 minute per month at 25°C. The RTC is calibrated at the factory by Dallas Semiconductor using nonvolatile tuning elements, and does not require additional calibration. For this reason, methods of field clock calibration are not available and not necessary. Clock accuracy is also affected by the electrical environment and caution should be taken to place the RTC in the lowest level EMI section of the PCB layout. For additional information please see application note 58.

## CLOCK ACCURACY (POWERCAP MODULE)

The DS1644 and DS9034PCX are each individually tested for accuracy. Once mounted together, the module will typically keep time accuracy to within ±1.53 minutes per month (35 ppm) at 25°C. Clock accuracy is also affected by the electrical environment and caution should be taken to place the RTC in the lowest level EMI section of the PCB layout. For additional information please see application note 58.

## DS1644 REGISTER MAP—BANK1 Table 2

| ADDRESS | DATA | | | | | | | | FUNCTION | |
|---|---|---|---|---|---|---|---|---|---|---|
| | $B_7$ | $B_6$ | $B_5$ | $B_4$ | $B_3$ | $B_2$ | $B_1$ | $B_0$ | | |
| 7FFF | — | — | — | — | — | — | — | — | Year | 00-99 |
| 7FFE | X | X | X | — | — | — | — | — | Month | 01-12 |
| 7FFD | X | X | - | — | — | — | — | — | Date | 01-31 |
| 7FFC | X | FT | X | X | X | — | — | — | Day | 01-07 |
| 7FFB | X | X | — | — | — | — | — | — | Hour | 00-23 |
| 7FFA | X | — | — | — | — | — | — | — | Minutes | 00-59 |
| 7FF9 | $\overline{OSC}$ | — | — | — | — | — | — | — | Seconds | 00-59 |
| 7FF8 | W | R | X | X | X | X | X | X | Control | A |

$\overline{OSC}$ = STOP BIT R = READ BIT FT = FREQUENCY TEST
W = WRITE BIT X = UNUSED

***Note:*** *All indicated "X" bits are unused but must be set to "0" during write cycles to ensure proper clock operation.*

## RETRIEVING DATA FROM RAM OR CLOCK

The DS1644 is in the read mode whenever $\overline{WE}$ (write enable) is high, and $\overline{CE}$ (chip enable) is low. The device architecture allows ripple-through access to any of the address locations in the NV SRAM. Valid data will be available at the DQ pins within $t_{AA}$ after the last address input is stable, providing that the $\overline{CE}$ and $\overline{OE}$ access times and states are satisfied. If $\overline{CE}$ or $\overline{OE}$ access times are not met, valid data will be available at the latter of chip enable access ($t_{CEA}$) or at output enable access time ($t_{OEA}$). The state of the data input/output pins (DQ) is controlled by $\overline{CE}$ and $\overline{OE}$. If the outputs are activated before $t_{AA}$, the data lines are driven to an intermediate state until $t_{AA}$. If the address inputs are changed while $\overline{CE}$ and $\overline{OE}$ remain valid, output data will remain valid for output data hold time ($t_{OH}$) but will then go indeterminate until the next address access.

## WRITING DATA TO RAM OR CLOCK

The DS1644 is in the write mode whenever $\overline{WE}$ and $\overline{CE}$ are in their active state. The start of a write is referenced to the latter occurring high to low transition of $\overline{WE}$ or $\overline{CE}$. The addresses must be held valid throughout the cycle. $\overline{CE}$ or $\overline{WE}$ must return inactive for a minimum of $t_{WR}$ prior to the initiation of another read or write cycle. Data in must be valid $t_{DS}$ prior to the end of write and remain valid for $t_{DH}$ afterward. In a typical application, the $\overline{OE}$ signal will be high during a write cycle. However, $\overline{OE}$ can be active provided that care is taken with the data bus to avoid bus contention. If $\overline{OE}$ is low prior to $\overline{WE}$ transitioning low the data bus can become active with read data defined by the address inputs. A low transition on $\overline{WE}$ will then disable the outputs $t_{WEZ}$ after $\overline{WE}$ goes active.

## DATA RETENTION MODE

When $V_{CC}$ is within nominal limits ($V_{CC}$ > 4.5 volts) the DS1644 can be accessed as described above with read or write cycles. However, when $V_{CC}$ is below the power-fail point $V_{PF}$ (point at which write protection occurs) the internal clock registers and RAM are blocked from access. This is accomplished internally by inhibiting access via the $\overline{CE}$ signal. At this time the power-fail output signal ($\overline{PFO}$) will be driven active low and will remain active until $V_{CC}$ returns to nominal levels. When $V_{CC}$ falls below the level of the internal battery supply, power input is switched from the $V_{CC}$ pin to the internal battery and clock activity, RAM, and clock data are maintained from the battery until $V_{CC}$ is returned to nominal level.

## ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Pin Relative to Ground……..-0.3V to +7.0V
Storage Temperature……...-40°C to +85°C, Noncondensing
Soldering Temperature……..…+260°C for 10 seconds (DIP Package) (See Note 7)
See IPC/JEDEC Standard J-STD-020A for Surface-Mount Devices

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.*

## OPERATING RANGE

| RANGE | TEMPERATURE | $V_{CC}$ |
|---|---|---|
| Commercial | 0°C to +70°C, Noncondensing | 5V ±10% |

## RECOMMENDED DC OPERATING CONDITIONS (Over the Operating Range)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 4.5 | | 5.5 | V | 1 |
| Logic 1 Voltage All Inputs | $V_{IH}$ | 2.2 | | $V_{CC}$+0.3 | V | |
| Logic 0 Voltage All Inputs | $V_{IL}$ | -0.3 | | 0.8 | V | |

## DC ELECTRICAL CHARACTERISTICS (Over the Operating Range)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Average $V_{CC}$ Power Supply Current | $I_{CC1}$ | | | 75 | mA | 3 |
| TTL Standby Current ($\overline{CE}$ =$V_{IH}$) | $I_{CC2}$ | | | 6 | mA | 3 |
| CMOS Standby Current ($\overline{CE}$ =$V_{CC}$-0.2V) | $I_{CC3}$ | | | 4.0 | mA | 3 |
| Input Leakage Current (any input) | $I_{IL}$ | -1 | | +1 | µA | |
| Output Leakage Current | $I_{OL}$ | -1 | | +1 | µA | |
| Output Logic 1 Voltage ($I_{OUT}$ = -1.0 mA) | $V_{OH}$ | 2.4 | | | V | |
| Output Logic 0 Voltage ($I_{OUT}$ = +2.1 mA) | $V_{OL}$ | | | 0.4 | V | |
| Power-Fail Voltage | $V_{PF}$ | 4.0 | | 4.5 | V | |

## AC ELECTRICAL CHARACTERISTICS (Over the Operating Range)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Read Cycle Time | $t_{RC}$ | 120 | | | ns | |
| Address Access Time | $t_{AA}$ | | | 120 | ns | |
| $\overline{CE}$ Access Time | $t_{CEA}$ | | | 120 | ns | |
| $\overline{CE}$ Data Off Time | $t_{CEZ}$ | | | 40 | ns | |
| Output Enable Access Time | $t_{OEA}$ | | | 100 | ns | |
| Output Enable Data Off Time | $t_{OEZ}$ | | | 40 | ns | |
| Output Enable to DQ Low-Z | $t_{OEL}$ | 5 | | | ns | |
| $\overline{CE}$ to DQ Low-Z | $t_{CEL}$ | 5 | | | ns | |
| Output Hold from Address | $t_{OH}$ | 5 | | | ns | |
| Write Cycle Time | $t_{WC}$ | 120 | | | ns | |
| Address Setup Time | $t_{AS}$ | 0 | | | ns | |
| $\overline{CE}$ Pulse Width | $t_{CEW}$ | 100 | | | ns | |
| Address Hold from End of Write | $t_{AH1}$ | 5 | | | ns | 5 |
| | $t_{AH2}$ | 30 | | | ns | 6 |
| Write Pulse Width | $t_{WEW}$ | 75 | | | ns | |
| $\overline{WE}$ Data Off Time | $t_{WEZ}$ | | | 40 | ns | |
| $\overline{WE}$ or $\overline{CE}$ Inactive Time | $t_{WR}$ | 10 | | | ns | |
| Data Setup Time | $t_{DS}$ | 85 | | | ns | |
| Data Hold Time High | $t_{DH1}$ | 0 | | | ns | 5 |
| | $t_{DH2}$ | 15 | | | ns | 6 |

## AC TEST CONDITIONS

Input Levels: 0V to 3V
Transition Times: 5 ns

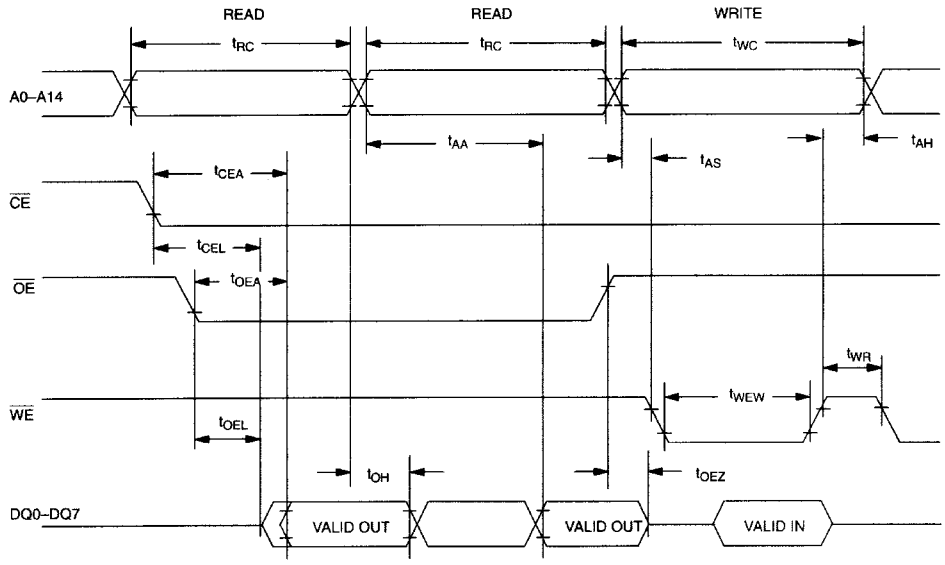
## CAPACITANCE ($T_A$ = +25°C)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Capacitance on all pins (except DQ) | $C_I$ | | | 7 | pF | |
| Capacitance on DQ pins | $C_{DQ}$ | | | 10 | pF | |

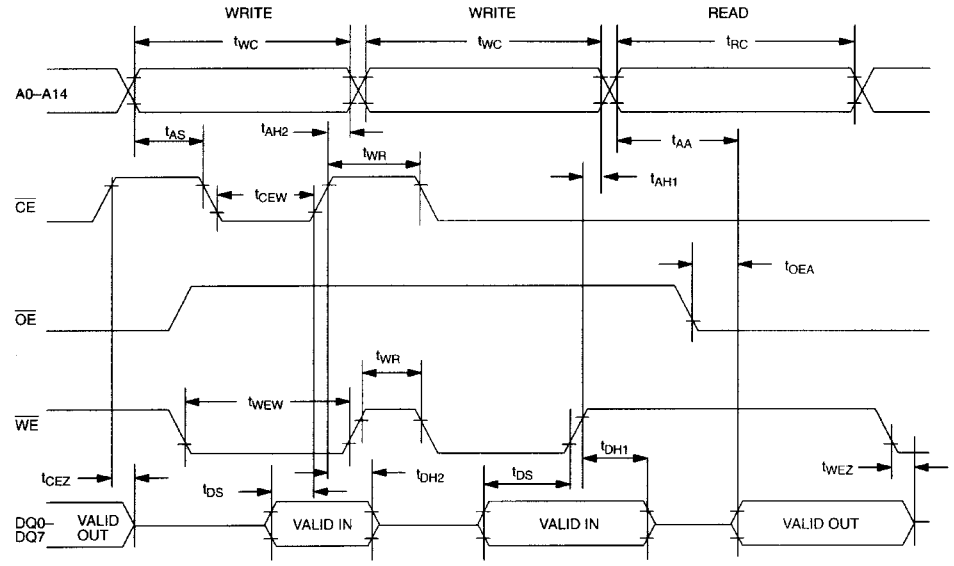
## AC ELECTRICAL CHARACTERISTICS (POWER-UP/DOWN TIMING) (Over the Operating Range)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| $\overline{CE}$ or $\overline{WE}$ at $V_{IH}$ before Power Down | $t_{PD}$ | 0 | | | µs | |
| $V_{PF}$ (Max) to $V_{PF}$ (Min) $V_{CC}$ Fall Time | $t_F$ | 300 | | | µs | |
| $V_{PF}$ (Min) to $V_{SO}$ $V_{CC}$ Fall Time | $t_{FB}$ | 10 | | | µs | |
| $V_{SO}$ to $V_{PF}$ (Min) $V_{CC}$ Rise Time | $t_{RB}$ | 1 | | | µs | |
| $V_{PF}$ (Min) to $V_{PF}$ (Max) $V_{CC}$ Rise Time | $t_R$ | 0 | | | µs | |
| Power-Up | $t_{REC}$ | 15 | | 35 | ms | |
| Expected Data Retention Time (Oscillator On) | $t_{DR}$ | 10 | | | years | 4 |

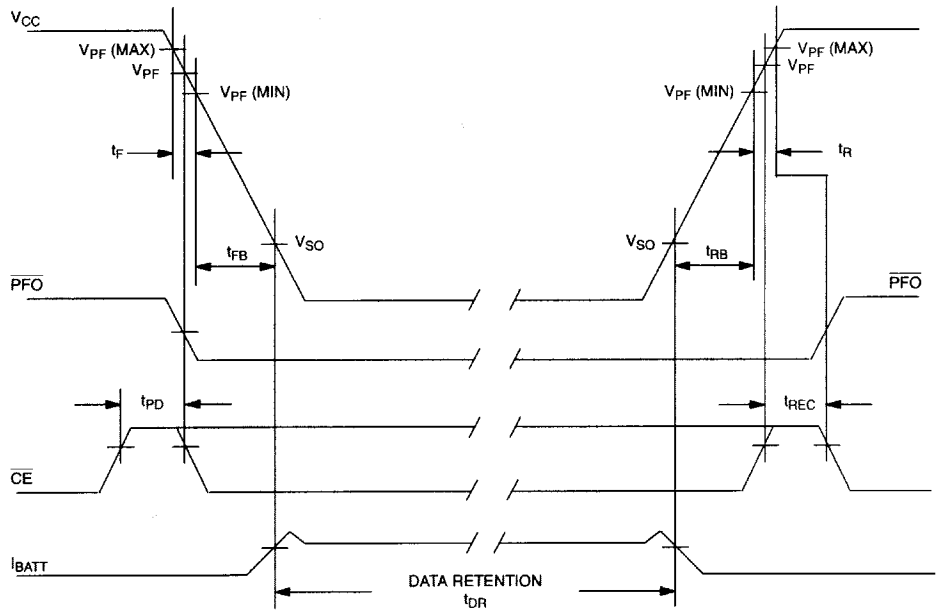
## DS1644 READ CYCLE TIMING



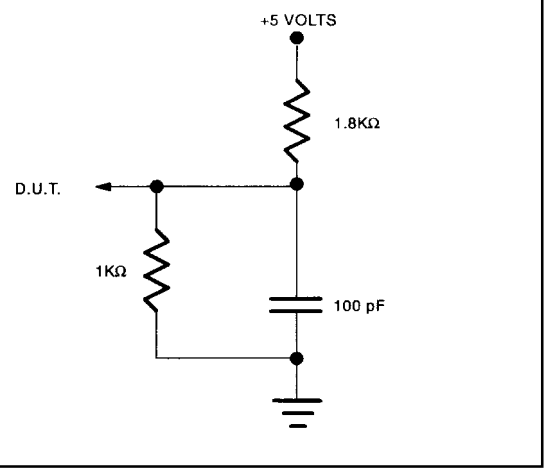

## DS1644 WRITE CYCLE TIMING



## POWER-DOWN/POWER-UP TIMING




## OUTPUT LOAD



## NOTES:

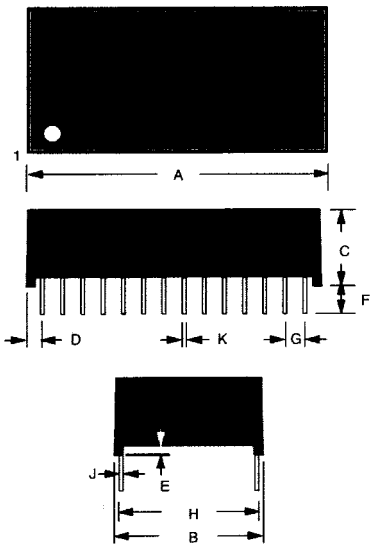
1. All voltages are referenced to ground.
2. Typical values are at 25°C and nominal supplies.
3. Outputs are open.
4. Data retention time is at 25°C and is calculated from the date code on the device package. The date code XXYY is the year followed by the week of the year in which the device was manufactured. For example, 9225 would mean the 25th week of 1992.
5. $t_{AH1}$, $t_{DH1}$ are measured from $\overline{WE}$ going high.
6. $t_{AH2}$, $t_{DH2}$ are measured from $\overline{CE}$ going high.
7. Real-Time Clock Modules (DIP) can be successfully processed through conventional wave-soldering techniques as long as temperatures as long as temperature exposure to the lithium energy source contained within does not exceed +85°C. Post solder cleaning with water washing techniques is acceptable, provided that ultrasonic vibration is not used.

   In addition, for the PowerCap version:
   a. Dallas Semiconductor recommends that PowerCap Module bases experience one pass through solder reflow oriented with the label side up (“live - bug”).
   b. Hand soldering and touch-up: Do not touch or apply the soldering iron to leads for more than 3 (three) seconds. To solder, apply flux to the pad, heat the lead frame pad and apply solder. To remove the part, apply flux, heat the lead frame pad until the solder reflows and use a solder wick to remove solder.

# PACKAGE INFORMATION

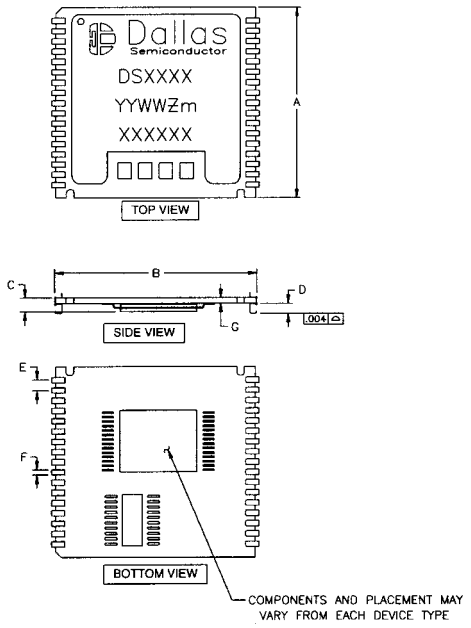
(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/DallasPackInfo**.)

## DS1644 28-PIN PACKAGE




| PKG | 28-PIN | |
|---|---|---|
| DIM | MIN | MAX |
| A IN. | 1.470 | 1.490 |
| MM | 37.34 | 37.85 |
| B IN. | 0.715 | 0.740 |
| MM | 18.16 | 18.80 |
| C IN. | 0.335 | 0.365 |
| MM | 8.51 | 9.27 |
| D IN. | 0.075 | 0.105 |
| MM | 1.91 | 2.67 |
| E IN. | 0.015 | 0.030 |
| MM | 0.38 | 0.76 |
| F IN. | 0.140 | 0.180 |
| MM | 3.56 | 4.57 |
| G IN. | 0.090 | 0.110 |
| MM | 2.29 | 2.79 |
| H IN. | 0.590 | 0.630 |
| MM | 14.99 | 16.00 |
| J IN. | 0.010 | 0.018 |
| MM | 0.25 | 0.45 |
| K IN. | 0.015 | 0.025 |
| MM | 0.38 | 0.64 |

## DS1644P



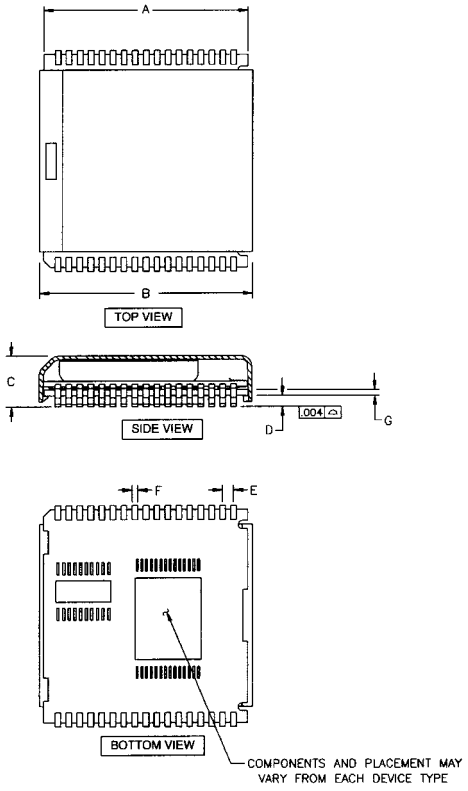

| PKG | INCHES | | |
|---|---|---|---|
| DIM | MIN | NOM | MAX |
| A | 0.920 | 0.925 | 0.930 |
| B | 0.980 | 0.985 | 0.990 |
| C | - | - | 0.080 |
| D | 0.052 | 0.055 | 0.058 |
| E | 0.048 | 0.050 | 0.052 |
| F | 0.015 | 0.020 | 0.025 |
| G | 0.025 | 0.027 | 0.030 |

**NOTE FOR THE PowerCap VERSION:**

a. DALLAS SEMICONDUCTOR RECOMMENDS THAT PowerCap MODULE BASES EXPERIENCE ONE PASS THROUGH SOLDER REFLOW ORIENTED WITH THE LABEL SIDE UP ("LIVE - BUG").

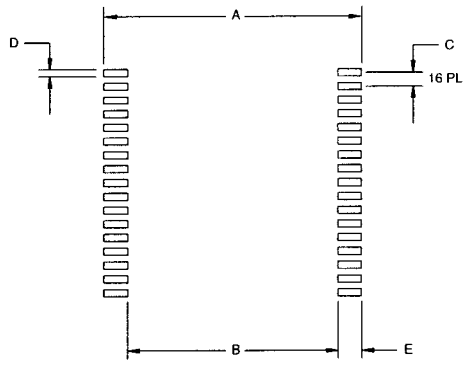
b. HAND SOLDERING AND TOUCH-UP: DO NOT TOUCH OR APPLY THE SOLDERING IRON TO LEADS FOR MORE THAN 3 SECONDS. TO SOLDER, APPLY FLUX TO THE PAD, HEAT THE LEAD FRAME PAD AND APPLY SOLDER. TO REMOVE THE PART, APPLY FLUX, HEAT THE LEAD FRAME PAD UNTIL THE SOLDER REFLOWS AND USE A SOLDER WICK TO REMOVE SOLDER.

## DS1644P WITH DS9034PCX ATTACHED




| PKG | INCHES | | |
|---|---|---|---|
| DIM | MIN | NOM | MAX |
| A | 0.920 | 0.925 | 0.930 |
| B | 0.955 | 0.960 | 0.965 |
| C | 0.240 | 0.245 | 0.250 |
| D | 0.052 | 0.055 | 0.058 |
| E | 0.048 | 0.050 | 0.052 |
| F | 0.015 | 0.020 | 0.025 |
| G | 0.020 | 0.025 | 0.030 |

## RECOMMENDED POWERCAP MODULE LAND PATTERN




| PKG | INCHES | | |
|---|---|---|---|
| DIM | MIN | NOM | MAX |
| A | - | 1.050 | - |
| B | - | 0.826 | - |
| C | - | 0.050 | - |
| D | - | 0.030 | - |
| E | - | 0.112 | - |



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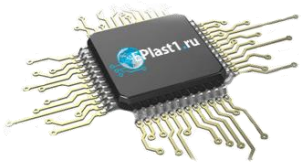
Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов;
- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits,General Dynamics и др.);

Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.




**Как с нами связаться**

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