
IEEE 802.11 b/g/n SmartConnect Wi-Fi Module

PRELIMINARY DATASHEET

Description

The Atmel® | SMART SAMW25 module is based on the industry-leading low-power 2.4GHz IEEE® 802.11 b/g/n Wi-Fi ATWINC1500 SoC (System on Chip) combined with the ARM® Cortex®-M0+ based microcontroller technology from Atmel.

This turnkey system provides an integrated software solution with application and security protocols such as TLS, integrated network services (TCP/IP stack) which are all available through Atmel Studio 6 integrated development environment (IDE). The Atmel SmartConnect modules offer the ideal solutions for designers seeking to add Wi-Fi connectivity with minimal previous experience in 802.11, IP Stack or RF. Atmel SmartConnect Wi-Fi from Atmel opens the door of the Internet of Things (IoT) to the vast array of battery-powered devices and applications requiring the integration of WLAN connectivity without compromising on cost or power consumption. While we compete with other Wi-Fi modules on size, RF performance, cost and other characteristics, our Atmel SmartConnect product family has a distinctive advantage when it comes to power consumption and power saving modes. The ATSAMW25 device is a standalone end point, where a complete small application can be executed on the module by itself.

Features

Key features with SAMW25 Wireless connectivity solution:

- Certified Wi-Fi ATWINC1500A-MU-T with SAMD21 application
- IEEE 802.11 b/g/n 20MHz (1x1) solution
- Single spatial stream in 2.4GHz ISM band
- Compact footprint: 33.863 x 14.882mm
- Radio:
 - Output power - 802.11b /11Mbps: 17dBm ±1dB
 - 802.11g /54Mbps: 15dBm ±1dB @ EVM -28dB
 - 802.11n /65Mbps: 13dBm ±1dB @ EVM -30dB
- Application processor:
 - Atmel SAMD21 ARM Cortex M0+ based microcontroller
 - 256KB embedded Flash and 32KB SRAM
 - Full-Speed USB Device and embedded Host

- CryptoAuthentication™ ATECC508 (optional) I/O operating voltage: 2.7 to 3.6V
- Power Amplifier and On-board Switching Regulator operating voltage: 2.7 to 4.6V
- Power states supported:
 - Provision (AP/ Sniffer) IDLE LISTEN
 - IDLE
 - SUSPEND
- Extreme low power, on-chip low power sleep oscillator
- Serial Host Interface SPI or UART
- Software Upgrade Over-the-Air (OTA)
- FCC, CE, IC, and TELEC Certified; RoHS compliant
- Security protocols; WPA/WPA2 Personal, TLS, SSL
- Network services; DHCP, DNS, TCP/IP (IPv4), UDP, HTTP, HTTPS

Target Applications

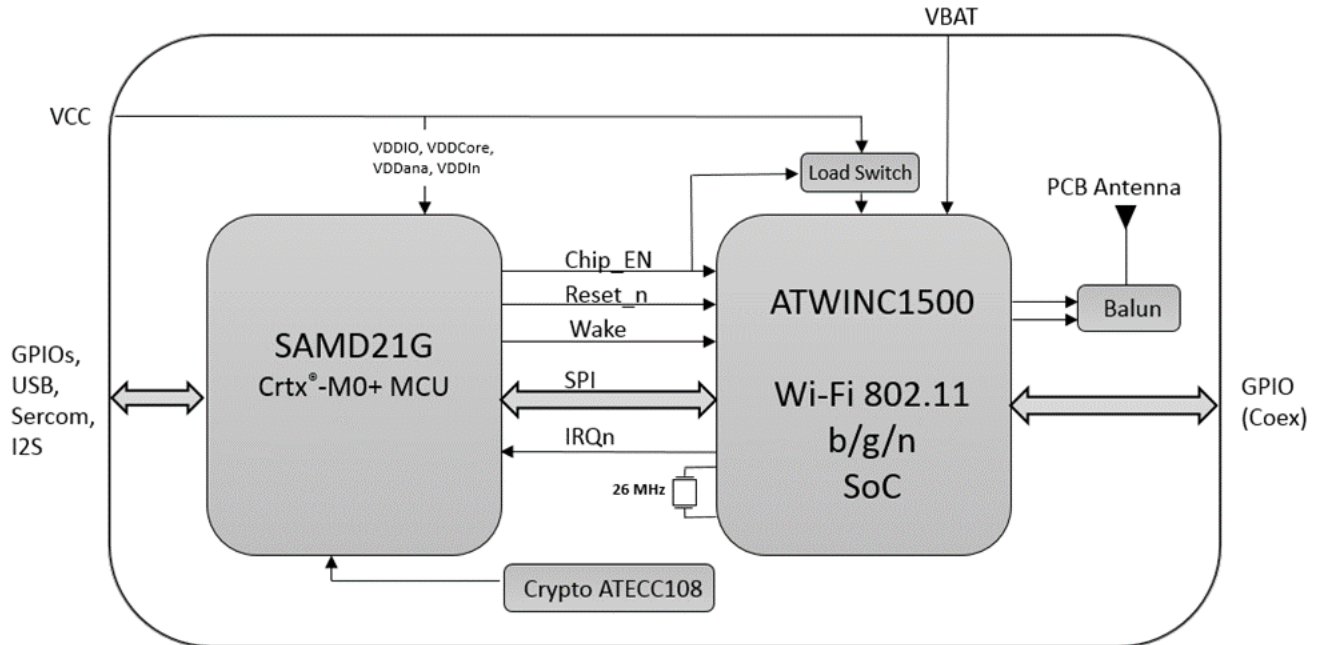
- IoT applications
- Smart appliances
- Multimedia streaming
- Safety and security
- Home automation
- Consumer electronics
- Industrial automation

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1 Block Diagram

Figure 1-1. ATSAMW25 Block Diagram



2 Ordering Information and IC Marking

Table 2-1. Ordering Details

| Atmel Ordering Code | Package |
|---------------------|---|
| ATSAMW25-MR210PA | WINC1500 + SAMD21 module. Tray Packing |
| ATSAMW25-MR510PA | WINC1500+SAMD21+ATECC508 module. Tray Packing |
| ATSAMW25-XPRO | Xplained board evaluation kit |

3 Pinout and Package Information

3.1 Pin Description

Figure 3-1. Pin Assignment

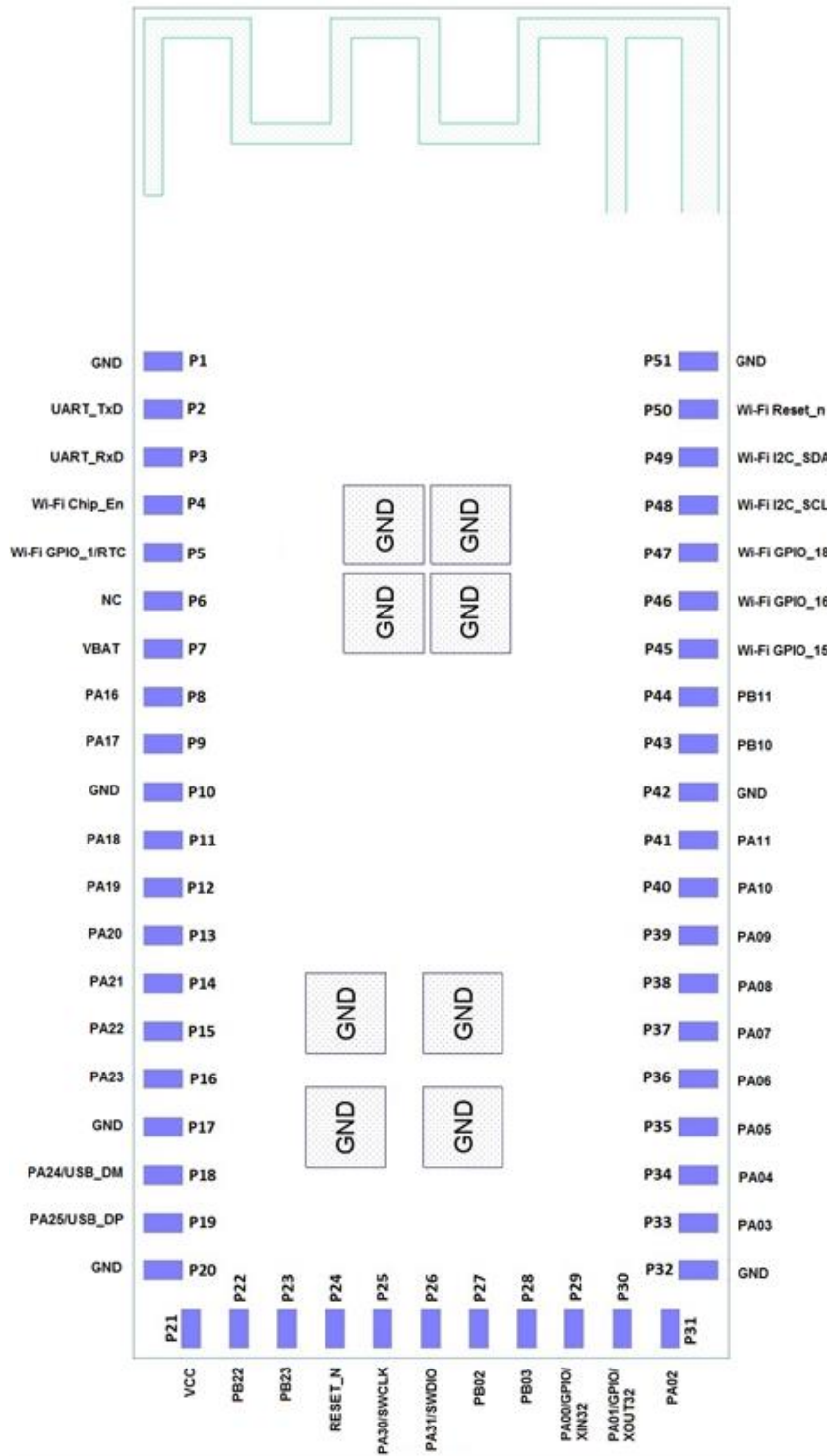


Table 3-1. Pin Description

| Pin # | Pin Description | I/O Type | Function (default) | Programmable Pullup/-down Resistor |
|-------|------------------|--|--|------------------------------------|
| 1 | GND | N/A | Common Ground | |
| 2 | UART_TxD | WINC1500 Output | Currently used only for Atmel debug. Not for customer use. Leave unconnected. | Yes – Pullup |
| 3 | UART_RxD | WINC1500 Input | Currently used only for Atmel debug. Not for customer use. Leave unconnected. | Yes – Pullup |
| 4 | Wi-Fi Chip_En | WINC1500 Input | Currently used only for Atmel debug. Not for customer use. Leave unconnected. | No |
| 5 | Wi-Fi GPIO_1/RTC | WINC1500 I/O | ATWINC1500 General purpose I/O. Can also be used to input a 32.768KHz Real Time Clock for accurate timing of Wi-Fi sleep intervals | Yes – Pullup |
| 6 | NC | - | No connect | |
| 7 | VBAT | Power | Supply for Wi-Fi RF Power Amplifier and Internal 1.3V Switching Regulator | |
| 8 | PA16 | See SAM D21G datasheet | See SAM D21G datasheet | Yes |
| 9 | PA17 | See SAM D21G datasheet | See SAM D21G datasheet | Yes |
| 10 | GND | Power | Ground | |
| 11 | PA18 | See SAM D21G datasheet | See SAM D21G datasheet | Yes |
| 12 | PA19 | See SAM D21G datasheet | See SAM D21G datasheet | Yes |
| 13 | PA20 | See SAM D21G datasheet | See SAM D21G datasheet | Yes |
| 14 | PA21 | See SAM D21G datasheet | See SAM D21G datasheet | Yes |
| 15 | PA22 | See SAM D21G datasheet | See SAM D21G datasheet | Yes |
| 16 | PA23 | See SAM D21G datasheet | See SAM D21G datasheet | Yes |
| 17 | GND | Power | Ground | |
| 18 | PA24/USB_DM | See SAM D21G datasheet | Host Interface USB Data minus pin | Yes |
| 19 | PA25/USB_DP | See SAM D21G datasheet | Host Interface USB Data Plus pin | Yes |
| 20 | GND | Power | Ground | |
| 21 | VCC | Power | Power supply for I/O | |
| 22 | PB22 | See SAM D21G datasheet | See SAM D21G datasheet | Yes |
| 23 | PB23 | See SAM D21G datasheet | See SAM D21G datasheet | Yes |
| 24 | RESET_N | Input see SAM D21G datasheet | System Reset. Low level on this pin resets the entire module. | Yes |
| 25 | PA30/SWCLK | See SAM D21G datasheet | Cortex Serial Wire Debug Interface CLK | Yes |

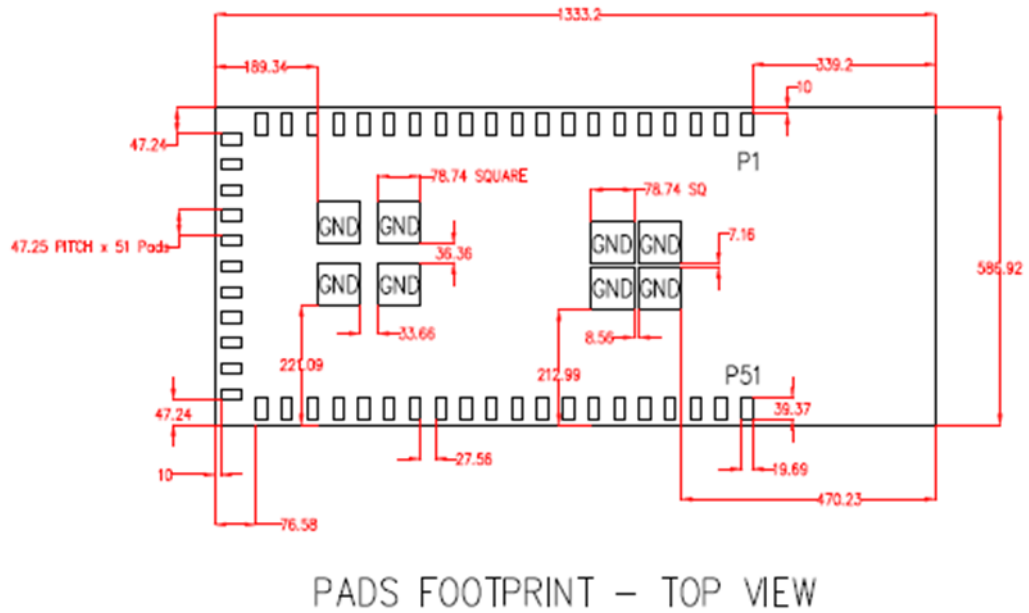
| Pin # | Pin Description | I/O Type | Function (default) | Programmable Pullup/-down Resistor |
|-------|------------------|--|---|------------------------------------|
| 26 | PA31/SWDIO | See SAM D21G datasheet | Cortex Serial Wire Debug Interface Data I/O | Yes |
| 27 | PB02 | See SAM D21G datasheet | See SAM D21G datasheet | Yes |
| 28 | PB03 | See SAM D21G datasheet | See SAM D21G datasheet | Yes |
| 29 | PA00/GPIO/XIN32 | See SAM D21G datasheet | See SAM D21G datasheet | Yes |
| 30 | PA01/GPIO/XOUT32 | See SAM D21G datasheet | See SAM D21G datasheet | Yes |
| 31 | PA02 | I/O | See SAM D21G datasheet | Yes |
| 32 | GND | Power | Ground | Yes |
| 33 | PA03 | See SAM D21G datasheet | See SAM D21G datasheet | Yes |
| 34 | PA04 | See SAM D21G datasheet | See SAM D21G datasheet | Yes |
| 35 | PA05 | See SAM D21G datasheet | See SAM D21G datasheet | Yes |
| 36 | PA06 | See SAM D21G datasheet | See SAM D21G datasheet | Yes |
| 37 | PA07 | See SAM D21G datasheet | See SAM D21G datasheet | Yes |
| 38 | PA08 | See SAM D21G datasheet | See SAM D21G datasheet | Yes |
| 39 | PA09 | See SAM D21G datasheet | See SAM D21G datasheet | Yes |
| 40 | PA10 | See SAM D21G datasheet | See SAM D21G datasheet | Yes |
| 41 | PA11 | See SAM D21G datasheet | See SAM D21G datasheet | Yes |
| 42 | GND | Power | Ground | |
| 43 | PB10 | See SAM D21G datasheet | See SAM D21G datasheet | Yes |
| 44 | PB11 | See SAM D21G datasheet | See SAM D21G datasheet | Yes |
| 45 | Wi-Fi GPIO_15 | WINC1500 I/O | ATWINC1500 General purpose I/O. Pin must not be driven or pulled high when the ATWINC1500 is in Suspend Mode. | Yes – Pullup |
| 46 | Wi-Fi GPIO_16 | WINC1500 I/O | ATWINC1500 General purpose I/O. Pin must not be driven or pulled high when the ATWINC1500 is in Suspend Mode. | Yes – Pullup |
| 47 | Wi-Fi GPIO_18 | WINC1500 I/O | ATWINC1500 General purpose I/O. Pin must not be driven or pulled high when the ATWINC1500 is in Suspend Mode. | Yes – Pullup |
| 48 | Wi-Fi I2C_SCL | WINC1500 I/O | Currently used only for Atmel debug. Not for customer use. Leave unconnected. | Yes – Pullup |
| 49 | Wi-Fi I2C_SDA | WINC1500 I/O | Currently used only for Atmel debug. Not for customer use. Leave unconnected. | Yes – Pullup |

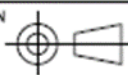
| Pin # | Pin Description | I/O Type | Function (default) | Programmable Pullup/-down Resistor |
|-------|-----------------|----------------|---|------------------------------------|
| 50 | Wi-Fi Reset_n | WINC1500 Input | Currently used only for Atmel debug. Not for customer use. Leave unconnected. | No |
| 51 | GND | Power | Ground | |

3.2 Package Description

The ATSAMW25-MR210PA package information.

Figure 3-2. SAMW25 MR210PA Package



| | | | | | |
|---|-------------------------|----------------------|---|--------|---------------|
| SCALE: 1:1 or AS NOTED | DATE: 10/17/14 | DRAWN: V. IRLANDA | TITLE: ATMEL CORP (LAKE FOREST) SAMW25-MR210PA PACKAGE OUTLINE DRAWING | | |
| DIMENSIONAL UNIT: MILS | UNTOLERANCED DIMENSIONS | ENGINEER: V. IRLANDA | | | |
| PROJECTION UNLESS SPECIFIED | ±3 MILS | CHECKED: V. IRLANDA | | | |
|  | ANGLE ±1° | APPROVED: | | | |
| | | CAD NAME: | DRAWING NUMBER: | REV. 1 | SHEET: 1 OF 1 |

4 Electrical Specifications

4.1 Absolute Ratings

All typical values are measured at $T = 25^{\circ}\text{C}$ unless otherwise specified. All minimum and maximum values are valid across operating temperature and voltage unless otherwise specified.

Table 4-1. Absolute Maximum Ratings

| Parameters | Minimum | Maximum | Unit |
|---|---------|---------|--------------------|
| VBAT power supply voltage | 0 | 5.0 | V |
| VCC power supply voltage | 0 | 3.63 | |
| Pin voltage with respect to GND and VCC | GND-0.3 | VCC+0.3 | |
| Storage temperature range | -40 | +125 | $^{\circ}\text{C}$ |

Table 4-2. General Operating Ratings

| Parameters | Minimum | Typical | Maximum | Unit |
|-----------------------------|---------|---------|---------|--------------------|
| VBATT | 2.7 | 3.30 | 4.2 | $^{\circ}\text{C}$ |
| VCC | 1.62 | 3.30 | 3.6 | |
| Operating temperature range | -40 | 25 | 85 | |

Table 4-3. Physical Characteristics

| Parameters | Value | Comments |
|----------------------|----------------------|----------|
| Size | 33.863 x 14.882mm | - |
| Connector pins pitch | see module footprint | - |

Table 4-4. I/O Pins Characteristics

| VDDIO Condition | Characteristic | Minimum | Typical | Maximum | Unit |
|--------------------|------------------------------|------------|---------|----------------------------|------|
| VDDIO _L | Input Low Voltage V_{IL} | -0.30 | | 0.60 | V |
| | Input High Voltage V_{IH} | VDDIO-0.60 | | VDDIO+0.30 | |
| | Output Low Voltage V_{OL} | | | 0.45 | |
| | Output High Voltage V_{OH} | VDDIO-0.50 | | | |
| VDDIO _M | Input Low Voltage V_{IL} | -0.30 | | 0.63 | |
| | Input High Voltage V_{IH} | VDDIO-0.60 | | VDDIO+0.30 | |
| | Output Low Voltage V_{OL} | | | 0.45 | |
| | Output High Voltage V_{OH} | VDDIO-0.50 | | | |
| VDDIO _H | Input Low Voltage V_{IL} | -0.30 | | 0.65 | |
| | Input High Voltage V_{IH} | VDDIO-0.60 | | VDDIO+0.30 (up to 3.60) | |

| VDDIO Condition | Characteristic | Minimum | Typical | Maximum | Unit |
|------------------|------------------------------|------------|---------|---------|------|
| | Output Low Voltage V_{OL} | | | 0.45 | V |
| | Output High Voltage V_{OH} | VDDIO-0.50 | | | |
| All | Output Loading | | | 20 | pF |
| All | Digital Input Load | | | 6 | |
| Pull-up resistor | | 76K | 90K | 104K | ohms |

I/O pin characteristics for pins 5, 45, 46, 47 (for all other I/O, see the [SAM D21G datasheet](#)).

4.2 Recommended Operating Conditions

Table 4-5. Recommended Operating Conditions

| Characteristic | Symbol | Minimum | Typical | Maximum | Unit |
|------------------------|--------|---------|---------|---------|------|
| I/O supply voltage | VDDIO | 2.7 | 3.3 | 3.6 | V |
| Battery supply voltage | VBATT | 3.0 | 3.6 | 4.2 | |
| Operating temperature | | -40 | | 85 | °C |

Notes: 1. I/O supply voltage is applied to the following pins: VDDIO_A, VDDIO.

2. Battery supply voltage is applied to following pins: VDD_BATT_PPA, VDD_BATT_PA, and VBATT_BUCK.

4.3 DC Electrical Characteristics

[Table 4-6](#) provides the DC characteristics for the ATSAMW25 digital pads.

Table 4-6. DC Electrical Characteristics

| VDDIO Condition | Characteristic | Minimum | Maximum | Unit |
|--------------------|------------------------------|------------|-------------------------|------|
| VDDIO _L | Input Low Voltage V_{IL} | -0.30 | 0.60 | V |
| | Input High Voltage V_{IH} | VDDIO-0.60 | VDDIO+0.30 | |
| | Output Low Voltage V_{OL} | | 0.45 | |
| | Output High Voltage V_{OH} | VDDIO-0.50 | | |
| VDDIO _M | Input Low Voltage V_{IL} | -0.30 | 0.63 | |
| | Input High Voltage V_{IH} | VDDIO-0.60 | VDDIO+0.30 | |
| | Output Low Voltage V_{OL} | | 0.45 | |
| | Output High Voltage V_{OH} | VDDIO-0.50 | | |
| VDDIO _H | Input Low Voltage V_{IL} | -0.30 | 0.65 | |
| | Input High Voltage V_{IH} | VDDIO-0.60 | VDDIO+0.30 (up to 3.60) | |
| | Output Low Voltage V_{OL} | | 0.45 | |
| | Output High Voltage V_{OH} | VDDIO-0.50 | | |
| All | Output Loading | | 20 | pF |
| All | Digital Input Load | | 6 | |

5 Application and Core Subsystems

5.1 Host Processor

The Atmel | SMART SAM D ARM Cortex-M0+ based microcontroller (MCU) series builds on decades of innovation and experience in embedded Flash microcontroller technology. It not only sets a new benchmark for flexibility and ease-of-use but also combines the performance and energy efficiency of an ARM Cortex-M0+ based MCU with an optimized architecture and peripheral set. The Atmel | SMART SAM D gives you a truly differentiated general-purpose microcontroller that is ideal for many low-power, cost-sensitive industrial and consumer applications.

5.1.1 Host MCU Description

A rich set of peripherals, flexibility and ease-of-use combined with low power consumption make the Atmel SAM D21 ideal for a wide range of home automation, consumer, metering, and industrial applications.

- ARM Cortex-M0+ based MCU running up to 48MHz
- 256KB embedded Flash and 32KB SRAM
- DMA and Event system
- Six flexible serial communication modules (SERCOM)
- Full-Speed USB Device and embedded Host
- 12-bit ADC (SAM D21G: 14 channels); 10-bit DAC
- Hardware touch support

5.1.2 Host MCU Key Features

- Low power consumption, down to 70 μ A/MHz
- Enhanced Analog Performance
 - ADC with offset and gain correction
 - Averaging, oversampling, and decimation
 - Flexible DAC
 - New low power internal oscillators
 - $\pm 2\%$ accuracy over operating range
- Digital Innovations
 - Programmable Event System
 - Enhanced TC for Control Applications
 - Programmable SERCOM module
 - I²C / SPI / USART / LIN2 / IrDA
 - Full Speed USB Device and Host
 - No external components needed
 - 6-12 channel DMA with CRC module
 - PTC Hardware touch module
 - I²S module with PDM support

5.2 Wi-Fi Core Processor

ATWINC1500A has a Cortus APS3 32-bit processor. This processor performs many of the MAC functions, including but not limited to association, authentication, power management, security key management, and MSDU aggregation/de-aggregation. In addition, the processor provides flexibility for various modes of operation, such as STA and AP modes.

5.2.1 Memory Subsystem

The APS3 core uses a 128KB instruction/boot ROM along with a 128KB instruction RAM and a 64KB data RAM. ATWINC1500A also has 4Mb of flash memory, which can be used for system software. In addition, the device uses a 128KB shared RAM, accessible by the processor and MAC, which allows the APS3 core to perform various data management tasks on the TX and RX data packets.

5.2.2 Non-Volatile Memory (eFuse)

ATWINC1500A has 768 bits of non-volatile eFuse memory that can be read by the CPU after device reset. This non-volatile one-time-programmable (OTP) memory can be used to store customer-specific parameters, such as MAC address; various calibration information, such as TX power, crystal frequency offset, etc.; and other software-specific configuration parameters. The eFuse is partitioned into six 128-bit banks. Each bank has the same bit map, which is shown in Figure 5-1. The purpose of the first 80 bits in each bank is fixed, and the remaining 48 bits are general-purpose software dependent bits, or reserved for future use. Since each bank can be programmed independently, this allows for several updates of the device parameters following the initial programming, e.g. updating MAC address. Refer to ATWINC1500A Programming Guide for the eFuse programming instructions.

Figure 5-1. eFuse Bit Map



6 WLAN Subsystem

The WLAN subsystem is composed of the Media Access Controller (MAC) and the Physical Layer (PHY). The following two subsections describe the MAC and PHY in detail.

6.1 MAC

6.1.1 Features

The ATWINC1500A IEEE802.11 MAC supports the following functions:

- IEEE 802.11b/g/n
- IEEE 802.11e WMM QoS EDCA/PCF multiple access categories traffic scheduling
- Advanced IEEE 802.11n features:
 - Transmission and reception of aggregated MPDUs (A-MPDU)
 - Transmission and reception of aggregated MSDUs (A-MSDU)
 - Immediate Block Acknowledgement
 - Reduced Interframe Spacing (RIFS)
- Support for IEEE802.11i and WPA security with key management
 - WEP 64/128
 - WPA-TKIP
 - 128-bit WPA2 CCMP (AES)
- Support for WAPI security
- Advanced power management
 - Standard 802.11 Power Save Mode
 - Wi-Fi Alliance WMM-PS (U-APSD)
- RTS-CTS and CTS-self support
- Supports either STA or AP mode in the infrastructure basic service set mode
- Supports independent basic service set (IBSS)

6.1.2 Description

The ATWINC1500A MAC is designed to operate at low power while providing high data throughput. The IEEE 802.11 MAC functions are implemented with a combination of dedicated data path engines, hardwired control logic, and a low-power, high-efficiency microprocessor. The combination of dedicated logic with a programmable processor provides optimal power efficiency and real-time response while providing the flexibility to accommodate evolving standards and future feature enhancements. Dedicated data path engines are used to implement data path functions with heavy computational. For example, an FCS engine checks the CRC of the transmitting and receiving packets, and a cipher engine performs all the required encryption and decryption operations for the WEP, WPA-TKIP, WPA2 CCMP-AES, and WAPI security requirements. Control functions which have real-time requirements are implemented using hardwired control logic modules. These logic modules offer real-time response while maintaining configurability via the processor. Examples of hardwired control logic modules are the channel access control module (implements EDCA/HCCA, Beacon TX control, interframe spacing, etc.), protocol timer module (responsible for the Network Access Vector, back-off timing, timing synchronization function, and slot management), MPDU handling module, aggregation/de-aggregation module, block ACK controller (implements the protocol requirements for burst block communication), and TX/RX control FSMs (coordinate data movement between PHY-MAC interface, cipher engine, and the DMA interface to the TX/RX FIFOs).

The MAC functions implemented solely in software on the microprocessor have the following characteristics:

- Functions with high memory requirements or complex data structures. Examples are association table management and power save queuing.
- Functions with low computational load or without critical real-time requirements. Examples are authentication and association.
- Functions which need flexibility and upgradeability. Examples are beacon frame processing and QoS scheduling.

6.2 PHY

6.2.1 Features

The ATWINC1500A IEEE802.11 PHY supports the following functions:

- Single antenna 1x1 stream in 20MHz channels
- Supports IEEE 802.11b DSSS-CCK modulation: 1, 2, 5.5, 11Mbps
- Supports IEEE 802.11g OFDM modulation: 6, 9, 12, 18, 24, 36, 48, 54Mbps
- Supports IEEE 802.11n HT modulations MCS0-7, 20MHz, 800 and 400ns guard interval: 6.5, 7.2, 13.0, 14.4, 19.5, 21.7, 26.0, 28.9, 39.0, 43.3, 52.0, 57.8, 58.5, 65.0, 72.2Mbps
- IEEE 802.11n mixed mode operation
- Per packet TX power control
- Advanced channel estimation/equalization, automatic gain control, CCA, carrier/symbol recovery, and frame detection

6.2.2 Description

The ATWINC1500A WLAN PHY is designed to achieve reliable and power-efficient physical layer communication specified by IEEE 802.11 b/g/n in single stream mode with 20MHz bandwidth. Advanced algorithms have been employed to achieve maximum throughput in a real world communication environment with impairments and interference. The PHY implements all the required functions such as FFT, filtering, FEC (Viterbi decoder), frequency and timing acquisition and tracking, channel estimation and equalization, carrier sensing, and clear channel assessment, as well as the automatic gain control.

6.3 Radio

6.3.1 Receiver Performance

Radio Performance under Typical Conditions: VBAT=3.3V; VDDIO=3.3V; Temp.: 25°C @ RF pins

Table 6-1. Receiver Performance

| Parameter | Description | Minimum | Typical ⁽¹⁾ | Maximum | Unit |
|---------------------|-------------|---------|------------------------|---------|------|
| Frequency | | 2,412 | | 2,484 | MHz |
| Sensitivity 802.11b | 1Mbps DSS | | -95.5 | | dBm |
| | 2Mbps DSS | | -93.5 | | |
| | 5.5Mbps DSS | | -91 | | |
| | 11Mbps DSS | | -87 | | |

| Parameter | Description | Minimum | Typical ⁽¹⁾ | Maximum | Unit |
|-----------------------------------|-------------|---------|------------------------|---------|------|
| Sensitivity 802.11g | 6Mbps OFDM | | -89 | | dBm |
| | 9Mbps OFDM | | -87.5 | | |
| | 12Mbps OFDM | | -86.5 | | |
| | 18Mbps OFDM | | -84.5 | | |
| | 24Mbps OFDM | | -81.5 | | |
| | 36Mbps OFDM | | -78 | | |
| | 48Mbps OFDM | | -74 | | |
| | 54Mbps OFDM | | -72 | | |
| Sensitivity 802.11n (BW=20MHz) | MCS 0 | | -87.5 | | dBm |
| | MCS 1 | | -85 | | |
| | MCS 2 | | -82 | | |
| | MCS 3 | | -79.5 | | |
| | MCS 4 | | -75.5 | | |
| | MCS 5 | | -72 | | |
| | MCS 6 | | -70 | | |
| | MCS 7 | | -68.5 | | |

Note: 1. Measured at RF pin assuming 50Ω differential; RF performance guaranteed for temperature range -30 to 85°C. 1dB derating in performance at -40°C.

6.3.2 Transmitter Performance

Radio Performance under Typical Conditions: VBAT=3.3V; VDDIO=3.3V; Temp.: 25°C @ RF pins

Table 6-2. Transmitter Performance

| Parameter | Description | Minimum | Typical ⁽¹⁾ | Maximum | Unit |
|--------------|------------------|---------|------------------------|---------|------|
| Frequency | | 2,412 | | 2,484 | MHz |
| Output power | 802.11b / 11Mbps | | 17 | | dBm |
| | 802.11g / 54Mbps | | 15@EVM -28dB | | |
| | 802.11n / 65Mbps | | 13@EVM -30dB | | |

Note: 1. Measured at 802.11 spec compliant EVM / Spectral Mask; Measured at RF pin assuming 50Ω differential RF performance guaranteed for temperature range -30 to 85°C. 1dB derating in performance at -40°C.

7 Recommended Reflow Profile

| Setpoints (Celsius) | | | | | | | | | |
|---------------------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Zone | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 |
| Top | 200 | 140 | 160 | 180 | 180 | 210 | 220 | 265 | 265 |
| Bottom | 200 | 140 | 160 | 180 | 180 | 210 | 220 | 265 | 265 |
| Conveyor Speed (cm/min): 65.0 | | | | | | | | | |



| PW= 64% | Max Rising Slope | Max Falling Slope | Soak Time 150-200C | Reflow Time /217C | Peak Temp | | | | | |
|---------|------------------|-------------------|--------------------|-------------------|-----------|------|-------|------|--------|------|
| <TC2> | 1.17 | -41% | -3.92 | -30% | 74.60 | -51% | 54.87 | -56% | 242.73 | -23% |
| <TC3> | 1.19 | -40% | -2.68 | 13% | 75.03 | -50% | 54.99 | -56% | 241.73 | -31% |
| <TC4> | 1.18 | -41% | -4.09 | -35% | 74.83 | -51% | 54.90 | -56% | 244.28 | -12% |
| <TC5> | 1.19 | -40% | -3.63 | -20% | 73.47 | -55% | 53.11 | -64% | 244.22 | -13% |
| <TC6> | 1.17 | -41% | -4.04 | -34% | 73.63 | -55% | 55.09 | -55% | 243.92 | -15% |
| Delta | 0.02 | | 1.41 | | 1.56 | | 1.98 | | 2.55 | |

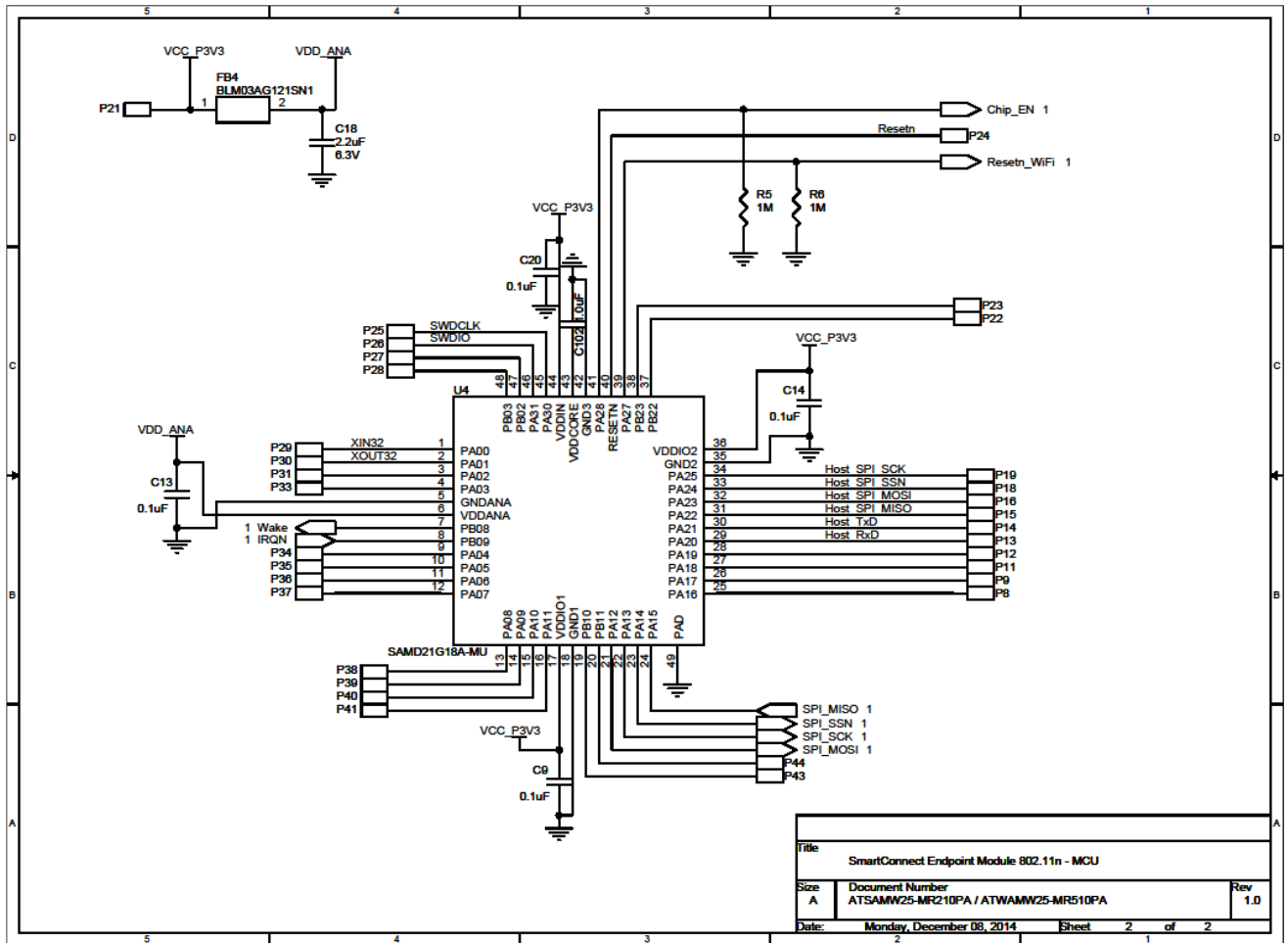
Process Window:

| | | | |
|--|-----------|------------|-----------------|
| Solder Paste: | RoHS | | |
| Statistic Name | Low Limit | High Limit | Units |
| Max Rising Slope (Target=2.0) (Calculate Slope over 90 Seconds) | 0 | 3 | Degrees/Second |
| Max Falling Slope (Calculate Slope over 6 Seconds) | -6 | -0.1 | Degrees/Second |
| Soak Time 150-200C | 60 | 120 | Seconds |
| Time Above Reflow - 217C | 45 | 90 | Seconds |
| Peak Temperature | 232 | 260 | Degrees Celsius |

8 Reference Design

The ATSAMW25-MR210PA reference design schematic is shown in Figure 8-1.

Figure 8-1. ATSAMW25-MR210PA Reference Schematic



9 Bill of Materials (BOM)

| Item | Qty. | Reference | Value | Description | Manufacturer | Part Number | Footprint |
|------|------|--|---------------|--|--------------------|----------------------------------|---------------|
| 1 | 1 | A1 | Antenna | Antenna, printed circuit, inverted F | | Non component | PCB F |
| 2 | 1 | C1 | 0.01µF | CAP,CER,0.01µF,10%,XSR,0201,10V,-55-125°C | Murata | GRM033R61A103KA01D | CS0201 |
| 3 | 13 | C2,C4,C5,C6,C8,C9,C11,C12,C13,C14,C19,C20,C25 | 0.1µF | CAP,CER,0.1µF,10%,XSR,0201,6.3V,-55-125°C | Murata | GRM033R60J104KE19D | CS0201 |
| 4 | 3 | C3,C10,C18 | 2.2µF | CAP,CER,2.2µF,10%,XSR,0402,6.3V,-55-85°C | TDK | C1005XSR0J225K | CS0402 |
| 5 | 1 | C7 | 1.0µF | CAP,CER,1.0µF,10%,XSR,0402,6.3V,-55-85°C | GRM155R60J10SKE19D | GRM155R60J10SKE19D | CS0402 |
| 6 | 2 | C15,C16 | 5.6pF | CAP,CER,5.6pF,0.5pF,NPO,0201,25V,-55-125°C | Murata | GRM0335C2A5R6DA01D | CS0201 |
| 7 | 2 | C17,C32 | 1.0pF | CAP,CER,1.0pF,0.1pF,NPO,0201,25V,-55-125°C | Murata | GRM0335C1E1R0BA01J | RS0201 |
| 8 | 1 | C21 | DNI | CAP,CER,1.0pF,0.1pF,NPO,0201,25V,-55-125°C | Murata | GRM0335C1E1R0BA01J | RS0201 |
| 9 | 1 | C22 | DNI | CAP,CER,0.5pF,0.1pF,NPO,0201,25V,-55-125°C | Murata | 500RGRM0335C1ER50BA0 | RS0201 |
| 10 | 2 | C23,C24 | 6.8pF | CAP,CER,6.8pF,0.5pF,NPO,0201,25V,-55-125°C | TDK | C0603C0G1E6R8D030BA | RS0201 |
| 11 | 1 | C33 | 0.7pF | CAP,CER,0.7pF,0.05pF,NPO,0201,25V,-55-125°C | TDK | C0603C0G1E0R7W030BF | RS0201 |
| 12 | 2 | C34,C35 | DNI | CAP,CER,0.5pF,0.1pF,NPO,0201,25V,-55-125°C | Murata | 500RGRM0335C1ER50BA01D0750R5AV4T | RS0201 |
| 13 | 1 | C102 | 1.0µF | CAP,CER,1.0µF,20%,XSR,0402,6.3V | Panasonic | ECJ-0EB0J105M | CS0402 |
| 14 | 4 | FB1,FB2,FB3,FB4 | BLM03AG121SN1 | FERRITE,120Ω@100MHz,200mA,0201,-55-125°C | Murata | BLM03AG121SN1 | FB50201 |
| 15 | 1 | L1 | 1µH | Power inductor,1µH,20%,940mA,0.125Ω,0603,shielded,-40-85°C | Murata | LQM18PN1R0MFRL | LS0603 |
| 16 | 1 | L5 | 15nH | Inductor,multilayer,15nH,5%,350mA,Q=8@100MHz,0402 | Murata | LQG15HS15NJ02D | LS0402 |
| 17 | 2 | L8,L9 | 3.3nH | Inductor,3.3nH,0.2nH,Q=13@500MHz,SRF=8.1GHz,0201,-55-125°C | Taiyo Yuden | HKQ0603S3N3C-T | LS0201 |
| 18 | 51 | P1,P2,P3,P4,P5,P6,P7,P8,P9,P10,P11,P12,P13,P14,P15,P16,P17,P18,P19,P20,P21,P22,P23,P24,P25,P26,P27,P28,P29,P30,P31,P32,P33,P34,P35,P36,P37,P38,P39,P40,P41,P42,P43,P44,P45,P46,P47,P48,P49,P50,P51 | PAD 0.7X1.2 | LGA module pad, 0.7mm x 1.2mm | | Non component | PAD 0.7x1.2mm |
| 19 | 1 | R1 | 2.0nH | Inductor,2.0nH,0.2nH,Q=13@500MHz,SRF=8.1GHz,0201,-55-125°C | Taiyo Yuden | HKQ0603S2N0C-T | RS0201 |
| 20 | 1 | R2 | 0.5pF | CAP,CER,0.5pF,0.1pF,NPO,0201,25V,-55-125°C | Murata | 500RGRM0335C1ER50BA0 | RS0201 |
| 21 | 1 | R3 | DNI | CAP,CER,0.5pF,0.1pF,NPO,0201,25V,-55-125°C | Murata | 500RGRM0335C1ER50BA0 | RS0201 |
| 22 | 1 | R4 | 1.2nH | Inductor,1.2nH,0.1nH,Q=14@500MHz,SRF=6GHz,0201,-55-125°C | Murata | LQP03TN1N2B02D | RS0201 |
| 23 | 3 | R5,R6,R7 | 1MΩ | Resistor, thick film,1MΩ,5%,0201 | Vishay | CRCW0201-105J | RS0201 |
| 24 | 9 | R8,R11,R12,R13,R14,R15,R16,R17,R18 | 0 | Resistor, thick film,0Ω,0201 | Panasonic | ERJ-1GN0R00C | RS0201 |
| 25 | 2 | R9,R10 | DNI | Resistor, thick film,0Ω,0201 | Panasonic | ERJ-1GN0R00C | RS0201 |
| 26 | 2 | R19,R20 | 4.7KΩ | Resistor, thick film,4.7kΩ,5%,0201 | Vishay | CRCW0201-472J | RS0201 |
| 27 | 1 | SH1 | SHIELD | Shield | | | SHIELD_164 |
| 28 | 1 | TP1 | DNI | Test point, surface mount,0.030"sq. | | Non component | TP_SMD-25SQ |
| 29 | 1 | U1 | ATWINC1500 | IC, Wi-Fi, 40QFN | Atmel | ATWINC1500 | 40QFN |
| 30 | 1 | U2 | ATECC108A | IC, memory, CryptoAuthentication,8UDFN | Atmel | ATECC108A-MAHDA | BUDFN |
| 31 | 1 | U3 | SI1865DDL | IC, load switch, 1.8V-12V in, RDSon=0.3Ω@2.5V,SC70-6 | Vishay | SI1865DDL | SC70-6 |
| 32 | 1 | U4 | SAMD21G18A-MU | MCU | Atmel | SAMD21G18A-MU | 48QFN |
| 33 | 1 | Y1 | 26MHz | XTAL,26MHz,CL=7.36pF,10ppm,-30-85°C,ESR=50,3.2x2.5mm | NDK | NX3225SA-26.000000MHZ-G3 | UM_ABM8 |

10 Application Schematics

Figure 10-1. Connections for the SAMW25



The basic power supply connections for the SAMW25 module are shown in [Figure 10-1](#). The test points shown (TP1 – TP6) should be added in case Atmel is required to debug the design.

The Wi-Fi chip can use its own internal oscillator for a Real Time Clock (RTC) or it can use an external 32.768KHz clock provided on the RTC pin. Using an external clock derived from a crystal oscillator can be used as a more accurate sleep timer for the Wi-Fi chip than its own internal oscillator. This in turn can reduce sleep current. If power consumption during sleep is a priority then a 32.768KHz crystal can be added to the SAMD21 module as shown in the reference design. The design shown above displays a connection from pin 15 (PA22) to pin 5 (GPIO_1).

GPIO_1 is the input pin for the Wi-Fi's Real Time Clock. PA22 can be configured to output a 32.768KHz RTC clock – derived from the 32.768KHz crystal - to be used as the source for the Wi-Fi's RTC. If cost is a priority versus power consumption, then the 32.768KHz crystal can be left off of the design and the PA22 – GPIO_1 connection can be deleted.

11 Design Guidelines

It is critical to follow the recommendations listed below to achieve the best RF performance:

- When the module is placed on the motherboard, a provision for the antenna must be made. There should be nothing under the portion of the module which contains the antenna. This means the antenna should not be placed directly on top of the motherboard PCB. This can be accomplished by, for example, placing the module at the edge of the board such that the module edge with the antenna extends beyond the main board edge by 6.5mm. Alternatively, a cutout in the motherboard can be provided under the antenna. The cutout should be at least 22mm x 6.5mm. Ground vias spaced 2.5mm apart should be placed all around the perimeter of the cutout. No large components should be placed near the antenna.
- Keep away from antenna, as far as possible, large metal objects to avoid electromagnetic field blocking
- Do not enclose the antenna within a metal shield
- Keep any components which may radiate noise or signals within the 2.4 – 2.5GHz frequency band far away from the antenna or better yet, shield those components. Any noise radiated from the main board in this frequency band will degrade the sensitivity of the module.
- The main board should have a solid ground plane. Each ground pin of the module (including each of the center ground pads) should have a via placed either in the pad or right next to the pad going down to the ground plane.
- Place a 10 μ F decoupling capacitor from VBAT to ground right next to pin 7. Place another 10 μ F capacitor from VCC to ground right next to pin 21.
- Contact Atmel for assistance if any other placement is required

12 Reference Documentation and Support

12.1 Reference Documents

Atmel offers a set of collateral documentation to ease integration and device ramp.

The following list of documents available on Atmel web or integrated into development tools.

Table 12-1. Reference Documents

| Title | Content |
|--------------------------------|---|
| Datasheet | This document |
| Design Files | User Guide, Schematic, PCB layout, Gerber, BOM, and System notes on: RF/Radio Full Test Report, radiation pattern, design guidelines, temperature performance, ESD. |
| Package | How to use package: Out of the Box starting guide, HW limitations and notes, SW Quick start guidelines. |
| Platform Getting started Guide | Best practices and recommendations to design a board with the product, including: Antenna Design for Wi-Fi (layout recommendations, types of antennas, impedance matching, using a power amplifier etc.), SPI/UART protocol between Wi-Fi SoC and the Host MCU. |
| HW Design Guide | Integration guide with clear description of: High level Arch, overview on how to write a networking application, list all API, parameters and structures. Features of the device, SPI/handshake protocol between device and host MCU, with flow/sequence/state diagram, timing. |
| SW Design Guide | Explain in details the flow chart and how to use each API to implement all generic use cases (e.g. start AP, start STA, provisioning, UDP, TCP, http, TLS, p2p, errors management, connection/transfer recovery mechanism/state diagram) - usage and sample application note. |

For a complete listing of development-support tools and documentation, visit <http://www.atmel.com/> or contact the nearest Atmel field representative.

12.2 Related Documents

- [1] ATSAM D21 Datasheet:
Web page: <http://www.atmel.com/products/microcontrollers/arm/sam-d.aspx?tab=documents>.
Document: [Atmel SAM D21 Datasheet](#) (.pdf file).
Then select the required device ([ATSAMD21E18A](#)) and get the latest datasheet (.pdf file).
- [2] [ATWINC1500 Datasheet](#).
- [3] [ATSAM W25 Network Controller Programming Guide](#).
- [4] [ATSAM W25 Starter Kit User Guide](#).

13 Revision History

| Doc Rev. | Date | Comments |
|----------|---------|---------------------------|
| 42395A | 03/2015 | Initial document release. |



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