14-Bit, 80 MSPS/155 MSPS, 1.8 V Dual Serial Output Analog-to-Digital Converter (ADC)

Data Sheet **AD9644**

FEATURES

- JESD204A coded serial digital outputs
- SNR = 73.7 dBFS at 70 MHz and 80 MSPS
- SNR = 71.7 dBFS at 70 MHz and 155 MSPS
- SFDR = 92 dBc at 70 MHz and 80 MSPS
- SFDR = 92 dBc at 70 MHz and 155 MSPS
- Low power: 423 mW at 80 MSPS, 567 mW at 155 MSPS
- 1.8 V supply operation
- Integer 1-to-8 input clock divider
- IF sampling frequencies to 250 MHz
- −148.6 dBFS/Hz input noise at 180 MHz and 80 MSPS
- −150.3 dBFS/Hz input noise at 180 MHz and 155 MSPS
- Programmable internal ADC voltage reference
- Flexible analog input range: 1.4 V p-p to 2.1 V p-p
- ADC clock duty cycle stabilizer
- Serial port control
- User-configurable, built-in self-test (BIST) capability
- Energy-saving power-down modes

APPLICATIONS

- Communications
- Diversity radio systems
- Multimode digital receivers (3G and 4G)
  - GSM, EDGE, W-CDMA, LTE,
  - CDMA2000, WiMAX, TD-SCDMA
- I/Q demodulation systems
- Smart antenna systems
- General-purpose software radios
- Broadband data applications
- Ultrasound equipment

FUNCTIONAL BLOCK DIAGRAM

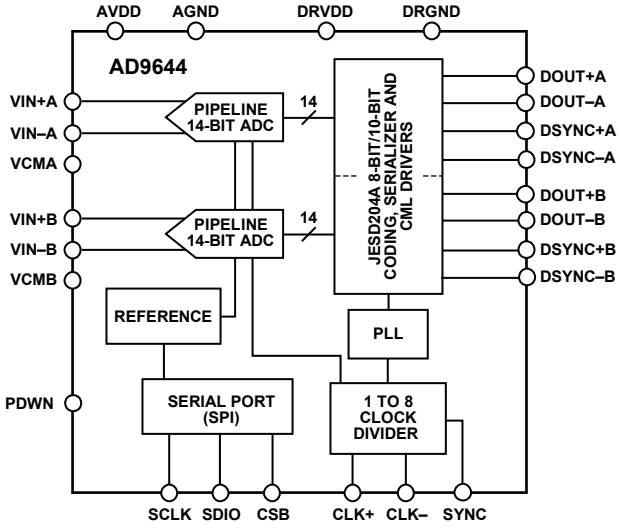

Figure 1. 48-Lead 7 mm × 7 mm LFCSP

PRODUCT HIGHLIGHTS

1. An on-chip PLL allows users to provide a single ADC sampling clock; the PLL multiplies the ADC sampling clock to produce the corresponding JESD204A data rate clock.
2. The configurable JESD204A output block supports up to 1.6 Gbps per channel data rate when using a dedicated data link per ADC or 3.2 Gbps data rate when using a single shared data link for both ADCs.
3. Proprietary differential input that maintains excellent SNR performance for input frequencies up to 250 MHz.
4. Operation from a single 1.8 V power supply.
5. Standard serial port interface (SPI) that supports various product features and functions, such as data formatting (offset binary, twos complement, or gray coding), controlling the clock DCS, power-down, test modes, voltage reference mode, and serial output configuration.

Rev. C

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REVISION HISTORY

1/12—Rev. B to Rev. C

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6/11—Rev. A to Rev. B

Added Figure 23 to Figure 40; Renumbered Sequentially ... 16
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4/11—Rev. 0 to Rev. A

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6/10—Revision 0: Initial Version

GENERAL DESCRIPTION

The AD9644 is a dual, 14-bit, analog-to-digital converter (ADC) with a high speed serial output interface and sampling speeds of either 80 MSPS or 155 MSPS.

The AD9644 is designed to support communications applications where high performance, combined with low cost, small size, and versatility, is desired. The JESD204A high speed serial interface reduces board routing requirements and lowers pin count requirements for the receiving device.

The dual ADC core features a multistage, differential pipelined architecture with integrated output error correction logic. Each ADC features wide bandwidth differential sample-and-hold analog input amplifiers that support a variety of user-selectable input ranges. An integrated voltage reference eases design considerations. A duty cycle stabilizer is provided to compensate for variations in the ADC clock duty cycle, allowing the converters to maintain excellent performance.

By default, the ADC output data is routed directly to the two external JESD204A serial output ports. These outputs are at CML voltage levels. Two modes are supported such that output coded data is either sent through one data link or two. (L = 1; F = 4 or L = 2; F = 2). Independent synchronization inputs (DSYNC) are provided for each channel.

Flexible power-down options allow significant power savings, when desired.

Programming for setup and control is accomplished using a 3-wire SPI-compatible serial interface.

The AD9644 is available in a 48-lead LFCSP and is specified over the industrial temperature range of −40°C to +85°C.

This product is protected by a U.S. patent.

SPECIFICATIONS

ADC DC SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, maximum sample rate, 1.75 V p-p differential input, VIN = −1.0 dBFS differential input, DCS enabled, unless otherwise noted.

Table 1.

		AD9644-80			AD9644-155			
Parameter	**Temperature**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
RESOLUTION	Full	14			14			Bits
ACCURACY								
No Missing Codes	Full		Guaranteed			Guaranteed		
Offset Error	Full		±2	±10		±2.2	±11	mV
Gain Error	Full	−7	−2.5	+1	−6	−1.5	+4	% FSR
Differential Nonlinearity (DNL)[1]	Full			±0.55			±0.55	LSB
	25°C		±0.3			±0.3		LSB
Integral Nonlinearity (INL)[1]	Full			±1.1			±1.25	LSB
	25°C		±0.5			±0.55		LSB
MATCHING CHARACTERISTIC								
Offset Error	Full	−7	+1.5	+10	−6	+1.5	+9	mV
Gain Error	Full	−1.5	+0.6	+2.75	−3.1	+0.75	+5	% FSR
TEMPERATURE DRIFT								
Offset Error	Full		±2			±2		ppm/°C
Gain Error	Full		±35			±144		ppm/°C
INPUT REFERRED NOISE	25°C		0.7			0.7		LSB rms
ANALOG INPUT								
Input Span	Full	1.383	1.75	2.087	1.383	1.75	2.087	V p-p
Input Capacitance[2]	Full		7			5		pF
Input Resistance	Full		20			20		kΩ
VCM OUTPUT LEVEL	Full	0.88	0.9	0.92	0.87	0.9	0.93	V
POWER SUPPLIES								
Supply Voltage								
AVDD	Full	1.7	1.8	1.9	1.7	1.8	1.9	V
DRVDD	Full	1.7	1.8	1.9	1.7	1.8	1.9	V
Supply Current								
IAVDD[1]	Full		175	190		226	242	mA
IDRVDD[1]	Full		60	67		89	97	mA
POWER CONSUMPTION								
Sine Wave Input1	Full		423	460		567	610	mW
Standby Power[3]	Full		85			168		mW
Power-Down Power	Full		15	27		18	27	mW

[1] Measured with a low input frequency, full-scale sine wave.
[2] Input capacitance refers to the effective capacitance between one differential input pin and AGND.
[3] Standby power is measured with a dc input and with the CLK pins inactive (set to AVDD or AGND).

ADC AC SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, maximum sample rate, 1.75 V p-p differential input, VIN = −1.0 dBFS differential input, DCS enabled, unless otherwise noted.

Table 2.

		AD9644-80			AD9644-155			
Parameter[1]	**Temperature**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
SIGNAL-TO-NOISE-RATIO (SNR)								
f_{IN} = 10 MHz	25°C		73.8			71.9		dBFS
f_{IN} = 70 MHz	25°C		73.7			71.7		dBFS
f_{IN} = 180 MHz	25°C		72.6			71.4		dBFS
AD9644BCPZ-80	Full	71.8						dBFS
AD9644CCPZ-80	Full	70.0						dBFS
AD9644BCPZ-155	Full				69.8			dBFS
f_{IN} = 220 MHz	25°C		72.0			71.0		dBFS
SIGNAL-TO-NOISE AND DISTORTION (SINAD)								
f_{IN} = 10 MHz	25°C		72.7			70.8		dBFS
f_{IN} = 70 MHz	25°C		72.6			70.7		dBFS
f_{IN} = 180 MHz	25°C		71.5			70.3		dBFS
AD9644BCPZ-80	Full	70.4						dBFS
AD9644CCPZ-80	Full	68.6						dBFS
AD9644BCPZ-155	Full				68.7			dBFS
f_{IN} = 220 MHz	25°C		71.1			69.9		dBFS
EFFECTIVE NUMBER OF BITS (ENOB)								
f_{IN} = 10 MHz	25°C		11.8			11.5		Bits
f_{IN} = 70 MHz	25°C		11.8			11.5		Bits
f_{IN} = 180 MHz	25°C		11.6			11.4		Bits
f_{IN} = 220 MHz	25°C		11.5			11.3		Bits
WORST SECOND OR THIRD HARMONIC								
f_{IN} = 10 MHz	25°C		−94			−94		dBc
f_{IN} = 70 MHz	25°C		−92			−92		dBc
f_{IN} = 180 MHz	25°C		−87			−92		dBc
AD9644BCPZ-80	Full			−80				dBc
AD9644CCPZ-80	Full			−73				dBc
AD9644BCPZ-155	Full						−80	dBc
f_{IN} = 220 MHz	25°C		−85			−90		dBc
SPURIOUS-FREE DYNAMIC RANGE (SFDR)								
f_{IN} = 10 MHz	25°C		94			94		dBc
f_{IN} = 70 MHz	25°C		92			92		dBc
f_{IN} = 180 MHz	25°C		87			92		dBc
AD9644BCPZ-80	Full	80						dBc
AD9644CCPZ-80	Full	73						dBc
AD9644BCPZ-155	Full				80			dBc
f_{IN} = 220 MHz	25°C		85			90		dBc
WORST OTHER (HARMONIC OR SPUR)								
f_{IN} = 10 MHz	25°C		−98			−97		dBc
f_{IN} = 70 MHz	25°C		−98			−97		dBc
f_{IN} = 180 MHz	25°C		−96			−95		dBc
AD9644BCPZ-80	Full			−90				dBc
AD9644CCPZ-80	Full			−87				dBc
AD9644BCPZ-155	Full						−89	dBc
f_{IN} = 220 MHz	25°C		−95			−94		dBc

Parameter[1]	Temperature	AD9644-80 Min	AD9644-80 Typ	AD9644-80 Max	AD9644-155 Min	AD9644-155 Typ	AD9644-155 Max	Unit
TWO-TONE SFDR								
f_{IN} = +30 MHz (−7 dBFS), +33 MHz (−7 dBFS)	25°C		93			90		dBc
f_{IN} = +169 MHz (−7 dBFS), +172 MHz (−7 dBFS)	25°C		89			89		dBc
CROSSTALK[2]	Full		−105			−105		dB
ANALOG INPUT BANDWIDTH[3]	25°C		780			780		MHz

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for a complete set of definitions.
[2] Crosstalk is measured at 100 MHz with −1.0 dBFS on one channel and no input on the alternate channel.
[3] Analog input bandwidth specifies the −3 dB input BW of the AD9644 input. The usable full-scale BW of the part with good performance is 250 MHz.

DIGITAL SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, maximum sample rate, 1.75 V p-p differential input, VIN = −1.0 dBFS differential input, and DCS enabled, unless otherwise noted.

Table 3.

Parameter	Temperature	AD9644-80/AD9644-155 Min	AD9644-80/AD9644-155 Typ	AD9644-80/AD9644-155 Max	Unit
DIFFERENTIAL CLOCK INPUTS (CLK+, CLK−)					
Logic Compliance			CMOS/LVDS/LVPECL		
Internal Common-Mode Bias	Full		0.9		V
Differential Input Voltage	Full	0.3		3.6	V p-p
Input Voltage Range	Full	AGND		AVDD	V
Input Common-Mode Range	Full	0.9		1.4	V
High Level Input Current	Full	−100		+100	µA
Low Level Input Current	Full	−100		+100	µA
Input Capacitance	Full		4		pF
Input Resistance	Full	8	10	12	kΩ
SYNC INPUT					
Logic Compliance			CMOS		
Internal Bias	Full		0.9		V
Input Voltage Range	Full	AGND		AVDD	V
High Level Input Voltage	Full	1.2		AVDD	V
Low Level Input Voltage	Full	AGND		0.6	V
High Level Input Current	Full	−100		+100	µA
Low Level Input Current	Full	−100		+100	µA
Input Capacitance	Full		1		pF
Input Resistance	Full	12	16	20	kΩ
DSYNC INPUT					
Logic Compliance			CMOS/LVDS		
Internal Bias	Full		0.9		V
Input Voltage Range	Full	AGND		AVDD	V
High Level Input Voltage	Full	1.2		AVDD	V
Low Level Input Voltage	Full	AGND		0.6	V
High Level Input Current	Full	−100		+100	µA
Low Level Input Current	Full	−100		+100	µA
Input Capacitance	Full		1		pF
Input Resistance	Full	12	16	20	kΩ

Parameter	Temperature	AD9644-80/AD9644-155 Min	Typ	Max	Unit
LOGIC INPUT (CSB)[1]					
Logic Compliance			CMOS		
High Level Input Voltage	Full	1.22		2.1	V
Low Level Input Voltage	Full	0		0.6	V
High Level Input Current	Full	−10		+10	µA
Low Level Input Current	Full	40		132	µA
Input Resistance	Full		26		kΩ
Input Capacitance	Full		2		pF
LOGIC INPUT (SCLK, PDWN)[2]					
Logic Compliance			CMOS		
High Level Input Voltage	Full	1.22		2.1	V
Low Level Input Voltage	Full	0		0.6	V
High Level Input Current (VIN = 1.8 V)	Full	−92		−135	µA
Low Level Input Current	Full	−10		+10	µA
Input Resistance	Full		26		kΩ
Input Capacitance	Full		2		pF
LOGIC INPUT/OUTPUT (SDIO)[1]					
Logic Compliance			CMOS		
High Level Input Voltage	Full	1.22		2.1	V
Low Level Input Voltage	Full	0		0.6	V
High Level Input Current	Full	−10		+10	µA
Low Level Input Current	Full	38		128	µA
Input Resistance	Full		26		kΩ
Input Capacitance	Full		5		pF
DIGITAL OUTPUTS					
Logic Compliance	Full		CML		
Differential Output Voltage (V_{OD})	Full	0.6	0.8	1.1	V
Output Offset Voltage (V_{OS})	Full	0.75	DRVDD/2	1.05	V

[1] Pull up.
[2] Pull down.

SWITCHING SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, maximum sample rate, 1.75 V p-p differential input, VIN = −1.0 dBFS differential input, and DCS enabled, unless otherwise noted.

Table 4.

		AD9644-80			AD9644-155			
Parameter	**Temperature**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
CLOCK INPUT PARAMETERS								
Input Clock Rate	Full			640			640	MHz
Conversion Rate[1]	Full	40		80	40		155	MSPS
CLK Period—Divide-by-1 Mode (t_{CLK})	Full	12.5			6.45			ns
CLK Pulse Width High (t_{CH})								
Divide-by-1 Mode, DCS Enabled	Full	3.75	6.25	8.75	1.935	3.225	4.515	ns
Divide-by-1 Mode, DCS Disabled	Full	5.95	6.25	6.55	3.065	3.225	3.385	ns
Divide-by-2 Mode Through Divide-by-8 Mode	Full	0.8			0.8			ns
Aperture Delay (t_A)	Full		0.78			0.78		ns
Aperture Uncertainty (Jitter, t_J)	Full		0.125			0.125		ps rms
DATA OUTPUT PARAMETERS								
Data Output Period or UI (Unit Interval)	Full		$1/(20 \times f_{CLK})$			$1/(20 \times f_{CLK})$		Seconds
Data Output Duty Cycle	25°C		50			50		%
Data Valid Time	25°C		0.78			0.74		UI
PLL Lock Time (t_{LOCK})	25°C		4			4		µs
Wake Up Time (Standby)	25°C		5			5		µs
Wake Up Time (Power-Down)[2]	25°C		2.5			2.5		ms
Pipeline Delay (Latency)	Full	23		24	23		24	CLK cycles
Data Rate per Channel (NRZ)	25°C		1.6			3.1		Gbps
Deterministic Jitter	25°C		40			40		ps
Random Jitter at 1.6 Gbps	25°C		9.5					ps rms
Random Jitter at 3.2 Gbps	25°C		5.2			5.2		ps rms
Output Rise/Fall Time	25°C		50			50		ps
TERMINATION CHARACTERISTICS								
Differential Termination Resistance	25°C		100			100		Ω
OUT-OF-RANGE RECOVERY TIME	25°C		2			2		CLK cycles

[1] Conversion rate is the clock rate after the divider.
[2] Wake-up time is defined as the time required to return to normal operation from power-down mode.

TIMING SPECIFICATIONS

Table 5.

Parameter	Conditions	Limit
SYNC TIMING REQUIREMENTS		
t_{SSYNC}	SYNC to rising edge of CLK+ setup time	0.30 ns typ
t_{HSYNC}	SYNC to rising edge of CLK+ hold time	0.30 ns typ
SPI TIMING REQUIREMENTS		
t_{DS}	Setup time between the data and the rising edge of SCLK	2 ns min
t_{DH}	Hold time between the data and the rising edge of SCLK	2 ns min
t_{CLK}	Period of the SCLK	40 ns min
t_S	Setup time between CSB and SCLK	2 ns min
t_H	Hold time between CSB and SCLK	2 ns min
t_{HIGH}	SCLK pulse width high	10 ns min
t_{LOW}	SCLK pulse width low	10 ns min
t_{EN_SDIO}	Time required for the SDIO pin to switch from an input to an output relative to the SCLK falling edge	10 ns min
t_{DIS_SDIO}	Time required for the SDIO pin to switch from an output to an input relative to the SCLK rising edge	10 ns min

Timing Diagrams

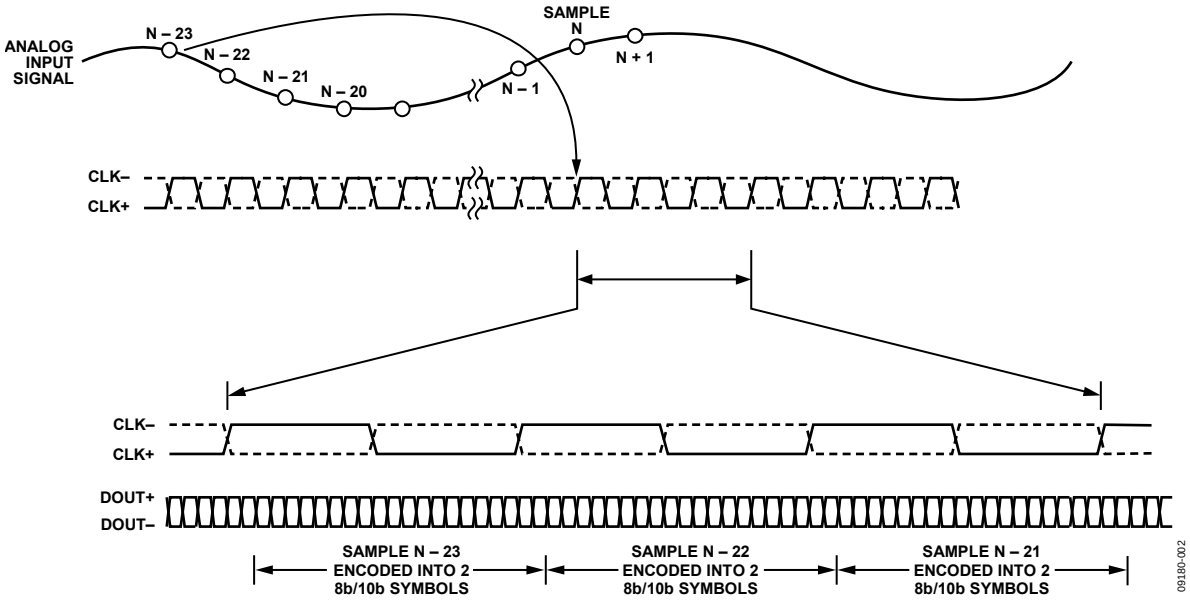


Figure 2. Data Output Timing

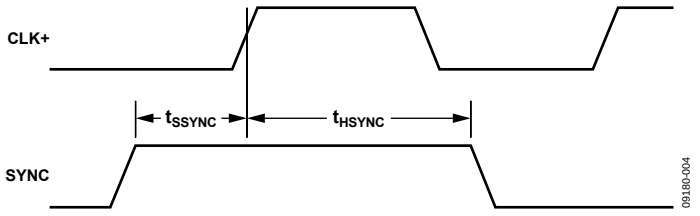


Figure 3. SYNC Input Timing Requirements

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
ELECTRICAL	
AVDD to AGND	−0.3 V to +2.0 V
DRVDD to AGND	−0.3 V to +2.0V
VIN+A/VIN+B, VIN−A/VIN−B to AGND	−0.3 V to AVDD + 0.2 V
CLK+, CLK− to AGND	−0.3 V to AVDD + 0.2 V
SYNC to AGND	−0.3 V to AVDD + 0.2 V
VCMA, VCMB to AGND	−0.3 V to AVDD + 0.2 V
CSB to AGND	−0.3 V to DRVDD + 0.2 V
SCLK to AGND	−0.3 V to DRVDD + 0.2 V
SDIO to AGND	−0.3 V to DRVDD + 0.2 V
PDWN to AGND	−0.3 V to DRVDD + 0.2 V
DOUT+A, DOUT0−A, DOUT0+B, DOUT−B to AGND	−0.3 V to DRVDD + 0.2 V
DSYNC+A, DSYNC−A, DSYNC+B, DSYNC−B to AGND	−0.3 V to DRVDD + 0.2 V
ENVIRONMENTAL	
Operating Temperature Range (Ambient)	−40°C to +85°C
Maximum Junction Temperature Under Bias	150°C
Storage Temperature Range (Ambient)	−65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

The exposed paddle must be soldered to the ground plane for the LFCSP package. Soldering the exposed paddle to the PCB increases the reliability of the solder joints and maximizes the thermal capability of the package.

Table 7. Thermal Resistance

Package Type	Airflow Velocity (m/sec)	θ_{JA}[1,2]	θ_{JC}[1,3]	θ_{JB}[1,4]	Unit
48-Lead LFCSP 7 mm × 7 mm (CP-48-8)	0	25	2	14	°C/W
	1.0	22			°C/W
	2.5	20			°C/W

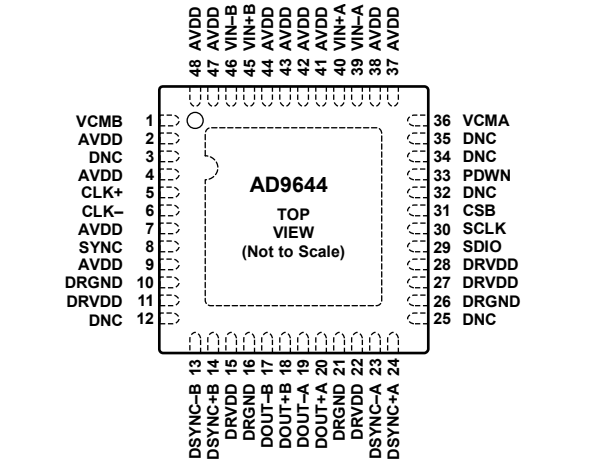
[1] Per JEDEC 51-7, plus JEDEC 25-5 2S2P test board.
[2] Per JEDEC JESD51-2 (still air) or JEDEC JESD51-6 (moving air).
[3] Per MIL-STD 883, Method 1012.1.
[4] Per JEDEC JESD51-8 (still air).

Typical θ_{JA} is specified for a 4-layer PCB with a solid ground plane. As shown Table 7, airflow improves heat dissipation, which reduces θ_{JA}. In addition, metal in direct contact with the package leads from metal traces, through holes, ground, and power planes, reduces θ_{JA}.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. DNC = DO NOT CONNECT.
2. THE EXPOSED THERMAL PAD ON THE BOTTOM OF THE PACKAGE PROVIDES THE ANALOG GROUND FOR THE PART. THIS EXPOSED PAD MUST BE CONNECTED TO GROUND FOR PROPER OPERATION.

Figure 4. LFCSP Pin Configuration (Top View)

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
ADC Power Supplies			
11, 15, 22, 27, 28	DRVDD	Supply	Digital Output Driver Supply (1.8 V Nominal).
2, 4, 7, 9, 37, 38, 41, 42, 43, 44, 47, 48	AVDD	Supply	Analog Power Supply (1.8 V Nominal).
3, 12, 25, 32, 34, 35	DNC		Do Not Connect.
10, 16, 21, 26	DRGND	Driver Ground	Digital Driver Supply Ground.
0	AGND, Exposed Pad	Ground	The exposed thermal pad on the bottom of the package provides the analog ground for the part. This exposed pad must be connected to ground for proper operation.
ADC Analog			
40	VIN+A	Input	Differential Analog Input Pin (+) for Channel A.
39	VIN−A	Input	Differential Analog Input Pin (−) for Channel A.
45	VIN+B	Input	Differential Analog Input Pin (+) for Channel B.
46	VIN−B	Input	Differential Analog Input Pin (−) for Channel B.
36	VCMA	Output	Common-Mode Level Bias Output for Channel A Analog Input.
1	VCMB	Output	Common-Mode Level Bias Output for Channel B Analog Input.
5	CLK+	Input	ADC Clock Input—True.
6	CLK−	Input	ADC Clock Input—Complement.
Digital Input			
8	SYNC	Input	Input Clock Divider Synchronization Pin.
24	DSYNC+A	Input	Active Low JESD204A LVDS Channel A SYNC Input—True/JESD204A CMOS Channel A SYNC Input.
23	DSYNC−A	Input	Active Low JESD204A LVDS Channel A SYNC Input—Complement.
14	DSYNC+B	Input	Active Low JESD204A LVDS Channel B SYNC Input—True/JESD204A CMOS Channel A SYNC Input.
13	DSYNC−B	Input	Active Low JESD204A LVDS Channel B SYNC Input—Complement.

Pin No.	Mnemonic	Type	Description
Digital Outputs			
20	DOUT+A	Output	Channel A CML Output Data—True.
19	DOUT−A	Output	Channel A CML Output Data—Complement.
18	DOUT+B	Output	Channel B CML Output Data—True.
17	DOUT−B	Output	Channel B CML Output Data—Complement.
SPI Control			
30	SCLK	Input	SPI Serial Clock.
29	SDIO	Input/Output	SPI Serial Data Input/Output.
31	CSB	Input	SPI Chip Select (Active Low).
ADC Configuration			
33	PDWN	Input	Power-Down Input. Using the SPI interface, this input can be configured as power-down or standby.

TYPICAL PERFORMANCE CHARACTERISTICS

AVDD = 1.8 V, DRVDD = 1.8 V, DCS enabled, 1.75 V p-p differential input, VIN = −1.0 dBFS, and 32k sample, T_A = 25°C, unless otherwise noted.

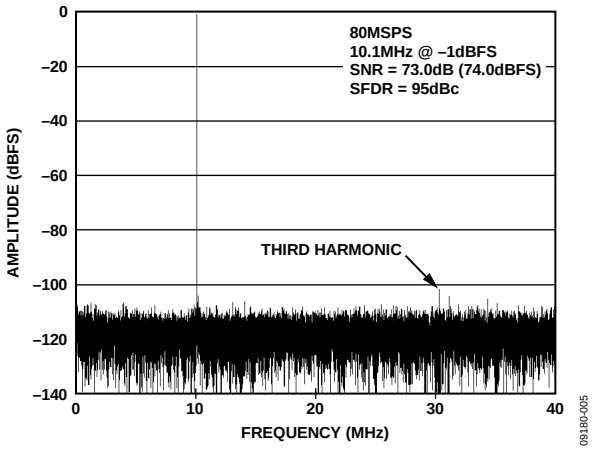


Figure 5. AD9644-80 Single-Tone FFT with f_{IN} = 10.1 MHz

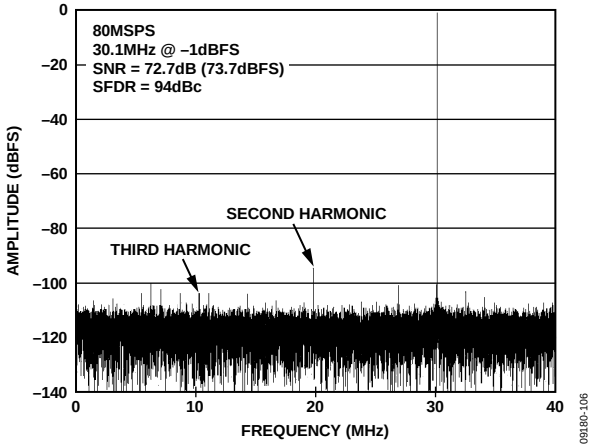


Figure 6. AD9644-80 Single-Tone FFT with f_{IN} = 30.1 MHz

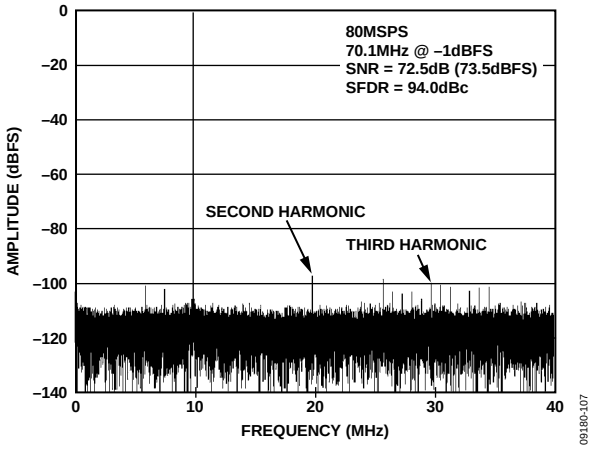


Figure 7. AD9644-80 Single-Tone FFT with f_{IN} = 70.1 MHz

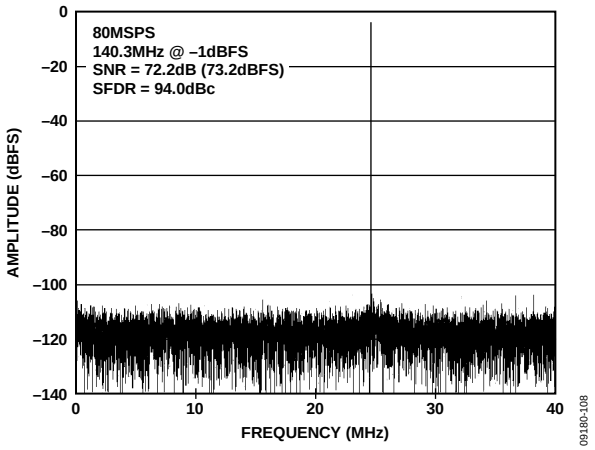


Figure 8. AD9644-80 Single-Tone FFT with f_{IN} = 140.1 MHz

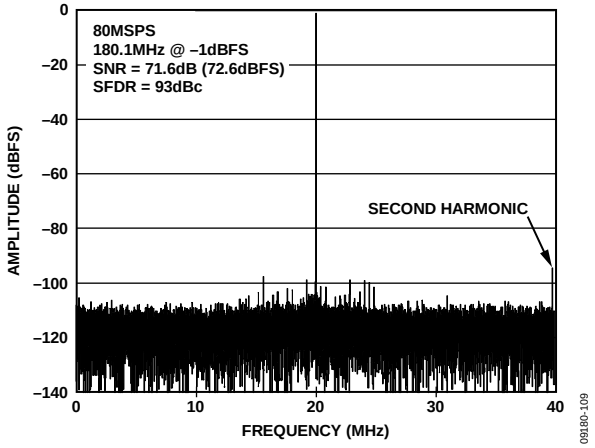


Figure 9. AD9644-80 Single-Tone FFT with f_{IN} = 180.1 MHz

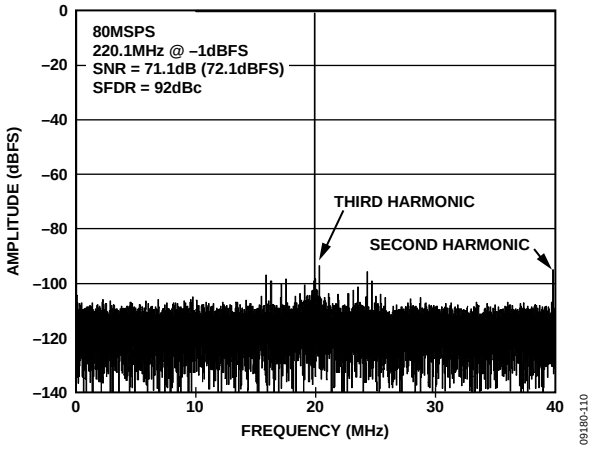


Figure 10. AD9644-80 Single-Tone FFT with f_{IN} = 220.1 MHz

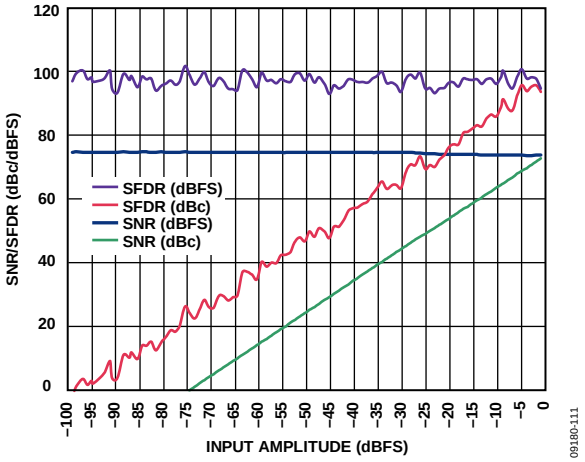


Figure 11. AD9644-80 Single-Tone SNR/SFDR vs. Input Amplitude (A_{IN}) with f_{IN} = 10.1 MHz, f_S = 80 MSPS

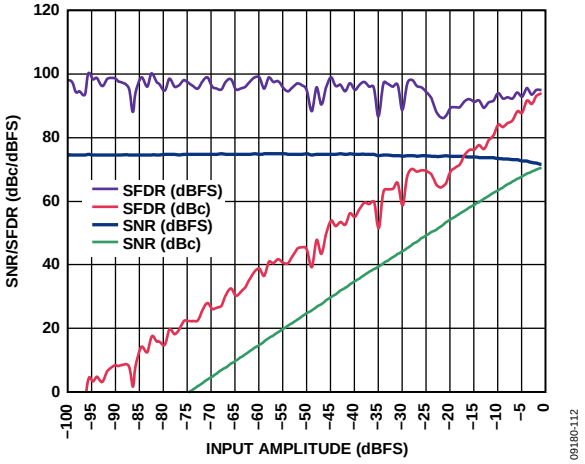


Figure 12. AD9644-80 Single-Tone SNR/SFDR vs. Input Amplitude (A_{IN}) with f_{IN} = 180 MHz, f_S = 80 MSPS

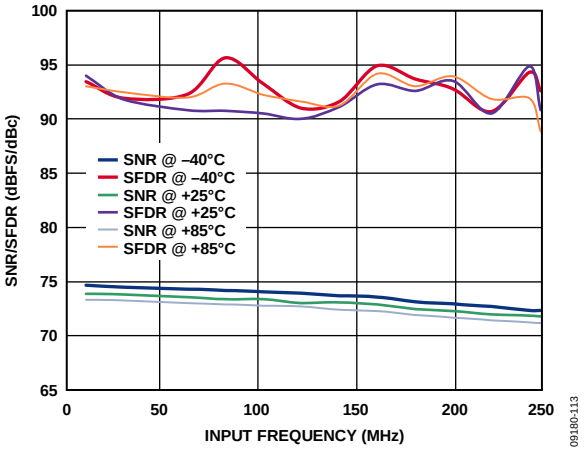


Figure 13. AD9644-80 Single-Tone SNR/SFDR vs. Input Frequency (f_{IN}) and Temperature with 1.75 V p-p Full-Scale, f_S = 80 MSPS

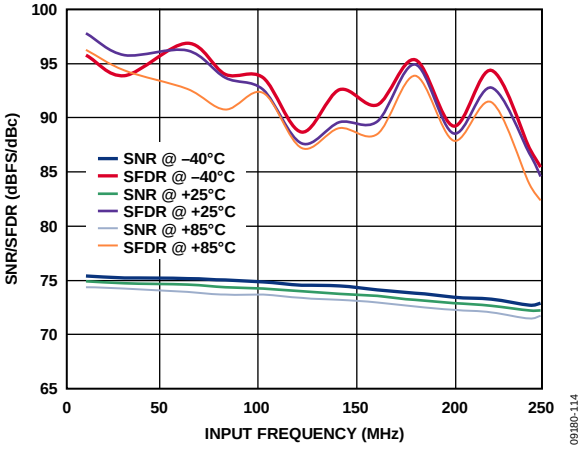


Figure 14. AD9644-80 Single-Tone SNR/SFDR vs. Input Frequency (f_{IN}) and Temperature with 2.0 V p-p Full-Scale, f_S = 80 MSPS

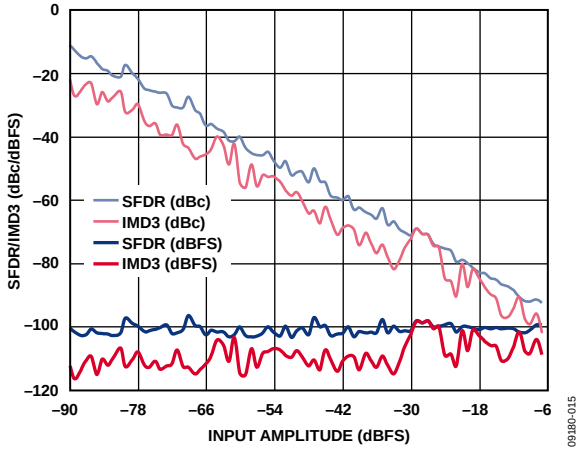


Figure 15. AD9644-80 Two-Tone SFDR/IMD3 vs. Input Amplitude (A_{IN}) with f_{IN1} = 29.9 MHz, f_{IN2} = 32.9 MHz, f_S = 80 MSPS

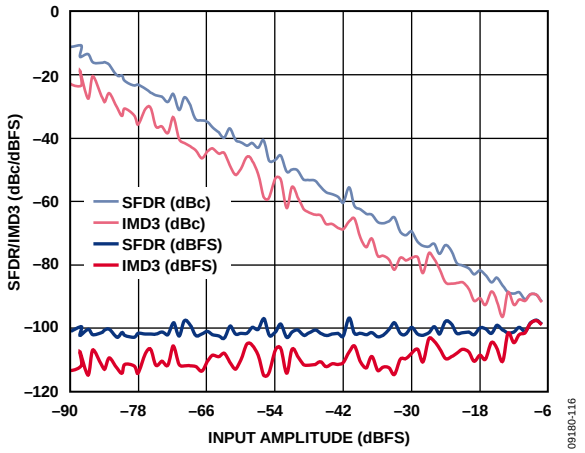


Figure 16. AD9644-80 Two-Tone SFDR/IMD3 vs. Input Amplitude (A_{IN}) with f_{IN1} = 169.1 MHz, f_{IN2} = 172.1 MHz, f_S = 80 MSPS

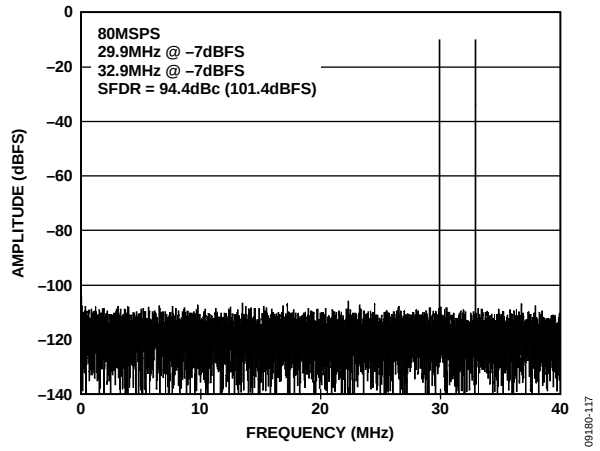


Figure 17. AD9644-80 Two-Tone FFT with f_{IN1} = 29.9 MHz and f_{IN2} = 32.9 MHz

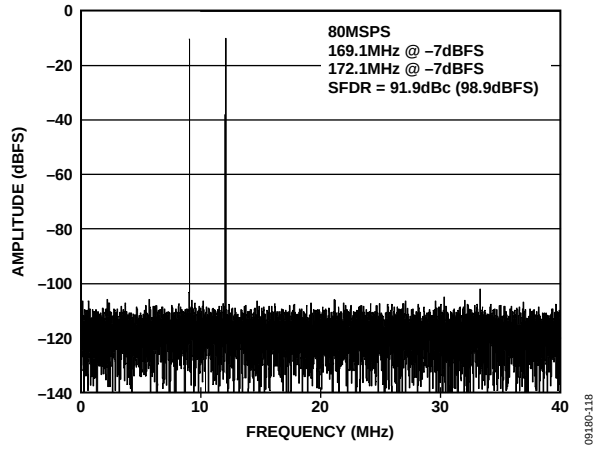


Figure 18. AD9644-80 Two-Tone FFT with f_{IN1} = 169.1 MHz and f_{IN2} = 172.1 MHz

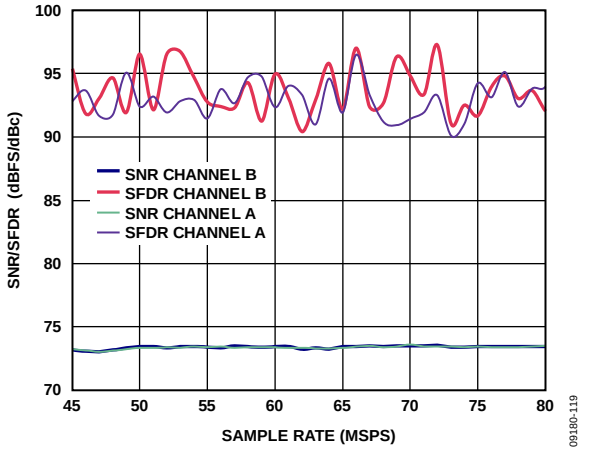


Figure 19. AD9644-80 Single-Tone SNR/SFDR vs. Sample Rate (f_S) with f_{IN} = 70. MHz

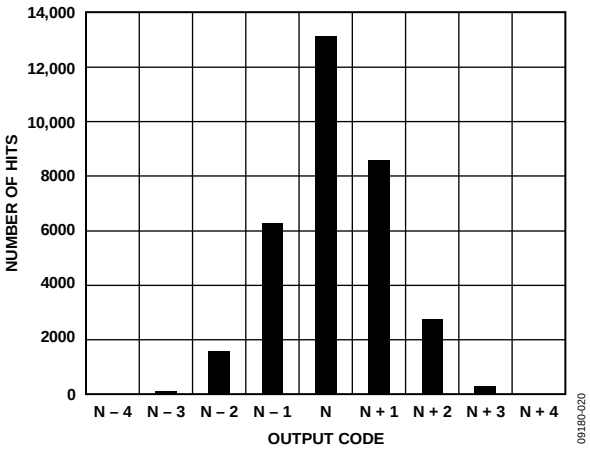


Figure 20. AD9644-80 Grounded Input Histogram

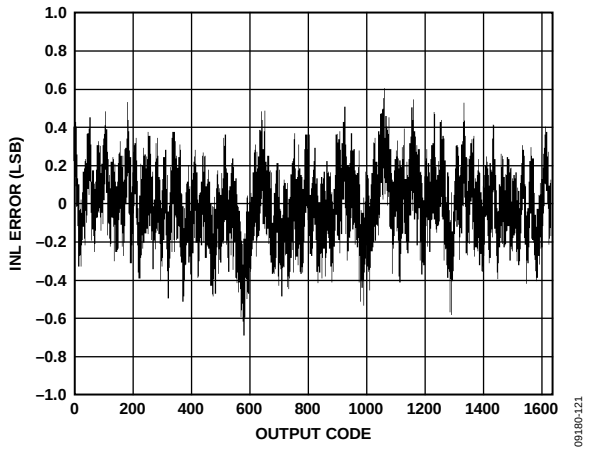


Figure 21. AD9644-80 INL with f_{IN} = 30.3 MHz

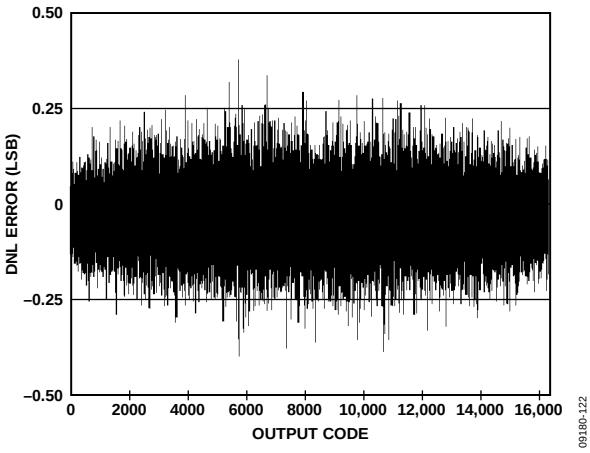


Figure 22. AD9644-80 DNL with f_{IN} = 30.3 MHz

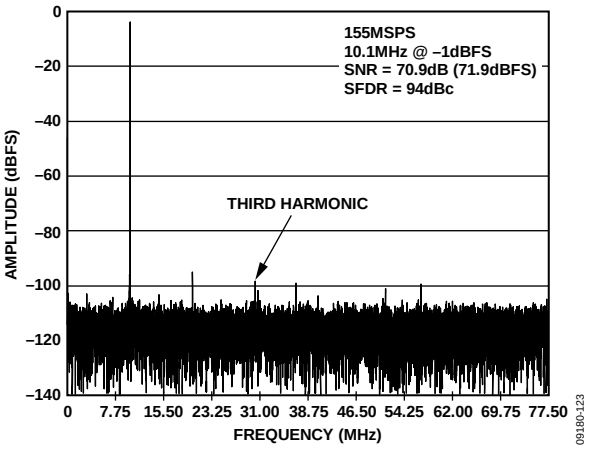


Figure 23. AD9644-155 Single-Tone FFT with f_{IN} = 10.1 MHz

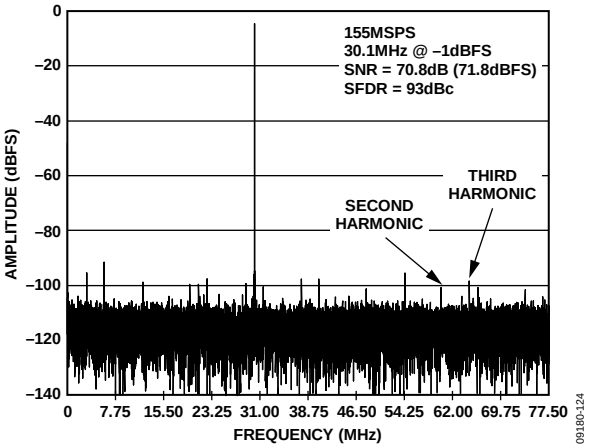


Figure 24. AD9644-155 Single-Tone FFT with f_{IN} = 30.1 MHz

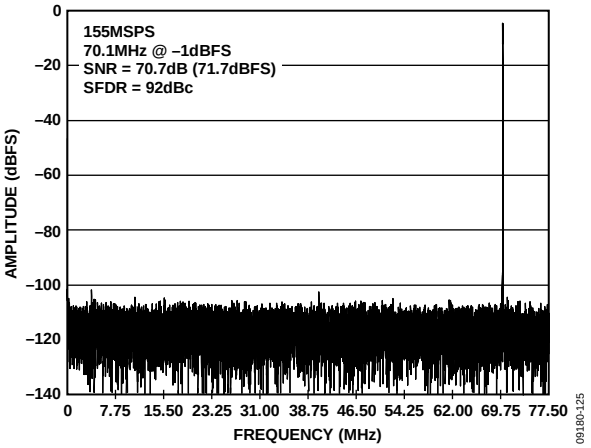


Figure 25. AD9644-155 Single-Tone FFT with f_{IN} = 70.1 MHz

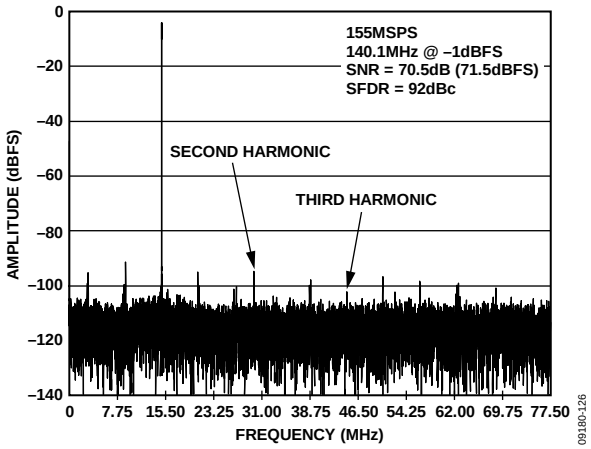


Figure 26. AD9644-155 Single-Tone FFT with f_{IN} = 140.1 MHz

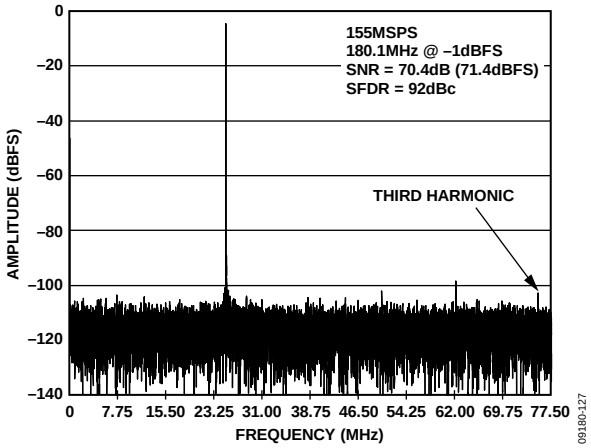


Figure 27. AD9644-155 Single-Tone FFT with f_{IN} = 180.1 MHz

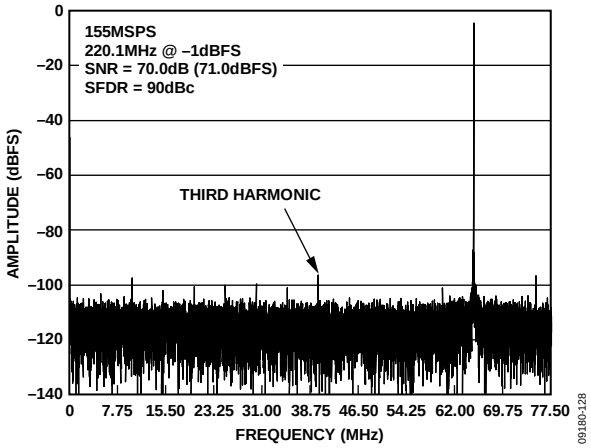


Figure 28. AD9644-155 Single-Tone FFT with f_{IN} = 220.1 MHz

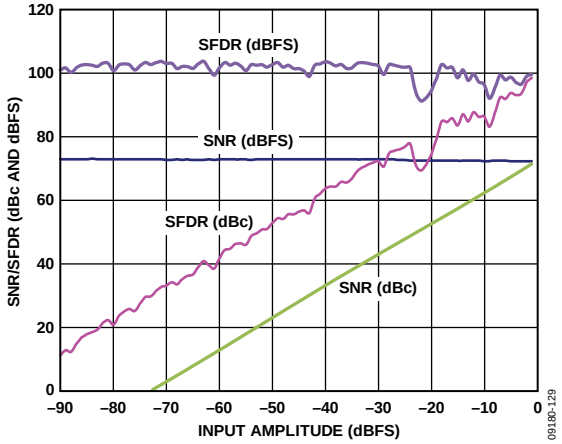


Figure 29. AD9644-155 Single-Tone SNR/SFDR vs. Input Amplitude (A_{IN}) with f_{IN} = 10.1 MHz, f_S = 80 MSPS

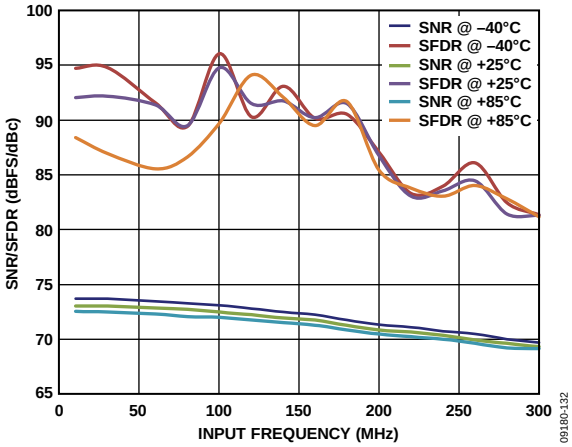


Figure 32. AD9644-155 Single-Tone SNR/SFDR vs. Input Frequency (f_{IN}) and Temperature with 2.0 V p-p Full-Scale, f_S = 80 MSPS

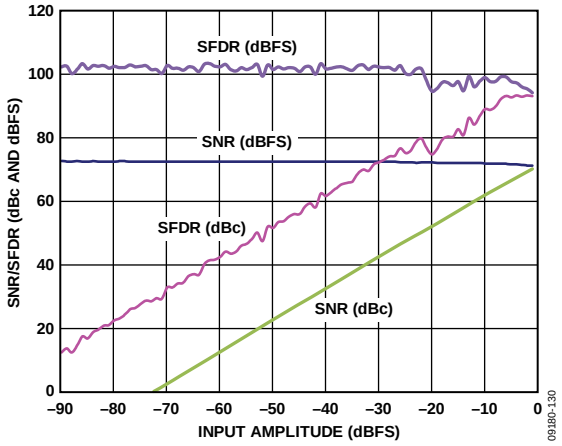


Figure 30. AD9644-155 Single-Tone SNR/SFDR vs. Input Amplitude (A_{IN}) with f_{IN} = 180 MHz, f_S = 80 MSPS

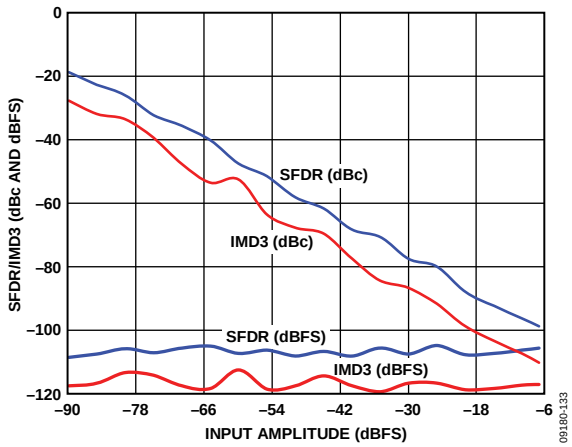


Figure 33. AD9644-155 Two-Tone SFDR/IMD3 vs. Input Amplitude (A_{IN}) with f_{IN1} = 29.9 MHz, f_{IN2} = 32.9 MHz, f_S = 80 MSPS

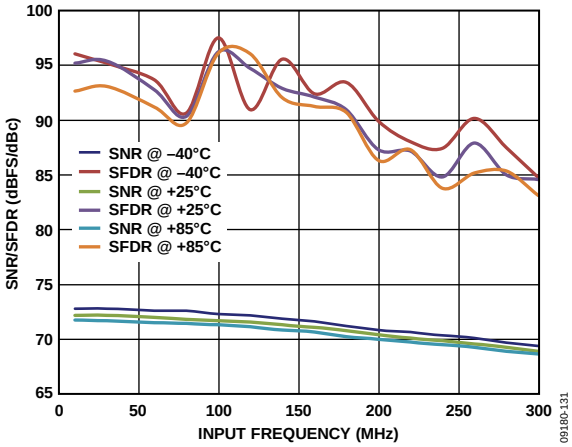


Figure 31. AD9644-155 Single-Tone SNR/SFDR vs. Input Frequency (f_{IN}) and Temperature with 1.75 V p-p Full-Scale, f_S = 80 MSPS

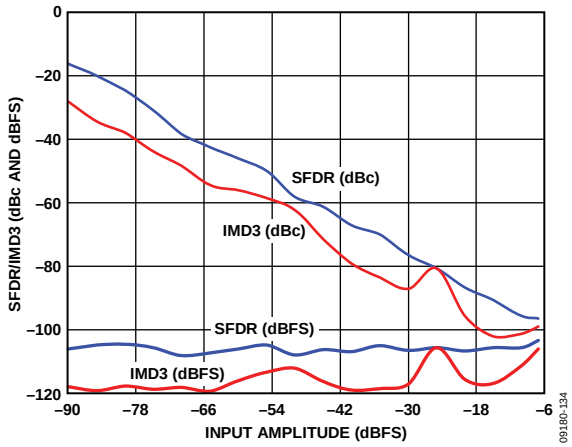


Figure 34. AD9644-155 Two-Tone SFDR/IMD3 vs. Input Amplitude (A_{IN}) with f_{IN1} = 169.1 MHz, f_{IN2} = 172.1 MHz, f_S = 80 MSPS

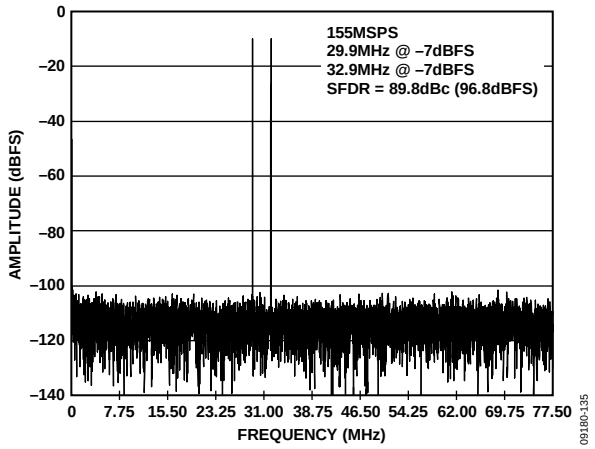


Figure 35. AD9644-155 Two-Tone FFT with f_{IN1} = 29.9 MHz and f_{IN2} = 32.9 MHz

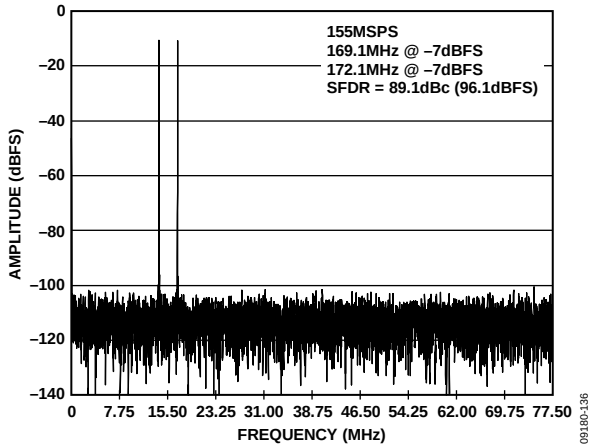


Figure 36. AD9644-155 Two-Tone FFT with f_{IN1} = 169.1 MHz and f_{IN2} = 172.1 MHz

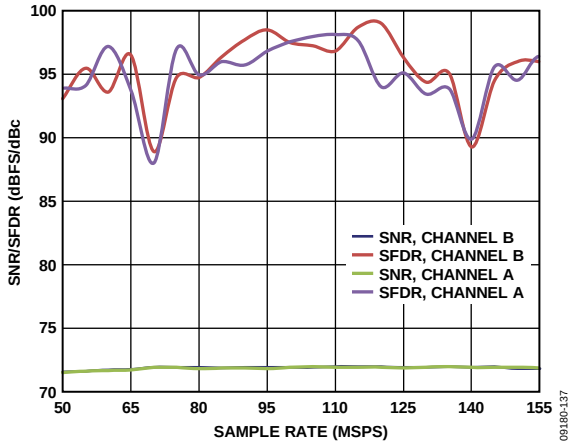


Figure 37. AD9644-155 Single-Tone SNR/SFDR vs. Sample Rate (f_S) with f_{IN} = 70. MHz

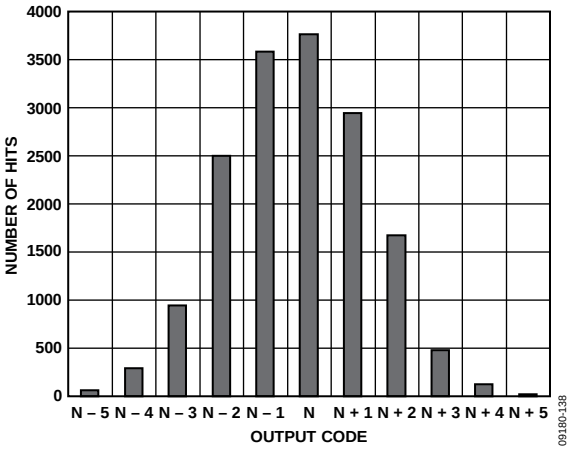


Figure 38. AD9644-155 Grounded Input Histogram

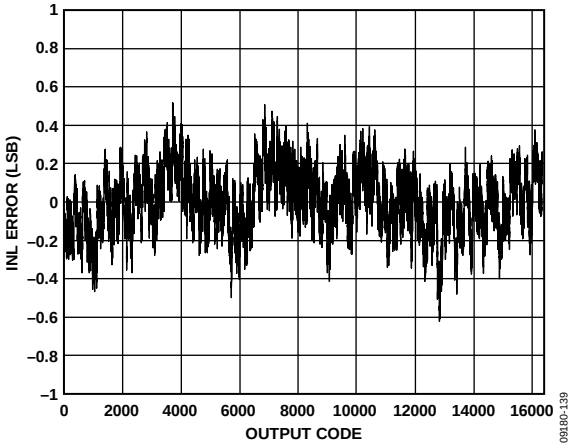


Figure 39. AD9644-155 INL with f_{IN} = 30.3 MHz

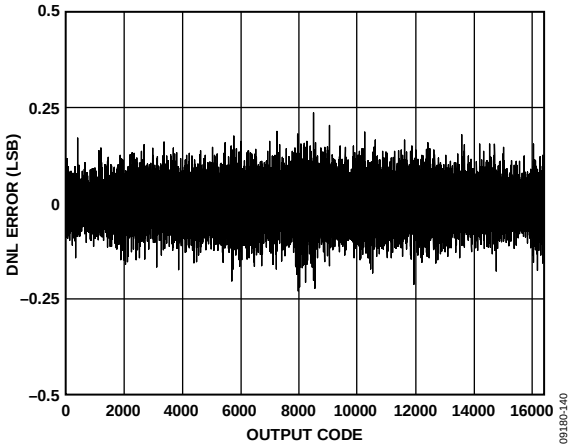


Figure 40. AD9644-155 DNL with f_{IN} = 30.3 MHz

EQUIVALENT CIRCUITS

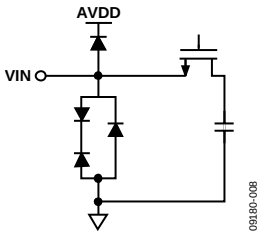


Figure 41. Equivalent Analog Input Circuit

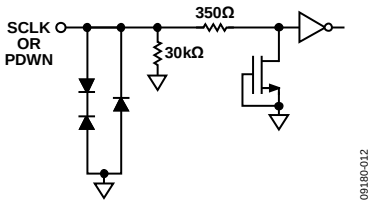


Figure 45. Equivalent SCLK or PDWN Input Circuit

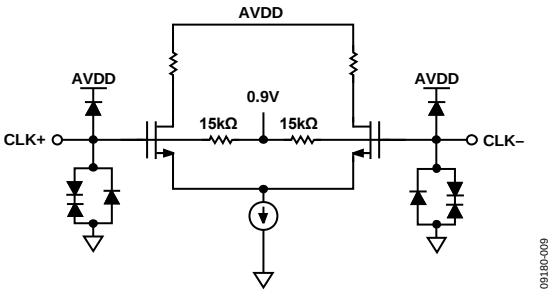


Figure 42. Equivalent Clock Input Circuit

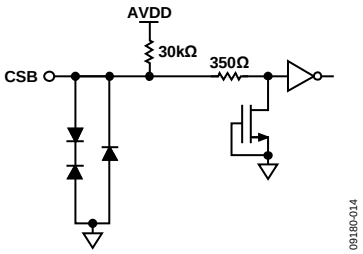


Figure 46. Equivalent CSB Input Circuit

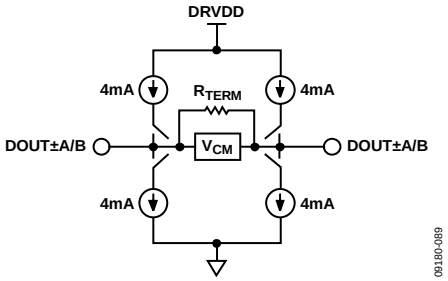


Figure 43. Digital CML Output

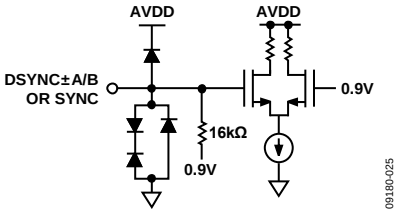


Figure 47. Equivalent SYNC and DSYNC Input Circuit

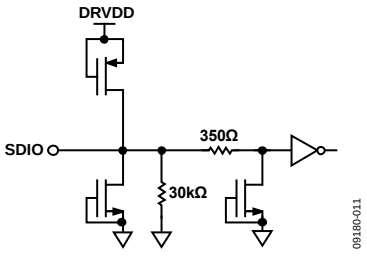


Figure 44. Equivalent SDIO Circuit

THEORY OF OPERATION

The AD9644 dual-core analog-to-digital converter (ADC) can be used for diversity reception of signals, in which the ADCs are operating identically on the same carrier but from two separate antennae. The ADCs can also be operated with independent analog inputs. The user can sample any $f_S/2$ frequency segment from dc to 250 MHz, using appropriate low-pass or band-pass filtering at the ADC inputs with little loss in ADC performance.

In nondiversity applications, the AD9644 can be used as a baseband or direct downconversion receiver, in which one ADC is used for I input data, and the other is used for Q input data.

Synchronization capability is provided to allow synchronized timing between multiple devices.

Programming and control of the AD9644 are accomplished using a 3-wire SPI-compatible serial interface.

ADC ARCHITECTURE

The AD9644 architecture consists of a dual front-end sample-and-hold circuit, followed by a pipelined, switched-capacitor ADC. The quantized outputs from each stage are combined into a final 14-bit result in the digital correction logic. The pipelined architecture permits the first stage to operate on a new input sample and the remaining stages to operate on the preceding samples. Sampling occurs on the rising edge of the clock.

Each stage of the pipeline, excluding the last, consists of a low resolution flash ADC connected to a switched-capacitor digital-to-analog converter (DAC) and an interstage residue amplifier (MDAC). The MDAC magnifies the difference between the reconstructed DAC output and the flash input for the next stage in the pipeline. One bit of redundancy is used in each stage to facilitate digital correction of flash errors. The last stage simply consists of a flash ADC.

The input stage of each channel contains a differential sampling circuit that can be ac- or dc-coupled in differential or single-ended modes. The output staging block aligns the data, corrects errors, and passes the data to the output buffers. The output buffers are powered from a separate supply, allowing digital output noise to be separated from the analog core. During power-down, the output buffers go into a high impedance state.

ANALOG INPUT CONSIDERATIONS

The analog input to the AD9644 is a differential switched-capacitor circuit that has been designed for optimum performance while processing a differential input signal.

The clock signal alternatively switches the input between sample mode and hold mode (see Figure 48). When the input is switched into sample mode, the signal source must be capable of charging the sample capacitors and settling within ½ of a clock cycle.

A small resistor in series with each input can help reduce the peak transient current required from the output stage of the driving source. A shunt capacitor can be placed across the inputs to provide dynamic charging currents. This passive network creates a low-pass filter at the ADC input; therefore, the precise values are dependent on the application.

In intermediate frequency (IF) undersampling applications, any shunt capacitors or series resistors should be reduced since the input sample capacitor is unbuffered. In combination with the driving source impedance, the shunt capacitors limit the input bandwidth. Refer to the AN-742 Application Note, *Frequency Domain Response of Switched-Capacitor ADCs*; the AN-827 Application Note, *A Resonant Approach to Interfacing Amplifiers to Switched-Capacitor ADCs*; and the *Analog Dialog* article, "Transformer-Coupled Front-End for Wideband A/D Converters," for more information on this subject (refer to www.analog.com).

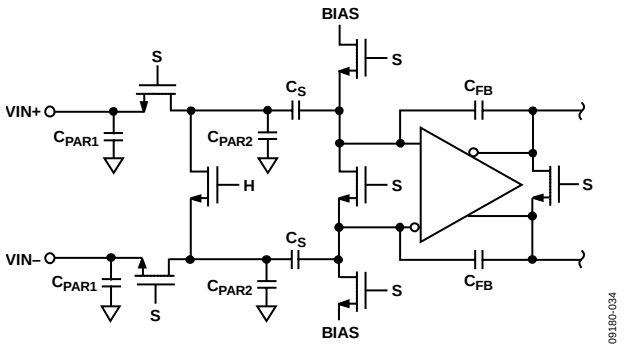


Figure 48. Switched-Capacitor Input

For best dynamic performance, the source impedances driving VIN+ and VIN− should be matched, and the inputs should be differentially balanced.

Input Common Mode

The analog inputs of the AD9644 are not internally dc biased. In ac-coupled applications, the user must provide this bias externally. Setting the device so that VCM = 0.5 × AVDD (or 0.9 V) is recommended for optimum performance. An on-board common-mode voltage reference is included in the design and is available from the VCMA and VCMB pins. Using the VCMA and VCMB outputs to set the input common mode is recommended. Optimum performance is achieved when the common-mode voltage of the analog input is set by the VCMA and VCMB pin voltages (typically 0.5 × AVDD). The VCMA and VCMB pins must be decoupled to ground by a 0.1 µF capacitor. This decoupling capacitor should be placed close to the pin to minimize the series resistance and inductance between the part and this capacitor.

Differential Input Configurations

Optimum performance is achieved while driving the AD9644 in a differential input configuration. For baseband applications, the AD8138, ADA4937-2, and ADA4938-2 differential drivers provide excellent performance and a flexible interface to the ADC.

The output common-mode voltage of the ADA4938-2 is easily set with the VCM pin of the AD9644 (see Figure 49), and the driver can be configured in a Sallen-Key filter topology to provide band limiting of the input signal.

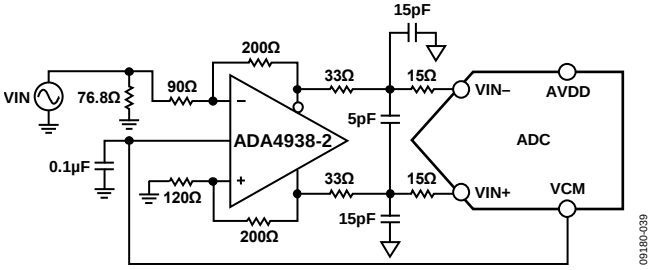


Figure 49. Differential Input Configuration Using the ADA4938-2

For baseband applications in which SNR is a key parameter, differential transformer coupling is the recommended input configuration. An example is shown in Figure 50. To bias the analog input, the VCM voltage can be connected to the center tap of the secondary winding of the transformer.

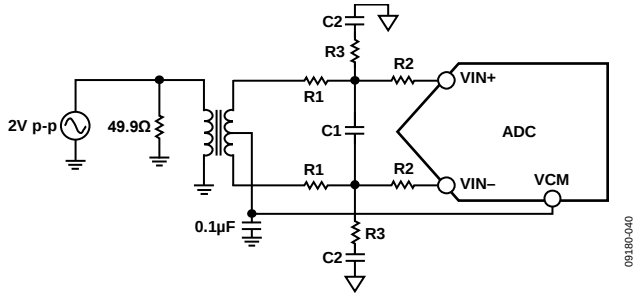


Figure 50. Differential Transformer-Coupled Configuration

The signal characteristics must be considered when selecting a transformer. Most RF transformers saturate at frequencies below a few megahertz (MHz). Excessive signal power can also cause core saturation, which leads to distortion.

At input frequencies in the second Nyquist zone and above, the noise performance of most amplifiers is not adequate to achieve the true SNR performance of the AD9644. For applications in which SNR is a key parameter, differential double balun coupling is the recommended input configuration (see Figure 51). In this configuration, the input is ac-coupled and the VCM is provided to each input through a 33 Ω resistor. These resistors compensate for losses in the input baluns to provide a 50 Ω impedance to the driver.

In the double balun and transformer configurations, the value of the input capacitors and resistors is dependent on the input frequency and source impedance. Based on these parameters the value of the input resistors and capacitors may need to be adjusted or some components may need to be removed. Table 9 displays recommended values to set the RC network for different input frequency ranges. However, these values are dependent on the input signal and bandwidth and should be used only as a starting guide. Note that the values given in Table 9 are for each R1, R2, C2, and R3 component shown in Figure 50 and Figure 51.

Table 9. Example RC Network

Frequency Range (MHz)	R1 Series (Ω)	C1 Differential (pF)	R2 Series (Ω)	C2 Shunt (pF)	R3 Shunt (Ω)
0 to 100	33	8.2	0	8.2	49.9
100 to 250	15	3.9	0	Open	Open

An alternative to using a transformer-coupled input at frequencies in the second Nyquist zone is to use the AD8376 variable gain amplifier. An example drive circuit including a band-pass filter is shown in Figure 52. See the AD8376 data sheet for more information.

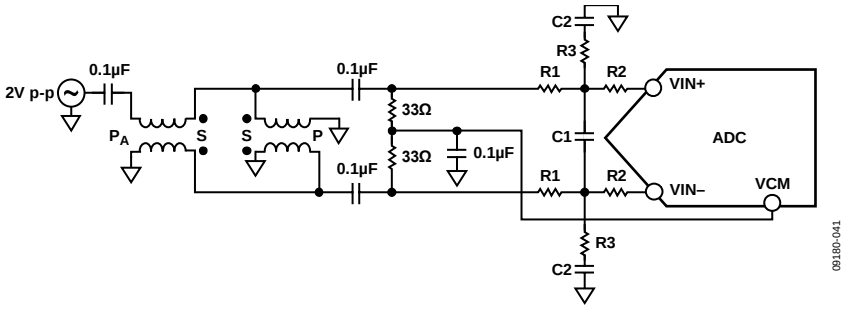


Figure 51. Differential Double Balun Input Configuration

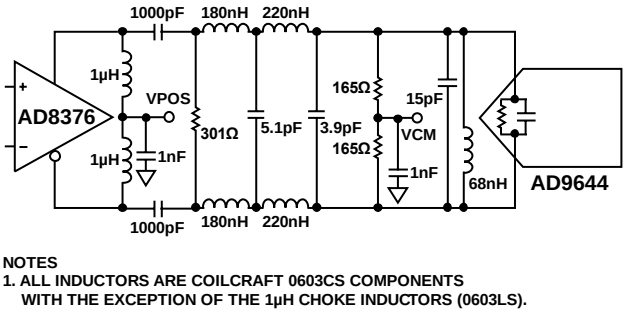


Figure 52. Differential Input Configuration Using the AD8376 (Filter Values Shown Are for a 20 MHz Bandwidth Filter Centered at 140 MHz)

VOLTAGE REFERENCE

A stable and accurate voltage reference is built into the AD9644. The input full scale range can be adjusted through the SPI port by adjusting Bit 0 through Bit 4 of Register 0x18. These bits can be used to change the full scale between 1.383 V p-p and 2.087 V p-p in 0.022 V steps, as shown in Table 17.

CLOCK INPUT CONSIDERATIONS

For optimum performance, the AD9644 sample clock inputs, CLK+ and CLK–, should be clocked with a differential signal. The signal is typically ac-coupled into the CLK+ and CLK– pins by means of a transformer or a passive component configuration. These pins are biased internally (see Figure 53) and require no external bias. If the inputs are floated, the CLK– pin is pulled low to prevent inadvertent clocking.

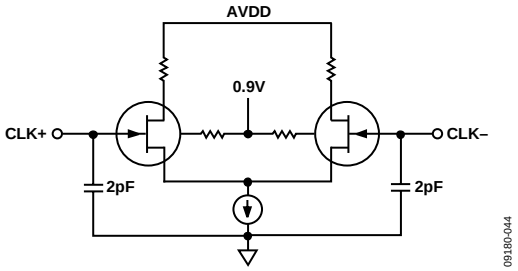


Figure 53. Equivalent Clock Input Circuit

Clock Input Options

The AD9644 has a very flexible clock input structure. Clock input can be a CMOS, LVDS, LVPECL, or sine wave signal. Regardless of the type of signal being used, clock source jitter is of the most concern, as described in the Jitter Considerations section. The minimum conversion rate of the AD9644 is 40 MSPS. At clock rates below 40 MSPS, dynamic performance of the AD9644 can degrade.

Figure 54 and Figure 55 show two preferred methods for clocking the AD9644 (at clock rates up to 640 MHz). A low jitter clock source is converted from a single-ended signal to a differential signal using either an RF balun or an RF transformer.

The RF balun configuration is recommended for clock frequencies between 125 MHz and 640 MHz, and the RF transformer is recommended for clock frequencies from 40 MHz to 200 MHz. The back-to-back Schottky diodes across the transformer/balun secondary limit clock excursions into the AD9644 to approximately 0.8 V p-p differential.

This limit helps prevent the large voltage swings of the clock from feeding through to other portions of the AD9644 while preserving the fast rise and fall times of the signal that are critical to a low jitter performance.

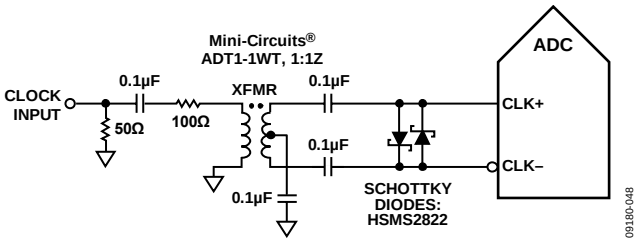


Figure 54. Transformer-Coupled Differential Clock (Up to 200 MHz)

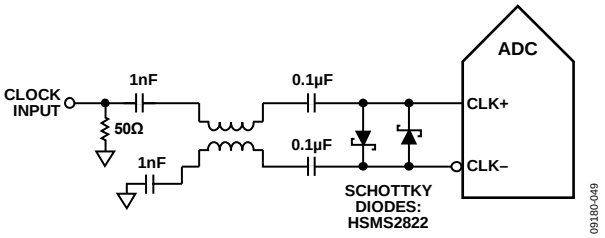


Figure 55. Balun-Coupled Differential Clock (Up to 640 MHz)

If a low jitter clock source is not available, another option is to ac couple a differential PECL signal to the sample clock input pins, as shown in Figure 56. The AD9510/AD9511/AD9512/AD9513/AD9514/AD9515/AD9516/AD9517/AD9518/AD9520/AD9522 clock drivers offer excellent jitter performance.

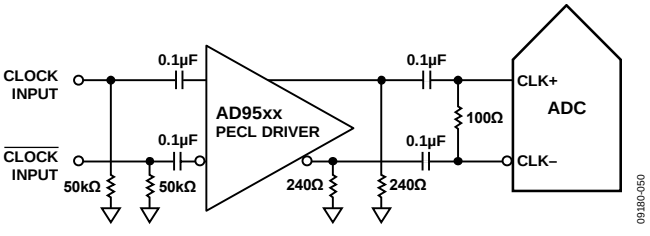


Figure 56. Differential PECL Sample Clock (Up to 640 MHz)

A third option is to ac-couple a differential LVDS signal to the sample clock input pins, as shown in Figure 57. The AD9510/AD9511/AD9512/AD9513/AD9514/AD9515/AD9516/AD9517/AD9518/AD9520/AD9522 clock drivers offer excellent jitter performance.

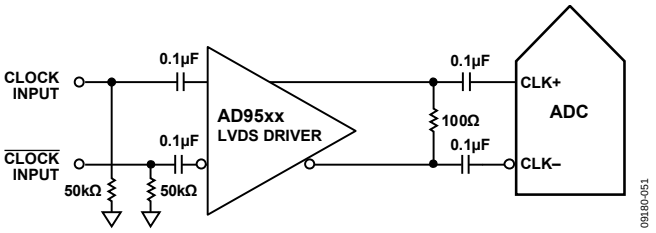


Figure 57. Differential LVDS Sample Clock (Up to 640 MHz)

In some applications, it may be acceptable to drive the sample clock inputs with a single-ended CMOS signal. In such applications, the CLK+ pin should be driven directly from a CMOS gate, and the CLK– pin should be bypassed to ground with a 0.1 µF capacitor (see Figure 58).

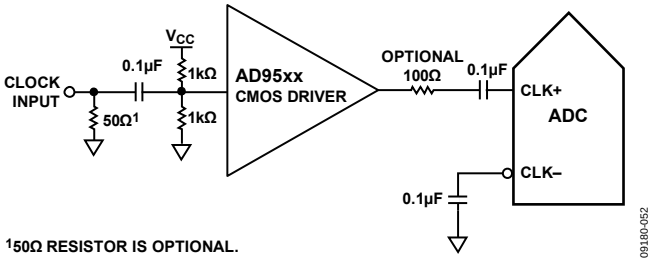


Figure 58. Single-Ended 1.8 V CMOS Input Clock (Up to 200 MHz)

Input Clock Divider

The AD9644 contains an input clock divider with the ability to divide the input clock by integer values between 1 and 8. For divide ratios other than 1 the duty cycle stabilizer is automatically enabled.

The AD9644 clock divider can be synchronized using the external SYNC input. Bit 1 and Bit 2 of Register 0x3A allow the clock divider to be resynchronized on every SYNC signal or only on the first SYNC signal after the register is written. A valid SYNC causes the clock divider to reset to its initial state. This synchronization feature allows multiple parts to have their clock dividers aligned to guarantee simultaneous input sampling.

Clock Duty Cycle

Typical high speed ADCs use both clock edges to generate a variety of internal timing signals and, as a result, may be sensitive to clock duty cycle. The AD9644 requires a tight tolerance on the clock duty cycle to maintain dynamic performance characteristics.

The AD9644 contains a duty cycle stabilizer (DCS) that retimes the nonsampling (falling) edge, providing an internal clock signal with a nominal 50% duty cycle. This allows the user to provide a wide range of clock input duty cycles without affecting the performance of the AD9644. Noise and distortion performance are nearly flat for a wide range of duty cycles with the DCS enabled.

Jitter in the rising edge of the input is still of paramount concern and is not easily reduced by the internal stabilization circuit. The loop has a time constant associated with it that must be considered in applications in which the clock rate can change dynamically. A wait time of 1.5 µs to 5 µs is required after a dynamic clock frequency increase or decrease before the DCS loop is relocked to the input signal. During the time period that the loop is not locked, the DCS loop is bypassed, and internal device timing is dependent on the duty cycle of the input clock signal. In such applications, it may be appropriate to disable the duty cycle stabilizer. In all other applications, enabling the DCS circuit is recommended to maximize ac performance.

Jitter Considerations

High speed, high resolution ADCs are sensitive to the quality of the clock input. For inputs near full scale, the degradation in SNR from the low frequency SNR (SNR_{LF}) at a given input frequency (f_{INPUT}) due to jitter (t_{JRMS}) can be calculated by

$$SNR_{HF} = -10 \log[(2\pi \times f_{INPUT} \times t_{JRMS})^2 + 10^{(-SNR_{LF}/10)}]$$

In the equation, the rms aperture jitter represents the clock input jitter specification. IF undersampling applications are particularly sensitive to jitter, as illustrated in Figure 59. The measured curve in Figure 59 was taken using an ADC clock source with approximately 65 fs of jitter, which combines with the 125 fs of jitter inherent in the AD9644 to produce the result shown.

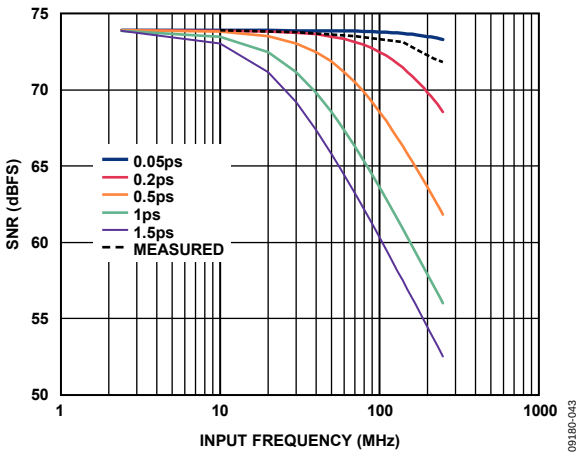


Figure 59. SNR vs. Input Frequency and Jitter

The clock input should be treated as an analog signal in cases in which aperture jitter may affect the dynamic range of the AD9644. Power supplies for clock drivers should be separated from the ADC output driver supplies to avoid modulating the clock signal with digital noise. Low jitter, crystal-controlled oscillators make the best clock sources. If the clock is generated from another type of source (by gating, dividing, or another method), it should be retimed by the original clock at the last step.

Refer to the AN-501 Application Note and the AN-756 Application Note (visit www.analog.com) for more information about jitter performance as it relates to ADCs.

CHANNEL/CHIP SYNCHRONIZATION

The AD9644 has a SYNC input that offers the user flexible synchronization options for synchronizing the clock divider. The clock divider sync feature is useful for guaranteeing synchronized sample clocks across multiple ADCs. The input clock divider can be enabled to synchronize on a single occurrence of the SYNC signal or on every occurrence.

The SYNC input is internally synchronized to the sample clock; however, to ensure that there is no timing uncertainty between multiple parts, the SYNC input signal should be externally synchronized to the input clock signal, meeting the setup and hold times shown in Table 5. The SYNC input should be driven using a single-ended CMOS-type signal.

POWER DISSIPATION AND STANDBY MODE

As shown in Figure 60 and Figure 61, the power dissipated by the AD9644 varies with its sample rate (AD9644-80 shown).

The data in Figure 60 and Figure 61 was taken in JESD204A serial output mode, using the same operating conditions as those used for the Typical Performance Characteristics.

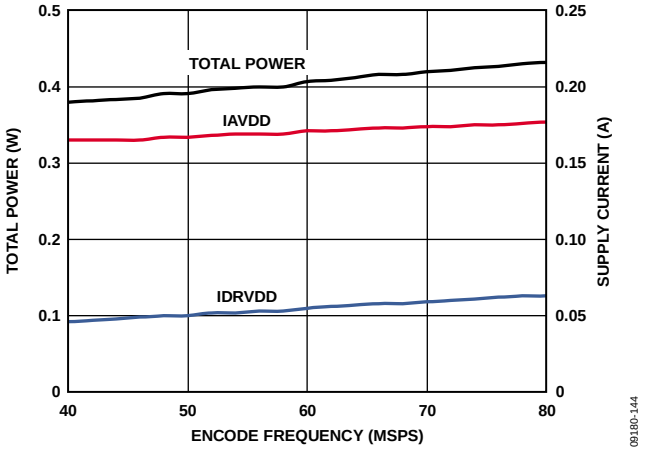


Figure 60. AD9644-80 Power and Current vs. Encode Frequency with f_{IN} = 10.1 MHz

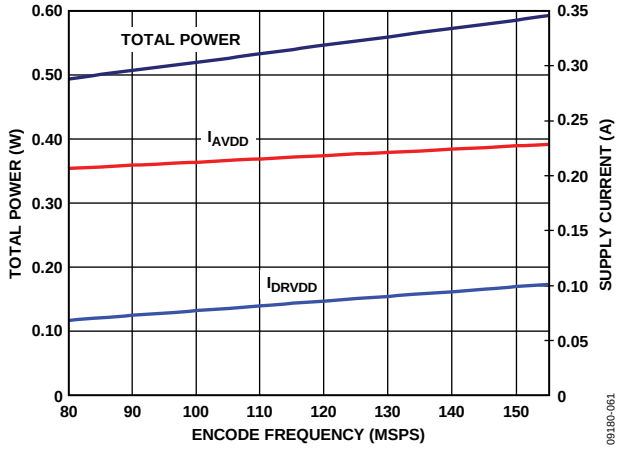


Figure 61. AD9644-155 Power and Current vs. Encode Frequency with f_{IN} = 10.1 MHz

By asserting PDWN (either through the SPI port or by asserting the PDWN pin high), the AD9644 is placed in power-down mode. In this state, the ADC typically dissipates 15 mW. During power-down, the output drivers are placed in a high impedance state. Asserting the PDWN pin low returns the AD9644 to its normal operating mode.

Low power dissipation in power-down mode is achieved by shutting down the reference, reference buffer, biasing networks, clock, and JESD204A outputs . Internal capacitors are discharged when entering power-down mode and then must be recharged when returning to normal operation.

When using the SPI port interface, the user can place the ADC in power-down mode or standby mode. Standby mode allows the user to keep the internal reference circuitry powered and the JESD204A outputs running when faster wake-up times are required.

DIGITAL OUTPUTS

JESD204A Transmit Top Level Description

The AD9644 digital output complies with the JEDEC Standard No. 204A (JESD204A), which describes a serial interface for data converters. JESD204A uses 8B/10B encoding as well as optional scrambling. K28.5 and K28.7 comma symbols are used for frame synchronization and the K28.3 control symbol is used for lane synchronization. The receiver is required to lock onto the serial data stream and recover the clock with the use of a PLL. For details on the output interface, users are encouraged to refer to the JESD204A standard.

The JESD204A transmit block is used to multiplex data from the two analog-to-digital converters onto two independent JESD204A Links. Each JESD204A Link is considered a separate instance of the JESD204A specification, has an independent DSYNC signal, and contains one or more lanes. Note that the JESD204 specification only allows one lane per link, while the JESD204A specification adds multilane support through an alignment procedure.

Each JESD204A Link is described according to the following nomenclature:

- S = samples transmitted/single converter/frame cycle
- M = number of converters/converter device (link)
- L = number of lanes/converter device (link)
- N = converter resolution
- N' = total number of bits per sample
- CF = number of control words/frame clock cycle/converter device (link)
- CS = number of control bits/conversion sample
- K = number of frames per multiframe
- HD = high density mode
- F = octets/frame
- C = control bit (overrange, overflow, underflow)
- T = tail bit
- SCR = scrambler enable/disable
- FCHK = checksum

Figure 62 shows a simplified block diagram of the AD9644 JESD204A links. The two links each have a primary and a secondary converter input and lane output. By default, the primary Input 0 of Link A is ADC Converter A and its primary lane Output 0 is sent on output Lane A. The primary Input 0 of Link B is ADC Converter B and its primary lane Output 0 is sent on output Lane B. Muxes throughout the design are used to enable secondary inputs/outputs and swap lane outputs for other configurations. The JESD204A block for AD9644 is designed to support the configurations described in Table 10 via a quick configuration register at Address 0x5E accessible via the SPI bus.

In addition to the default mode, the user can program the AD9644 to output both ADC channels on a single lane (F = 4). This mode allows use of a single high speed data lane, which simplifies board layout and connector requirements. In Figure 64 the ADC A output is represented by Word 0 and the ADC B output by Word 1. The third output mode utilizes a single link to support both channels. In single link mode, the DSYNCA pin is used to support both outputs. This mode is useful for optimal alignment between the output channels.

The 8B/10B encoding works by taking eight bits of data (an octet) and encoding them into a 10-bit symbol. By default in the AD9644, the 14-bit converter word is broken into two octets. Bit 13 through Bit 6 are in the first octet. The second octet contains Bit 5 through Bit 0 and two tail bits. The MSB of the tail bits can also be used to indicate an out-of-range condition. The tail bits are configured using the JESD204A link control Register 1, Address 0x60, Bit 6.

The two resulting octets are optionally scrambled and encoded into their corresponding 10-bit code. The scrambling function is controlled by the JESD204A scrambling and lane configuration register, Address 0x06E, Bit 7. Figure 63 shows how the 14-bit data is taken from the ADC, the tail bits are added, the two octets are scrambled, and how the octets are encoded into two 10-bit symbols. Figure 63 illustrates the default data format.

The scrambler uses a self-synchronizing polynomial-based algorithm defined by the equation $1 + x^{14} + x^{15}$. The descrambler in the receiver should be a self-synchronizing version of the scrambler polynomial. Figure 65 shows the corresponding receiver data path.

Refer to JEDEC Standard No. 204A-April 2008, Section 5.1, for complete transport layer and data format details and Section 5.2 for a complete explanation of scrambling and descrambling.

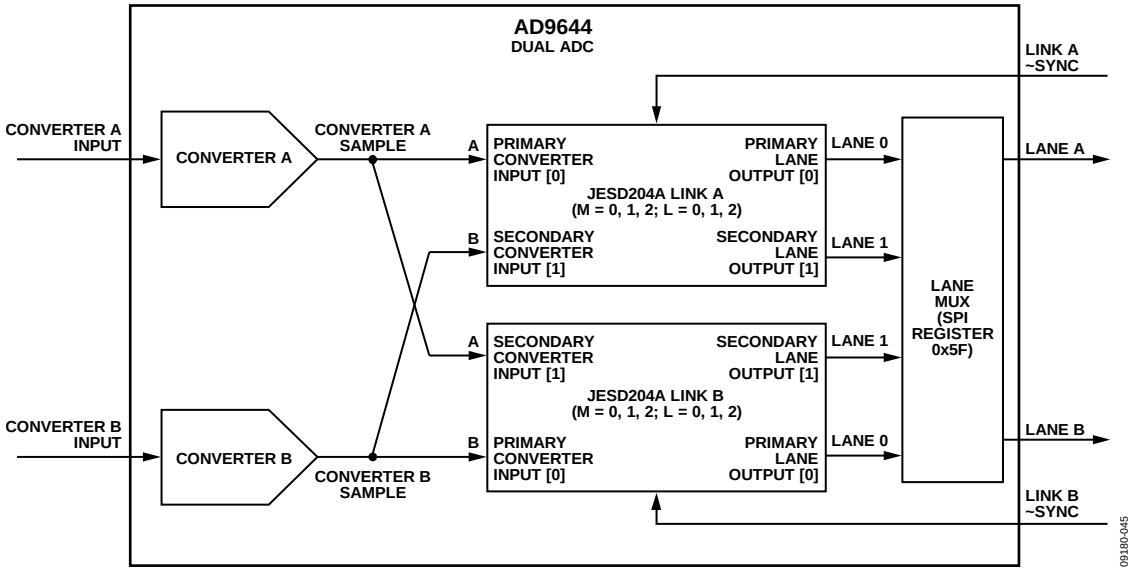


Figure 62. AD9644 Transmit Link Simplified Block Diagram

Table 10. AD9644 JESD204A Typical Configurations

AD9644 Configuration	JESK204A Link A Settings	JESD204A Link B Settings	Comments
Two Converters Two JESD204A Links One Lane Per Link	M = 1; L = 1; S = 1; F = 2 N′ = 16; CF = 0 CS = 0, 1, 2; K = N/A SCR = 0, 1; HD = 0	M = 1; L = 1; S = 1; F = 2 N′ = 16; CF = 0 CS = 0, 1, 2; K = N/A SCR = 0, 1; HD = 0	Maximum sample rate = 80 MSPS or 155 MSPS
Two Converters One JESD204A Link Two Lanes Per Link	M = 2; L = 2; S = 1; F = 2 N′ = 16 CF = 0; CS = 0, 1, 2 K = 16; SCR = 0, 1; HD = 0	Disabled	Maximum sample rate = 80 MSPS or 155 MSPS Required for applications needing two aligned samples (I/Q applications)
Two Converters One JESD204A Link One Lane Per Link	M = 2; L = 1; S = 1; F = 4 N′ = 16 CF = 0; CS = 0, 1, 2 K = 8; SCR = 0, 1; HD = 0	Disabled	Maximum sample rate = 80 MSPS

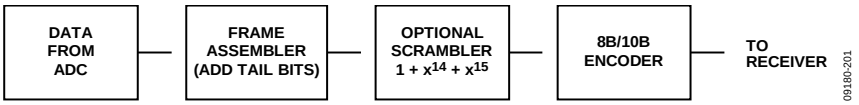


Figure 63. AD9644 ADC Output Data Path

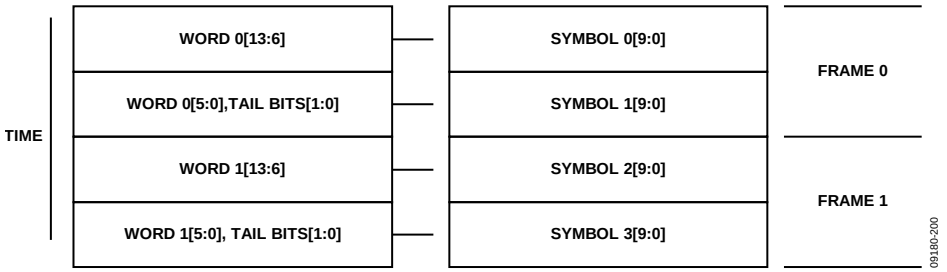


Figure 64. AD9644 14-Bit Data Transmission with Tail Bits

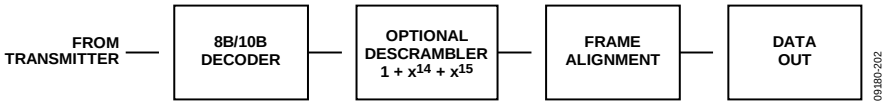


Figure 65. Required Receiver Data Path

Initial Frame Synchronization

The serial interface must synchronize to the frame boundaries before data can be properly decoded. The JESD204A standard has a synchronization routine to identify the frame boundary. When the DSYNC pin is taken low for at least two clock cycles, the AD9644 enters the code group synchronization mode. The AD9644 transmits the K28.5 comma symbol until the receiver achieves synchronization. The receiver should then deassert the sync signal (take DSYNC high) and the AD9644 begins the initial lane alignment sequence (when enabled through Bits[3:2] of Address 0x60) and subsequently begins transmitting sample data. The first non-K28.5 symbol corresponds to the first octet in a frame.

The DSYNC input can be driven either from a differential LVDS source or by using a single-ended CMOS driver circuit. The DSYNC input default to LVDS mode but can be set to CMOS mode by setting Bit 4 in SPI Address 0x61. If it is driven differentially from an LVDS source, then an external 100 Ω termination resistor should be provided. If the DSYNC input is driven single-ended then the CMOS signal should be connected to the DSYNC+ signal and the DSYNC– signal should be left disconnected.

Table 11. AD9644 JESD204A Frame Alignment Monitoring and Correction Replacement Characters

Scrambling	Lane Synchronization	Character to be Replaced	Last Octet in Multiframe	Replacement Character
Off	On	Last octet in frame repeated from previous frame	No	K28.7 (0xFC)
Off	On	Last octet in frame repeated from previous frame	Yes	K28.3 (0x7C)
Off	Off	Last octet in frame repeated from previous frame	Not applicable	K28.7 (0xFC)
On	On	Last octet in frame equals D28.7 (0xFC)	No	K28.7 (0xFC)
On	On	Last octet in frame equals D28.3 (0x7C)	Yes	K28.3 (0x7C)
On	Off	Last octet in frame equals D28.7 (0x7C)	Not applicable	K28.7 (0xFC)

Frame and Lane Alignment Monitoring and Correction

Frame alignment monitoring and correction is part of the JESD204A specification. The 14-bit word requires two octets to transmit all the data. The two octets (MSB and LSB), where F = 2, make up a frame. During normal operating conditions frame alignment is monitored via alignment characters, which are inserted under certain conditions at the end of a frame. Table 11 summarizes the conditions for character insertion along with the expected characters under the various operation modes. If lane synchronization is enabled, the replacement character value depends on whether the octet is at the end of a frame or at the end of a multiframe.

Based on the operating mode, the receiver can ensure that it is still synchronized to the frame boundary by correctly receiving the replacement characters.

Digital Outputs and Timing

The AD9644 has differential digital outputs that power up by default. The driver current is derived on chip and sets the output current at each output equal to a nominal 4 mA. Each output presents a 100 Ω dynamic internal termination to reduce unwanted reflections.

A 100 Ω differential termination resistor should be placed at each receiver input to result in a nominal 400 mV peak-to-peak swing at the receiver (see Figure 66). Alternatively, single-ended 50 Ω termina-tion can be used. When single-ended termination is used, the termination voltage should be DRVDD/2; otherwise, ac coupling capacitors can be used to terminate to any single-ended voltage.

The AD9644 digital outputs can interface with custom ASICs and FPGA receivers, providing superior switching performance in noisy environments. Single point-to-point network topologies are recommended with a single differential 100 Ω termination resistor placed as close to the receiver logic as possible. The common mode of the digital output automatically biases itself to half the supply of the receiver (that is, the common-mode voltage is 0.9 V for a receiver supply of 1.8 V) if dc-coupled connecting is used (see Figure 67). For receiver logic that is not within the bounds of the DRVDD supply, an ac-coupled connection should be used. Simply place a 0.1 µF capacitor on each output pin and derive a 100 Ω differential termination close to the receiver side.

If there is no far-end receiver termination or if there is poor differential trace routing, timing errors may result. To avoid such timing errors, it is recommended that the trace length be less than six inches and that the differential output traces be close together and at equal lengths.

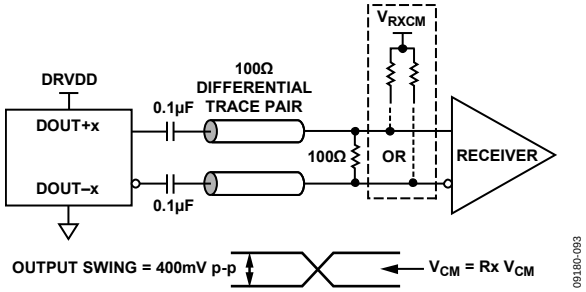


Figure 66. AC-Coupled Digital Output Termination Example

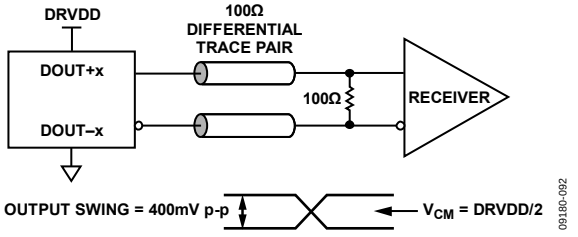


Figure 67. DC-Coupled Digital Output Termination Example

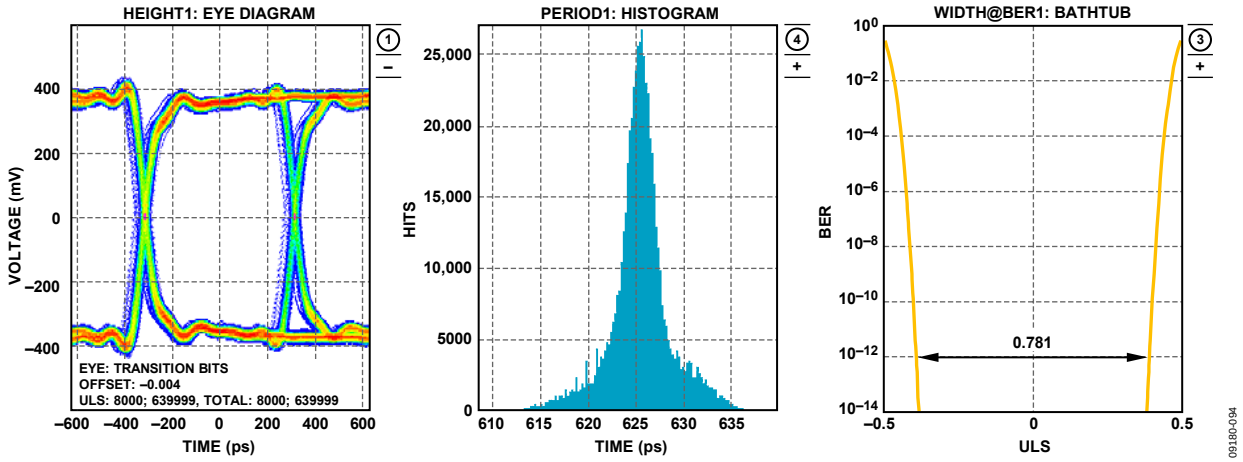


Figure 68. AD9644-80 Digital Outputs Data Eye, Histogram and Bathtub, External 100 Ω Terminations

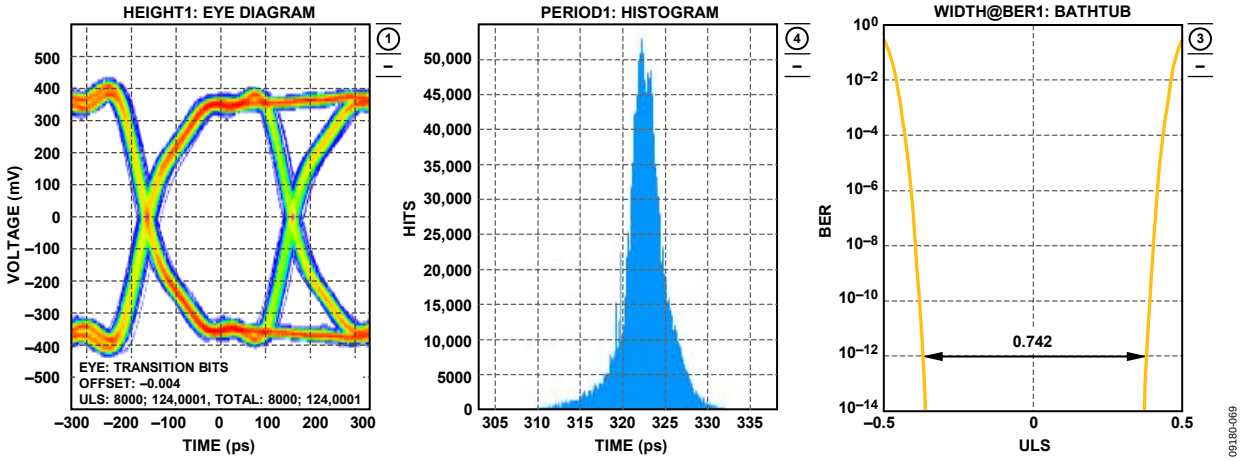


Figure 69. AD9644-155 Digital Outputs Data Eye, Histogram and Bathtub, External 100 Ω Terminations

Figure 68 and Figure 69 shows an example of the digital output (default) data eye and a time interval error (TIE) jitter histogram.

Additional SPI options allow the user to further increase the output driver voltage swing of all four outputs to drive longer trace lengths (see Address 0x15 in Table 17). Even though this produces sharper rise and fall times on the data edges and is less prone to bit errors, the power dissipation of the DRVDD supply increases when this option is used. See the Memory Map section for more details.

The format of the output data is twos complement by default. Table 12 provides an example of this output coding format. To change the output data format to offset binary or gray code, see the Memory Map section (Address 0x14 in Table 17).

Table 12. Digital Output Coding

Code	(VIN+) – (VIN–), Input Span = 1.75 V p-p (V)	Digital Output Twos Complement ([D13:D0])
8191	+0.875	01 1111 1111 1111
0	0.00	00 0000 0000 0000
–1	–0.000107	11 1111 1111 1111
–8192	–0.875	10 0000 0000 0000

The lowest typical clock rate is 40 MSPS. For clock rates slower than 60 MSPS, the user should set Bit 3 to 0 in the serial control register (Address 0x21 in Table 17). This option sets the PLL loop bandwidth to use clock rates between 40 MSPS and 60 MSPS.

Setting Bit 2 in the output mode register (Address 0x14) allows the user to invert the digital samples from their nominal state. As shown in Figure 64, the MSB is transmitted first in the data output serial stream.

BUILT-IN SELF-TEST (BIST) AND OUTPUT TEST

The AD9644 includes built-in test features designed to enable verification of the integrity of each channel as well as facilitate board level debugging. A BIST (built-in self-test) feature is included that verifies the integrity of the digital datapath of the AD9644. Various output test options are also provided to place predictable values on the outputs of the AD9644.

BUILT-IN SELF-TEST (BIST)

The BIST is a thorough test of the digital portion of the selected AD9644 signal path. When enabled, the test runs from an internal pseudorandom noise (PN) source through the digital datapath starting at the ADC block output. The BIST sequence runs for 512 cycles and stops. The BIST signature value for Channel A and/or Channel B is placed in Register 0x24 and Register 0x25. The outputs are not disconnected during this test, so the PN sequence can be observed as it runs. The PN sequence can be continued from its last value or reset from the beginning, based on the value programmed in Register 0x0E, Bit 2. The BIST signature result varies based on the channel configuration.

OUTPUT TEST MODES

Digital Test patterns can be inserted at various points along the signal path within the AD9644 as shown in Figure 70. The ability to inject these signals at several locations facilitates debugging of the JESD204A serial communication link.

The Register 0x0D allows test signals generated at the output of the ADC core to be fed directly into the input of the serial Link. The output test options available from Register 0x0D are shown in Table 17. When an output test mode is enabled, the analog section of the ADC is disconnected from the digital back end blocks and the test pattern is run through the output formatting block. Some of the test patterns are subject to output formatting, and some are not. The seed value for the PN sequence tests can be forced if the PN reset bits are used to hold the generator in reset mode by setting Bit 4 or Bit 5 of Register 0x0D. These tests can be performed with or without an analog signal (if present, the analog signal is ignored), but they do require an encode clock.

For more information, see the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*.

There are nine digital output test pattern options available that can be initiated through the SPI (see Table 14 for the output bit sequencing options). This feature is useful when validating receiver capture and timing. Some test patterns have two serial sequential words and can be alternated in various ways, depending on the test pattern selected. Note that some patterns do not adhere to the data format select option. In addition, custom user-defined test patterns can be assigned in the user pattern registers (Address 0x19 through Address 0x20).

The PN sequence short pattern produces a pseudorandom bit sequence that repeats itself every $2^9 - 1$ (511) bits. A description of the PN sequence short and how it is generated can be found in Section 5.1 of the ITU-T O.150 (05/96) recommendation. The only difference is that the starting value must be a specific value instead of all 1s (see Table 13 for the initial values).

The PN sequence long pattern produces a pseudorandom bit sequence that repeats itself every $2^{23} - 1$ (8,388,607) bits. A description of the PN sequence long and how it is generated can be found in Section 5.6 of the ITU-T O.150 (05/96) standard. The only differences are that the starting value must be a specific value instead of all 1s (see Table 13 for the initial values) and that the AD9644 inverts the bit stream with relation to the ITU-T standard.

Table 13. PN Sequence

Sequence	Initial Value	First Three Output Samples (MSB First)
PN Sequence Short	0x0092	0x125B, 0x3C9A, 0x2660
PN Sequence Long	0x3AFF	0x3FD7, 0x0002, 0x36E0

The Register 0x62 allows patterns similar to those described in Table 14 to be input at different points along the data path. This allows the user to provide predictable output data on the serial link without it having been manipulated by the internal formatting logic. Refer to Table 17 for additional information on the test modes available in Register 0x62.

Table 14. Flexible Output Test Modes from SPI Register 0x0D

Output Test Mode Bit Sequence	Pattern Name	Digital Output Word 1 (Default Twos Complement Format)	Digital Output Word 2 (Default Twos Complement Format)	Subject to Data Format Select
0000	Off (default)	Not applicable	Not applicable	Yes
0001	Midscale short	00 0000 0000 0000	Same	Yes
0010	+Full-scale short	01 1111 1111 1111	Same	Yes
0011	−Full-scale short	10 0000 0000 0000	Same	Yes
0100	Checkerboard	10 1010 1010 1010	01 0101 0101 0101	No
0101	PN sequence long	Not applicable	Not applicable	Yes
0110	PN sequence short	Not applicable	Not applicable	Yes
0111	One-/zero-word toggle	1111 1111 1111	0000 0000 0000	No
1000	User test mode	User data from Register 0x19 to Register 0x20	User data from Register 0x19 to Register 0x20	Yes
1001 to 1110	Not used	Not applicable	Not applicable	
1111	Ramp output	N	N + 1	No

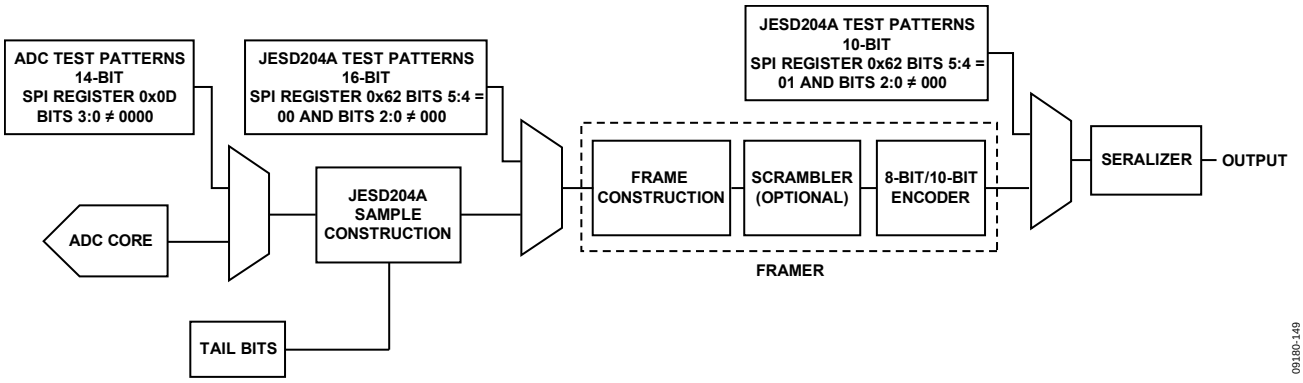


Figure 70. Block Diagram Showing Digital Test Modes

SERIAL PORT INTERFACE (SPI)

The AD9644 serial port interface (SPI) allows the user to configure the converter for specific functions or operations through a structured register space provided inside the ADC. The SPI gives the user added flexibility and customization, depending on the application. Addresses are accessed via the serial port and can be written to or read from via the port. Memory is organized into bytes that can be further divided into fields, which are documented in the Memory Map section. For detailed operational information, see the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*.

CONFIGURATION USING THE SPI

Three pins define the SPI of this ADC: the SCLK pin, the SDIO pin, and the CSB pin (see Table 15). The SCLK (a serial clock) is used to synchronize the read and write data presented from and to the ADC. The SDIO (serial data input/output) is a dual-purpose pin that allows data to be sent to and read from the internal ADC memory map registers. The CSB (chip select bar) is an active-low control that enables or disables the read and write cycles.

Table 15. Serial Port Interface Pins

Pin	Function
SCLK	Serial Clock. The serial shift clock input is used to synchronize serial interface reads and writes.
SDIO	Serial Data Input/Output. A dual-purpose pin that typically serves as an input or an output, depending on the instruction being sent and the relative position in the timing frame.
CSB	Chip Select Bar. An active-low control that gates the read and write cycles.

The falling edge of the CSB, in conjunction with the rising edge of the SCLK, determines the start of the framing. An example of the serial timing and its definitions can be found in Figure 71 and Table 5.

Other modes involving the CSB are available. The CSB can be held low indefinitely, which permanently enables the device; this is called streaming. The CSB can stall high between bytes to allow for additional external timing. When CSB is tied high, SPI functions are placed in high impedance mode.

During an instruction phase, a 16-bit instruction is transmitted. Data follows the instruction phase, and its length is determined by the W0 and W1 bits.

In addition to word length, the instruction phase determines whether the serial frame is a read or write operation, allowing the serial port to be used both to program the chip and to read the contents of the on-chip memory. The first bit of the first byte in a multibyte serial data transfer frame indicates whether a read command or a write command is issued. If the instruction is a readback operation, performing a readback causes the serial data input/output (SDIO) pin to change direction from an input to an output at the appropriate point in the serial frame.

All data is composed of 8-bit words. Data can be sent in MSB-first mode or in LSB-first mode. MSB first is the default on power-up and can be changed via the SPI port configuration register. For more information about this and other features, see the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*.

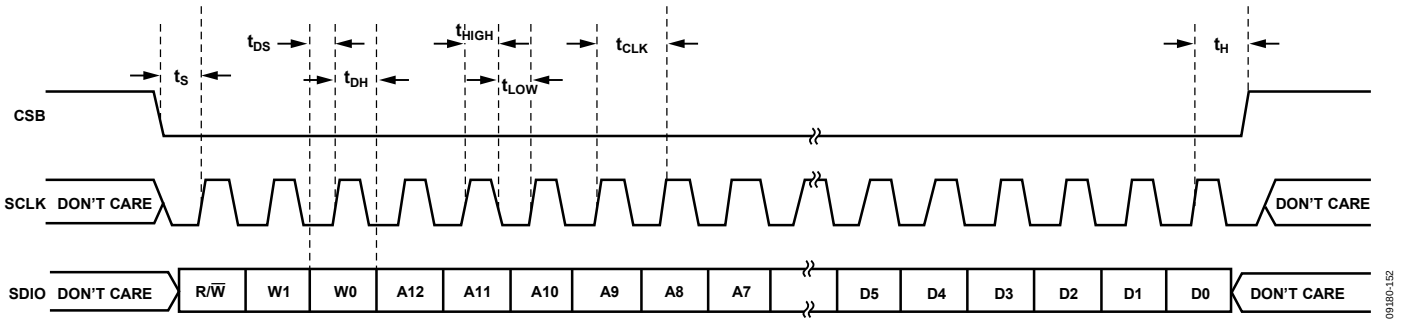


Figure 71. Serial Port Interface Timing Diagram

HARDWARE INTERFACE

The pins described in Table 15 comprise the physical interface between the user programming device and the serial port of the AD9644. The SCLK pin and the CSB pin function as inputs when using the SPI interface. The SDIO pin is bidirectional, functioning as an input during write phases and as an output during readback.

The SPI interface is flexible enough to be controlled by either FPGAs or microcontrollers. One method for SPI configuration is described in detail in the AN-812 Application Note, *Microcontroller-Based Serial Port Interface (SPI) Boot Circuit*.

The SPI port should not be active during periods when the full dynamic performance of the converter is required. Because the SCLK signal, the CSB signal, and the SDIO signal are typically asynchronous to the ADC clock, noise from these signals can degrade converter performance. If the on-board SPI bus is used for other devices, it may be necessary to provide buffers between this bus and the AD9644 to prevent these signals from transitioning at the converter inputs during critical sampling periods.

SPI ACCESSIBLE FEATURES

Table 16 provides a brief description of the general features that are accessible via the SPI. These features are described in detail in the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*. The AD9644 part-specific features are described in detail in the Memory Map Register Descriptions section.

Table 16. Features Accessible Using the SPI

Feature Name	Description
Mode	Allows the user to set either power-down mode or standby mode
Clock	Allows the user to access the DCS, set the clock divider, set the clock divider phase, and enable the sync
Offset	Allows the user to digitally adjust the converter offset
Test I/O	Allows the user to set test modes to have known data on output bits
Full Scale	Allows the user to set the input full scale voltage
JESD204A	Allows user to configure the JESD204A output

MEMORY MAP

READING THE MEMORY MAP REGISTER TABLE

Each row in the memory map register table has eight bit locations. The memory map is roughly divided into four sections: the chip configuration registers (Address 0x00 to Address 0x02); the channel index and transfer registers (Address 0x05 and Address 0xFF); the ADC functions registers, including setup, control, and test (Address 0x08 to Address 0x3A); and the JESD204A configuration registers (Address 0x5E to Address 0x79).

The memory map register table (see Table 17) lists the default hexadecimal value for each hexadecimal address shown. The column with the heading Bit 7 (MSB) is the start of the default hexadecimal value given. For example, Address 0x18, the input span select register, has a hexadecimal default value of 0x00. This means that Bit 0 through Bit 4 = 0, and the remaining bits are 0s. This setting is the default reference selection setting. The default value uses a 1.75 V p-p reference. For more information on this function and others, see the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*. This application note details the functions con-trolled by Register 0x00 to Register 0xFF.

Open Locations

All address and bit locations that are not included in Table 17 are not currently supported for this device. Unused bits of a valid address location should be written with 0s. Writing to these locations is required only when part of an address location is open (for example, Address 0x18). If the entire address location is open (for example, Address 0x13), this address location should not be written.

Default Values

After the AD9644 is reset, critical registers are loaded with default values. The default values for the registers are given in the memory map register table, Table 17.

Logic Levels

An explanation of logic level terminology follows:

- "Bit is set" is synonymous with "bit is set to Logic 1" or "writing Logic 1 for the bit."
- "Clear a bit" is synonymous with "bit is set to Logic 0" or "writing Logic 0 for the bit."

Transfer Register Map

Address 0x08 through Address 0x79 are shadowed. Writes to these addresses do not affect part operation until a transfer command is issued by writing 0x01 to Address 0xFF, setting the transfer bit. This allows these registers to be updated internally and simultaneously when the transfer bit is set. The internal update takes place when the transfer bit is set, and the bit autoclears.

Channel-Specific Registers

Some channel setup functions, such as the channel output mode, can be programmed differently for each ADC or link channel. In these cases, channel address locations are internally duplicated for each channel. These registers and bits are designated in Table 17 as local. These local registers and bits can be accessed by setting the appropriate Channel A/Link A or Channel B/Link B bits in Register 0x05.

If both bits are set in register 0x05, the subsequent write affects the registers of both channels/links. In a SPI read cycle, only Channel A/Link A or Channel B/Link B should be set to read one of the two registers. If both bits are set during an SPI read cycle, the part returns the value for Channel A/Link A. Registers and bits designated as global in Table 17 affect the entire part or the channel features for which independent settings are not allowed between channels. The settings in Register 0x05 do not affect the global registers and bits.

MEMORY MAP REGISTER TABLE

All address and bit locations that are not included in Table 17 are not currently supported for this device.

Table 17. Memory Map Registers

Addr (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value (Hex)	Default/ Comments
Chip Configuration Registers											
0x00	SPI port configuration (global)[1]	0	LSB first	Soft reset	1	1	Soft reset	LSB first	0	0x18	Nibbles are mirrored so that LSB-first or MSB-first mode is set correctly, regardless of shift mode. To control this register, all channel index bits in Register 0x05 must be set.
0x01	Chip ID (global)	8-bit chip ID[7:0] (AD9644 = 0x7E) (default)								0x7E	Read only
0x02	Chip grade (global)	Open	Open	Speed grade ID 00 = 80 MSPS 10 = 155 MSPS		Open	Open	Open	Open		Speed grade ID differentiates devices; read only
Channel Index and Transfer Registers											
0x05	Channel index (global)	Open	Open	Open	Open	Open	Open	ADC B and Link B (default)	ADC A and Link A (default)	0x03	Bits set to determine which device on the chip receives next write command; local registers only
0xFF	Transfer (global)	Open	Open	Open	Open	Open	Open	Open	Transfer	0x00	Synchro-nously transfers data from master shift register to slave
ADC Functions											
0x08	Power modes (local)	Open	Open	External power-down pin function (local) 0 = power-down 1 = standby	Open	Open	Open	Internal power-down mode (local) 00 = normal operation 01 = full power-down 10 = standby 11 = reserved		0x00	Determines various generic modes of chip operation
0x09	Global clock (global)	Open	Open	Open	Open	Open	Open	Open	Duty cycle stabilizer (default)	0x01	
0x0A	PLL status (global)	PLL Locked	Open	Open	Open	Open	Open	Open	Open	0x00	Read Only
0x0B	Clock divide (global)	Open	Open	Input clock divider phase adjust 000 = no delay 001 = 1 input clock cycle 010 = 2 input clock cycles 011 = 3 input clock cycles 100 = 4 input clock cycles 101 = 5 input clock cycles 110 = 6 input clock cycles 111 = 7 input clock cycles			Clock divide ratio 000 = divide by 1 001 = divide by 2 010 = divide by 3 011 = divide by 4 100 = divide by 5 101 = divide by 6 110 = divide by 7 111 = divide by 8			0x00	Clock divide values other than 000 automatically causes duty cycle stabilizer to become active

Addr (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value (Hex)	Default/ Comments
0x0D	Test mode (local)	User test mode control 0 = continuous/repeat pattern 1 = single pattern	Open	Reset PN long generator	Reset PN short generator	Output test mode 0000 = off (default) 0001 = midscale short 0010 = positive FS 0011 = negative FS 0100 = alternating checkerboard 0101 = PN long sequence 0110 = PN short sequence 0111 = one/zero word toggle 1000 = user test mode 1001 to 1110 = unused 1111 = ramp output				0x00	When this register is set, test data is used in place of normal ADC data
0x0E	BIST enable (global)	Open	Open	Open	Open	Open	Reset BIST sequence	Open	BIST enable	0x00	
0x10	Offset adjust (local)	Open	Open	Offset adjust in LSBs from +31 to −32 (twos complement format)						0x00	
0x14	Output mode	Open	Open	Open	Output disable (local)	Open	Output invert (local)	Output format 00 = offset binary 01 = twos complement (default) 10 = gray code 11 = offset binary (local)		0x01	Configures outputs and the format of the data
0x15	Output adjust (global)	Open	Open	Open	Open	Open	Open	Output drive level adjust 11 = 320 mV 00 = 400 mV 10 = 440 mV 01 = 500 mV		0x00	
0x18	Input span select (global)	Open	Open	Open	Full-scale input voltage selection 01111 = 2.087 V p-p … 00001 = 1.772 V p-p 00000 = 1.75 V p-p (default) 11111 = 1.727 V p-p … 10000 = 1.383 V p-p					0x00	Full-scale input adjustment in 0.022 V steps
0x19	User Test Pattern 1 LSB (global)	User Test Pattern 1 [7:0]								0x00	
0x1A	User Test Pattern 1 MSB (global)	User Test Pattern 1 [15:8]								0x00	
0x1B	User Test Pattern 2 LSB (global)	User Test Pattern 2 [7:0]								0x00	
0x1C	User Test Pattern 2 MSB (global)	User Test Pattern 2 [15:8]								0x00	
0x1D	User Test Pattern 3 LSB (global)	User Test Pattern 3 [7:0]								0x00	
0x1E	User Test Pattern 3 MSB (global)	User Test Pattern 3 [15:8]								0x00	
0x1F	User Test Pattern 4 LSB (global)	User Test Pattern 4 [7:0]								0x00	
0x20	User Test Pattern 4 MSB (global)	User Test Pattern 4 [15:8]								0x00	
0x21	PLL Control (global)	Open	Open	Open	Open	PLL Low encode rate enable	Open	Open	Open	0x00	Bit 3 must be enabled if ADC clock rate is less than 60 MSPS

Addr (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value (Hex)	Default/ Comments
0x24	BIST signature LSB (local)	BIST signature[7:0]								0x00	Read only
0x25	BIST signature MSB (local)	BIST signature[15:8]								0x00	Read only
0x3A	Sync control (global)	Open	Open	Open	Open	Open	Clock divider next sync only	Clock divider sync enable	Master sync buffer enable	0x00	
JESD204A Configuration Registers											
0x5E	JESD204A quick configure (global)	Open	Open	Open	Open	Open	000 = default—configuration determined by other registers 001 = two converters using two links with one lane per link 010 = two converters using one link with two lanes per link 011 = two converters using one link and a single lane 100 to 111: reserved			0x00	Changes settings of Address 0x5F to Address 0x60 and Address 0x6E to Address 0x72 (self clearing)
0x5F	JESD204A lane assignment (global)	Open	Open	Open	Open	JESD204A serial lane control 0000 = one lane per link. Link A: Lane 0 sent on Lane A, Link B: Lane 0 Sent on Lane B 0001 = one lane per link. Link A: Lane 0 sent on Lane B, Link B: Lane 0 Sent on Lane A. 0010 = two lanes per link. Link A: Lane 0, Lane 1 sent on Lane A, Lane B. Link B disabled. 0011 = two lanes per link. Link A: Lane 0, Lane 1 sent on Lane B, Lane A. Link B disabled. 0100 = two lanes per link. Link B: Lane 0, Lane 1 sent on Lane A, Lane B. Link A disabled. 0101 = two lanes per link. Link B: Lane 0, 1 sent on Lane B, Lane A. Link A disabled. 0110 to 1111: reserved			0x00	
0x60	JESD204A Link Control Register 1 (local)	Open	Serial tail bit enable	Serial test sample enable	Serial lane synchronization enable	Serial lane alignment sequence mode 00 = disabled 01 = enabled 10 = reserved 11 = always on test mode		Frame alignment character insertion disable	Serial transmit link powered down	0x00	
0x61	JESD204A Link Control Register 2 (local)	Local DSYNC mode 00 = individual mode 01 = global mode 10 = DSYNC active mode 11 = DSYNC pin disabled		DSYNC pin input inverted	CMOS DSYNC input 0 = LVDS 1 = CMOS	Open	Bypass 8b/10b encoding	Invert transmit bits	Mirror serial output bits	0x00	
0x62	JESD204A Link Control Register 3 (local)	Disable CHKSUM	Open	Link test generation input selection 00 = 16-bit data injected at sample input to the link 01 = 10-bit data injected at output of 8b/10b encoder 10 = reserved 11 = reserved		Open	Link test generation mode 000 = normal operation 001 = alternating checker board 010 = 1/0 word toggle 011 = PN sequence—long 100 = PN sequence—short 101 = user test pattern data continuous 110 = user test pattern data single 111 = ramp output			0x00	
0x63	JESD204A Link Control Register 4 (local)	Initial lane assignment sequence repeat count								0x00	
0x64	JESD204A device identification number (DID) (local)	JESD204A serial device identification (DID) number								0x00	

Addr (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value (Hex)	Default/ Comments
0x65	JESD204A bank identification number (BID) (local)	Open	Open	Open	Open	JESD204A serial bank identification number (BID)				0x00	
0x66	JESD204A lane identification number (LID) for Lane 0 (local)	Open	Open	Open	JESD204A serial lane identification (LID) number for Lane 0					0x00	
0x67	JESD204A lane identification number (LID) for Lane 1 (local)	Open	Open	Open	JESD204A serial lane identification (LID) number for Lane 1					0x01	
0x6E	JESD204A scrambler (SCR) and lane (L) configuration register	Enable serial scrambler mode (SCR) (local)	Open	Open	Open	Open	Open	Open	Lane control (global) 0 = one lane per link (L = 1) 1 = two lanes per link (L = 2)	0x80	
0x6F	JESD204A number of octets per frame (F) (global)	JESD204A number of octets per frame (F)—these bits are calculated based on the equation: F = M × (2 ÷ L)								0x01	Read only
0x70	JESD204A number of frames per multiframe (K) (local)	Open	Open	Open	JESD204A number of frames per multiframe (K)					0x0F	
0x71	JESD204A number of converters per link (M) (global)	Open	Open	Open	Open	Open	Open	Open	Number of converters per link (M) 0 = link connected to one ADC (M = 1) 1 = link connected to two ADCs (M = 2)	0x00	
0x72	JESD 204A ADC resolution (N) and control bits per sample (CS) (local)	Number of control bits per sample (CS) 00 = no control bits (CS = 0) 01 = one control bit (CS = 1) 10 = two control bits (CS = 2) 11 = unused		Open	Converter resolution (N) (read only)					0x4D	
0x73	JESD204A total bits per sample (N') (global)	Open	Open	Open	Total bits per sample (N') (read only)					0x0F	Read only
0x74	JESD204A samples per converter (S) frame cycle (global)	Open	Open	Open	Samples per converter (S) frame cycle (read only) Always 1 for the AD9644					0x00	Read only
0x75	JESD204A HD and CF configuration (global)	Enable high density format (HD = 0, read only)	Open	Open	Number of control words per frame clock cycle per Link (CF) – always 0 for the AD9644 (read only)					0x00	Read only

Addr (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value (Hex)	Default/ Comments
0x76	JESD204A serial reserved Field 1 (RES1)	Serial Reserved Field 1 (RES1) – these registers are available for customer use								0x00	
0x77	JESD204A serial reserved Field 2 (RES2)	Serial Reserved Field 2 (RES2) – these registers are available for customer use								0x00	
0x78	JESD204A checksum value (FCHK) for Lane 0 (local)	Serial checksum value for Lane 0 (FCHK)								0x00	Read only
0x79	JESD204A checksum value (FCHK) for lane 1 (local)	Serial checksum value for Lane 1 (FCHK)								0x00	Read only

[1] The channel index register at Address 0x05 should be set to 0x03 (default) when writing to Address 0x00.

MEMORY MAP REGISTER DESCRIPTIONS

For additional information about functions controlled in Register 0x00 to Register 0x25, see the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*.

Sync Control (Register 0x3A)

Bits[7:3]—Open

Bit 2—Clock Divider Next Sync Only

If the master sync buffer enable bit (Address 0x3A, Bit 0) and the clock divider sync enable bit (Address 0x3A, Bit 1) are high, Bit 2 allows the clock divider to sync to the first sync pulse it receives and to ignore the rest. The clock divider sync enable bit (Address 0x3A, Bit 1) resets after it syncs.

Bit 1—Clock Divider Sync Enable

Bit 1 gates the sync pulse to the clock divider. The sync signal is enabled when Bit 1 is high and Bit 0 is high. This is continuous sync mode.

Bit 0—Master Sync Buffer Enable

Bit 0 must be high to enable any of the sync functions. If the sync capability is not used this bit should remain low to conserve power.

JESD204A Quick Configure (Register 0x5E)

Bits[7:3]—Reserved

Bits[2:0]—Register Quick Configuration

Writes to Bits[2:0] of this register configure the part for the most popular modes of operation for the JESD204A link. The intent of this register is to simplify the part setup for typical serial link operation modes. Writing values other than 0x0 to this register causes registers throughout the JESD204A memory map to be updated. Once these registers have been written the affected JESD204A configuration register reads back with their new values and can be updated. These bits are self clearing and always read back as 0b000.

000: default—configuration determined by other registers

001: two converters using two links with one lane per link (maximum sample rate = 80 MHz or 155 MHz) Each link configuration:
M = 1; N' = 16; CF = 0; K = 16; S = 1; F = 2; L = 1; HD = 0;

010 = two converters using one link with two lanes per link (Maximum sample rate = 80 MHz or 155 MHz). Each link configuration:
M = 2; N' = 16; CF = 0; K = 16; S = 1; F = 2; L = 2; HD = 0; uses DSYNCA pin for synchronization. Setting this mode sets Address 0x5F = 0x02 and sets Address 0x60 = 0x14 for Link A and sets Address 0x60 = 0x01 for Link B.

011 = two converters using one link and a single lane (maximum sample rate = 78.125 MHz). Each link configuration: M = 2; N' = 16; CF = 0; K = 8;S = 1; F = 4; L = 1; HD = 0; uses DSYNCA pin for synchronization and DOUTA for output signals.

100 to 111: reserved.

JESD204A Lane Assignment (Register 0x5F)

Bits[7:4]—Reserved

Bits[3:0]—JESD204A Serial Lane Control

These bits set the lane usage. See Figure 62.

0000: one lane per link. Link A: Lane 0 sent on Lane A, Link B: Lane 0 sent on Lane B.

0001: one lane per link. Link A: Lane 0 sent on Lane B, Link B: Lane 0 sent on Lane A.

0010: two lanes per link. Link A: Lane 0, one sent on Lane A, Link B disabled.

0011: two lanes per link. Link A: Lane 0, one sent on Lane B, Lane A. Link B disabled.

0100: two lanes per link. Link B: Lane 0, one sent on Lane A, Lane B. Link A disabled.

0101: two lanes per link. Link B: Lane 0, one sent on Lane B, Lane A. Link A disabled.

0110 to 1111: reserved for future use.

JESD204A Link Control Register 1 (Register 0x60)

Bit 7—Reserved

Bit 6—Serial Tail Bit Enable

If this bit is set, the unused tail bits are padded with a pseudo random number sequence from a 31-bit LFSR (see JESD204A 5.1.4).

Bit 5—Serial Test Sample Enable

If this bit is set, JESD204A test samples are enabled—transport layer test sample sequence (as specified in JESD204A section 5.1.6.2) is sent on all link lanes.

Bit 4—Serial Lane Synchronization Enable

If this bit is set, lane synchronization is enabled. Both sides perform lane sync. Frame alignment character insertion uses either /K28.3/ or /K28.7/ control characters (see JESD204A 5.3.3.4).

Bits[3:2]—Serial Lane Alignment Sequence Mode

00: initial lane alignment sequence disabled.

01: initial lane alignment sequence enabled.

10: reserved.

11: initial lane alignment sequence always on test mode—JESD204A data link layer test mode where repeated lane alignment sequence is sent on all lanes.

Bit 1—Frame Alignment Character Insertion Disable

If Bit 1 is set, the frame alignment character insertion is disabled per JESD204A section 5.3.3.4.

Bit 0—Serial Transmit Link Powered Down

If Bit 0 is set high, the serial transmit link is held in reset with its clock gated off. The JESD204A transmitter should be powered down when changing any of the link configuration bits.

JESD204A Link Control Register 2 (Register 0x61)

Bits[7:6]—Local DSYNC Mode

00: individual/separate mode. Each link is controlled by a separate DSYNC pin that independently controls code group synchronization.

01: global mode. Any DSYNC signal causes the link to begin code group synchronization.

10: sync active mode. DSYNC signal is active—force code group synchronization.

11: DSYNC pin disabled.

Bit 5—DSYNC Pin Input Inverted

If this bit is set, the DSYNC pin of the link is inverted (active high).

Bit 4—CMOS DSYNC Input

0: LVDS differential pair DSYNC input (default)

1: CMOS single ended DSYNC input

Bit 3—Open

Bit 2—Bypass 8b/10b Encoding

If this bit is set the 8b/10b encoding is bypassed and the most significant bits are set to 0.

Bit 1—Invert Transmit Bits

Setting this bit inverts the 10 serial output bits. This effectively inverts the output signals.

Bit 0—Mirror Serial Output Bits

Setting this bit reverses the order of the 10b outputs.

JESD204A Link Control Register 3 (Register 0x62)

Bit 7—Disable CHKSUM

Setting this bit high disables the CHKSUM configuration parameter (for testing purposes only).

Bit 6—Open

Bits[5:4]—Link Test Generation Input Selection

00: 16-bit test generation data injected at sample input to the link.

01: 10-bit test generation data injected at output of 8b/10b encoder (at input to PHY).

10: reserved.

11: reserved.

Bit 3—Open

Bits[2:0]—Link Test Generation Mode

000: normal operation (test mode disabled).

001: alternating checker board.

010: 1/0 word toggle.

011: PN sequence—long.

100: PN sequence—short.

101: continuous/repeat user test mode—most significant bits from user pattern (1, 2, 3, 4) placed on the output for 1 clock cycle and then repeat. (output user pattern 1, 2, 3, 4, 1, 2, 3, 4, 1, 2, 3, 4…).

110: single user test mode—most significant bits from user pattern (1, 2, 3, 4) placed on the output for 1 clock cycle and then output all zeros. (output user pattern 1, 2, 3, 4, then output all zeros).

111: ramp output.

JESD204A Link Control Register 4 (Register 0x63)

Bits[7:0]—Initial Lane Alignment Sequence Repeat Count

Specifies the number of times the initial lane alignment sequence (ILAS) is repeated. If 0 is programmed the ILAS does not repeat. If 1 is programmed the ILAS repeat one time and so on. See Register 0x60, Bits[3:2] to enable the ILAS and for a test mode to continuously enable the initial lane alignment sequence.

JESD204A Device Identification Number (DID) (Register 0x64)

Bits[7:0]—Serial Device Identification (DID) Number

JESD204A Bank Identification Number (BID) (Register 0x65)

Bits[7:4]—Open

Bits[3:0]—Serial Bank Identification (DID) Number

JESD204A Lane Identification Number (LID) for Lane 0 (Register 0x66)

Bits[7:5]—Open

Bits[4:0]—Serial Lane Identification (LID) Number for Lane 0.

JESD204A Lane Identification Number (LID) for Lane 1 (Register 0x67)

Bits[7:5]—Open

Bits[4:0]—Serial Lane Identification (LID) Number for Lane 1.

JESD204A Scrambler (SCR) and Lane Configuration Registers (Register 0x6E)

Bit 7—Enable Serial Scrambler Mode

Setting this bit high enables the scrambler (SCR = 1).

Bits[6:1]—Open

Bit[0]—Serial Lane Control.

00000: one lane per link (L = 1).

00001: two lanes per link (L = 2).

00010: 11111—reserved.

JESD204A Number of Octets Per Frame (F) (Register 0x6F—Read Only)

Bits[7:0]—Number of Octets per Frame (F)

The readback from this register is calculated from the following equation: F = (M × 2)/L

Valid values for F for the AD9644 are:

F = 2, with M = 1 and L = 1

F = 4, with M = 2 and L = 1

F = 2, with M = 2 and L = 2

JESD204A Number of Frames Per Multiframe (Register 0x70)

Bits[7:5]—Reserved

Bits[4:0]—Number of Frames per Multiframe (K).

JESD204A Number of Converters Per Link (M) (Register 0x71)

Bits[7:1]—Reserved

Bit 0—Number of Converters per Link per Device (M).

0: link connected to one ADC. Only primary input used (M = 1).

1: link connected to two ADCs. Primary and secondary inputs used (M = 2).

JESD204A ADC Resolution (N) and Control Bits Per Sample (CS) (Register 0x72)

Bits[7:6]—Number of Control Bits per Sample (CS)

00: no control bits sent per sample (CS = 0).

01: one control bits sent per sample—overrange bit enabled. (CS = 1).

10: two control bits sent per sample—overflow/underflow bits enabled (CS = 2).

11: unused.

Bit 5—Open

Bits[4:0]—Converter Resolution (N)

Read only bits showing the converter resolution (reads back 13 (0xD) for 14-bit resolution).

JESD204A Total Bits Per Sample (N') (Register 0x73)

Bits[7:5]—Open

Bits[4:0]—Total Number of Bits per Sample (N')

Read only bits showing the total number of bits per sample—1 (reads back 15 (0xF) for 16 bits per sample).

JESD204A Samples Per Converter (S) Frame Cycle (Register 0x74)

Bits[7:5]—Open

Bits[4:0]—Samples per Converter Frame Cycle (S)

Read only bits showing the number of samples per converter frame cycle −1 (reads back 0 (0x0) for 1 sample per converter frame).

JESD204A HD and CF Configuration (Register 0x75)

Bit 7—Enable High Density Format (Read Only)

Read only bit—always 0 in the AD9644.

Bits[6:5]—Reserved

Bits[4:0]—Number of Control Words per Frame Clock Cycle per Link (CF)

Read only bits—reads back 0x0 for the AD9644.

JESD204A Serial Reserved Field 1 (Register 0x76)

Bits[7:0]—Serial Reserved Field 1 (RES1)

This read/write register is available for customer use.

JESD204A Serial Reserved Field 2 (Register 0x77)

Bits[7:0]—Serial Reserved Field 2 (RES2)

This read/write register is available for customer use.

JESD204A Serial Checksum Value for Lane 0 (Register 0x78)

Bits[7:0]—Serial Checksum Value for Lane 0

This read only register is automatically calculated for each lane. Sum (all link configuration parameters for Lane 0) mode 256.

JESD204A Serial Checksum Value for Lane 1 (Register 0x79)

Bits[7:0]—Serial Checksum Value for Lane 1

This read only register is automatically calculated for each lane. Sum (all link configuration parameters for Lane 1) mode 256.

APPLICATIONS INFORMATION

DESIGN GUIDELINES

Before starting design and layout of the AD9644 as a system, it is recommended that the designer become familiar with these guidelines, which discuss the special circuit connections and layout requirements that are needed for certain pins.

Power and Ground Recommendations

When connecting power to the AD9644, it is recommended that two separate 1.8 V supplies be used. Use one supply for analog (AVDD); use a separate supply for the digital outputs (DRVDD). For both AVDD and DRVDD several different decoupling capacitors should be used to cover both high and low frequencies. Place these capacitors close to the point of entry at the PCB level and close to the pins of the part, with minimal trace length.

A single PCB ground plane should be sufficient when using the AD9644. With proper decoupling and smart partitioning of the PCB analog, digital, and clock sections, optimum performance is easily achieved.

Exposed Paddle Thermal Heat Slug Recommendations

It is mandatory that the exposed paddle on the underside of the ADC be connected to analog ground (AGND) to achieve the best electrical and thermal performance. A continuous, exposed (no solder mask) copper plane on the PCB should mate to the AD9644 exposed paddle, Pin 0.

The copper plane should have several vias to achieve the lowest possible resistive thermal path for heat dissipation to flow through the bottom of the PCB. These vias should be filled or plugged to prevent solder wicking through the vias, which can compromise the connection.

To maximize the coverage and adhesion between the ADC and the PCB, a silkscreen should be overlaid to partition the continuous plane on the PCB into several uniform sections. This provides several tie points between the ADC and the PCB during the reflow process. Using one continuous plane with no partitions guarantees only one tie point between the ADC and the PCB. For detailed information about packaging and PCB layout of chip scale packages, see the AN-772 Application Note, *A Design and Manufacturing Guide for the Lead Frame Chip Scale Package (LFCSP)*, at www.analog.com.

VCMA and VCMB

The VCMA and VCMB pins should be decoupled to ground with a 0.1 μF capacitor, as shown in Figure 50.

SPI Port

The SPI port should not be active during periods when the full dynamic performance of the converter is required. Because the SCLK, CSB, and SDIO signals are typically asynchronous to the ADC clock, noise from these signals can degrade converter performance. If the on-board SPI bus is used for other devices, it may be necessary to provide buffers between this bus and the AD9644 to keep these signals from transitioning at the converter inputs during critical sampling periods.

OUTLINE DIMENSIONS

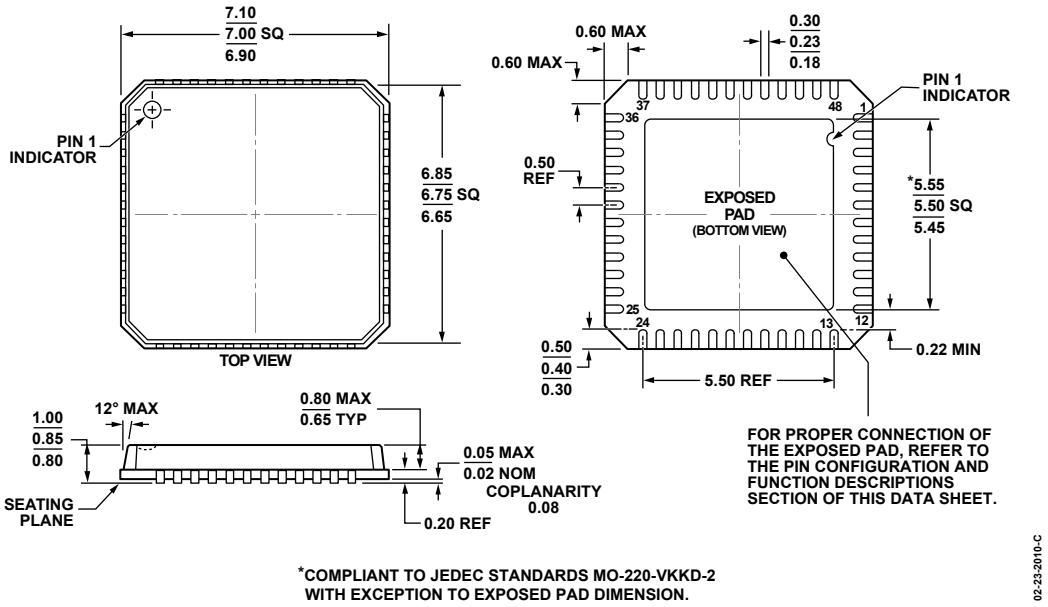


Figure 72. 48-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
7 mm × 7 mm Body, Very Thin Quad
(CP-48-8)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD9644BCPZ-80	−40°C to +85°C	48-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-48-8
AD9644BCPZRL7-80	−40°C to +85°C	48-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-48-8
AD9644CCPZ-80	−40°C to +85°C	48-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-48-8
AD9644CCPZRL7-80	−40°C to +85°C	48-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-48-8
AD9644BCPZ-155	−40°C to +85°C	48-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-48-8
AD9644BCPZRL7-155	−40°C to +85°C	48-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-48-8
AD9644-80KITZ		Evaluation Board	
AD9644-155KITZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

NOTES

D09180-0-1/12(C)

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- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
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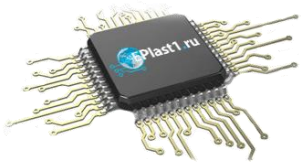
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

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