MIC2103/04

75V, Synchronous Buck Controllers featuring Adaptive On-Time Control

Hyper Speed Control™ Family

General Description

The Micrel MIC2103/04 are constant-frequency, synchronous buck controllers featuring a unique adaptive ON-time control architecture. The MIC2103/04 operates over an input supply range from 4.5V to 75V and can be used to supply up to 15A of output current. The output voltage is adjustable down to 0.8V with a guaranteed accuracy of ±1%. The device operates with programmable switching frequency from 200kHz to 600kHz.

Micrel's Hyper Light Load™ architecture provides the same high-efficiency and ultra fast transient response as the Hyper Speed Control architecture under the medium to heavy loads, but also maintains high efficiency under light load conditions by transitioning to variable frequency, discontinuous-mode operation.

The MIC2103/04 offers a full suite of protection features to ensure protection of the IC during fault conditions. These include under-voltage lockout to ensure proper operation under power-sag conditions, internal soft-start to reduce inrush current, fold-back current limit, "hiccup" mode short-circuit protection and thermal shutdown.

All support documentation can be found on Micrel's web site at: www.micrel.com.

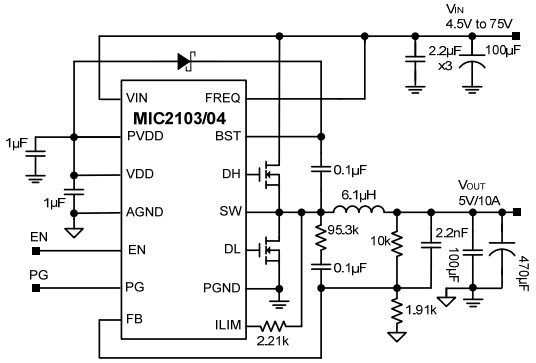
Features

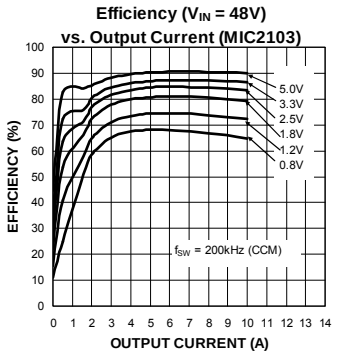
- Hyper Speed Control architecture enables
  - High delta V operation (V_{IN} = 75V and V_{OUT} = 1.2V)
  - Any Capacitor™ stable
- 4.5V to 75V input voltage
- 0.8V Reference Voltage with ±1% accuracy
- 200kHz to 600kHz, programmable switching frequency
- Hyper Light Load Control (MIC2103 only)
- Hyper Speed Control (MIC2104 only)
- Enable input, Power-Good output
- Built-in 5V regulator for single-supply operation
- Programmable current limit and fold-back "hiccup" mode short-circuit protection
- 5ms internal soft-start, internal compensation, and thermal shutdown
- Supports safe start-up into a pre-biased output
- –40°C to +125°C junction temperature range
- Available in 16-pin 3mm x 3mm MLF® package

Applications

- Distributed power systems
- Networking/Telecom Infrastructure
- Printers, scanners, graphic cards and video cards

Typical Application





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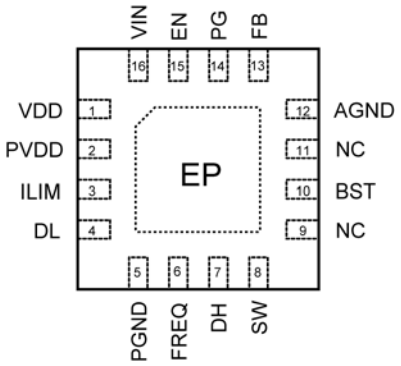
Ordering Information

Part Number	Switching Frequency	Features	Package	Junction Temperature Range	Lead Finish
MIC2103YML	200kHz to 600kHz	Hyper Light Load	16-pin 3mm x 3mm MLF	–40°C to +125°C	Pb-Free
MIC2104YML	200kHz to 600kHz	Hyper Speed Control	16-pin 3mm x 3mm MLF	–40°C to +125°C	Pb-Free

Pin Configuration



16-Pin 3mm x 3mm MLF (ML)
(TOP VIEW)

Pin Description

Pin Number	Pin Name	Pin Function
1	VDD	Internal +5V linear regulator output. VDD is the internal supply bus for the device. A 1µF ceramic capacitor from VDD to AGND is required for decoupling. In the applications with VIN<+5.5V, VDD should be tied to VIN to by-pass the linear regulator.
2	PVDD	5V supply input for the low-side N-channel MOSFET driver, which can be tied to VDD externally. A 1µF ceramic capacitor from PVDD to PGND is recommended for decoupling.
3	ILIM	Current Limit Setting. Connect a resistor from SW to ILIM to set the over-current threshold for the converter.
4	DL	Low-Side Drive output. High-current driver output for external low-side MOSFET of a buck converter. The DL driving voltage swings from ground to V_{DD}. Adding a small resistor between DL pin and the gate of the low-side N-channel MOSFET can slow down the turn-on and turn-off speed of the MOSFET.
5	PGND	Power Ground. PGND is the return path for the buck converter power stage. The PGND pin connects to the sources of low-side N-Channel external MOSFET, the negative terminals of input capacitors, and the negative terminals of output capacitors. The return path for the power ground should be as small as possible and separate from the Signal ground (AGND) return path.
6	FREQ	Switching Frequency Adjust input. Tie this pin to VIN to operate at 600kHz and place a resistor divider to reduce the frequency.
7	DH	High-Side Drive output. High-current driver output for external high-side MOSFET of a buck converter. The DH driving voltage is floating on the switch node voltage (V_{SW}). Adding a small resistor between DH pin and the gate of the high-side N-channel MOSFET can slow down the turn-on and turn-off speed of the MOSFET.
8	SW	Switch Node and Current-Sense input. High current output driver return. The SW pin connects directly to the switch node. Due to the high-speed switching on this pin, the SW pin should be routed away from sensitive nodes. The SW pin also senses the current by monitoring the voltage across the low-side MOSFET during OFF time. In order to sense the current accurately, connect the low-side MOSFET drain to the SW pin using a Kelvin connection.

Pin Description (Continued)

Pin Number	Pin Name	Pin Function
9, 11	NC	No connection.
10	BST	Voltage Supply Pin input for the high-side N-channel MOSFET driver, which can be powered by a bootstrapped circuit connected between VDD and SW, using a Schottky diode and a 0.1µF ceramic capacitor. Adding a small resistor at BST pin can slow down the turn-on speed of the high-side MOSFET.
12	AGND	Signal ground for VDD and the control circuitry, which is connected to Thermal Pad electronically. The signal ground return path should be separate from the power ground (PGND) return path.
13	FB	Feedback input. Input to the transconductance amplifier of the control loop. The FB pin is regulated to 0.8V. A resistor divider connecting the feedback to the output is used to set the desired output voltage.
14	PG	Power Good output. Open Drain Output, an external pull-up resistor to VDD or external power rails is required.
15	EN	Enable input. A logic signal to enable or disable the buck converter operation. The EN pin is CMOS compatible. Logic high enables the device, logic low shutdowns the regulator. In the disable mode, the V_{DD} supply current for the device is minimized to 0.7mA typically.
16	VIN	Supply voltage. The VIN operating voltage range is from 4.5V to 75V. A 1µF ceramic capacitor from VIN to AGND is required for decoupling.
EP	ePad	Exposed Pad. Connect the EPAD to PGND plain on the PCB to improve the thermal performance.

Absolute Maximum Ratings[1]

V_{IN} ..... –0.3V to +76V
V_{DD}, V_{PVDD} ..... –0.3V to +6V
V_{SW}, V_{FREQ}, V_{ILIM}, V_{EN} ..... –0.3V to (V_{IN} +0.3V)
V_{BST} to V_{SW} ..... –0.3V to 6V
V_{BST} ..... –0.3V to 82V
V_{PG} ..... –0.3V to (V_{DD} + 0.3V)
V_{FB} ..... –0.3V to (V_{DD} + 0.3V)
PGND to AGND ..... –0.3V to +0.3V
Junction Temperature ..... +150°C
Storage Temperature (T_S) ..... –65°C to +150°C
Lead Temperature (soldering, 10sec) ..... 260°C
ESD Rating[2] ..... ESD Sensitive

Operating Ratings[3]

Supply Voltage (V_{IN}) ..... 4.5V to 75V
Enable Input (V_{EN}) ..... 0V to V_{IN}
V_{SW}, V_{FEQ}, V_{ILIM}, V_{EN} ..... 0V to V_{IN}
Junction Temperature (T_J) ..... –40°C to +125°C
Junction Thermal Resistance
3mm x 3mm MLF-16 (θ_{JA}) ..... 50.8°C/W
3mm x 3mm MLF-16 (θ_{JC}) ..... 25.3°C/W

Electrical Characteristics[4]

V_{IN} = 48V, V_{OUT} = 5V, V_{BST} – V_{SW} = 5V; T_A = 25°C, unless noted. **Bold** values indicate –40°C ≤ T_J ≤ +125°C.

Parameter	Condition	Min	Typ	Max	Units
Power Supply Input					
Input Voltage Range (V_{IN})[5]		**4.5**		**75**	V
Quiescent Supply Current (MIC2103)	V_{FB} = 1.5V		400	**750**	µA
Quiescent Supply Current (MIC2104)	V_{FB} = 1.5V		2.1	**3**	mA
Shutdown Supply Current	SW unconnected, V_{EN} = 0V		0.1	**10**	µA
VDD Supply					
VDD Output Voltage	V_{IN} = 7V to 75V, I_{DD} = 10mA	**4.8**	5.2	**5.4**	V
VDD UVLO Threshold	V_{DD} rising	**3.8**	4.2	**4.6**	V
VDD UVLO Hysteresis			400		mV
Load Regulation	I_{DD} = 0 to 40mA	0.6	2	3.6	%
Reference					
Feedback Reference Voltage	T_J = 25°C (±1.0%)	0.792	0.8	0.808	V
	-40°C ≤ T_J ≤ 125°C (±2%)	**0.784**	**0.8**	**0.816**	
FB Bias Current	V_{FB} = 0.8V		5	**500**	nA
Enable Control					
EN Logic Level High		**1.8**			V
EN Logic Level Low				**0.6**	V
EN Hysteresis			200		mV
EN Bias Current	V_{EN} = 48V		23	**40**	µA

Electrical Characteristics[4] (Continued)

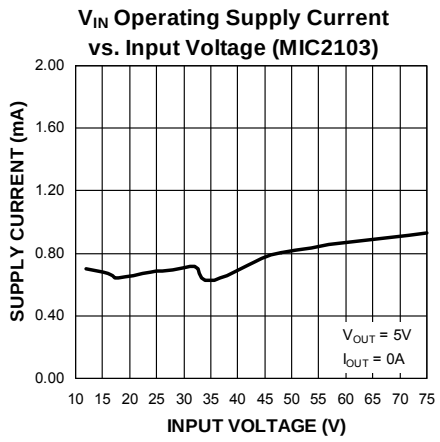
V_{IN} = 48V, V_{OUT} = 5V, $V_{BST} – V_{SW}$ = 5V; T_A = 25°C, unless noted. **Bold** values indicate –40°C ≤ T_J ≤ +125°C.

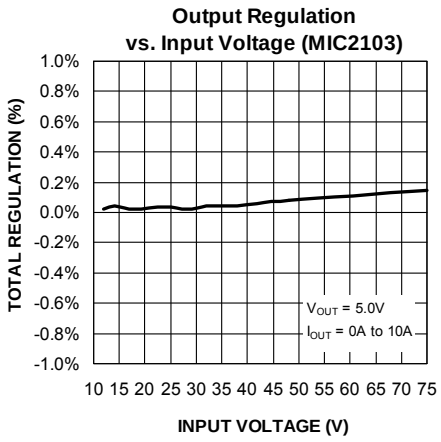
Oscillator					
Switching Frequency	$V_{FREQ} = V_{IN}$	**400**	600	**750**	kHz
	V_{FREQ} = 50%V_{IN}		300		
Maximum Duty Cycle			85		%
Minimum Duty Cycle	V_{FB} > 0.8V		0		%
Minimum Off-Time		140	200	260	ns
Soft Start					
Soft-Start time			5		ms
Short Circuit Protection					
Current-Limit Threshold	V_{FB} = 0.79V	-30	-14	0	mV
Short-Circuit Threshold	V_{FB} = 0V	-23	-7	9	mV
Current-Limit Source Current	V_{FB} = 0.79V	60	80	100	µA
Short-Circuit Source Current	V_{FB} = 0V	27	36	47	µA
FET Drivers					
DH, DL Output Low Voltage	I_{SINK} = 10mA			**0.1**	V
DH, DL Output High Voltage	I_{SOURCE} = 10mA	V_{PVDD} - 0.1V Or V_{BST} - 0.1V			V
DH On-Resistance, High State			2.1	**3.3**	Ω
DH On-Resistance, Low State			1.8	**3.3**	Ω
DL On-Resistance, High State			1.8	**3.3**	Ω
DL On-Resistance, Low State			1.2	**2.3**	Ω
SW, BST Leakage Current				50	µA
Power Good					
Power Good Threshold Voltage	Sweep V_{FB} from Low to High	**85**	90	**95**	%V_{OUT}
Power Good Hysteresis	Sweep V_{FB} from High to Low		6		%V_{OUT}
Power Good Delay Time	Sweep V_{FB} from Low to High		100		µs
Power Good Low Voltage	V_{FB} < 90% x V_{NOM}, I_{PG} = 1mA		70	**200**	mV
Thermal Protection					
Over-Temperature Shutdown	T_J Rising		160		°C
Over-Temperature Shutdown Hysteresis			4		°C

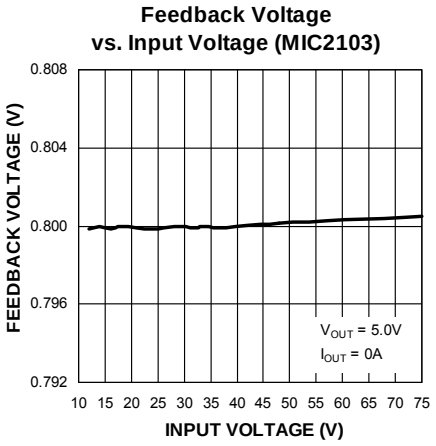
Notes:

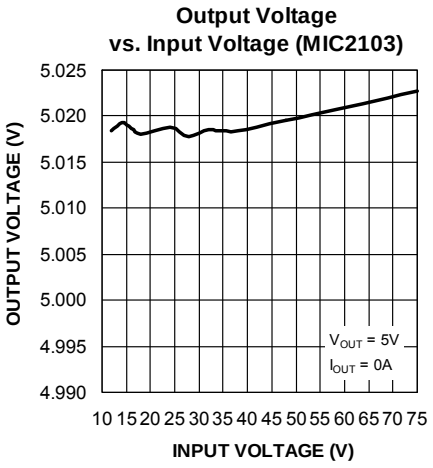
1. Exceeding the absolute maximum rating may damage the device.
2. Devices are ESD sensitive. Handling precautions recommended. Human body model, 1.5kΩ in series with 100pF.
3. The device is not guaranteed to function outside operating range.
4. Specification for packaged product only.
5. The application is fully functional at low V_{DD} (supply of the control section) if the external MOSFETs have low voltage V_{TH}.

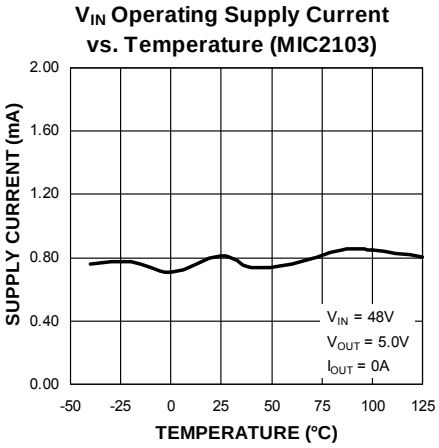
Typical Characteristics

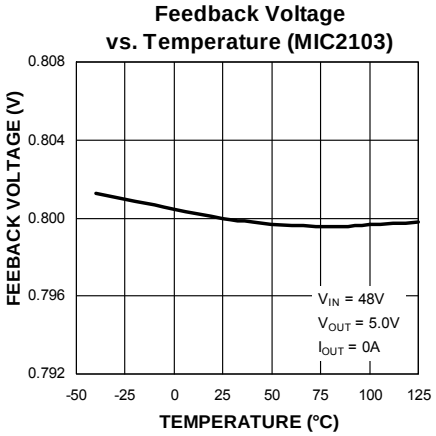


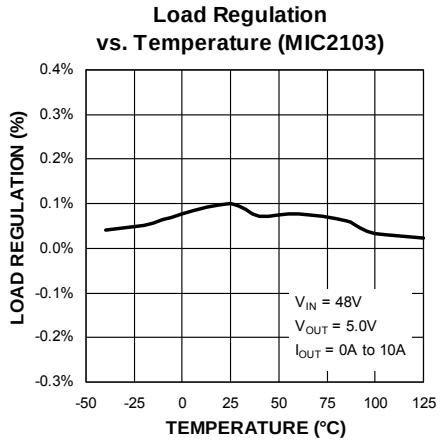


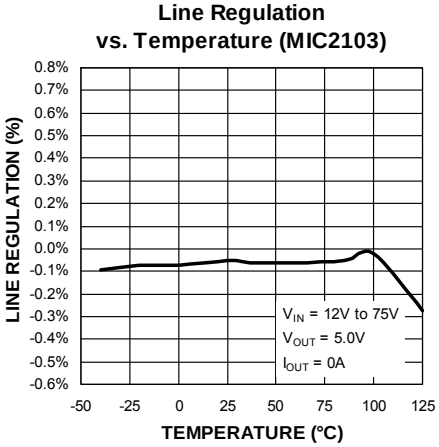


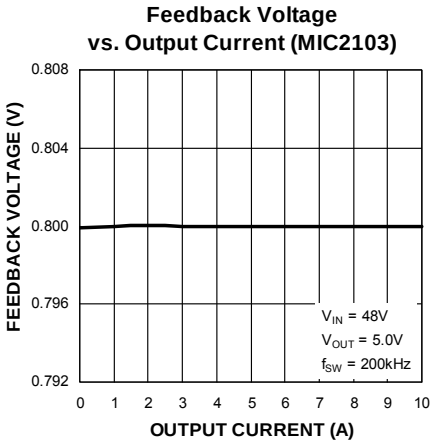






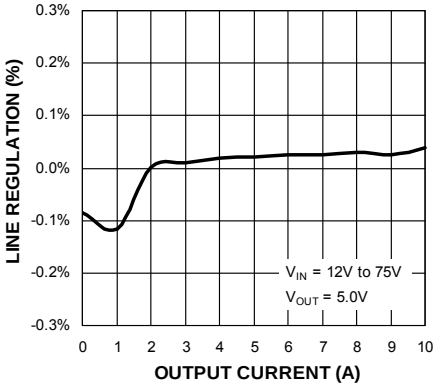




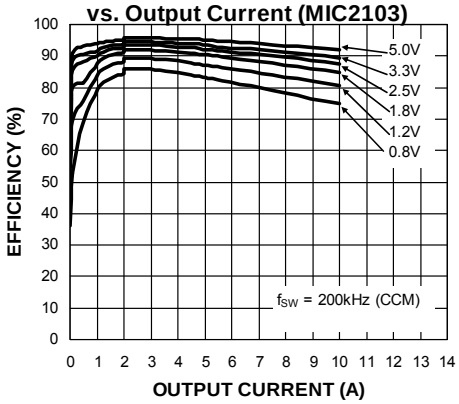


Typical Characteristics (Continued)

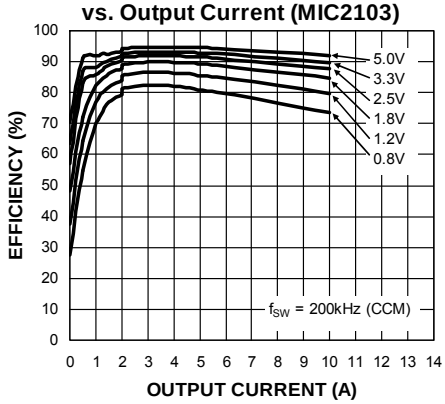
Line Regulation vs. Output Current (MIC2103)



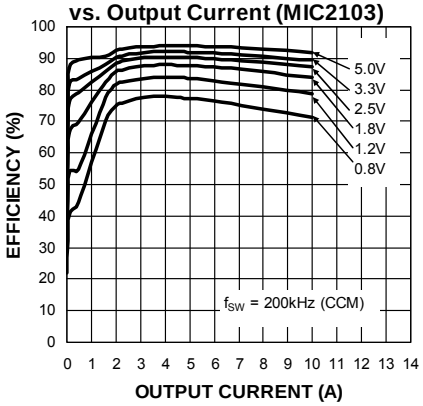
Efficiency (V_{IN} =12V) vs. Output Current (MIC2103)



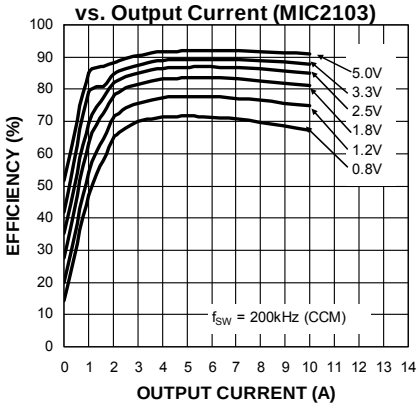
Efficiency (V_{IN} = 18V) vs. Output Current (MIC2103)



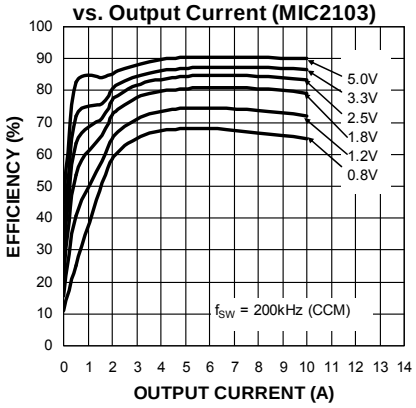
Efficiency (V_{IN} = 24V) vs. Output Current (MIC2103)



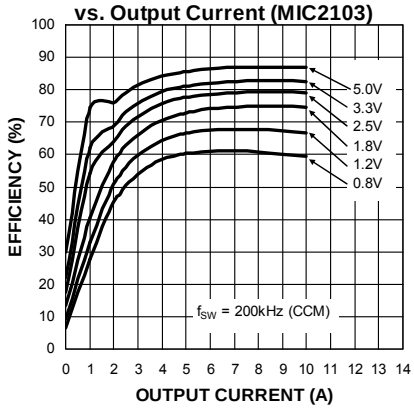
Efficiency (V_{IN} = 38V) vs. Output Current (MIC2103)



Efficiency (V_{IN} = 48V) vs. Output Current (MIC2103)

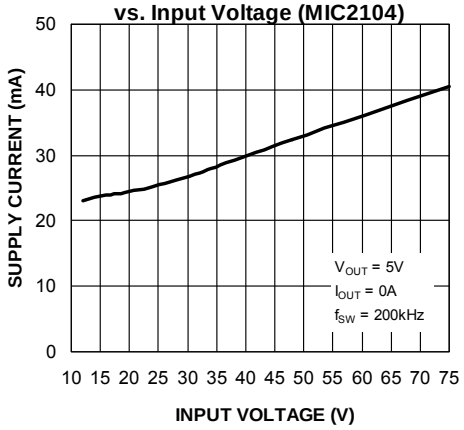


Efficiency (V_{IN} = 75V) vs. Output Current (MIC2103)

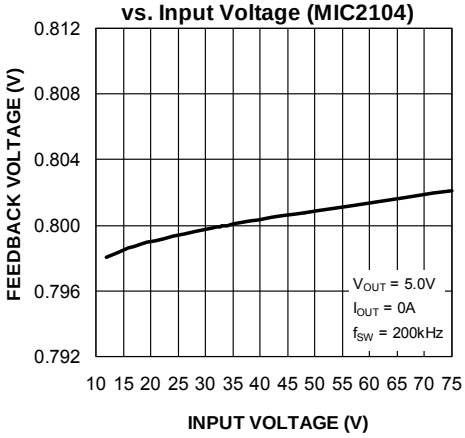


Typical Characteristics (Continued)

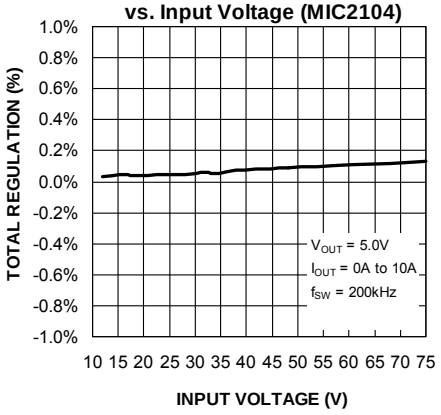
V_{IN} Operating Supply Current vs. Input Voltage (MIC2104)



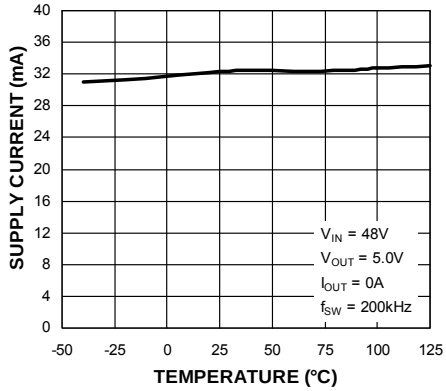
Feedback Voltage vs. Input Voltage (MIC2104)



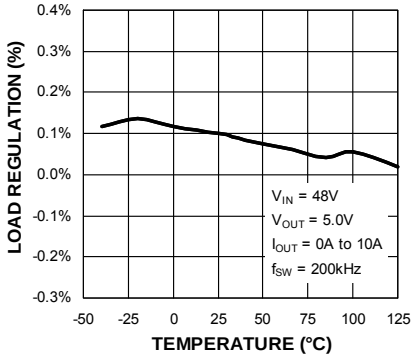
Output Regulation vs. Input Voltage (MIC2104)



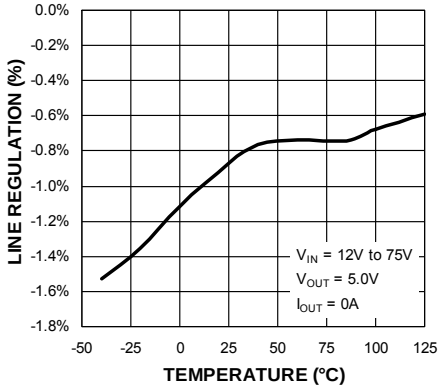
V_{IN} Operating Supply Current vs. Temperature (MIC2104)



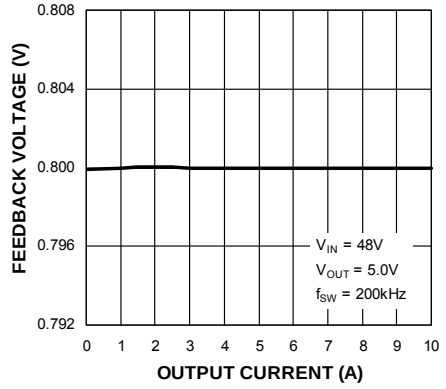
Load Regulation vs. Temperature (MIC2104)



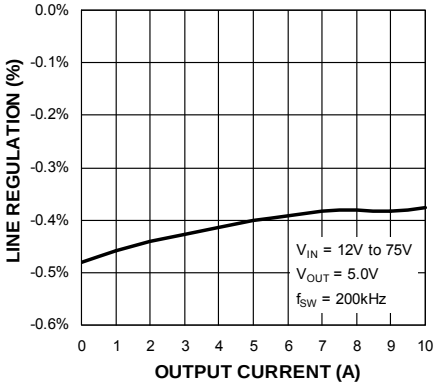
Line Regulation vs. Temperature (MIC2104)



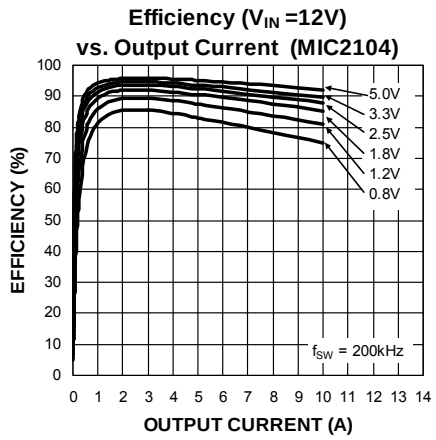
Feedback Voltage vs. Output Current (MIC2104)

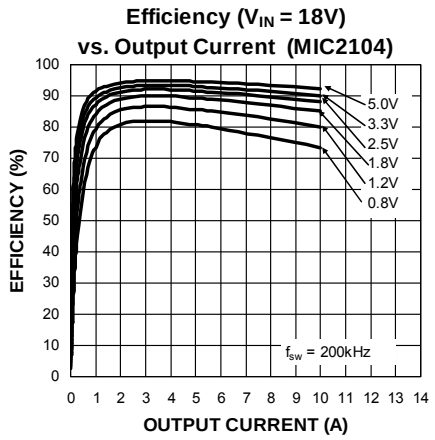


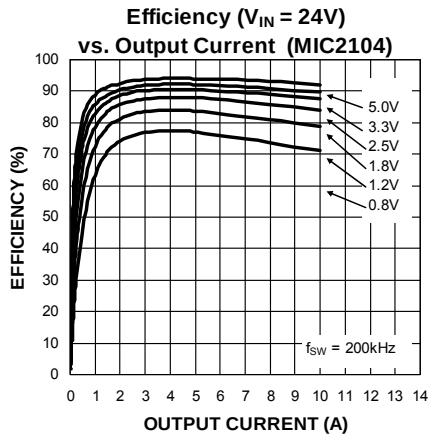
Line Regulation vs. Output Current (MIC2104)

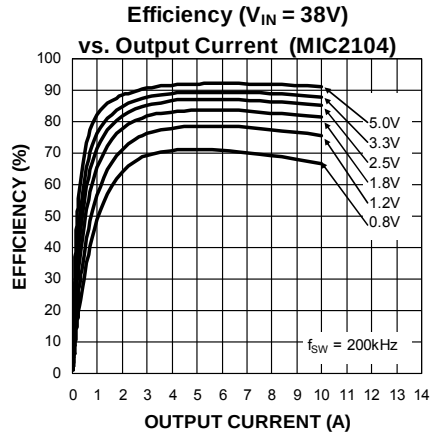


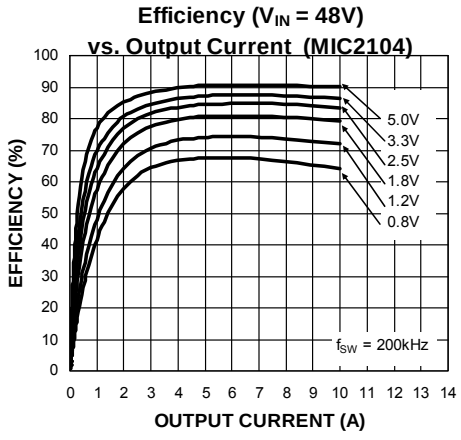
Typical Characteristics (Continued)

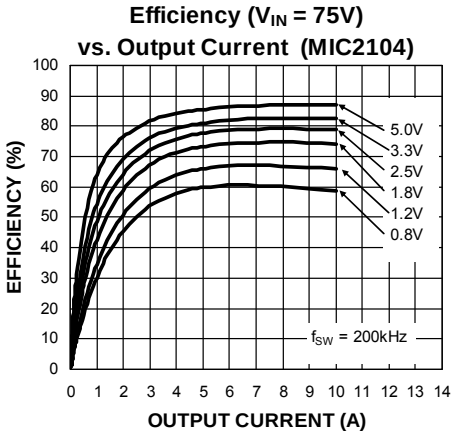


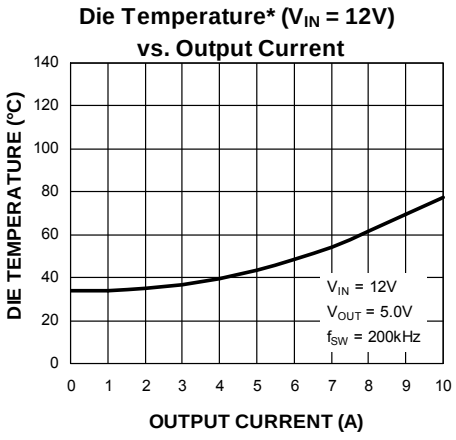


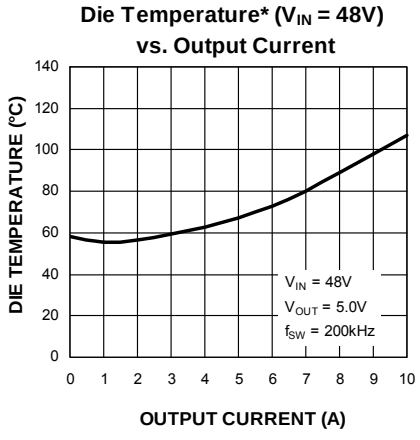


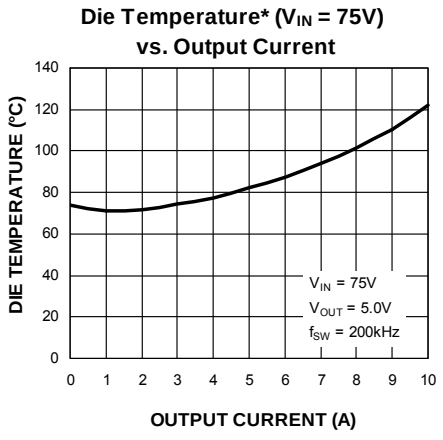








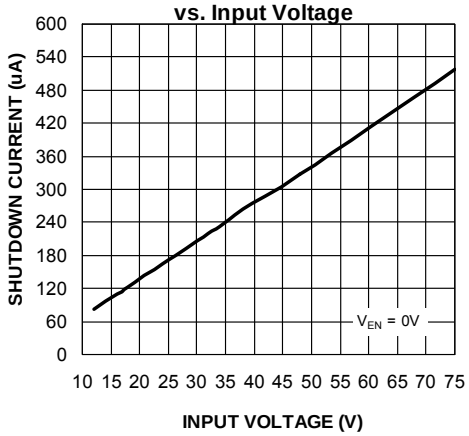




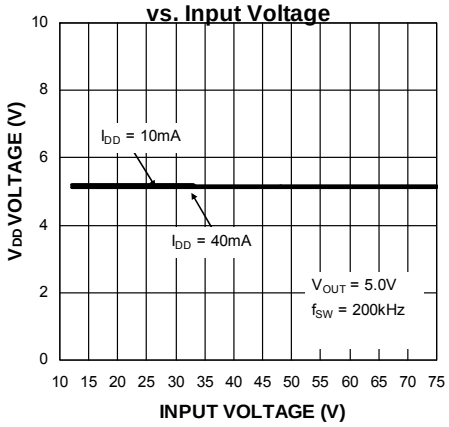
* **Case Temperature**: The temperature measurement was taken at the hottest point on the MIC2103 case mounted on a 5 square inch PCB, see Thermal Measurement section. Actual results will depend upon the size of the PCB, ambient temperature and proximity to other heat emitting components.

Typical Characteristics (Continued)

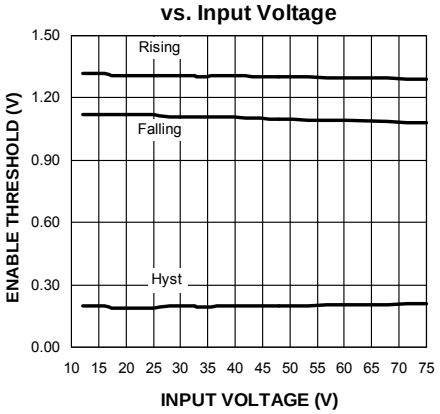
V_{IN} Shutdown Current vs. Input Voltage



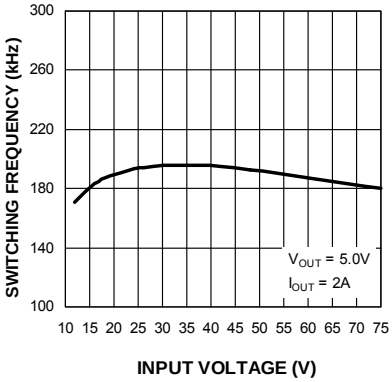
V_{DD} Voltage vs. Input Voltage



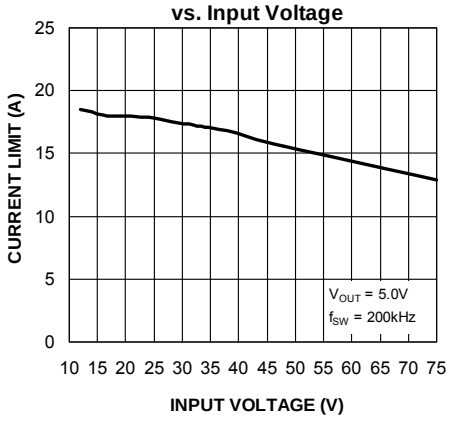
Enable Threshold vs. Input Voltage



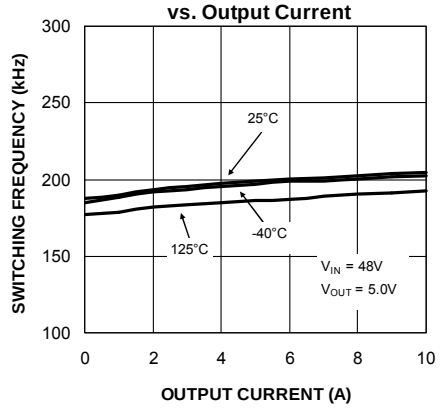
Switching Frequency vs. Input Voltage



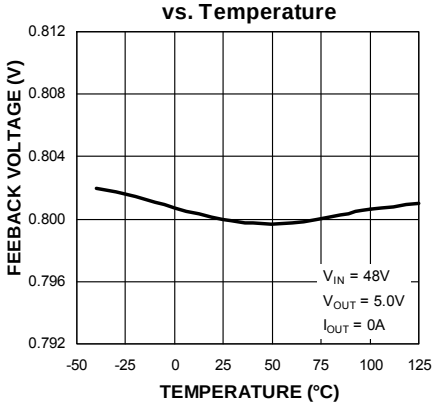
Output Peak Current Limit vs. Input Voltage



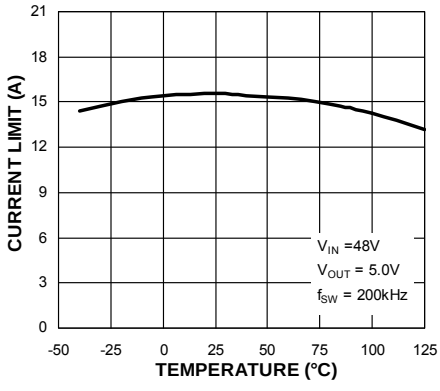
Switching Frequency vs. Output Current



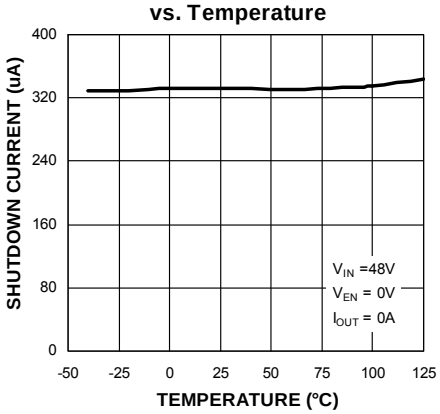
Feedback Voltage vs. Temperature



Output Peak Current Limit vs. Temperature

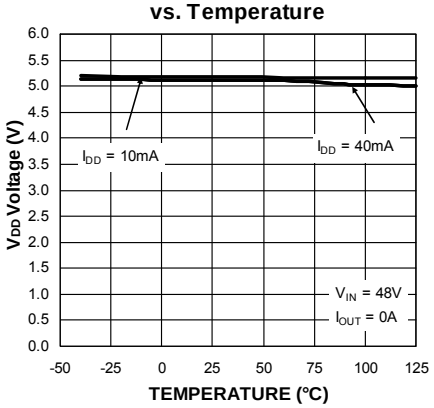


V_{IN} Shutdown Current vs. Temperature

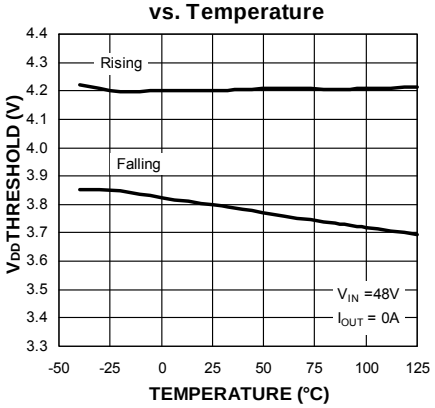


Typical Characteristics (Continued)

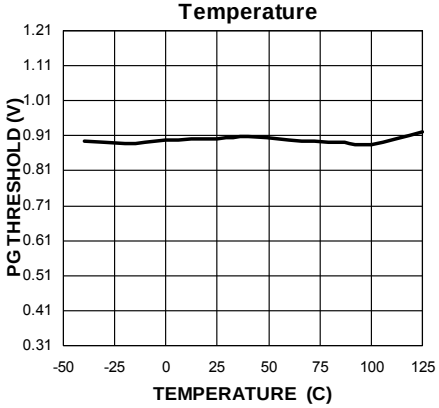
V_{DD} Voltage vs. Temperature



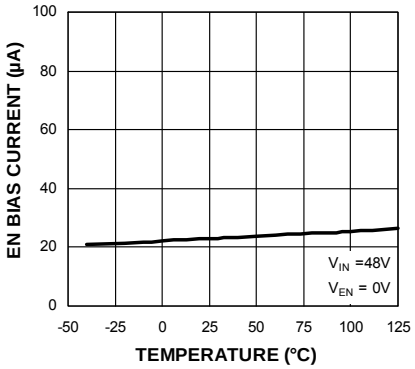
V_{DD} UVLO Threshold vs. Temperature



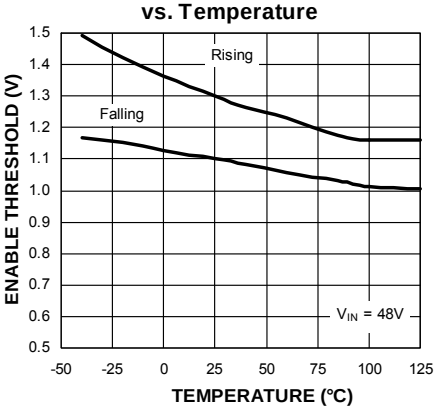
PG Threshold/VREF Ratio vs. Temperature



EN Bias Current vs. Temperature

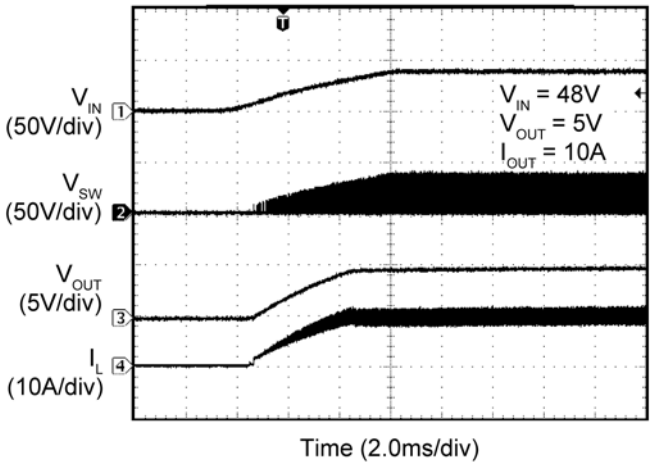


Enable Threshold vs. Temperature

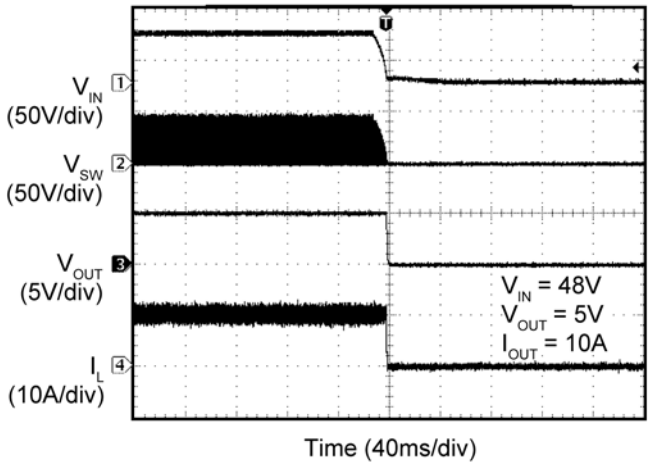


Functional Characteristics

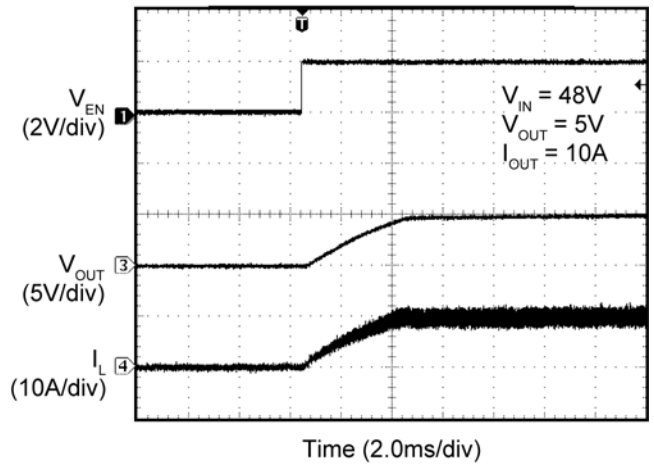
V_{IN} Soft Turn-On



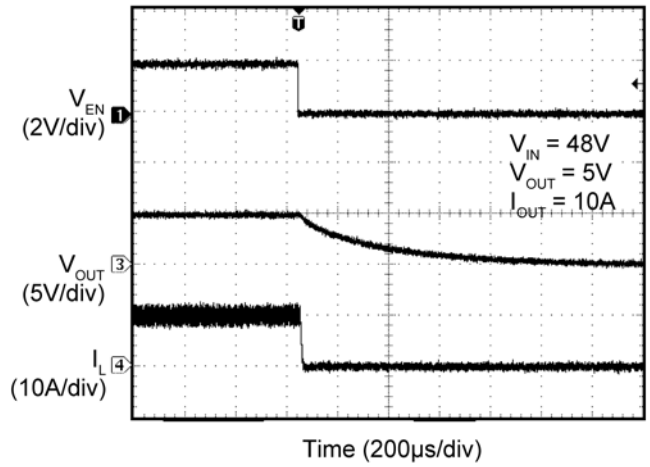
V_{IN} Soft Turn-Off



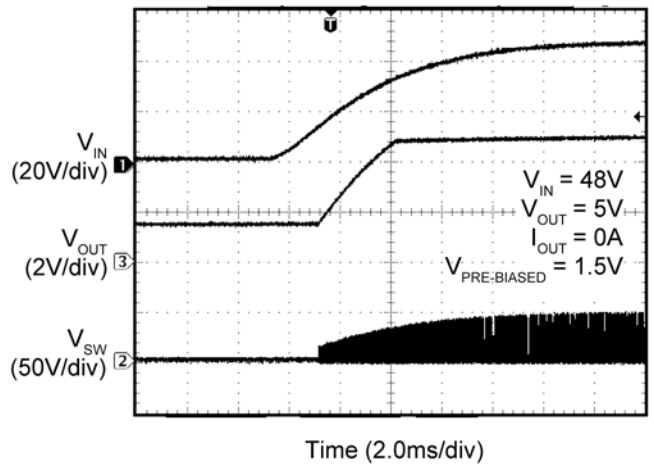
Enable Turn-On Delay and Rise Time



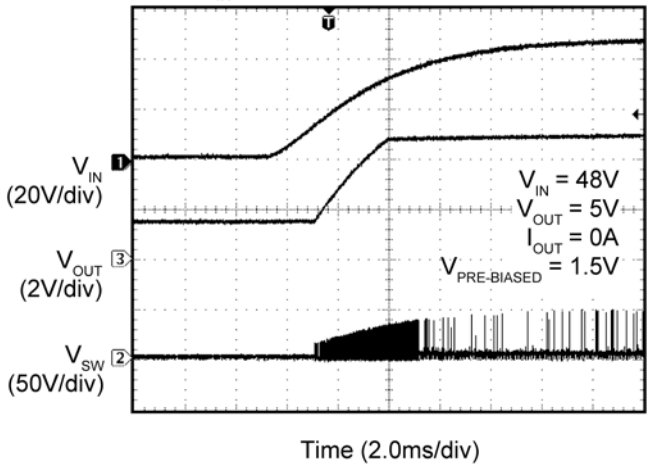
Enable Turn-Off Delay and Fall Time



MIC2104 V_{IN} Start-up with Pre-Biased Output

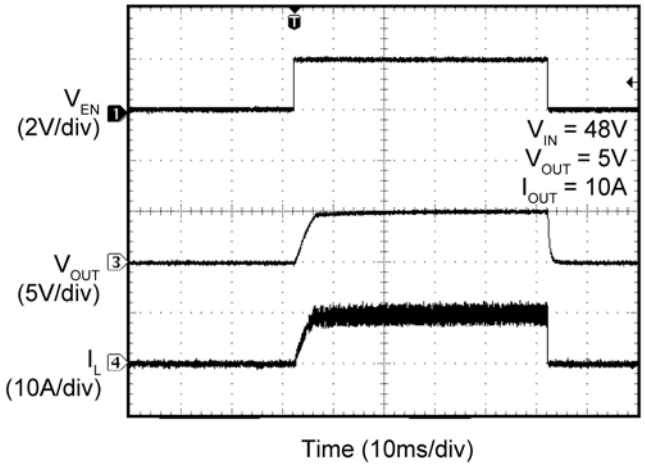


MIC2103 V_{IN} Start-up with Pre-Biased Output

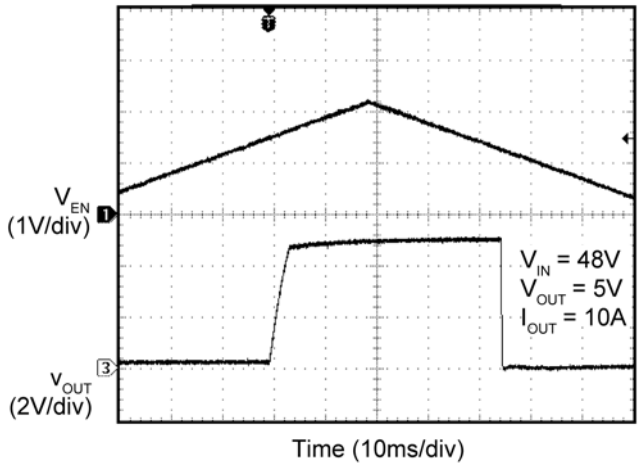


Functional Characteristics (Continued)

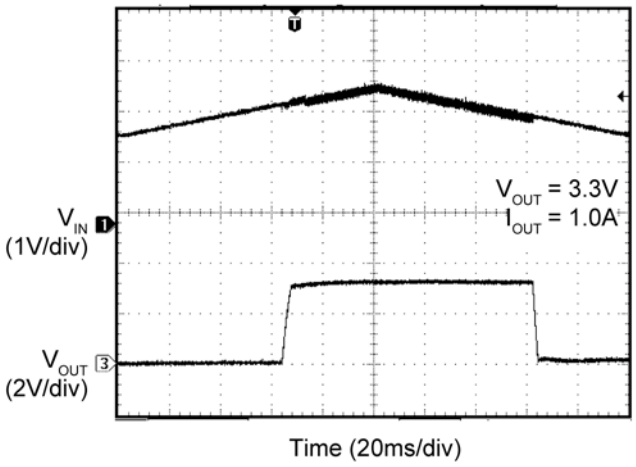
Enable Turn-On/Turn-Off



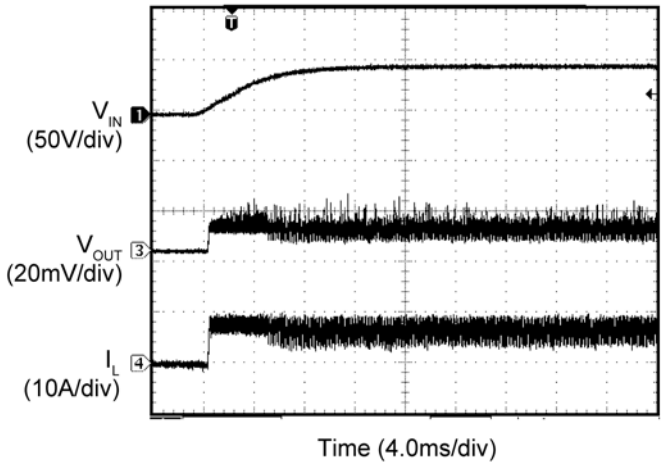
Enable Thresholds



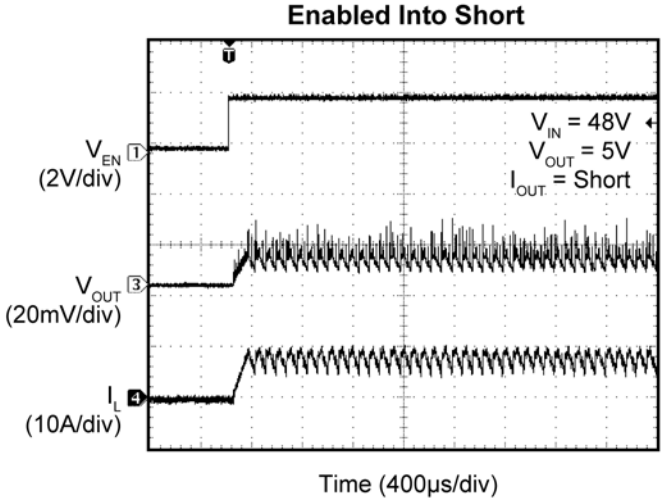
V_{IN} UVLO Thresholds



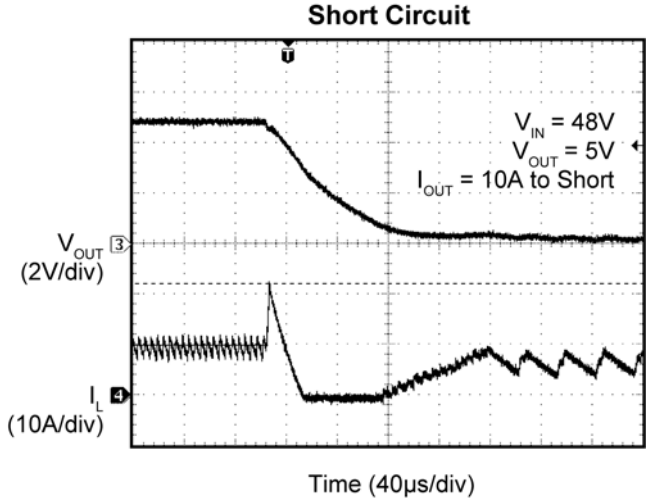
Power Up into Short Circuit



Enabled Into Short

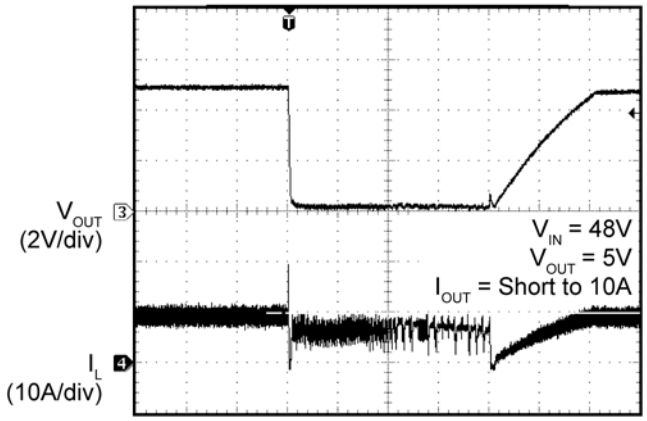


Short Circuit

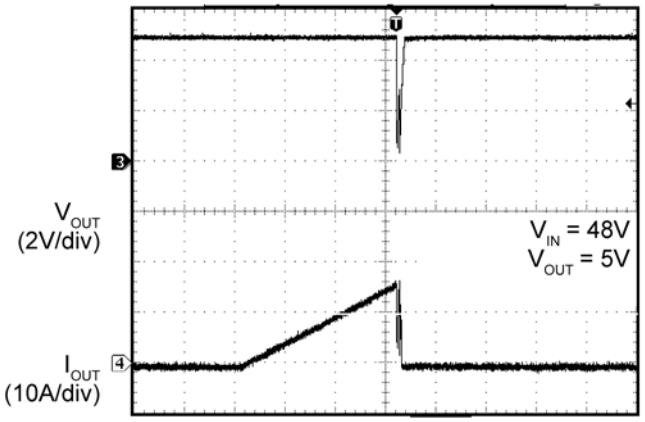


Functional Characteristics (Continued)

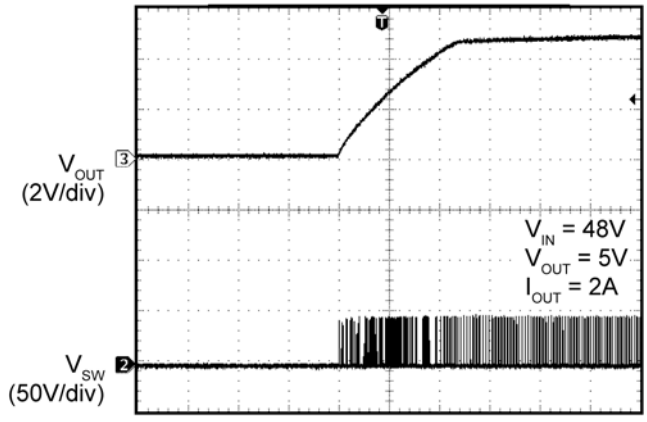
Output Recovery from Short Circuit



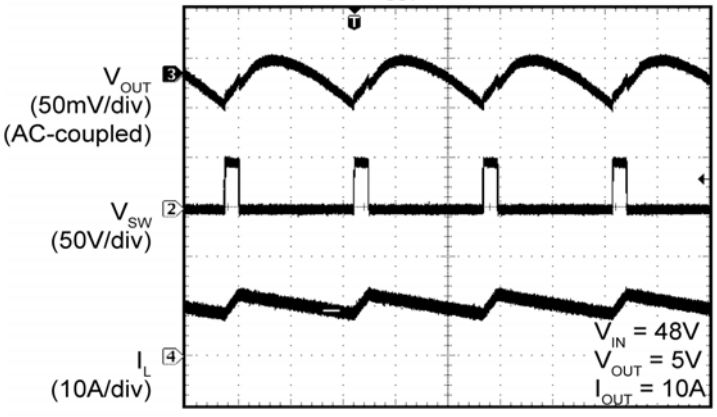
Output Peak Current Limit Threshold



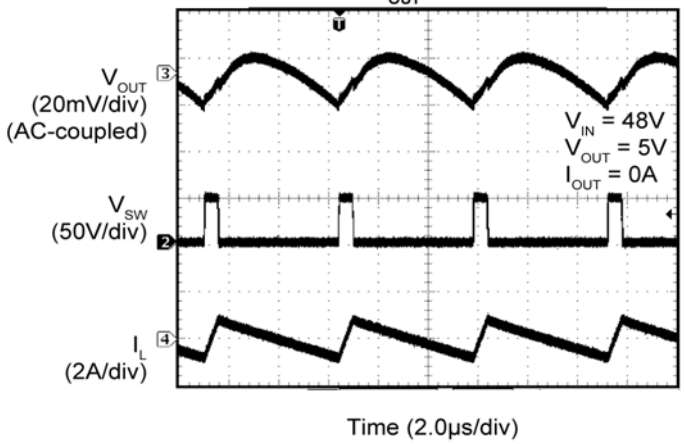
Output Recovery from Thermal Shutdown



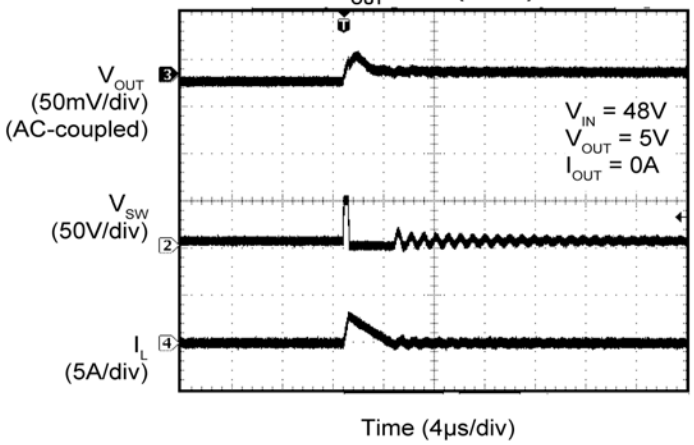
MIC2104 Switching Waveforms
I_{OUT} = 10A



MIC2104 Switching Waveforms
I_{OUT} = 0A

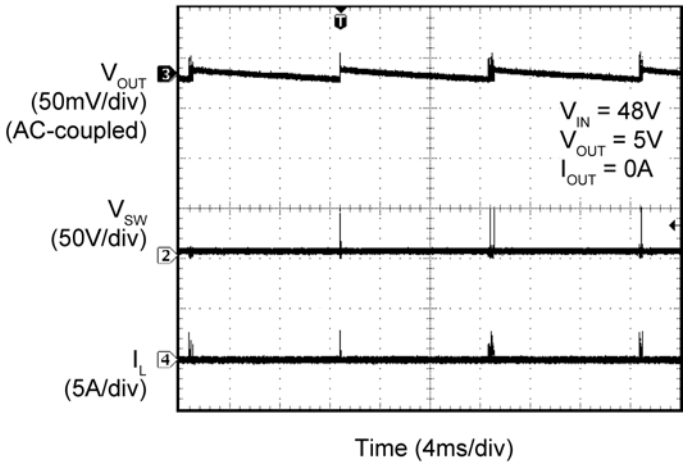


MIC2103 Switching Waveforms
I_{OUT} = 0A (DCM)

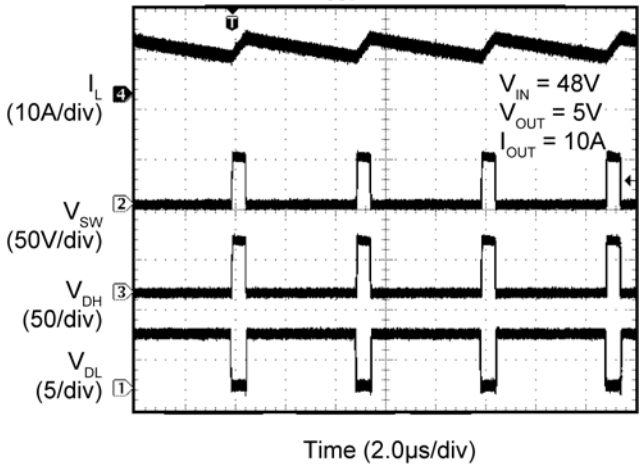


Functional Characteristics (Continued)

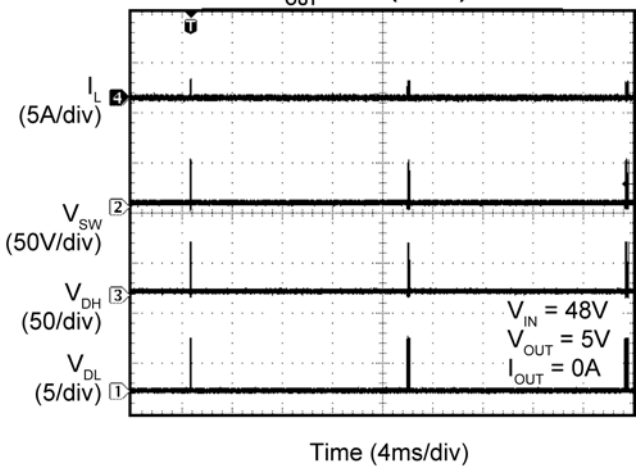
MIC2103 Switching Waveforms
I_{OUT} = 0A (DCM)



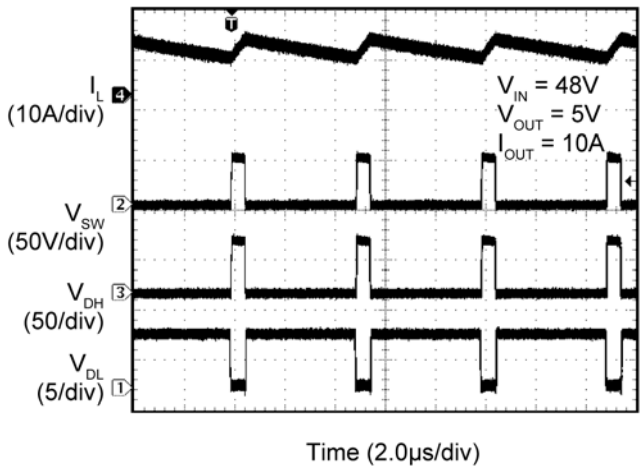
MIC2103 Switching Waveforms
I_{OUT} = 10A



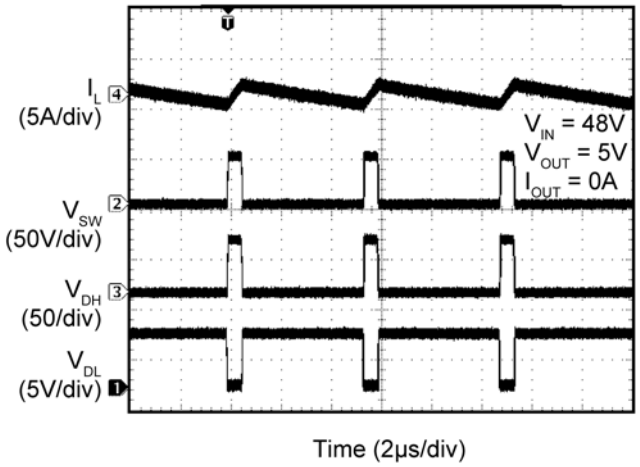
MIC2103 Switching Waveforms
I_{OUT} = 0A (DCM)



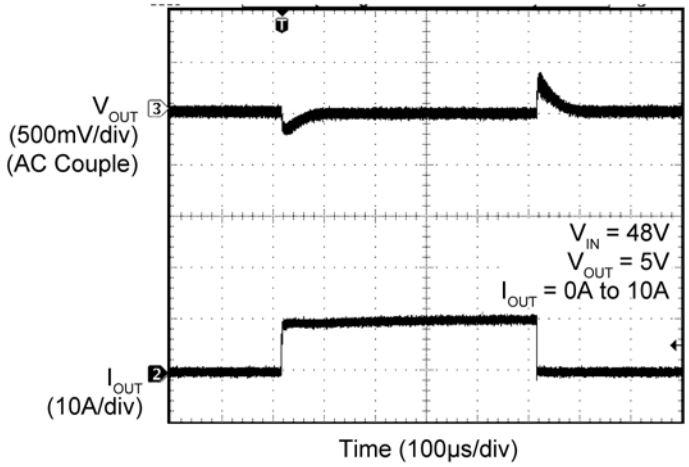
MIC2104 Switching Waveforms
I_{OUT} = 10A



MIC2104 Switching Waveforms; I_{OUT} = 0A

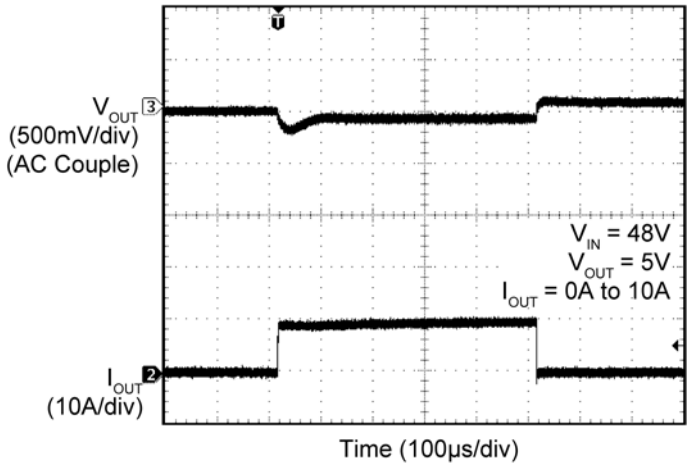


MIC2104 Transient Response

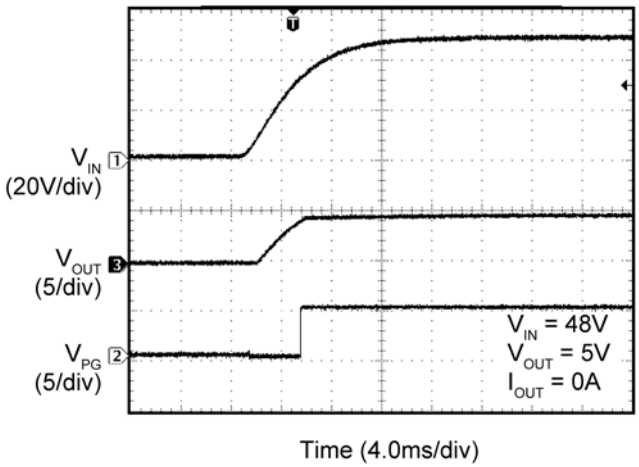


Functional Characteristics (Continued)

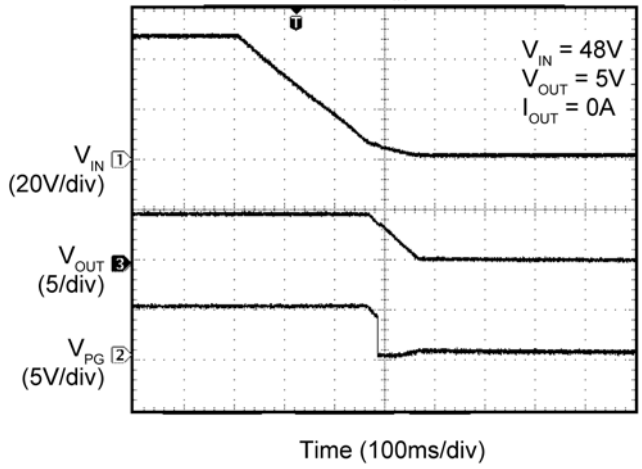
MIC2103 Transient Response



Power Good at V_{IN} Soft Turn-On



Power Good at V_{IN} Soft Turn-Off



Functional Diagram

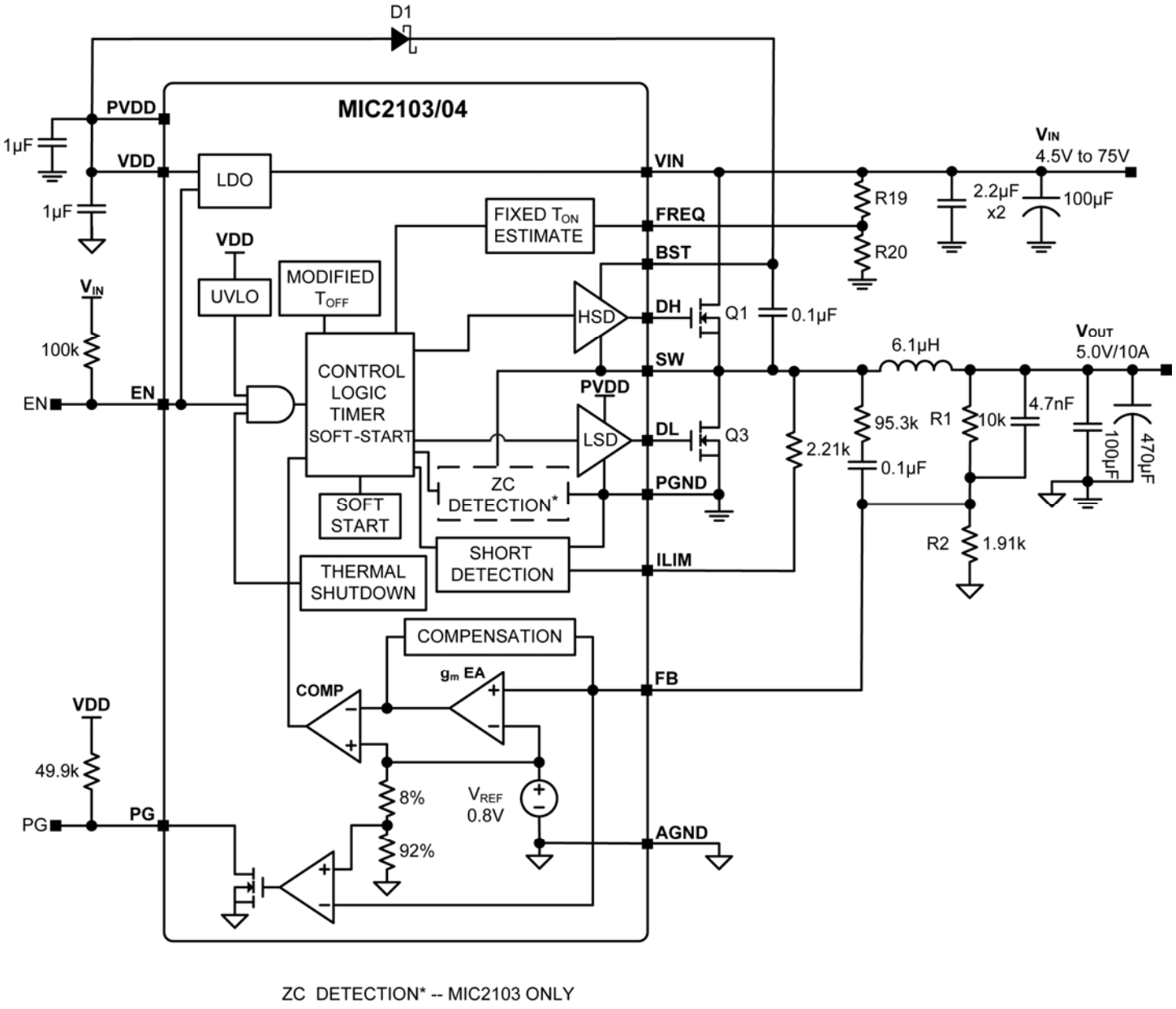


Figure 1. MIC2103/04 Functional Diagram

Functional Description

The MIC2103/04 are adaptive on-time synchronous buck controllers built for high-input voltage to low-output voltage conversion applications. They are designed to operate over a wide input voltage range, from 4.5V to 75V, and the output is adjustable with an external resistive divider. An adaptive on-time control scheme is employed to obtain a constant switching frequency and to simplify the control compensation. Over-current protection is implemented by sensing low-side MOSFET's $R_{DS(ON)}$. The device features internal soft-start, enable, UVLO, and thermal shutdown.

Theory of Operation

Figure 1 illustrates the block diagram of the MIC2103/04. The output voltage is sensed by the MIC2103/04 feedback pin FB via the voltage divider R1 and R2, and compared to a 0.8V reference voltage V_{REF} at the error comparator through a low-gain transconductance (g_m) amplifier. If the feedback voltage decreases and the amplifier output is below 0.8V, thenthe error comparator will trigger the control logic and generate an ON-time period. The ON-time period length is predetermined by the "Fixed t_{ON} Estimator" circuitry:

$$t_{ON(estimated)} = \frac{V_{OUT}}{V_{IN} \times f_{SW}} \qquad \text{(Eq. 1)}$$

where V_{OUT} is the output voltage, V_{IN} is the power stage input voltage, and f_{SW} is the switching frequency.

At the end of the ON-time period, the internal high-side driver turns off the high-side MOSFET and the low-side driver turns on the low-side MOSFET. The OFF-time period length depends upon the feedback voltage in most cases. When the feedback voltage decreases and the output of the g_m amplifier is below 0.8V, the ON-time period is triggered and the OFF-time period ends. If the OFF-time period determined by the feedback voltage is less than the minimum OFF-time $t_{OFF(min)}$, which is about 200ns, the MIC2103/04 control logic will apply the $t_{OFF(min)}$ instead. $T_{OFF(min)}$ is required to maintain enough energy in the boost capacitor (C_{BST}) to drive the high-side MOSFET.

The maximum duty cycle is obtained from the 200ns $t_{OFF(min)}$:

$$D_{MAX} = \frac{t_S - t_{OFF(MIN)}}{t_S} = 1 - \frac{200ns}{t_S} \qquad \text{(Eq. 2)}$$

where $t_S = 1/f_{SW}$. It is not recommended to use MIC2103/04 with a OFF-time close to $t_{OFF(min)}$ during steady-state operation.

The adaptive ON-time control scheme results in a constant switching frequency in the MIC2103/04. The actual ON-time and resulting switching frequency will vary with the different rising and falling times of the external MOSFETs. Also, the minimum t_{ON} results in a lower switching frequency in high V_{IN} to V_{OUT} applications. During load transients, the switching frequency is changed due to the varying OFF-time.

To illustrate the control loop operation, we will analyze both the steady-state and load transient scenarios. For easy analysis, the gain of the g_m amplifier is assumed to be 1. With this assumption, the inverting input of the error comparator is the same as the feedback voltage.

Figure 2 shows the MIC2103/04 control loop timing during steady-state operation. During steady-state, the g_m amplifier senses the feedback voltage ripple, which is proportional to the output voltage ripple plus injected voltage ripple, to trigger the ON-time period. The ON-time is predetermined by the t_{ON} estimator. The termination of the OFF-time is controlled by the feedback voltage. At the valley of the feedback voltage ripple, which occurs when V_{FB} falls below V_{REF}, the OFF period ends and the next ON-time period is triggered through the control logic circuitry.

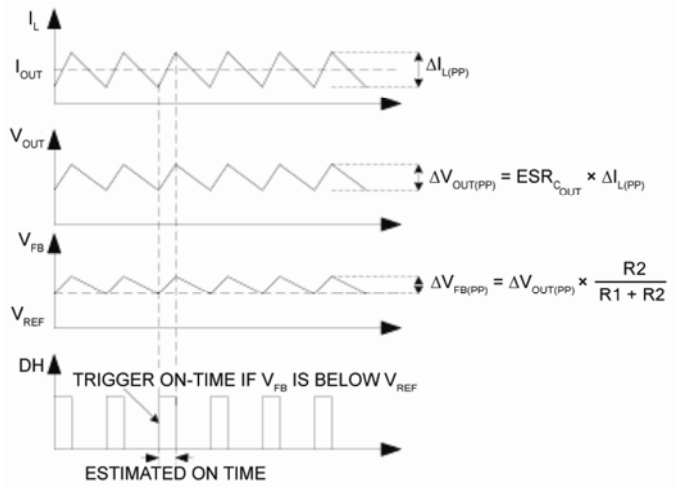


Figure 2. MIC2103/04 Control Loop Timing

Figure 3a shows the operation of the MIC2103/04 during a load transient. The output voltage drops due to the sudden load increase, which causes the V_{FB} to be less than V_{REF}. This will cause the error comparator to trigger an ON-time period. At the end of the ON-time period, a minimum OFF-time $t_{OFF(min)}$ is generated to charge C_{BST} since the feedback voltage is still below V_{REF}. Then, the next ON-time period is triggered due to the low feedback voltage. Therefore, the switching frequency changes during the load transient, but returns to the nominal fixed frequency once the output has stabilized at the new load current level. With the varying duty cycle and switching frequency, the output recovery time is fast and the output voltage deviation is small in MIC2103/04 converter.

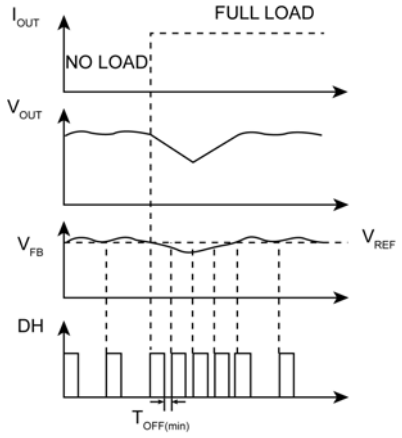


Figure 3a. MIC2103/04 Load Transient Response

Unlike true current-mode control, the MIC2103/04 uses the output voltage ripple to trigger an ON-time period. The output voltage ripple is proportional to the inductor current ripple if the ESR of the output capacitor is large enough.

In order to meet the stability requirements, the MIC2103/04 feedback voltage ripple should be in phase with the inductor current ripple and are large enough to be sensed by the g_m amplifier and the error comparator. The recommended feedback voltage ripple is 20mV~100mV over full input voltage range. If a low ESR output capacitor is selected, then the feedback voltage ripple may be too small to be sensed by the g_m amplifier and the error comparator. Also, the output voltage ripple and the feedback voltage ripple are not necessarily in phase with the inductor current ripple if the ESR of the output capacitor is very low. In these cases, ripple injection is required to ensure proper operation. Please refer to "Ripple Injection" subsection in *Application Information* for more details about the ripple injection technique.

Discontinuous Mode (MIC2103 only)

In continuous mode, the inductor current is always greater than zero; however, at light loads, the MIC2103 is able to force the inductor current to operate in discontinuous mode. Discontinuous mode is where the inductor current falls to zero, as indicated by trace (I_L) shown in Figure 3b. During this period, the efficiency is optimized by shutting down all the non-essential circuits and minimizing the supply current. The MIC2103 wakes up and turns on the high-side MOSFET when the feedback voltage V_{FB} drops below 0.8V.

The MIC2103 has a zero crossing comparator (ZC Detection) that monitors the inductor current by sensing the voltage drop across the low-side MOSFET during its ON-time. If the V_{FB} > 0.8V and the inductor current goes slightly negative, then the MIC2103 automatically powers down most of the IC circuitry and goes into a low-power mode.

Once the MIC2103 goes into discontinuous mode, both LSD and HSD are low, which turns off the high-side and low-side MOSFETs. The load current is supplied by the output capacitors and V_{OUT} drops. If the drop of V_{OUT} causes V_{FB} to go below V_{REF}, then all the circuits will wake up into normal continuous mode. First, the bias currents of most circuits reduced during the discontinuous mode are restored, then a t_{ON} pulse is triggered before the drivers are turned on to avoid any possible glitches. Finally, the high-side driver is turned on. Figure 3b shows the control loop timing in discontinuous mode.

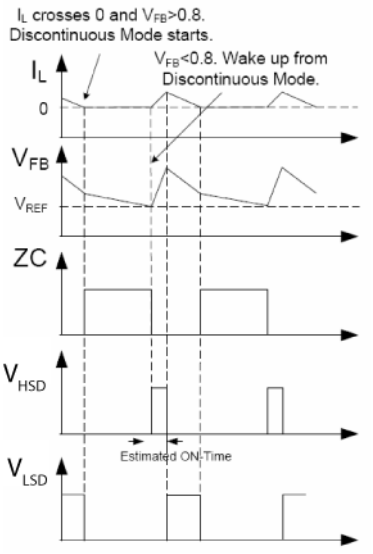


Figure 3b. MIC2103 Control Loop Timing (Discontinuous Mode)

During discontinuous mode, the bias current of most circuits are reduced. As a result, the total power supply current during discontinuous mode is only about 400μA, allowing the MIC2103 to achieve high efficiency in light load applications.

Soft-Start

Soft-start reduces the power supply input surge current at startup by controlling the output voltage rise time. The input surge appears while the output capacitor is charged up. A slower output rise time will draw a lower input surge current.

The MIC2103/04 implements an internal digital soft-start by making the 0.8V reference voltage V_{REF} ramp from 0 to 100% in about 6ms with 9.7mV steps. Therefore, the output voltage is controlled to increase slowly by a stair-case V_{FB} ramp. Once the soft-start cycle ends, the related circuitry is disabled to reduce current consumption. V_{DD} must be powered up at the same time or after V_{IN} to make the soft-start function correctly.

Current Limit

The MIC2103/04 uses the $R_{DS(ON)}$ and external resistor connected from ILIM pin to SW node to decide the current limit.

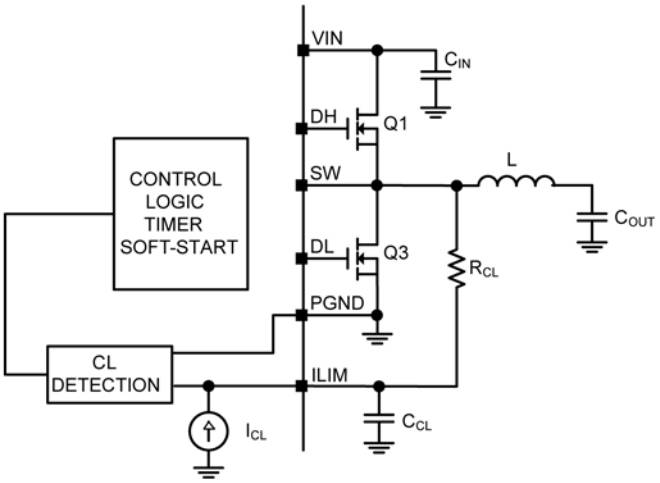


Figure 4. MIC2103/04 Current Limiting Circuit

In each switching cycle of the MIC2103/04 converter, the inductor current is sensed by monitoring the low-side MOSFET in the OFF period. The sensed voltage V(ILIM) is compared with the power ground (PGND) after a blanking time of 150nS. In this way the drop voltage over the resistor R_{CL} (V_{CL}) is compared with the drop over the bottom FET generating the short current limit. The small capacitor (C_{CL}) connected from ILIM pin to PGND filters the switching node ringing during the off time allowing a better short limit measurement. The time constant created by R_{CL} and C_{CL} should be much less than the minimum off time.

The V_{CL} drop allows programming of short limit through the value of the resistor (R_{CL}), If the absolute value of the voltage drop on the bottom FET is greater than $V_{CL'}$ in that case the V(ILIM) is lower than PGND and a short circuit event is triggered. A hiccup cycle to treat the short event is generated. The hiccup sequence including the soft start reduces the stress on the switching FETs and protects the load and supply for severe short conditions.

The short circuit current limit can be programmed by using the following formula.

$$R_{CL} = \frac{(I_{CLIM} - \Delta_{PP} \times 0.5) \times R_{DS(ON)} + V_{CL}}{I_{CL}} \qquad \text{(Eq. 3)}$$

Where I_{SH} = Desired Current limit

Δ_{PP} = Inductor current peak to peak

$R_{DS\ (ON)}$ = On resistance of low-side power MOSFET

V_{CL} = Current limit threshold, the typical value is 14mV in EC table

I_{CL} = Current Limit source current, the typical value is 80μA in EC table.

In case of hard short, the short limit is folded down to allow an indefinite hard short on the output without any destructive effect. It is mandatory to make sure that the inductor current used to charge the output capacitance during soft start is under the folded short limit, otherwise the supply will go in hiccup mode and may not be finishing the soft start successfully.

The MOSFET $R_{DS(ON)}$ varies 30 to 40% with temperature; therefore, it is recommended to add a 50% margin to I_{CL} in the above equation to avoid false current limiting due to increased MOSFET junction temperature rise. It is also recommended to connect SW pin directly to the drain of the low-side MOSFET to accurately sense the MOSFETs $R_{DS(ON)}$.

MOSFET Gate Drive

The MIC2103/04 high-side drive circuit is designed to switch an N-Channel MOSFET. Figure 1 shows a bootstrap circuit, consisting of D1 (a Schottky diode is recommended) and C_{BST}. This circuit supplies energy to the high-side drive circuit. Capacitor C_{BST} is charged while the low-side MOSFET is on and the voltage on the SW pin is approximately 0V. When the high-side MOSFET driver is turned on, energy from C_{BST} is used to turn the MOSFET on. As the high-side MOSFET turns on, the voltage on the SW pin increases to approximately V_{IN}. Diode D1 is reverse biased and C_{BST} floats high while continuing to keep the high-side MOSFET on. The bias current of the high-side driver is less than 10mA so a 0.1µF to 1µF is sufficient to hold the gate voltage with minimal droop for the power stroke (high-side switching) cycle, i.e., ΔBST = 10mA x 3.33µs/0.1µF = 333mV. When the low-side MOSFET is turned back on, C_{BST} is recharged through D1. A small resistor R_G, which is in series with C_{BST}, can be used to slow down the turn-on time of the high-side N-channel MOSFET.

The drive voltage is derived from the V_{DD} supply voltage. The nominal low-side gate drive voltage is V_{DD} and the nominal high-side gate drive voltage is approximately $V_{DD} – V_{DIODE}$, where V_{DIODE} is the voltage drop across D1. An approximate 30ns delay between the high-side and low-side driver transitions is used to prevent current from simultaneously flowing unimpeded through both MOSFETs.

Application Information

Setting the Switching Frequency

The MIC2103/04 are adjustable-frequency, synchronous buck controllers featuring a unique adaptive on-time control architecture. The switching frequency can be adjusted between 200kHz and 600kHz by changing the resistor divider network consisting of R19 and R20.

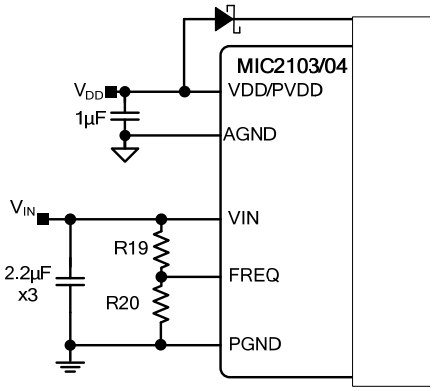


Figure 5. Switching Frequency Adjustment

The following formula gives the estimated switching frequency:

$$f_{SW\_ADJ} = f_O \times \frac{R20}{R19 + R20} \qquad \text{(Eq. 4)}$$

Where f_O = Switching Frequency when R19 is 100k and R20 being open, f_O is typically 550kHz. For a more precise setting, it is recommended to use the following graph:

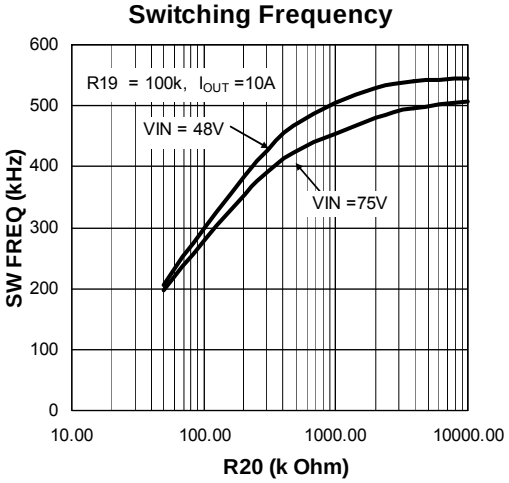


Figure 6. Switching Frequency vs. R20

MOSFET Selection

The MIC2103/04 controllers work from input voltages of 4.5V to 75V and have an internal 5V V_{DD} LDO. This internal V_{DD} LDO provides power to turn the external N-Channel power MOSFETs for the high-side and low-side switches. For applications where V_{DD} < 5V, it is necessary that the power MOSFETs used are sub-logic level and are in full conduction mode for V_{GS} of 2.5V. For applications when V_{DD} > 5V; logic-level MOSFETs, whose operation is specified at V_{GS} = 4.5V must be used.

There are different criteria for choosing the high-side and low-side MOSFETs. These differences are more significant at lower duty cycles. In such an application, the high-side MOSFET is then required to switch as quickly as possible in order to minimize transition losses, whereas the low-side MOSFET can switch slower, but must handle larger RMS currents. When the duty cycle approaches 50%, the current carrying capability of the high-side MOSFET starts to become critical.

It is important to note that the on-resistance of a MOSFET increases with increasing temperature. A 75°C rise in junction temperature will increase the channel resistance of the MOSFET by 50% to 75% of the resistance specified at 25°C. This change in resistance must be accounted for when calculating MOSFET power dissipation and in calculating the value of current limit. Total gate charge is the charge required to turn the MOSFET on and off under specified operating conditions (V_{DS} and V_{GS}). The gate charge is supplied by the MIC2103/04 gate-drive circuit. At 200kHz switching frequency, the gate charge can be a significant source of power dissipation in the MIC2103/04. At low output load, this power dissipation is noticeable as a reduction in efficiency. The average current required to drive the high-side MOSFET is:

$$I_{G[high\text{-}side]}(avg) = Q_G \times f_{SW} \qquad \text{(Eq. 5)}$$

where:

$I_{G[high\text{-}side]}(avg)$ = Average high-side MOSFET gate current

Q_G = Total gate charge for the high-side MOSFET taken from the manufacturer's data sheet for $V_{GS} = V_{DD}$.

f_{SW} = Switching Frequency

The low-side MOSFET is turned on and off at V_{DS} = 0 because an internal body diode or external freewheeling diode is conducting during this time. The switching loss for the low-side MOSFET is usually negligible. Also, the

gate-drive current for the low-side MOSFET is more accurately calculated using C_{ISS} at V_{DS} = 0 instead of gate charge.

For the low-side MOSFET:

$$I_{G[low-side]}(avg) = C_{ISS} \times V_{GS} \times f_{SW} \quad \text{(Eq. 6)}$$

Since the current from the gate drive comes from the V_{DD}, the power dissipated in the MIC2103/04 due to gate drive is:

$$P_{GATEDRIVE} = V_{DD} \times (I_{G[high-side]}(avg) + I_{G[low-side]}(avg)) \quad \text{(Eq. 7)}$$

A convenient figure of merit for switching MOSFETs is the on resistance multiplied by the total gate charge; $R_{DS(ON)}$ × Q_G. Lower numbers translate into higher efficiency. Low gate-charge logic-level MOSFETs are a good choice for use with the MIC2103/04. Also, the $R_{DS(ON)}$ of the low-side MOSFET will determine the current-limit value. Please refer to "Current Limit" subsection is *Functional Description* for more details.

Parameters that are important to MOSFET switch selection are:

- Voltage rating
- On-resistance
- Total gate charge

The voltage ratings for the high-side and low-side MOSFETs are essentially equal to the power stage input voltage V_{HSD}. A safety factor of 20% should be added to the V_{DS}(max) of the MOSFETs to account for voltage spikes due to circuit parasitic elements.

The power dissipated in the MOSFETs is the sum of the conduction losses during the on-time ($P_{CONDUCTION}$) and the switching losses during the period of time when the MOSFETs turn on and off (P_{AC}).

$$P_{SW} = P_{CONDUCTION} + P_{AC} \quad \text{(Eq. 8)}$$

$$P_{CONDUCTION} = I_{SW(RMS)}^2 \times R_{DS(ON)} \quad \text{(Eq. 9)}$$

$$P_{AC} = P_{AC(off)} + P_{AC(on)} \quad \text{(Eq. 10)}$$

where:

$R_{DS(ON)}$ = On-resistance of the MOSFET switch

D = Duty Cycle = V_{OUT} / V_{HSD}

Making the assumption that the turn-on and turn-off transition times are equal; the transition times can be approximated by:

$$t_T = \frac{C_{ISS} \times V_{IN} + C_{OSS} \times V_{HSD}}{I_G} \quad \text{(Eq. 11)}$$

where:

C_{ISS} and C_{OSS} are measured at V_{DS} = 0

I_G = Gate-drive current

The total high-side MOSFET switching loss is:

$$P_{AC} = (V_{HSD} + V_D) \times I_{PK} \times t_T \times f_{SW} \quad \text{(Eq. 12)}$$

where:

t_T = Switching transition time

V_D = Body diode drop (0.5V)

f_{SW} = Switching Frequency

The high-side MOSFET switching losses increase with the switching frequency and the input voltage V_{HSD}. The low-side MOSFET switching losses are negligible and can be ignored for these calculations.

Inductor Selection

Values for inductance, peak, and RMS currents are required to select the output inductor. The input and output voltages and the inductance value determine the peak-to-peak inductor ripple current. Generally, higher inductance values are used with higher input voltages. Larger peak-to-peak ripple currents will increase the power dissipation in the inductor and MOSFETs. Larger output ripple currents will also require more output capacitance to smooth out the larger ripple current. Smaller peak-to-peak ripple currents require a larger inductance value and therefore a larger and more expensive inductor.

A good compromise between size, loss and cost is to set the inductor ripple current to be equal to 20% of the maximum output current.

The inductance value is calculated by Equation 13:

$$L = \frac{V_{OUT} \times (V_{IN(max)} - V_{OUT})}{V_{IN(max)} \times f_{sw} \times 20\% \times I_{OUT(max)}} \quad \text{(Eq. 13)}$$

where:

f_{SW} = Switching frequency

20% = Ratio of AC ripple current to DC output current

$V_{IN(max)}$ = Maximum power stage input voltage

The peak-to-peak inductor current ripple is:

$$\Delta I_{L(pp)} = \frac{V_{OUT} \times (V_{IN(max)} - V_{OUT})}{V_{IN(max)} \times f_{sw} \times L} \quad \text{(Eq. 14)}$$

The peak inductor current is equal to the average output current plus one half of the peak-to-peak inductor current ripple.

$$I_{L(pk)} = I_{OUT(max)} + 0.5 \times \Delta I_{L(pp)} \quad \text{(Eq. 15)}$$

The RMS inductor current is used to calculate the I^2R losses in the inductor.

$$I_{L(RMS)} = \sqrt{I_{OUT(max)}^2 + \frac{\Delta I_{L(PP)}^2}{12}} \quad \text{(Eq. 16)}$$

Maximizing efficiency requires the proper selection of core material and minimizing the winding resistance. The high frequency operation of the MIC2103/04 requires the use of ferrite materials for all but the most cost sensitive applications. Lower cost iron powder cores may be used but the increase in core loss will reduce the efficiency of the power supply. This is especially noticeable at low output power. The winding resistance decreases efficiency at the higher output current levels. The winding resistance must be minimized although this usually comes at the expense of a larger inductor. The power dissipated in the inductor is equal to the sum of the core and copper losses. At higher output loads, the core losses are usually insignificant and can be ignored. At lower output currents, the core losses can be a significant contributor. Core loss information is usually available from the magnetic vendor.

Copper loss in the inductor is calculated by Equation 17:

$$P_{INDUCTOR(Cu)} = I_{L(RMS)}^2 \times R_{WINDING} \quad \text{(Eq. 17)}$$

The resistance of the copper wire, $R_{WINDING}$, increases with the temperature. The value of the winding resistance used should be at the operating temperature.

$$P_{WINDING(Ht)} = R_{WINDING(20°C)} \times (1 + 0.0042 \times (T_H - T_{20°C})) \quad \text{(Eq. 18)}$$

where:

T_H = temperature of wire under full load

$T_{20°C}$ = ambient temperature

$R_{WINDING(20°C)}$ = room temperature winding resistance (usually specified by the manufacturer)

Output Capacitor Selection

The type of the output capacitor is usually determined by its ESR (equivalent series resistance). Voltage and RMS current capability are two other important factors for selecting the output capacitor. Recommended capacitor types are tantalum, low-ESR aluminum electrolytic, OS-CON and POSCAP. The output capacitor's ESR is usually the main cause of the output ripple. The output capacitor ESR also affects the control loop from a stability point of view. The maximum value of ESR is calculated:

$$ESR_{C_{OUT}} \leq \frac{\Delta V_{OUT(pp)}}{\Delta I_{L(PP)}} \quad \text{(Eq. 19)}$$

where:

$\Delta V_{OUT(pp)}$ = peak-to-peak output voltage ripple

$\Delta I_{L(PP)}$ = peak-to-peak inductor current ripple

The total output ripple is a combination of the ESR and output capacitance. The total ripple is calculated in Equation 20:

$$\Delta V_{OUT(pp)} = \sqrt{\left(\frac{\Delta I_{L(PP)}}{C_{OUT} \times f_{SW} \times 8}\right)^2 + \left(\Delta I_{L(PP)} \times ESR_{C_{OUT}}\right)^2} \quad \text{(Eq. 20)}$$

where:

D = duty cycle

C_{OUT} = output capacitance value

f_{sw} = switching frequency

As described in the "Theory of Operation" subsection in *Functional Description*, the MIC2103/04 requires at least 20mV peak-to-peak ripple at the FB pin to make the g_m amplifier and the error comparator behave properly. Also, the output voltage ripple should be in phase with the inductor current. Therefore, the output voltage ripple caused by the output capacitors value should be much

smaller than the ripple caused by the output capacitor ESR. If low ESR capacitors, such as ceramic capacitors, are selected as the output capacitors, a ripple injection method should be applied to provide enough feedback voltage ripple. Please refer to the "Ripple Injection" subsection for more details.

The voltage rating of the capacitor should be twice the output voltage for a tantalum and 20% greater for aluminum electrolytic or OS-CON. The output capacitor RMS current is calculated in Equation 21:

$$I_{C_{OUT}(RMS)} = \frac{\Delta I_{L(PP)}}{\sqrt{12}} \quad \text{(Eq. 21)}$$

The power dissipated in the output capacitor is:

$$P_{DISS(C_{OUT})} = I_{C_{OUT}(RMS)}^{2} \times ESR_{C_{OUT}} \quad \text{(Eq. 22)}$$

Input Capacitor Selection

The input capacitor for the power stage input V_{IN} should be selected for ripple current rating and voltage rating. Tantalum input capacitors may fail when subjected to high inrush currents, caused by turning the input supply on. A tantalum input capacitor's voltage rating should be at least two times the maximum input voltage to maximize reliability. Aluminum electrolytic, OS-CON, and multilayer polymer film capacitors can handle the higher inrush currents without voltage de-rating. The input voltage ripple will primarily depend on the input capacitor's ESR. The peak input current is equal to the peak inductor current, so:

$$\Delta V_{IN} = I_{L(pk)} \times ESR_{CIN} \quad \text{(Eq. 23)}$$

The input capacitor must be rated for the input current ripple. The RMS value of input capacitor current is determined at the maximum output current. Assuming the peak-to-peak inductor current ripple is low:

$$I_{CIN(RMS)} \approx I_{OUT(max)} \times \sqrt{D \times (1-D)} \quad \text{(Eq. 24)}$$

The power dissipated in the input capacitor is:

$$P_{DISS(CIN)} = I_{CIN(RMS)}^{2} \times ESR_{CIN} \quad \text{(Eq. 25)}$$

Voltage Setting Components

The MIC2103 requires two resistors to set the output voltage as shown in Figure 7:

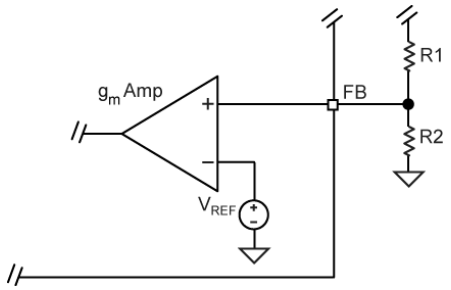


Figure 7. Voltage-Divider Configuration

The output voltage is determined by the equation:

$$V_{OUT} = V_{FB} \times (1 + \frac{R1}{R2}) \quad \text{(Eq. 26)}$$

where, V_{FB} = 0.8V. A typical value of R1 can be between 3kΩ and 10kΩ. If R1 is too large, it may allow noise to be introduced into the voltage feedback loop. If R1 is too small in value, it will decrease the efficiency of the power supply, especially at light loads. Once R1 is selected, R2 can be calculated using:

$$R2 = \frac{V_{FB} \times R1}{V_{OUT} - V_{FB}} \quad \text{(Eq. 27)}$$

Ripple Injection

The V_{FB} ripple required for proper operation of the MIC2103/04 g_m amplifier and error comparator is 20mV to 100mV. However, the output voltage ripple is generally designed as 1% to 2% of the output voltage. For a low output voltage, such as a 1V, the output voltage ripple is only 10mV to 20mV, and the feedback voltage ripple is less than 20mV. If the feedback voltage ripple is so small that the g_m amplifier and error comparator cannot sense it, then the MIC2103/04 will lose control and the output voltage is not regulated. In order to have some amount of V_{FB} ripple, a ripple injection method is applied for low output voltage ripple applications.

The applications are divided into three situations according to the amount of the feedback voltage ripple:

1. Enough ripple at the feedback voltage due to the large ESR of the output capacitors.

   As shown in Figure 8a, the converter is stable without any ripple injection. The feedback voltage ripple is:

$$\Delta V_{FB(pp)} = \frac{R2}{R1+R2} \times ESR_{C_{OUT}} \times \Delta I_{L(pp)} \quad \text{(Eq. 28)}$$

where $\Delta I_{L(pp)}$ is the peak-to-peak value of the inductor current ripple.

2. Inadequate ripple at the feedback voltage due to the small ESR of the output capacitors.

   The output voltage ripple is fed into the FB pin through a feed-forward capacitor C_{ff} in this situation, as shown in Figure 8b. The typical C_{ff} value is between 1nF and 100nF. With the feed-forward capacitor, the feedback voltage ripple is very close to the output voltage ripple:

$$\Delta V_{FB(pp)} \approx ESR \times \Delta I_{L(pp)} \quad \text{(Eq. 29)}$$

3. Virtually no ripple at the FB pin voltage due to the very-low ESR of the output capacitors:

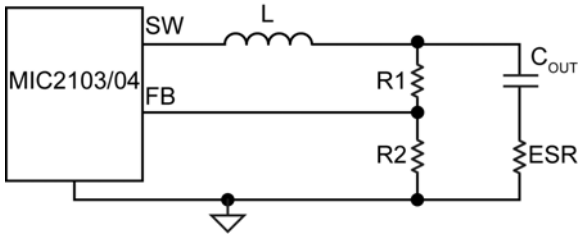


Figure 8a. Enough Ripple at FB

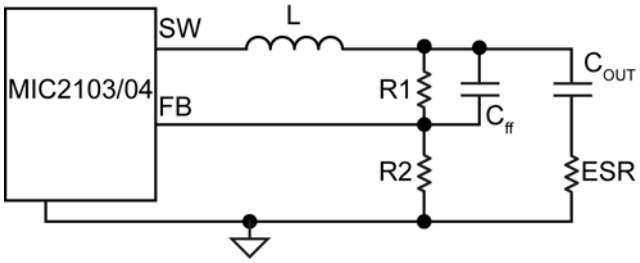


Figure 8b. Inadequate Ripple at FB

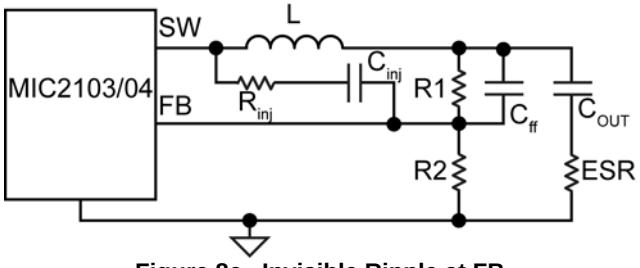


Figure 8c. Invisible Ripple at FB

In this situation, the output voltage ripple is less than 20mV. Therefore, additional ripple is injected into the FB pin from the switching node SW via a resistor R_{inj} and a capacitor C_{inj}, as shown in Figure 8c. The injected ripple is:

$$\Delta V_{FB(pp)} = V_{IN} \times K_{div} \times D \times (1-D) \times \frac{1}{f_{SW} \times \tau} \quad \text{(Eq. 30)}$$

$$K_{div} = \frac{R1//R2}{R_{inj} + R1//R2} \quad \text{(Eq. 31)}$$

where:

V_{IN} = Power stage input voltage

D = Duty cycle

f_{SW} = Switching frequency

$\tau = (R1//R2//R_{inj}) \times C_{ff}$

In Equations 30 and 32, it is assumed that the time constant associated with C_{ff} must be much greater than the switching period:

$$\frac{1}{f_{SW} \times \tau} = \frac{T}{\tau} << 1 \quad \text{(Eq. 32)}$$

If the voltage divider resistors R1 and R2 are in the kΩ range, then a C_{ff} of 1nF to 100nF can easily satisfy the large time constant requirements. Also, a 100nF injection capacitor C_{inj} is used in order to be considered as short for a wide range of the frequencies.

The process of sizing the ripple injection resistor and capacitors is:

Step 1. Select C_{ff} to feed all output ripples into the feedback pin and make sure the large time constant assumption is satisfied. Typical choice of C_{ff} is 1nF to 100nF if R1 and R2 are in kΩ range.

Step 2. Select R_{inj} according to the expected feedback voltage ripple using Equation 33:

$$K_{div} = \frac{\Delta V_{FB(pp)}}{V_{IN}} \times \frac{f_{SW} \times \tau}{D \times (1-D)} \quad \text{(Eq. 33)}$$

Then the value of R_{inj} is obtained as:

$$R_{inj} = (R1//R2) \times \left(\frac{1}{K_{div}} - 1\right) \quad \text{(Eq. 34)}$$

Step 3. Select C_{inj} as 100nF, which could be considered as short for a wide range of the frequencies.

PCB Layout Guidelines

Warning: To minimize EMI and output noise, follow these layout recommendations.

PCB Layout is critical to achieve reliable, stable and efficient performance. A ground plane is required to control EMI and minimize the inductance in power, signal and return paths.

The following guidelines should be followed to insure proper operation of the MIC2103 converter.

IC

- The 1µF ceramic capacitors, which are connected to the VDD and PVDD pins, must be located right at the IC. The VDD pin is very noise sensitive and placement of the capacitor is very critical. Use wide traces to connect to the VDD and PGND pins.
- The signal ground pin (GND) must be connected directly to the ground planes. Do not route the GND pin to the PGND pin on the top layer.
- Place the IC close to the point of load (POL).
- Use fat traces to route the input and output power lines.
- Signal and power grounds should be kept separate and connected at only one location.

Input Capacitor

- Place the input capacitor next.
- Place the input capacitors on the same side of the board and as close to the MOSFETs as possible.
- Place several vias to the ground plane close to the input capacitor ground terminal.
- Use either X7R or X5R dielectric input capacitors. Do not use Y5V or Z5U type capacitors.
- Do not replace the ceramic input capacitor with any other type of capacitor. Any type of capacitor can be placed in parallel with the input capacitor.
- If a Tantalum input capacitor is placed in parallel with the input capacitor, it must be recommended for switching regulator applications and the operating voltage must be derated by 50%.
- In “Hot-Plug” applications, a Tantalum or Electrolytic bypass capacitor must be used to limit the over-voltage spike seen on the input supply with power is suddenly applied.

RC Snubber

- Place the RC snubber on the same side of the board and as close to the SW pin as possible.

Inductor

- Keep the inductor connection to the switch node (SW) short.
- Do not route any digital lines underneath or close to the inductor.
- Keep the switch node (SW) away from the feedback (FB) pin.
- The SW pin should be connected directly to the drain of the low-side MOSFET to accurate sense the voltage across the low-side MOSFET.
- To minimize noise, place a ground plane underneath the inductor.

Output Capacitor

- Use a wide trace to connect the output capacitor ground terminal to the input capacitor ground terminal.
- Phase margin will change as the output capacitor value and ESR changes. Contact the factory if the output capacitor is different from what is shown in the BOM.
- The feedback trace should be separate from the power trace and connected as close as possible to the output capacitor. Sensing a long high-current load trace can degrade the DC load regulation.

MOSFETs

- Low-side MOSFET gate drive trace (DL pin to MOSFET gate pin) must be short and routed over a ground plane. The ground plane should be the connection between the MOSFET source and PGND.
- Chose a low-side MOSFET with a high C_{GS}/C_{GD} ratio and a low internal gate resistance to minimize the effect of dv/dt inducted turn-on.
- Do not put a resistor between the Low-side MOSFET gate drive output and the gate.
- Use a 4.5V V_{GS} rated MOSFET. Its higher gate threshold voltage is more immune to glitches than a 2.5V or 3.3V rated MOSFET. MOSFETs that are rated for operation at less than 4.5V V_{GS} should not be used.

Evaluation Board Schematic

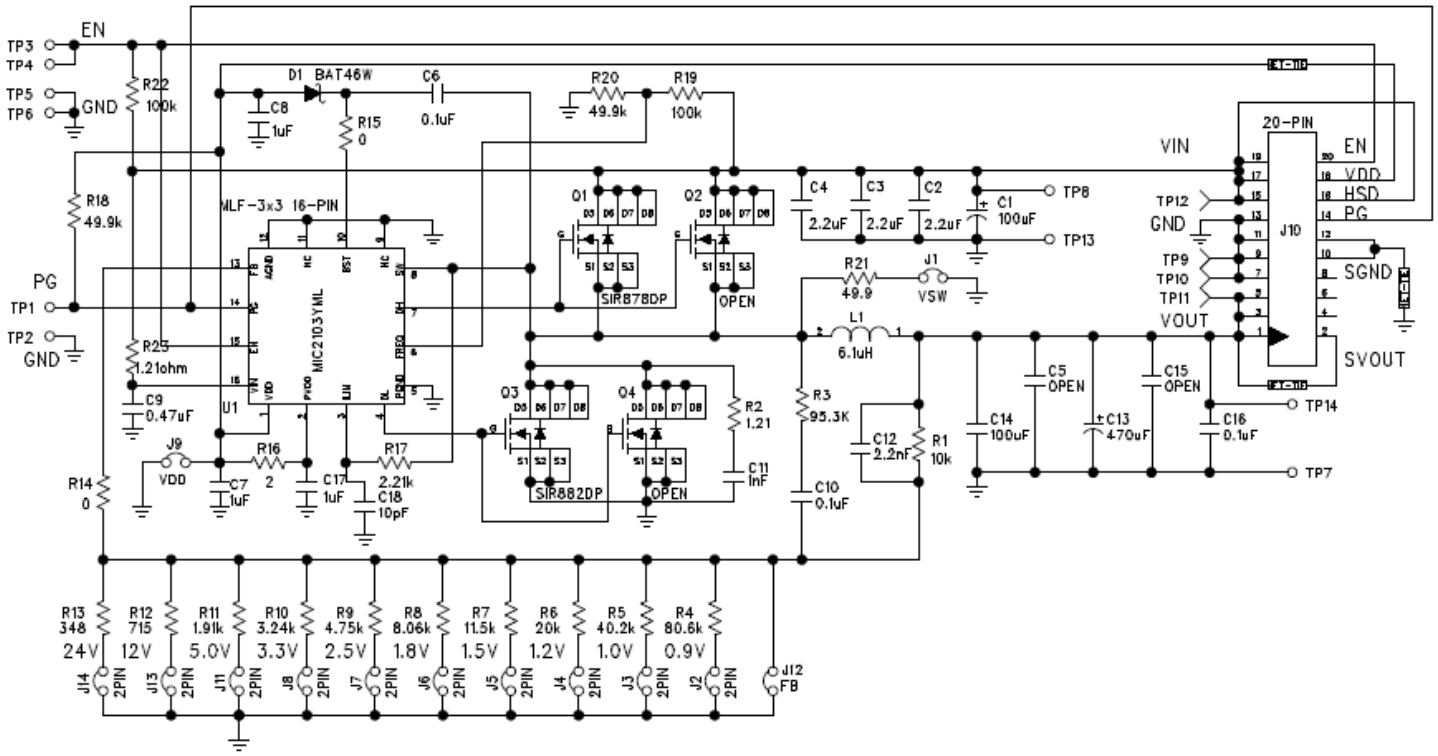


Figure 9. Schematic of MIC2103/04 Evaluation Board
(J1, J9, J12, R14, and R21 are for testing purposes)

Bill of Materials

Item	Part Number	Manufacturer	Description	Qty
C1	EEU-FC2A101	Panasonic[1]	100µF Aluminum Capacitor, 100V	1
C2, C3, C4	GRM32ER72A225K	Murata[2]	2.2µF/100V Ceramic Capacitor, X7R, Size 1210	3
	C3225X7R2A225K	TDK[3]		
	12101C225KAT2A	AVX[4]		
C14	GRM32ER60J107ME20L	Murata	100µF/6.3V Ceramic Capacitor, X5R, Size 1210	1
	12106D107MAT2A	AVX		
	C3225X5ROJ107M	TDK		
C6, C16	GRM188R71H104KA93D	Murata	0.1µF/50V Ceramic Capacitor, X7R, Size 0603	2
	06035C104KAT2A	AVX		
	C1608X7R1H104K	TDK		
C7, C8, C17	GRM188R70J105KA01D	Murata	1µF/6.3V Ceramic Capacitor, X7R, Size 0603	3
	06036C105KAT2A	AVX		
	C1608X5R0J105K	TDK		
C9	GRM21BR72A474KA73	Murata	0.47µF/100V Ceramic Capacitor, X7R, Size 0805	1
	08051C474KAT2A	AVX		
C10	GRM188R72A104KA35D	Murata	0.1µF/100V Ceramic Capacitor, X7R, Size 0603	1
	C1608X7S2A104K	TDK	0.1µF/100V,X7S,0603	
C11	GRM188R72A102KA01D	Murata	1nF/100V Cermiac Capacitor, X7R, Size 0603	1
	06031C102KAT2A	AVX		
	C1608X7R2A102K	TDK		
C12	GRM188R72A222KA01D	Murata	2.2nF/100V Cermiac Capacitor, X7R, Size 0603	1
	06031C222KAT2A	AVX		
	C1608X7R2A222K	TDK		
C13	6SEPC470MX	Sanyo[5]	470µF/6.3V, 7m-ohms, OSCON	1
	6SEPC470M	Sanyo	470µF/6.3V, 7m-ohms, OSCON	
C15 (OPEN)	6TPB470M	Sanyo	470µF/6.3V, POSCAP	
C5 (OPEN)	GRM32ER60J107ME20L	Murata	100µF/6.3V Ceramic Capacitor, X7R, Size 1210	
C18	GCM1885C2A100JA16D	Murata	10pF, 100V, 0603, NPO	1
	06031A100JAT2A	AVX		
D1	BAT46W-TP	MCC[6]	100V Small Signal Schottky Diode, SOD123	1
L1	CDEP147NP-6R1MC-95	Sumida[7]	6.1µH Inductor, 14.8A RMS Current	1

Notes:

1. Panasonic: www.panasonic.com.
2. Murata: www.murata.com.
3. TDK: www.tdk.com.
4. AVX: www.avx.com
5. Sanyo: www.sanyo.com.
6. MCC.: www.mccsemi.com.
7. Sumida: www.sumida.com.

Bill of Materials (Continued)

Item	Part Number	Manufacturer	Description	Qty
Q1	SIR878DP	Vishay[8]	MOSFET, N-CH, Power SO-8	1
Q3	SIR882DP	Vishay	MOSFET, N-CH, Power SO-8	1
Q2, Q4 (OPEN)				
R1	CRCW060310K0FKEA	Vishay Dale	10kΩ Resistor, Size 0603, 1%	1
R2, R23	CRCW08051R21FKEA	Vishay Dale	1.21Ω Resistor, Size 0805, 5%	2
R3	CRCW060395K30FKEA	Vishay Dale	95.3kΩ Resistor, Size 0603, 1%	1
R4	CRCW060380K6FKEA	Vishay Dale	80.6kΩ Resistor, Size 0603, 1%	1
R5	CRCW060340K2FKEA	Vishay Dale	40.2kΩ Resistor, Size 0603, 1%	1
R6	CRCW060320K0FKEA	Vishay Dale	20kΩ Resistor, Size 0603, 1%	1
R7	CRCW060311K5FKEA	Vishay Dale	11.5kΩ Resistor, Size 0603, 1%	1
R8	CRCW06038K06FKEA	Vishay Dale	8.06kΩ Resistor, Size 0603, 1%	1
R9	CRCW06034K75FKEA	Vishay Dale	4.75kΩ Resistor, Size 0603, 1%	1
R10	CRCW06033K24FKEA	Vishay Dale	3.24kΩ Resistor, Size 0603, 1%	1
R11	CRCW06031K91FKEA	Vishay Dale	1.91kΩ Resistor, Size 0603, 1%	1
R12 (OPEN)	CRCW0603715R0FKEA	Vishay Dale	715Ω Resistor, Size 0603, 1%	
R13 (OPEN)	CRCW0603348R0FKEA	Vishay Dale	348Ω Resistor, Size 0603, 1%	
R14, R15	CRCW06030000FKEA	Vishay Dale	0Ω Resistor, Size 0603, 5%	2
R16	CRCW08052R0FKEA	Vishay Dale	2Ω Resistor, Size 0805, 5%	1
R17	CRCW06032K21FKEA	Vishay Dale	2.21kΩ Resistor, Size 0603, 1%	1
R18, R20	CRCW060349K9FKEA	Vishay Dale	49.9kΩ Resistor, Size 0603, 1%	2
R19, R22	CRCW0603100K0FKEA	Vishay Dale	100kΩ Resistor, Size 0603, 1%	2
R21	CRCW060349R9FKEA	Vishay Dale	49.9Ω Resistor, Size 0603, 1%	1
U1	**MIC2103YML** **MIC2104YML**	**Micrel. Inc.[9]**	**75V Synchronous Buck DC-DC Controller**	**1**

Notes:

8. Vishay: www.vishay.com.

9. Micrel, Inc.: www.micrel.com.

PCB Layout

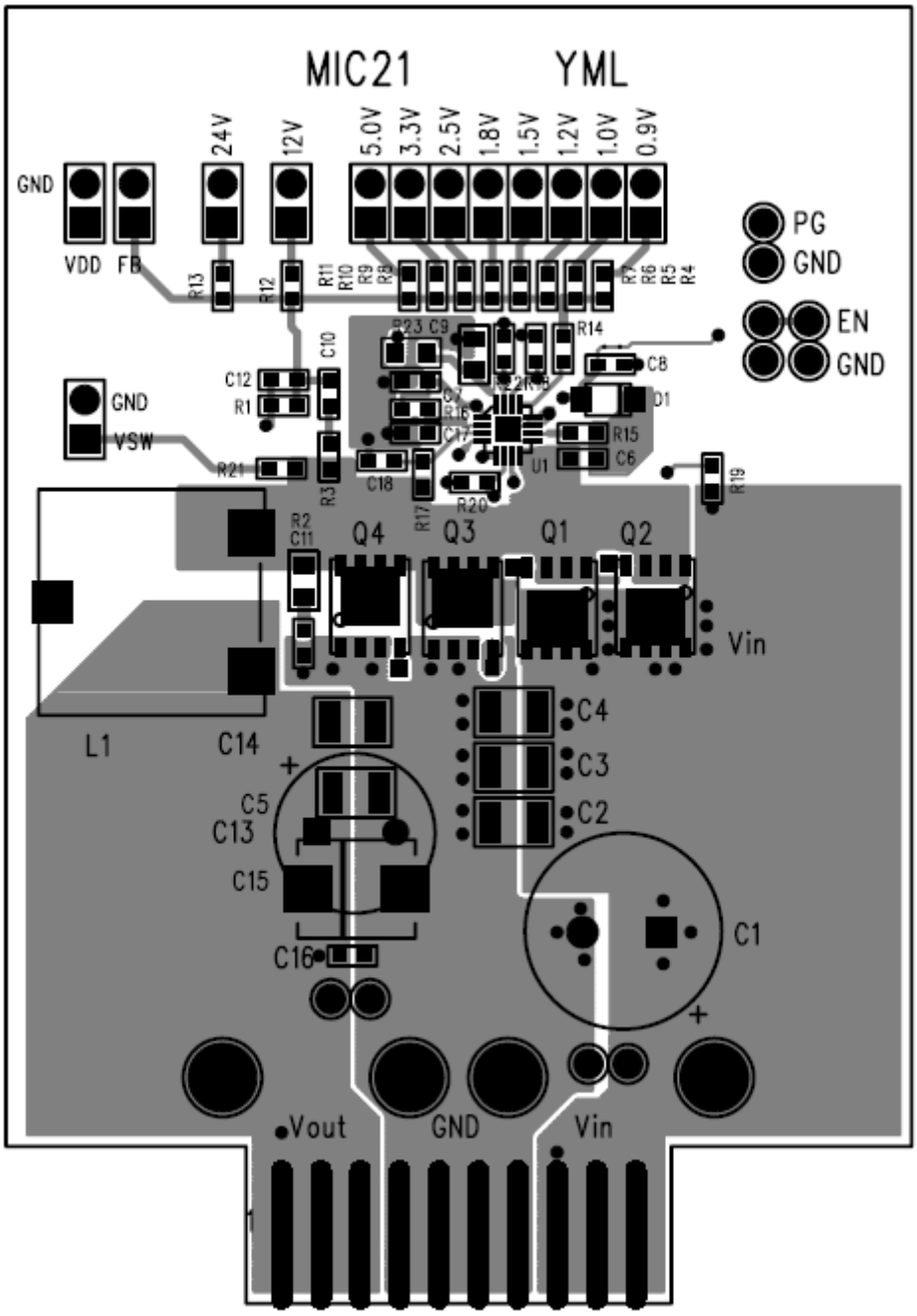


Figure 10. MIC2103/04 Evaluation Board Top Layer

PCB Layout (Continued)

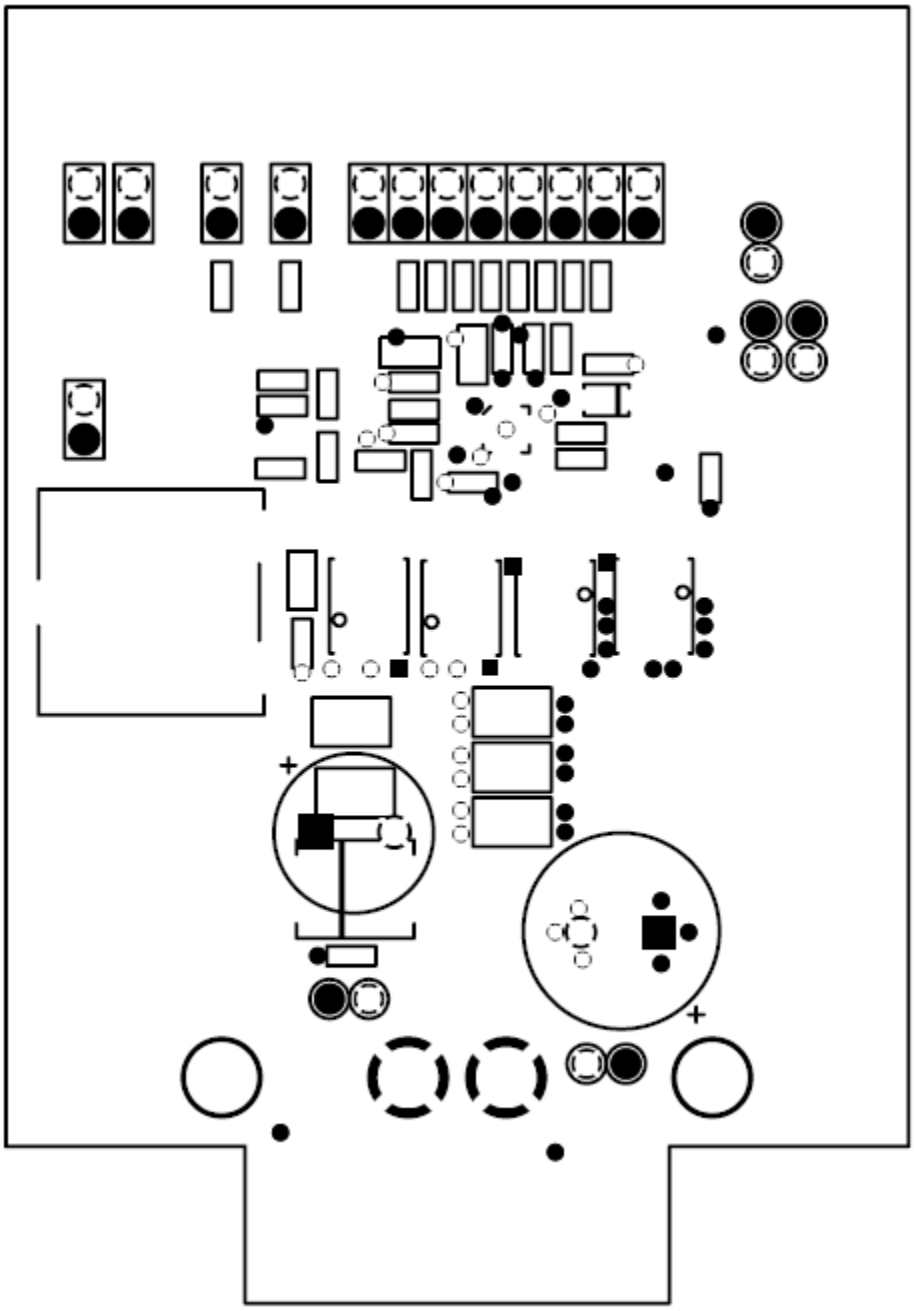


Figure 11. MIC2103/04 Evaluation Board Mid-Layer 1 (Ground Plane)

PCB Layout (Continued)

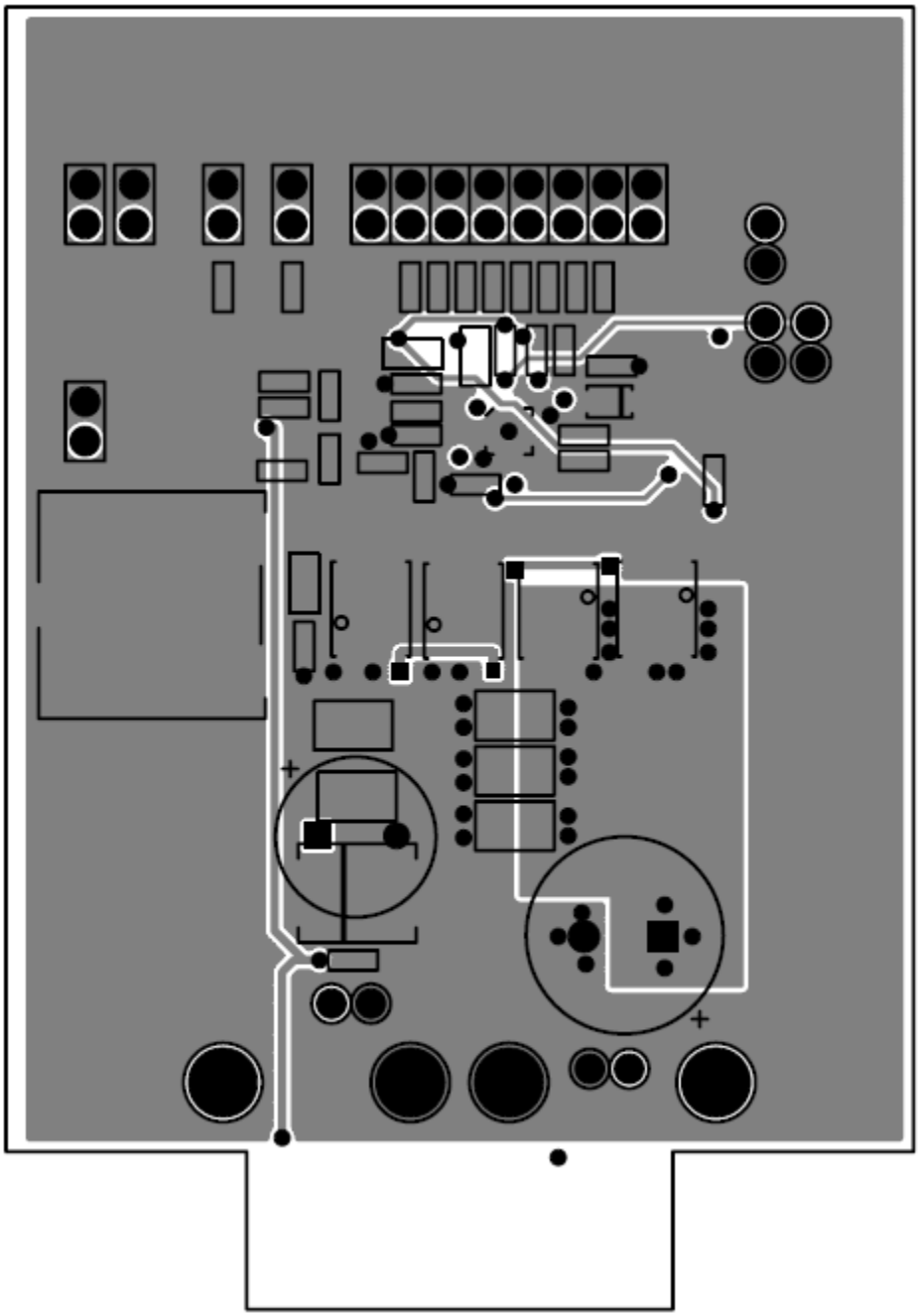


Figure 12. MIC2103/04 Evaluation Board Mid-Layer 2

PCB Layout (Continued)

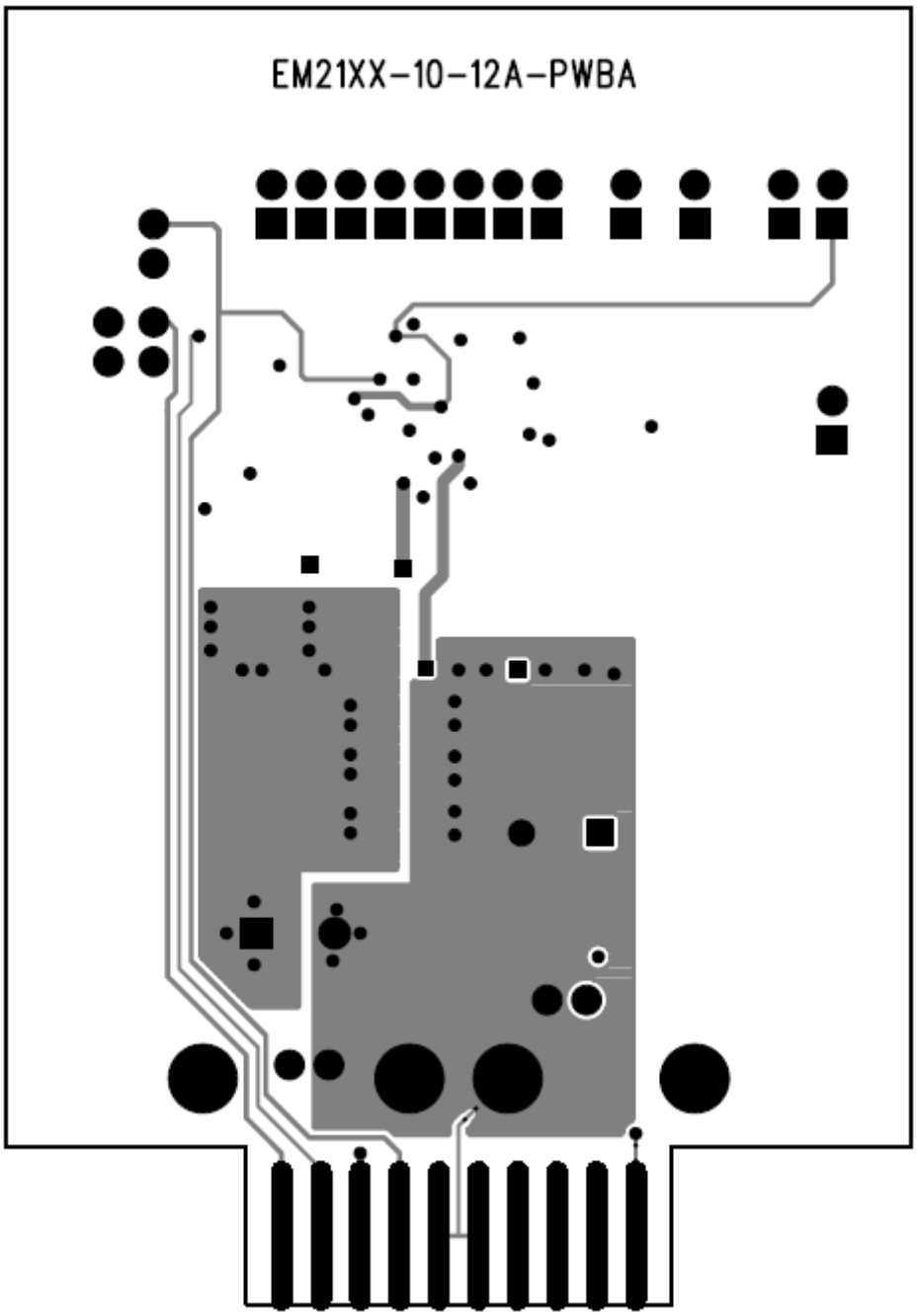
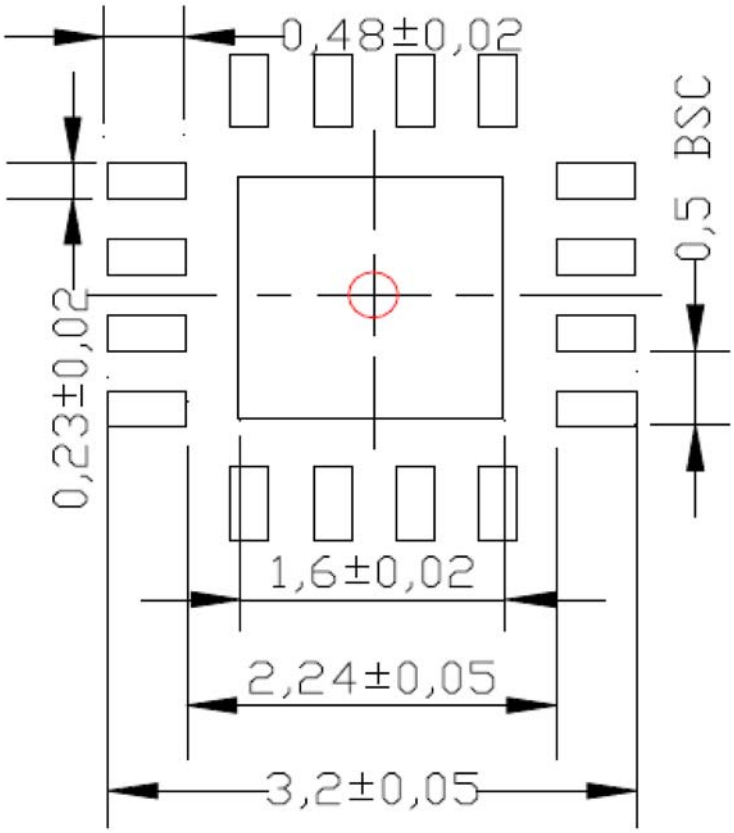


Figure 13. MIC2103/04 Evaluation Board Bottom Layer

Recommended Land Pattern

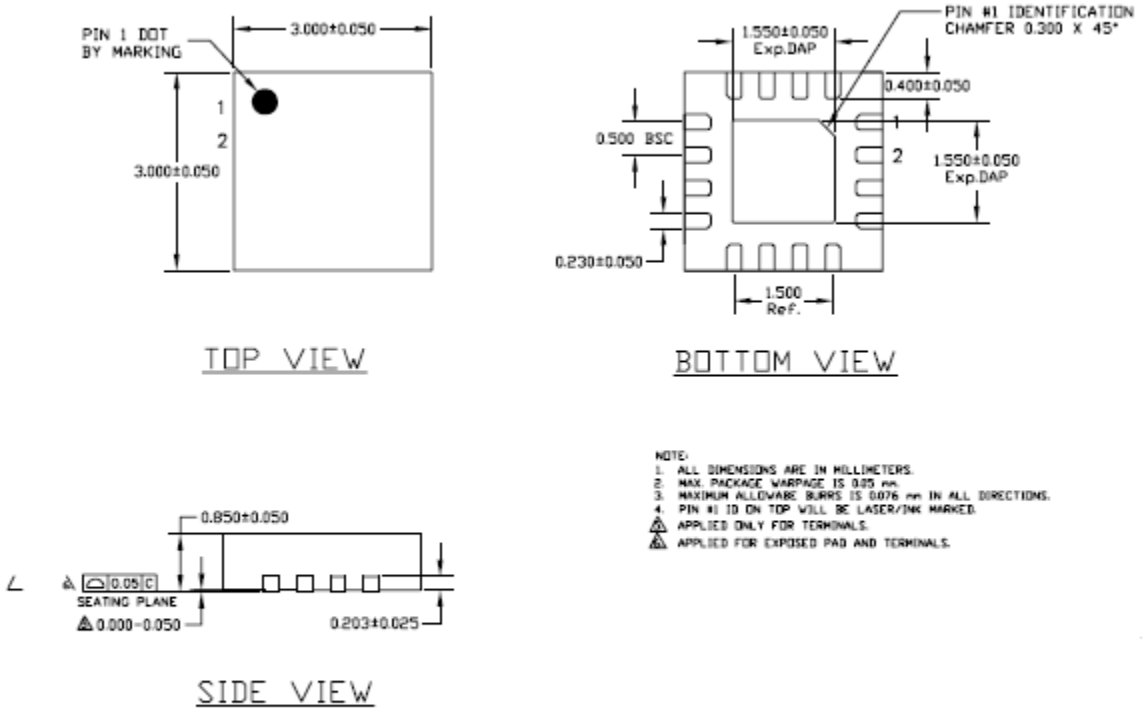


Red circle indicates Thermal Via. Size should be .300mm – .350mm in diameter and it should be connected to GND plane for maximum thermal performance.

ALL UNITS ARE IN mm, TOLERANCE ±0.05, IF NOT NOTED

LP # MLF33D-16LD-LP-1

Package Information



16-Pin 3mm × 3mm MLF (ML)

MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA
TEL +1 (408) 944-0800 FAX +1 (408) 474-1000 WEB http://www.micrel.com

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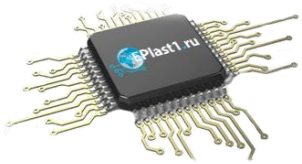
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

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