RL78/G14

RENESAS MCU

R01DS0053EJ0331
Rev. 3.31
Feb 14, 2020

True low-power platform (66 µA/MHz, and 0.60 µA for operation with only RTC and LVD) for the general-purpose applications, with 1.6-V to 5.5-V operation, 16- to 512-Kbyte code flash memory, and 44 DMIPS at 32 MHz

# 1. OUTLINE

## 1.1 Features

**Ultra-Low Power Consumption Technology**
- $V_{DD}$ = single power supply voltage of 1.6 to 5.5 V which can operate a 1.8 V device at a low voltage
- HALT mode
- STOP mode
- SNOOZE mode

**RL78 CPU Core**
- CISC architecture with 3-stage pipeline
- Minimum instruction execution time: Can be changed from high speed (0.03125 µs: @ 32 MHz operation with high-speed on-chip oscillator) to ultra-low speed (30.5 µs: @ 32.768 kHz operation with subsystem clock)
- Multiply/divide/multiply & accumulate instructions are supported.
- Address space: 1 MB
- General-purpose registers: (8-bit register × 8) × 4 banks
- On-chip RAM: 2.5 to 48 KB

**Code Flash Memory**
- Code flash memory: 16 to 512 KB
- Block size: 1 KB
- Prohibition of block erase and rewriting (security function)
- On-chip debug function
- Self-programming (with boot swap function/flash shield window function)

**Data Flash Memory**
- Data flash memory: 4 KB and 8 KB
- Back ground operation (BGO): Instructions can be executed from the program memory while rewriting the data flash memory.
- Number of rewrites: 1,000,000 times (TYP.)
- Voltage of rewrites: $V_{DD}$ = 1.8 to 5.5 V

**High-speed On-chip Oscillator**
- Select from 64 MHz, 48 MHz, 32 MHz, 24 MHz, 16 MHz, 12 MHz, 8 MHz, 6 MHz, 4 MHz, 3 MHz, 2 MHz, and 1 MHz
- High accuracy: ±1.0% ($V_{DD}$ = 1.8 to 5.5 V, $T_A$ = -20 to +85°C)

**Operating Ambient Temperature**
- $T_A$ = -40 to +85°C (A: Consumer applications, D: Industrial applications)
- $T_A$ = -40 to +105°C (G: Industrial applications)

**Power Management and Reset Function**
- On-chip power-on-reset (POR) circuit
- On-chip voltage detector (LVD) (Select interrupt and reset from 14 levels)

**Data Transfer Controller (DTC)**
- Transfer modes: Normal transfer mode, repeat transfer mode, block transfer mode
- Activation sources: Activated by interrupt sources.
- Chain transfer function

**Event Link Controller (ELC)**
- Event signals of 19 to 26 types can be linked to the specified peripheral function.

**Serial Interfaces**
- CSI: 3 to 8 channels
- UART/UART (LIN-bus supported): 3 or 4 channels
- $I^2C$/simplified $I^2C$: 3 to 8 channels

**Timer**
- 16-bit timer: 8 to 12 channels (Timer Array Unit (TAU): 4 to 8 channels, Timer RJ: 1 channel, Timer RD: 2 channels, Timer RG: 1 channel)
- 12-bit interval timer: 1 channel
- Real-time clock: 1 channel (calendar for 99 years, alarm function, and clock correction function)
- Watchdog timer: 1 channel (operable with the dedicated low-speed on-chip oscillator)

**A/D Converter**
- 8/10-bit resolution A/D converter ($V_{DD}$ = 1.6 to 5.5 V)
- Analog input: 8 to 20 channels
- Internal reference voltage (1.45 V) and temperature sensor

**D/A Converter**
- 8-bit resolution D/A converter ($V_{DD}$ = 1.6 to 5.5 V)
- Analog output: None or up to two channels
- Output voltage: 0 V to $V_{DD}$
- Real-time output function

**Comparator**
- None or up to two channels
- Operating modes: Comparator high-speed mode, comparator low-speed mode, window mode
- The external reference voltage or internal reference voltage can be selected as the reference voltage.

**I/O Port**
- I/O port: 26 to 92 (N-ch open drain I/O [withstand voltage of 6 V]: 2 to 4, N-ch open drain I/O [$V_{DD}$ withstand voltage/$EV_{DD}$ withstand voltage]: 10 to 28)
- Can be set to N-ch open drain, TTL input buffer, and on-chip pull-up resistor
- Different potential interface: Can connect to a 1.8/2.5/3 V device
- On-chip key interrupt function
- On-chip clock output/buzzer output controller

**Others**
- On-chip BCD (binary-coded decimal) correction circuit

**Remark** The functions mounted depend on the product. See **1.6 Outline of Functions**.

○ ROM, RAM capacities

| Flash ROM | Data flash | RAM | RL78/G14 | | | |
|---|---|---|---|---|---|---|
| | | | 30 pins | 32 pins | 36 pins | 40 pins |
| 192 KB | 8 KB | 20 KB | — | — | — | R5F104EH |
| 128 KB | 8 KB | 16 KB | R5F104AG | R5F104BG | R5F104CG | R5F104EG |
| 96 KB | 8 KB | 12 KB | R5F104AF | R5F104BF | R5F104CF | R5F104EF |
| 64 KB | 4 KB | 5.5 KB Note | R5F104AE | R5F104BE | R5F104CE | R5F104EE |
| 48 KB | 4 KB | 5.5 KB Note | R5F104AD | R5F104BD | R5F104CD | R5F104ED |
| 32 KB | 4 KB | 4 KB | R5F104AC | R5F104BC | R5F104CC | R5F104EC |
| 16 KB | 4 KB | 2.5 KB | R5F104AA | R5F104BA | R5F104CA | R5F104EA |

| Flash ROM | Data flash | RAM | RL78/G14 | | | |
|---|---|---|---|---|---|---|
| | | | 44 pins | 48 pins | 52 pins | 64 pins |
| 512 KB | 8 KB | 48 KB Note | — | R5F104GL | — | R5F104LL |
| 384 KB | 8 KB | 32 KB | — | R5F104GK | — | R5F104LK |
| 256 KB | 8 KB | 24 KB Note | R5F104FJ | R5F104GJ | R5F104JJ | R5F104LJ |
| 192 KB | 8 KB | 20 KB | R5F104FH | R5F104GH | R5F104JH | R5F104LH |
| 128 KB | 8 KB | 16 KB | R5F104FG | R5F104GG | R5F104JG | R5F104LG |
| 96 KB | 8 KB | 12 KB | R5F104FF | R5F104GF | R5F104JF | R5F104LF |
| 64 KB | 4 KB | 5.5 KB Note | R5F104FE | R5F104GE | R5F104JE | R5F104LE |
| 48 KB | 4 KB | 5.5 KB Note | R5F104FD | R5F104GD | R5F104JD | R5F104LD |
| 32 KB | 4 KB | 4 KB | R5F104FC | R5F104GC | R5F104JC | R5F104LC |
| 16 KB | 4 KB | 2.5 KB | R5F104FA | R5F104GA | — | — |

| Flash ROM | Data flash | RAM | RL78/G14 | |
|---|---|---|---|---|
| | | | 80 pins | 100 pins |
| 512 KB | 8 KB | 48 KB Note | R5F104ML | R5F104PL |
| 384 KB | 8 KB | 32 KB | R5F104MK | R5F104PK |
| 256 KB | 8 KB | 24 KB Note | R5F104MJ | R5F104PJ |
| 192 KB | 8 KB | 20 KB | R5F104MH | R5F104PH |
| 128 KB | 8 KB | 16 KB | R5F104MG | R5F104PG |
| 96 KB | 8 KB | 12 KB | R5F104MF | R5F104PF |

**Note** The flash library uses RAM in self-programming and rewriting of the data flash memory.
The target products and start address of the RAM areas used by the flash library are shown below.
R5F104xD (x = A to C, E to G, J, L): Start address FE900H
R5F104xE (x = A to C, E to G, J, L): Start address FE900H
R5F104xJ (x = F, G, J, L, M, P): Start address F9F00H
R5F104xL (x = G, L, M, P): Start address F3F00H
For the RAM areas used by the flash library, see **Self RAM list of Flash Self-Programming Library for RL78 Family (R20UT2944)**.

## 1.2 Ordering Information

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**Figure 1 - 1 Part Number, Memory Size, and Package of RL78/G14**

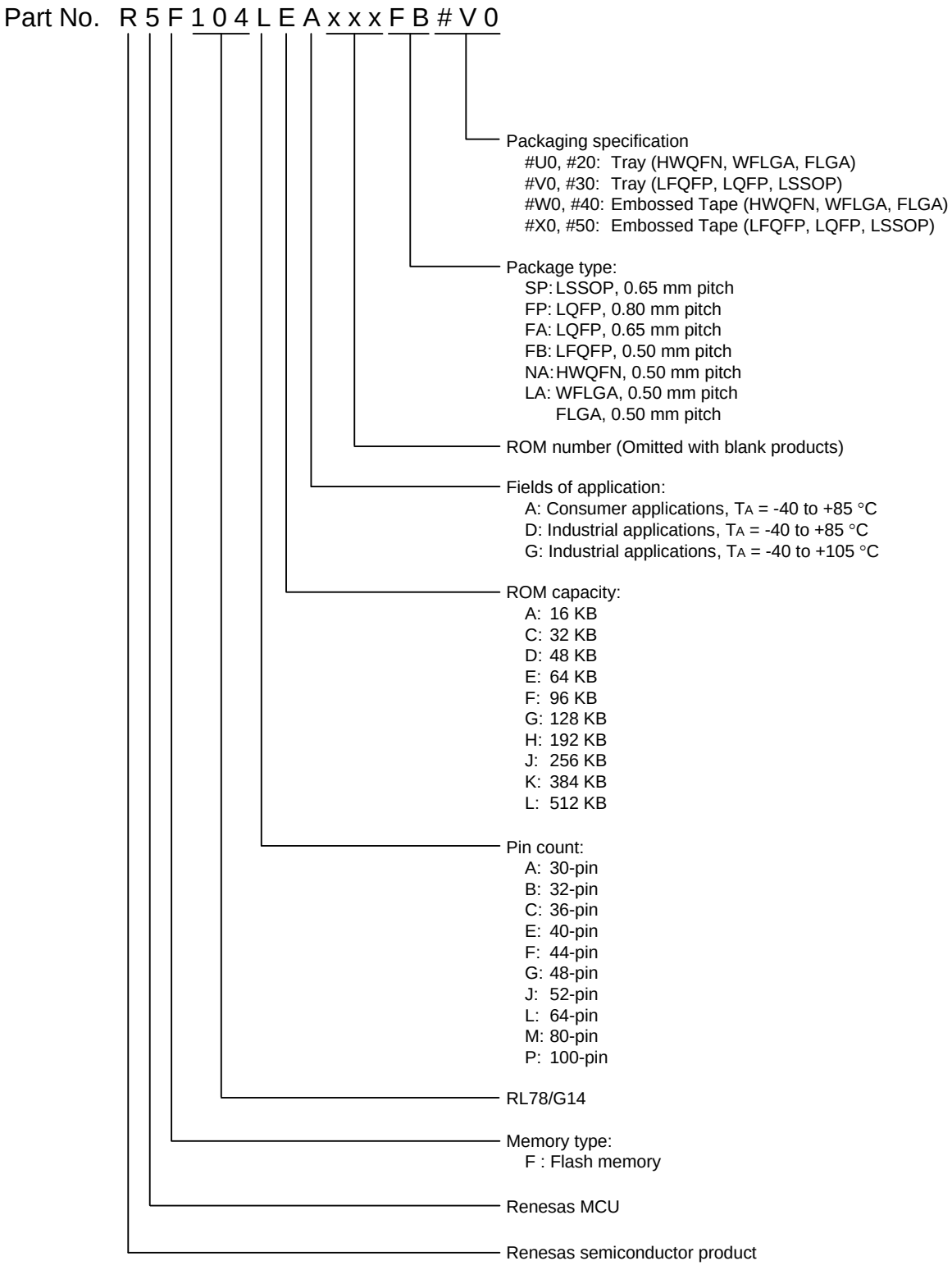

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**Table 1 - 1 List of Ordering Part Numbers (1/12)**

| Pin count | Package | Fields of Application Note | Ordering Part Number | RENESAS Code |
|---|---|---|---|---|
| 30 pins | 30-pin plastic LSSOP (7.62 mm (300), 0.65 mm pitch) | A | R5F104AAASP#V0, R5F104ACASP#V0, R5F104ADASP#V0, R5F104AEASP#V0, R5F104AFASP#V0, R5F104AGASP#V0<br>R5F104AAASP#X0, R5F104ACASP#X0, R5F104ADASP#X0, R5F104AEASP#X0, R5F104AFASP#X0, R5F104AGASP#X0<br>R5F104AAASP#30, R5F104ACASP#30, R5F104ADASP#30, R5F104AEASP#30, R5F104AFASP#30, R5F104AGASP#30<br>R5F104AAASP#50, R5F104ACASP#50, R5F104ADASP#50, R5F104AEASP#50, R5F104AFASP#50, R5F104AGASP#50 | PLSP0030JB-B |
| | | D | R5F104AADSP#V0, R5F104ACDSP#V0, R5F104ADDSP#V0, R5F104AEDSP#V0, R5F104AFDSP#V0, R5F104AGDSP#V0<br>R5F104AADSP#X0, R5F104ACDSP#X0, R5F104ADDSP#X0, R5F104AEDSP#X0, R5F104AFDSP#X0, R5F104AGDSP#X0<br>R5F104AADSP#30, R5F104ACDSP#30, R5F104ADDSP#30, R5F104AEDSP#30, R5F104AFDSP#30, R5F104AGDSP#30<br>R5F104AADSP#50, R5F104ACDSP#50, R5F104ADDSP#50, R5F104AEDSP#50, R5F104AFDSP#50, R5F104AGDSP#50 | |
| | | G | R5F104AAGSP#V0, R5F104ACGSP#V0, R5F104ADGSP#V0, R5F104AEGSP#V0, R5F104AFGSP#V0, R5F104AGGSP#V0<br>R5F104AAGSP#X0, R5F104ACGSP#X0, R5F104ADGSP#X0, R5F104AEGSP#X0, R5F104AFGSP#X0, R5F104AGGSP#X0<br>R5F104AAGSP#30, R5F104ACGSP#30, R5F104ADGSP#30, R5F104AEGSP#30, R5F104AFGSP#30, R5F104AGGSP#30<br>R5F104AAGSP#50, R5F104ACGSP#50, R5F104ADGSP#50, R5F104AEGSP#50, R5F104AFGSP#50, R5F104AGGSP#50 | |

**Note** For the fields of application, refer to **Figure 1 - 1 Part Number, Memory Size, and Package of RL78/G14**.

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**Table 1 - 1 List of Ordering Part Numbers (2/12)**

| Pin count | Package | Fields of Application Note | Ordering Part Number | RENESAS Code |
|---|---|---|---|---|
| 32 pins | 32-pin plastic HWQFN (5 × 5 mm, 0.5 mm pitch) | A | R5F104BAANA#U0, R5F104BCANA#U0, R5F104BDANA#U0, R5F104BEANA#U0, R5F104BFANA#U0, R5F104BGANA#U0<br>R5F104BAANA#W0, R5F104BCANA#W0, R5F104BDANA#W0, R5F104BEANA#W0, R5F104BFANA#W0, R5F104BGANA#W0 | PWQN0032KB-A |
| | | | R5F104BAANA#20, R5F104BCANA#20, R5F104BDANA#20, R5F104BEANA#20, R5F104BFANA#20, R5F104BGANA#20<br>R5F104BAANA#40, R5F104BCANA#40, R5F104BDANA#40, R5F104BEANA#40, R5F104BFANA#40, R5F104BGANA#40 | PWQN0032KE-A |
| | | D | R5F104BADNA#U0, R5F104BCDNA#U0, R5F104BDDNA#U0, R5F104BEDNA#U0, R5F104BFDNA#U0, R5F104BGDNA#U0<br>R5F104BADNA#W0, R5F104BCDNA#W0, R5F104BDDNA#W0, R5F104BEDNA#W0, R5F104BFDNA#W0, R5F104BGDNA#W0 | PWQN0032KB-A |
| | | G | R5F104BAGNA#U0, R5F104BCGNA#U0, R5F104BDGNA#U0, R5F104BEGNA#U0, R5F104BFGNA#U0, R5F104BGGNA#U0<br>R5F104BAGNA#W0, R5F104BCGNA#W0, R5F104BDGNA#W0, R5F104BEGNA#W0, R5F104BFGNA#W0, R5F104BGGNA#W0 | |
| | | | R5F104BAGNA#20, R5F104BCGNA#20, R5F104BDGNA#20, R5F104BEGNA#20, R5F104BFGNA#20, R5F104BGGNA#20<br>R5F104BAGNA#40, R5F104BCGNA#40, R5F104BDGNA#40, R5F104BEGNA#40, R5F104BFGNA#40, R5F104BGGNA#40 | PWQN0032KE-A |
| | 32-pin plastic LQFP (7 × 7 mm, 0.8 mm pitch) | A | R5F104BAAFP#V0, R5F104BCAFP#V0, R5F104BDAFP#V0, R5F104BEAFP#V0, R5F104BFAFP#V0, R5F104BGAFP#V0<br>R5F104BAAFP#X0, R5F104BCAFP#X0, R5F104BDAFP#X0, R5F104BEAFP#X0, R5F104BFAFP#X0, R5F104BGAFP#X0<br>R5F104BAAFP#30, R5F104BCAFP#30, R5F104BDAFP#30, R5F104BEAFP#30, R5F104BFAFP#30, R5F104BGAFP#30<br>R5F104BAAFP#50, R5F104BCAFP#50, R5F104BDAFP#50, R5F104BEAFP#50, R5F104BFAFP#50, R5F104BGAFP#50 | PLQP0032GB-A |
| | | D | R5F104BADFP#V0, R5F104BCDFP#V0, R5F104BDDFP#V0, R5F104BEDFP#V0, R5F104BFDFP#V0, R5F104BGDFP#V0<br>R5F104BADFP#X0, R5F104BCDFP#X0, R5F104BDDFP#X0, R5F104BEDFP#X0, R5F104BFDFP#X0, R5F104BGDFP#X0<br>R5F104BADFP#30, R5F104BCDFP#30, R5F104BDDFP#30, R5F104BEDFP#30, R5F104BFDFP#30, R5F104BGDFP#30<br>R5F104BADFP#50, R5F104BCDFP#50, R5F104BDDFP#50, R5F104BEDFP#50, R5F104BFDFP#50, R5F104BGDFP#50 | |
| | | G | R5F104BAGFP#V0, R5F104BCGFP#V0, R5F104BDGFP#V0, R5F104BEGFP#V0, R5F104BFGFP#V0, R5F104BGGFP#V0<br>R5F104BAGFP#X0, R5F104BCGFP#X0, R5F104BDGFP#X0, R5F104BEGFP#X0, R5F104BFGFP#X0, R5F104BGGFP#X0<br>R5F104BAGFP#30, R5F104BCGFP#30, R5F104BDGFP#30, R5F104BEGFP#30, R5F104BFGFP#30, R5F104BGGFP#30<br>R5F104BAGFP#50, R5F104BCGFP#50, R5F104BDGFP#50, R5F104BEGFP#50, R5F104BFGFP#50, R5F104BGGFP#50 | |

**Note** For the fields of application, refer to **Figure 1 - 1 Part Number, Memory Size, and Package of RL78/G14**.

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**Table 1 - 1 List of Ordering Part Numbers (3/12)**

| Pin count | Package | Fields of Application Note | Ordering Part Number | RENESAS Code |
|---|---|---|---|---|
| 36 pins | 36-pin plastic WFLGA (4 × 4 mm, 0.5 mm pitch) | A | R5F104CAALA#U0, R5F104CCALA#U0, R5F104CDALA#U0, R5F104CEALA#U0, R5F104CFALA#U0, R5F104CGALA#U0<br>R5F104CAALA#W0, R5F104CCALA#W0, R5F104CDALA#W0, R5F104CEALA#W0, R5F104CFALA#W0, R5F104CGALA#W0 | PWLG0036KA-A |
| | | G | R5F104CAGLA#U0, R5F104CCGLA#U0, R5F104CDGLA#U0, R5F104CEGLA#U0, R5F104CFGLA#U0, R5F104CGGLA#U0<br>R5F104CAGLA#W0, R5F104CCGLA#W0, R5F104CDGLA#W0, R5F104CEGLA#W0, R5F104CFGLA#W0, R5F104CGGLA#W0 | |
| 40 pins | 40-pin plastic HWQFN (6 × 6 mm, 0.5 mm pitch) | A | R5F104EAANA#U0, R5F104ECANA#U0, R5F104EDANA#U0, R5F104EEANA#U0, R5F104EFANA#U0, R5F104EGANA#U0, R5F104EHANA#U0<br>R5F104EAANA#W0, R5F104ECANA#W0, R5F104EDANA#W0, R5F104EEANA#W0, R5F104EFANA#W0, R5F104EGANA#W0, R5F104EHANA#W0 | PWQN0040KC-A |
| | | D | R5F104EADNA#U0, R5F104ECDNA#U0, R5F104EDDNA#U0, R5F104EEDNA#U0, R5F104EFDNA#U0, R5F104EGDNA#U0, R5F104EHDNA#U0<br>R5F104EADNA#W0, R5F104ECDNA#W0, R5F104EDDNA#W0, R5F104EEDNA#W0, R5F104EFDNA#W0, R5F104EGDNA#W0, R5F104EHDNA#W0 | |
| | | G | R5F104EAGNA#U0, R5F104ECGNA#U0, R5F104EDGNA#U0, R5F104EEGNA#U0, R5F104EFGNA#U0, R5F104EGGNA#U0, R5F104EHGNA#U0<br>R5F104EAGNA#W0, R5F104ECGNA#W0, R5F104EDGNA#W0, R5F104EEGNA#W0, R5F104EFGNA#W0, R5F104EGGNA#W0, R5F104EHGNA#W0 | |

**Note** For the fields of application, refer to **Figure 1 - 1 Part Number, Memory Size, and Package of RL78/G14**.

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**Table 1 - 1 List of Ordering Part Numbers (4/12)**

| Pin count | Package | Fields of Application Note | Ordering Part Number | RENESAS Code |
|---|---|---|---|---|
| 44 pins | 44-pin plastic LQFP (10 × 10 mm, 0.8 mm pitch) | A | R5F104FAAFP#V0, R5F104FCAFP#V0, R5F104FDAFP#V0, R5F104FEAFP#V0, R5F104FFAFP#V0, R5F104FGAFP#V0, R5F104FHAFP#V0, R5F104FJAFP#V0<br>R5F104FAAFP#X0, R5F104FCAFP#X0, R5F104FDAFP#X0, R5F104FEAFP#X0, R5F104FFAFP#X0, R5F104FGAFP#X0, R5F104FHAFP#X0, R5F104FJAFP#X0 | PLQP0044GC-A |
| | | | R5F104FAAFP#30, R5F104FCAFP#30, R5F104FDAFP#30, R5F104FEAFP#30, R5F104FFAFP#30, R5F104FGAFP#30, R5F104FHAFP#30, R5F104FJAFP#30<br>R5F104FAAFP#50, R5F104FCAFP#50, R5F104FDAFP#50, R5F104FEAFP#50, R5F104FFAFP#50, R5F104FGAFP#50, R5F104FHAFP#50, R5F104FJAFP#50 | PLQP0044GC-A/ PLQP0044GC-D |
| | | D | R5F104FADFP#V0, R5F104FCDFP#V0, R5F104FDDFP#V0, R5F104FEDFP#V0, R5F104FFDFP#V0, R5F104FGDFP#V0, R5F104FHDFP#V0, R5F104FJDFP#V0<br>R5F104FADFP#X0, R5F104FCDFP#X0, R5F104FDDFP#X0, R5F104FEDFP#X0, R5F104FFDFP#X0, R5F104FGDFP#X0, R5F104FHDFP#X0, R5F104FJDFP#X0 | PLQP0044GC-A |
| | | | R5F104FADFP#30, R5F104FCDFP#30, R5F104FDDFP#30, R5F104FEDFP#30, R5F104FFDFP#30, R5F104FGDFP#30, R5F104FHDFP#30, R5F104FJDFP#30<br>R5F104FADFP#50, R5F104FCDFP#50, R5F104FDDFP#50, R5F104FEDFP#50, R5F104FFDFP#50, R5F104FGDFP#50, R5F104FHDFP#50, R5F104FJDFP#50 | PLQP0044GC-A/ PLQP0044GC-D |
| | | G | R5F104FAGFP#V0, R5F104FCGFP#V0, R5F104FDGFP#V0, R5F104FEGFP#V0, R5F104FFGFP#V0, R5F104FGGFP#V0, R5F104FHGFP#V0, R5F104FJGFP#V0<br>R5F104FAGFP#X0, R5F104FCGFP#X0, R5F104FDGFP#X0, R5F104FEGFP#X0, R5F104FFGFP#X0, R5F104FGGFP#X0, R5F104FHGFP#X0, R5F104FJGFP#X0 | PLQP0044GC-A |
| | | | R5F104FAGFP#30, R5F104FCGFP#30, R5F104FDGFP#30, R5F104FEGFP#30, R5F104FFGFP#30, R5F104FGGFP#30, R5F104FHGFP#30, R5F104FJGFP#30<br>R5F104FAGFP#50, R5F104FCGFP#50, R5F104FDGFP#50, R5F104FEGFP#50, R5F104FFGFP#50, R5F104FGGFP#50, R5F104FHGFP#50, R5F104FJGFP#50 | PLQP0044GC-A/ PLQP0044GC-D |

**Note** For the fields of application, refer to **Figure 1 - 1 Part Number, Memory Size, and Package of RL78/G14**.

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**Table 1 - 1 List of Ordering Part Numbers (5/12)**

| Pin count | Package | Fields of Application Note | Ordering Part Number | RENESAS Code |
|---|---|---|---|---|
| 48 pins | 48-pin plastic LFQFP (7 × 7 mm, 0.5 mm pitch) | A | R5F104GAAFB#V0, R5F104GCAFB#V0, R5F104GDAFB#V0, R5F104GEAFB#V0, R5F104GFAFB#V0, R5F104GGAFB#V0, R5F104GHAFB#V0, R5F104GJAFB#V0<br>R5F104GAAFB#X0, R5F104GCAFB#X0, R5F104GDAFB#X0, R5F104GEAFB#X0, R5F104GFAFB#X0, R5F104GGAFB#X0, R5F104GHAFB#X0, R5F104GJAFB#X0 | PLQP0048KF-A |
| | | | R5F104GAAFB#30, R5F104GCAFB#30, R5F104GDAFB#30, R5F104GEAFB#30, R5F104GFAFB#30, R5F104GGAFB#30, R5F104GHAFB#30, R5F104GJAFB#30, R5F104GKAFB#30, R5F104GLAFB#30<br>R5F104GAAFB#50, R5F104GCAFB#50, R5F104GDAFB#50, R5F104GEAFB#50, R5F104GFAFB#50, R5F104GGAFB#50, R5F104GHAFB#50, R5F104GJAFB#50, R5F104GKAFB#50, R5F104GLAFB#50 | PLQP0048KB-B |
| | | D | R5F104GADFB#V0, R5F104GCDFB#V0, R5F104GDDFB#V0, R5F104GEDFB#V0, R5F104GFDFB#V0, R5F104GGDFB#V0, R5F104GHDFB#V0, R5F104GJDFB#V0<br>R5F104GADFB#X0, R5F104GCDFB#X0, R5F104GDDFB#X0, R5F104GEDFB#X0, R5F104GFDFB#X0, R5F104GGDFB#X0, R5F104GHDFB#X0, R5F104GJDFB#X0 | PLQP0048KF-A |
| | | | R5F104GADFB#30, R5F104GCDFB#30, R5F104GDDFB#30, R5F104GEDFB#30, R5F104GFDFB#30, R5F104GGDFB#30, R5F104GHDFB#30, R5F104GJDFB#30<br>R5F104GADFB#50, R5F104GCDFB#50, R5F104GDDFB#50, R5F104GEDFB#50, R5F104GFDFB#50, R5F104GGDFB#50, R5F104GHDFB#50, R5F104GJDFB#50 | PLQP0048KB-B |
| | | G | R5F104GAGFB#V0, R5F104GCGFB#V0, R5F104GDGFB#V0, R5F104GEGFB#V0, R5F104GFGFB#V0, R5F104GGGFB#V0, R5F104GHGFB#V0, R5F104GJGFB#V0<br>R5F104GAGFB#X0, R5F104GCGFB#X0, R5F104GDGFB#X0, R5F104GEGFB#X0, R5F104GFGFB#X0, R5F104GGGFB#X0, R5F104GHGFB#X0, R5F104GJGFB#X0 | PLQP0048KF-A |
| | | | R5F104GAGFB#30, R5F104GCGFB#30, R5F104GDGFB#30, R5F104GEGFB#30, R5F104GFGFB#30, R5F104GGGFB#30, R5F104GHGFB#30, R5F104GJGFB#30, R5F104GKGFB#30, R5F104GLGFB#30<br>R5F104GAGFB#50, R5F104GCGFB#50, R5F104GDGFB#50, R5F104GEGFB#50, R5F104GFGFB#50, R5F104GGGFB#50, R5F104GHGFB#50, R5F104GJGFB#50, R5F104GKGFB#50, R5F104GLGFB#50 | PLQP0048KB-B |

**Note** For the fields of application, refer to **Figure 1 - 1 Part Number, Memory Size, and Package of RL78/G14**.

**Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.**

<R>

**Table 1 - 1 List of Ordering Part Numbers (6/12)**

| Pin count | Package | Fields of Application Note | Ordering Part Number | RENESAS Code |
|---|---|---|---|---|
| 48 pins | 48-pin plastic HWQFN (7 × 7 mm, 0.5 mm pitch) | A | R5F104GAANA#U0, R5F104GCANA#U0, R5F104GDANA#U0, R5F104GEANA#U0, R5F104GFANA#U0, R5F104GGANA#U0, R5F104GHANA#U0, R5F104GJANA#U0, R5F104GKANA#U0, R5F104GLANA#U0<br>R5F104GAANA#W0, R5F104GCANA#W0, R5F104GDANA#W0, R5F104GEANA#W0, R5F104GFANA#W0, R5F104GGANA#W0, R5F104GHANA#W0, R5F104GJANA#W0, R5F104GKANA#W0, R5F104GLANA#W0 | PWQN0048KB-A |
| | | D | R5F104GADNA#U0, R5F104GCDNA#U0, R5F104GDDNA#U0, R5F104GEDNA#U0, R5F104GFDNA#U0, R5F104GGDNA#U0, R5F104GHDNA#U0, R5F104GJDNA#U0<br>R5F104GADNA#W0, R5F104GCDNA#W0, R5F104GDDNA#W0, R5F104GEDNA#W0, R5F104GFDNA#W0, R5F104GGDNA#W0, R5F104GHDNA#W0, R5F104GJDNA#W0 | |
| | | G | R5F104GAGNA#U0, R5F104GCGNA#U0, R5F104GDGNA#U0, R5F104GEGNA#U0, R5F104GFGNA#U0, R5F104GGGNA#U0, R5F104GHGNA#U0, R5F104GJGNA#U0, R5F104GKGNA#U0, R5F104GLGNA#U0<br>R5F104GAGNA#W0, R5F104GCGNA#W0, R5F104GDGNA#W0, R5F104GEGNA#W0, R5F104GFGNA#W0, R5F104GGGNA#W0, R5F104GHGNA#W0, R5F104GJGNA#W0, R5F104GKGNA#W0, R5F104GLGNA#W0 | |

**Note** For the fields of application, refer to **Figure 1 - 1 Part Number, Memory Size, and Package of RL78/G14**.

**Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.**

<R>

**Table 1 - 1 List of Ordering Part Numbers (7/12)**

| Pin count | Package | Fields of Application Note | Ordering Part Number | RENESAS Code |
|---|---|---|---|---|
| 52 pins | 52-pin plastic LQFP (10 × 10 mm, 0.65 mm pitch) | A | R5F104JCAFA#V0, R5F104JDAFA#V0, R5F104JEAFA#V0, R5F104JFAFA#V0, R5F104JGAFA#V0, R5F104JHAFA#V0, R5F104JJAFA#V0<br>R5F104JCAFA#X0, R5F104JDAFA#X0, R5F104JEAFA#X0, R5F104JFAFA#X0, R5F104JGAFA#X0, R5F104JHAFA#X0, R5F104JJAFA#X0<br>R5F104JCAFA#30, R5F104JDAFA#30, R5F104JEAFA#30, R5F104JFAFA#30, R5F104JGAFA#30, R5F104JHAFA#30, R5F104JJAFA#30<br>R5F104JCAFA#50, R5F104JDAFA#50, R5F104JEAFA#50, R5F104JFAFA#50, R5F104JGAFA#50, R5F104JHAFA#50, R5F104JJAFA#50 | PLQP0052JA-A |
| | | D | R5F104JCDFA#V0, R5F104JDDFA#V0, R5F104JEDFA#V0, R5F104JFDFA#V0, R5F104JGDFA#V0, R5F104JHDFA#V0, R5F104JJDFA#V0<br>R5F104JCDFA#X0, R5F104JDDFA#X0, R5F104JEDFA#X0, R5F104JFDFA#X0, R5F104JGDFA#X0, R5F104JHDFA#X0, R5F104JJDFA#X0<br>R5F104JCDFA#30, R5F104JDDFA#30, R5F104JEDFA#30, R5F104JFDFA#30, R5F104JGDFA#30, R5F104JHDFA#30, R5F104JJDFA#30<br>R5F104JCDFA#50, R5F104JDDFA#50, R5F104JEDFA#50, R5F104JFDFA#50, R5F104JGDFA#50, R5F104JHDFA#50, R5F104JJDFA#50 | |
| | | G | R5F104JCGFA#V0, R5F104JDGFA#V0, R5F104JEGFA#V0, R5F104JFGFA#V0, R5F104JGGFA#V0, R5F104JHGFA#V0, R5F104JJGFA#V0<br>R5F104JCGFA#X0, R5F104JDGFA#X0, R5F104JEGFA#X0, R5F104JFGFA#X0, R5F104JGGFA#X0, R5F104JHGFA#X0, R5F104JJGFA#X0<br>R5F104JCGFA#30, R5F104JDGFA#30, R5F104JEGFA#30, R5F104JFGFA#30, R5F104JGGFA#30, R5F104JHGFA#30, R5F104JJGFA#30<br>R5F104JCGFA#50, R5F104JDGFA#50, R5F104JEGFA#50, R5F104JFGFA#50, R5F104JGGFA#50, R5F104JHGFA#50, R5F104JJGFA#50 | |

**Note** For the fields of application, refer to **Figure 1 - 1 Part Number, Memory Size, and Package of RL78/G14**.

**Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.**

<R>

**Table 1 - 1 List of Ordering Part Numbers (8/12)**

| Pin count | Package | Fields of Application Note | Ordering Part Number | RENESAS Code |
|---|---|---|---|---|
| 64 pins | 64-pin plastic LQFP (12 × 12 mm, 0.65 mm pitch) | A | R5F104LCAFA#V0, R5F104LDAFA#V0, R5F104LEAFA#V0, R5F104LFAFA#V0, R5F104LGAFA#V0, R5F104LHAFA#V0, R5F104LJAFA#V0<br>R5F104LCAFA#X0, R5F104LDAFA#X0, R5F104LEAFA#X0, R5F104LFAFA#X0, R5F104LGAFA#X0, R5F104LHAFA#X0, R5F104LJAFA#X0<br>R5F104LCAFA#30, R5F104LDAFA#30, R5F104LEAFA#30, R5F104LFAFA#30, R5F104LGAFA#30, R5F104LHAFA#30, R5F104LJAFA#30, R5F104LKAFA#30, R5F104LLAFA#30<br>R5F104LCAFA#50, R5F104LDAFA#50, R5F104LEAFA#50, R5F104LFAFA#50, R5F104LGAFA#50, R5F104LHAFA#50, R5F104LJAFA#50, R5F104LKAFA#50, R5F104LLAFA#50 | PLQP0064JA-A |
| | | D | R5F104LCDFA#V0, R5F104LDDFA#V0, R5F104LEDFA#V0, R5F104LFDFA#V0, R5F104LGDFA#V0, R5F104LHDFA#V0, R5F104LJDFA#V0<br>R5F104LCDFA#X0, R5F104LDDFA#X0, R5F104LEDFA#X0, R5F104LFDFA#X0, R5F104LGDFA#X0, R5F104LHDFA#X0, R5F104LJDFA#X0<br>R5F104LCDFA#30, R5F104LDDFA#30, R5F104LEDFA#30, R5F104LFDFA#30, R5F104LGDFA#30, R5F104LHDFA#30, R5F104LJDFA#30<br>R5F104LCDFA#50, R5F104LDDFA#50, R5F104LEDFA#50, R5F104LFDFA#50, R5F104LGDFA#50, R5F104LHDFA#50, R5F104LJDFA#50 | |
| | | G | R5F104LCGFA#V0, R5F104LDGFA#V0, R5F104LEGFA#V0, R5F104LFGFA#V0, R5F104LGGFA#V0, R5F104LHGFA#V0, R5F104LJGFA#V0<br>R5F104LCGFA#X0, R5F104LDGFA#X0, R5F104LEGFA#X0, R5F104LFGFA#X0, R5F104LGGFA#X0, R5F104LHGFA#X0, R5F104LJGFA#X0<br>R5F104LCGFA#30, R5F104LDGFA#30, R5F104LEGFA#30, R5F104LFGFA#30, R5F104LGGFA#30, R5F104LHGFA#30, R5F104LJGFA#30, R5F104LKGFA#30, R5F104LLGFA#30<br>R5F104LCGFA#50, R5F104LDGFA#50, R5F104LEGFA#50, R5F104LFGFA#50, R5F104LGGFA#50, R5F104LHGFA#50, R5F104LJGFA#50, R5F104LKGFA#50, R5F104LLGFA#50 | |

**Note** For the fields of application, refer to **Figure 1 - 1 Part Number, Memory Size, and Package of RL78/G14**.

**Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.**

<R>

**Table 1 - 1 List of Ordering Part Numbers (9/12)**

| Pin count | Package | Fields of Application Note | Ordering Part Number | RENESAS Code |
|---|---|---|---|---|
| 64 pins | 64-pin plastic LFQFP (10 × 10 mm, 0.5 mm pitch) | A | R5F104LCAFB#V0, R5F104LDAFB#V0, R5F104LEAFB#V0, R5F104LFAFB#V0, R5F104LGAFB#V0, R5F104LHAFB#V0, R5F104LJAFB#V0<br>R5F104LCAFB#X0, R5F104LDAFB#X0, R5F104LEAFB#X0, R5F104LFAFB#X0, R5F104LGAFB#X0, R5F104LHAFB#X0, R5F104LJAFB#X0 | PLQP0064KF-A |
| | | | R5F104LCAFB#30, R5F104LDAFB#30, R5F104LEAFB#30, R5F104LFAFB#30, R5F104LGAFB#30, R5F104LHAFB#30, R5F104LJAFB#30, R5F104LKAFB#30, R5F104LLAFB#30<br>R5F104LCAFB#50, R5F104LDAFB#50, R5F104LEAFB#50, R5F104LFAFB#50, R5F104LGAFB#50, R5F104LHAFB#50, R5F104LJAFB#50, R5F104LKAFB#50, R5F104LLAFB#50 | PLQP0064KB-C |
| | | D | R5F104LCDFB#V0, R5F104LDDFB#V0, R5F104LEDFB#V0, R5F104LFDFB#V0, R5F104LGDFB#V0, R5F104LHDFB#V0, R5F104LJDFB#V0<br>R5F104LCDFB#X0, R5F104LDDFB#X0, R5F104LEDFB#X0, R5F104LFDFB#X0, R5F104LGDFB#X0, R5F104LHDFB#X0, R5F104LJDFB#X0 | PLQP0064KF-A |
| | | | R5F104LCDFB#30, R5F104LDDFB#30, R5F104LEDFB#30, R5F104LFDFB#30, R5F104LGDFB#30, R5F104LHDFB#30, R5F104LJDFB#30<br>R5F104LCDFB#50, R5F104LDDFB#50, R5F104LEDFB#50, R5F104LFDFB#50, R5F104LGDFB#50, R5F104LHDFB#50, R5F104LJDFB#50 | PLQP0064KB-C |
| | | G | R5F104LCGFB#V0, R5F104LDGFB#V0, R5F104LEGFB#V0, R5F104LFGFB#V0, R5F104LGGFB#V0, R5F104LHGFB#V0, R5F104LJGFB#V0<br>R5F104LCGFB#X0, R5F104LDGFB#X0, R5F104LEGFB#X0, R5F104LFGFB#X0, R5F104LGGFB#X0, R5F104LHGFB#X0, R5F104LJGFB#X0 | PLQP0064KF-A |
| | | | R5F104LCGFB#30, R5F104LDGFB#30, R5F104LEGFB#30, R5F104LFGFB#30, R5F104LGGFB#30, R5F104LHGFB#30, R5F104LJGFB#30, R5F104LKGFB#30, R5F104LLGFB#30<br>R5F104LCGFB#50, R5F104LDGFB#50, R5F104LEGFB#50, R5F104LFGFB#50, R5F104LGGFB#50, R5F104LHGFB#50, R5F104LJGFB#50, R5F104LKGFB#50, R5F104LLGFB#50 | PLQP0064KB-C |

**Note** For the fields of application, refer to **Figure 1 - 1 Part Number, Memory Size, and Package of RL78/G14**.

**Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.**

<R>

**Table 1 - 1 List of Ordering Part Numbers (10/12)**

| Pin count | Package | Fields of Application Note | Ordering Part Number | RENESAS Code |
|---|---|---|---|---|
| 64 pins | 64-pin plastic FLGA (5 × 5 mm, 0.5 mm pitch) | A | R5F104LCALA#U0, R5F104LDALA#U0, R5F104LEALA#U0, R5F104LFALA#U0, R5F104LGALA#U0, R5F104LHALA#U0, R5F104LJALA#U0, R5F104LKALA#U0, R5F104LLALA#U0<br>R5F104LCALA#W0, R5F104LDALA#W0, R5F104LEALA#W0, R5F104LFALA#W0, R5F104LGALA#W0, R5F104LHALA#W0, R5F104LJALA#W0, R5F104LKALA#W0, R5F104LLALA#W0 | PWLG0064KA-A |
| | | G | R5F104LCGLA#U0, R5F104LDGLA#U0, R5F104LEGLA#U0, R5F104LFGLA#U0, R5F104LGGLA#U0, R5F104LHGLA#U0, R5F104LJGLA#U0, R5F104LKGLA#U0, R5F104LLGLA#U0<br>R5F104LCGLA#W0, R5F104LDGLA#W0, R5F104LEGLA#W0, R5F104LFGLA#W0, R5F104LGGLA#W0, R5F104LHGLA#W0, R5F104LJGLA#W0, R5F104LKGLA#W0, R5F104LLGLA#W0 | |
| | 64-pin plastic LQFP (14 × 14 mm, 0.8 mm pitch) | A | R5F104LCAFP#V0, R5F104LDAFP#V0, R5F104LEAFP#V0, R5F104LFAFP#V0, R5F104LGAFP#V0, R5F104LHAFP#V0, R5F104LJAFP#V0<br>R5F104LCAFP#X0, R5F104LDAFP#X0, R5F104LEAFP#X0, R5F104LFAFP#X0, R5F104LGAFP#X0, R5F104LHAFP#X0, R5F104LJAFP#X0<br>R5F104LCAFP#30, R5F104LDAFP#30, R5F104LEAFP#30, R5F104LFAFP#30, R5F104LGAFP#30, R5F104LHAFP#30, R5F104LJAFP#30<br>R5F104LCAFP#50, R5F104LDAFP#50, R5F104LEAFP#50, R5F104LFAFP#50, R5F104LGAFP#50, R5F104LHAFP#50, R5F104LJAFP#50 | PLQP0064GA-A |
| | | D | R5F104LCDFP#V0, R5F104LDDFP#V0, R5F104LEDFP#V0, R5F104LFDFP#V0, R5F104LGDFP#V0, R5F104LHDFP#V0, R5F104LJDFP#V0<br>R5F104LCDFP#X0, R5F104LDDFP#X0, R5F104LEDFP#X0, R5F104LFDFP#X0, R5F104LGDFP#X0, R5F104LHDFP#X0, R5F104LJDFP#X0<br>R5F104LCDFP#30, R5F104LDDFP#30, R5F104LEDFP#30, R5F104LFDFP#30, R5F104LGDFP#30, R5F104LHDFP#30, R5F104LJDFP#30<br>R5F104LCDFP#50, R5F104LDDFP#50, R5F104LEDFP#50, R5F104LFDFP#50, R5F104LGDFP#50, R5F104LHDFP#50, R5F104LJDFP#50 | |
| | | G | R5F104LCGFP#V0, R5F104LDGFP#V0, R5F104LEGFP#V0, R5F104LFGFP#V0, R5F104LGGFP#V0, R5F104LHGFP#V0, R5F104LJGFP#V0<br>R5F104LCGFP#X0, R5F104LDGFP#X0, R5F104LEGFP#X0, R5F104LFGFP#X0, R5F104LGGFP#X0, R5F104LHGFP#X0, R5F104LJGFP#X0<br>R5F104LCGFP#30, R5F104LDGFP#30, R5F104LEGFP#30, R5F104LFGFP#30, R5F104LGGFP#30, R5F104LHGFP#30, R5F104LJGFP#30<br>R5F104LCGFP#50, R5F104LDGFP#50, R5F104LEGFP#50, R5F104LFGFP#50, R5F104LGGFP#50, R5F104LHGFP#50, R5F104LJGFP#50 | |

**Note** For the fields of application, refer to **Figure 1 - 1 Part Number, Memory Size, and Package of RL78/G14**.

**Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.**

<R>

**Table 1 - 1 List of Ordering Part Numbers (11/12)**

| Pin count | Package | Fields of Application Note | Ordering Part Number | RENESAS Code |
|---|---|---|---|---|
| 80 pins | 80-pin plastic LFQFP (12 × 12 mm, 0.5 mm pitch) | A | R5F104MFAFB#V0, R5F104MGAFB#V0, R5F104MHAFB#V0, R5F104MJAFB#V0<br>R5F104MFAFB#X0, R5F104MGAFB#X0, R5F104MHAFB#X0, R5F104MJAFB#X0 | PLQP0080KE-A |
| | | | R5F104MFAFB#30, R5F104MGAFB#30, R5F104MHAFB#30, R5F104MJAFB#30, R5F104MKAFB#30, R5F104MLAFB#30<br>R5F104MFAFB#50, R5F104MGAFB#50, R5F104MHAFB#50 R5F104MJAFB#50, R5F104MKAFB#50, R5F104MLAFB#50 | PLQP0080KB-B |
| | | D | R5F104MFDFB#V0, R5F104MGDFB#V0, R5F104MHDFB#V0, R5F104MJDFB#V0<br>R5F104MFDFB#X0, R5F104MGDFB#X0, R5F104MHDFB#X0, R5F104MJDFB#X0 | PLQP0080KE-A |
| | | | R5F104MFDFB#30, R5F104MGDFB#30, R5F104MHDFB#30, R5F104MJDFB#30<br>R5F104MFDFB#50, R5F104MGDFB#50, R5F104MHDFB#50, R5F104MJDFB#50 | PLQP0080KB-B |
| | | G | R5F104MFGFB#V0, R5F104MGGFB#V0, R5F104MHGFB#V0, R5F104MJGFB#V0<br>R5F104MFGFB#X0, R5F104MGGFB#X0, R5F104MHGFB#X0, R5F104MJGFB#X0 | PLQP0080KE-A |
| | | | R5F104MFGFB#30, R5F104MGGFB#30, R5F104MHGFB#30, R5F104MJGFB#30, R5F104MKGFB#30, R5F104MLGFB#30<br>R5F104MFGFB#50, R5F104MGGFB#50, R5F104MHGFB#50, R5F104MJGFB#50, R5F104MKGFB#50, R5F104MLGFB#50 | PLQP0080KB-B |
| | 80-pin plastic LQFP (14 × 14 mm, 0.65 mm pitch) | A | R5F104MFAFA#V0, R5F104MGAFA#V0, R5F104MHAFA#V0, R5F104MJAFA#V0<br>R5F104MFAFA#X0, R5F104MGAFA#X0, R5F104MHAFA#X0, R5F104MJAFA#X0<br>R5F104MFAFA#30, R5F104MGAFA#30, R5F104MHAFA#30, R5F104MJAFA#30, R5F104MKAFA#30, R5F104MLAFA#30<br>R5F104MFAFA#50, R5F104MGAFA#50, R5F104MHAFA#50, R5F104MJAFA#50, R5F104MKAFA#50, R5F104MLAFA#50 | PLQP0080JB-E |
| | | D | R5F104MFDFA#V0, R5F104MGDFA#V0, R5F104MHDFA#V0, R5F104MJDFA#V0<br>R5F104MFDFA#X0, R5F104MGDFA#X0, R5F104MHDFA#X0, R5F104MJDFA#X0<br>R5F104MFDFA#30, R5F104MGDFA#30, R5F104MHDFA#30, R5F104MJDFA#30<br>R5F104MFDFA#50, R5F104MGDFA#50, R5F104MHDFA#50, R5F104MJDFA#50 | |
| | | G | R5F104MFGFA#V0, R5F104MGGFA#V0, R5F104MHGFA#V0, R5F104MJGFA#V0<br>R5F104MFGFA#X0, R5F104MGGFA#X0, R5F104MHGFA#X0, R5F104MJGFA#X0<br>R5F104MFGFA#30, R5F104MGGFA#30, R5F104MHGFA#30, R5F104MJGFA#30, R5F104MKGFA#30, R5F104MLGFA#30<br>R5F104MFGFA#50, R5F104MGGFA#50, R5F104MHGFA#50, R5F104MJGFA#50, R5F104MKGFA#50, R5F104MLGFA#50 | |

**Note** For the fields of application, refer to **Figure 1 - 1 Part Number, Memory Size, and Package of RL78/G14**.

**Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.**

<R>

**Table 1 - 1 List of Ordering Part Numbers (12/12)**

| Pin count | Package | Fields of Application Note | Ordering Part Number | RENESAS Code |
|---|---|---|---|---|
| 100 pins | 100-pin plastic LFQFP (14 × 14 mm, 0.5 mm pitch) | A | R5F104PFAFB#V0, R5F104PGAFB#V0, R5F104PHAFB#V0, R5F104PJAFB#V0<br>R5F104PFAFB#X0, R5F104PGAFB#X0, R5F104PHAFB#X0, R5F104PJAFB#X0 | PLQP0100KE-A |
| | | | R5F104PFAFB#30, R5F104PGAFB#30, R5F104PHAFB#30, R5F104PJAFB#30, R5F104PKAFB#30, R5F104PLAFB#30<br>R5F104PFAFB#50, R5F104PGAFB#50, R5F104PHAFB#50, R5F104PJAFB#50, R5F104PKAFB#50, R5F104PLAFB#50 | PLQP0100KB-B |
| | | D | R5F104PFDFB#V0, R5F104PGDFB#V0, R5F104PHDFB#V0, R5F104PJDFB#V0<br>R5F104PFDFB#X0, R5F104PGDFB#X0, R5F104PHDFB#X0, R5F104PJDFB#X0 | PLQP0100KE-A |
| | | | R5F104PFDFB#30, R5F104PGDFB#30, R5F104PHDFB#30, R5F104PJDFB#30<br>R5F104PFDFB#50, R5F104PGDFB#50, R5F104PHDFB#50, R5F104PJDFB#50 | PLQP0100KB-B |
| | | G | R5F104PFGFB#V0, R5F104PGGFB#V0, R5F104PHGFB#V0, R5F104PJGFB#V0<br>R5F104PFGFB#X0, R5F104PGGFB#X0, R5F104PHGFB#X0, R5F104PJGFB#X0 | PLQP0100KE-A |
| | | | R5F104PFGFB#30, R5F104PGGFB#30, R5F104PHGFB#30, R5F104PJGFB#30, R5F104PKGFB#30, R5F104PLGFB#30<br>R5F104PFGFB#50, R5F104PGGFB#50, R5F104PHGFB#50, R5F104PJGFB#50, R5F104PKGFB#50, R5F104PLGFB#50 | PLQP0100KB-B |
| | 100-pin plastic LQFP (14 × 20 mm, 0.65 mm pitch) | A | R5F104PFAFA#V0, R5F104PGAFA#V0, R5F104PHAFA#V0, R5F104PJAFA#V0<br>R5F104PFAFA#X0, R5F104PGAFA#X0, R5F104PHAFA#X0, R5F104PJAFA#X0<br>R5F104PFAFA#30, R5F104PGAFA#30, R5F104PHAFA#30, R5F104PJAFA#30, R5F104PKAFA#30, R5F104PLAFA#30<br>R5F104PFAFA#50, R5F104PGAFA#50, R5F104PHAFA#50, R5F104PJAFA#50, R5F104PKAFA#50, R5F104PLAFA#50 | PLQP0100JC-A |
| | | D | R5F104PFDFA#V0, R5F104PGDFA#V0, R5F104PHDFA#V0, R5F104PJDFA#V0<br>R5F104PFDFA#X0, R5F104PGDFA#X0, R5F104PHDFA#X0, R5F104PJDFA#X0<br>R5F104PFDFA#30, R5F104PGDFA#30, R5F104PHDFA#30, R5F104PJDFA#30<br>R5F104PFDFA#50, R5F104PGDFA#50, R5F104PHDFA#50, R5F104PJDFA#50 | |
| | | G | R5F104PFGFA#V0, R5F104PGGFA#V0, R5F104PHGFA#V0, R5F104PJGFA#V0<br>R5F104PFGFA#X0, R5F104PGGFA#X0, R5F104PHGFA#X0, R5F104PJGFA#X0<br>R5F104PFGFA#30, R5F104PGGFA#30, R5F104PHGFA#30, R5F104PJGFA#30, R5F104PKGFA#30, R5F104PLGFA#30<br>R5F104PFGFA#50, R5F104PGGFA#50, R5F104PHGFA#50, R5F104PJGFA#50, R5F104PKGFA#50, R5F104PLGFA#50 | |

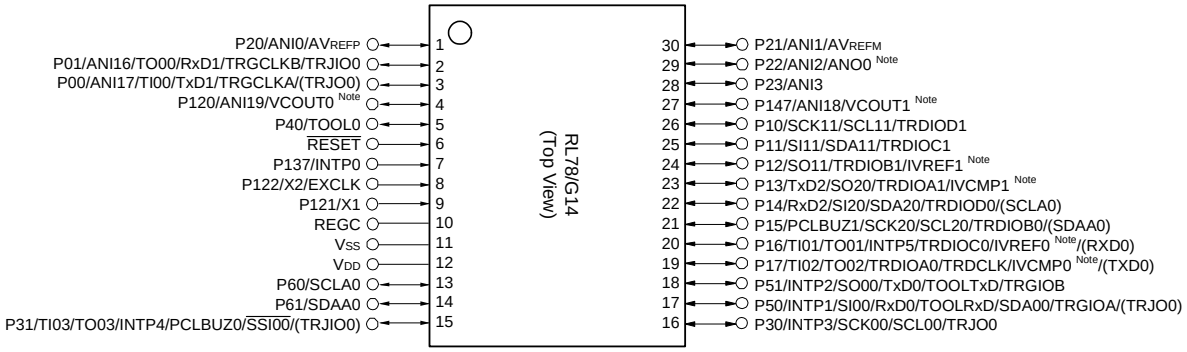
**Note** For the fields of application, refer to **Figure 1 - 1 Part Number, Memory Size, and Package of RL78/G14**.

**Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.**

## 1.3 Pin Configuration (Top View)

### 1.3.1 30-pin products

• 30-pin plastic LSSOP (7.62 mm (300), 0.65 mm pitch)




**Note** Mounted on the 96 KB or more code flash memory products.

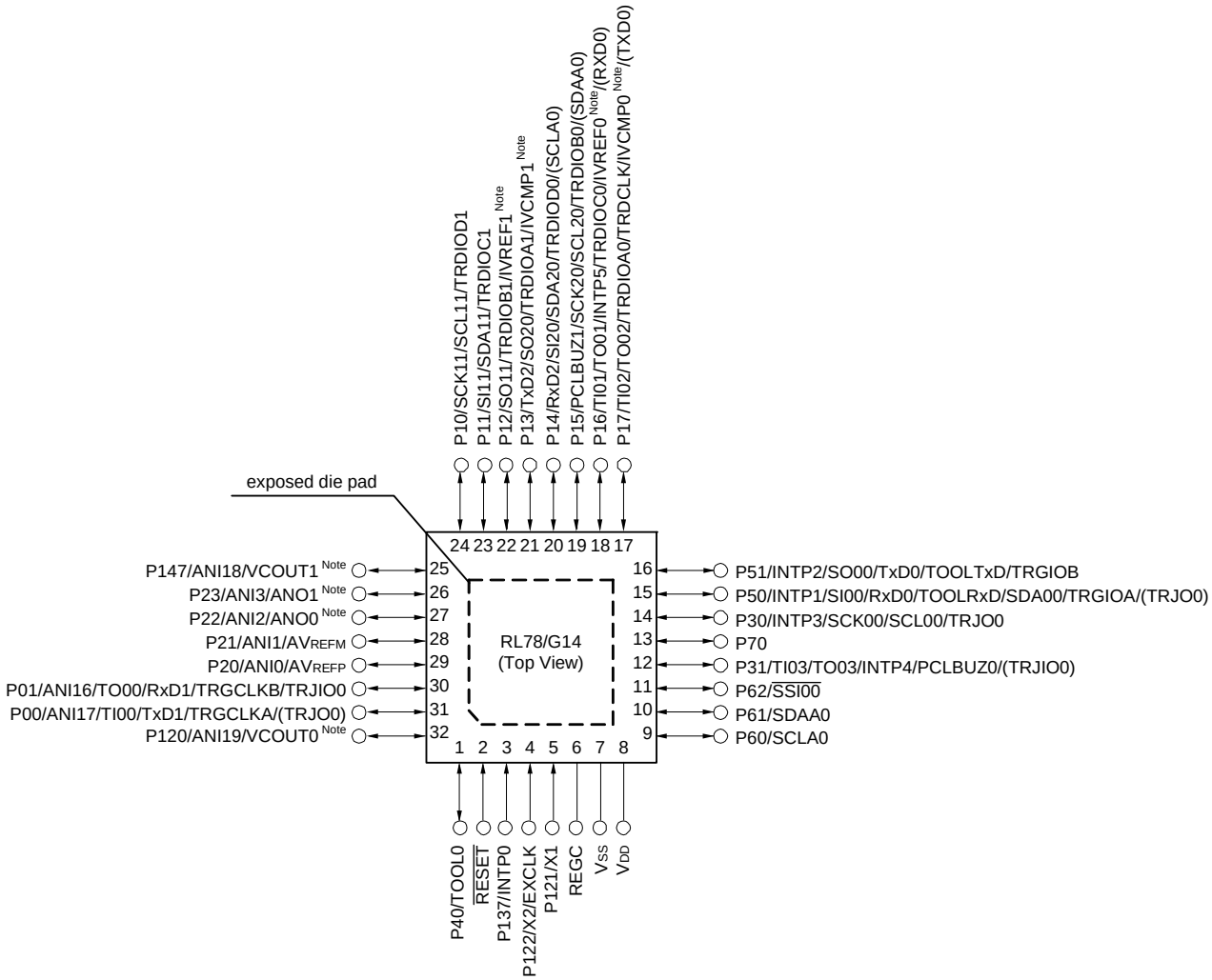
**Caution** **Connect the REGC pin to Vss pin via a capacitor (0.47 to 1 μF).**

**Remark 1.** For pin identification, see **1.4 Pin Identification**.

**Remark 2.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).

### 1.3.2 32-pin products

• 32-pin plastic HWQFN (5 × 5 mm, 0.5 mm pitch)




**Note** Mounted on the 96 KB or more code flash memory products.

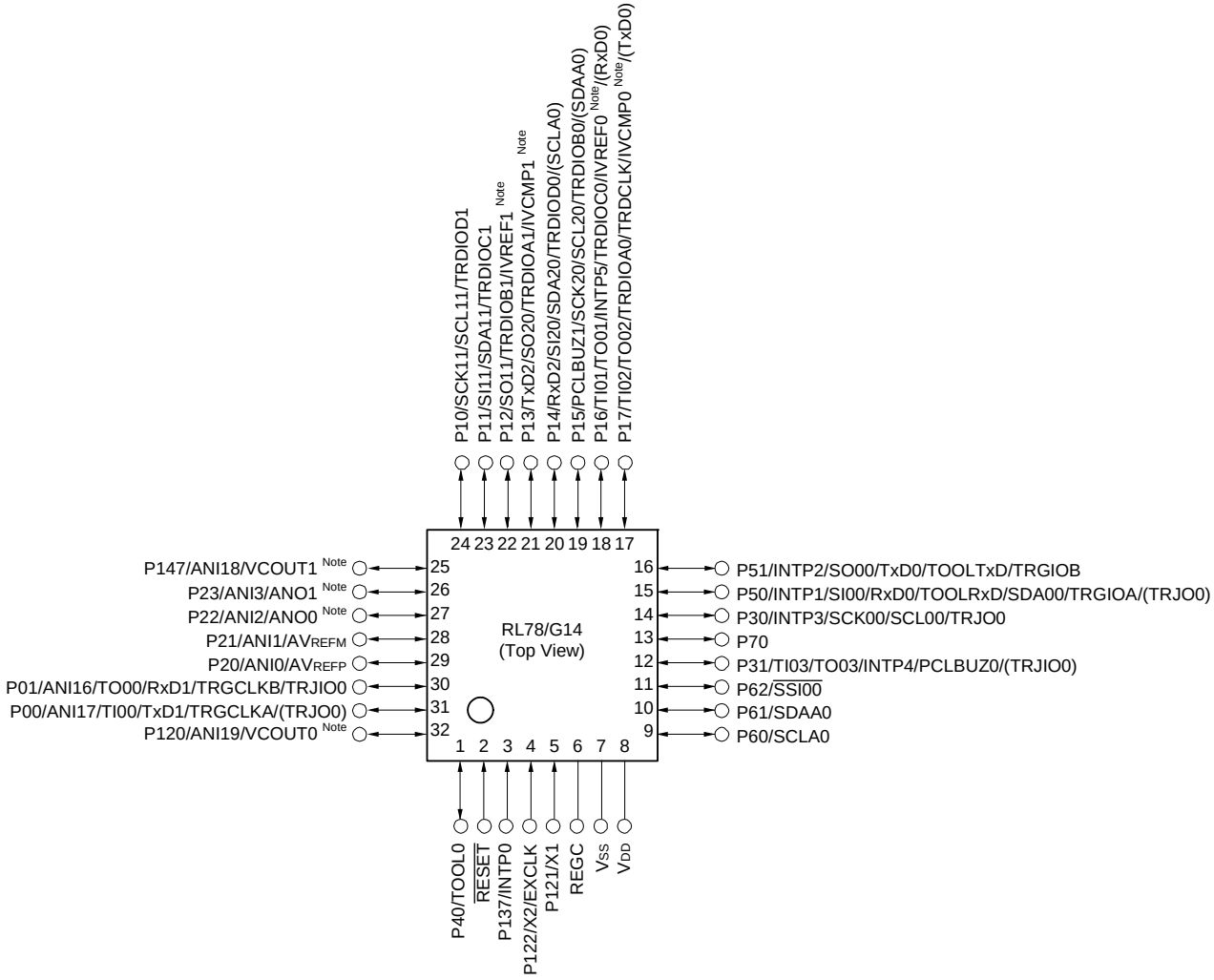
**Caution** **Connect the REGC pin to Vss pin via a capacitor (0.47 to 1 μF).**

**Remark 1.** For pin identification, see **1.4 Pin Identification**.

**Remark 2.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).

**Remark 3.** It is recommended to connect an exposed die pad to Vss.

• 32-pin plastic LQFP (7 × 7 mm, 0.8 mm pitch)




**Note** Mounted on the 96 KB or more code flash memory products.

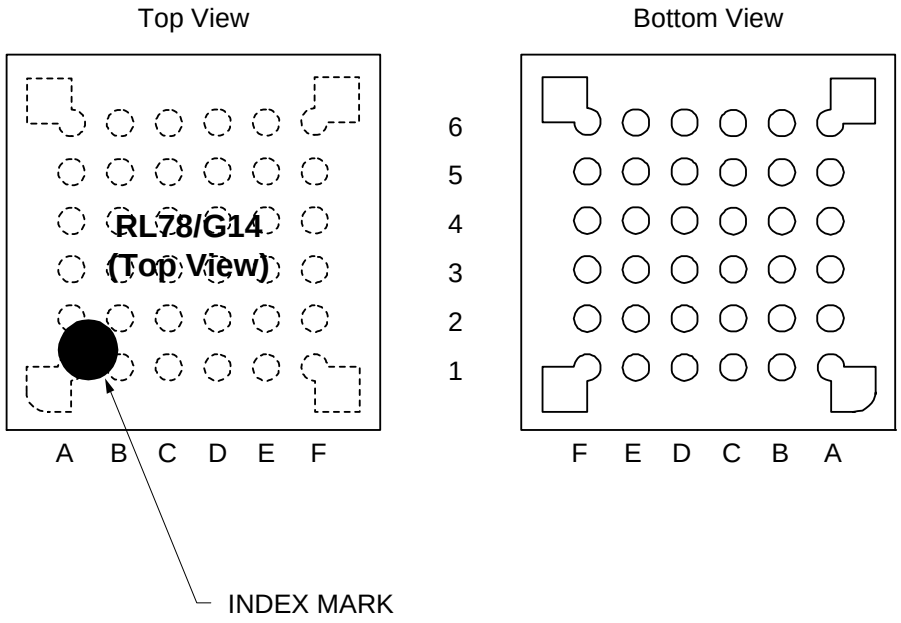
**Caution** **Connect the REGC pin to Vss pin via a capacitor (0.47 to 1 μF).**

**Remark 1.** For pin identification, see **1.4 Pin Identification**.

**Remark 2.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).

### 1.3.3 36-pin products

• 36-pin plastic WFLGA (4 × 4 mm, 0.5 mm pitch)




| | A | B | C | D | E | F | |
|---|---|---|---|---|---|---|---|
| 6 | P60/SCLA0 | VDD | P121/X1 | P122/X2/EXCLK | P137/INTP0 | P40/TOOL0 | 6 |
| 5 | P62/$\overline{SSI00}$ | P61/SDAA0 | VSS | REGC | $\overline{RESET}$ | P120/ANI19/ VCOUT0 Note | 5 |
| 4 | P72/SO21 | P71/SI21/ SDA21 | P14/RxD2/SI20/ SDA20/TRDIOD0/ (SCLA0) | P31/TI03/TO03/ INTP4/PCLBUZ0/ (TRJIO0) | P00/TI00/TxD1/ TRGCLKA/ (TRJO0) | P01/TO00/ RxD1/TRGCLKB/ TRJIO0 | 4 |
| 3 | P50/INTP1/ SI00/RxD0/ TOOLRxD/ SDA00/TRGIOA/ (TRJO0) | P70/SCK21/ SCL21 | P15/PCLBUZ1/ SCK20/SCL20/ TRDIOB0/ (SDAA0) | P22/ANI2/ ANO0 Note | P20/ANI0/ AVREFP | P21/ANI1/ AVREFM | 3 |
| 2 | P30/INTP3/ SCK00/SCL00/ TRJO0 | P16/TI01/TO01/ INTP5/TRDIOC0/ IVREF0 Note/ (RXD0) | P12/SO11/ TRDIOB1/ IVREF1 Note | P11/SI11/ SDA11/ TRDIOC1 | P24/ANI4 | P23/ANI3/ ANO1 Note | 2 |
| 1 | P51/INTP2/ SO00/TxD0/ TOOLTxD/ TRGIOB | P17/TI02/TO02/ TRDIOA0/ TRDCLK/ IVCMP0 Note/ (TXD0) | P13/TxD2/ SO20/TRDIOA1/ IVCMP1 Note | P10/SCK11/ SCL11/ TRDIOD1 | P147/ANI18/ VCOUT1 Note | P25/ANI5 | 1 |
| | A | B | C | D | E | F | |

**Note** Mounted on the 96 KB or more code flash memory products.

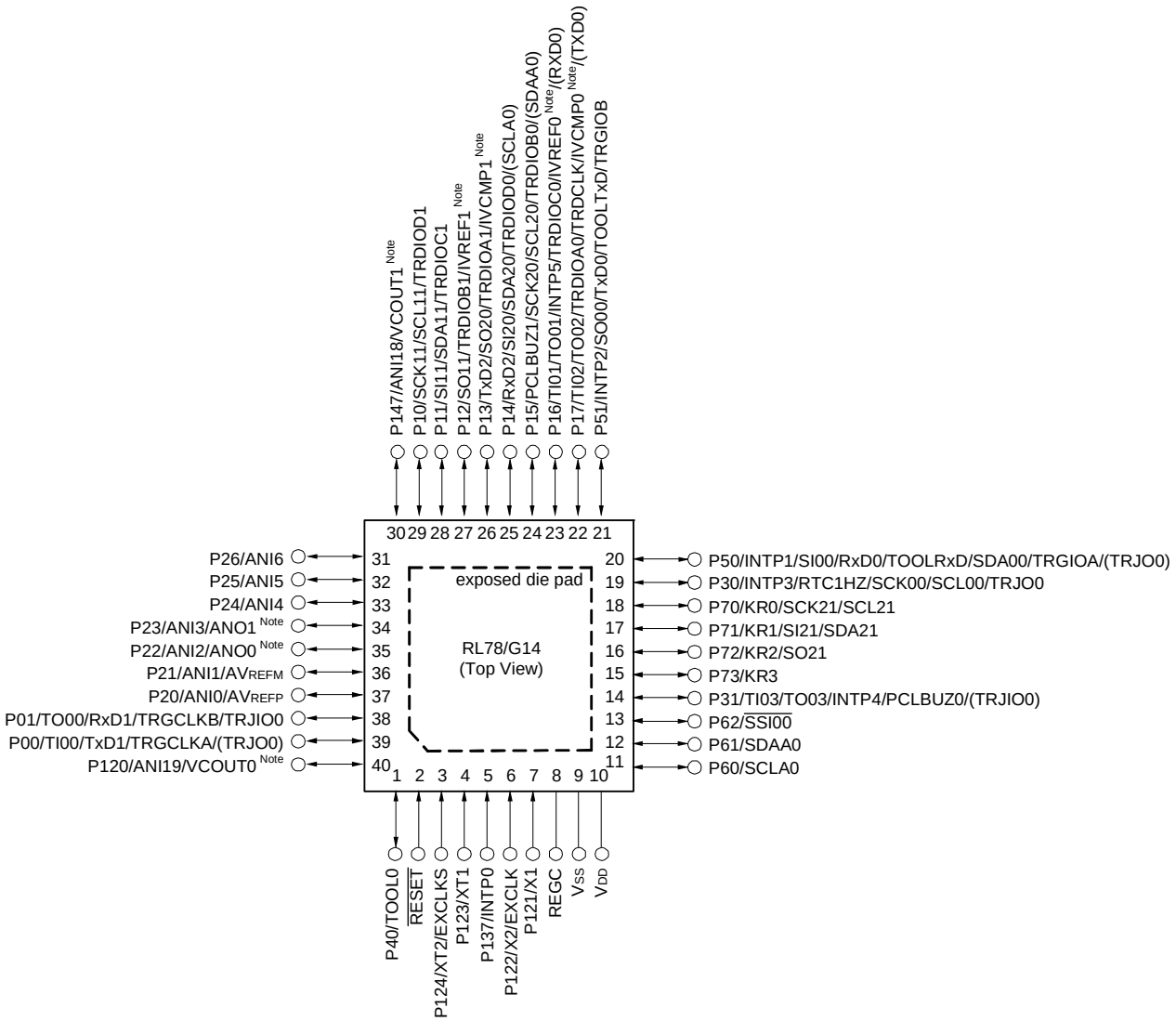
**Caution** **Connect the REGC pin to Vss pin via a capacitor (0.47 to 1 μF).**

**Remark 1.** For pin identification, see **1.4 Pin Identification**.

**Remark 2.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).

### 1.3.4 40-pin products

• 40-pin plastic HWQFN (6 × 6 mm, 0.5 mm pitch)




**Note** Mounted on the 96 KB or more code flash memory products.

**Caution Connect the REGC pin to Vss pin via a capacitor (0.47 to 1 μF).**

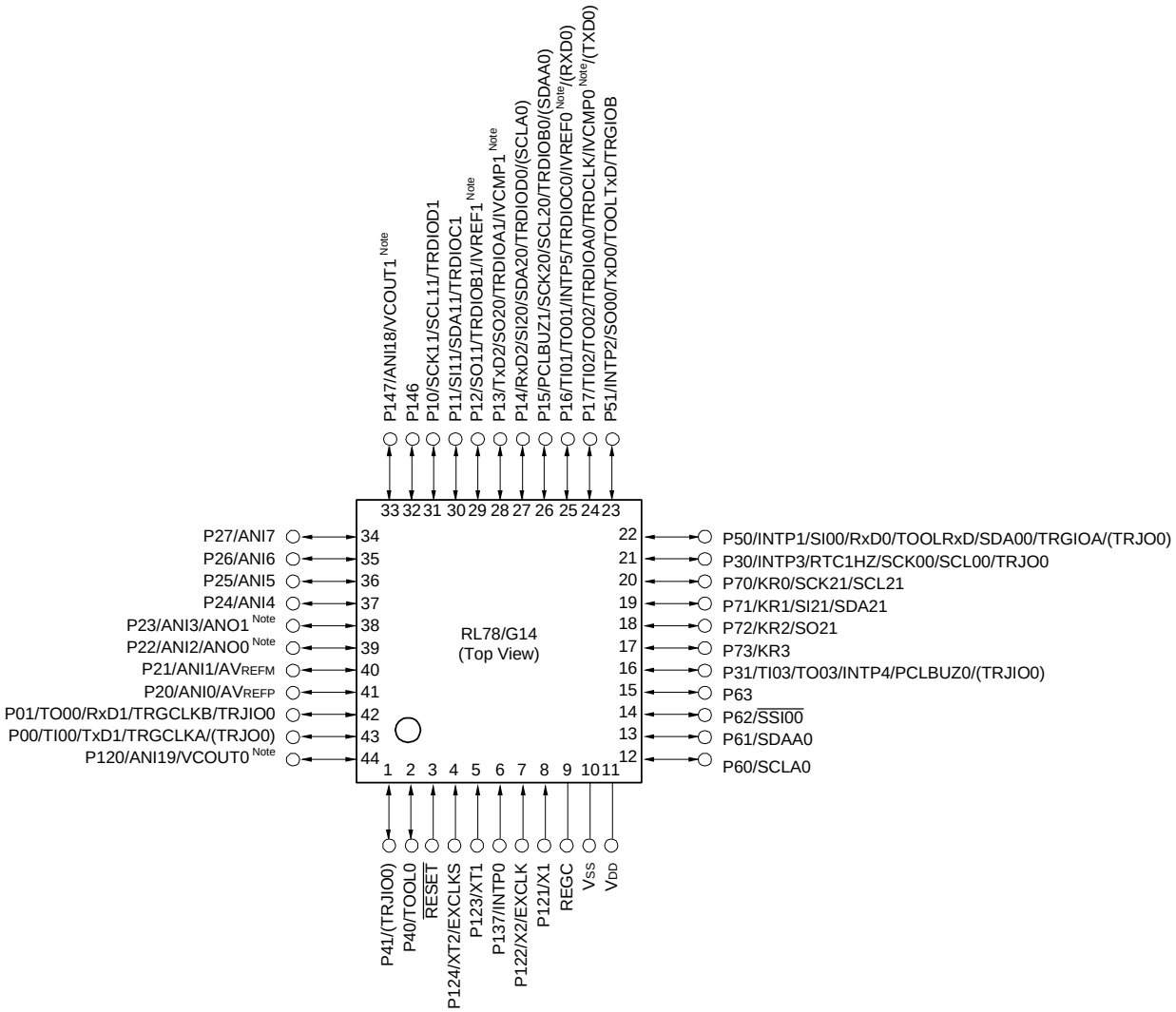
**Remark 1.** For pin identification, see **1.4 Pin Identification**.

**Remark 2.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).

**Remark 3.** It is recommended to connect an exposed die pad to Vss.

### 1.3.5 44-pin products

• 44-pin plastic LQFP (10 × 10 mm, 0.8 mm pitch)




**Note** Mounted on the 96 KB or more code flash memory products.

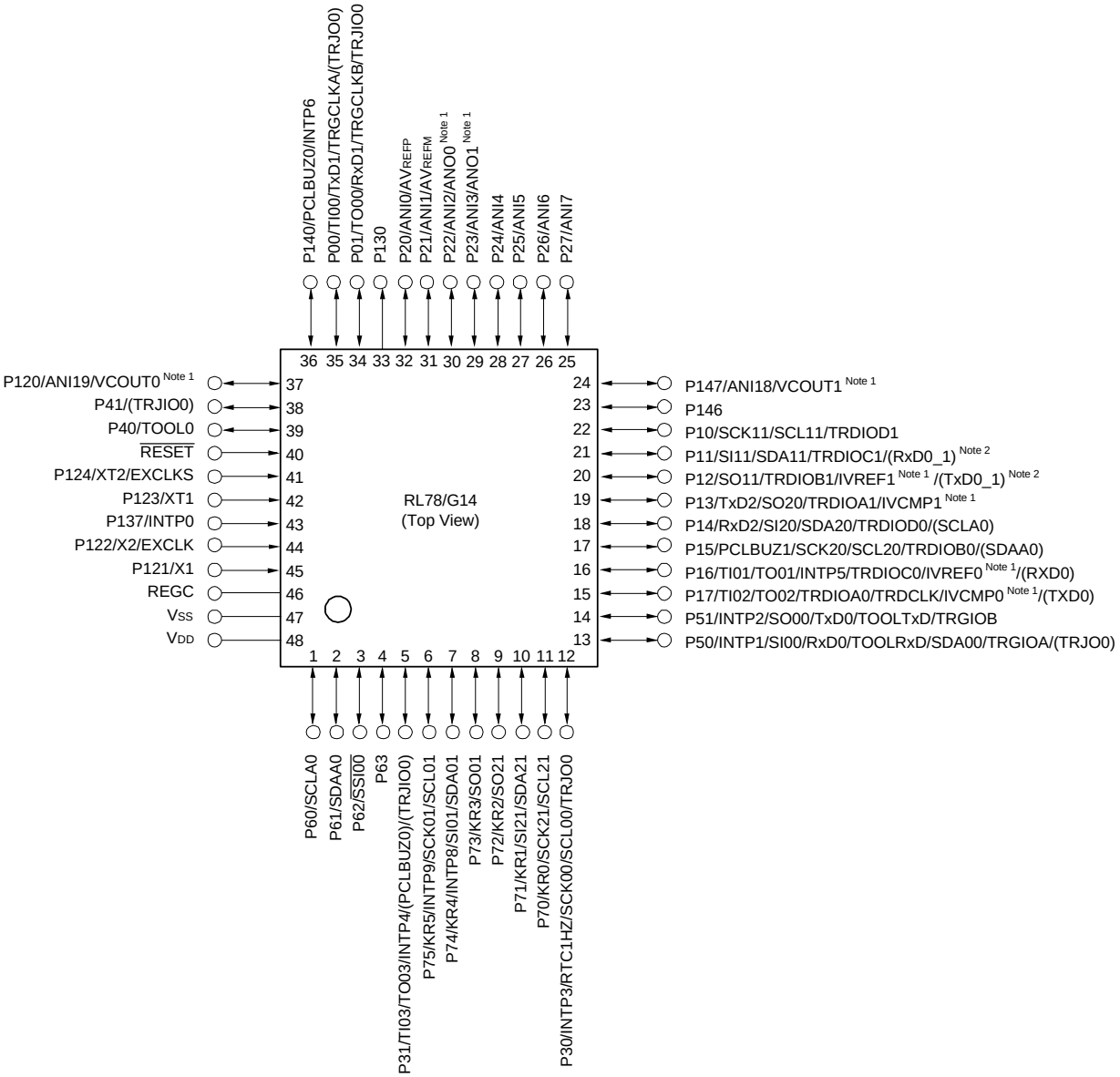
**Caution** **Connect the REGC pin to Vss pin via a capacitor (0.47 to 1 μF).**

**Remark 1.** For pin identification, see **1.4 Pin Identification**.

**Remark 2.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).

### 1.3.6 48-pin products

• 48-pin plastic LFQFP (7 × 7 mm, 0.5 mm pitch)




**Note 1.** Mounted on the 96 KB or more code flash memory products.

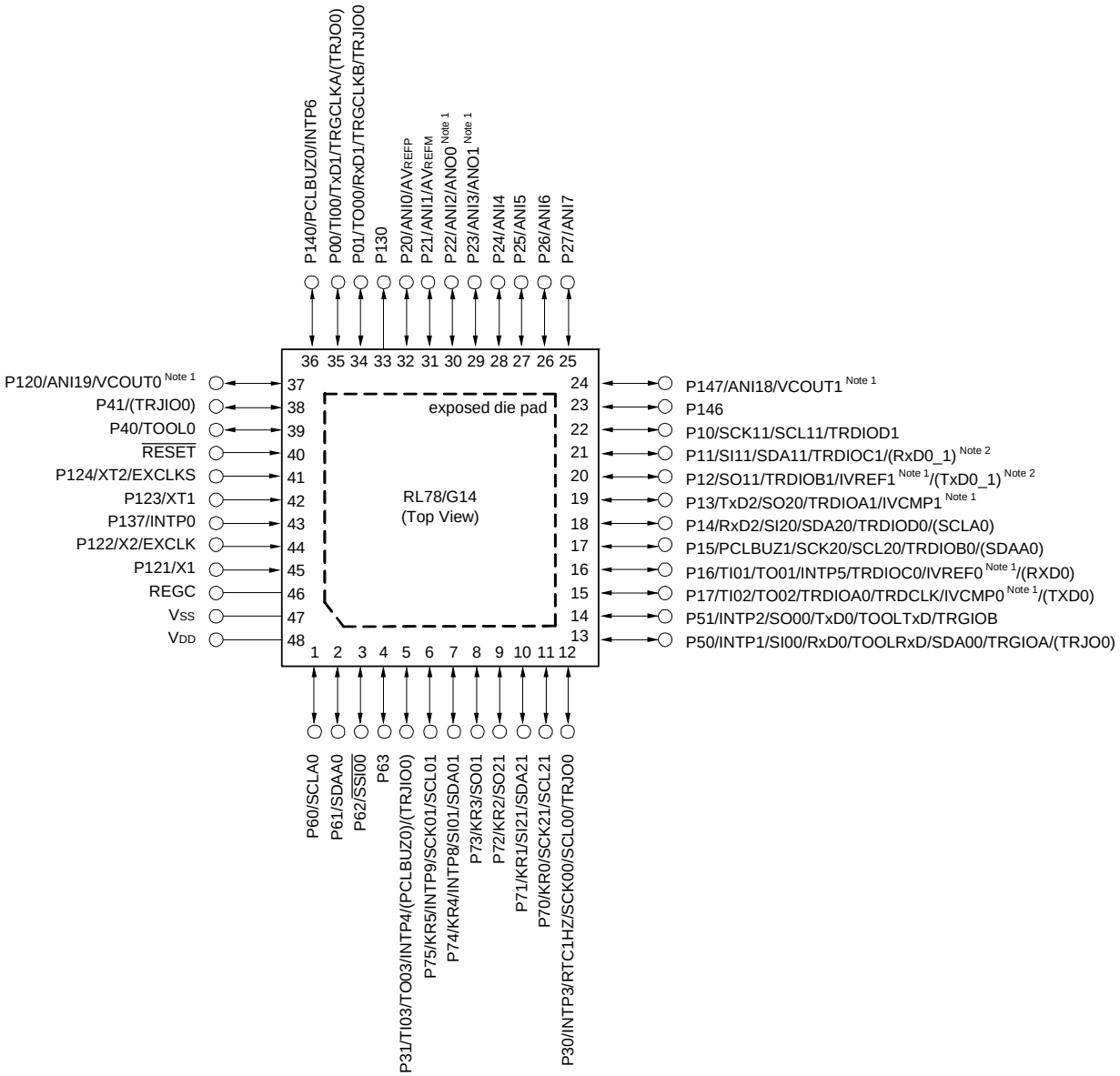
**Note 2.** Mounted on the 384 KB or more code flash memory products.

**Caution Connect the REGC pin to Vss pin via a capacitor (0.47 to 1 μF).**

**Remark 1.** For pin identification, see **1.4 Pin Identification**.

**Remark 2.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).

• 48-pin plastic HWQFN (7 × 7 mm, 0.5 mm pitch)




**Note 1.** Mounted on the 96 KB or more code flash memory products.

**Note 2.** Mounted on the 384 KB or more code flash memory products.

**Caution** **Connect the REGC pin to Vss pin via a capacitor (0.47 to 1 μF).**

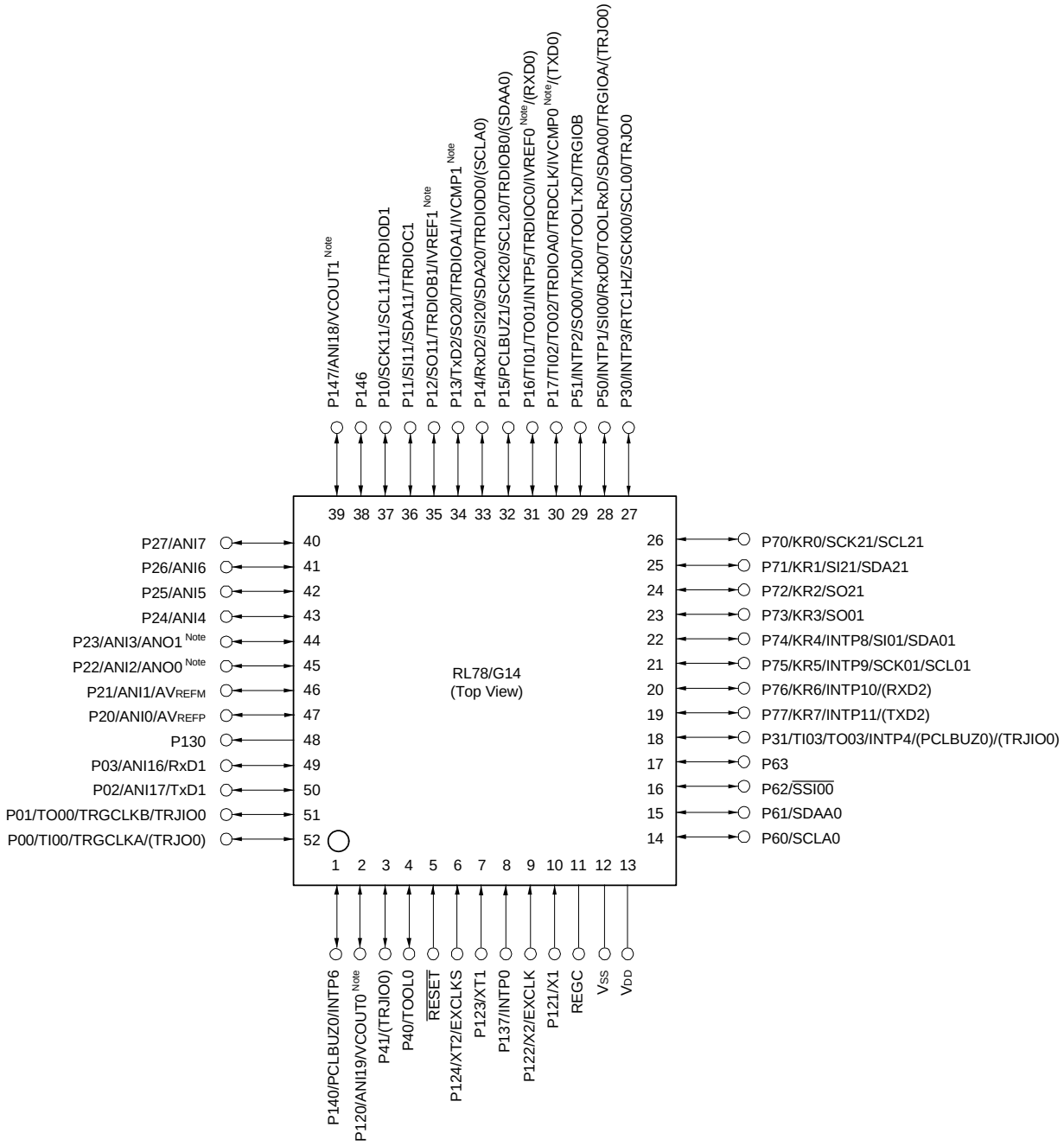
**Remark 1.** For pin identification, see **1.4 Pin Identification**.

**Remark 2.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).

**Remark 3.** It is recommended to connect an exposed die pad to Vss.

### 1.3.7 52-pin products

• 52-pin plastic LQFP (10 × 10 mm, 0.65 mm pitch)




**Note** Mounted on the 96 KB or more code flash memory products.

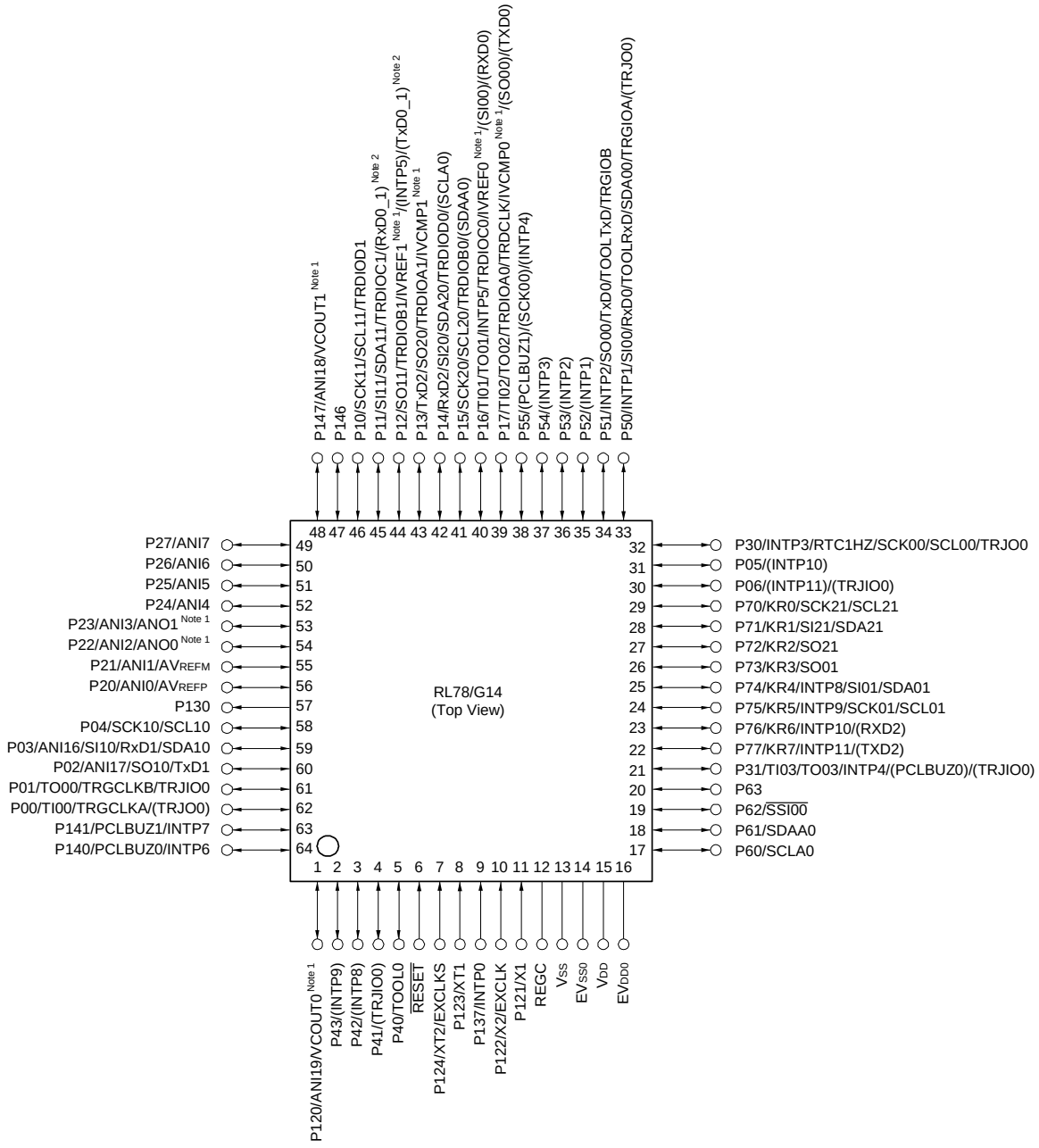
**Caution** **Connect the REGC pin to Vss pin via a capacitor (0.47 to 1 μF).**

**Remark 1.** For pin identification, see **1.4 Pin Identification**.

**Remark 2.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).

### 1.3.8 64-pin products

- 64-pin plastic LQFP (14 × 14 mm, 0.8 mm pitch)
- 64-pin plastic LQFP (12 × 12 mm, 0.65 mm pitch)
- 64-pin plastic LFQFP (10 × 10 mm, 0.5 mm pitch)




**Note 1.** Mounted on the 96 KB or more code flash memory products.

**Note 2.** Mounted on the 384 KB or more code flash memory products.

**Caution 1. Make EVSS0 pin the same potential as VSS pin.**

**Caution 2. Make VDD pin the potential that is higher than EVDD0 pin.**

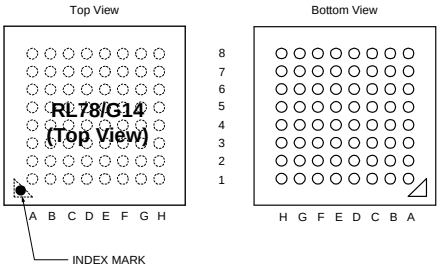
**Caution 3. Connect the REGC pin to VSS pin via a capacitor (0.47 to 1 μF).**

**Remark 1.** For pin identification, see **1.4 Pin Identification**.

**Remark 2.** When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the VDD and EVDD0 pins and connect the VSS and EVSS0 pins to separate ground lines.

**Remark 3.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).

• 64-pin plastic FLGA (5 × 5 mm, 0.5 mm pitch)




| | A | B | C | D | E | F | G | H | |
|---|---|---|---|---|---|---|---|---|---|
| 8 | $EV_{DD0}$ | $EV_{SS0}$ | P121/X1 | P122/X2/ EXCLK | P137/INTP0 | P123/XT1 | P124/XT2/ EXCLKS | P120/ANI19/ $VCOUT0$ Note 1 | 8 |
| 7 | P60/SCLA0 | $V_{DD}$ | $V_{SS}$ | REGC | $\overline{RESET}$ | P01/TO00/ TRGCLKB/ TRJIO0 | P00/TI00/ TRGCLKA/ (TRJO0) | P140/ PCLBUZ0/ INTP6 | 7 |
| 6 | P61/SDAA0 | P62/$\overline{SSI00}$ | P63 | P40/TOOL0 | P41/(TRJIO0) | P43/(INTP9) | P02/ANI17/ SO10/TxD1 | P141/ PCLBUZ1/ INTP7 | 6 |
| 5 | P77/KR7/ INTP11/(TXD2) | P31/TI03/ TO03/INTP4/ (PCLBUZ0)/ (TRJIO0) | P53/(INTP2) | P42/(INTP8) | P03/ANI16/ SI10/RxD1/ SDA10 | P04/SCK10/ SCL10 | P130 | P20/ANI0/ $AV_{REFP}$ | 5 |
| 4 | P75/KR5/ INTP9/ SCK01/ SCL01 | P76/KR6/ INTP10/ (RXD2) | P52/(INTP1) | P54/(INTP3) | P16/TI01/ TO01/INTP5/ TRDIOC0/ IVREF0 Note 1/ (SI00)/(RXD0) | P21/ANI1/ $AV_{REFM}$ | P22/ANI2/ ANO0 Note 1 | P23/ANI3/ ANO1 Note 1 | 4 |
| 3 | P70/KR0/ SCK21/ SCL21 | P73/KR3/ SO01 | P74/KR4/ INTP8/SI01/ SDA01 | P17/TI02/TO02/ TRDIOA0/ TRDCLK/ IVCMP0 Note 1/ (SO00)/(TXD0) | P15/SCK20/ SCL20/ TRDIOB0/ (SDAA0) | P12/SO11/ TRDIOB1/ IVREF1 Note 1/ (INTP5)/ (TxD0_1) Note 2 | P24/ANI4 | P26/ANI6 | 3 |
| 2 | P30/INTP3/ RTC1HZ/ SCK00/ SCL00/TRJO0 | P72/KR2/ SO21 | P71/KR1/ SI21/SDA21 | P06/(INTP11)/ (TRJIO0) | P14/RxD2/ SI20/SDA20/ TRDIOD0/ (SCLA0) | P11/SI11/ SDA11/ TRDIOC1/ (RxD0_1) Note 2 | P25/ANI5 | P27/ANI7 | 2 |
| 1 | P05/(INTP10) | P50/INTP1/ SI00/RxD0/ TOOLRxD/ SDA00/ TRGIOA/ (TRJO0) | P51/INTP2/ SO00/TxD0/ TOOLTxD/ TRGIOB | P55/ (PCLBUZ1)/ (SCK00)/ (INTP4) | P13/TxD2/ SO20/ TRDIOA1/ IVCMP1 Note 1 | P10/SCK11/ SCL11/ TRDIOD1 | P146 | P147/ANI18/ VCOUT1 Note 1 | 1 |
| | A | B | C | D | E | F | G | H | |

**Note 1.** Mounted on the 96 KB or more code flash memory products.

**Note 2.** Mounted on the 384 KB or more code flash memory products.

**Caution 1. Make $EV_{SS0}$ pin the same potential as VSS pin.**

**Caution 2. Make $V_{DD}$ pin the potential that is higher than $EV_{DD0}$ pin.**

**Caution 3. Connect the REGC pin to $V_{SS}$ pin via a capacitor (0.47 to 1 μF).**

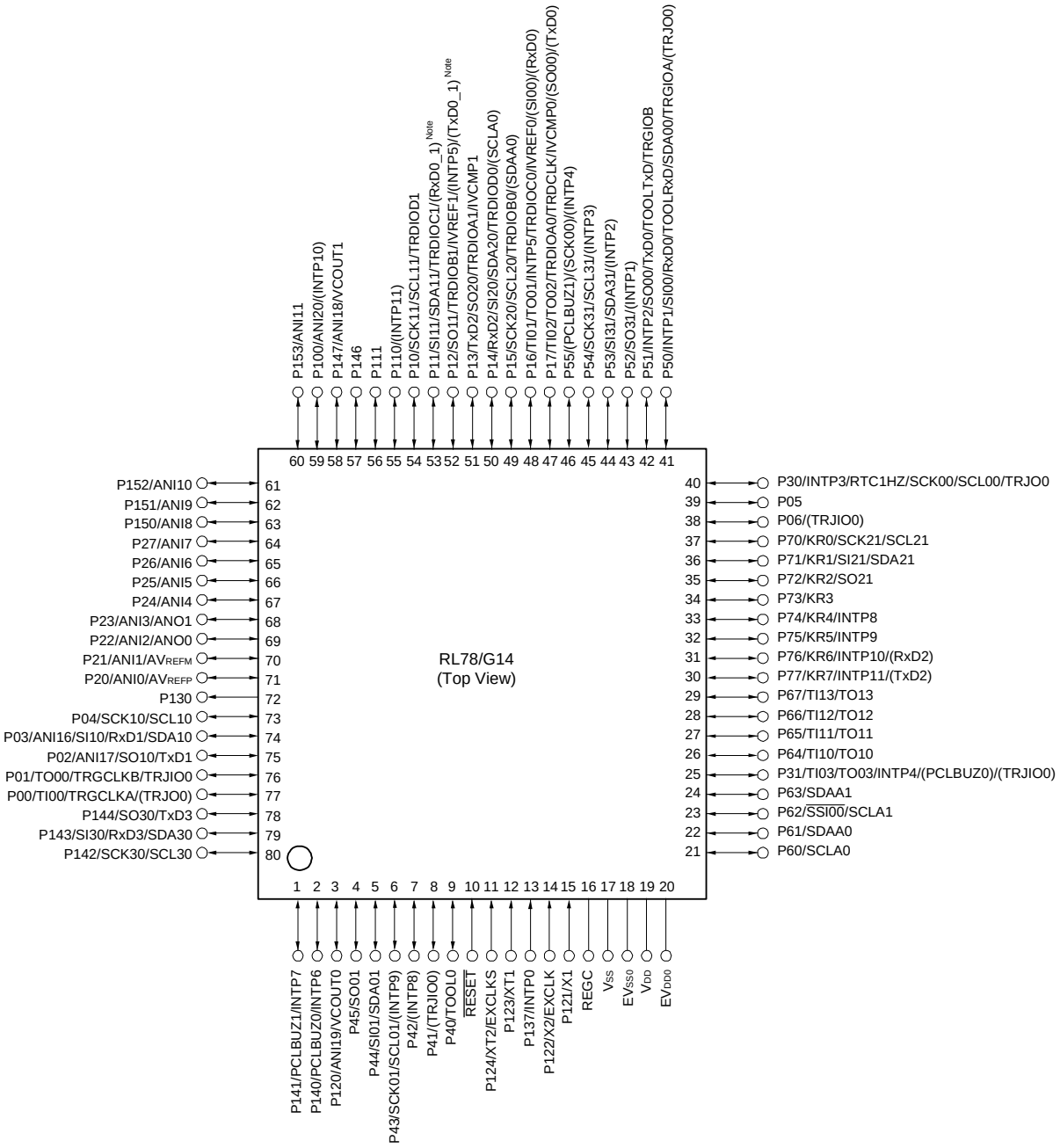
**Remark 1.** For pin identification, see **1.4 Pin Identification**.

**Remark 2.** When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the $V_{DD}$ and $EV_{DD0}$ pins and connect the $V_{SS}$ and $EV_{SS0}$ pins to separate ground lines.

**Remark 3.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).

### 1.3.9 80-pin products

- 80-pin plastic LQFP (14 × 14 mm, 0.65 mm pitch)
- 80-pin plastic LFQFP (12 × 12 mm, 0.5 mm pitch)



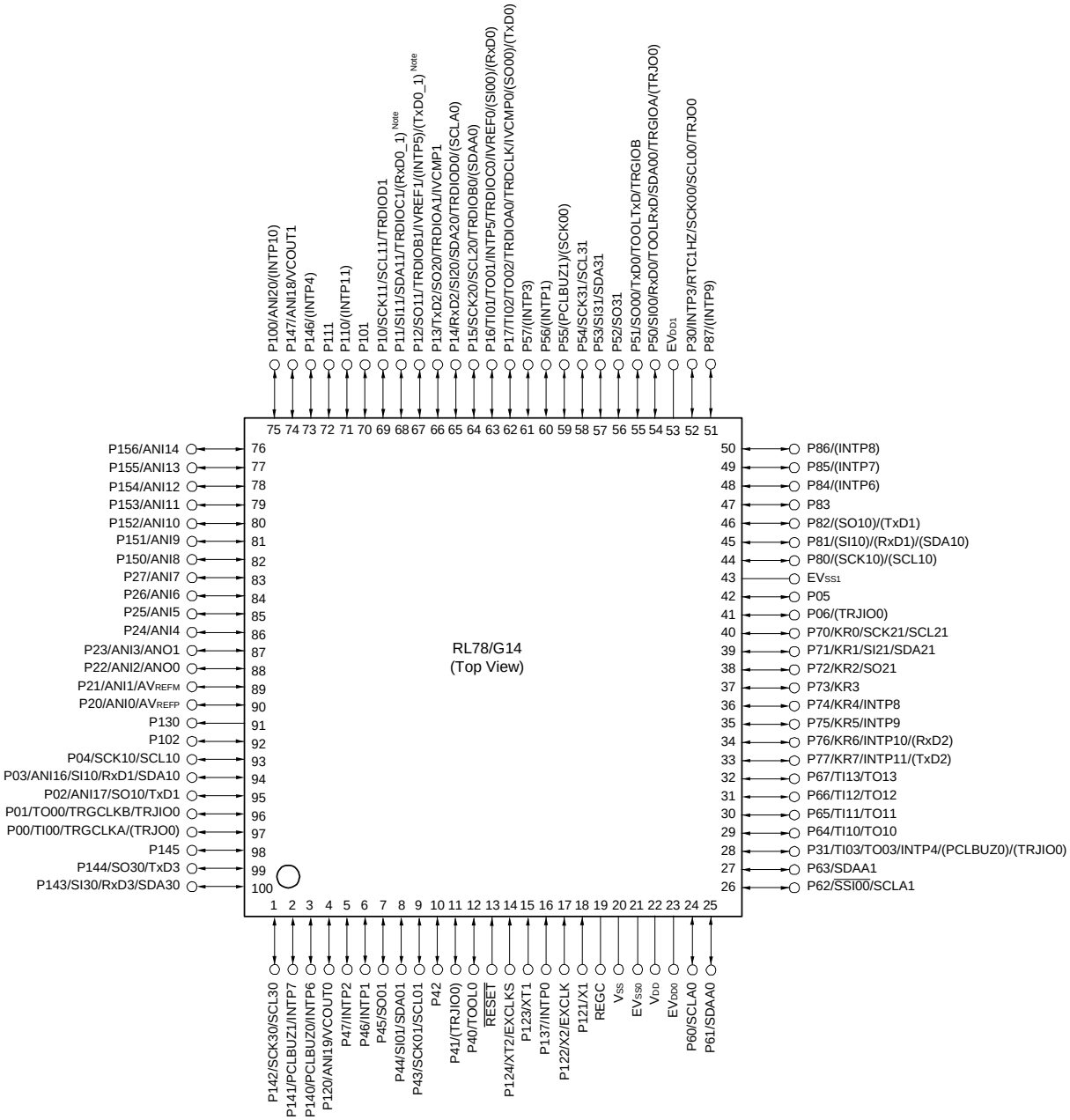

**Note** Mounted on the 384 KB or more code flash memory products.

**Caution 1. Make $EV_{SS0}$ pin the same potential as $V_{SS}$ pin.**
**Caution 2. Make $V_{DD}$ pin the potential that is higher than $EV_{DD0}$ pin.**
**Caution 3. Connect the REGC pin to $V_{SS}$ pin via a capacitor (0.47 to 1 μF).**

**Remark 1.** For pin identification, see **1.4 Pin Identification**.
**Remark 2.** When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the $V_{DD}$ and $EV_{DD0}$ pins and connect the $V_{SS}$ and $EV_{SS0}$ pins to separate ground lines.
**Remark 3.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).

## 1.3.10 100-pin products

• 100-pin plastic LFQFP (14 × 14 mm, 0.5 mm pitch)




**Note** Mounted on the 384 KB or more code flash memory products.

**Caution 1. Make EVSS0, EVSS1 pins the same potential as VSS pin.**

**Caution 2. Make VDD pin the potential that is higher than EVDD0, EVDD1 pins (EVDD0 = EVDD1).**

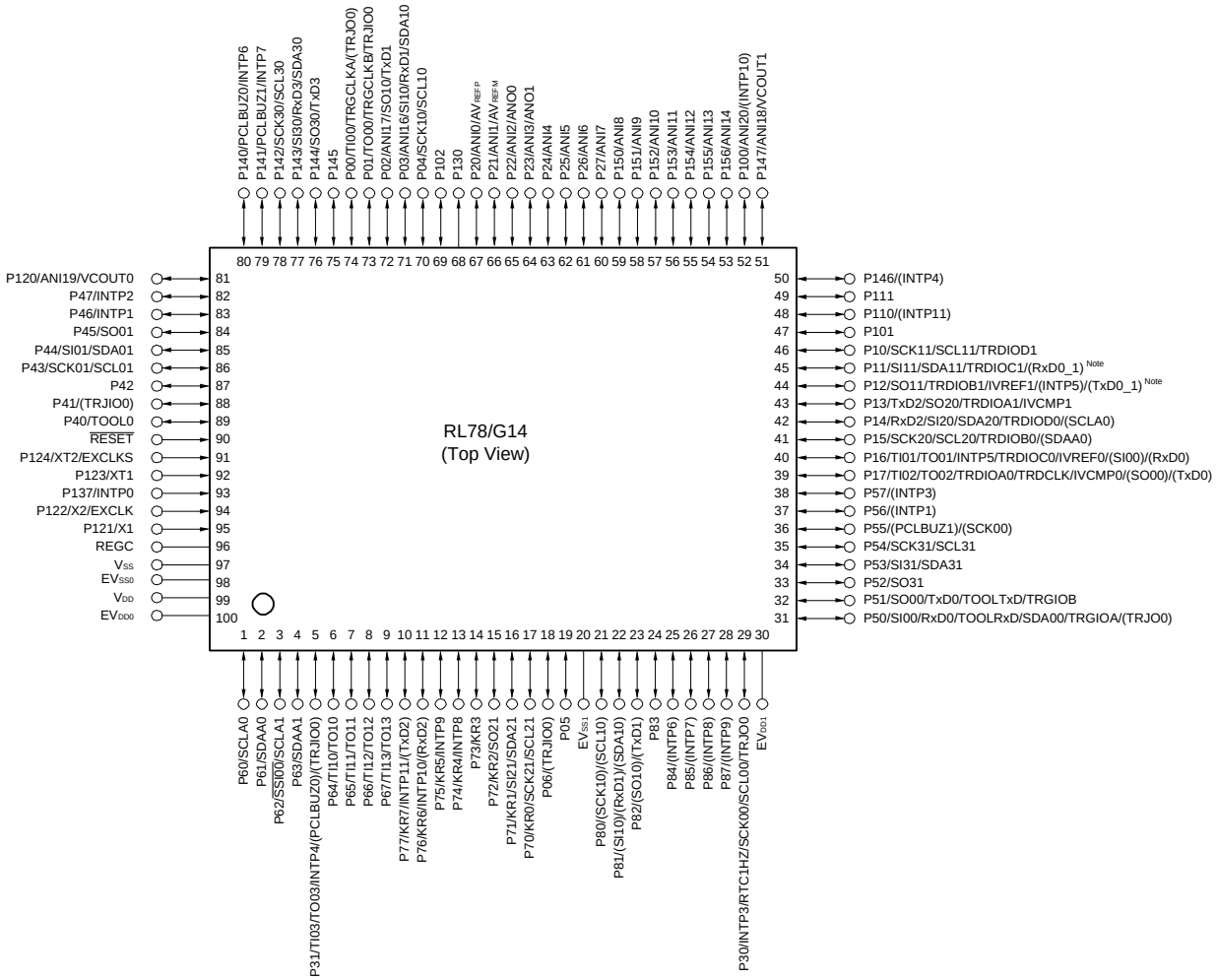
**Caution 3. Connect the REGC pin to VSS pin via a capacitor (0.47 to 1 μF).**

**Remark 1.** For pin identification, see **1.4 Pin Identification**.

**Remark 2.** When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the VDD, EVDD0 and EVDD1 pins and connect the VSS, EVSS0 and EVSS1 pins to separate ground lines.

**Remark 3.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).

• 100-pin plastic LQFP (14 × 20 mm, 0.65 mm pitch)




**Note** Mounted on the 384 KB or more code flash memory products.

**Caution 1. Make EVSS0, EVSS1 pins the same potential as VSS pin.**

**Caution 2. Make VDD pin the potential that is higher than EVDD0, EVDD1 pins (EVDD0 = EVDD1).**

**Caution 3. Connect the REGC pin to VSS pin via a capacitor (0.47 to 1 μF).**

**Remark 1.** For pin identification, see **1.4 Pin Identification**.

**Remark 2.** When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the VDD, EVDD0 and EVDD1 pins and connect the VSS, EVSS0 and EVSS1 pins to separate ground lines.

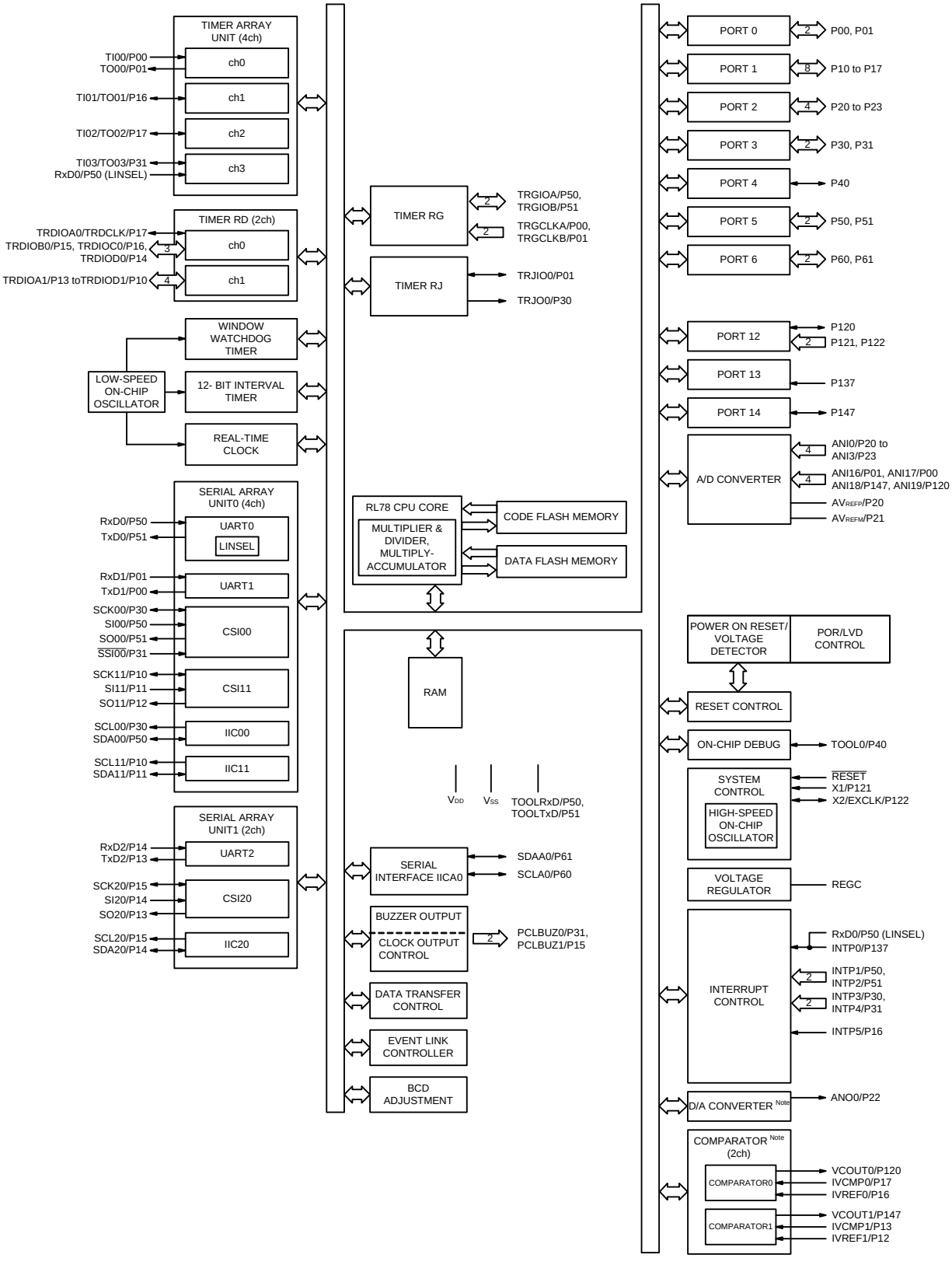
**Remark 3.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).

## 1.4 Pin Identification

| | | | |
|---|---|---|---|
| ANI0 to ANI14, | | RxD0 to RxD3: | Receive data |
| ANI16 to ANI20: | Analog output | SCK00, SCK01, SCK10, | |
| ANO0, ANO1: | Analog output | SCK11, SCK20, SCK21, | |
| $AV_{REFM}$: | A/D converter reference | SCK30, SCK31, | |
| | potential (– side) input | SCLA0, SCLA1: | Serial clock input/output |
| $AV_{REFP}$: | A/D converter reference | SCL00, SCL01, SCL10, SCL11, | |
| | potential (+ side) input | SCL20, SCL21, SCL30, | |
| $EV_{DD0}$, $EV_{DD1}$: | Power supply for port | SCL31: | Serial clock output |
| $EV_{SS0}$, $EV_{SS1}$: | Ground for port | SDAA0, SDAA1, SDA00, | |
| EXCLK: | External clock input | SDA01, SDA10, SDA11, | |
| | (main system clock) | SDA20, SDA21, SDA30, | |
| EXCLKS: | External clock input | SDA31: | Serial data input/output |
| | (subsystem clock) | SI00, SI01, SI10, SI11, | |
| INTP0 to INTP11: | External interrupt input | SI20, SI21, SI30, SI31: | Serial data input |
| IVCMP0, IVCMP1: | Comparator input | SO00, SO01, SO10, | |
| IVREF0, IVREF1: | Comparator reference input | SO11, SO20, SO21, | |
| KR0 to KR7: | Key return | SO30, SO31: | Serial data output |
| P00 to P06: | Port 0 | $\overline{SSI00}$: | Serial interface chip select input |
| P10 to P17: | Port 1 | TI00 to TI03, | |
| P20 to P27: | Port 2 | TI10 to TI13: | Timer input |
| P30, P31: | Port 3 | TO00 to TO03, | |
| P40 to P47: | Port 4 | TO10 to TO13, TRJO0: | Timer output |
| P50 to P57: | Port 5 | TOOL0: | Data input/output for tool |
| P60 to P67: | Port 6 | TOOLRxD, TOOLTxD: | Data input/output for external device |
| P70 to P77: | Port 7 | TRDCLK, TRGCLKA, | |
| P80 to P87: | Port 8 | TRGCLKB: | Timer external input clock |
| P100 to P102: | Port 10 | TRDIOA0, TRDIOB0, | |
| P110, P111: | Port 11 | TRDIOC0, TRDIOD0, | |
| P120 to P124: | Port 12 | TRDIOA1, TRDIOB1, | |
| P130, P137: | Port 13 | TRDIOC1, TRDIOD1, | |
| P140 to P147: | Port 14 | TRGIOA, TRGIOB, TRJIO0: | Timer input/output |
| P150 to P156: | Port 15 | TxD0 to TxD3: | Transmit data |
| PCLBUZ0, PCLBUZ1: | Programmable clock | VCOUT0, VCOUT1: | Comparator output |
| | output/buzzer output | $V_{DD}$: | Power supply |
| REGC: | Regulator capacitance | $V_{SS}$: | Ground |
| $\overline{RESET}$: | Reset | X1, X2: | Crystal oscillator (main system clock) |
| RTC1HZ: | Real-time clock correction clock (1 Hz) output | XT1, XT2: | Crystal oscillator (subsystem clock) |

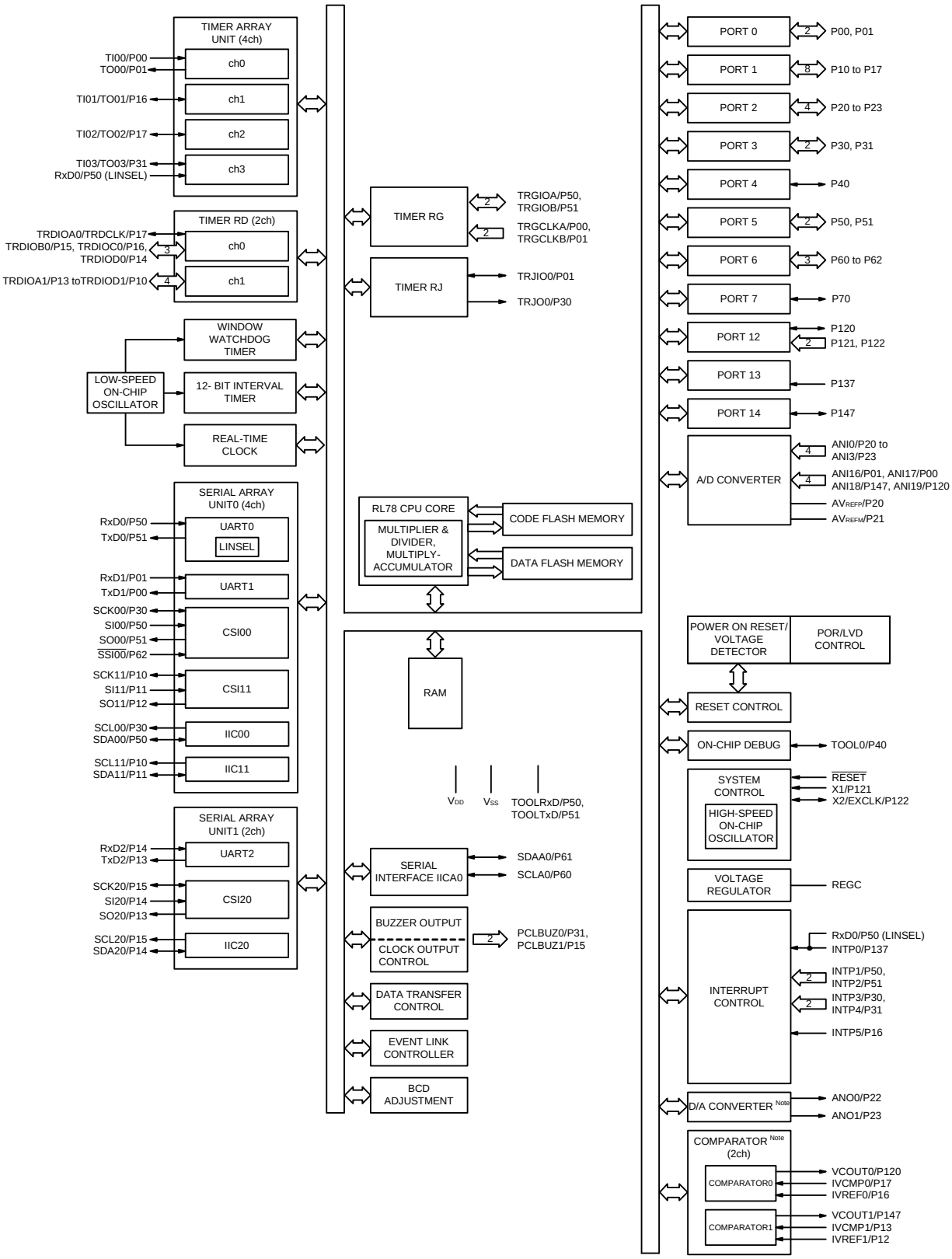
## 1.5 Block Diagram

### 1.5.1 30-pin products



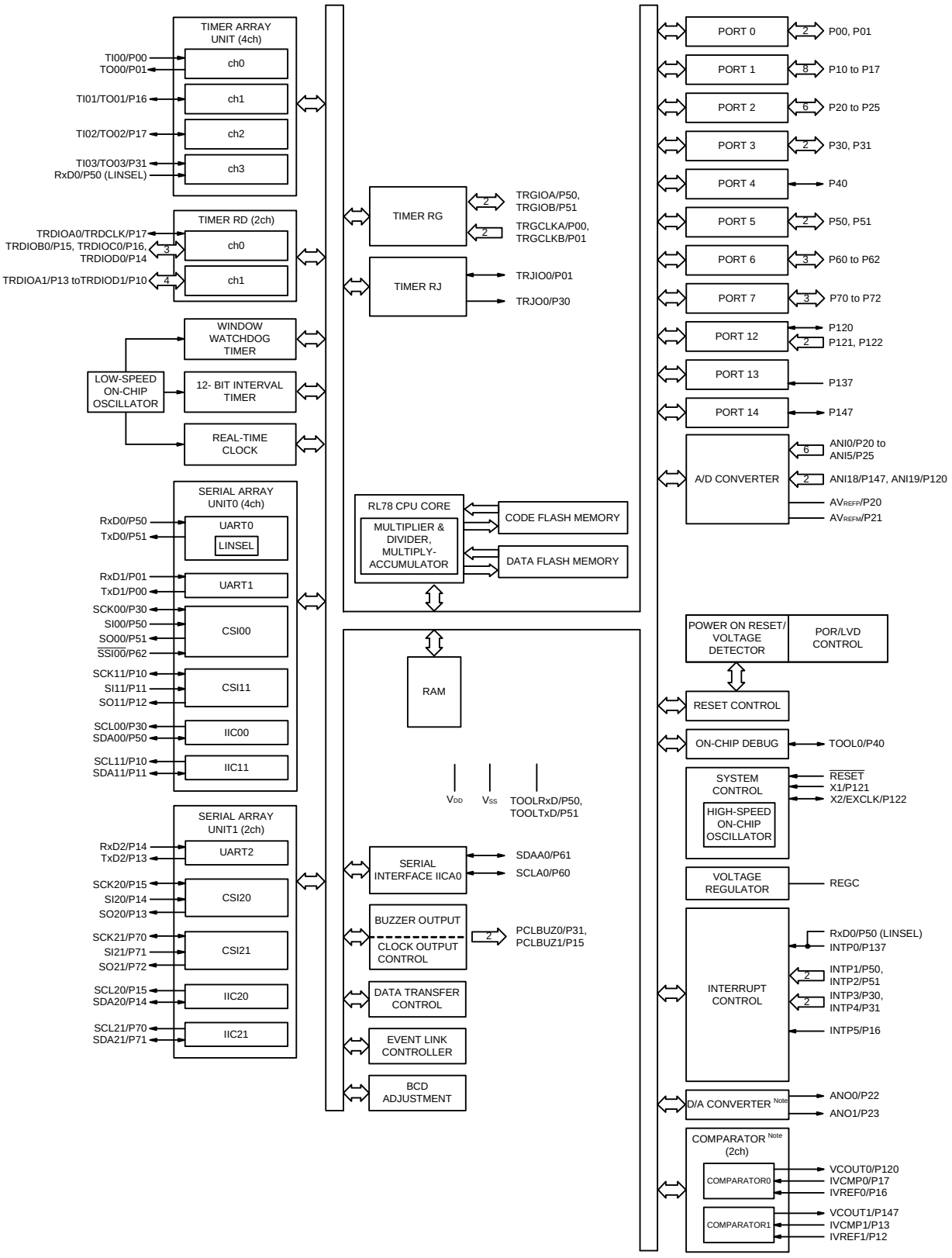

**Note** Mounted on the 96 KB or more code flash memory products.

## 1.5.2 32-pin products



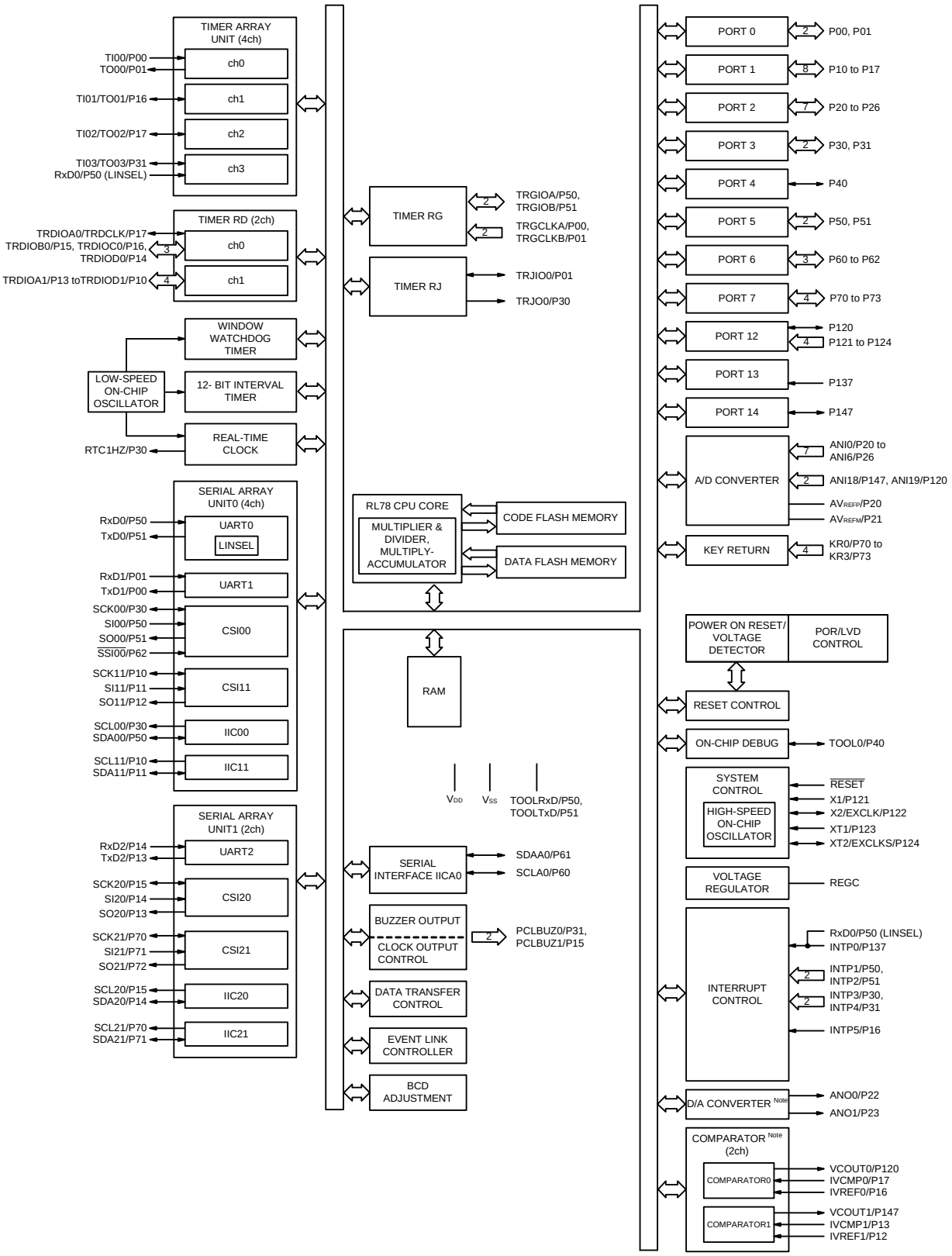

**Note** Mounted on the 96 KB or more code flash memory products.

## 1.5.3 36-pin products



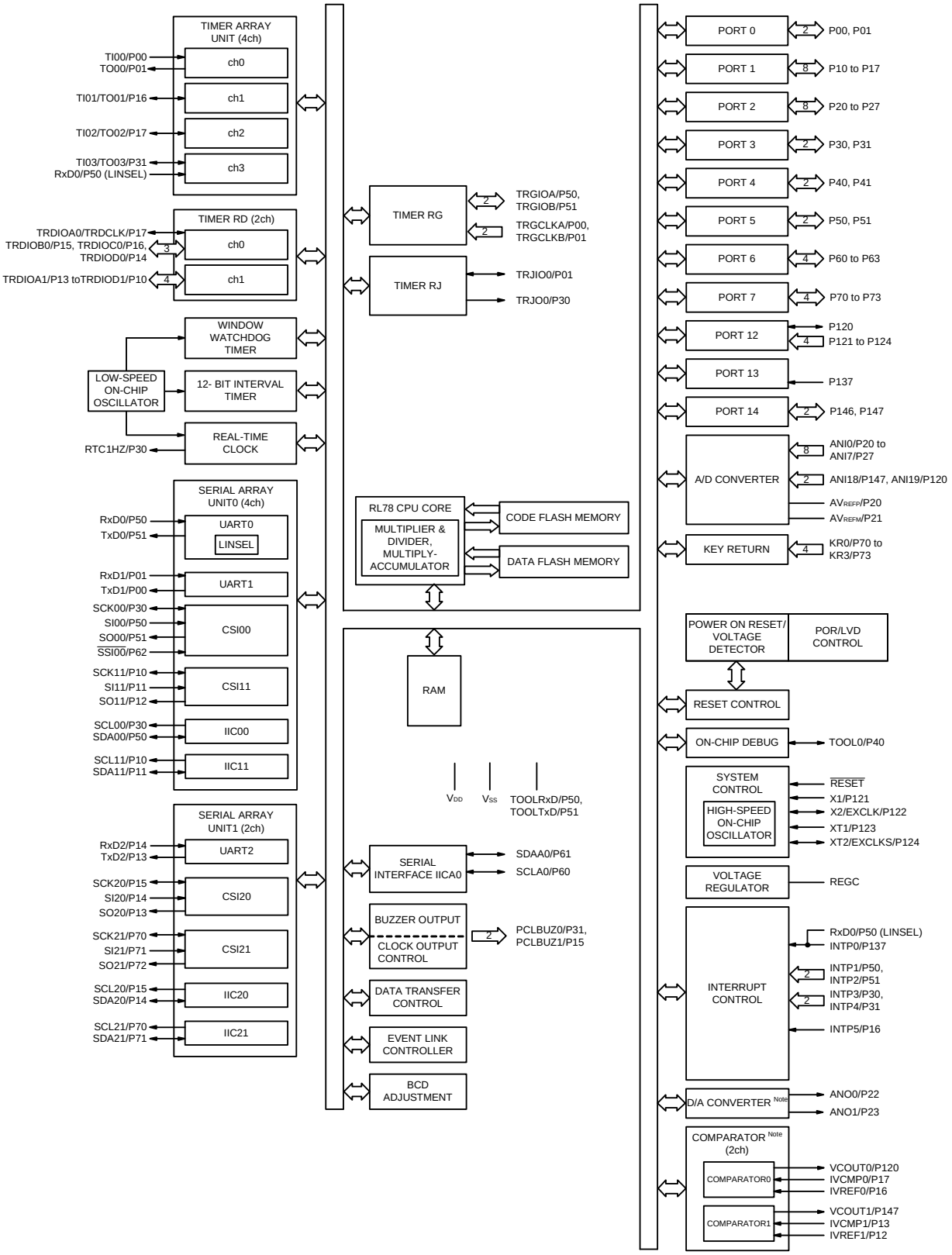

**Note** Mounted on the 96 KB or more code flash memory products.

## 1.5.4 40-pin products



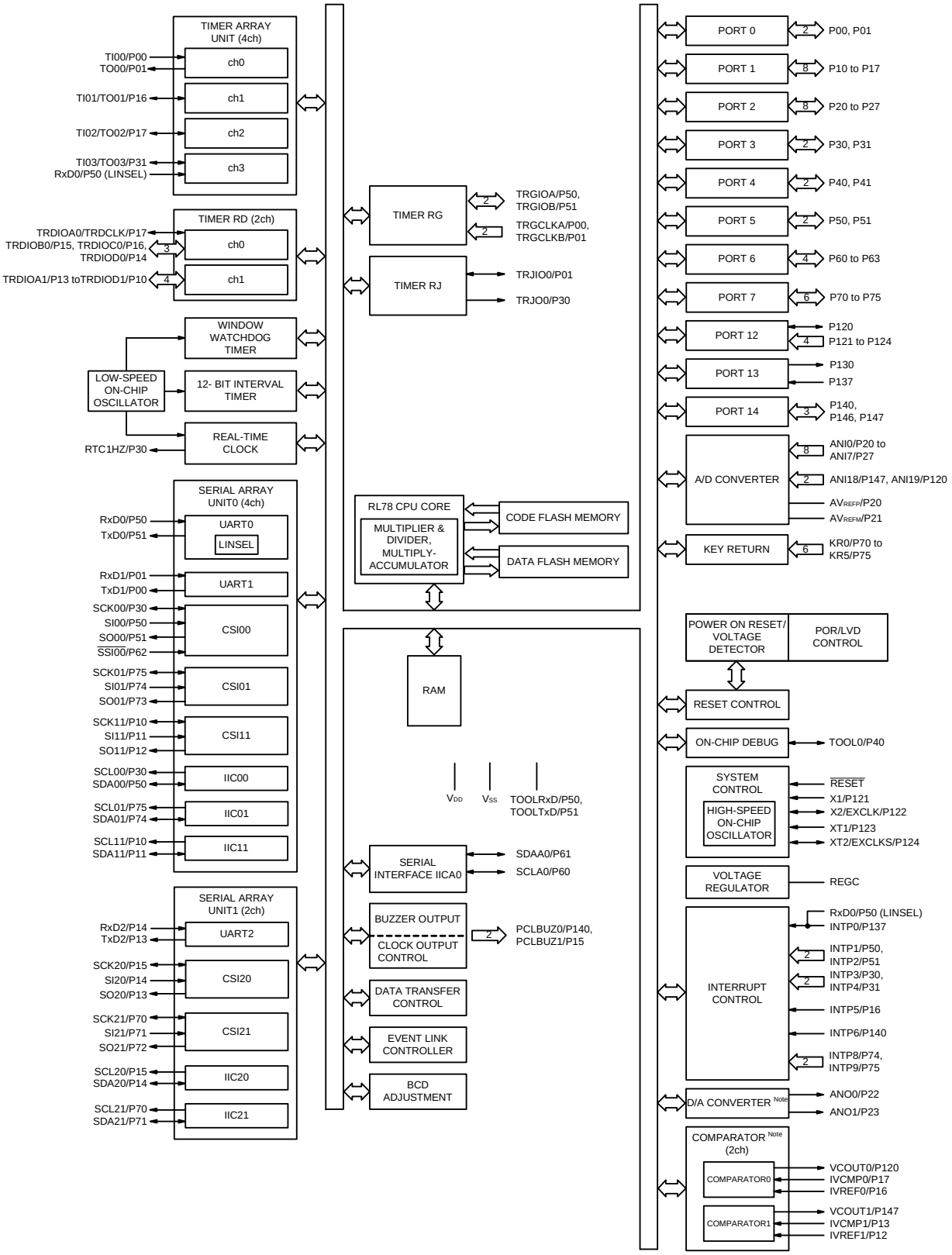

**Note** Mounted on the 96 KB or more code flash memory products.

## 1.5.5 44-pin products



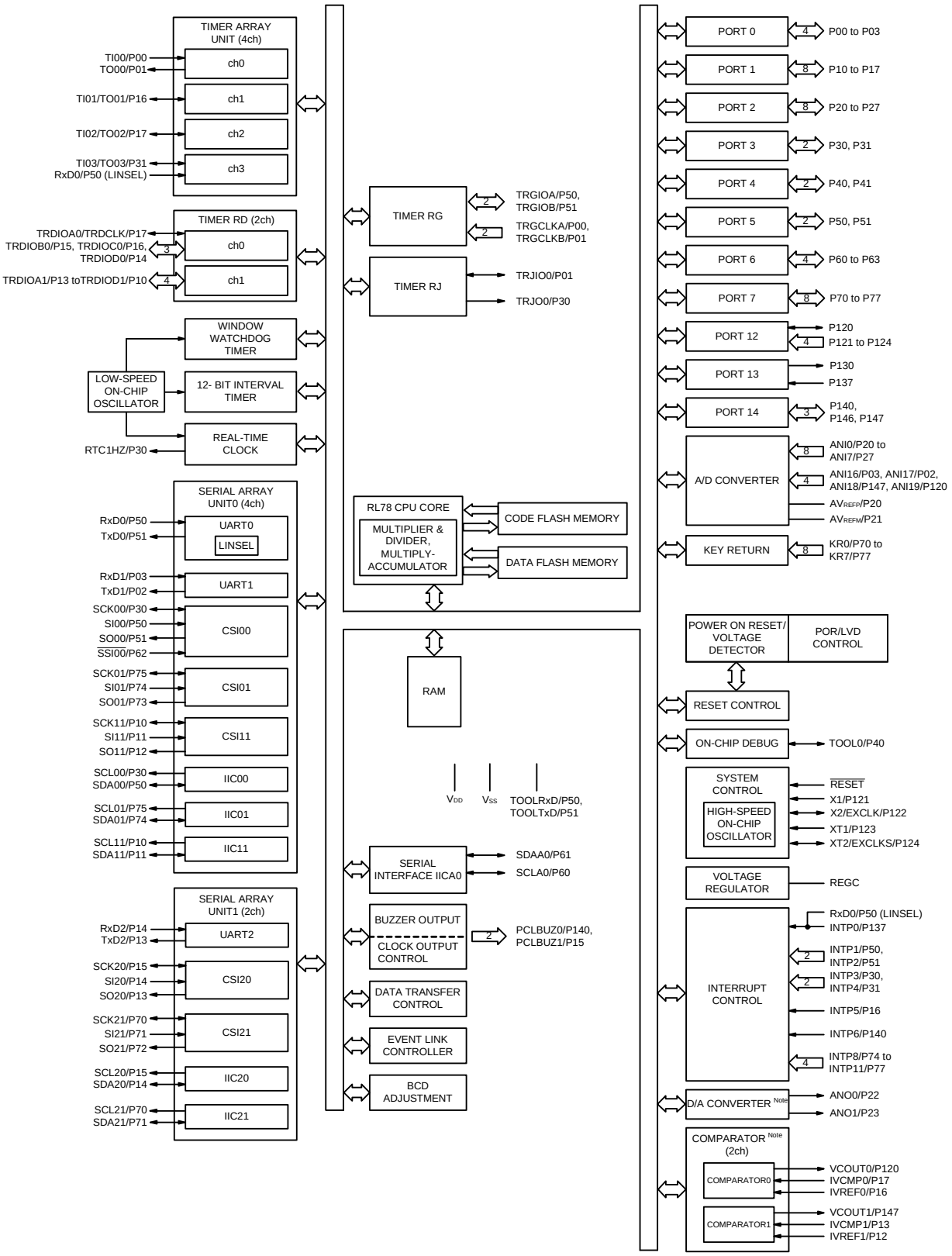

**Note** Mounted on the 96 KB or more code flash memory products.

## 1.5.6 48-pin products



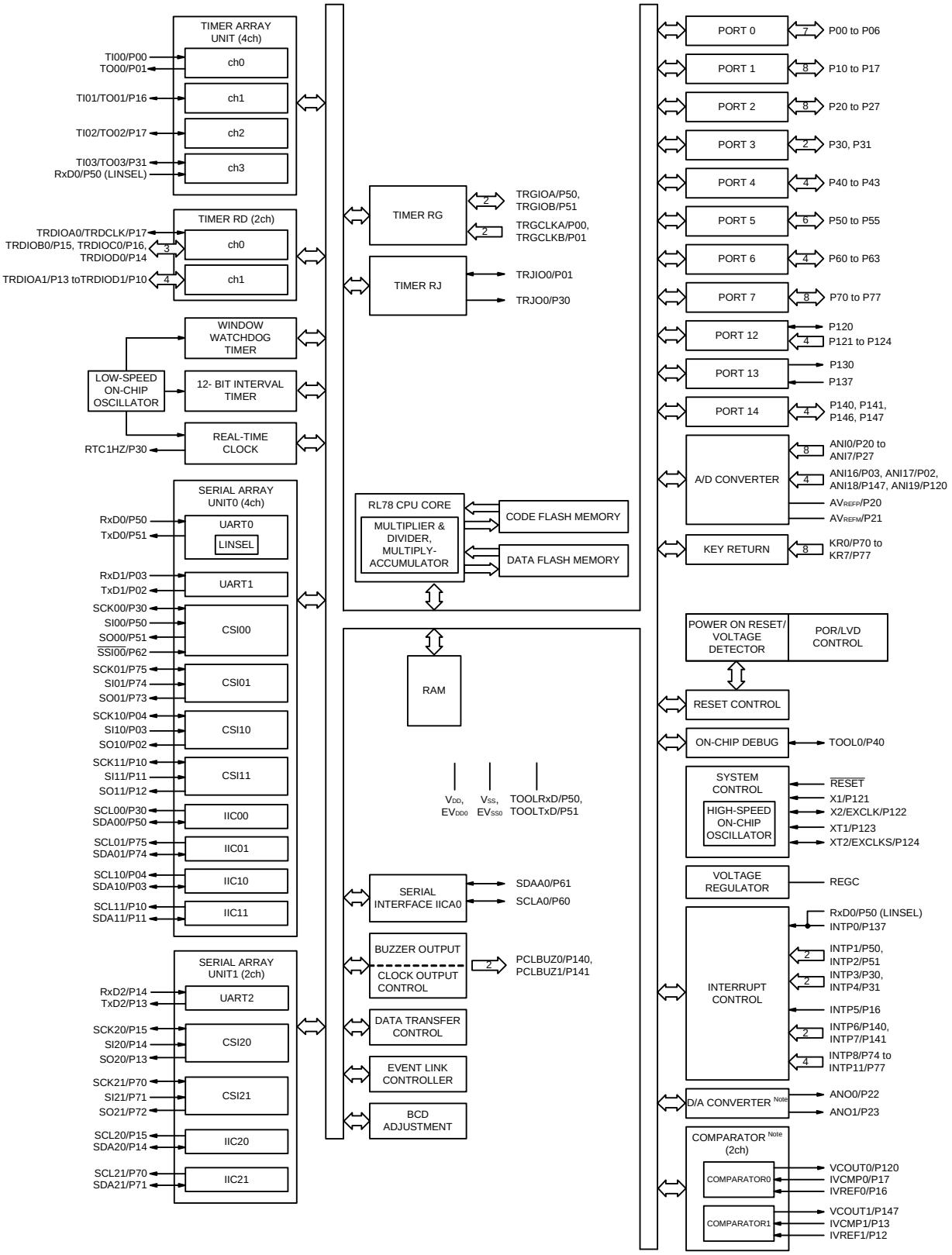

**Note** Mounted on the 96 KB or more code flash memory products.

## 1.5.7 52-pin products



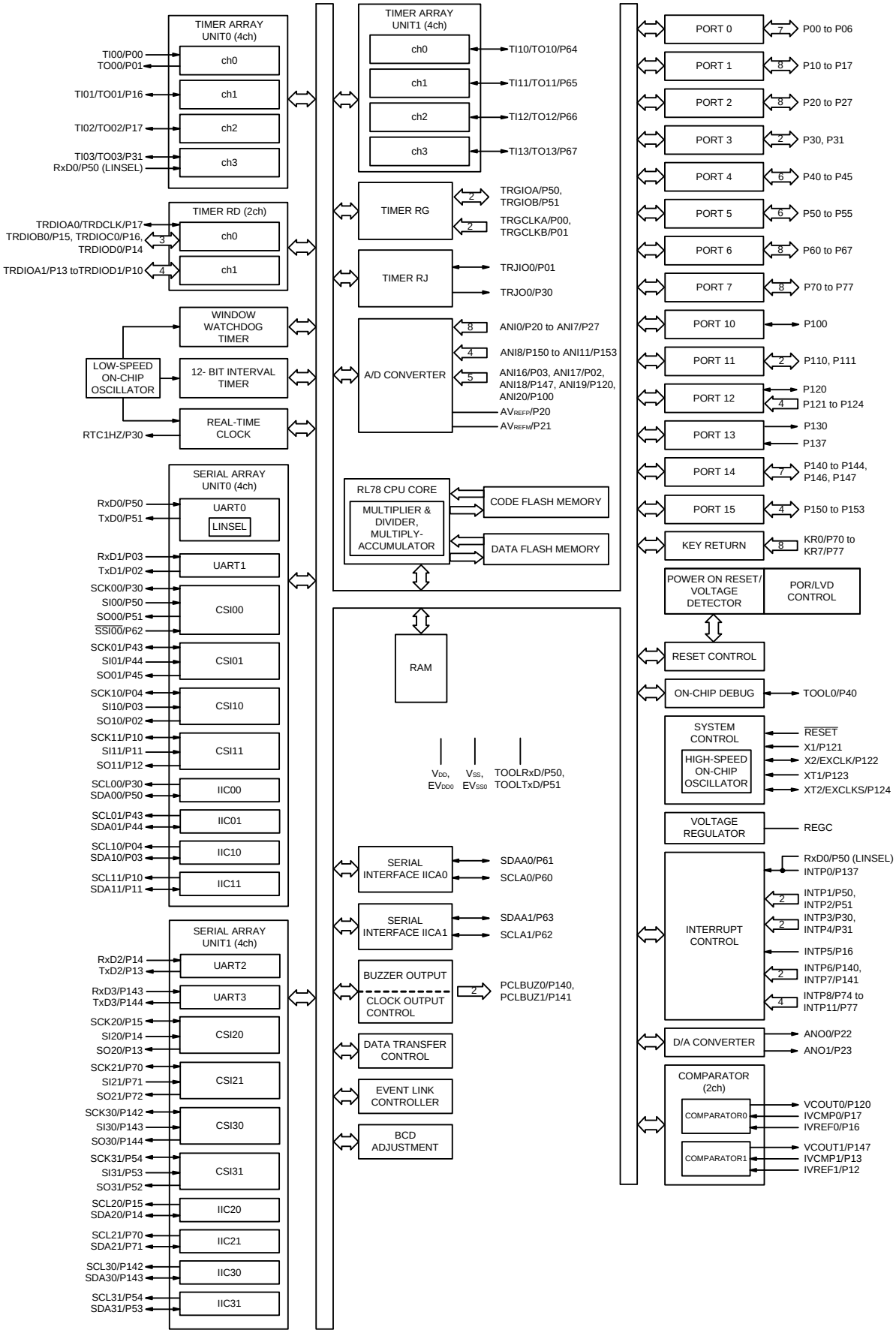

**Note** Mounted on the 96 KB or more code flash memory products.

## 1.5.8 64-pin products

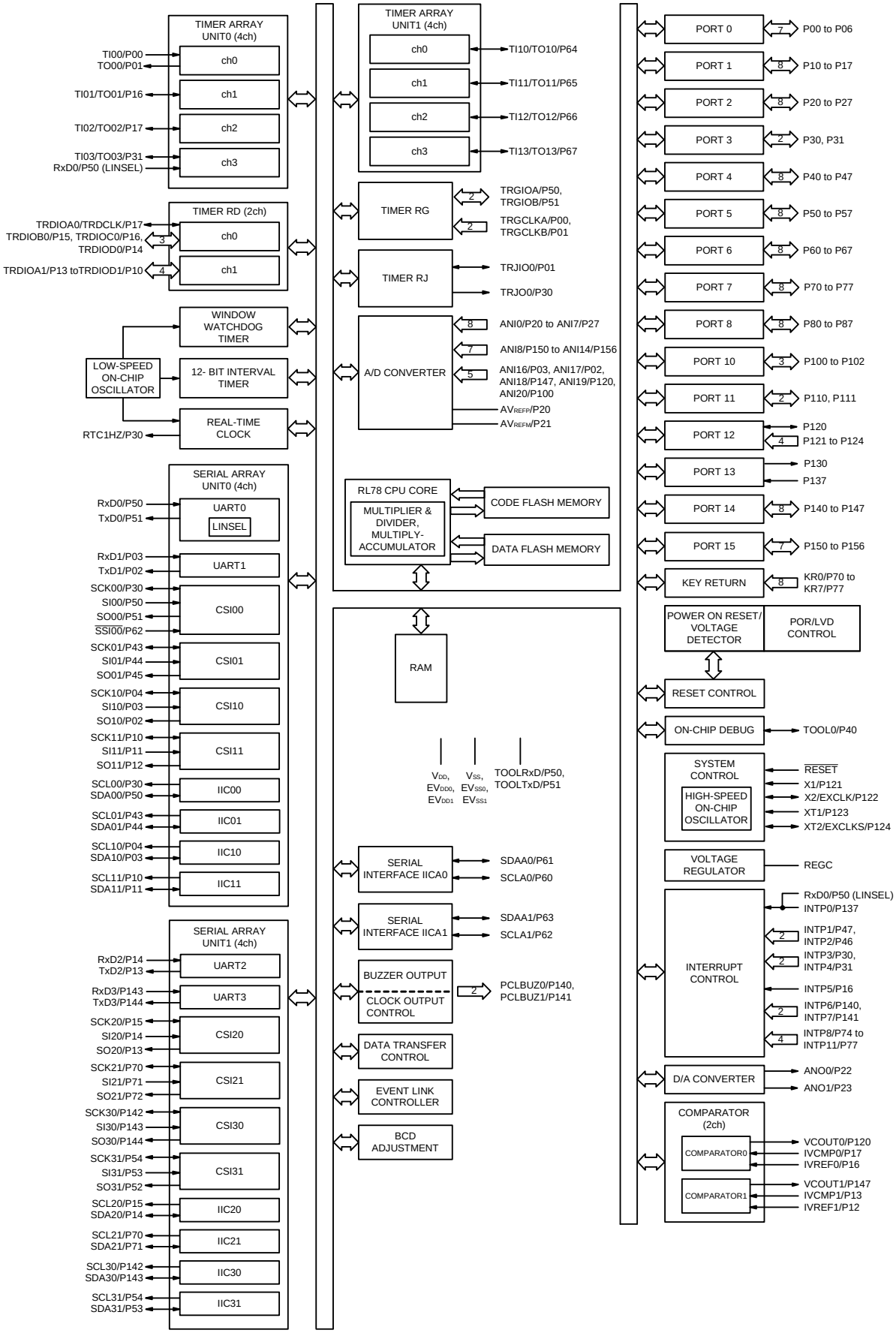



**Note** Mounted on the 96 KB or more code flash memory products.

## 1.5.9 80-pin products



## 1.5.10 100-pin products



## 1.6 Outline of Functions

[30-pin, 32-pin, 36-pin, 40-pin products (code flash memory 16 KB to 64 KB)]

**Caution This outline describes the functions at the time when Peripheral I/O redirection register 0, 1 (PIOR0, 1) are set to 00H.**

(1/2)

| Item | | 30-pin | 32-pin | 36-pin | 40-pin |
|---|---|---|---|---|---|
| | | R5F104Ax (x = A, C to E) | R5F104Bx (x = A, C to E) | R5F104Cx (x = A, C to E) | R5F104Ex (x = A, C to E) |
| Code flash memory (KB) | | 16 to 64 | 16 to 64 | 16 to 64 | 16 to 64 |
| Data flash memory (KB) | | 4 | 4 | 4 | 4 |
| RAM (KB) | | 2.5 to 5.5 Note | 2.5 to 5.5 Note | 2.5 to 5.5 Note | 2.5 to 5.5 Note |
| Address space | | 1 MB | | | |
| Main system clock | High-speed system clock | X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK)<br>HS (high-speed main) mode: 1 to 20 MHz ($V_{DD}$ = 2.7 to 5.5 V),<br>HS (high-speed main) mode: 1 to 16 MHz ($V_{DD}$ = 2.4 to 5.5 V),<br>LS (low-speed main) mode: 1 to 8 MHz ($V_{DD}$ = 1.8 to 5.5 V),<br>LV (low-voltage main) mode: 1 to 4 MHz ($V_{DD}$ = 1.6 to 5.5 V) | | | |
| | High-speed on-chip oscillator clock ($f_{IH}$) | HS (high-speed main) mode: 1 to 32 MHz ($V_{DD}$ = 2.7 to 5.5 V),<br>HS (high-speed main) mode: 1 to 16 MHz ($V_{DD}$ = 2.4 to 5.5 V),<br>LS (low-speed main) mode: 1 to 8 MHz ($V_{DD}$ = 1.8 to 5.5 V),<br>LV (low-voltage main) mode: 1 to 4 MHz ($V_{DD}$ = 1.6 to 5.5 V) | | | |
| Subsystem clock | | — | | | XT1 (crystal) oscillation, external subsystem clock input (EXCLKS) 32.768 kHz |
| Low-speed on-chip oscillator clock | | 15 kHz (TYP.): $V_{DD}$ = 1.6 to 5.5 V | | | |
| General-purpose register | | 8 bits × 32 registers (8 bits × 8 registers × 4 banks) | | | |
| Minimum instruction execution time | | 0.03125 μs (High-speed on-chip oscillator clock: $f_{IH}$ = 32 MHz operation) | | | |
| | | 0.05 μs (High-speed system clock: $f_{MX}$ = 20 MHz operation) | | | |
| | | — | | | 30.5 μs (Subsystem clock: $f_{SUB}$ = 32.768 kHz operation) |
| Instruction set | | • Data transfer (8/16 bits)<br>• Adder and subtractor/logical operation (8/16 bits)<br>• Multiplication (8 bits × 8 bits, 16 bits × 16 bits), Division (16 bits ÷ 16 bits, 32 bits ÷ 32 bits)<br>• Multiplication and Accumulation (16 bits × 16 bits + 32 bits)<br>• Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc. | | | |
| I/O port | Total | 26 | 28 | 32 | 36 |
| | CMOS I/O | 21 | 22 | 26 | 28 |
| | CMOS input | 3 | 3 | 3 | 5 |
| | CMOS output | — | — | — | — |
| | N-ch open-drain I/O (6 V tolerance) | 2 | 3 | 3 | 3 |
| Timer | 16-bit timer | 8 channels<br>(TAU: 4 channels, Timer RJ: 1 channel, Timer RD: 2 channels, Timer RG: 1 channel) | | | |
| | Watchdog timer | 1 channel | | | |
| | Real-time clock (RTC) | 1 channel | | | |
| | 12-bit interval timer | 1 channel | | | |
| | Timer output | Timer outputs: 13 channels<br>PWM outputs: 9 channels | | | |
| | RTC output | — | | | 1<br>• 1 Hz (subsystem clock: $f_{SUB}$ = 32.768 kHz) |

(**Note** is listed on the next page.)

**Note** The flash library uses RAM in self-programming and rewriting of the data flash memory.
The target products and start address of the RAM areas used by the flash library are shown below.
R5F104xD (x = A to C, E to G, J, L): Start address FE900H
R5F104xE (x = A to C, E to G, J, L): Start address FE900H
For the RAM areas used by the flash library, see **Self RAM list of Flash Self-Programming Library for RL78 Family (R20UT2944)**.

(2/2)

| Item | | 30-pin | 32-pin | 36-pin | 40-pin |
|---|---|---|---|---|---|
| | | R5F104Ax (x = A, C to E) | R5F104Bx (x = A, C to E) | R5F104Cx (x = A, C to E) | R5F104Ex (x = A, C to E) |
| Clock output/buzzer output | | 2 | 2 | 2 | 2 |
| | | [30-pin, 32-pin, 36-pin products]<br>• 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: $f_{MAIN}$ = 20 MHz operation)<br>[40-pin products]<br>• 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: $f_{MAIN}$ = 20 MHz operation)<br>• 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (Subsystem clock: $f_{SUB}$ = 32.768 kHz operation) | | | |
| 8/10-bit resolution A/D converter | | 8 channels | 8 channels | 8 channels | 9 channels |
| Serial interface | | [30-pin, 32-pin products]<br>• CSI: 1 channel/UART (UART supporting LIN-bus): 1 channel/simplified $I^2C$: 1 channel<br>• CSI: 1 channel/UART: 1 channel/simplified $I^2C$: 1 channel<br>• CSI: 1 channel/UART: 1 channel/simplified $I^2C$: 1 channel<br>[36-pin, 40-pin products]<br>• CSI: 1 channel/UART (UART supporting LIN-bus): 1 channel/simplified $I^2C$: 1 channel<br>• CSI: 1 channel/UART: 1 channel/simplified $I^2C$: 1 channel<br>• CSI: 2 channels/UART: 1 channel/simplified $I^2C$: 2 channels | | | |
| | $I^2C$ bus | 1 channel | 1 channel | 1 channel | 1 channel |
| Data transfer controller (DTC) | | 28 sources | | | 29 sources |
| Event link controller (ELC) | | Event input: 19<br>Event trigger output: 7 | | | Event input: 20<br>Event trigger output: 7 |
| Vectored interrupt sources | Internal | 24 | 24 | 24 | 24 |
| | External | 6 | 6 | 6 | 7 |
| Key interrupt | | — | — | — | 4 |
| Reset | | • Reset by $\overline{\text{RESET}}$ pin<br>• Internal reset by watchdog timer<br>• Internal reset by power-on-reset<br>• Internal reset by voltage detector<br>• Internal reset by illegal instruction execution Note<br>• Internal reset by RAM parity error<br>• Internal reset by illegal-memory access | | | |
| Power-on-reset circuit | | • Power-on-reset: 1.51 ±0.04 V ($T_A$ = –40 to +85°C)<br>1.51 ±0.06 V ($T_A$ = –40 to +105°C)<br>• Power-down-reset: 1.50 ±0.04 V ($T_A$ = –40 to +85°C)<br>1.50 ±0.06 V ($T_A$ = –40 to +105°C) | | | |
| Voltage detector | | 1.63 V to 4.06 V (14 stages) | | | |
| On-chip debug function | | Provided | | | |
| Power supply voltage | | $V_{DD}$ = 1.6 to 5.5 V ($T_A$ = –40 to +85°C)<br>$V_{DD}$ = 2.4 to 5.5 V ($T_A$ = –40 to +105°C) | | | |
| Operating ambient temperature | | $T_A$ = –40 to +85°C (A: Consumer applications, D: Industrial applications),<br>$T_A$ = -40 to +105°C (G: Industrial applications) | | | |

**Note** The illegal instruction is generated when instruction code FFH is executed.
Reset by the illegal instruction execution not is issued by emulation with the in-circuit emulator or on-chip debug emulator.

[30-pin, 32-pin, 36-pin, 40-pin products (code flash memory 96 KB to 256 KB)]

**Caution This outline describes the functions at the time when Peripheral I/O redirection register 0, 1 (PIOR0, 1) are set to 00H.**

(1/2)

| Item | | 30-pin | 32-pin | 36-pin | 40-pin |
|---|---|---|---|---|---|
| | | R5F104Ax (x = F, G) | R5F104Bx (x = F, G) | R5F104Cx (x = F, G) | R5F104Ex (x = F to H) |
| Code flash memory (KB) | | 96 to 128 | 96 to 128 | 96 to 128 | 96 to 192 |
| Data flash memory (KB) | | 8 | 8 | 8 | 8 |
| RAM (KB) | | 12 to 16 Note | 12 to 16 Note | 12 to 16 Note | 12 to 20 Note |
| Address space | | 1 MB | | | |
| Main system clock | High-speed system clock | X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK)<br>HS (high-speed main) mode: 1 to 20 MHz ($V_{DD}$ = 2.7 to 5.5 V),<br>HS (high-speed main) mode: 1 to 16 MHz ($V_{DD}$ = 2.4 to 5.5 V),<br>LS (low-speed main) mode: 1 to 8 MHz ($V_{DD}$ = 1.8 to 5.5 V),<br>LV (low-voltage main) mode: 1 to 4 MHz ($V_{DD}$ = 1.6 to 5.5 V) | | | |
| | High-speed on-chip oscillator clock ($f_{IH}$) | HS (high-speed main) mode: 1 to 32 MHz ($V_{DD}$ = 2.7 to 5.5 V),<br>HS (high-speed main) mode: 1 to 16 MHz ($V_{DD}$ = 2.4 to 5.5 V),<br>LS (low-speed main) mode: 1 to 8 MHz ($V_{DD}$ = 1.8 to 5.5 V),<br>LV (low-voltage main) mode: 1 to 4 MHz ($V_{DD}$ = 1.6 to 5.5 V) | | | |
| Subsystem clock | | — | | | XT1 (crystal) oscillation, external subsystem clock input (EXCLKS) 32.768 kHz |
| Low-speed on-chip oscillator clock | | 15 kHz (TYP.): $V_{DD}$ = 1.6 to 5.5 V | | | |
| General-purpose register | | 8 bits × 32 registers (8 bits × 8 registers × 4 banks) | | | |
| Minimum instruction execution time | | 0.03125 μs (High-speed on-chip oscillator clock: $f_{IH}$ = 32 MHz operation) | | | |
| | | 0.05 μs (High-speed system clock: $f_{MX}$ = 20 MHz operation) | | | |
| | | — | | | 30.5 μs (Subsystem clock: $f_{SUB}$ = 32.768 kHz operation) |
| Instruction set | | • Data transfer (8/16 bits)<br>• Adder and subtractor/logical operation (8/16 bits)<br>• Multiplication (8 bits × 8 bits, 16 bits × 16 bits), Division (16 bits ÷ 16 bits, 32 bits ÷ 32 bits)<br>• Multiplication and Accumulation (16 bits × 16 bits + 32 bits)<br>• Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc. | | | |
| I/O port | Total | 26 | 28 | 32 | 36 |
| | CMOS I/O | 21 | 22 | 26 | 28 |
| | CMOS input | 3 | 3 | 3 | 5 |
| | CMOS output | — | — | — | — |
| | N-ch open-drain I/O (6 V tolerance) | 2 | 3 | 3 | 3 |
| Timer | 16-bit timer | 8 channels<br>(TAU: 4 channels, Timer RJ: 1 channel, Timer RD: 2 channels, Timer RG: 1 channel) | | | |
| | Watchdog timer | 1 channel | | | |
| | Real-time clock (RTC) | 1 channel | | | |
| | 12-bit interval timer | 1 channel | | | |
| | Timer output | Timer outputs: 13 channels<br>PWM outputs: 9 channels | | | |
| | RTC output | — | | | 1<br>• 1 Hz (subsystem clock: $f_{SUB}$ = 32.768 kHz) |

(**Note** is listed on the next page.)

**Note** The flash library uses RAM in self-programming and rewriting of the data flash memory.
The target products and start address of the RAM areas used by the flash library are shown below.
R5F104xJ (x = F, G, J, L, M, P): Start address F9F00H
For the RAM areas used by the flash library, see **Self RAM list of Flash Self-Programming Library for RL78 Family (R20UT2944)**.

(2/2)

| Item | | 30-pin<br>R5F104Ax<br>(x = F, G) | 32-pin<br>R5F104Bx<br>(x = F, G) | 36-pin<br>R5F104Cx<br>(x = F, G) | 40-pin<br>R5F104Ex<br>(x = F to H) |
|---|---|---|---|---|---|
| Clock output/buzzer output | | 2 | 2 | 2 | 2 |
| | | [30-pin, 32-pin, 36-pin products]<br>• 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: $f_{MAIN}$ = 20 MHz operation)<br>[40-pin products]<br>• 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: $f_{MAIN}$ = 20 MHz operation)<br>• 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (Subsystem clock: $f_{SUB}$ = 32.768 kHz operation) | | | |
| 8/10-bit resolution A/D converter | | 8 channels | 8 channels | 8 channels | 9 channels |
| D/A converter | | 1 channel | 2 channels | | |
| Comparator | | 2 channels | | | |
| Serial interface | | [30-pin, 32-pin products]<br>• CSI: 1 channel/UART (UART supporting LIN-bus): 1 channel/simplified $I^2C$: 1 channel<br>• CSI: 1 channel/UART: 1 channel/simplified $I^2C$: 1 channel<br>• CSI: 1 channel/UART: 1 channel/simplified $I^2C$: 1 channel<br>[36-pin, 40-pin products]<br>• CSI: 1 channel/UART (UART supporting LIN-bus): 1 channel/simplified $I^2C$: 1 channel<br>• CSI: 1 channel/UART: 1 channel/simplified $I^2C$: 1 channel<br>• CSI: 2 channels/UART: 1 channel/simplified $I^2C$: 2 channels | | | |
| | $I^2C$ bus | 1 channel | 1 channel | 1 channel | 1 channel |
| Data transfer controller (DTC) | | 30 sources | | | 31 sources |
| Event link controller (ELC) | | Event input: 21<br>Event trigger output: 8 | Event input: 21, Event trigger output: 9 | | Event input: 22<br>Event trigger output: 9 |
| Vectored interrupt sources | Internal | 24 | 24 | 24 | 24 |
| | External | 6 | 6 | 6 | 7 |
| Key interrupt | | — | — | — | 4 |
| Reset | | • Reset by $\overline{\text{RESET}}$ pin<br>• Internal reset by watchdog timer<br>• Internal reset by power-on-reset<br>• Internal reset by voltage detector<br>• Internal reset by illegal instruction execution Note<br>• Internal reset by RAM parity error<br>• Internal reset by illegal-memory access | | | |
| Power-on-reset circuit | | • Power-on-reset: 1.51 ±0.04 V ($T_A$ = –40 to +85°C)<br>1.51 ±0.06 V ($T_A$ = –40 to +105°C)<br>• Power-down-reset: 1.50 ±0.04 V ($T_A$ = –40 to +85°C)<br>1.50 ±0.06 V ($T_A$ = –40 to +105°C) | | | |
| Voltage detector | | 1.63 V to 4.06 V (14 stages) | | | |
| On-chip debug function | | Provided | | | |
| Power supply voltage | | $V_{DD}$ = 1.6 to 5.5 V ($T_A$ = –40 to +85°C)<br>$V_{DD}$ = 2.4 to 5.5 V ($T_A$ = –40 to +105°C) | | | |
| Operating ambient temperature | | $T_A$ = –40 to +85°C (A: Consumer applications, D: Industrial applications),<br>$T_A$ = -40 to +105°C (G: Industrial applications) | | | |

**Note** The illegal instruction is generated when instruction code FFH is executed.
Reset by the illegal instruction execution not is issued by emulation with the in-circuit emulator or on-chip debug emulator.

[44-pin, 48-pin, 52-pin, 64-pin products (code flash memory 16 KB to 64 KB)]

**Caution This outline describes the functions at the time when Peripheral I/O redirection register 0, 1 (PIOR0, 1) are set to 00H.**

(1/2)

| Item | | 44-pin<br>R5F104Fx<br>(x = A, C to E) | 48-pin<br>R5F104Gx<br>(x = A, C to E) | 52-pin<br>R5F104Jx<br>(x = C to E) | 64-pin<br>R5F104Lx<br>(x = C to E) |
|---|---|---|---|---|---|
| Code flash memory (KB) | | 16 to 64 | 16 to 64 | 32 to 64 | 32 to 64 |
| Data flash memory (KB) | | 4 | 4 | 4 | 4 |
| RAM (KB) | | 2.5 to 5.5 Note | 2.5 to 5.5 Note | 4 to 5.5 Note | 4 to 5.5 Note |
| Address space | | 1 MB | | | |
| Main system clock | High-speed system clock | X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK)<br>HS (high-speed main) mode: 1 to 20 MHz ($V_{DD}$ = 2.7 to 5.5 V),<br>HS (high-speed main) mode: 1 to 16 MHz ($V_{DD}$ = 2.4 to 5.5 V),<br>LS (low-speed main) mode: 1 to 8 MHz ($V_{DD}$ = 1.8 to 5.5 V),<br>LV (low-voltage main) mode: 1 to 4 MHz ($V_{DD}$ = 1.6 to 5.5 V) | | | |
| | High-speed on-chip oscillator clock ($f_{IH}$) | HS (high-speed main) mode: 1 to 32 MHz ($V_{DD}$ = 2.7 to 5.5 V),<br>HS (high-speed main) mode: 1 to 16 MHz ($V_{DD}$ = 2.4 to 5.5 V),<br>LS (low-speed main) mode: 1 to 8 MHz ($V_{DD}$ = 1.8 to 5.5 V),<br>LV (low-voltage main) mode: 1 to 4 MHz ($V_{DD}$ = 1.6 to 5.5 V) | | | |
| Subsystem clock | | XT1 (crystal) oscillation, external subsystem clock input (EXCLKS) 32.768 kHz | | | |
| Low-speed on-chip oscillator clock | | 15 kHz (TYP.): $V_{DD}$ = 1.6 to 5.5 V | | | |
| General-purpose register | | 8 bits × 32 registers (8 bits × 8 registers × 4 banks) | | | |
| Minimum instruction execution time | | 0.03125 μs (High-speed on-chip oscillator clock: $f_{IH}$ = 32 MHz operation) | | | |
| | | 0.05 μs (High-speed system clock: $f_{MX}$ = 20 MHz operation) | | | |
| | | 30.5 μs (Subsystem clock: $f_{SUB}$ = 32.768 kHz operation) | | | |
| Instruction set | | • Data transfer (8/16 bits)<br>• Adder and subtractor/logical operation (8/16 bits)<br>• Multiplication (8 bits × 8 bits, 16 bits × 16 bits), Division (16 bits ÷ 16 bits, 32 bits ÷ 32 bits)<br>• Multiplication and Accumulation (16 bits × 16 bits + 32 bits)<br>• Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc. | | | |
| I/O port | Total | 40 | 44 | 48 | 58 |
| | CMOS I/O | 31 | 34 | 38 | 48 |
| | CMOS input | 5 | 5 | 5 | 5 |
| | CMOS output | — | 1 | 1 | 1 |
| | N-ch open-drain I/O (6 V tolerance) | 4 | 4 | 4 | 4 |
| Timer | 16-bit timer | 8 channels<br>(TAU: 4 channels, Timer RJ: 1 channel, Timer RD: 2 channels, Timer RG: 1 channel) | | | |
| | Watchdog timer | 1 channel | | | |
| | Real-time clock (RTC) | 1 channel | | | |
| | 12-bit interval timer | 1 channel | | | |
| | Timer output | Timer outputs: 13 channels<br>PWM outputs: 9 channels | | | |
| | RTC output | 1<br>• 1 Hz (subsystem clock: $f_{SUB}$ = 32.768 kHz) | | | |

(**Note** is listed on the next page.)

**Note** The flash library uses RAM in self-programming and rewriting of the data flash memory.
The target products and start address of the RAM areas used by the flash library are shown below.
R5F104xD (x = A to C, E to G, J, L): Start address FE900H
R5F104xE (x = A to C, E to G, J, L): Start address FE900H
For the RAM areas used by the flash library, see **Self RAM list of Flash Self-Programming Library for RL78 Family (R20UT2944)**.

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| Item | | 44-pin<br>R5F104Fx<br>(x = A, C to E) | 48-pin<br>R5F104Gx<br>(x = A, C to E) | 52-pin<br>R5F104Jx<br>(x = C to E) | 64-pin<br>R5F104Lx<br>(x = C to E) |
|---|---|---|---|---|---|
| Clock output/buzzer output | | 2 | 2 | 2 | 2 |
| | | • 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: $f_{MAIN}$ = 20 MHz operation)<br>• 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (Subsystem clock: $f_{SUB}$ = 32.768 kHz operation) | | | |
| 8/10-bit resolution A/D converter | | 10 channels | 10 channels | 12 channels | 12 channels |
| Serial interface | | [44-pin products]<br>• CSI: 1 channel/UART (UART supporting LIN-bus): 1 channel/simplified $I^2C$: 1 channel<br>• CSI: 1 channel/UART: 1 channel/simplified $I^2C$: 1 channel<br>• CSI: 2 channels/UART: 1 channel/simplified $I^2C$: 2 channels<br>[48-pin, 52-pin products]<br>• CSI: 2 channels/UART (UART supporting LIN-bus): 1 channel/simplified $I^2C$: 2 channels<br>• CSI: 1 channel/UART: 1 channel/simplified $I^2C$: 1 channel<br>• CSI: 2 channels/UART: 1 channel/simplified $I^2C$: 2 channels<br>[64-pin products]<br>• CSI: 2 channels/UART (UART supporting LIN-bus): 1 channel/simplified $I^2C$: 2 channels<br>• CSI: 2 channels/UART: 1 channel/simplified $I^2C$: 2 channels<br>• CSI: 2 channels/UART: 1 channel/simplified $I^2C$: 2 channels | | | |
| | $I^2C$ bus | 1 channel | 1 channel | 1 channel | 1 channel |
| Data transfer controller (DTC) | | 29 sources | 30 sources | | 31 sources |
| Event link controller (ELC) | | Event input: 20<br>Event trigger output: 7 | | | |
| Vectored interrupt sources | Internal | 24 | 24 | 24 | 24 |
| | External | 7 | 10 | 12 | 13 |
| Key interrupt | | 4 | 6 | 8 | 8 |
| Reset | | • Reset by $\overline{\text{RESET}}$ pin<br>• Internal reset by watchdog timer<br>• Internal reset by power-on-reset<br>• Internal reset by voltage detector<br>• Internal reset by illegal instruction execution Note<br>• Internal reset by RAM parity error<br>• Internal reset by illegal-memory access | | | |
| Power-on-reset circuit | | • Power-on-reset: 1.51 ±0.04 V ($T_A$ = –40 to +85°C)<br>1.51 ±0.06 V ($T_A$ = –40 to +105°C)<br>• Power-down-reset: 1.50 ±0.04 V ($T_A$ = –40 to +85°C)<br>1.50 ±0.06 V ($T_A$ = –40 to +105°C) | | | |
| Voltage detector | | 1.63 V to 4.06 V (14 stages) | | | |
| On-chip debug function | | Provided | | | |
| Power supply voltage | | $V_{DD}$ = 1.6 to 5.5 V ($T_A$ = -40 to +85°C)<br>$V_{DD}$ = 2.4 to 5.5 V ($T_A$ = -40 to +105°C) | | | |
| Operating ambient temperature | | $T_A$ = –40 to +85°C (A: Consumer applications, D: Industrial applications),<br>$T_A$ = -40 to +105°C (G: Industrial applications) | | | |

**Note** The illegal instruction is generated when instruction code FFH is executed.
Reset by the illegal instruction execution is not issued by emulation with the in-circuit emulator or on-chip debug emulator.

[44-pin, 48-pin, 52-pin, 64-pin products (code flash memory 96 KB to 256 KB)]

**Caution This outline describes the functions at the time when Peripheral I/O redirection register 0, 1 (PIOR0, 1) are set to 00H.**

(1/2)

| Item | | 44-pin<br>R5F104Fx<br>(x = F to H, J) | 48-pin<br>R5F104Gx<br>(x = F to H, J) | 52-pin<br>R5F104Jx<br>(x = F to H, J) | 64-pin<br>R5F104Lx<br>(x = F to H, J) |
|---|---|---|---|---|---|
| Code flash memory (KB) | | 96 to 256 | 96 to 256 | 96 to 256 | 96 to 256 |
| Data flash memory (KB) | | 8 | 8 | 8 | 8 |
| RAM (KB) | | 12 to 24 Note | 12 to 24 Note | 12 to 24 Note | 12 to 24 Note |
| Address space | | 1 MB | | | |
| Main system clock | High-speed system clock | X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK)<br>HS (high-speed main) mode: 1 to 20 MHz ($V_{DD}$ = 2.7 to 5.5 V),<br>HS (high-speed main) mode: 1 to 16 MHz ($V_{DD}$ = 2.4 to 5.5 V),<br>LS (low-speed main) mode: 1 to 8 MHz ($V_{DD}$ = 1.8 to 5.5 V),<br>LV (low-voltage main) mode: 1 to 4 MHz ($V_{DD}$ = 1.6 to 5.5 V) | | | |
| | High-speed on-chip oscillator clock ($f_{IH}$) | HS (high-speed main) mode: 1 to 32 MHz ($V_{DD}$ = 2.7 to 5.5 V),<br>HS (high-speed main) mode: 1 to 16 MHz ($V_{DD}$ = 2.4 to 5.5 V),<br>LS (low-speed main) mode: 1 to 8 MHz ($V_{DD}$ = 1.8 to 5.5 V),<br>LV (low-voltage main) mode: 1 to 4 MHz ($V_{DD}$ = 1.6 to 5.5 V) | | | |
| Subsystem clock | | XT1 (crystal) oscillation, external subsystem clock input (EXCLKS) 32.768 kHz | | | |
| Low-speed on-chip oscillator clock | | 15 kHz (TYP.): $V_{DD}$ = 1.6 to 5.5 V | | | |
| General-purpose register | | 8 bits × 32 registers (8 bits × 8 registers × 4 banks) | | | |
| Minimum instruction execution time | | 0.03125 μs (High-speed on-chip oscillator clock: $f_{IH}$ = 32 MHz operation) | | | |
| | | 0.05 μs (High-speed system clock: $f_{MX}$ = 20 MHz operation) | | | |
| | | 30.5 μs (Subsystem clock: $f_{SUB}$ = 32.768 kHz operation) | | | |
| Instruction set | | • Data transfer (8/16 bits)<br>• Adder and subtractor/logical operation (8/16 bits)<br>• Multiplication (8 bits × 8 bits, 16 bits × 16 bits), Division (16 bits ÷ 16 bits, 32 bits ÷ 32 bits)<br>• Multiplication and Accumulation (16 bits × 16 bits + 32 bits)<br>• Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc. | | | |
| I/O port | Total | 40 | 44 | 48 | 58 |
| | CMOS I/O | 31 | 34 | 38 | 48 |
| | CMOS input | 5 | 5 | 5 | 5 |
| | CMOS output | — | 1 | 1 | 1 |
| | N-ch open-drain I/O (6 V tolerance) | 4 | 4 | 4 | 4 |
| Timer | 16-bit timer | 8 channels<br>(TAU: 4 channels, Timer RJ: 1 channel, Timer RD: 2 channels, Timer RG: 1 channel) | | | |
| | Watchdog timer | 1 channel | | | |
| | Real-time clock (RTC) | 1 channel | | | |
| | 12-bit interval timer | 1 channel | | | |
| | Timer output | Timer outputs: 14 channels<br>PWM outputs: 9 channels | | | |
| | RTC output | 1<br>• 1 Hz (subsystem clock: $f_{SUB}$ = 32.768 kHz) | | | |

(**Note** is listed on the next page.)

**Note** The flash library uses RAM in self-programming and rewriting of the data flash memory.
The target products and start address of the RAM areas used by the flash library are shown below.
R5F104xJ (x = F, G, J, L, M, P): Start address F9F00H
For the RAM areas used by the flash library, see **Self RAM list of Flash Self-Programming Library for RL78 Family (R20UT2944)**.

(2/2)

| Item | | 44-pin<br>R5F104Fx<br>(x = F to H, J) | 48-pin<br>R5F104Gx<br>(x = F to H, J) | 52-pin<br>R5F104Jx<br>(x = F to H, J) | 64-pin<br>R5F104Lx<br>(x = F to H, J) |
|---|---|---|---|---|---|
| Clock output/buzzer output | | 2 | 2 | 2 | 2 |
| | | • 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: $f_{MAIN}$ = 20 MHz operation)<br>• 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (Subsystem clock: $f_{SUB}$ = 32.768 kHz operation) | | | |
| 8/10-bit resolution A/D converter | | 10 channels | 10 channels | 12 channels | 12 channels |
| D/A converter | | 2 channels | | | |
| Comparator | | 2 channels | | | |
| Serial interface | | [44-pin products]<br>• CSI: 1 channel/UART (UART supporting LIN-bus): 1 channel/simplified $I^2C$: 1 channel<br>• CSI: 1 channel/UART: 1 channel/simplified $I^2C$: 1 channel<br>• CSI: 2 channels/UART: 1 channel/simplified $I^2C$: 2 channels<br>[48-pin, 52-pin products]<br>• CSI: 2 channels/UART (UART supporting LIN-bus): 1 channel/simplified $I^2C$: 2 channels<br>• CSI: 1 channel/UART: 1 channel/simplified $I^2C$: 1 channel<br>• CSI: 2 channels/UART: 1 channel/simplified $I^2C$: 2 channels<br>[64-pin products]<br>• CSI: 2 channels/UART (UART supporting LIN-bus): 1 channel/simplified $I^2C$: 2 channels<br>• CSI: 2 channels/UART: 1 channel/simplified $I^2C$: 2 channels<br>• CSI: 2 channels/UART: 1 channel/simplified $I^2C$: 2 channels | | | |
| | $I^2C$ bus | 1 channel | 1 channel | 1 channel | 1 channel |
| Data transfer controller (DTC) | | 31 sources | 32 sources | | 33 sources |
| Event link controller (ELC) | | Event input: 22<br>Event trigger output: 9 | | | |
| Vectored interrupt sources | Internal | 24 | 24 | 24 | 24 |
| | External | 7 | 10 | 12 | 13 |
| Key interrupt | | 4 | 6 | 8 | 8 |
| Reset | | • Reset by $\overline{\text{RESET}}$ pin<br>• Internal reset by watchdog timer<br>• Internal reset by power-on-reset<br>• Internal reset by voltage detector<br>• Internal reset by illegal instruction execution Note<br>• Internal reset by RAM parity error<br>• Internal reset by illegal-memory access | | | |
| Power-on-reset circuit | | • Power-on-reset: 1.51 ±0.04 V ($T_A$ = –40 to +85°C)<br>1.51 ±0.06 V ($T_A$ = –40 to +105°C)<br>• Power-down-reset: 1.50 ±0.04 V ($T_A$ = –40 to +85°C)<br>1.50 ±0.06 V ($T_A$ = –40 to +105°C) | | | |
| Voltage detector | | 1.63 V to 4.06 V (14 stages) | | | |
| On-chip debug function | | Provided | | | |
| Power supply voltage | | $V_{DD}$ = 1.6 to 5.5 V ($T_A$ = -40 to +85°C)<br>$V_{DD}$ = 2.4 to 5.5 V ($T_A$ = -40 to +105°C) | | | |
| Operating ambient temperature | | $T_A$ = -40 to +85°C (A: Consumer applications, D: Industrial applications),<br>$T_A$ = -40 to +105°C (G: Industrial applications) | | | |

**Note** The illegal instruction is generated when instruction code FFH is executed.
Reset by the illegal instruction execution is not issued by emulation with the in-circuit emulator or on-chip debug emulator.

[48-pin, 64-pin products (code flash memory 384 KB to 512 KB)]

**Caution This outline describes the functions at the time when Peripheral I/O redirection register 0, 1 (PIOR0, 1) are set to 00H.**

(1/2)

| Item | | 48-pin | 64-pin |
|---|---|---|---|
| | | R5F104Gx (x = K, L) | R5F104Lx (x = K, L) |
| Code flash memory (KB) | | 384 to 512 | 384 to 512 |
| Data flash memory (KB) | | 8 | 8 |
| RAM (KB) | | 32 to 48 Note | 32 to 48 Note |
| Address space | | 1 MB | |
| Main system clock | High-speed system clock | X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK)<br>HS (high-speed main) mode: 1 to 20 MHz ($V_{DD}$ = 2.7 to 5.5 V),<br>HS (high-speed main) mode: 1 to 16 MHz ($V_{DD}$ = 2.4 to 5.5 V),<br>LS (low-speed main) mode: 1 to 8 MHz ($V_{DD}$ = 1.8 to 5.5 V),<br>LV (low-voltage main) mode: 1 to 4 MHz ($V_{DD}$ = 1.6 to 5.5 V) | |
| | High-speed on-chip oscillator clock ($f_{IH}$) | HS (high-speed main) mode: 1 to 32 MHz ($V_{DD}$ = 2.7 to 5.5 V),<br>HS (high-speed main) mode: 1 to 16 MHz ($V_{DD}$ = 2.4 to 5.5 V),<br>LS (low-speed main) mode: 1 to 8 MHz ($V_{DD}$ = 1.8 to 5.5 V),<br>LV (low-voltage main) mode: 1 to 4 MHz ($V_{DD}$ = 1.6 to 5.5 V) | |
| Subsystem clock | | XT1 (crystal) oscillation, external subsystem clock input (EXCLKS) 32.768 kHz | |
| Low-speed on-chip oscillator clock | | 15 kHz (TYP.): $V_{DD}$ = 1.6 to 5.5 V | |
| General-purpose register | | 8 bits × 32 registers (8 bits × 8 registers × 4 banks) | |
| Minimum instruction execution time | | 0.03125 μs (High-speed on-chip oscillator clock: $f_{IH}$ = 32 MHz operation) | |
| | | 0.05 μs (High-speed system clock: $f_{MX}$ = 20 MHz operation) | |
| | | 30.5 μs (Subsystem clock: $f_{SUB}$ = 32.768 kHz operation) | |
| Instruction set | | • Data transfer (8/16 bits)<br>• Adder and subtractor/logical operation (8/16 bits)<br>• Multiplication (8 bits × 8 bits, 16 bits × 16 bits), Division (16 bits ÷ 16 bits, 32 bits ÷ 32 bits)<br>• Multiplication and Accumulation (16 bits × 16 bits + 32 bits)<br>• Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc. | |
| I/O port | Total | 44 | 58 |
| | CMOS I/O | 34 | 48 |
| | CMOS input | 5 | 5 |
| | CMOS output | 1 | 1 |
| | N-ch open-drain I/O (6 V tolerance) | 4 | 4 |
| Timer | 16-bit timer | 8 channels<br>(TAU: 4 channels, Timer RJ: 1 channel, Timer RD: 2 channels, Timer RG: 1 channel) | |
| | Watchdog timer | 1 channel | |
| | Real-time clock (RTC) | 1 channel | |
| | 12-bit interval timer | 1 channel | |
| | Timer output | Timer outputs: 14 channels<br>PWM outputs: 9 channels | |
| | RTC output | 1<br>• 1 Hz (subsystem clock: $f_{SUB}$ = 32.768 kHz) | |

(**Note** is listed on the next page.)

**Note** The flash library uses RAM in self-programming and rewriting of the data flash memory.
The target products and start address of the RAM areas used by the flash library are shown below.
R5F104xL (x = G, L, M, P): Start address F3F00H
For the RAM areas used by the flash library, see **Self RAM list of Flash Self-Programming Library for RL78 Family (R20UT2944)**.

(2/2)

| Item | | 48-pin<br>R5F104Gx<br>(x = K, L) | 64-pin<br>R5F104Lx<br>(x = K, L) |
|---|---|---|---|
| Clock output/buzzer output | | 2 | 2 |
| | | • 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz<br>(Main system clock: $f_{MAIN}$ = 20 MHz operation)<br>• 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz<br>(Subsystem clock: $f_{SUB}$ = 32.768 kHz operation) | |
| 8/10-bit resolution A/D converter | | 10 channels | 12 channels |
| D/A converter | | 2 channels | |
| Comparator | | 2 channels | |
| Serial interface | | [48-pin products]<br>• CSI: 2 channels/UART (UART supporting LIN-bus): 1 channel/simplified $I^2C$: 2 channels<br>• CSI: 1 channel/UART: 1 channel/simplified $I^2C$: 1 channel<br>• CSI: 2 channels/UART: 1 channel/simplified $I^2C$: 2 channels<br>[64-pin products]<br>• CSI: 2 channels/UART (UART supporting LIN-bus): 1 channel/simplified $I^2C$: 2 channels<br>• CSI: 2 channels/UART: 1 channel/simplified $I^2C$: 2 channels<br>• CSI: 2 channels/UART: 1 channel/simplified $I^2C$: 2 channels | |
| | $I^2C$ bus | 1 channel | 1 channel |
| Data transfer controller (DTC) | | 32 sources | 33 sources |
| Event link controller (ELC) | | Event input: 22<br>Event trigger output: 9 | |
| Vectored interrupt sources | Internal | 24 | 24 |
| | External | 10 | 13 |
| Key interrupt | | 6 | 8 |
| Reset | | • Reset by $\overline{\text{RESET}}$ pin<br>• Internal reset by watchdog timer<br>• Internal reset by power-on-reset<br>• Internal reset by voltage detector<br>• Internal reset by illegal instruction execution Note<br>• Internal reset by RAM parity error<br>• Internal reset by illegal-memory access | |
| Power-on-reset circuit | | • Power-on-reset: 1.51 ±0.04 V ($T_A$ = –40 to +85°C)<br>1.51 ±0.06 V ($T_A$ = –40 to +105°C)<br>• Power-down-reset: 1.50 ±0.04 V ($T_A$ = –40 to +85°C)<br>1.50 ±0.06 V ($T_A$ = –40 to +105°C) | |
| Voltage detector | | 1.63 V to 4.06 V (14 stages) | |
| On-chip debug function | | Provided | |
| Power supply voltage | | $V_{DD}$ = 1.6 to 5.5 V ($T_A$ = -40 to +85°C)<br>$V_{DD}$ = 2.4 to 5.5 V ($T_A$ = -40 to +105°C) | |
| Operating ambient temperature | | $T_A$ = -40 to +85°C (A: Consumer applications, D: Industrial applications),<br>$T_A$ = -40 to +105°C (G: Industrial applications) | |

**Note** The illegal instruction is generated when instruction code FFH is executed.
Reset by the illegal instruction execution is not issued by emulation with the in-circuit emulator or on-chip debug emulator.

[80-pin, 100-pin products (code flash memory 96 KB to 256 KB)]

**Caution This outline describes the functions at the time when Peripheral I/O redirection register 0, 1 (PIOR0, 1) are set to 00H.**

(1/2)

| Item | | 80-pin | 100-pin |
|---|---|---|---|
| | | R5F104Mx (x = F to H, J) | R5F104Px (x = F to H, J) |
| Code flash memory (KB) | | 96 to 256 | 96 to 256 |
| Data flash memory (KB) | | 8 | 8 |
| RAM (KB) | | 12 to 24 Note | 12 to 24 Note |
| Address space | | 1 MB | |
| Main system clock | High-speed system clock | X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK)<br>HS (high-speed main) mode: 1 to 20 MHz ($V_{DD}$ = 2.7 to 5.5 V),<br>HS (high-speed main) mode: 1 to 16 MHz ($V_{DD}$ = 2.4 to 5.5 V),<br>LS (low-speed main) mode: 1 to 8 MHz ($V_{DD}$ = 1.8 to 5.5 V),<br>LV (low-voltage main) mode: 1 to 4 MHz ($V_{DD}$ = 1.6 to 5.5 V) | |
| | High-speed on-chip oscillator clock ($f_{IH}$) | HS (high-speed main) mode: 1 to 32 MHz ($V_{DD}$ = 2.7 to 5.5 V),<br>HS (high-speed main) mode: 1 to 16 MHz ($V_{DD}$ = 2.4 to 5.5 V),<br>LS (low-speed main) mode: 1 to 8 MHz ($V_{DD}$ = 1.8 to 5.5 V),<br>LV (low-voltage main) mode: 1 to 4 MHz ($V_{DD}$ = 1.6 to 5.5 V) | |
| Subsystem clock | | XT1 (crystal) oscillation, external subsystem clock input (EXCLKS) 32.768 kHz | |
| Low-speed on-chip oscillator clock | | 15 kHz (TYP.): $V_{DD}$ = 1.6 to 5.5 V | |
| General-purpose register | | 8 bits × 32 registers (8 bits × 8 registers × 4 banks) | |
| Minimum instruction execution time | | 0.03125 μs (High-speed on-chip oscillator clock: $f_{IH}$ = 32 MHz operation) | |
| | | 0.05 μs (High-speed system clock: $f_{MX}$ = 20 MHz operation) | |
| | | 30.5 μs (Subsystem clock: $f_{SUB}$ = 32.768 kHz operation) | |
| Instruction set | | • Data transfer (8/16 bits)<br>• Adder and subtractor/logical operation (8/16 bits)<br>• Multiplication (8 bits × 8 bits, 16 bits × 16 bits), Division (16 bits ÷ 16 bits, 32 bits ÷ 32 bits)<br>• Multiplication and Accumulation (16 bits × 16 bits + 32 bits)<br>• Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc. | |
| I/O port | Total | 74 | 92 |
| | CMOS I/O | 64 | 82 |
| | CMOS input | 5 | 5 |
| | CMOS output | 1 | 1 |
| | N-ch open-drain I/O (6 V tolerance) | 4 | 4 |
| Timer | 16-bit timer | 12 channels<br>(TAU: 8 channels, Timer RJ: 1 channel, Timer RD: 2 channels, Timer RG: 1 channel) | |
| | Watchdog timer | 1 channel | |
| | Real-time clock (RTC) | 1 channel | |
| | 12-bit interval timer | 1 channel | |
| | Timer output | Timer outputs: 18 channels<br>PWM outputs: 12 channels | |
| | RTC output | 1<br>• 1 Hz (subsystem clock: $f_{SUB}$ = 32.768 kHz) | |

**Note** In the case of the 24 KB, this is about 23 KB when the self-programming function and data flash function are used (For details, see **CHAPTER 3** in the RL78/G14 User's Manual).

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| Item | | 80-pin<br>R5F104Mx<br>(x = F to H, J) | 100-pin<br>R5F104Px<br>(x = F to H, J) |
|---|---|---|---|
| Clock output/buzzer output | | 2 | 2 |
| | | • 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz<br>(Main system clock: $f_{MAIN}$ = 20 MHz operation)<br>• 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz<br>(Subsystem clock: $f_{SUB}$ = 32.768 kHz operation) | |
| 8/10-bit resolution A/D converter | | 17 channels | 20 channels |
| D/A converter | | 2 channels | 2 channels |
| Comparator | | 2 channels | 2 channels |
| Serial interface | | [80-pin, 100-pin products]<br>• CSI: 2 channels/UART (UART supporting LIN-bus): 1 channel/simplified $I^2C$: 2 channels<br>• CSI: 2 channels/UART: 1 channel/simplified $I^2C$: 2 channels<br>• CSI: 2 channels/UART: 1 channel/simplified $I^2C$: 2 channels<br>• CSI: 2 channels/UART: 1 channel/simplified $I^2C$: 2 channels | |
| | $I^2C$ bus | 2 channels | 2 channels |
| Data transfer controller (DTC) | | 39 sources | 39 sources |
| Event link controller (ELC) | | Event input: 26<br>Event trigger output: 9 | |
| Vectored interrupt sources | Internal | 32 | 32 |
| | External | 13 | 13 |
| Key interrupt | | 8 | 8 |
| Reset | | • Reset by $\overline{\text{RESET}}$ pin<br>• Internal reset by watchdog timer<br>• Internal reset by power-on-reset<br>• Internal reset by voltage detector<br>• Internal reset by illegal instruction execution Note<br>• Internal reset by RAM parity error<br>• Internal reset by illegal-memory access | |
| Power-on-reset circuit | | • Power-on-reset: 1.51 ±0.04 V ($T_A$ = –40 to +85°C)<br>1.51 ±0.06 V ($T_A$ = –40 to +105°C)<br>• Power-down-reset: 1.50 ±0.04 V ($T_A$ = –40 to +85°C)<br>1.50 ±0.06 V ($T_A$ = –40 to +105°C) | |
| Voltage detector | | 1.63 V to 4.06 V (14 stages) | |
| On-chip debug function | | Provided | |
| Power supply voltage | | $V_{DD}$ = 1.6 to 5.5 V ($T_A$ = -40 to +85°C)<br>$V_{DD}$ = 2.4 to 5.5 V ($T_A$ = -40 to +105°C) | |
| Operating ambient temperature | | $T_A$ = -40 to +85°C (A: Consumer applications, D: Industrial applications),<br>$T_A$ = -40 to +105°C (G: Industrial applications) | |

**Note** The illegal instruction is generated when instruction code FFH is executed.
Reset by the illegal instruction execution is not issued by emulation with the in-circuit emulator or on-chip debug emulator.

[80-pin, 100-pin products (code flash memory 384 KB to 512 KB)]

**Caution This outline describes the functions at the time when Peripheral I/O redirection register 0, 1 (PIOR0, 1) are set to 00H.**

(1/2)

| Item | | 80-pin | 100-pin |
|---|---|---|---|
| | | R5F104Mx (x = K, L) | R5F104Px (x = K, L) |
| Code flash memory (KB) | | 384 to 512 | 384 to 512 |
| Data flash memory (KB) | | 8 | 8 |
| RAM (KB) | | 32 to 48 Note | 32 to 48 Note |
| Address space | | 1 MB | |
| Main system clock | High-speed system clock | X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK)<br>HS (high-speed main) mode: 1 to 20 MHz ($V_{DD}$ = 2.7 to 5.5 V),<br>HS (high-speed main) mode: 1 to 16 MHz ($V_{DD}$ = 2.4 to 5.5 V),<br>LS (low-speed main) mode: 1 to 8 MHz ($V_{DD}$ = 1.8 to 5.5 V),<br>LV (low-voltage main) mode: 1 to 4 MHz ($V_{DD}$ = 1.6 to 5.5 V) | |
| | High-speed on-chip oscillator clock ($f_{IH}$) | HS (high-speed main) mode: 1 to 32 MHz ($V_{DD}$ = 2.7 to 5.5 V),<br>HS (high-speed main) mode: 1 to 16 MHz ($V_{DD}$ = 2.4 to 5.5 V),<br>LS (low-speed main) mode: 1 to 8 MHz ($V_{DD}$ = 1.8 to 5.5 V),<br>LV (low-voltage main) mode: 1 to 4 MHz ($V_{DD}$ = 1.6 to 5.5 V) | |
| Subsystem clock | | XT1 (crystal) oscillation, external subsystem clock input (EXCLKS) 32.768 kHz | |
| Low-speed on-chip oscillator clock | | 15 kHz (TYP.): $V_{DD}$ = 1.6 to 5.5 V | |
| General-purpose register | | 8 bits × 32 registers (8 bits × 8 registers × 4 banks) | |
| Minimum instruction execution time | | 0.03125 μs (High-speed on-chip oscillator clock: $f_{IH}$ = 32 MHz operation) | |
| | | 0.05 μs (High-speed system clock: $f_{MX}$ = 20 MHz operation) | |
| | | 30.5 μs (Subsystem clock: $f_{SUB}$ = 32.768 kHz operation) | |
| Instruction set | | • Data transfer (8/16 bits)<br>• Adder and subtractor/logical operation (8/16 bits)<br>• Multiplication (8 bits × 8 bits, 16 bits × 16 bits), Division (16 bits ÷ 16 bits, 32 bits ÷ 32 bits)<br>• Multiplication and Accumulation (16 bits × 16 bits + 32 bits)<br>• Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc. | |
| I/O port | Total | 74 | 92 |
| | CMOS I/O | 64 | 82 |
| | CMOS input | 5 | 5 |
| | CMOS output | 1 | 1 |
| | N-ch open-drain I/O (6 V tolerance) | 4 | 4 |
| Timer | 16-bit timer | 12 channels<br>(TAU: 8 channels, Timer RJ: 1 channel, Timer RD: 2 channels, Timer RG: 1 channel) | |
| | Watchdog timer | 1 channel | |
| | Real-time clock (RTC) | 1 channel | |
| | 12-bit interval timer | 1 channel | |
| | Timer output | Timer outputs: 18 channels<br>PWM outputs: 12 channels | |
| | RTC output | 1<br>• 1 Hz (subsystem clock: $f_{SUB}$ = 32.768 kHz) | |

**Note** In the case of the 48 KB, this is about 47 KB when the self-programming function and data flash function are used (For details, see **CHAPTER 3** in the RL78/G14 User's Manual).

(2/2)

| Item | | 80-pin<br>R5F104Mx<br>(x = K, L) | 100-pin<br>R5F104Px<br>(x = K, L) |
|---|---|---|---|
| Clock output/buzzer output | | 2 | 2 |
| | | • 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: $f_{MAIN}$ = 20 MHz operation)<br>• 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (Subsystem clock: $f_{SUB}$ = 32.768 kHz operation) | |
| 8/10-bit resolution A/D converter | | 17 channels | 20 channels |
| D/A converter | | 2 channels | 2 channels |
| Comparator | | 2 channels | 2 channels |
| Serial interface | | [80-pin, 100-pin products]<br>• CSI: 2 channels/UART (UART supporting LIN-bus): 1 channel/simplified $I^2C$: 2 channels<br>• CSI: 2 channels/UART: 1 channel/simplified $I^2C$: 2 channels<br>• CSI: 2 channels/UART: 1 channel/simplified $I^2C$: 2 channels<br>• CSI: 2 channels/UART: 1 channel/simplified $I^2C$: 2 channels | |
| | $I^2C$ bus | 2 channels | 2 channels |
| Data transfer controller (DTC) | | 39 sources | 39 sources |
| Event link controller (ELC) | | Event input: 26<br>Event trigger output: 9 | |
| Vectored interrupt sources | Internal | 32 | 32 |
| | External | 13 | 13 |
| Key interrupt | | 8 | 8 |
| Reset | | • Reset by $\overline{\text{RESET}}$ pin<br>• Internal reset by watchdog timer<br>• Internal reset by power-on-reset<br>• Internal reset by voltage detector<br>• Internal reset by illegal instruction execution Note<br>• Internal reset by RAM parity error<br>• Internal reset by illegal-memory access | |
| Power-on-reset circuit | | • Power-on-reset: 1.51 ±0.04 V ($T_A$ = –40 to +85°C)<br>1.51 ±0.06 V ($T_A$ = –40 to +105°C)<br>• Power-down-reset: 1.50 ±0.04 V ($T_A$ = –40 to +85°C)<br>1.50 ±0.06 V ($T_A$ = –40 to +105°C) | |
| Voltage detector | | 1.63 V to 4.06 V (14 stages) | |
| On-chip debug function | | Provided | |
| Power supply voltage | | $V_{DD}$ = 1.6 to 5.5 V ($T_A$ = -40 to +85°C)<br>$V_{DD}$ = 2.4 to 5.5 V ($T_A$ = -40 to +105°C) | |
| Operating ambient temperature | | $T_A$ = -40 to +85°C (A: Consumer applications, D: Industrial applications),<br>$T_A$ = -40 to +105°C (G: Industrial applications) | |

**Note** The illegal instruction is generated when instruction code FFH is executed.
Reset by the illegal instruction execution is not issued by emulation with the in-circuit emulator or on-chip debug emulator.

# 2. ELECTRICAL SPECIFICATIONS ($T_A$ = -40 to +85°C)

This chapter describes the following electrical specifications.

Target products A: Consumer applications $T_A$ = -40 to +85°C
R5F104xxAxx
D: Industrial applications $T_A$ = -40 to +85°C
R5F104xxDxx
G: Industrial applications when $T_A$ = -40 to +105°C products is used in the range of $T_A$ = -40 to +85°C
R5F104xxGxx

**Caution 1. The RL78 microcontrollers have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.**

**Caution 2. With products not provided with an $EV_{DD0}$, $EV_{DD1}$, $EV_{SS0}$, or $EV_{SS1}$ pin, replace $EV_{DD0}$ and $EV_{DD1}$ with $V_{DD}$, or replace $EV_{SS0}$ and $EV_{SS1}$ with $V_{SS}$.**

**Caution 3. The pins mounted depend on the product. Refer to 2.1 Port Functions to 2.2.1 Functions for each product in the RL78/G14 User's Manual.**

## 2.1 Absolute Maximum Ratings

**Absolute Maximum Ratings** **(1/2)**

| Parameter | Symbols | Conditions | Ratings | Unit |
|---|---|---|---|---|
| Supply voltage | $V_{DD}$ | | -0.5 to +6.5 | V |
| | $EV_{DD0}$, $EV_{DD1}$ | $EV_{DD0}$ = $EV_{DD1}$ | -0.5 to +6.5 | V |
| | $EV_{SS0}$, $EV_{SS1}$ | $EV_{SS0}$ = $EV_{SS1}$ | -0.5 to +0.3 | V |
| REGC pin input voltage | $V_{IREGC}$ | REGC | -0.3 to +2.8 and -0.3 to $V_{DD}$ +0.3 Note 1 | V |
| Input voltage | $V_{I1}$ | P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P140 to P147 | -0.3 to $EV_{DD0}$ +0.3 and -0.3 to $V_{DD}$ +0.3 Note 2 | V |
| | $V_{I2}$ | P60 to P63 (N-ch open-drain) | -0.3 to +6.5 | V |
| | $V_{I3}$ | P20 to P27, P121 to P124, P137, P150 to P156, EXCLK, EXCLKS, $\overline{\text{RESET}}$ | -0.3 to $V_{DD}$ +0.3 Note 2 | V |
| Output voltage | $V_{O1}$ | P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147 | -0.3 to $EV_{DD0}$ +0.3 and -0.3 to $V_{DD}$ +0.3 Note 2 | V |
| | $V_{O2}$ | P20 to P27, P150 to P156 | -0.3 to $V_{DD}$ +0.3 Note 2 | V |
| Analog input voltage | $V_{AI1}$ | ANI16 to ANI20 | -0.3 to $EV_{DD0}$ +0.3 and -0.3 to $AV_{REF}$(+) +0.3 Notes 2, 3 | V |
| | $V_{AI2}$ | ANI0 to ANI14 | -0.3 to $V_{DD}$ +0.3 and -0.3 to $AV_{REF}$(+) +0.3 Notes 2, 3 | V |

**Note 1.** Connect the REGC pin to $V_{SS}$ via a capacitor (0.47 to 1 μF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

**Note 2.** Must be 6.5 V or lower.

**Note 3.** Do not exceed $AV_{REF}$ (+) + 0.3 V in case of A/D conversion target pin.

**Caution** **Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

**Remark 1.** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**Remark 2.** $AV_{REF}$ (+): + side reference voltage of the A/D converter.

**Remark 3.** $V_{SS}$: Reference voltage

**Absolute Maximum Ratings** **(2/2)**

| Parameter | Symbols | Conditions | | Ratings | Unit |
|---|---|---|---|---|---|
| Output current, high | $I_{OH1}$ | Per pin | P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147 | -40 | mA |
| | | Total of all pins -170 mA | P00 to P04, P40 to P47, P102, P120, P130, P140 to P145 | -70 | mA |
| | | | P05, P06, P10 to P17, P30, P31, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100, P101, P110, P111, P146, P147 | -100 | mA |
| | $I_{OH2}$ | Per pin | P20 to P27, P150 to P156 | -0.5 | mA |
| | | Total of all pins | | -2 | mA |
| Output current, low | $I_{OL1}$ | Per pin | P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147 | 40 | mA |
| | | Total of all pins 170 mA | P00 to P04, P40 to P47, P102, P120, P130, P140 to P145 | 70 | mA |
| | | | P05, P06, P10 to P17, P30, P31, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P100, P101, P110, P111, P146, P147 | 100 | mA |
| | $I_{OL2}$ | Per pin | P20 to P27, P150 to P156 | 1 | mA |
| | | Total of all pins | | 5 | mA |
| Operating ambient temperature | $T_A$ | In normal operation mode | | -40 to +85 | °C |
| | | In flash memory programming mode | | | |
| Storage temperature | $T_{stg}$ | | | -65 to +150 | °C |

**Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

## 2.2 Oscillator Characteristics

### 2.2.1 X1, XT1 characteristics

**($T_A$ = -40 to +85°C, 1.6 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Resonator | Resonator | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| X1 clock oscillation frequency ($f_X$) Note | Ceramic resonator/ crystal resonator | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 1.0 | | 20.0 | MHz |
| | | 2.4 V ≤ $V_{DD}$ < 2.7 V | 1.0 | | 16.0 | |
| | | 1.8 V ≤ $V_{DD}$ < 2.4 V | 1.0 | | 8.0 | |
| | | 1.6 V ≤ $V_{DD}$ < 1.8 V | 1.0 | | 4.0 | |
| XT1 clock oscillation frequency ($f_{XT}$) Note | Crystal resonator | | 32 | 32.768 | 35 | kHz |

**Note** Indicates only permissible oscillator frequency ranges. Refer to **AC Characteristics** for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

**Caution Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.**

**Remark** When using the X1 oscillator and XT1 oscillator, refer to **5.4 System Clock Oscillator** in the RL78/G14 User's Manual.

### 2.2.2 On-chip oscillator characteristics

**($T_A$ = -40 to +85°C, 1.6 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Oscillators | Parameters | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| High-speed on-chip oscillator clock frequency Notes 1, 2 | $f_{IH}$ | | | 1 | | 32 | MHz |
| High-speed on-chip oscillator clock frequency accuracy | | -20 to +85°C | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | -1.0 | | +1.0 | % |
| | | | 1.6 V ≤ $V_{DD}$ < 1.8 V | -5.0 | | +5.0 | % |
| | | -40 to -20°C | 1.8 V ≤ $V_{DD}$ < 5.5 V | -1.5 | | +1.5 | % |
| | | | 1.6 V ≤ $V_{DD}$ < 1.8 V | -5.5 | | +5.5 | % |
| Low-speed on-chip oscillator clock frequency | $f_{IL}$ | | | | 15 | | kHz |
| Low-speed on-chip oscillator clock frequency accuracy | | | | -15 | | +15 | % |

**Note 1.** High-speed on-chip oscillator frequency is selected with bits 0 to 4 of the option byte (000C2H) and bits 0 to 2 of the HOCODIV register.

**Note 2.** This only indicates the oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

## 2.3 DC Characteristics

### 2.3.1 Pin characteristics

**($T_A$ = -40 to +85°C, 1.6 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)** **(1/5)**

| Items | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Output current, high Note 1 | $I_{OH1}$ | Per pin for P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147 | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V | | | -10.0 Note 2 | mA |
| | | Total of P00 to P04, P40 to P47, P102, P120, P130, P140 to P145 (When duty ≤ 70% Note 3) | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V | | | -55.0 | mA |
| | | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V | | | -10.0 | mA |
| | | | 1.8 V ≤ $EV_{DD0}$ < 2.7 V | | | -5.0 | mA |
| | | | 1.6 V ≤ $EV_{DD0}$ < 1.8 V | | | -2.5 | mA |
| | | Total of P05, P06, P10 to P17, P30, P31, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100, P101, P110, P111, P146, P147 (When duty ≤ 70% Note 3) | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V | | | -80.0 | mA |
| | | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V | | | -19.0 | mA |
| | | | 1.8 V ≤ $EV_{DD0}$ < 2.7 V | | | -10.0 | mA |
| | | | 1.6 V ≤ $EV_{DD0}$ < 1.8 V | | | -5.0 | mA |
| | | Total of all pins (When duty ≤ 70% Note 3) | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V | | | -135.0 Note 4 | mA |
| | $I_{OH2}$ | Per pin for P20 to P27, P150 to P156 | 1.6 V ≤ $V_{DD}$ ≤ 5.5 V | | | -0.1 Note 2 | mA |
| | | Total of all pins (When duty ≤ 70% Note 3) | 1.6 V ≤ $V_{DD}$ ≤ 5.5 V | | | -1.5 | mA |

**Note 1.** Value of current at which the device operation is guaranteed even if the current flows from the $EV_{DD0}$, $EV_{DD1}$, $V_{DD}$ pins to an output pin.

**Note 2.** Do not exceed the total current value.

**Note 3.** Specification under conditions where the duty factor ≤ 70%.
The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = ($I_{OH}$ × 0.7)/(n × 0.01)

<Example> Where n = 80% and $I_{OH}$ = -10.0 mA
Total output current of pins = (-10.0 × 0.7)/(80 × 0.01) ≈ -8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor.
A current higher than the absolute maximum rating must not flow into one pin.

**Note 4.** -100 mA for industrial applications (R5F104xxDxx, R5F104xxGxx).

**Caution** **P00, P02 to P04, P10, P11, P13 to P15, P17, P30, P43 to P45, P50 to P55, P71, P74, P80 to P82, and P142 to P144 do not output high level in N-ch open-drain mode.**

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**($T_A$ = -40 to +85°C, 1.6 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)** **(2/5)**

| Items | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Output current, low Note 1 | $I_{OL1}$ | Per pin for P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147 | | | | 20.0 Note 2 | mA |
| | | Per pin for P60 to P63 | | | | 15.0 Note 2 | mA |
| | | Total of P00 to P04, P40 to P47, P102, P120, P130, P140 to P145 (When duty ≤ 70% Note 3) | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V | | | 70.0 | mA |
| | | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V | | | 15.0 | mA |
| | | | 1.8 V ≤ $EV_{DD0}$ < 2.7 V | | | 9.0 | mA |
| | | | 1.6 V ≤ $EV_{DD0}$ < 1.8 V | | | 4.5 | mA |
| | | Total of P05, P06, P10 to P17, P30, P31, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P100, P101, P110, P111, P146, P147 (When duty ≤ 70% Note 3) | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V | | | 80.0 | mA |
| | | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V | | | 35.0 | mA |
| | | | 1.8 V ≤ $EV_{DD0}$ < 2.7 V | | | 20.0 | mA |
| | | | 1.6 V ≤ $EV_{DD0}$ < 1.8 V | | | 10.0 | mA |
| | | Total of all pins (When duty ≤ 70% Note 3) | | | | 150.0 | mA |
| | $I_{OL2}$ | Per pin for P20 to P27, P150 to P156 | | | | 0.4 Note 2 | mA |
| | | Total of all pins (When duty ≤ 70% Note 3) | 1.6 V ≤ $V_{DD}$ ≤ 5.5 V | | | 5.0 | mA |

**Note 1.** Value of current at which the device operation is guaranteed even if the current flows from an output pin to the $EV_{SS0}$, $EV_{SS1}$, and $V_{SS}$ pins.

**Note 2.** Do not exceed the total current value.

**Note 3.** Specification under conditions where the duty factor ≤ 70%.
The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = ($I_{OL}$ × 0.7)/(n × 0.01)

<Example> Where n = 80% and $I_{OL}$ = 10.0 mA
Total output current of pins = (10.0 × 0.7)/(80 × 0.01) ≈ 8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor.
A current higher than the absolute maximum rating must not flow into one pin.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**($T_A$ = -40 to +85°C, 1.6 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)** **(3/5)**

| Items | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Input voltage, high | $V_{IH1}$ | P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P140 to P147 | Normal input buffer | 0.8 $EV_{DD0}$ | | $EV_{DD0}$ | V |
| | $V_{IH2}$ | P01, P03, P04, P10, P14 to P17, P30, P43, P44, P50, P53 to P55, P80, P81, P142, P143 | TTL input buffer 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V | 2.2 | | $EV_{DD0}$ | V |
| | | | TTL input buffer 3.3 V ≤ $EV_{DD0}$ < 4.0 V | 2.0 | | $EV_{DD0}$ | V |
| | | | TTL input buffer 1.6 V ≤ $EV_{DD0}$ < 3.3 V | 1.5 | | $EV_{DD0}$ | V |
| | $V_{IH3}$ | P20 to P27, P150 to P156 | | 0.7 $V_{DD}$ | | $V_{DD}$ | V |
| | $V_{IH4}$ | P60 to P63 | | 0.7 $EV_{DD0}$ | | 6.0 | V |
| | $V_{IH5}$ | P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$ | | 0.8 $V_{DD}$ | | $V_{DD}$ | V |
| Input voltage, low | $V_{IL1}$ | P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P140 to P147 | Normal input buffer | 0 | | 0.2 $EV_{DD0}$ | V |
| | $V_{IL2}$ | P01, P03, P04, P10, P14 to P17, P30, P43, P44, P50, P53 to P55, P80, P81, P142, P143 | TTL input buffer 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V | 0 | | 0.8 | V |
| | | | TTL input buffer 3.3 V ≤ $EV_{DD0}$ < 4.0 V | 0 | | 0.5 | V |
| | | | TTL input buffer 1.6 V ≤ $EV_{DD0}$ < 3.3 V | 0 | | 0.32 | V |
| | $V_{IL3}$ | P20 to P27, P150 to P156 | | 0 | | 0.3 $V_{DD}$ | V |
| | $V_{IL4}$ | P60 to P63 | | 0 | | 0.3 $EV_{DD0}$ | V |
| | $V_{IL5}$ | P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$ | | 0 | | 0.2 $V_{DD}$ | V |

**Caution The maximum value of $V_{IH}$ of pins P00, P02 to P04, P10, P11, P13 to P15, P17, P30, P43 to P45, P50 to P55, P71, P74, P80 to P82, and P142 to P144 is $EV_{DD0}$, even in the N-ch open-drain mode.**

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**($T_A$ = -40 to +85°C, 1.6 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)** **(4/5)**

| Items | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Output voltage, high | $V_{OH1}$ | P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147 | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, $I_{OH1}$ = -10.0 mA | $EV_{DD0}$ - 1.5 | | | V |
| | | | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, $I_{OH1}$ = -3.0 mA | $EV_{DD0}$ - 0.7 | | | V |
| | | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V, $I_{OH1}$ = -1.5 mA | $EV_{DD0}$ - 0.5 | | | V |
| | | | 1.6 V ≤ $EV_{DD0}$ < 1.8 V, $I_{OH1}$ = -1.0 mA | $EV_{DD0}$ - 0.5 | | | V |
| | $V_{OH2}$ | P20 to P27, P150 to P156 | 1.6 V ≤ $V_{DD}$ ≤ 5.5 V, $I_{OH2}$ = -100 μA | $V_{DD}$ - 0.5 | | | V |
| Output voltage, low | $V_{OL1}$ | P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147 | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, $I_{OL1}$ = 20.0 mA | | | 1.3 | V |
| | | | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, $I_{OL1}$ = 8.5 mA | | | 0.7 | V |
| | | | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V, $I_{OL1}$ = 3.0 mA | | | 0.6 | V |
| | | | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V, $I_{OL1}$ = 1.5 mA | | | 0.4 | V |
| | | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V, $I_{OL1}$ = 0.6 mA | | | 0.4 | V |
| | | | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V, $I_{OL1}$ = 0.3 mA | | | 0.4 | V |
| | $V_{OL2}$ | P20 to P27, P150 to P156 | 1.6 V ≤ $V_{DD}$ ≤ 5.5 V, $I_{OL2}$ = 400 μA | | | 0.4 | V |
| | $V_{OL3}$ | P60 to P63 | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, $I_{OL3}$ = 15.0 mA | | | 2.0 | V |
| | | | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, $I_{OL3}$ = 5.0 mA | | | 0.4 | V |
| | | | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V, $I_{OL3}$ = 3.0 mA | | | 0.4 | V |
| | | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V, $I_{OL3}$ = 2.0 mA | | | 0.4 | V |
| | | | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V, $I_{OL3}$ = 1.0 mA | | | 0.4 | V |

**Caution** **P00, P02 to P04, P10, P11, P13 to P15, P17, P30, P43 to P45, P50 to P55, P71, P74, P80 to P82, P142 to P144 do not output high level in N-ch open-drain mode.**

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**($T_A$ = -40 to +85°C, 1.6 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)** **(5/5)**

| Items | Symbol | Conditions | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|
| Input leakage current, high | $I_{LIH1}$ | P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P140 to P147 | $V_I$ = $EV_{DD0}$ | | | | 1 | μA |
| | $I_{LIH2}$ | P20 to P27, P137, P150 to P156, $\overline{\text{RESET}}$ | $V_I$ = $V_{DD}$ | | | | 1 | μA |
| | $I_{LIH3}$ | P121 to P124 (X1, X2, EXCLK, XT1, XT2, EXCLKS) | $V_I$ = $V_{DD}$ | In input port or external clock input | | | 1 | μA |
| | | | | In resonator connection | | | 10 | μA |
| Input leakage current, low | $I_{LIL1}$ | P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P140 to P147 | $V_I$ = $EV_{SS0}$ | | | | -1 | μA |
| | $I_{LIL2}$ | P20 to P27, P137, P150 to P156, $\overline{\text{RESET}}$ | $V_I$ = $V_{SS}$ | | | | -1 | μA |
| | $I_{LIL3}$ | P121 to P124 (X1, X2, EXCLK, XT1, XT2, EXCLKS) | $V_I$ = $V_{SS}$ | In input port or external clock input | | | -1 | μA |
| | | | | In resonator connection | | | -10 | μA |
| On-chip pull-up resistance | $R_U$ | P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P140 to P147 | $V_I$ = $EV_{SS0}$, In input port | | 10 | 20 | 100 | kΩ |

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

## 2.3.2 Supply current characteristics

**(1) Flash ROM: 16 to 64 KB of 30- to 64-pin products**

**($T_A$ = -40 to +85°C, 1.6 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = 0 V) (1/2)**

| Parameter | Symbol | Conditions | | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| Supply current Note 1 | IDD1 | Operating mode | HS (high-speed main) mode Note 5 | $f_{HOCO}$ = 64 MHz, $f_{IH}$ = 32 MHz Note 3 | Basic operation | $V_{DD}$ = 5.0 V | | 2.4 | | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 2.4 | | |
| | | | | $f_{HOCO}$ = 32 MHz, $f_{IH}$ = 32 MHz Note 3 | Basic operation | $V_{DD}$ = 5.0 V | | 2.1 | | |
| | | | | | | $V_{DD}$ = 3.0 V | | 2.1 | | |
| | | | HS (high-speed main) mode Note 5 | $f_{HOCO}$ = 64 MHz, $f_{IH}$ = 32 MHz Note 3 | Normal operation | $V_{DD}$ = 5.0 V | | 5.1 | 8.7 | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 5.1 | 8.7 | |
| | | | | $f_{HOCO}$ = 32 MHz, $f_{IH}$ = 32 MHz Note 3 | Normal operation | $V_{DD}$ = 5.0 V | | 4.8 | 8.1 | |
| | | | | | | $V_{DD}$ = 3.0 V | | 4.8 | 8.1 | |
| | | | | $f_{HOCO}$ = 48 MHz, $f_{IH}$ = 24 MHz Note 3 | Normal operation | $V_{DD}$ = 5.0 V | | 4.0 | 6.9 | |
| | | | | | | $V_{DD}$ = 3.0 V | | 4.0 | 6.9 | |
| | | | | $f_{HOCO}$ = 24 MHz, $f_{IH}$ = 24 MHz Note 3 | Normal operation | $V_{DD}$ = 5.0 V | | 3.8 | 6.3 | |
| | | | | | | $V_{DD}$ = 3.0 V | | 3.8 | 6.3 | |
| | | | | $f_{HOCO}$ = 16 MHz, $f_{IH}$ = 16 MHz Note 3 | Normal operation | $V_{DD}$ = 5.0 V | | 2.8 | 4.6 | |
| | | | | | | $V_{DD}$ = 3.0 V | | 2.8 | 4.6 | |
| | | | LS (low-speed main) mode Note 5 | $f_{HOCO}$ = 8 MHz, $f_{IH}$ = 8 MHz Note 3 | Normal operation | $V_{DD}$ = 3.0 V | | 1.3 | 2.0 | mA |
| | | | | | | $V_{DD}$ = 2.0 V | | 1.3 | 2.0 | |
| | | | LV (low-voltage main) mode Note 5 | $f_{HOCO}$ = 4 MHz, $f_{IH}$ = 4 MHz Note 3 | Normal operation | $V_{DD}$ = 3.0 V | | 1.3 | 1.8 | mA |
| | | | | | | $V_{DD}$ = 2.0 V | | 1.3 | 1.8 | |
| | | | HS (high-speed main) mode Note 5 | $f_{MX}$ = 20 MHz Note 2, $V_{DD}$ = 5.0 V | Normal operation | Square wave input | | 3.3 | 5.3 | mA |
| | | | | | | Resonator connection | | 3.4 | 5.5 | |
| | | | | $f_{MX}$ = 20 MHz Note 2, $V_{DD}$ = 3.0 V | Normal operation | Square wave input | | 3.3 | 5.3 | |
| | | | | | | Resonator connection | | 3.4 | 5.5 | |
| | | | | $f_{MX}$ = 10 MHz Note 2, $V_{DD}$ = 5.0 V | Normal operation | Square wave input | | 2.0 | 3.1 | |
| | | | | | | Resonator connection | | 2.1 | 3.2 | |
| | | | | $f_{MX}$ = 10 MHz Note 2, $V_{DD}$ = 3.0 V | Normal operation | Square wave input | | 2.0 | 3.1 | |
| | | | | | | Resonator connection | | 2.1 | 3.2 | |
| | | | LS (low-speed main) mode Note 5 | $f_{MX}$ = 8 MHz Note 2, $V_{DD}$ = 3.0 V | Normal operation | Square wave input | | 1.2 | 1.9 | mA |
| | | | | | | Resonator connection | | 1.2 | 2.0 | |
| | | | | $f_{MX}$ = 8 MHz Note 2, $V_{DD}$ = 2.0 V | Normal operation | Square wave input | | 1.2 | 1.9 | |
| | | | | | | Resonator connection | | 1.2 | 2.0 | |
| | | | Subsystem clock operation | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = -40°C | Normal operation | Square wave input | | 4.7 | 6.1 | µA |
| | | | | | | Resonator connection | | 4.7 | 6.1 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +25°C | Normal operation | Square wave input | | 4.7 | 6.1 | |
| | | | | | | Resonator connection | | 4.7 | 6.1 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +50°C | Normal operation | Square wave input | | 4.8 | 6.7 | |
| | | | | | | Resonator connection | | 4.8 | 6.7 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +70°C | Normal operation | Square wave input | | 4.8 | 7.5 | |
| | | | | | | Resonator connection | | 4.8 | 7.5 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +85°C | Normal operation | Square wave input | | 5.4 | 8.9 | |
| | | | | | | Resonator connection | | 5.4 | 8.9 | |

(**Notes** and **Remarks** are listed on the next page.)

**Note 1.** Total current flowing into $V_{DD}$ and $EV_{DD0}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$, $EV_{DD0}$ or $V_{SS}$, $EV_{SS0}$. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

**Note 2.** When high-speed on-chip oscillator and subsystem clock are stopped.

**Note 3.** When high-speed system clock and subsystem clock are stopped.

**Note 4.** When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.

**Note 5.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 32 MHz
2.4 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 16 MHz
LS (low-speed main) mode: 1.8 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 8 MHz
LV (low-voltage main) mode: 1.6 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 4 MHz

**Remark 1.** $f_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

**Remark 2.** $f_{HOCO}$: High-speed on-chip oscillator clock frequency (64 MHz max.)

**Remark 3.** $f_{IH}$: High-speed on-chip oscillator clock frequency (32 MHz max.)

**Remark 4.** $f_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)

**Remark 5.** Except subsystem clock operation, temperature condition of the TYP. value is $T_A$ = 25°C

### (1) Flash ROM: 16 to 64 KB of 30- to 64-pin products

**($T_A$ = -40 to +85°C, 1.6 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = 0 V)** **(2/2)**

| Parameter | Symbol | Conditions | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|
| Supply current Note 1 | $I_{DD2}$ Note 2 | HALT mode | HS (high-speed main) mode Note 7 | $f_{HOCO}$ = 64 MHz, $f_{IH}$ = 32 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.80 | 3.09 | mA |
| | | | | | $V_{DD}$ = 3.0 V | | 0.80 | 3.09 | |
| | | | | $f_{HOCO}$ = 32 MHz, $f_{IH}$ = 32 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.49 | 2.40 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.49 | 2.40 | |
| | | | | $f_{HOCO}$ = 48 MHz, $f_{IH}$ = 24 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.62 | 2.40 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.62 | 2.40 | |
| | | | | $f_{HOCO}$ = 24 MHz, $f_{IH}$ = 24 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.4 | 1.83 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.4 | 1.83 | |
| | | | | $f_{HOCO}$ = 16 MHz, $f_{IH}$ = 16 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.37 | 1.38 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.37 | 1.38 | |
| | | | LS (low-speed main) mode Note 7 | $f_{HOCO}$ = 8 MHz, $f_{IH}$ = 8 MHz Note 4 | $V_{DD}$ = 3.0 V | | 260 | 710 | μA |
| | | | | | $V_{DD}$ = 2.0 V | | 260 | 710 | |
| | | | LV (low-voltage main) mode Note 7 | $f_{HOCO}$ = 4 MHz, $f_{IH}$ = 4 MHz Note 4 | $V_{DD}$ = 3.0 V | | 420 | 700 | μA |
| | | | | | $V_{DD}$ = 2.0 V | | 420 | 700 | |
| | | | HS (high-speed main) mode Note 7 | $f_{MX}$ = 20 MHz Note 3, $V_{DD}$ = 5.0 V | Square wave input | | 0.28 | 1.55 | mA |
| | | | | | Resonator connection | | 0.40 | 1.74 | |
| | | | | $f_{MX}$ = 20 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 0.28 | 1.55 | |
| | | | | | Resonator connection | | 0.40 | 1.74 | |
| | | | | $f_{MX}$ = 10 MHz Note 3, $V_{DD}$ = 5.0 V | Square wave input | | 0.19 | 0.86 | |
| | | | | | Resonator connection | | 0.25 | 0.93 | |
| | | | | $f_{MX}$ = 10 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 0.19 | 0.86 | |
| | | | | | Resonator connection | | 0.25 | 0.93 | |
| | | | LS (low-speed main) mode Note 7 | $f_{MX}$ = 8 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 95 | 550 | μA |
| | | | | | Resonator connection | | 140 | 590 | |
| | | | | $f_{MX}$ = 8 MHz Note 3, $V_{DD}$ = 2.0 V | Square wave input | | 95 | 550 | |
| | | | | | Resonator connection | | 140 | 590 | |
| | | | Subsystem clock operation | $f_{SUB}$ = 32.768 kHz Note 5, $T_A$ = -40°C | Square wave input | | 0.25 | 0.57 | μA |
| | | | | | Resonator connection | | 0.44 | 0.76 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 5, $T_A$ = +25°C | Square wave input | | 0.30 | 0.57 | |
| | | | | | Resonator connection | | 0.49 | 0.76 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 5, $T_A$ = +50°C | Square wave input | | 0.36 | 1.17 | |
| | | | | | Resonator connection | | 0.59 | 1.36 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 5, $T_A$ = +70°C | Square wave input | | 0.49 | 1.97 | |
| | | | | | Resonator connection | | 0.72 | 2.16 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 5, $T_A$ = +85°C | Square wave input | | 0.97 | 3.37 | |
| | | | | | Resonator connection | | 1.16 | 3.56 | |
| | $I_{DD3}$ Note 6 | STOP mode Note 8 | $T_A$ = -40°C | | | | 0.18 | 0.51 | μA |
| | | | $T_A$ = +25°C | | | | 0.24 | 0.51 | |
| | | | $T_A$ = +50°C | | | | 0.29 | 1.10 | |
| | | | $T_A$ = +70°C | | | | 0.41 | 1.90 | |
| | | | $T_A$ = +85°C | | | | 0.90 | 3.30 | |

(**Notes** and **Remarks** are listed on the next page.)

**Note 1.** Total current flowing into $V_{DD}$ and $EV_{DD0}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$, $EV_{DD0}$ or $V_{SS}$, $EV_{SS0}$. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

**Note 2.** During HALT instruction execution by flash memory.

**Note 3.** When high-speed on-chip oscillator and subsystem clock are stopped.

**Note 4.** When high-speed system clock and subsystem clock are stopped.

**Note 5.** When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.

**Note 6.** Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.

**Note 7.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: $2.7\ V \le V_{DD} \le 5.5\ V$@1 MHz to 32 MHz
$2.4\ V \le V_{DD} \le 5.5\ V$@1 MHz to 16 MHz
LS (low-speed main) mode: $1.8\ V \le V_{DD} \le 5.5\ V$@1 MHz to 8 MHz
LV (low-voltage main) mode: $1.6\ V \le V_{DD} \le 5.5\ V$@1 MHz to 4 MHz

**Note 8.** Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.

**Remark 1.** $f_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

**Remark 2.** $f_{HOCO}$: High-speed on-chip oscillator clock frequency (64 MHz max.)

**Remark 3.** $f_{IH}$: High-speed on-chip oscillator clock frequency (32 MHz max.)

**Remark 4.** $f_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)

**Remark 5.** Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is $T_A$ = 25°C

### (2) Flash ROM: 96 to 256 KB of 30- to 100-pin products

**($T_A$ = -40 to +85°C, 1.6 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V) (1/2)**

| Parameter | Symbol | Conditions | | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| Supply current Note 1 | $I_{DD1}$ | Operating mode | HS (high-speed main) mode Note 5 | $f_{HOCO}$ = 64 MHz, $f_{IH}$ = 32 MHz Note 3 | Basic operation | $V_{DD}$ = 5.0 V | | 2.6 | | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 2.6 | | |
| | | | | $f_{HOCO}$ = 32 MHz, $f_{IH}$ = 32 MHz Note 3 | Basic operation | $V_{DD}$ = 5.0 V | | 2.3 | | |
| | | | | | | $V_{DD}$ = 3.0 V | | 2.3 | | |
| | | | HS (high-speed main) mode Note 5 | $f_{HOCO}$ = 64 MHz, $f_{IH}$ = 32 MHz Note 3 | Normal operation | $V_{DD}$ = 5.0 V | | 5.4 | 10.2 | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 5.4 | 10.2 | |
| | | | | $f_{HOCO}$ = 32 MHz, $f_{IH}$ = 32 MHz Note 3 | Normal operation | $V_{DD}$ = 5.0 V | | 5.0 | 9.6 | |
| | | | | | | $V_{DD}$ = 3.0 V | | 5.0 | 9.6 | |
| | | | | $f_{HOCO}$ = 48 MHz, $f_{IH}$ = 24 MHz Note 3 | Normal operation | $V_{DD}$ = 5.0 V | | 4.2 | 7.8 | |
| | | | | | | $V_{DD}$ = 3.0 V | | 4.2 | 7.8 | |
| | | | | $f_{HOCO}$ = 24 MHz, $f_{IH}$ = 24 MHz Note 3 | Normal operation | $V_{DD}$ = 5.0 V | | 4.0 | 7.4 | |
| | | | | | | $V_{DD}$ = 3.0 V | | 4.0 | 7.4 | |
| | | | | $f_{HOCO}$ = 16 MHz, $f_{IH}$ = 16 MHz Note 3 | Normal operation | $V_{DD}$ = 5.0 V | | 3.0 | 5.3 | |
| | | | | | | $V_{DD}$ = 3.0 V | | 3.0 | 5.3 | |
| | | | LS (low-speed main) mode Note 5 | $f_{HOCO}$ = 8 MHz, $f_{IH}$ = 8 MHz Note 3 | Normal operation | $V_{DD}$ = 3.0 V | | 1.4 | 2.3 | mA |
| | | | | | | $V_{DD}$ = 2.0 V | | 1.4 | 2.3 | |
| | | | LV (low-voltage main) mode Note 5 | $f_{HOCO}$ = 4 MHz, $f_{IH}$ = 4 MHz Note 3 | Normal operation | $V_{DD}$ = 3.0 V | | 1.3 | 1.9 | mA |
| | | | | | | $V_{DD}$ = 2.0 V | | 1.3 | 1.9 | |
| | | | HS (high-speed main) mode Note 5 | $f_{MX}$ = 20 MHz Note 2, $V_{DD}$ = 5.0 V | Normal operation | Square wave input | | 3.4 | 6.2 | mA |
| | | | | | | Resonator connection | | 3.6 | 6.4 | |
| | | | | $f_{MX}$ = 20 MHz Note 2, $V_{DD}$ = 3.0 V | Normal operation | Square wave input | | 3.4 | 6.2 | |
| | | | | | | Resonator connection | | 3.6 | 6.4 | |
| | | | | $f_{MX}$ = 10 MHz Note 2, $V_{DD}$ = 5.0 V | Normal operation | Square wave input | | 2.1 | 3.6 | |
| | | | | | | Resonator connection | | 2.2 | 3.7 | |
| | | | | $f_{MX}$ = 10 MHz Note 2, $V_{DD}$ = 3.0 V | Normal operation | Square wave input | | 2.1 | 3.6 | |
| | | | | | | Resonator connection | | 2.2 | 3.7 | |
| | | | LS (low-speed main) mode Note 5 | $f_{MX}$ = 8 MHz Note 2, $V_{DD}$ = 3.0 V | Normal operation | Square wave input | | 1.2 | 2.2 | mA |
| | | | | | | Resonator connection | | 1.2 | 2.3 | |
| | | | | $f_{MX}$ = 8 MHz Note 2, $V_{DD}$ = 2.0 V | Normal operation | Square wave input | | 1.2 | 2.2 | |
| | | | | | | Resonator connection | | 1.2 | 2.3 | |
| | | | Subsystem clock operation | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = -40°C | Normal operation | Square wave input | | 4.9 | 7.1 | µA |
| | | | | | | Resonator connection | | 4.9 | 7.1 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +25°C | Normal operation | Square wave input | | 4.9 | 7.1 | |
| | | | | | | Resonator connection | | 4.9 | 7.1 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +50°C | Normal operation | Square wave input | | 5.1 | 8.8 | |
| | | | | | | Resonator connection | | 5.1 | 8.8 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +70°C | Normal operation | Square wave input | | 5.5 | 10.5 | |
| | | | | | | Resonator connection | | 5.5 | 10.5 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +85°C | Normal operation | Square wave input | | 6.5 | 14.5 | |
| | | | | | | Resonator connection | | 6.5 | 14.5 | |

(**Notes** and **Remarks** are listed on the next page.)

**Note 1.** Total current flowing into $V_{DD}$, $EV_{DD0}$, and $EV_{DD1}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$, $EV_{DD0}$, and $EV_{DD1}$, or $V_{SS}$, $EV_{SS0}$, and $EV_{SS1}$. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, D/A converter, comparator, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

**Note 2.** When high-speed on-chip oscillator and subsystem clock are stopped.

**Note 3.** When high-speed system clock and subsystem clock are stopped.

**Note 4.** When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the 12-bit interval timer and watchdog timer.

**Note 5.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 32 MHz
2.4 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 16 MHz
LS (low-speed main) mode: 1.8 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 8 MHz
LV (low-voltage main) mode: 1.6 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 4 MHz

**Remark 1.** $f_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

**Remark 2.** $f_{HOCO}$: High-speed on-chip oscillator clock frequency (64 MHz max.)

**Remark 3.** $f_{IH}$: High-speed on-chip oscillator clock frequency (32 MHz max.)

**Remark 4.** $f_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)

**Remark 5.** Except subsystem clock operation, temperature condition of the TYP. value is $T_A$ = 25°C

### (2) Flash ROM: 96 to 256 KB of 30- to 100-pin products

**($T_A$ = -40 to +85°C, 1.6 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)** **(2/2)**

| Parameter | Symbol | Conditions | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|
| Supply current Note 1 | $I_{DD2}$ Note 2 | HALT mode | HS (high-speed main) mode Note 7 | $f_{HOCO}$ = 64 MHz, $f_{IH}$ = 32 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.79 | 3.32 | mA |
| | | | | | $V_{DD}$ = 3.0 V | | 0.79 | 3.32 | |
| | | | | $f_{HOCO}$ = 32 MHz, $f_{IH}$ = 32 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.49 | 2.63 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.49 | 2.63 | |
| | | | | $f_{HOCO}$ = 48 MHz, $f_{IH}$ = 24 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.62 | 2.57 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.62 | 2.57 | |
| | | | | $f_{HOCO}$ = 24 MHz, $f_{IH}$ = 24 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.4 | 2.00 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.4 | 2.00 | |
| | | | | $f_{HOCO}$ = 16 MHz, $f_{IH}$ = 16 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.38 | 1.49 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.38 | 1.49 | |
| | | | LS (low-speed main) mode Note 7 | $f_{HOCO}$ = 8 MHz, $f_{IH}$ = 8 MHz Note 4 | $V_{DD}$ = 3.0 V | | 250 | 800 | μA |
| | | | | | $V_{DD}$ = 2.0 V | | 250 | 800 | |
| | | | LV (low-voltage main) mode Note 7 | $f_{HOCO}$ = 4 MHz, $f_{IH}$ = 4 MHz Note 4 | $V_{DD}$ = 3.0 V | | 420 | 755 | μA |
| | | | | | $V_{DD}$ = 2.0 V | | 420 | 755 | |
| | | | HS (high-speed main) mode Note 7 | $f_{MX}$ = 20 MHz Note 3, $V_{DD}$ = 5.0 V | Square wave input | | 0.30 | 1.63 | mA |
| | | | | | Resonator connection | | 0.40 | 1.85 | |
| | | | | $f_{MX}$ = 20 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 0.30 | 1.63 | |
| | | | | | Resonator connection | | 0.40 | 1.85 | |
| | | | | $f_{MX}$ = 10 MHz Note 3, $V_{DD}$ = 5.0 V | Square wave input | | 0.20 | 0.89 | |
| | | | | | Resonator connection | | 0.25 | 0.97 | |
| | | | | $f_{MX}$ = 10 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 0.20 | 0.89 | |
| | | | | | Resonator connection | | 0.25 | 0.97 | |
| | | | LS (low-speed main) mode Note 7 | $f_{MX}$ = 8 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 110 | 580 | μA |
| | | | | | Resonator connection | | 140 | 630 | |
| | | | | $f_{MX}$ = 8 MHz Note 3, $V_{DD}$ = 2.0 V | Square wave input | | 110 | 580 | |
| | | | | | Resonator connection | | 140 | 630 | |
| | | | Subsystem clock operation | $f_{SUB}$ = 32.768 kHz Note 5, $T_A$ = -40°C | Square wave input | | 0.28 | 0.66 | μA |
| | | | | | Resonator connection | | 0.47 | 0.85 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 5, $T_A$ = +25°C | Square wave input | | 0.34 | 0.66 | |
| | | | | | Resonator connection | | 0.53 | 0.85 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 5, $T_A$ = +50°C | Square wave input | | 0.37 | 2.35 | |
| | | | | | Resonator connection | | 0.56 | 2.54 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 5, $T_A$ = +70°C | Square wave input | | 0.61 | 4.08 | |
| | | | | | Resonator connection | | 0.80 | 4.27 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 5, $T_A$ = +85°C | Square wave input | | 1.55 | 8.09 | |
| | | | | | Resonator connection | | 1.74 | 8.28 | |
| | $I_{DD3}$ Note 6 | STOP mode Note 8 | $T_A$ = -40°C | | | | 0.19 | 0.57 | μA |
| | | | $T_A$ = +25°C | | | | 0.25 | 0.57 | |
| | | | $T_A$ = +50°C | | | | 0.33 | 2.26 | |
| | | | $T_A$ = +70°C | | | | 0.52 | 3.99 | |
| | | | $T_A$ = +85°C | | | | 1.46 | 8.00 | |

(**Notes** and **Remarks** are listed on the next page.)

**Note 1.** Total current flowing into $V_{DD}$, $EV_{DD0}$, and $EV_{DD1}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$, $EV_{DD0}$, and $EV_{DD1}$, or $V_{SS}$, $EV_{SS0}$, and $EV_{SS1}$. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, D/A converter, comparator, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

**Note 2.** During HALT instruction execution by flash memory.

**Note 3.** When high-speed on-chip oscillator and subsystem clock are stopped.

**Note 4.** When high-speed system clock and subsystem clock are stopped.

**Note 5.** When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.

**Note 6.** Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.

**Note 7.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 32 MHz
2.4 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 16 MHz
LS (low-speed main) mode: 1.8 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 8 MHz
LV (low-voltage main) mode: 1.6 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 4 MHz

**Note 8.** Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.

**Remark 1.** $f_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

**Remark 2.** $f_{HOCO}$: High-speed on-chip oscillator clock frequency (64 MHz max.)

**Remark 3.** $f_{IH}$: High-speed on-chip oscillator clock frequency (32 MHz max.)

**Remark 4.** $f_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)

**Remark 5.** Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is $T_A$ = 25°C

### (3) Flash ROM: 384 to 512 KB of 48- to 100-pin products

**($T_A$ = -40 to +85°C, 1.6 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V) (1/2)**

| Parameter | Symbol | Conditions | | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| Supply current Note 1 | $I_{DD1}$ | Operating mode | HS (high-speed main) mode Note 5 | $f_{HOCO}$ = 64 MHz, $f_{IH}$ = 32 MHz Note 3 | Basic operation | $V_{DD}$ = 5.0 V | | 2.9 | | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 2.9 | | |
| | | | | $f_{HOCO}$ = 32 MHz, $f_{IH}$ = 32 MHz Note 3 | Basic operation | $V_{DD}$ = 5.0 V | | 2.5 | | |
| | | | | | | $V_{DD}$ = 3.0 V | | 2.5 | | |
| | | | HS (high-speed main) mode Note 5 | $f_{HOCO}$ = 64 MHz, $f_{IH}$ = 32 MHz Note 3 | Normal operation | $V_{DD}$ = 5.0 V | | 6.0 | 11.2 | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 6.0 | 11.2 | |
| | | | | $f_{HOCO}$ = 32 MHz, $f_{IH}$ = 32 MHz Note 3 | Normal operation | $V_{DD}$ = 5.0 V | | 5.5 | 10.6 | |
| | | | | | | $V_{DD}$ = 3.0 V | | 5.5 | 10.6 | |
| | | | | $f_{HOCO}$ = 48 MHz, $f_{IH}$ = 24 MHz Note 3 | Normal operation | $V_{DD}$ = 5.0 V | | 4.7 | 8.6 | |
| | | | | | | $V_{DD}$ = 3.0 V | | 4.7 | 8.6 | |
| | | | | $f_{HOCO}$ = 24 MHz, $f_{IH}$ = 24 MHz Note 3 | Normal operation | $V_{DD}$ = 5.0 V | | 4.4 | 8.2 | |
| | | | | | | $V_{DD}$ = 3.0 V | | 4.4 | 8.2 | |
| | | | | $f_{HOCO}$ = 16 MHz, $f_{IH}$ = 16 MHz Note 3 | Normal operation | $V_{DD}$ = 5.0 V | | 3.3 | 5.9 | |
| | | | | | | $V_{DD}$ = 3.0 V | | 3.3 | 5.9 | |
| | | | LS (low-speed main) mode Note 5 | $f_{HOCO}$ = 8 MHz, $f_{IH}$ = 8 MHz Note 3 | Normal operation | $V_{DD}$ = 3.0 V | | 1.5 | 2.5 | mA |
| | | | | | | $V_{DD}$ = 2.0 V | | 1.5 | 2.5 | |
| | | | LV (low-voltage main) mode Note 5 | $f_{HOCO}$ = 4 MHz, $f_{IH}$ = 4 MHz Note 3 | Normal operation | $V_{DD}$ = 3.0 V | | 1.5 | 2.1 | mA |
| | | | | | | $V_{DD}$ = 2.0 V | | 1.5 | 2.1 | |
| | | | HS (high-speed main) mode Note 5 | $f_{MX}$ = 20 MHz Note 2, $V_{DD}$ = 5.0 V | Normal operation | Square wave input | | 3.7 | 6.8 | mA |
| | | | | | | Resonator connection | | 3.9 | 7.0 | |
| | | | | $f_{MX}$ = 20 MHz Note 2, $V_{DD}$ = 3.0 V | Normal operation | Square wave input | | 3.7 | 6.8 | |
| | | | | | | Resonator connection | | 3.9 | 7.0 | |
| | | | | $f_{MX}$ = 10 MHz Note 2, $V_{DD}$ = 5.0 V | Normal operation | Square wave input | | 2.3 | 4.1 | |
| | | | | | | Resonator connection | | 2.3 | 4.2 | |
| | | | | $f_{MX}$ = 10 MHz Note 2, $V_{DD}$ = 3.0 V | Normal operation | Square wave input | | 2.3 | 4.1 | |
| | | | | | | Resonator connection | | 2.3 | 4.2 | |
| | | | LS (low-speed main) mode Note 5 | $f_{MX}$ = 8 MHz Note 2, $V_{DD}$ = 3.0 V | Normal operation | Square wave input | | 1.4 | 2.4 | mA |
| | | | | | | Resonator connection | | 1.4 | 2.5 | |
| | | | | $f_{MX}$ = 8 MHz Note 2, $V_{DD}$ = 2.0 V | Normal operation | Square wave input | | 1.4 | 2.4 | |
| | | | | | | Resonator connection | | 1.4 | 2.5 | |
| | | | Subsystem clock operation | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = -40°C | Normal operation | Square wave input | | 5.2 | | µA |
| | | | | | | Resonator connection | | 5.2 | | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +25°C | Normal operation | Square wave input | | 5.3 | 7.7 | |
| | | | | | | Resonator connection | | 5.3 | 7.7 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +50°C | Normal operation | Square wave input | | 5.5 | 10.6 | |
| | | | | | | Resonator connection | | 5.5 | 10.6 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +70°C | Normal operation | Square wave input | | 5.9 | 13.2 | |
| | | | | | | Resonator connection | | 6.0 | 13.2 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +85°C | Normal operation | Square wave input | | 6.8 | 17.5 | |
| | | | | | | Resonator connection | | 6.9 | 17.5 | |

(**Notes** and **Remarks** are listed on the next page.)

**Note 1.** Total current flowing into $V_{DD}$, $EV_{DD0}$, and $EV_{DD1}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$, $EV_{DD0}$, and $EV_{DD1}$, or $V_{SS}$, $EV_{SS0}$, and $EV_{SS1}$. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, D/A converter, comparator, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

**Note 2.** When high-speed on-chip oscillator and subsystem clock are stopped.

**Note 3.** When high-speed system clock and subsystem clock are stopped.

**Note 4.** When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the 12-bit interval timer and watchdog timer.

**Note 5.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 32 MHz
2.4 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 16 MHz
LS (low-speed main) mode: 1.8 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 8 MHz
LV (low-voltage main) mode: 1.6 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 4 MHz

**Remark 1.** $f_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

**Remark 2.** $f_{HOCO}$: High-speed on-chip oscillator clock frequency (64 MHz max.)

**Remark 3.** $f_{IH}$: High-speed on-chip oscillator clock frequency (32 MHz max.)

**Remark 4.** $f_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)

**Remark 5.** Except subsystem clock operation, temperature condition of the TYP. value is $T_A$ = 25°C

### (3) Flash ROM: 384 to 512 KB of 48- to 100-pin products

**($T_A$ = -40 to +85°C, 1.6 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)** **(2/2)**

| Parameter | Symbol | Conditions | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|
| Supply current Note 1 | $I_{DD2}$ Note 2 | HALT mode | HS (high-speed main) mode Note 7 | $f_{HOCO}$ = 64 MHz, $f_{IH}$ = 32 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.93 | 3.32 | mA |
| | | | | | $V_{DD}$ = 3.0 V | | 0.93 | 3.32 | |
| | | | | $f_{HOCO}$ = 32 MHz, $f_{IH}$ = 32 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.5 | 2.63 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.5 | 2.63 | |
| | | | | $f_{HOCO}$ = 48 MHz, $f_{IH}$ = 24 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.72 | 2.60 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.72 | 2.60 | |
| | | | | $f_{HOCO}$ = 24 MHz, $f_{IH}$ = 24 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.42 | 2.03 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.42 | 2.03 | |
| | | | | $f_{HOCO}$ = 16 MHz, $f_{IH}$ = 16 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.39 | 1.50 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.39 | 1.50 | |
| | | | LS (low-speed main) mode Note 7 | $f_{HOCO}$ = 8 MHz, $f_{IH}$ = 8 MHz Note 4 | $V_{DD}$ = 3.0 V | | 270 | 800 | μA |
| | | | | | $V_{DD}$ = 2.0 V | | 270 | 800 | |
| | | | LV (low-voltage main) mode Note 7 | $f_{HOCO}$ = 4 MHz, $f_{IH}$ = 4 MHz Note 4 | $V_{DD}$ = 3.0 V | | 450 | 755 | μA |
| | | | | | $V_{DD}$ = 2.0 V | | 450 | 755 | |
| | | | HS (high-speed main) mode Note 7 | $f_{MX}$ = 20 MHz Note 3, $V_{DD}$ = 5.0 V | Square wave input | | 0.31 | 1.69 | mA |
| | | | | | Resonator connection | | 0.41 | 1.91 | |
| | | | | $f_{MX}$ = 20 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 0.31 | 1.69 | |
| | | | | | Resonator connection | | 0.41 | 1.91 | |
| | | | | $f_{MX}$ = 10 MHz Note 3, $V_{DD}$ = 5.0 V | Square wave input | | 0.21 | 0.94 | |
| | | | | | Resonator connection | | 0.26 | 1.02 | |
| | | | | $f_{MX}$ = 10 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 0.21 | 0.94 | |
| | | | | | Resonator connection | | 0.26 | 1.02 | |
| | | | LS (low-speed main) mode Note 7 | $f_{MX}$ = 8 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 110 | 610 | μA |
| | | | | | Resonator connection | | 150 | 660 | |
| | | | | $f_{MX}$ = 8 MHz Note 3, $V_{DD}$ = 2.0 V | Square wave input | | 110 | 610 | |
| | | | | | Resonator connection | | 150 | 660 | |
| | | | Subsystem clock operation | $f_{SUB}$ = 32.768 kHz Note 5, $T_A$ = -40°C | Square wave input | | 0.31 | | μA |
| | | | | | Resonator connection | | 0.50 | | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 5, $T_A$ = +25°C | Square wave input | | 0.38 | 0.76 | |
| | | | | | Resonator connection | | 0.57 | 0.95 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 5, $T_A$ = +50°C | Square wave input | | 0.47 | 3.59 | |
| | | | | | Resonator connection | | 0.70 | 3.78 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 5, $T_A$ = +70°C | Square wave input | | 0.80 | 6.20 | |
| | | | | | Resonator connection | | 1.00 | 6.39 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 5, $T_A$ = +85°C | Square wave input | | 1.65 | 10.56 | |
| | | | | | Resonator connection | | 1.84 | 10.75 | |
| | $I_{DD3}$ Note 6 | STOP mode Note 8 | $T_A$ = -40°C | | | | 0.19 | | μA |
| | | | $T_A$ = +25°C | | | | 0.30 | 0.59 | |
| | | | $T_A$ = +50°C | | | | 0.41 | 3.42 | |
| | | | $T_A$ = +70°C | | | | 0.80 | 6.03 | |
| | | | $T_A$ = +85°C | | | | 1.53 | 10.39 | |

(**Notes** and **Remarks** are listed on the next page.)

**Note 1.** Total current flowing into $V_{DD}$, $EV_{DD0}$, and $EV_{DD1}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$, $EV_{DD0}$, and $EV_{DD1}$, or $V_{SS}$, $EV_{SS0}$, and $EV_{SS1}$. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, D/A converter, comparator, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

**Note 2.** During HALT instruction execution by flash memory.

**Note 3.** When high-speed on-chip oscillator and subsystem clock are stopped.

**Note 4.** When high-speed system clock and subsystem clock are stopped.

**Note 5.** When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.

**Note 6.** Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.

**Note 7.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 32 MHz
2.4 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 16 MHz
LS (low-speed main) mode: 1.8 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 8 MHz
LV (low-voltage main) mode: 1.6 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 4 MHz

**Note 8.** Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.

**Remark 1.** $f_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

**Remark 2.** $f_{HOCO}$: High-speed on-chip oscillator clock frequency (64 MHz max.)

**Remark 3.** $f_{IH}$: High-speed on-chip oscillator clock frequency (32 MHz max.)

**Remark 4.** $f_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)

**Remark 5.** Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is $T_A$ = 25°C

### (4) Peripheral Functions (Common to all products)

**($T_A$ = -40 to +85°C, 1.6 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Low-speed on-chip oscillator operating current | $I_{FIL}$ Note 1 | | | | 0.20 | | μA |
| RTC operating current | $I_{RTC}$ Notes 1, 2, 3 | | | | 0.02 | | μA |
| 12-bit interval timer operating current | $I_{IT}$ Notes 1, 2, 4 | | | | 0.02 | | μA |
| Watchdog timer operating current | $I_{WDT}$ Notes 1, 2, 5 | $f_{IL}$ = 15 kHz | | | 0.22 | | μA |
| A/D converter operating current | $I_{ADC}$ Notes 1, 6 | When conversion at maximum speed | Normal mode, $AV_{REFP}$ = $V_{DD}$ = 5.0 V | | 1.3 | 1.7 | mA |
| | | | Low voltage mode, $AV_{REFP}$ = $V_{DD}$ = 3.0 V | | 0.5 | 0.7 | mA |
| A/D converter reference voltage current | $I_{ADREF}$ Note 1 | | | | 75.0 | | μA |
| Temperature sensor operating current | $I_{TMPS}$ Note 1 | | | | 75.0 | | μA |
| D/A converter operating current | $I_{DAC}$ Notes 1, 11, 13 | Per D/A converter channel | | | | 1.5 | mA |
| Comparator operating current | $I_{CMP}$ Notes 1, 12, 13 | $V_{DD}$ = 5.0 V, Regulator output voltage = 2.1 V | Window mode | | 12.5 | | μA |
| | | | Comparator high-speed mode | | 6.5 | | μA |
| | | | Comparator low-speed mode | | 1.7 | | μA |
| | | $V_{DD}$ = 5.0 V, Regulator output voltage = 1.8 V | Window mode | | 8.0 | | μA |
| | | | Comparator high-speed mode | | 4.0 | | μA |
| | | | Comparator low-speed mode | | 1.3 | | μA |
| LVD operating current | $I_{LVD}$ Notes 1, 7 | | | | 0.08 | | μA |
| Self-programming operating current | $I_{FSP}$ Notes 1, 9 | | | | 2.50 | 12.20 | mA |
| BGO operating current | $I_{BGO}$ Notes 1, 8 | | | | 2.50 | 12.20 | mA |
| SNOOZE operating current | $I_{SNOZ}$ Note 1 | ADC operation | The mode is performed Note 10 | | 0.50 | 0.60 | mA |
| | | | The A/D conversion operations are performed, Low voltage mode, $AV_{REFP}$ = $V_{DD}$ = 3.0 V | | 1.20 | 1.44 | |
| | | CSI/UART operation | | | 0.70 | 0.84 | |
| | | DTC operation | | | 3.10 | | |

**Note 1.** Current flowing to $V_{DD}$.

**Note 2.** When high speed on-chip oscillator and high-speed system clock are stopped.

**Note 3.** Current flowing only to the real-time clock (RTC) (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either $I_{DD1}$ or $I_{DD2}$, and $I_{RTC}$, when the real-time clock operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, $I_{FIL}$ should be added. $I_{DD2}$ subsystem clock operation includes the operational current of the real-time clock.

**Note 4.** Current flowing only to the 12-bit interval timer (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either $I_{DD1}$ or $I_{DD2}$, and $I_{IT}$, when the 12-bit interval timer operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, $I_{FIL}$ should be added.

**Note 5.** Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The supply current of the RL78 microcontrollers is the sum of $I_{DD1}$, $I_{DD2}$ or $I_{DD3}$ and $I_{WDT}$ when the watchdog timer is in operation.

**Note 6.** Current flowing only to the A/D converter. The supply current of the RL78 microcontrollers is the sum of $I_{DD1}$ or $I_{DD2}$ and $I_{ADC}$ when the A/D converter operates in an operation mode or the HALT mode.

**Note 7.** Current flowing only to the LVD circuit. The supply current of the RL78 microcontrollers is the sum of $I_{DD1}$, $I_{DD2}$ or $I_{DD3}$ and $I_{LVD}$ when the LVD circuit is in operation.

**Note 8.** Current flowing during programming of the data flash.

**Note 9.** Current flowing during self-programming.

**Note 10.** For shift time to the SNOOZE mode, see **23.3.3 SNOOZE mode** in the RL78/G14 User's Manual.

**Note 11.** Current flowing only to the D/A converter. The supply current of the RL78 microcontrollers is the sum of $I_{DD1}$ or $I_{DD2}$ and $I_{DAC}$ when the D/A converter operates in an operation mode or the HALT mode.

**Note 12.** Current flowing only to the comparator circuit. The supply current of the RL78 microcontrollers is the sum of $I_{DD1}$, $I_{DD2}$, or $I_{DD3}$ and $I_{CMP}$ when the comparator circuit is in operation.

**Note 13.** A comparator and D/A converter are provided in products with 96 KB or more code flash memory.

**Remark 1.** $f_{IL}$: Low-speed on-chip oscillator clock frequency

**Remark 2.** $f_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)

**Remark 3.** $f_{CLK}$: CPU/peripheral hardware clock frequency

**Remark 4.** Temperature condition of the TYP. value is $T_A$ = 25°C

## 2.4 AC Characteristics

**($T_A$ = -40 to +85°C, 1.6 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)** **(1/2)**

| Items | Symbol | Conditions | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|
| Instruction cycle (minimum instruction execution time) | $T_{CY}$ | Main system clock ($f_{MAIN}$) operation | HS (high-speed main) mode | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 0.03125 | | 1 | μs |
| | | | | 2.4 V ≤ $V_{DD}$ < 2.7 V | 0.0625 | | 1 | μs |
| | | | LS (low-speed main) mode | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | 0.125 | | 1 | μs |
| | | | LV (low-voltage main) mode | 1.6 V ≤ $V_{DD}$ ≤ 5.5 V | 0.25 | | 1 | μs |
| | | Subsystem clock ($f_{SUB}$) operation | | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | 28.5 | 30.5 | 31.3 | μs |
| | | In the self-programming mode | HS (high-speed main) mode | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 0.03125 | | 1 | μs |
| | | | | 2.4 V ≤ $V_{DD}$ < 2.7 V | 0.0625 | | 1 | μs |
| | | | LS (low-speed main) mode | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | 0.125 | | 1 | μs |
| | | | LV (low-voltage main) mode | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | 0.25 | | 1 | μs |
| External system clock frequency | $f_{EX}$ | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | | | 1.0 | | 20.0 | MHz |
| | | 2.4 V ≤ $V_{DD}$ ≤ 2.7 V | | | 1.0 | | 16.0 | MHz |
| | | 1.8 V ≤ $V_{DD}$ < 2.4 V | | | 1.0 | | 8.0 | MHz |
| | | 1.6 V ≤ $V_{DD}$ < 1.8 V | | | 1.0 | | 4.0 | MHz |
| | $f_{EXS}$ | | | | 32 | | 35 | kHz |
| External system clock input high-level width, low-level width | $t_{EXH}$, $t_{EXL}$ | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | | | 24 | | | ns |
| | | 2.4 V ≤ $V_{DD}$ ≤ 2.7 V | | | 30 | | | ns |
| | | 1.8 V ≤ $V_{DD}$ < 2.4 V | | | 60 | | | ns |
| | | 1.6 V ≤ $V_{DD}$ < 1.8 V | | | 120 | | | ns |
| | $t_{EXHS}$, $t_{EXLS}$ | | | | 13.7 | | | μs |
| TI00 to TI03, TI10 to TI13 input high-level width, low-level width | $t_{TIH}$, $t_{TIL}$ | | | | 1/$f_{MCK}$ + 10 Note | | | ns |
| Timer RJ input cycle | $f_C$ | TRJIO | | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | 100 | | | ns |
| | | | | 1.8 V ≤ $EV_{DD0}$ < 2.7 V | 300 | | | ns |
| | | | | 1.6 V ≤ $EV_{DD0}$ < 1.8 V | 500 | | | ns |
| Timer RJ input high-level width, low-level width | $t_{TJIH}$, $t_{TJIL}$ | TRJIO | | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | 40 | | | ns |
| | | | | 1.8 V ≤ $EV_{DD0}$ < 2.7 V | 120 | | | ns |
| | | | | 1.6 V ≤ $EV_{DD0}$ < 1.8 V | 200 | | | ns |

**Note** The following conditions are required for low voltage interface when $EV_{DD0}$ < $V_{DD}$
1.8 V ≤ $EV_{DD0}$ < 2.7 V: MIN. 125 ns
1.6 V ≤ $EV_{DD0}$ < 1.8 V: MIN. 250 ns

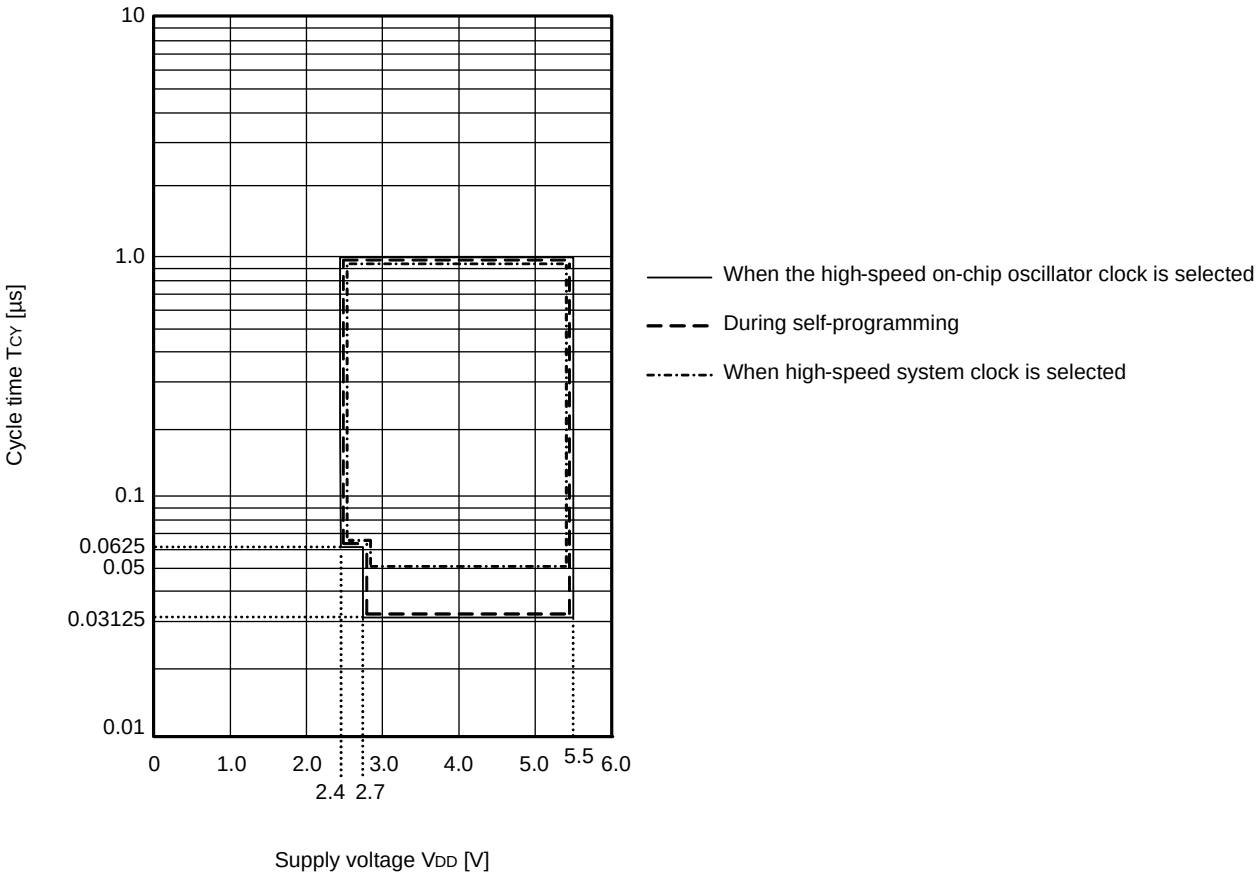
**Remark** $f_{MCK}$: Timer array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of timer mode register mn (TMRmn). m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3))

**($T_A$ = -40 to +85°C, 1.6 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)** **(2/2)**

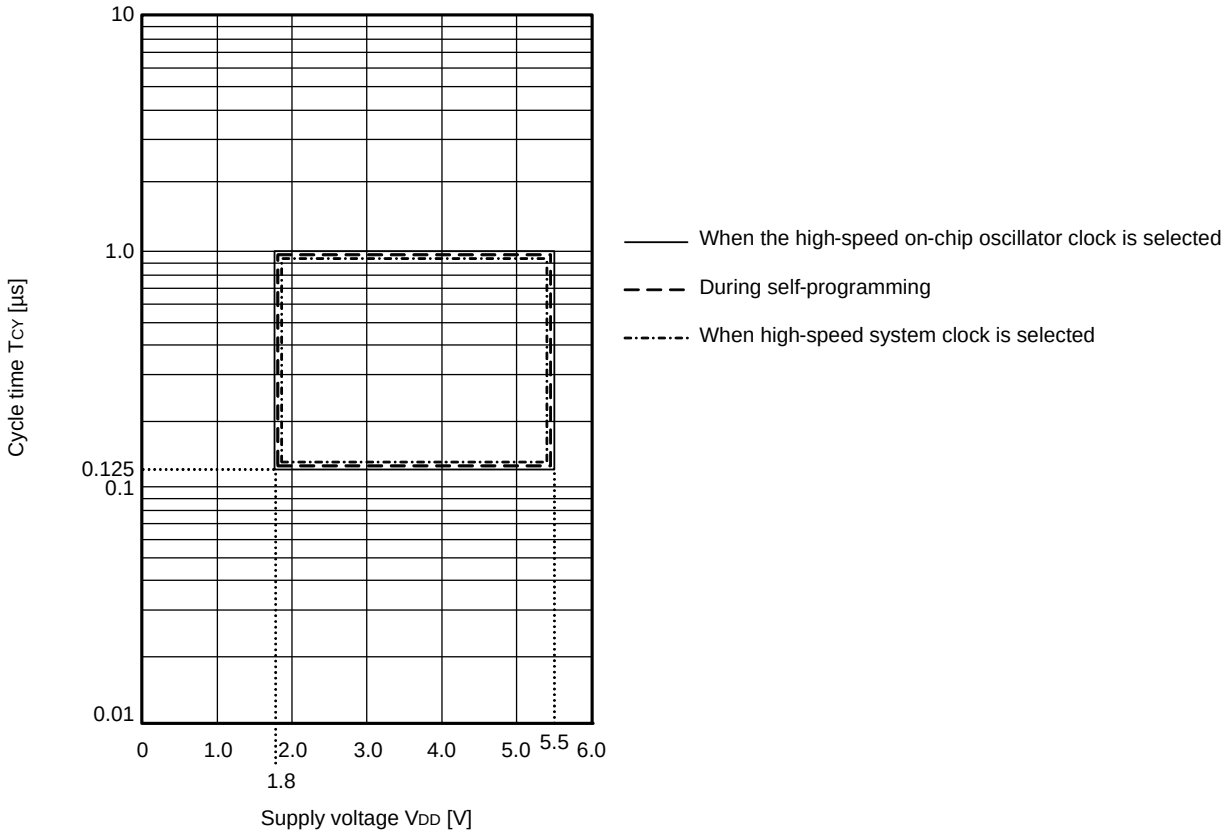
| Items | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Timer RD input high-level width, low-level width | $t_{TDIH}$, $t_{TDIL}$ | TRDIOA0, TRDIOA1, TRDIOB0, TRDIOB1, TRDIOC0, TRDIOC1, TRDIOD0, TRDIOD1 | | 3/$f_{CLK}$ | | | ns |
| Timer RD forced cutoff signal input low-level width | $t_{TDSIL}$ | P130/INTP0 | 2MHz < $f_{CLK}$ ≤ 32 MHz | 1 | | | µs |
| | | | $f_{CLK}$ ≤ 2 MHz | 1/$f_{CLK}$ + 1 | | | |
| Timer RG input high-level width, low-level width | $t_{TGIH}$, $t_{TGIL}$ | TRGIOA, TRGIOB | | 2.5/$f_{CLK}$ | | | ns |
| TO00 to TO03, TO10 to TO13, TRJIO0, TRJO0, TRDIOA0, TRDIOA1, TRDIOB0, TRDIOB1, TRDIOC0, TRDIOC1, TRDIOD0, TRDIOD1, TRGIOA, TRGIOB output frequency | $f_{TO}$ | HS (high-speed main) mode | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V | | | 16 | MHz |
| | | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V | | | 8 | MHz |
| | | | 1.8 V ≤ $EV_{DD0}$ < 2.7 V | | | 4 | MHz |
| | | | 1.6 V ≤ $EV_{DD0}$ < 1.8 V | | | 2 | MHz |
| | | LS (low-speed main) mode | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | | | 4 | MHz |
| | | | 1.6 V ≤ $EV_{DD0}$ < 1.8 V | | | 2 | MHz |
| | | LV (low-voltage main) mode | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V | | | 2 | MHz |
| PCLBUZ0, PCLBUZ1 output frequency | $f_{PCL}$ | HS (high-speed main) mode | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V | | | 16 | MHz |
| | | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V | | | 8 | MHz |
| | | | 1.8 V ≤ $EV_{DD0}$ < 2.7 V | | | 4 | MHz |
| | | | 1.6 V ≤ $EV_{DD0}$ < 1.8 V | | | 2 | MHz |
| | | LS (low-speed main) mode | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | | | 4 | MHz |
| | | | 1.6 V ≤ $EV_{DD0}$ < 1.8 V | | | 2 | MHz |
| | | LV (low-voltage main) mode | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | | | 4 | MHz |
| | | | 1.6 V ≤ $EV_{DD0}$ < 1.8 V | | | 2 | MHz |
| Interrupt input high-level width, low-level width | $t_{INTH}$, $t_{INTL}$ | INTP0 | 1.6 V ≤ $V_{DD}$ ≤ 5.5 V | 1 | | | µs |
| | | INTP1 to INTP11 | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V | 1 | | | µs |
| Key interrupt input low-level width | $t_{KR}$ | KR0 to KR7 | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | 250 | | | ns |
| | | | 1.6 V ≤ $EV_{DD0}$ < 1.8 V | 1 | | | µs |
| $\overline{\text{RESET}}$ low-level width | $t_{RSL}$ | | | 10 | | | µs |

Minimum Instruction Execution Time during Main System Clock Operation

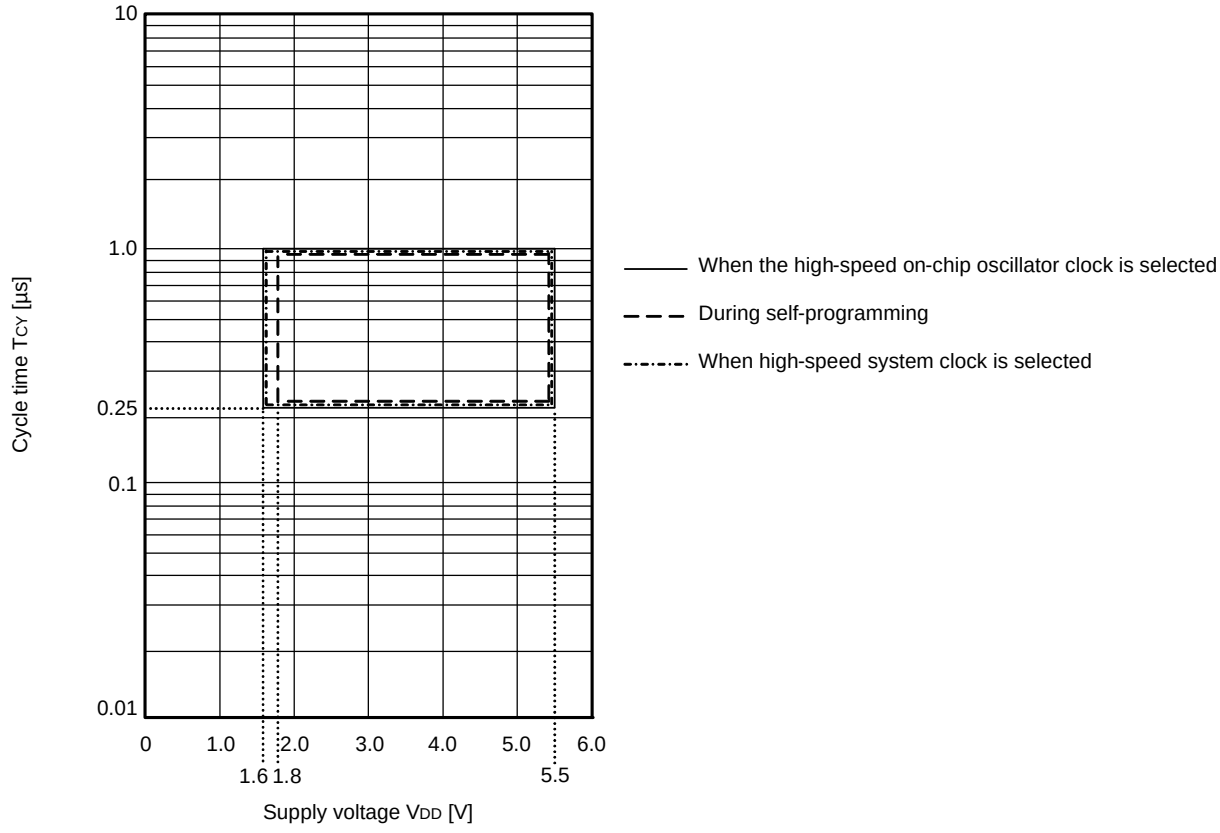
$T_{CY}$ vs $V_{DD}$ (HS (high-speed main) mode)



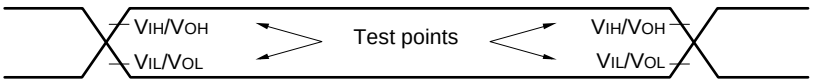
$T_{CY}$ vs $V_{DD}$ (LS (low-speed main) mode)



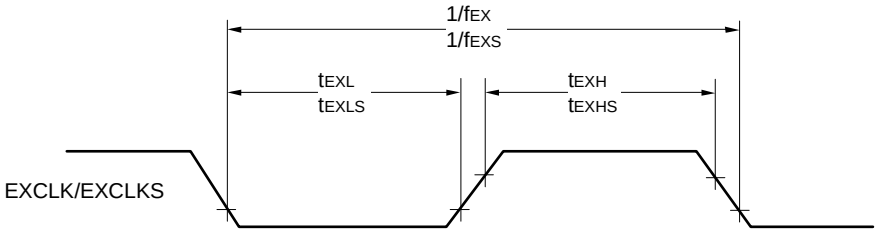

$T_{CY}$ vs $V_{DD}$ (LV (low-voltage main) mode)



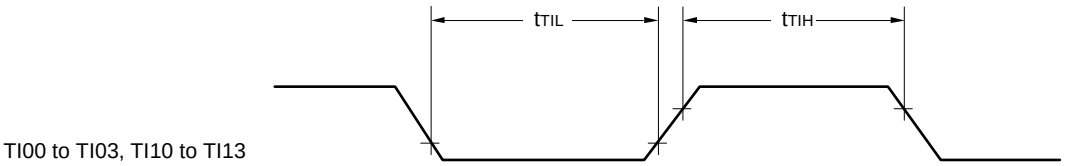
AC Timing Test Points

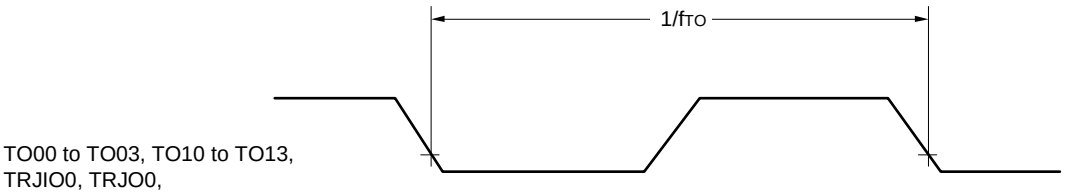


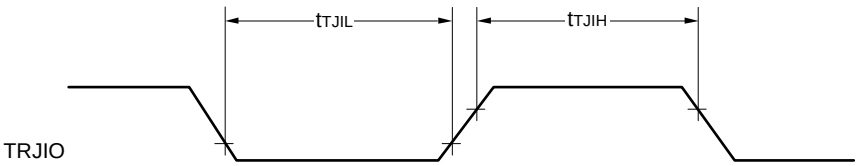

External System Clock Timing

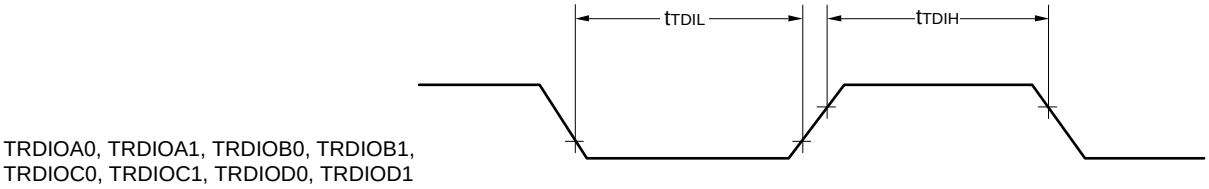


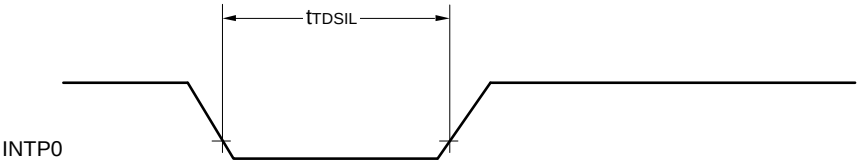

TI/TO Timing

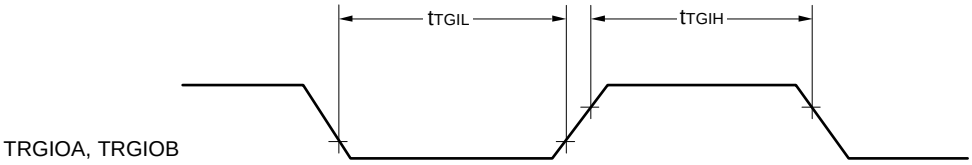


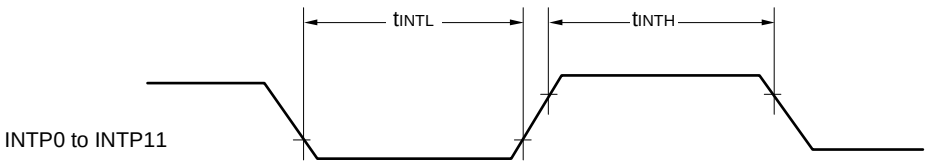

tTJIL
tTJIH
TRJIO


tTDIL
tTDIH
TRDIOA0, TRDIOA1, TRDIOB0, TRDIOB1,
TRDIOC0, TRDIOC1, TRDIOD0, TRDIOD1

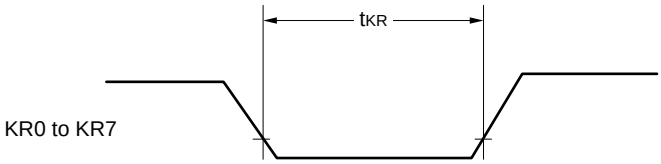

tTDSIL
INTP0


tTGIL
tTGIH
TRGIOA, TRGIOB

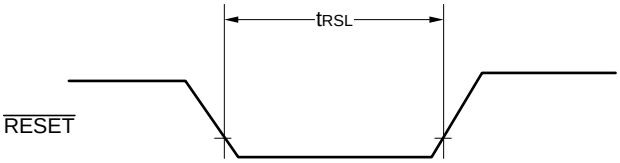
Interrupt Request Input Timing




Key Interrupt Input Timing

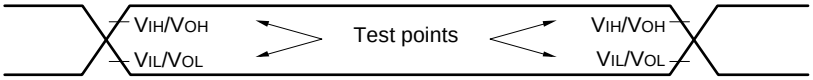



$\overline{\text{RESET}}$ Input Timing



## 2.5 Peripheral Functions Characteristics

AC Timing Test Points




### 2.5.1 Serial array unit

**(1) During communication at same potential (UART mode)**

**($T_A$ = -40 to +85°C, 1.6 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LV (low-voltage main) Mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| Transfer rate Note 1 | | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V | | $f_{MCK}$/6 Note 2 | | $f_{MCK}$/6 | | $f_{MCK}$/6 | bps |
| | | Theoretical value of the maximum transfer rate $f_{MCK}$ = $f_{CLK}$ Note 3 | | 5.3 | | 1.3 | | 0.6 | Mbps |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | | $f_{MCK}$/6 Note 2 | | $f_{MCK}$/6 | | $f_{MCK}$/6 | bps |
| | | Theoretical value of the maximum transfer rate $f_{MCK}$ = $f_{CLK}$ Note 3 | | 5.3 | | 1.3 | | 0.6 | Mbps |
| | | 1.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | $f_{MCK}$/6 Note 2 | | $f_{MCK}$/6 Note 2 | | $f_{MCK}$/6 | bps |
| | | Theoretical value of the maximum transfer rate $f_{MCK}$ = $f_{CLK}$ Note 3 | | 5.3 | | 1.3 | | 0.6 | Mbps |
| | | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V | — | | | $f_{MCK}$/6 Note 2 | | $f_{MCK}$/6 | bps |
| | | Theoretical value of the maximum transfer rate $f_{MCK}$ = $f_{CLK}$ Note 3 | — | | | 1.3 | | 0.6 | Mbps |

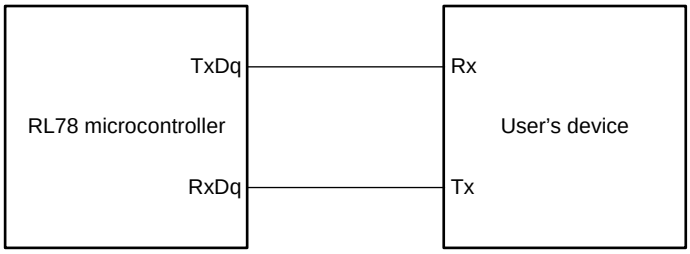
**Note 1.** Transfer rate in the SNOOZE mode is 4800 bps only.
However, the SNOOZE mode cannot be used when FRQSEL4 = 1.

**Note 2.** The following conditions are required for low voltage interface when $EV_{DD0}$ < $V_{DD}$.
2.4 V ≤ $EV_{DD0}$ < 2.7 V: MAX. 2.6 Mbps
1.8 V ≤ $EV_{DD0}$ < 2.4 V: MAX. 1.3 Mbps
1.6 V ≤ $EV_{DD0}$ < 1.8 V: MAX. 0.6 Mbps

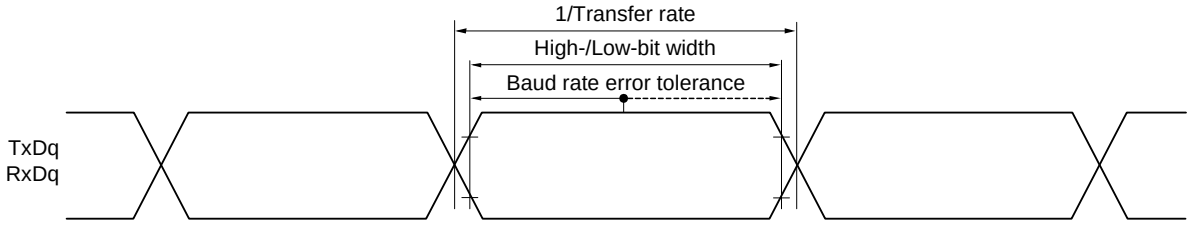
**Note 3.** The maximum operating frequencies of the CPU/peripheral hardware clock ($f_{CLK}$) are:
HS (high-speed main) mode: 32 MHz (2.7 V ≤ $V_{DD}$ ≤ 5.5 V)
16 MHz (2.4 V ≤ $V_{DD}$ ≤ 5.5 V)
LS (low-speed main) mode: 8 MHz (1.8 V ≤ $V_{DD}$ ≤ 5.5 V)
LV (low-voltage main) mode: 4 MHz (1.6 V ≤ $V_{DD}$ ≤ 5.5 V)

**Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

**UART mode connection diagram (during communication at same potential)**




**UART mode bit width (during communication at same potential) (reference)**




**Remark 1.** q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 5, 14)

**Remark 2.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

### (2) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output, corresponding CSI00 only)

**($T_A$ = -40 to +85°C, 2.7 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) mode | | LS (low-speed main) mode | | LV (low-voltage main) mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCKp cycle time | $t_{KCY1}$ | $t_{KCY1}$ ≥ 2/$f_{CLK}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V | 62.5 | | 250 | | 500 | | ns |
| | | | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | 83.3 | | 250 | | 500 | | ns |
| SCKp high-/low-level width | $t_{KH1}$, $t_{KL1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V | | $t_{KCY1}$/2 - 7 | | $t_{KCY1}$/2 - 50 | | $t_{KCY1}$/2 - 50 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | $t_{KCY1}$/2 - 10 | | $t_{KCY1}$/2 - 50 | | $t_{KCY1}$/2 - 50 | | ns |
| SIp setup time (to SCKp↑) Note 1 | $t_{SIK1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 23 | | 110 | | 110 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 33 | | 110 | | 110 | | ns |
| SIp hold time (from SCKp↑) Note 2 | $t_{KSI1}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 10 | | 10 | | 10 | | ns |
| Delay time from SCKp↓ to SOp output Note 3 | $t_{KSO1}$ | C = 20 pF Note 4 | | | 10 | | 10 | | 10 | ns |

**Note 1.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 2.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 3.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 4.** C is the load capacitance of the SCKp and SOp output lines.

**Caution Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

**Remark 1.** This value is valid only when CSI00’s peripheral I/O redirect function is not used.

**Remark 2.** p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0),
g: PIM and POM numbers (g = 1)

**Remark 3.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,
n: Channel number (mn = 00))

### (3) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)

**($T_A$ = -40 to +85°C, 1.6 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) mode | | LS (low-speed main) mode | | LV (low-voltage main) mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCKp cycle time | $t_{KCY1}$ | $t_{KCY1} \geq 4/f_{CLK}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | 125 | | 500 | | 1000 | | ns |
| | | | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V | 250 | | 500 | | 1000 | | ns |
| | | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | 500 | | 500 | | 1000 | | ns |
| | | | 1.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | 1000 | | 1000 | | 1000 | | ns |
| | | | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V | — | | 1000 | | 1000 | | ns |
| SCKp high-/low-level width | $t_{KH1}$, $t_{KL1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V | | $t_{KCY1}$/2 - 12 | | $t_{KCY1}$/2 - 50 | | $t_{KCY1}$/2 - 50 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | $t_{KCY1}$/2 - 18 | | $t_{KCY1}$/2 - 50 | | $t_{KCY1}$/2 - 50 | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V | | $t_{KCY1}$/2 - 38 | | $t_{KCY1}$/2 - 50 | | $t_{KCY1}$/2 - 50 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | | $t_{KCY1}$/2 - 50 | | $t_{KCY1}$/2 - 50 | | $t_{KCY1}$/2 - 50 | | ns |
| | | 1.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | $t_{KCY1}$/2 - 100 | | $t_{KCY1}$/2 - 100 | | $t_{KCY1}$/2 - 100 | | ns |
| | | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V | | — | | $t_{KCY1}$/2 - 100 | | $t_{KCY1}$/2 - 100 | | ns |
| SIp setup time (to SCKp↑) Note 1 | $t_{SIK1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 44 | | 110 | | 110 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 44 | | 110 | | 110 | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 75 | | 110 | | 110 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 110 | | 110 | | 110 | | ns |
| | | 1.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 220 | | 220 | | 220 | | ns |
| | | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V | | — | | 220 | | 220 | | ns |
| SIp hold time (from SCKp↑) Note 2 | $t_{KSI1}$ | 1.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 19 | | 19 | | 19 | | ns |
| | | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V | | — | | 19 | | 19 | | ns |
| Delay time from SCKp↓ to SOp output Note 3 | $t_{KSO1}$ | 1.7 V ≤ $EV_{DD0}$ ≤ 5.5 V C = 30 pF Note 4 | | | 25 | | 25 | | 25 | ns |
| | | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V C = 30 pF Note 4 | | | — | | 25 | | 25 | ns |

**Note 1.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 2.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 3.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 4.** C is the load capacitance of the SCKp and SOp output lines.

**Caution Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

**Remark 1.** p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM number (g = 0, 1, 3 to 5, 14)

**Remark 2.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

### (4) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)

**($T_A$ = -40 to +85°C, 1.6 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V) (1/2)**

| Parameter | Symbol | Conditions | | HS (high-speed main) mode | | LS (low-speed main) mode | | LV (low-voltage main) mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCKp cycle time Note 5 | $t_{KCY2}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V | 20 MHz < $f_{MCK}$ | 8/$f_{MCK}$ | | — | | — | | ns |
| | | | $f_{MCK}$ ≤ 20 MHz | 6/$f_{MCK}$ | | 6/$f_{MCK}$ | | 6/$f_{MCK}$ | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | 16 MHz < $f_{MCK}$ | 8/$f_{MCK}$ | | — | | — | | ns |
| | | | $f_{MCK}$ ≤ 16 MHz | 6/$f_{MCK}$ | | 6/$f_{MCK}$ | | 6/$f_{MCK}$ | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 6/$f_{MCK}$ and 500 | | 6/$f_{MCK}$ and 500 | | 6/$f_{MCK}$ and 500 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 6/$f_{MCK}$ and 750 | | 6/$f_{MCK}$ and 750 | | 6/$f_{MCK}$ and 750 | | ns |
| | | 1.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 6/$f_{MCK}$ and 1500 | | 6/$f_{MCK}$ and 1500 | | 6/$f_{MCK}$ and 1500 | | ns |
| | | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V | | — | | 6/$f_{MCK}$ and 1500 | | 6/$f_{MCK}$ and 1500 | | ns |
| SCKp high-/low-level width | $t_{KH2}$, $t_{KL2}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V | | $t_{KCY2}$/2 - 7 | | $t_{KCY2}$/2 - 7 | | $t_{KCY2}$/2 - 7 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | $t_{KCY2}$/2 - 8 | | $t_{KCY2}$/2 - 8 | | $t_{KCY2}$/2 - 8 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | | $t_{KCY2}$/2 - 18 | | $t_{KCY2}$/2 - 18 | | $t_{KCY2}$/2 - 18 | | ns |
| | | 1.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | $t_{KCY2}$/2 - 66 | | $t_{KCY2}$/2 - 66 | | $t_{KCY2}$/2 - 66 | | ns |
| | | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V | | — | | $t_{KCY2}$/2 - 66 | | $t_{KCY2}$/2 - 66 | | ns |
| SIp setup time (to SCKp↑) Note 1 | $t_{SIK2}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 1/$f_{MCK}$ + 20 | | 1/$f_{MCK}$ + 30 | | 1/$f_{MCK}$ + 30 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 1/$f_{MCK}$ + 30 | | 1/$f_{MCK}$ + 30 | | 1/$f_{MCK}$ + 30 | | ns |
| | | 1.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 1/$f_{MCK}$ + 40 | | 1/$f_{MCK}$ + 40 | | 1/$f_{MCK}$ + 40 | | ns |
| | | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V | | — | | 1/$f_{MCK}$ + 40 | | 1/$f_{MCK}$ + 40 | | ns |
| SIp hold time (from SCKp↑) Note 2 | $t_{KSI2}$ | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 1/$f_{MCK}$ + 31 | | 1/$f_{MCK}$ + 31 | | 1/$f_{MCK}$ + 31 | | ns |
| | | 1.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 1/$f_{MCK}$ + 250 | | 1/$f_{MCK}$ + 250 | | 1/$f_{MCK}$ + 250 | | ns |
| | | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V | | — | | 1/$f_{MCK}$ + 250 | | 1/$f_{MCK}$ + 250 | | ns |
| Delay time from SCKp↓ to SOp output Note 3 | $t_{KSO2}$ | C = 30 pF Note 4 | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 2/$f_{MCK}$ + 44 | | 2/$f_{MCK}$ + 110 | | 2/$f_{MCK}$ + 110 | ns |
| | | | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 2/$f_{MCK}$ + 75 | | 2/$f_{MCK}$ + 110 | | 2/$f_{MCK}$ + 110 | ns |
| | | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 2/$f_{MCK}$ + 100 | | 2/$f_{MCK}$ + 110 | | 2/$f_{MCK}$ + 110 | ns |
| | | | 1.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 2/$f_{MCK}$ + 220 | | 2/$f_{MCK}$ + 220 | | 2/$f_{MCK}$ + 220 | ns |
| | | | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V | | — | | 2/$f_{MCK}$ + 220 | | 2/$f_{MCK}$ + 220 | ns |

**Note 1.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 2.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 3.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 4.** C is the load capacitance of the SOp output lines.

**Note 5.** The maximum transfer rate when using the SNOOZE mode is 1 Mbps.

**Caution Select the normal input buffer for the SIp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

**Remark 1.** p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31), m: Unit number (m = 0, 1),
n: Channel number (n = 0 to 3), g: PIM number (g = 0, 1, 3 to 5, 14)

**Remark 2.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,
n: Channel number (mn = 00 to 03, 10 to 13))

### (4) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)

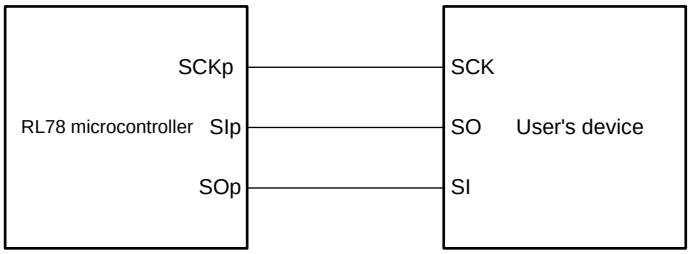
**($T_A$ = -40 to +85°C, 1.6 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)** **(2/2)**

| Parameter | Symbol | Conditions | | HS (high-speed main) mode | | LS (low-speed main) mode | | LV (low-voltage main) mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| $\overline{SSI00}$ setup time | $t_{SSIK}$ | DAPmn = 0 | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | 120 | | 120 | | 120 | | ns |
| | | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | 200 | | 200 | | 200 | | ns |
| | | | 1.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | 400 | | 400 | | 400 | | ns |
| | | | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V | — | | 400 | | 400 | | ns |
| | | DAPmn = 1 | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | 1/$f_{MCK}$ + 120 | | 1/$f_{MCK}$ + 120 | | 1/$f_{MCK}$ + 120 | | ns |
| | | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | 1/$f_{MCK}$ + 200 | | 1/$f_{MCK}$ + 200 | | 1/$f_{MCK}$ + 200 | | ns |
| | | | 1.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | 1/$f_{MCK}$ + 400 | | 1/$f_{MCK}$ + 400 | | 1/$f_{MCK}$ + 400 | | ns |
| | | | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V | — | | 1/$f_{MCK}$ + 400 | | 1/$f_{MCK}$ + 400 | | ns |
| $\overline{SSI00}$ hold time | $t_{KSSI}$ | DAPmn = 0 | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | 1/$f_{MCK}$ + 120 | | 1/$f_{MCK}$ + 120 | | 1/$f_{MCK}$ + 120 | | ns |
| | | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | 1/$f_{MCK}$ + 200 | | 1/$f_{MCK}$ + 200 | | 1/$f_{MCK}$ + 200 | | ns |
| | | | 1.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | 1/$f_{MCK}$ + 400 | | 1/$f_{MCK}$ + 400 | | 1/$f_{MCK}$ + 400 | | ns |
| | | | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V | — | | 1/$f_{MCK}$ + 400 | | 1/$f_{MCK}$ + 400 | | ns |
| | | DAPmn = 1 | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | 120 | | 120 | | 120 | | ns |
| | | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | 200 | | 200 | | 200 | | ns |
| | | | 1.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | 400 | | 400 | | 400 | | ns |
| | | | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V | — | | 400 | | 400 | | ns |

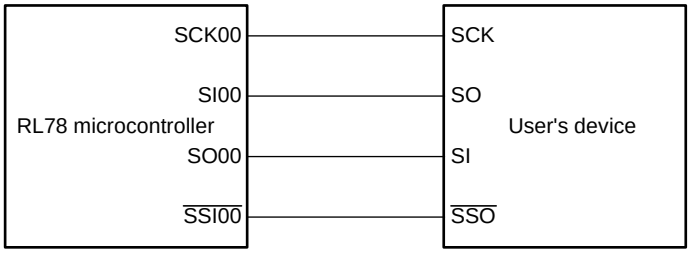
**Caution** **Select the normal input buffer for the SIp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

**Remark** p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM number (g = 3, 5)

**CSI mode connection diagram (during communication at same potential)**

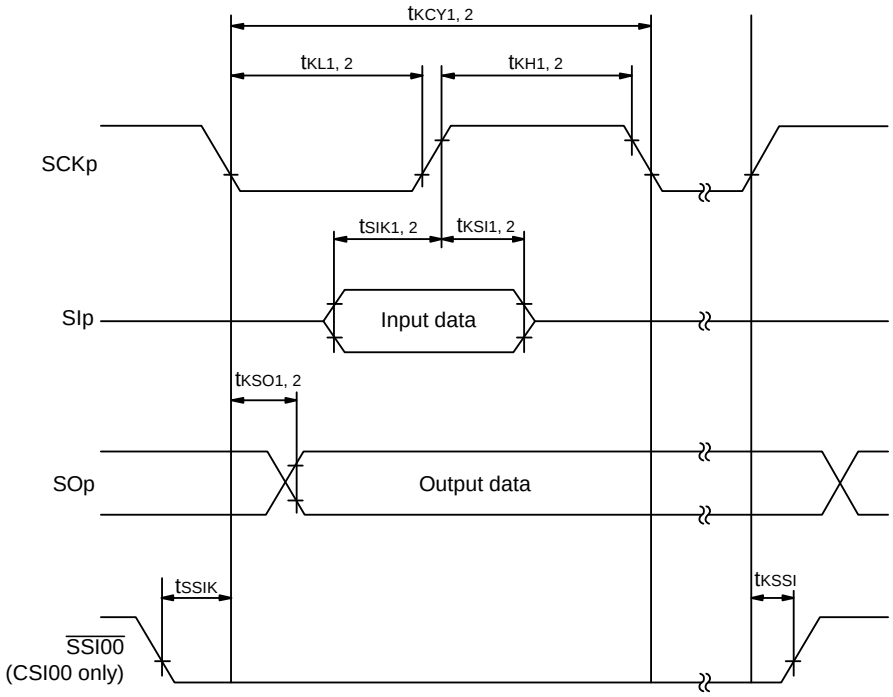



**CSI mode connection diagram (during communication at same potential)**
**(Slave Transmission of slave select input function (CSI00))**

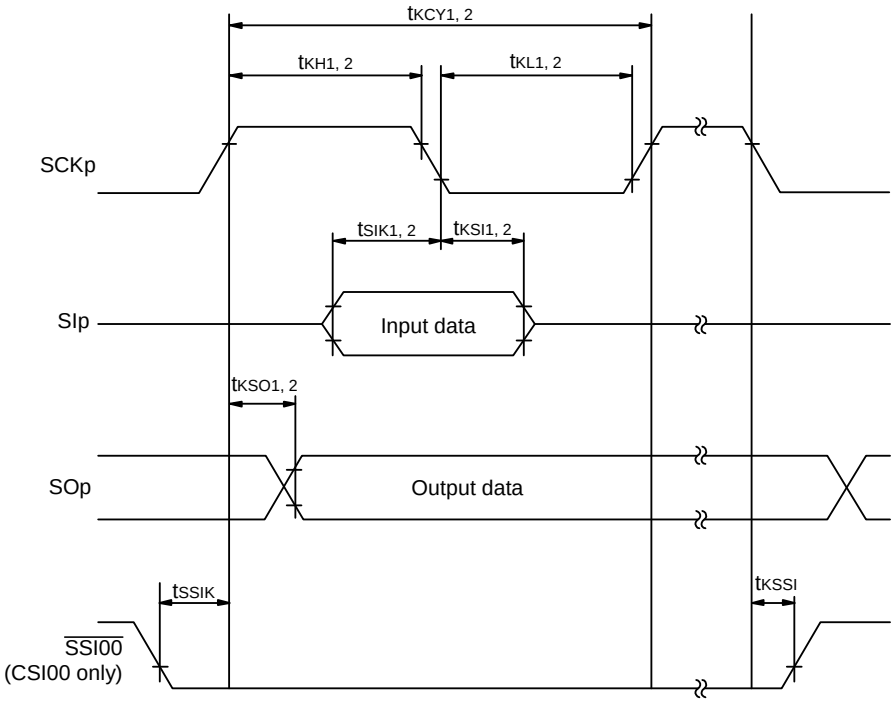



**Remark 1.** p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31)
**Remark 2.** m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13)

**CSI mode serial transfer timing (during communication at same potential)**
**(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)**




**CSI mode serial transfer timing (during communication at same potential)**
**(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**




**Remark 1.** p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31)
**Remark 2.** m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13)

### (5) During communication at same potential (simplified I²C mode)

**($T_A$ = -40 to +85°C, 1.6 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)** **(1/2)**

| Parameter | Symbol | Conditions | HS (high-speed main) mode | | LS (low-speed main) mode | | LV (low-voltage main) mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCLr clock frequency | $f_{SCL}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | | 1000 Note 1 | | 400 Note 1 | | 400 Note 1 | kHz |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V, $C_b$ = 100 pF, $R_b$ = 3 kΩ | | 400 Note 1 | | 400 Note 1 | | 400 Note 1 | kHz |
| | | 1.8 V ≤ $EV_{DD0}$ < 2.7 V, $C_b$ = 100 pF, $R_b$ = 5 kΩ | | 300 Note 1 | | 300 Note 1 | | 300 Note 1 | kHz |
| | | 1.7 V ≤ $EV_{DD0}$ < 1.8 V, $C_b$ = 100 pF, $R_b$ = 5 kΩ | | 250 Note 1 | | 250 Note 1 | | 250 Note 1 | kHz |
| | | 1.6 V ≤ $EV_{DD0}$ < 1.8 V, $C_b$ = 100 pF, $R_b$ = 5 kΩ | | — | | 250 Note 1 | | 250 Note 1 | kHz |
| Hold time when SCLr = “L” | $t_{LOW}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 475 | | 1150 | | 1150 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V, $C_b$ = 100 pF, $R_b$ = 3 kΩ | 1150 | | 1150 | | 1150 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ < 2.7 V, $C_b$ = 100 pF, $R_b$ = 5 kΩ | 1550 | | 1550 | | 1550 | | ns |
| | | 1.7 V ≤ $EV_{DD0}$ < 1.8 V, $C_b$ = 100 pF, $R_b$ = 5 kΩ | 1850 | | 1850 | | 1850 | | ns |
| | | 1.6 V ≤ $EV_{DD0}$ < 1.8 V, $C_b$ = 100 pF, $R_b$ = 5 kΩ | — | | 1850 | | 1850 | | ns |
| Hold time when SCLr = “H” | $t_{HIGH}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 475 | | 1150 | | 1150 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V, $C_b$ = 100 pF, $R_b$ = 3 kΩ | 1150 | | 1150 | | 1150 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ < 2.7 V, $C_b$ = 100 pF, $R_b$ = 5 kΩ | 1550 | | 1550 | | 1550 | | ns |
| | | 1.7 V ≤ $EV_{DD0}$ < 1.8 V, $C_b$ = 100 pF, $R_b$ = 5 kΩ | 1850 | | 1850 | | 1850 | | ns |
| | | 1.6 V ≤ $EV_{DD0}$ < 1.8 V, $C_b$ = 100 pF, $R_b$ = 5 kΩ | — | | 1850 | | 1850 | | ns |

(**Notes** and **Caution** are listed on the next page, and **Remarks** are listed on the page after the next page.)

### (5) During communication at same potential (simplified I²C mode)

**($T_A$ = -40 to +85°C, 1.6 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)** **(2/2)**

| Parameter | Symbol | Conditions | HS (high-speed main) mode | | LS (low-speed main) mode | | LV (low-voltage main) mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| Data setup time (reception) | $t_{SU:DAT}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 1/$f_{MCK}$ + 85 Note 2 | | 1/$f_{MCK}$ + 145 Note 2 | | 1/$f_{MCK}$ + 145 Note 2 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V, $C_b$ = 100 pF, $R_b$ = 3 kΩ | 1/$f_{MCK}$ + 145 Note 2 | | 1/$f_{MCK}$ + 145 Note 2 | | 1/$f_{MCK}$ + 145 Note 2 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ < 2.7 V, $C_b$ = 100 pF, $R_b$ = 5 kΩ | 1/$f_{MCK}$ + 230 Note 2 | | 1/$f_{MCK}$ + 230 Note 2 | | 1/$f_{MCK}$ + 230 Note 2 | | ns |
| | | 1.7 V ≤ $EV_{DD0}$ < 1.8 V, $C_b$ = 100 pF, $R_b$ = 5 kΩ | 1/$f_{MCK}$ + 290 Note 2 | | 1/$f_{MCK}$ + 290 Note 2 | | 1/$f_{MCK}$ + 290 Note 2 | | ns |
| | | 1.6 V ≤ $EV_{DD0}$ < 1.8 V, $C_b$ = 100 pF, $R_b$ = 5 kΩ | — | | 1/$f_{MCK}$ + 290 Note 2 | | 1/$f_{MCK}$ + 290 Note 2 | | ns |
| Data hold time (transmission) | $t_{HD:DAT}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 0 | 305 | 0 | 305 | 0 | 305 | ns |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V, $C_b$ = 100 pF, $R_b$ = 3 kΩ | 0 | 355 | 0 | 355 | 0 | 355 | ns |
| | | 1.8 V ≤ $EV_{DD0}$ < 2.7 V, $C_b$ = 100 pF, $R_b$ = 5 kΩ | 0 | 405 | 0 | 405 | 0 | 405 | ns |
| | | 1.7 V ≤ $EV_{DD0}$ < 1.8 V, $C_b$ = 100 pF, $R_b$ = 5 kΩ | 0 | 405 | 0 | 405 | 0 | 405 | ns |
| | | 1.6 V ≤ $EV_{DD0}$ < 1.8 V, $C_b$ = 100 pF, $R_b$ = 5 kΩ | — | | 0 | 405 | 0 | 405 | ns |

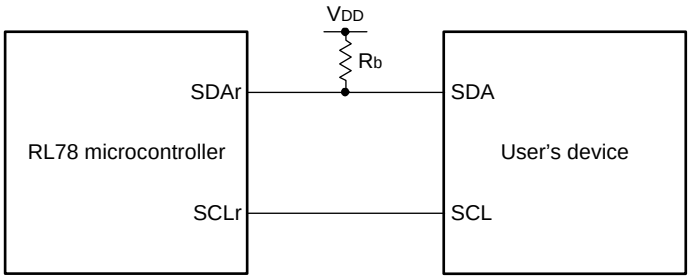
**Note 1.** The value must also be equal to or less than $f_{MCK}$/4.

**Note 2.** Set the $f_{MCK}$ value to keep the hold time of SCLr = “L” and SCLr = “H”.

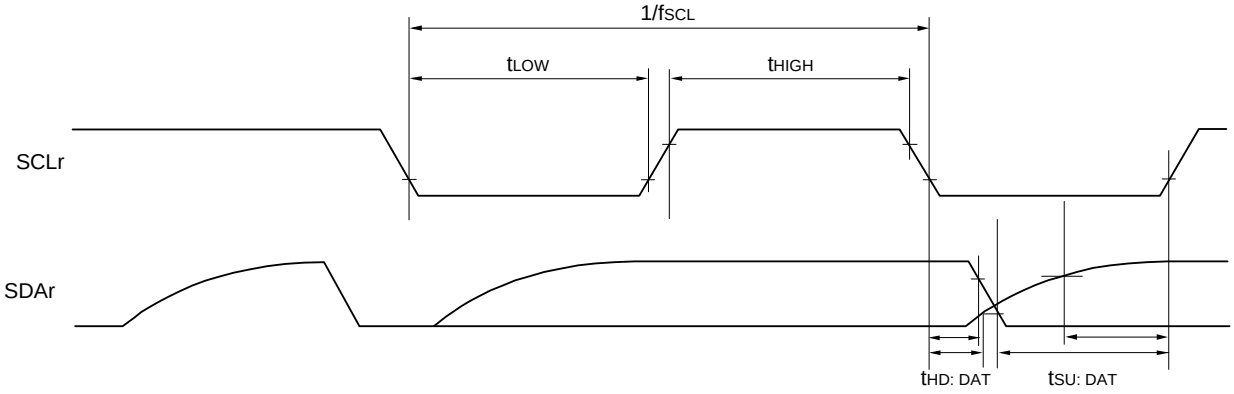
**Caution Select the normal input buffer and the N-ch open drain output ($V_{DD}$ tolerance (for the 30- to 52-pin products)/$EV_{DD}$ tolerance (for the 64- to 100-pin products)) mode for the SDAr pin and the normal output mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register h (POMh).**

(**Remarks** are listed on the next page.)

**Simplified I²C mode connection diagram (during communication at same potential)**




**Simplified I²C mode serial transfer timing (during communication at same potential)**




**Remark 1.** $R_b$[Ω]: Communication line (SDAr) pull-up resistance, $C_b$[F]: Communication line (SDAr, SCLr) load capacitance

**Remark 2.** r: IIC number (r = 00, 01, 10, 11, 20, 21, 30, 31), g: PIM number (g = 0, 1, 3 to 5, 14), h: POM number (h = 0, 1, 3 to 5, 7, 14)

**Remark 3.** $f_{MCK}$: Serial array unit operation clock frequency (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), mn = 00 to 03, 10 to 13)

### (6) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode)

**($T_A$ = -40 to +85°C, 1.6 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V) (1/2)**

| Parameter | Symbol | Conditions | | HS (high-speed main) mode | | LS (low-speed main) mode | | LV (low-voltage main) mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| Transfer rate | | reception | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V | | $f_{MCK}$/6 Note 1 | | $f_{MCK}$/6 Note 1 | | $f_{MCK}$/6 Note 1 | bps |
| | | | Theoretical value of the maximum transfer rate $f_{MCK}$ = $f_{CLK}$ Note 4 | | 5.3 | | 1.3 | | 0.6 | Mbps |
| | | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | | $f_{MCK}$/6 Note 1 | | $f_{MCK}$/6 Note 1 | | $f_{MCK}$/6 Note 1 | bps |
| | | | Theoretical value of the maximum transfer rate $f_{MCK}$ = $f_{CLK}$ Note 4 | | 5.3 | | 1.3 | | 0.6 | Mbps |
| | | | 1.8 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V | | $f_{MCK}$/6 Notes 1, 2, 3 | | $f_{MCK}$/6 Notes 1, 2 | | $f_{MCK}$/6 Notes 1, 2 | bps |
| | | | Theoretical value of the maximum transfer rate $f_{MCK}$ = $f_{CLK}$ Note 4 | | 5.3 | | 1.3 | | 0.6 | Mbps |

**Note 1.** Transfer rate in the SNOOZE mode is 4800 bps only.
However, the SNOOZE mode cannot be used when FRQSEL4 = 1.

**Note 2.** Use it with $EV_{DD0}$ ≥ $V_b$.

**Note 3.** The following conditions are required for low voltage interface when $EV_{DD0}$ < $V_{DD}$.
2.4 V ≤ $EV_{DD0}$ < 2.7 V: MAX. 2.6 Mbps
1.8 V ≤ $EV_{DD0}$ < 2.4 V: MAX. 1.3 Mbps

**Note 4.** The maximum operating frequencies of the CPU/peripheral hardware clock ($f_{CLK}$) are:
HS (high-speed main) mode: 32 MHz (2.7 V ≤ $V_{DD}$ ≤ 5.5 V)
16 MHz (2.4 V ≤ $V_{DD}$ ≤ 5.5 V)
LS (low-speed main) mode: 8 MHz (1.8 V ≤ $V_{DD}$ ≤ 5.5 V)
LV (low-voltage main) mode: 4 MHz (1.6 V ≤ $V_{DD}$ ≤ 5.5 V)

**Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output ($V_{DD}$ tolerance (for the 30- to 52-pin products)/$EV_{DD}$ tolerance (for the 64- to 100-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

**Remark 1.** $V_b$ [V]: Communication line voltage

**Remark 2.** q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 5, 14)

**Remark 3.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13)

**Remark 4.** UART2 cannot communicate at different potential when bit 1 (PIOR01) of peripheral I/O redirection register 0 (PIOR0) is 1.

### (6) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode)

**($T_A$ = -40 to +85°C, 1.6 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)** **(2/2)**

| Parameter | Symbol | Conditions | | HS (high-speed main) mode | | LS (low-speed main) mode | | LV (low-voltage main) mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| Transfer rate | | transmission | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V | | Note 1 | | Note 1 | | Note 1 | bps |
| | | | Theoretical value of the maximum transfer rate $C_b$ = 50 pF, $R_b$ = 1.4 kΩ, $V_b$ = 2.7 V | | 2.8 Note 2 | | 2.8 Note 2 | | 2.8 Note 2 | Mbps |
| | | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | | Note 3 | | Note 3 | | Note 3 | bps |
| | | | Theoretical value of the maximum transfer rate $C_b$ = 50 pF, $R_b$ = 2.7 kΩ, $V_b$ = 2.3 V | | 1.2 Note 4 | | 1.2 Note 4 | | 1.2 Note 4 | Mbps |
| | | | 1.8 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V | | Notes 5, 6 | | Notes 5, 6 | | Notes 5, 6 | bps |
| | | | Theoretical value of the maximum transfer rate $C_b$ = 50 pF, $R_b$ = 5.5 kΩ, $V_b$ = 1.6 V | | 0.43 Note 7 | | 0.43 Note 7 | | 0.43 Note 7 | Mbps |

**Note 1.** The smaller maximum transfer rate derived by using $f_{MCK}$/6 or the following expression is the valid maximum transfer rate.
Expression for calculating the transfer rate when 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V and 2.7 V ≤ $V_b$ ≤ 4.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides

**Note 2.** This value as an example is calculated when the conditions described in the “Conditions” column are met.
Refer to **Note 1** above to calculate the maximum transfer rate under conditions of the customer.

**Note 3.** The smaller maximum transfer rate derived by using $f_{MCK}$/6 or the following expression is the valid maximum transfer rate.
Expression for calculating the transfer rate when 2.7 V ≤ $EV_{DD0}$ < 4.0 V and 2.3 V ≤ $V_b$ ≤ 2.7 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides

**Note 4.** This value as an example is calculated when the conditions described in the “Conditions” column are met.
Refer to **Note 3** above to calculate the maximum transfer rate under conditions of the customer.

**Note 5.** Use it with $EV_{DD0} \geq V_b$.

**Note 6.** The smaller maximum transfer rate derived by using $f_{MCK}$/6 or the following expression is the valid maximum transfer rate.
Expression for calculating the transfer rate when 1.8 V ≤ $EV_{DD0}$ < 3.3 V and 1.6 V ≤ $V_b$ ≤ 2.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

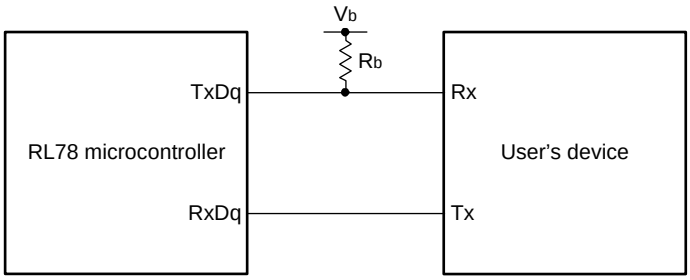
* This value is the theoretical value of the relative difference between the transmission and reception sides

**Note 7.** This value as an example is calculated when the conditions described in the “Conditions” column are met.
Refer to **Note 6** above to calculate the maximum transfer rate under conditions of the customer.

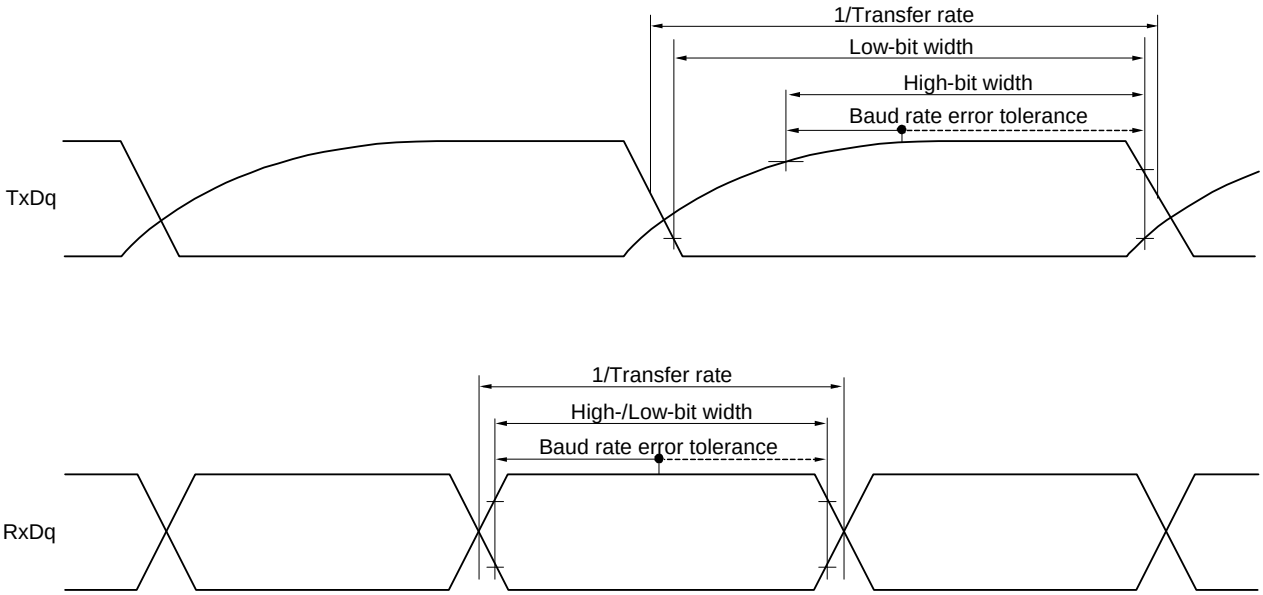
**Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output ($V_{DD}$ tolerance (for the 30- to 52-pin products)/$EV_{DD}$ tolerance (for the 64- to 100-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

(**Remarks** are listed on the next page.)

**UART mode connection diagram (during communication at different potential)**




**UART mode bit width (during communication at different potential) (reference)**




**Remark 1.** $R_b$[Ω]: Communication line (TxDq) pull-up resistance,
$C_b$[F]: Communication line (TxDq) load capacitance, $V_b$[V]: Communication line voltage

**Remark 2.** q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 5, 14)

**Remark 3.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

**Remark 4.** UART2 cannot communicate at different potential when bit 1 (PIOR01) of peripheral I/O redirection register 0 (PIOR0) is 1.

### (7) Communication at different potential (2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output, corresponding CSI00 only)

**($T_A$ = -40 to +85°C, 2.7 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V) (1/2)**

| Parameter | Symbol | Conditions | | HS (high-speed main) mode | | LS (low-speed main) mode | | LV (low-voltage main) mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCKp cycle time | $t_{KCY1}$ | $t_{KCY1} \geq 2/f_{CLK}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 20 pF, $R_b$ = 1.4 kΩ | 200 | | 1150 | | 1150 | | ns |
| | | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 20 pF, $R_b$ = 2.7 kΩ | 300 | | 1150 | | 1150 | | ns |
| SCKp high-level width | $t_{KH1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 20 pF, $R_b$ = 1.4 kΩ | | $t_{KCY1}$/2 - 50 | | $t_{KCY1}$/2 - 50 | | $t_{KCY1}$/2 - 50 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 20 pF, $R_b$ = 2.7 kΩ | | $t_{KCY1}$/2 - 120 | | $t_{KCY1}$/2 - 120 | | $t_{KCY1}$/2 - 120 | | ns |
| SCKp low-level width | $t_{KL1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 20 pF, $R_b$ = 1.4 kΩ | | $t_{KCY1}$/2 - 7 | | $t_{KCY1}$/2 - 50 | | $t_{KCY1}$/2 - 50 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 20 pF, $R_b$ = 2.7 kΩ | | $t_{KCY1}$/2 - 10 | | $t_{KCY1}$/2 - 50 | | $t_{KCY1}$/2 - 50 | | ns |
| SIp setup time (to SCKp↑) Note 1 | $t_{SIK1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 20 pF, $R_b$ = 1.4 kΩ | | 58 | | 479 | | 479 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 20 pF, $R_b$ = 2.7 kΩ | | 121 | | 479 | | 479 | | ns |
| SIp hold time (from SCKp↑) Note 1 | $t_{KSI1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 20 pF, $R_b$ = 1.4 kΩ | | 10 | | 10 | | 10 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 20 pF, $R_b$ = 2.7 kΩ | | 10 | | 10 | | 10 | | ns |
| Delay time from SCKp↓ to SOp output Note 1 | $t_{KSO1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 20 pF, $R_b$ = 1.4 kΩ | | | 60 | | 60 | | 60 | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 20 pF, $R_b$ = 2.7 kΩ | | | 130 | | 130 | | 130 | ns |

(**Notes**, **Caution**, and **Remarks** are listed on the next page.)

### (7) Communication at different potential (2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output, corresponding CSI00 only)

**($T_A$ = -40 to +85°C, 2.7 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V) (2/2)**

| Parameter | Symbol | Conditions | HS (high-speed main) mode | | LS (low-speed main) mode | | LV (low-voltage main) mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SIp setup time (to SCKp↓) Note 2 | $t_{SIK1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 20 pF, $R_b$ = 1.4 kΩ | 23 | | 110 | | 110 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 20 pF, $R_b$ = 2.7 kΩ | 33 | | 110 | | 110 | | ns |
| SIp hold time (from SCKp↓) Note 2 | $t_{KSI1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 20 pF, $R_b$ = 1.4 kΩ | 10 | | 10 | | 10 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 20 pF, $R_b$ = 2.7 kΩ | 10 | | 10 | | 10 | | ns |
| Delay time from SCKp↑ to SOp output Note 2 | $t_{KSO1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 20 pF, $R_b$ = 1.4 kΩ | | 10 | | 10 | | 10 | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 20 pF, $R_b$ = 2.7 kΩ | | 10 | | 10 | | 10 | ns |

**Note 1.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

**Note 2.** When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output ($V_{DD}$ tolerance (for the 30- to 52-pin products)/$EV_{DD}$ tolerance (for the 64- to 100-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

**Remark 1.** $R_b$[Ω]: Communication line (SCKp, SOp) pull-up resistance, $C_b$[F]: Communication line (SCKp, SOp) load capacitance, $V_b$[V]: Communication line voltage

**Remark 2.** p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM number (g = 3, 5)

**Remark 3.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00))

**Remark 4.** This value is valid only when CSI00's peripheral I/O redirect function is not used.

### (8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output)

**($T_A$ = -40 to +85°C, 1.8 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V) (1/3)**

| Parameter | Symbol | Conditions | | HS (high-speed main) mode | | LS (low-speed main) mode | | LV (low-voltage main) mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCKp cycle time | $t_{KCY1}$ | $t_{KCY1} \geq 4/f_{CLK}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | 300 | | 1150 | | 1150 | | ns |
| | | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | 500 | | 1150 | | 1150 | | ns |
| | | | 1.8 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | 1150 | | 1150 | | 1150 | | ns |
| SCKp high-level width | $t_{KH1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | | $t_{KCY1}$/2 - 75 | | $t_{KCY1}$/2 - 75 | | $t_{KCY1}$/2 - 75 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | | $t_{KCY1}$/2 - 170 | | $t_{KCY1}$/2 - 170 | | $t_{KCY1}$/2 - 170 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | | $t_{KCY1}$/2 - 458 | | $t_{KCY1}$/2 - 458 | | $t_{KCY1}$/2 - 458 | | ns |
| SCKp low-level width | $t_{KL1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | | $t_{KCY1}$/2 - 12 | | $t_{KCY1}$/2 - 50 | | $t_{KCY1}$/2 - 50 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | | $t_{KCY1}$/2 - 18 | | $t_{KCY1}$/2 - 50 | | $t_{KCY1}$/2 - 50 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | | $t_{KCY1}$/2 - 50 | | $t_{KCY1}$/2 - 50 | | $t_{KCY1}$/2 - 50 | | ns |

**Note** Use it with $EV_{DD0} \geq V_b$.

**Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output ($V_{DD}$ tolerance (for the 30- to 52-pin products)/$EV_{DD}$ tolerance (for the 64- to 100-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

(**Remarks** are listed two pages after the next page.)

### (8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output)

**($T_A$ = -40 to +85°C, 1.8 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V) (2/3)**

| Parameter | Symbol | Conditions | HS (high-speed main) mode | | LS (low-speed main) mode | | LV (low-voltage main) mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SIp setup time (to SCKp↑) Note 1 | $t_{SIK1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | 81 | | 479 | | 479 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | 177 | | 479 | | 479 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | 479 | | 479 | | 479 | | ns |
| SIp hold time (from SCKp↑) Note 1 | $t_{KSI1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | 19 | | 19 | | 19 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | 19 | | 19 | | 19 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | 19 | | 19 | | 19 | | ns |
| Delay time from SCKp↓ to SOp output Note 1 | $t_{KSO1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | | 100 | | 100 | | 100 | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | | 195 | | 195 | | 195 | ns |
| | | 1.8 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | | 483 | | 483 | | 483 | ns |

**Note 1.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

**Note 2.** Use it with $EV_{DD0}$ ≥ $V_b$.

**Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output ($V_{DD}$ tolerance (for the 30- to 52-pin products)/$EV_{DD}$ tolerance (for the 64- to 100-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

(**Remarks** are listed on the page after the next page.)

### (8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output)

**($T_A$ = -40 to +85°C, 1.8 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V) (3/3)**

| Parameter | Symbol | Conditions | HS (high-speed main) mode | | LS (low-speed main) mode | | LV (low-voltage main) mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SIp setup time (to SCKp↓) Note 1 | $t_{SIK1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | 44 | | 110 | | 110 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | 44 | | 110 | | 110 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | 110 | | 110 | | 110 | | ns |
| SIp hold time (from SCKp↓) Note 1 | $t_{KSI1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | 19 | | 19 | | 19 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | 19 | | 19 | | 19 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | 19 | | 19 | | 19 | | ns |
| Delay time from SCKp↑ to SOp output Note 1 | $t_{KSO1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | | 25 | | 25 | | 25 | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | | 25 | | 25 | | 25 | ns |
| | | 1.8 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | | 25 | | 25 | | 25 | ns |

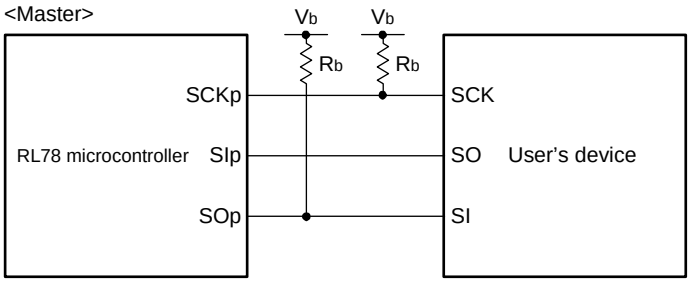
**Note 1.** When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 2.** Use it with $EV_{DD0}$ ≥ $V_b$.

**Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output ($V_{DD}$ tolerance (for the 30- to 52-pin products)/$EV_{DD}$ tolerance (for the 64- to 100-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

(**Remarks** are listed on the next page.)

**CSI mode connection diagram (during communication at different potential**



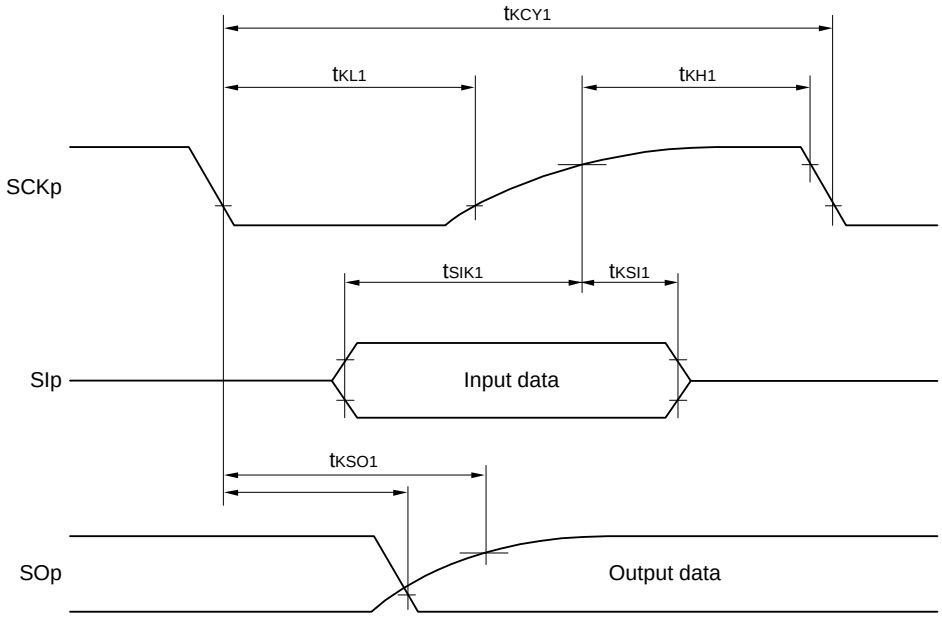

**Remark 1.** $R_b$[Ω]: Communication line (SCKp, SOp) pull-up resistance, $C_b$[F]: Communication line (SCKp, SOp) load capacitance, $V_b$[V]: Communication line voltage

**Remark 2.** p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM and POM number (g = 0, 1, 3 to 5, 14)

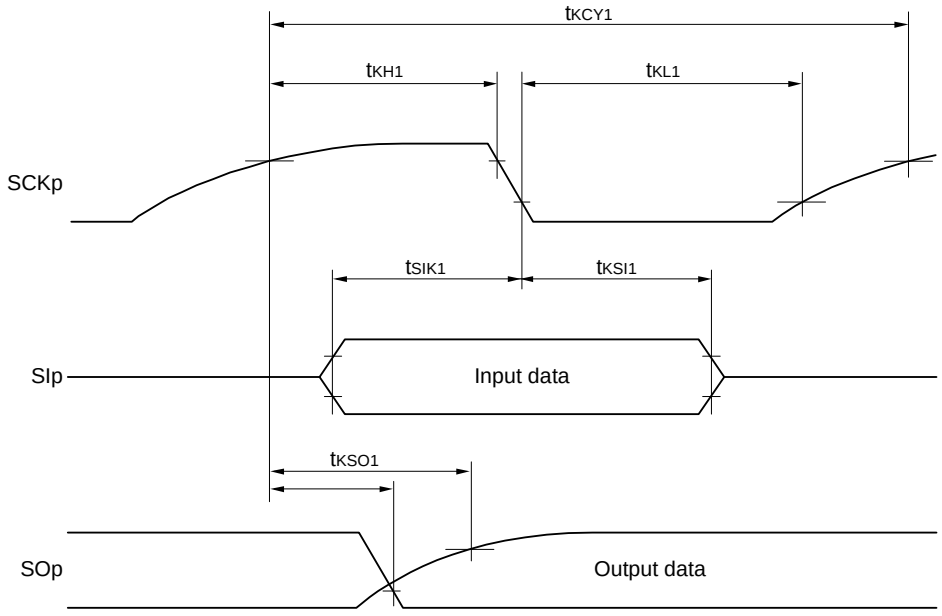
**Remark 3.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00))

**Remark 4.** CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

**CSI mode serial transfer timing (master mode) (during communication at different potential)**
**(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)**




**CSI mode serial transfer timing (master mode) (during communication at different potential)**
**(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**




**Remark 1.** p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM and POM number (g = 0, 1, 3 to 5, 14)

**Remark 2.** CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

### (9) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)

**($T_A$ = -40 to +85°C, 1.8 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) mode | | LS (low-speed main) mode | | LV (low-voltage main) mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCKp cycle time Note 1 | $t_{KCY2}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V | 24 MHz < $f_{MCK}$ | 14/$f_{MCK}$ | | — | | — | | ns |
| | | | 20 MHz < $f_{MCK}$ ≤ 24 MHz | 12/$f_{MCK}$ | | — | | — | | ns |
| | | | 8 MHz < $f_{MCK}$ ≤ 20 MHz | 10/$f_{MCK}$ | | — | | — | | ns |
| | | | 4 MHz < $f_{MCK}$ ≤ 8 MHz | 8/$f_{MCK}$ | | 16/$f_{MCK}$ | | — | | ns |
| | | | $f_{MCK}$ ≤ 4 MHz | 6/$f_{MCK}$ | | 10/$f_{MCK}$ | | 10/$f_{MCK}$ | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | 24 MHz < $f_{MCK}$ | 20/$f_{MCK}$ | | — | | — | | ns |
| | | | 20 MHz < $f_{MCK}$ ≤ 24 MHz | 16/$f_{MCK}$ | | — | | — | | ns |
| | | | 16 MHz < $f_{MCK}$ ≤ 20 MHz | 14/$f_{MCK}$ | | — | | — | | ns |
| | | | 8 MHz < $f_{MCK}$ ≤ 16 MHz | 12/$f_{MCK}$ | | — | | — | | ns |
| | | | 4 MHz < $f_{MCK}$ ≤ 8 MHz | 8/$f_{MCK}$ | | 16/$f_{MCK}$ | | — | | ns |
| | | | $f_{MCK}$ ≤ 4 MHz | 6/$f_{MCK}$ | | 10/$f_{MCK}$ | | 10/$f_{MCK}$ | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2 | 24 MHz < $f_{MCK}$ | 48/$f_{MCK}$ | | — | | — | | ns |
| | | | 20 MHz < $f_{MCK}$ ≤ 24 MHz | 36/$f_{MCK}$ | | — | | — | | ns |
| | | | 16 MHz < $f_{MCK}$ ≤ 20 MHz | 32/$f_{MCK}$ | | — | | — | | ns |
| | | | 8 MHz < $f_{MCK}$ ≤ 16 MHz | 26/$f_{MCK}$ | | — | | — | | ns |
| | | | 4 MHz < $f_{MCK}$ ≤ 8 MHz | 16/$f_{MCK}$ | | 16/$f_{MCK}$ | | — | | ns |
| | | | $f_{MCK}$ ≤ 4 MHz | 10/$f_{MCK}$ | | 10/$f_{MCK}$ | | 10/$f_{MCK}$ | | ns |
| SCKp high-/low-level width | $t_{KH2}$, $t_{KL2}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V | | $t_{KCY2}$/2 - 12 | | $t_{KCY2}$/2 - 50 | | $t_{KCY2}$/2 - 50 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | | $t_{KCY2}$/2 - 18 | | $t_{KCY2}$/2 - 50 | | $t_{KCY2}$/2 - 50 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2 | | $t_{KCY2}$/2 - 50 | | $t_{KCY2}$/2 - 50 | | $t_{KCY2}$/2 - 50 | | ns |
| SIp setup time (to SCKp↑) Note 3 | $t_{SIK2}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V | | 1/$f_{MCK}$ + 20 | | 1/$f_{MCK}$ + 30 | | 1/$f_{MCK}$ + 30 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | | 1/$f_{MCK}$ + 20 | | 1/$f_{MCK}$ + 30 | | 1/$f_{MCK}$ + 30 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2 | | 1/$f_{MCK}$ + 30 | | 1/$f_{MCK}$ + 30 | | 1/$f_{MCK}$ + 30 | | ns |
| SIp hold time (from SCKp↑) Note 4 | $t_{KSI2}$ | | | 1/$f_{MCK}$ + 31 | | 1/$f_{MCK}$ + 31 | | 1/$f_{MCK}$ + 31 | | ns |
| Delay time from SCKp↓ to SOp output Note 5 | $t_{KSO2}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | | | 2/$f_{MCK}$ + 120 | | 2/$f_{MCK}$ + 573 | | 2/$f_{MCK}$ + 573 | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | | | 2/$f_{MCK}$ + 214 | | 2/$f_{MCK}$ + 573 | | 2/$f_{MCK}$ + 573 | ns |
| | | 1.8 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2, $C_b$ = 30 pF, $R_v$ = 5.5 kΩ | | | 2/$f_{MCK}$ + 573 | | 2/$f_{MCK}$ + 573 | | 2/$f_{MCK}$ + 573 | ns |

(**Notes**, **Caution**, and **Remarks** are listed on the next page.)

**Note 1.** Transfer rate in the SNOOZE mode: MAX. 1 Mbps

**Note 2.** Use it with $EV_{DD0} \geq V_b$.

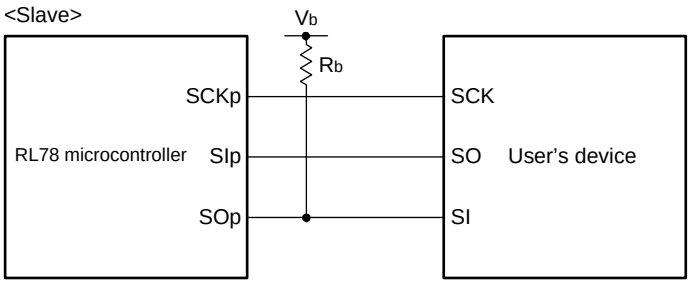
**Note 3.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 4.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 5.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Caution Select the TTL input buffer for the SIp pin and SCKp pin, and the N-ch open drain output ($V_{DD}$ tolerance (for the 30- to 52-pin products)/$EV_{DD}$ tolerance (for the 64- to 100-pin products)) mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

**CSI mode connection diagram (during communication at different potential)**



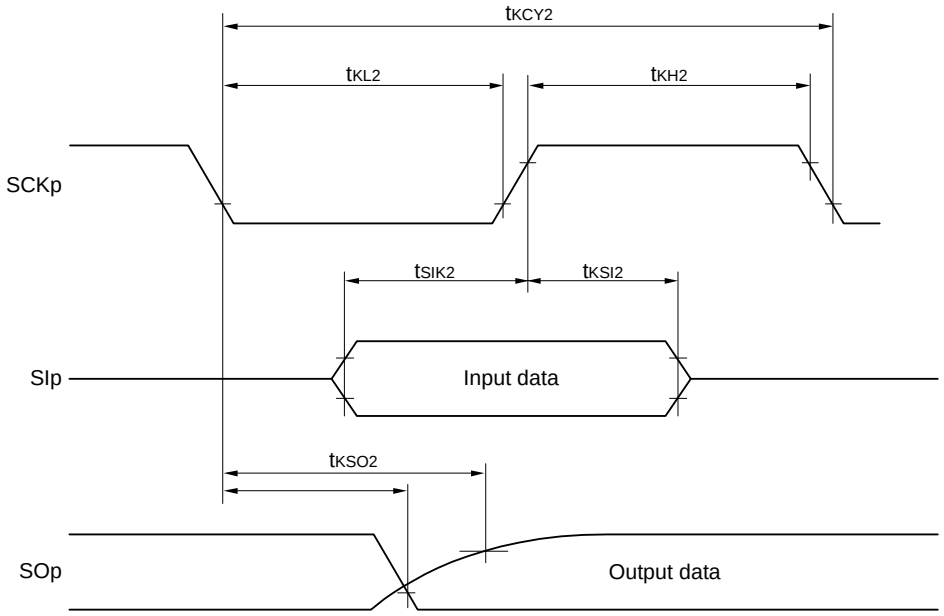

**Remark 1.** $R_b$[Ω]: Communication line (SOp) pull-up resistance, $C_b$[F]: Communication line (SOp) load capacitance, $V_b$[V]: Communication line voltage

**Remark 2.** p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM and POM number (g = 0, 1, 3 to 5, 14)

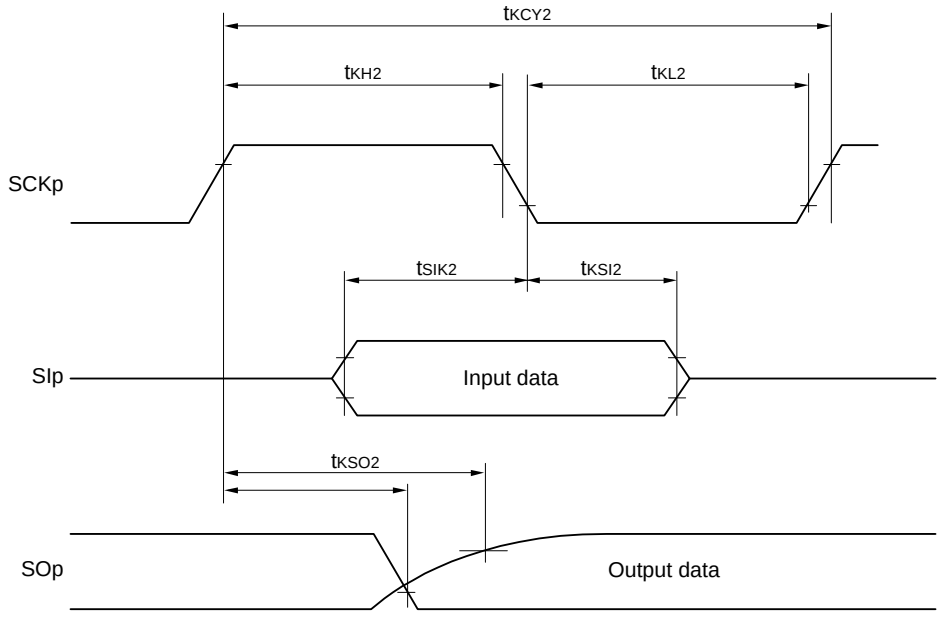
**Remark 3.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00, 01, 02, 10, 12, 13))

**Remark 4.** CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.
Also, communication at different potential cannot be performed during clock synchronous serial communication with the slave select function.

**CSI mode serial transfer timing (slave mode) (during communication at different potential)**
**(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)**




**CSI mode serial transfer timing (slave mode) (during communication at different potential)**
**(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**




**Remark 1.** p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM and POM number (g = 0, 1, 3 to 5, 14)

**Remark 2.** CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.
Also, communication at different potential cannot be performed during clock synchronous serial communication with the slave select function.

### (10) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I²C mode)

**($T_A$ = -40 to +85°C, 1.8 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)** **(1/2)**

| Parameter | Symbol | Conditions | HS (high-speed main) mode | | LS (low-speed main) mode | | LV (low-voltage main) mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCLr clock frequency | $f_{SCL}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | | 1000 Note 1 | | 300 Note 1 | | 300 Note 1 | kHz |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | | 1000 Note 1 | | 300 Note 1 | | 300 Note 1 | kHz |
| | | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 100 pF, $R_b$ = 2.8 kΩ | | 400 Note 1 | | 300 Note 1 | | 300 Note 1 | kHz |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 100 pF, $R_b$ = 2.7 kΩ | | 400 Note 1 | | 300 Note 1 | | 300 Note 1 | kHz |
| | | 1.8 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2, $C_b$ = 100 pF, $R_b$ = 5.5 kΩ | | 300 Note 1 | | 300 Note 1 | | 300 Note 1 | kHz |
| Hold time when SCLr = “L” | $t_{LOW}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 475 | | 1550 | | 1550 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 475 | | 1550 | | 1550 | | ns |
| | | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 100 pF, $R_b$ = 2.8 kΩ | 1150 | | 1550 | | 1550 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 100 pF, $R_b$ = 2.7 kΩ | 1150 | | 1550 | | 1550 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2, $C_b$ = 100 pF, $R_b$ = 5.5 kΩ | 1550 | | 1550 | | 1550 | | ns |
| Hold time when SCLr = “H” | $t_{HIGH}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 245 | | 610 | | 610 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 200 | | 610 | | 610 | | ns |
| | | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 100 pF, $R_b$ = 2.8 kΩ | 675 | | 610 | | 610 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 100 pF, $R_b$ = 2.7 kΩ | 600 | | 610 | | 610 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2, $C_b$ = 100 pF, $R_b$ = 5.5 kΩ | 610 | | 610 | | 610 | | ns |

### (10) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified $I^2C$ mode)

**($T_A$ = -40 to +85°C, 1.8 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)** **(2/2)**

| Parameter | Symbol | Conditions | HS (high-speed main) mode | | LS (low-speed main) mode | | LV (low-voltage main) mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| Data setup time (reception) | $t_{SU:DAT}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 1/$f_{MCK}$ + 135 Note 3 | | 1/$f_{MCK}$ + 190 Note 3 | | 1/$f_{MCK}$ + 190 Note 3 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 1/$f_{MCK}$ + 135 Note 3 | | 1/$f_{MCK}$ + 190 Note 3 | | 1/$f_{MCK}$ + 190 Note 3 | | ns |
| | | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 100 pF, $R_b$ = 2.8 kΩ | 1/$f_{MCK}$ + 190 Note 3 | | 1/$f_{MCK}$ + 190 Note 3 | | 1/$f_{MCK}$ + 190 Note 3 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 100 pF, $R_b$ = 2.7 kΩ | 1/$f_{MCK}$ + 190 Note 3 | | 1/$f_{MCK}$ + 190 Note 3 | | 1/$f_{MCK}$ + 190 Note 3 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2, $C_b$ = 100 pF, $R_b$ = 5.5 kΩ | 1/$f_{MCK}$ + 190 Note 3 | | 1/$f_{MCK}$ + 190 Note 3 | | 1/$f_{MCK}$ + 190 Note 3 | | ns |
| Data hold time (transmission) | $t_{HD:DAT}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 0 | 305 | 0 | 305 | 0 | 305 | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 0 | 305 | 0 | 305 | 0 | 305 | ns |
| | | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 100 pF, $R_b$ = 2.8 kΩ | 0 | 355 | 0 | 355 | 0 | 355 | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 100 pF, $R_b$ = 2.7 kΩ | 0 | 355 | 0 | 355 | 0 | 355 | ns |
| | | 1.8 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2, $C_b$ = 100 pF, $R_b$ = 5.5 kΩ | 0 | 405 | 0 | 405 | 0 | 405 | ns |

**Note 1.** The value must also be equal to or less than $f_{MCK}$/4.

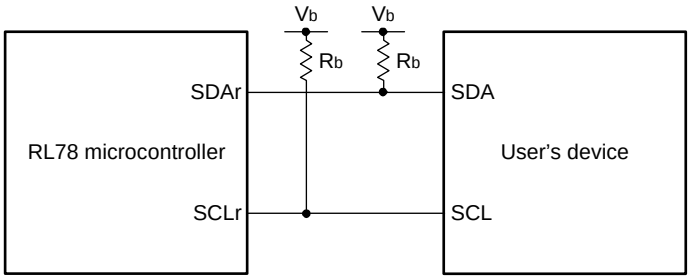
**Note 2.** Use it with $EV_{DD0}$ ≥ $V_b$.

**Note 3.** Set the $f_{MCK}$ value to keep the hold time of SCLr = “L” and SCLr = “H”.

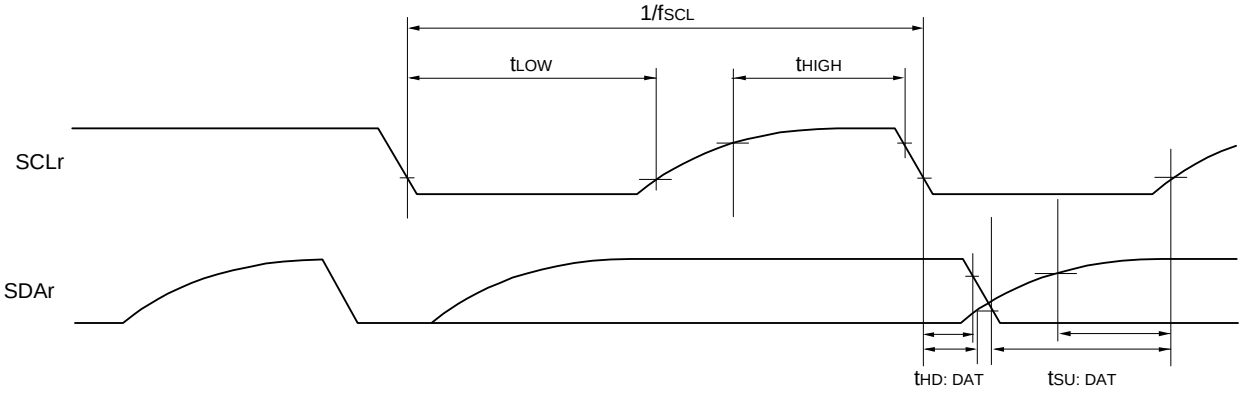
**Caution Select the TTL input buffer and the N-ch open drain output ($V_{DD}$ tolerance (for the 30- to 52-pin products)/$EV_{DD}$ tolerance (for the 64- to 100-pin products)) mode for the SDAr pin and the N-ch open drain output ($V_{DD}$ tolerance (for the 30- to 52-pin products)/$EV_{DD}$ tolerance (for the 64- to 100-pin products)) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

(**Remarks** are listed on the next page.)

**Simplified I²C mode connection diagram (during communication at different potential)**




**Simplified I²C mode serial transfer timing (during communication at different potential)**




**Remark 1.** $R_b$[Ω]: Communication line (SDAr, SCLr) pull-up resistance, $C_b$[F]: Communication line (SDAr, SCLr) load capacitance, $V_b$[V]: Communication line voltage

**Remark 2.** r: IIC number (r = 00, 01, 10, 11, 20, 30, 31), g: PIM, POM number (g = 0, 1, 3 to 5, 14)

**Remark 3.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), mn = 00, 01, 02, 10, 12, 13)

## 2.5.2 Serial interface IICA

### (1) $I^2C$ standard mode

**($T_A$ = -40 to +85°C, 1.6 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)** **(1/2)**

| Parameter | Symbol | Conditions | | HS (high-speed main) mode | | LS (low-speed main) mode | | LV (low-voltage main) mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCLA0 clock frequency | $f_{SCL}$ | Standard mode: $f_{CLK}$ ≥ 1 MHz | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | 0 | 100 | 0 | 100 | 0 | 100 | kHz |
| | | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | 0 | 100 | 0 | 100 | 0 | 100 | kHz |
| | | | 1.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | 0 | 100 | 0 | 100 | 0 | 100 | kHz |
| | | | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V | — | | 0 | 100 | 0 | 100 | kHz |
| Setup time of restart condition | $t_{SU: STA}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 4.7 | | 4.7 | | 4.7 | | µs |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 4.7 | | 4.7 | | 4.7 | | µs |
| | | 1.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 4.7 | | 4.7 | | 4.7 | | µs |
| | | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V | | — | | 4.7 | | 4.7 | | µs |
| Hold time Note 1 | $t_{HD: STA}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 4.0 | | 4.0 | | 4.0 | | µs |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 4.0 | | 4.0 | | 4.0 | | µs |
| | | 1.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 4.0 | | 4.0 | | 4.0 | | µs |
| | | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V | | — | | 4.0 | | 4.0 | | µs |
| Hold time when SCLA0 = “L” | $t_{LOW}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 4.7 | | 4.7 | | 4.7 | | µs |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 4.7 | | 4.7 | | 4.7 | | µs |
| | | 1.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 4.7 | | 4.7 | | 4.7 | | µs |
| | | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V | | — | | 4.7 | | 4.7 | | µs |
| Hold time when SCLA0 = “H” | $t_{HIGH}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 4.0 | | 4.0 | | 4.0 | | µs |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 4.0 | | 4.0 | | 4.0 | | µs |
| | | 1.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 4.0 | | 4.0 | | 4.0 | | µs |
| | | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V | | — | | 4.0 | | 4.0 | | µs |

(**Notes**, **Caution**, and **Remark** are listed on the next page.)

### (1) $I^2C$ standard mode

**($T_A$ = -40 to +85°C, 1.6 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)** **(2/2)**

| Parameter | Symbol | Conditions | HS (high-speed main) mode | | LS (low-speed main) mode | | LV (low-voltage main) mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| Data setup time (reception) | $t_{SU: DAT}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | 250 | | 250 | | 250 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | 250 | | 250 | | 250 | | ns |
| | | 1.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | 250 | | 250 | | 250 | | ns |
| | | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V | — | | 250 | | 250 | | ns |
| Data hold time (transmission) Note 2 | $t_{HD: DAT}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | 0 | 3.45 | 0 | 3.45 | 0 | 3.45 | µs |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | 0 | 3.45 | 0 | 3.45 | 0 | 3.45 | µs |
| | | 1.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | 0 | 3.45 | 0 | 3.45 | 0 | 3.45 | µs |
| | | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V | — | | 0 | 3.45 | 0 | 3.45 | µs |
| Setup time of stop condition | $t_{SU: STO}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | 4.0 | | 4.0 | | 4.0 | | µs |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | 4.0 | | 4.0 | | 4.0 | | µs |
| | | 1.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | 4.0 | | 4.0 | | 4.0 | | µs |
| | | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V | — | | 4.0 | | 4.0 | | µs |
| Bus-free time | $t_{BUF}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | 4.7 | | 4.7 | | 4.7 | | µs |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | 4.7 | | 4.7 | | 4.7 | | µs |
| | | 1.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | 4.7 | | 4.7 | | 4.7 | | µs |
| | | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V | — | | 4.7 | | 4.7 | | µs |

**Note 1.** The first clock pulse is generated after this period when the start/restart condition is detected.

**Note 2.** The maximum value (MAX.) of $t_{HD: DAT}$ is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

**Caution** **The values in the above table are applied even when bit 2 (PIOR02) in the peripheral I/O redirection register 0 (PIOR0) is 1. At this time, the pin characteristics ($I_{OH1}$, $I_{OL1}$, $V_{OH1}$, $V_{OL1}$) must satisfy the values in the redirect destination.**

**Remark** The maximum value of $C_b$ (communication line capacitance) and the value of $R_b$ (communication line pull-up resistor) at that time in each mode are as follows.

Standard mode: $C_b$ = 400 pF, $R_b$ = 2.7 kΩ

### (2) $I^2C$ fast mode

**($T_A$ = -40 to +85°C, 1.6 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) mode | | LS (low-speed main) mode | | LV (low-voltage main) mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCLA0 clock frequency | $f_{SCL}$ | Fast mode: $f_{CLK}$ ≥ 3.5 MHz | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | 0 | 400 | 0 | 400 | 0 | 400 | kHz |
| | | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | 0 | 400 | 0 | 400 | 0 | 400 | kHz |
| Setup time of restart condition | $t_{SU: STA}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 0.6 | | 0.6 | | 0.6 | | µs |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 0.6 | | 0.6 | | 0.6 | | µs |
| Hold time Note 1 | $t_{HD: STA}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 0.6 | | 0.6 | | 0.6 | | µs |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 0.6 | | 0.6 | | 0.6 | | µs |
| Hold time when SCLA0 = “L” | $t_{LOW}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 1.3 | | 1.3 | | 1.3 | | µs |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 1.3 | | 1.3 | | 1.3 | | µs |
| Hold time when SCLA0 = “H” | $t_{HIGH}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 0.6 | | 0.6 | | 0.6 | | µs |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 0.6 | | 0.6 | | 0.6 | | µs |
| Data setup time (reception) | $t_{SU: DAT}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 100 | | 100 | | 100 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 100 | | 100 | | 100 | | ns |
| Data hold time (transmission) Note 2 | $t_{HD: DAT}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 0 | 0.9 | 0 | 0.9 | 0 | 0.9 | µs |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 0 | 0.9 | 0 | 0.9 | 0 | 0.9 | µs |
| Setup time of stop condition | $t_{SU: STO}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 0.6 | | 0.6 | | 0.6 | | µs |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 0.6 | | 0.6 | | 0.6 | | µs |
| Bus-free time | $t_{BUF}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 1.3 | | 1.3 | | 1.3 | | µs |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 1.3 | | 1.3 | | 1.3 | | µs |

**Note 1.** The first clock pulse is generated after this period when the start/restart condition is detected.

**Note 2.** The maximum value (MAX.) of $t_{HD: DAT}$ is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

**Caution The values in the above table are applied even when bit 2 (PIOR02) in the peripheral I/O redirection register 0 (PIOR0) is 1. At this time, the pin characteristics ($I_{OH1}$, $I_{OL1}$, $V_{OH1}$, $V_{OL1}$) must satisfy the values in the redirect destination.**

**Remark** The maximum value of $C_b$ (communication line capacitance) and the value of $R_b$ (communication line pull-up resistor) at that time in each mode are as follows.

Fast mode: $C_b$ = 320 pF, $R_b$ = 1.1 kΩ

### (3) $I^2C$ fast mode plus

**($T_A$ = -40 to +85°C, 1.6 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) mode | | LS (low-speed main) mode | | LV (low-voltage main) mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCLA0 clock frequency | $f_{SCL}$ | Fast mode plus: $f_{CLK}$ ≥ 10 MHz | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | 0 | 1000 | — | | — | | kHz |
| Setup time of restart condition | $t_{SU: STA}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 0.26 | | — | | — | | µs |
| Hold time Note 1 | $t_{HD: STA}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 0.26 | | — | | — | | µs |
| Hold time when SCLA0 = "L" | $t_{LOW}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 0.5 | | — | | — | | µs |
| Hold time when SCLA0 = "H" | $t_{HIGH}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 0.26 | | — | | — | | µs |
| Data setup time (reception) | $t_{SU: DAT}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 50 | | — | | — | | ns |
| Data hold time (transmission) Note 2 | $t_{HD: DAT}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 0 | 0.45 | — | | — | | µs |
| Setup time of stop condition | $t_{SU: STO}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 0.26 | | — | | — | | µs |
| Bus-free time | $t_{BUF}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 0.5 | | — | | — | | µs |

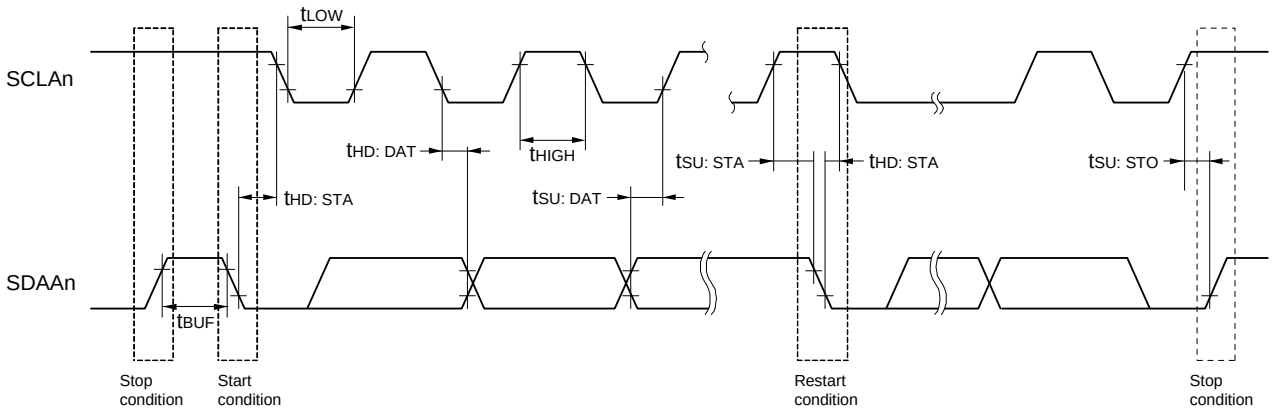
**Note 1.** The first clock pulse is generated after this period when the start/restart condition is detected.

**Note 2.** The maximum value (MAX.) of $t_{HD: DAT}$ is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

**Caution The values in the above table are applied even when bit 2 (PIOR02) in the peripheral I/O redirection register 0 (PIOR0) is 1. At this time, the pin characteristics ($I_{OH1}$, $I_{OL1}$, $V_{OH1}$, $V_{OL1}$) must satisfy the values in the redirect destination.**

**Note 3.** The maximum value of $C_b$ (communication line capacitance) and the value of $R_b$ (communication line pull-up resistor) at that time in each mode are as follows.
Fast mode plus: $C_b$ = 120 pF, $R_b$ = 1.1 kΩ

**IICA serial transfer timing**




**Remark** n = 0, 1

## 2.6 Analog Characteristics

### 2.6.1 A/D converter characteristics

**Classification of A/D converter characteristics**

| Reference Voltage / Input channel | Reference voltage (+) = $AV_{REFP}$ Reference voltage (-) = $AV_{REFM}$ | Reference voltage (+) = $V_{DD}$ Reference voltage (-) = $V_{SS}$ | Reference voltage (+) = $V_{BGR}$ Reference voltage (-)= $AV_{REFM}$ |
|---|---|---|---|
| ANI0 to ANI14 | Refer to **2.6.1 (1)**. | Refer to **2.6.1 (3)**. | Refer to **2.6.1 (4)**. |
| ANI16 to ANI20 | Refer to **2.6.1 (2)**. | | |
| Internal reference voltage<br>Temperature sensor output voltage | Refer to **2.6.1 (1)**. | | — |

**(1) When reference voltage (+) = $AV_{REFP}$/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = $AV_{REFM}$/ANI1 (ADREFM = 1), target pin: ANI2 to ANI14, internal reference voltage, and temperature sensor output voltage**

**($T_A$ = -40 to +85°C, 1.6 V ≤ $AV_{REFP}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V, Reference voltage (+) = $AV_{REFP}$, Reference voltage (-) = $AV_{REFM}$ = 0 V)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Resolution | RES | | | 8 | | 10 | bit |
| Overall error Note 1 | AINL | 10-bit resolution<br>$AV_{REFP}$ = $V_{DD}$ Note 3 | 1.8 V ≤ $AV_{REFP}$ ≤ 5.5 V | | 1.2 | ±3.5 | LSB |
| | | | 1.6 V ≤ $AV_{REFP}$ ≤ 5.5 V Note 4 | | 1.2 | ±7.0 | LSB |
| Conversion time | $t_{CONV}$ | 10-bit resolution<br>Target pin: ANI2 to ANI14 | 3.6 V ≤ $V_{DD}$ ≤ 5.5 V | 2.125 | | 39 | μs |
| | | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 3.1875 | | 39 | μs |
| | | | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | 17 | | 39 | μs |
| | | | 1.6 V ≤ $V_{DD}$ ≤ 5.5 V | 57 | | 95 | μs |
| | | 10-bit resolution<br>Target pin: Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode) | 3.6 V ≤ $V_{DD}$ ≤ 5.5 V | 2.375 | | 39 | μs |
| | | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 3.5625 | | 39 | μs |
| | | | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | 17 | | 39 | μs |
| Zero-scale error Notes 1, 2 | $E_{ZS}$ | 10-bit resolution<br>$AV_{REFP}$ = $V_{DD}$ Note 3 | 1.8 V ≤ $AV_{REFP}$ ≤ 5.5 V | | | ±0.25 | %FSR |
| | | | 1.6 V ≤ $AV_{REFP}$ ≤ 5.5 V Note 4 | | | ±0.50 | %FSR |
| Full-scale error Notes 1, 2 | $E_{FS}$ | 10-bit resolution<br>$AV_{REFP}$ = $V_{DD}$ Note 3 | 1.8 V ≤ $AV_{REFP}$ ≤ 5.5 V | | | ±0.25 | %FSR |
| | | | 1.6 V ≤ $AV_{REFP}$ ≤ 5.5 V Note 4 | | | ±0.50 | %FSR |
| Integral linearity error Note 1 | ILE | 10-bit resolution<br>$AV_{REFP}$ = $V_{DD}$ Note 3 | 1.8 V ≤ $AV_{REFP}$ ≤ 5.5 V | | | ±2.5 | LSB |
| | | | 1.6 V ≤ $AV_{REFP}$ ≤ 5.5 V Note 4 | | | ±5.0 | LSB |
| Differential linearity error Note 1 | DLE | 10-bit resolution<br>$AV_{REFP}$ = $V_{DD}$ Note 3 | 1.8 V ≤ $AV_{REFP}$ ≤ 5.5 V | | | ±1.5 | LSB |
| | | | 1.6 V ≤ $AV_{REFP}$ ≤ 5.5 V Note 4 | | | ±2.0 | LSB |
| Analog input voltage | $V_{AIN}$ | ANI2 to ANI14 | | 0 | | $AV_{REFP}$ | V |
| | | Internal reference voltage<br>(2.4 V ≤ $V_{DD}$ ≤ 5.5 V, HS (high-speed main) mode) | | $V_{BGR}$ Note 5 | | | V |
| | | Temperature sensor output voltage<br>(2.4 V ≤ $V_{DD}$ ≤ 5.5 V, HS (high-speed main) mode) | | $V_{TMPS25}$ Note 5 | | | V |

**Note 1.** Excludes quantization error (±1/2 LSB).

**Note 2.** This value is indicated as a ratio (%FSR) to the full-scale value.

**Note 3.** When $AV_{REFP}$ < $V_{DD}$, the MAX. values are as follows.

Overall error: Add ±1.0 LSB to the MAX. value when $AV_{REFP}$ = $V_{DD}$.

Zero-scale error/Full-scale error: Add ±0.05%FSR to the MAX. value when $AV_{REFP}$ = $V_{DD}$.

Integral linearity error/ Differential linearity error: Add ±0.5 LSB to the MAX. value when $AV_{REFP}$ = $V_{DD}$.

**Note 4.** Values when the conversion time is set to 57 μs (min.) and 95 μs (max.).

**Note 5.** Refer to **2.6.2 Temperature sensor characteristics/internal reference voltage characteristic**.

**(2) When reference voltage (+) = $AV_{REFP}$/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = $AV_{REFM}$/ANI1 (ADREFM = 1), target pin: ANI16 to ANI20**

**($T_A$ = -40 to +85°C, 1.6 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, 1.6 V ≤ $AV_{REFP}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V, Reference voltage (+) = $AV_{REFP}$, Reference voltage (-) = $AV_{REFM}$ = 0 V)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Resolution | RES | | | 8 | | 10 | bit |
| Overall error Note 1 | AINL | 10-bit resolution<br>$EV_{DD0}$ ≤ $AV_{REFP}$ = $V_{DD}$ Notes 3, 4 | 1.8 V ≤ $AV_{REFP}$ ≤ 5.5 V | | 1.2 | ±5.0 | LSB |
| | | | 1.6 V ≤ $AV_{REFP}$ ≤ 5.5 V Note 5 | | 1.2 | ±8.5 | LSB |
| Conversion time | $t_{CONV}$ | 10-bit resolution<br>Target ANI pin: ANI16 to ANI20 | 3.6 V ≤ $V_{DD}$ ≤ 5.5 V | 2.125 | | 39 | μs |
| | | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 3.1875 | | 39 | μs |
| | | | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | 17 | | 39 | μs |
| | | | 1.6 V ≤ $V_{DD}$ ≤ 5.5 V | 57 | | 95 | μs |
| Zero-scale error Notes 1, 2 | $E_{ZS}$ | 10-bit resolution<br>$EV_{DD0}$ ≤ $AV_{REFP}$ = $V_{DD}$ Notes 3, 4 | 1.8 V ≤ $AV_{REFP}$ ≤ 5.5 V | | | ±0.35 | %FSR |
| | | | 1.6 V ≤ $AV_{REFP}$ ≤ 5.5 V Note 5 | | | ±0.60 | %FSR |
| Full-scale error Notes 1, 2 | $E_{FS}$ | 10-bit resolution<br>$EV_{DD0}$ ≤ $AV_{REFP}$ = $V_{DD}$ Notes 3, 4 | 1.8 V ≤ $AV_{REFP}$ ≤ 5.5 V | | | ±0.35 | %FSR |
| | | | 1.6 V ≤ $AV_{REFP}$ ≤ 5.5 V Note 5 | | | ±0.60 | %FSR |
| Integral linearity error Note 1 | ILE | 10-bit resolution<br>$EV_{DD0}$ ≤ $AV_{REFP}$ = $V_{DD}$ Notes 3, 4 | 1.8 V ≤ $AV_{REFP}$ ≤ 5.5 V | | | ±3.5 | LSB |
| | | | 1.6 V ≤ $AV_{REFP}$ ≤ 5.5 V Note 5 | | | ±6.0 | LSB |
| Differential linearity error Note 1 | DLE | 10-bit resolution<br>$EV_{DD0}$ ≤ $AV_{REFP}$ = $V_{DD}$ Notes 3, 4 | 1.8 V ≤ $AV_{REFP}$ ≤ 5.5 V | | | ±2.0 | LSB |
| | | | 1.6 V ≤ $AV_{REFP}$ ≤ 5.5 V Note 5 | | | ±2.5 | LSB |
| Analog input voltage | $V_{AIN}$ | ANI16 to ANI20 | | 0 | | $AV_{REFP}$ and $EV_{DD0}$ | V |

**Note 1.** Excludes quantization error (±1/2 LSB).

**Note 2.** This value is indicated as a ratio (%FSR) to the full-scale value.

**Note 3.** When $EV_{DD0}$ ≤ $AV_{REFP}$ ≤ $V_{DD}$, the MAX. values are as follows.

Overall error: Add ±1.0 LSB to the MAX. value when $AV_{REFP}$ = $V_{DD}$.

Zero-scale error/Full-scale error: Add ±0.05%FSR to the MAX. value when $AV_{REFP}$ = $V_{DD}$.

Integral linearity error/ Differential linearity error: Add ±0.5 LSB to the MAX. value when $AV_{REFP}$ = $V_{DD}$.

**Note 4.** When $AV_{REFP}$ < $EV_{DD0}$ ≤ $V_{DD}$, the MAX. values are as follows.

Overall error: Add ±4.0 LSB to the MAX. value when $AV_{REFP}$ = $V_{DD}$.

Zero-scale error/Full-scale error: Add ±0.20%FSR to the MAX. value when $AV_{REFP}$ = $V_{DD}$.

Integral linearity error/ Differential linearity error: Add ±2.0 LSB to the MAX. value when $AV_{REFP}$ = $V_{DD}$.

**Note 5.** When the conversion time is set to 57 μs (min.) and 95 μs (max.).

### (3) When reference voltage (+) = $V_{DD}$ (ADREFP1 = 0, ADREFP0 = 0), reference voltage (-) = $V_{SS}$ (ADREFM = 0), target pin: ANI0 to ANI14, ANI16 to ANI20, internal reference voltage, and temperature sensor output voltage

**($T_A$ = -40 to +85°C, 1.6 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V, Reference voltage (+) = $V_{DD}$, Reference voltage (-) = $V_{SS}$)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Resolution | RES | | | 8 | | 10 | bit |
| Overall error Note 1 | AINL | 10-bit resolution | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | | 1.2 | ±7.0 | LSB |
| | | | 1.6 V ≤ $V_{DD}$ ≤ 5.5 V Note 3 | | 1.2 | ±10.5 | LSB |
| Conversion time | $t_{CONV}$ | 10-bit resolution<br>Target pin: ANI0 to ANI14, ANI16 to ANI20 | 3.6 V ≤ $V_{DD}$ ≤ 5.5 V | 2.125 | | 39 | μs |
| | | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 3.1875 | | 39 | μs |
| | | | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | 17 | | 39 | μs |
| | | | 1.6 V ≤ $V_{DD}$ ≤ 5.5 V | 57 | | 95 | μs |
| | | 10-bit resolution<br>Target pin: internal reference voltage, and temperature sensor output voltage<br>(HS (high-speed main) mode) | 3.6 V ≤ $V_{DD}$ ≤ 5.5 V | 2.375 | | 39 | μs |
| | | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 3.5625 | | 39 | μs |
| | | | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | 17 | | 39 | μs |
| Zero-scale error Notes 1, 2 | $E_{ZS}$ | 10-bit resolution | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | | | ±0.60 | %FSR |
| | | | 1.6 V ≤ $V_{DD}$ ≤ 5.5 V Note 3 | | | ±0.85 | %FSR |
| Full-scale error Notes 1, 2 | $E_{FS}$ | 10-bit resolution | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | | | ±0.60 | %FSR |
| | | | 1.6 V ≤ $V_{DD}$ ≤ 5.5 V Note 3 | | | ±0.85 | %FSR |
| Integral linearity error Note 1 | ILE | 10-bit resolution | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | | | ±4.0 | LSB |
| | | | 1.6 V ≤ $V_{DD}$ ≤ 5.5 V Note 3 | | | ±6.5 | LSB |
| Differential linearity error Note 1 | DLE | 10-bit resolution | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | | | ±2.0 | LSB |
| | | | 1.6 V ≤ $V_{DD}$ ≤ 5.5 V Note 3 | | | ±2.5 | LSB |
| Analog input voltage | $V_{AIN}$ | ANI0 to ANI14 | | 0 | | $V_{DD}$ | V |
| | | ANI16 to ANI20 | | 0 | | $EV_{DD0}$ | V |
| | | Internal reference voltage<br>(2.4 V ≤ $V_{DD}$ ≤ 5.5 V, HS (high-speed main) mode) | | $V_{BGR}$ Note 4 | | | V |
| | | Temperature sensor output voltage<br>(2.4 V ≤ $V_{DD}$ ≤ 5.5 V, HS (high-speed main) mode) | | $V_{TMPS25}$ Note 4 | | | V |

**Note 1.** Excludes quantization error (±1/2 LSB).

**Note 2.** This value is indicated as a ratio (% FSR) to the full-scale value.

**Note 3.** When the conversion time is set to 57 μs (min.) and 95 μs (max.).

**Note 4.** Refer to **2.6.2 Temperature sensor characteristics/internal reference voltage characteristic**.

**(4) When reference voltage (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), reference voltage (-) = $AV_{REFM}$/ANI1 (ADREFM = 1), target pin: ANI0, ANI2 to ANI14, ANI16 to ANI20**

**($T_A$ = -40 to +85°C, 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, 1.6 V ≤ $EV_{DD}$ = $EV_{DD1}$ ≤ $V_{DD}$, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V, Reference voltage (+) = $V_{BGR}$ Note 3, Reference voltage (-) = $AV_{REFM}$ = 0 V Note 4, HS (high-speed main) mode)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Resolution | RES | | | | 8 | | bit |
| Conversion time | $t_{CONV}$ | 8-bit resolution | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | 17 | | 39 | μs |
| Zero-scale error Notes 1, 2 | $E_{ZS}$ | 8-bit resolution | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | | | ±0.60 | % FSR |
| Integral linearity error Note 1 | ILE | 8-bit resolution | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | | | ±2.0 | LSB |
| Differential linearity error Note 1 | DLE | 8-bit resolution | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | | | ±1.0 | LSB |
| Analog input voltage | $V_{AIN}$ | | | 0 | | $V_{BGR}$ Note 3 | V |

**Note 1.** Excludes quantization error (±1/2 LSB).

**Note 2.** This value is indicated as a ratio (% FSR) to the full-scale value.

**Note 3.** Refer to **2.6.2 Temperature sensor characteristics/internal reference voltage characteristic**.

**Note 4.** When reference voltage (-) = $V_{SS}$, the MAX. values are as follows.

Zero-scale error: Add ±0.35%FSR to the MAX. value when reference voltage (-) = $AV_{REFM}$.

Integral linearity error: Add ±0.5 LSB to the MAX. value when reference voltage (-) = $AV_{REFM}$.

Differential linearity error: Add ±0.2 LSB to the MAX. value when reference voltage (-) = $AV_{REFM}$.

### 2.6.2 Temperature sensor characteristics/internal reference voltage characteristic

**($T_A$ = -40 to +85°C, 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V, HS (high-speed main) mode)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Temperature sensor output voltage | $V_{TMPS25}$ | Setting ADS register = 80H, $T_A$ = +25°C | | 1.05 | | V |
| Internal reference voltage | $V_{BGR}$ | Setting ADS register = 81H | 1.38 | 1.45 | 1.5 | V |
| Temperature coefficient | $F_{VTMPS}$ | Temperature sensor that depends on the temperature | | -3.6 | | mV/°C |
| Operation stabilization wait time | $t_{AMP}$ | | 5 | | | μs |

### 2.6.3 D/A converter characteristics

**($T_A$ = -40 to +85°C, 1.6 V ≤ $EV_{SS0}$ = $EV_{SS1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Resolution | RES | | | | | 8 | bit |
| Overall error | AINL | Rload = 4 MΩ | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | | | ±2.5 | LSB |
| | | Rload = 8 MΩ | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | | | ±2.5 | LSB |
| Settling time | $t_{SET}$ | Cload = 20 pF | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | | | 3 | μs |
| | | | 1.6 V ≤ $V_{DD}$ < 2.7 V | | | 6 | μs |

## 2.6.4 Comparator

**($T_A$ = -40 to +85°C, 1.6 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Input voltage range | Ivref | | | 0 | | $EV_{DD0}$ - 1.4 | V |
| | Ivcmp | | | -0.3 | | $EV_{DD0}$ + 0.3 | V |
| Output delay | td | $V_{DD}$ = 3.0 V<br>Input slew rate > 50 mV/µs | Comparator high-speed mode, standard mode | | | 1.2 | µs |
| | | | Comparator high-speed mode, window mode | | | 2.0 | µs |
| | | | Comparator low-speed mode, standard mode | | 3.0 | 5.0 | µs |
| High-electric-potential reference voltage | VTW+ | Comparator high-speed mode, window mode | | | 0.76 $V_{DD}$ | | V |
| Low-electric-potential reference voltage | VTW- | Comparator high-speed mode, window mode | | | 0.24 $V_{DD}$ | | V |
| Operation stabilization wait time | $t_{CMP}$ | | | 100 | | | µs |
| Internal reference voltage Note | $V_{BGR}$ | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, HS (high-speed main) mode | | 1.38 | 1.45 | 1.50 | V |

**Note** Not usable in LS (low-speed main) mode, LV (low-voltage main) mode, sub-clock operation, or STOP mode.

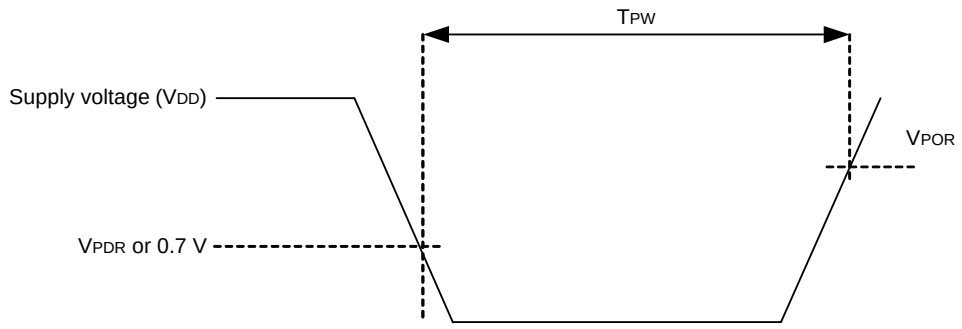
## 2.6.5 POR circuit characteristics

**($T_A$ = -40 to +85°C, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Power on/down reset threshold | $V_{POR}$ | Voltage threshold on $V_{DD}$ rising | 1.47 | 1.51 | 1.55 | V |
| | $V_{PDR}$ | Voltage threshold on $V_{DD}$ falling Note 1 | 1.46 | 1.50 | 1.54 | V |
| Minimum pulse width Note 2 | $T_{PW}$ | | 300 | | | µs |

**Note 1.** However, when the operating voltage falls while the LVD is off, enter STOP mode, or enable the reset status using the external reset pin before the voltage falls below the operating voltage range shown in 2.4 AC Characteristics.

**Note 2.** Minimum time required for a POR reset when $V_{DD}$ exceeds below $V_{PDR}$. This is also the minimum time required for a POR reset from when $V_{DD}$ exceeds below 0.7 V to when $V_{DD}$ exceeds $V_{POR}$ while STOP mode is entered or the main system clock is stopped through setting bit 0 (HIOSTOP) and bit 7 (MSTOP) in the clock operation status control register (CSC).



## 2.6.6 LVD circuit characteristics

**(1) Reset Mode and Interrupt Mode**

**($T_A$ = -40 to +85°C, $V_{PDR} \leq V_{DD} \leq$ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Voltage detection threshold | Supply voltage level | $V_{LVD0}$ | Rising edge | 3.98 | 4.06 | 4.14 | V |
| | | | Falling edge | 3.90 | 3.98 | 4.06 | V |
| | | $V_{LVD1}$ | Rising edge | 3.68 | 3.75 | 3.82 | V |
| | | | Falling edge | 3.60 | 3.67 | 3.74 | V |
| | | $V_{LVD2}$ | Rising edge | 3.07 | 3.13 | 3.19 | V |
| | | | Falling edge | 3.00 | 3.06 | 3.12 | V |
| | | $V_{LVD3}$ | Rising edge | 2.96 | 3.02 | 3.08 | V |
| | | | Falling edge | 2.90 | 2.96 | 3.02 | V |
| | | $V_{LVD4}$ | Rising edge | 2.86 | 2.92 | 2.97 | V |
| | | | Falling edge | 2.80 | 2.86 | 2.91 | V |
| | | $V_{LVD5}$ | Rising edge | 2.76 | 2.81 | 2.87 | V |
| | | | Falling edge | 2.70 | 2.75 | 2.81 | V |
| | | $V_{LVD6}$ | Rising edge | 2.66 | 2.71 | 2.76 | V |
| | | | Falling edge | 2.60 | 2.65 | 2.70 | V |
| | | $V_{LVD7}$ | Rising edge | 2.56 | 2.61 | 2.66 | V |
| | | | Falling edge | 2.50 | 2.55 | 2.60 | V |
| | | $V_{LVD8}$ | Rising edge | 2.45 | 2.50 | 2.55 | V |
| | | | Falling edge | 2.40 | 2.45 | 2.50 | V |
| | | $V_{LVD9}$ | Rising edge | 2.05 | 2.09 | 2.13 | V |
| | | | Falling edge | 2.00 | 2.04 | 2.08 | V |
| | | $V_{LVD10}$ | Rising edge | 1.94 | 1.98 | 2.02 | V |
| | | | Falling edge | 1.90 | 1.94 | 1.98 | V |
| | | $V_{LVD11}$ | Rising edge | 1.84 | 1.88 | 1.91 | V |
| | | | Falling edge | 1.80 | 1.84 | 1.87 | V |
| | | $V_{LVD12}$ | Rising edge | 1.74 | 1.77 | 1.81 | V |
| | | | Falling edge | 1.70 | 1.73 | 1.77 | V |
| | | $V_{LVD13}$ | Rising edge | 1.64 | 1.67 | 1.70 | V |
| | | | Falling edge | 1.60 | 1.63 | 1.66 | V |
| Minimum pulse width | | $t_{LW}$ | | 300 | | | µs |
| Detection delay time | | | | | | 300 | µs |

**(2) Interrupt & Reset Mode**

**($T_A$ = -40 to +85°C, $V_{PDR} \le V_{DD} \le$ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|
| Voltage detection threshold | $V_{LVDA0}$ | $V_{POC2}$, $V_{POC1}$, $V_{POC0}$ = 0, 0, 0, falling reset voltage | | | 1.60 | 1.63 | 1.66 | V |
| | $V_{LVDA1}$ | LVIS1, LVIS0 = 1, 0 | | Rising release reset voltage | 1.74 | 1.77 | 1.81 | V |
| | | | | Falling interrupt voltage | 1.70 | 1.73 | 1.77 | V |
| | $V_{LVDA2}$ | LVIS1, LVIS0 = 0, 1 | | Rising release reset voltage | 1.84 | 1.88 | 1.91 | V |
| | | | | Falling interrupt voltage | 1.80 | 1.84 | 1.87 | V |
| | $V_{LVDA3}$ | LVIS1, LVIS0 = 0, 0 | | Rising release reset voltage | 2.86 | 2.92 | 2.97 | V |
| | | | | Falling interrupt voltage | 2.80 | 2.86 | 2.91 | V |
| | $V_{LVDB0}$ | $V_{POC2}$, $V_{POC1}$, $V_{POC0}$ = 0, 0, 1, falling reset voltage | | | 1.80 | 1.84 | 1.87 | V |
| | $V_{LVDB1}$ | LVIS1, LVIS0 = 1, 0 | | Rising release reset voltage | 1.94 | 1.98 | 2.02 | V |
| | | | | Falling interrupt voltage | 1.90 | 1.94 | 1.98 | V |
| | $V_{LVDB2}$ | LVIS1, LVIS0 = 0, 1 | | Rising release reset voltage | 2.05 | 2.09 | 2.13 | V |
| | | | | Falling interrupt voltage | 2.00 | 2.04 | 2.08 | V |
| | $V_{LVDB3}$ | LVIS1, LVIS0 = 0, 0 | | Rising release reset voltage | 3.07 | 3.13 | 3.19 | V |
| | | | | Falling interrupt voltage | 3.00 | 3.06 | 3.12 | V |
| | $V_{LVDC0}$ | $V_{POC2}$, $V_{POC1}$, $V_{POC0}$ = 0, 1, 0, falling reset voltage | | | 2.40 | 2.45 | 2.50 | V |
| | $V_{LVDC1}$ | LVIS1, LVIS0 = 1, 0 | | Rising release reset voltage | 2.56 | 2.61 | 2.66 | V |
| | | | | Falling interrupt voltage | 2.50 | 2.55 | 2.60 | V |
| | $V_{LVDC2}$ | LVIS1, LVIS0 = 0, 1 | | Rising release reset voltage | 2.66 | 2.71 | 2.76 | V |
| | | | | Falling interrupt voltage | 2.60 | 2.65 | 2.70 | V |
| | $V_{LVDC3}$ | LVIS1, LVIS0 = 0, 0 | | Rising release reset voltage | 3.68 | 3.75 | 3.82 | V |
| | | | | Falling interrupt voltage | 3.60 | 3.67 | 3.74 | V |
| | $V_{LVDD0}$ | $V_{POC2}$, $V_{POC1}$, $V_{POC0}$ = 0, 1, 1, falling reset voltage | | | 2.70 | 2.75 | 2.81 | V |
| | $V_{LVDD1}$ | LVIS1, LVIS0 = 1, 0 | | Rising release reset voltage | 2.86 | 2.92 | 2.97 | V |
| | | | | Falling interrupt voltage | 2.80 | 2.86 | 2.91 | V |
| | $V_{LVDD2}$ | LVIS1, LVIS0 = 0, 1 | | Rising release reset voltage | 2.96 | 3.02 | 3.08 | V |
| | | | | Falling interrupt voltage | 2.90 | 2.96 | 3.02 | V |
| | $V_{LVDD3}$ | LVIS1, LVIS0 = 0, 0 | | Rising release reset voltage | 3.98 | 4.06 | 4.14 | V |
| | | | | Falling interrupt voltage | 3.90 | 3.98 | 4.06 | V |

## 2.6.7 Power supply voltage rising slope characteristics

**($T_A$ = -40 to +85°C, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Power supply voltage rising slope | $S_{VDD}$ | | | | 54 | V/ms |

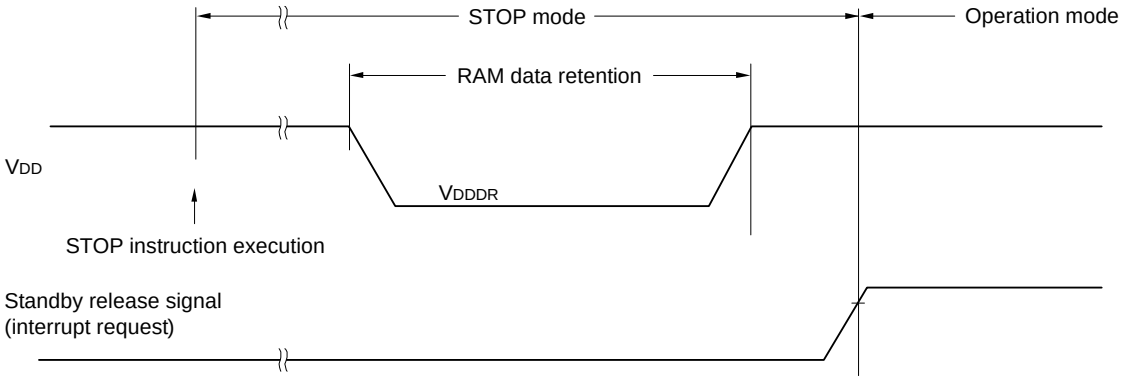
**Caution Make sure to keep the internal reset state by the LVD circuit or an external reset until $V_{DD}$ reaches the operating voltage range shown in 2.4 AC Characteristics.**

## 2.7 RAM Data Retention Characteristics

**($T_A$ = -40 to +85°C, $V_{SS}$ = 0V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Data retention supply voltage | $V_{DDDR}$ | | 1.46 Note | | 5.5 | V |

**Note** The value depends on the POR detection voltage. When the voltage drops, the RAM data is retained before a POR reset is effected, but RAM data is not retained when a POR reset is effected.




## 2.8 Flash Memory Programming Characteristics

**($T_A$ = -40 to +85°C, 1.8 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| System clock frequency | $f_{CLK}$ | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | 1 | | 32 | MHz |
| Number of code flash rewrites<br>Notes 1, 2, 3 | $C_{erwr}$ | Retained for 20 years<br>$T_A$ = 85°C | 1,000 | | | Times |
| Number of data flash rewrites<br>Notes 1, 2, 3 | | Retained for 1 year<br>$T_A$ = 25°C | | 1,000,000 | | |
| | | Retained for 5 years<br>$T_A$ = 85°C | 100,000 | | | |
| | | Retained for 20 years<br>$T_A$ = 85°C | 10,000 | | | |

**Note 1.** 1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until next rewrite after the rewrite.

**Note 2.** When using flash memory programmer and Renesas Electronics self-programming library

**Note 3.** These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

## 2.9 Dedicated Flash Memory Programmer Communication (UART)

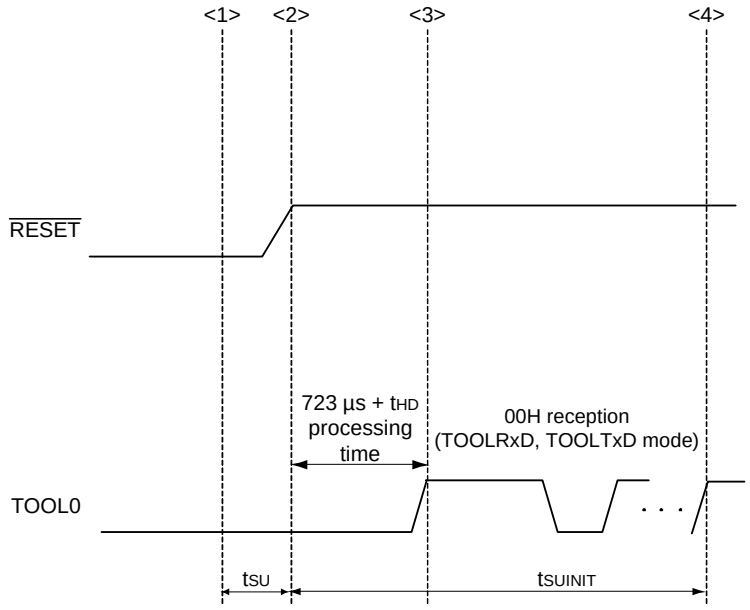
**($T_A$ = -40 to +85°C, 1.8 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Transfer rate | | During serial programming | 115,200 | | 1,000,000 | bps |

## 2.10 Timing of Entry to Flash Memory Programming Modes

**($T_A$ = -40 to +85°C, 1.8 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| How long from when an external reset ends until the initial communication settings are specified | $t_{SUINIT}$ | POR and LVD reset must end before the external reset ends. | | | 100 | ms |
| How long from when the TOOL0 pin is placed at the low level until an external reset ends | $t_{SU}$ | POR and LVD reset must end before the external reset ends. | 10 | | | μs |
| How long the TOOL0 pin must be kept at the low level after an external reset ends (excluding the processing time of the firmware to control the flash memory) | $t_{HD}$ | POR and LVD reset must end before the external reset ends. | 1 | | | ms |




<1> The low level is input to the TOOL0 pin.
<2> The external reset ends (POR and LVD reset must end before the external reset ends).
<3> The TOOL0 pin is set to the high level.
<4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

**Remark** $t_{SUINIT}$: The segment shows that it is necessary to finish specifying the initial communication settings within 100 ms from when the external resets end.
$t_{SU}$: How long from when the TOOL0 pin is placed at the low level until a pin reset ends
$t_{HD}$: How long to keep the TOOL0 pin at the low level from when the external resets end (excluding the processing time of the firmware to control the flash memory)

# 3. ELECTRICAL SPECIFICATIONS (G: INDUSTRIAL APPLICATIONS $T_A$ = -40 to +105°C)

This chapter describes the following electrical specifications.

Target products G: Industrial applications $T_A$ = -40 to +105°C

R5F104xxGxx

**Caution 1. The RL78 microcontrollers have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.**

**Caution 2. With products not provided with an $EV_{DD0}$, $EV_{DD1}$, $EV_{SS0}$, or $EV_{SS1}$ pin, replace $EV_{DD0}$ and $EV_{DD1}$ with $V_{DD}$, or replace $EV_{SS0}$ and $EV_{SS1}$ with $V_{SS}$.**

**Caution 3. The pins mounted depend on the product. Refer to 2.1 Port Functions to 2.2.1 Functions for each product in the RL78/G14 User's Manual.**

**Caution 4. Please contact Renesas Electronics sales office for derating of operation under $T_A$ = +85 to +105°C. Derating is the systematic reduction of load for the sake of improved reliability.**

**Remark** When RL78/G14 is used in the range of $T_A$ = -40 to +85°C, see **2. ELECTRICAL SPECIFICATIONS ($T_A$ = -40 to +85°C)**.

Operation of products rated “G: Industrial applications ($T_A$ = -40 to + 105°C)” at ambient operating temperatures above 85°C differs from that of products rated “A: Consumer applications” and “D: Industrial applications” in the ways listed below.

| Parameter | A: Consumer applications, D: Industrial applications | G: Industrial applications |
|---|---|---|
| Operating ambient temperature | $T_A$ = -40 to +85°C | $T_A$ = -40 to +105°C |
| Operating mode<br>Operating voltage range | HS (high-speed main) mode:<br>2.7 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 32 MHz<br>2.4 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 16 MHz<br>LS (low-speed main) mode:<br>1.8 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 8 MHz<br>LV (low-voltage main) mode:<br>1.6 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 4 MHz | HS (high-speed main) mode only:<br>2.7 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 32 MHz<br>2.4 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 16 MHz |
| High-speed on-chip oscillator clock accuracy | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V:<br>±1.0% @ $T_A$ = -20 to +85°C<br>±1.5% @ $T_A$ = -40 to -20°C<br>1.6 V ≤ $V_{DD}$ < 1.8 V:<br>±5.0% @ $T_A$ = -20 to +85°C<br>±5.5% @ $T_A$ = -40 to -20°C | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V:<br>±2.0% @ $T_A$ = +85 to +105°C<br>±1.0% @ $T_A$ = -20 to +85°C<br>±1.5% @ $T_A$ = -40 to -20°C |
| Serial array unit | UART<br>CSI: $f_{CLK}$/2 (16 Mbps supported), $f_{CLK}$/4<br>Simplified $I^2C$ communication | UART<br>CSI: $f_{CLK}$/4<br>Simplified $I^2C$ communication |
| IICA | Standard mode<br>Fast mode<br>Fast mode plus | Standard mode<br>Fast mode |
| Voltage detector | • Rising: 1.67 V to 4.06 V (14 stages)<br>• Falling: 1.63 V to 3.98 V (14 stages) | • Rising: 2.61 V to 4.06 V (8 stages)<br>• Falling: 2.55 V to 3.98 V (8 stages) |

**Remark** The electrical characteristics of products rated “G: Industrial applications ($T_A$ = -40 to + 105°C)” at ambient operating temperatures above 85°C differ from those of products rated “A: Consumer applications” and “D: Industrial applications”. For details, refer to **3.1** to **3.10**.

## 3.1 Absolute Maximum Ratings

**Absolute Maximum Ratings** **(1/2)**

| Parameter | Symbols | Conditions | Ratings | Unit |
|---|---|---|---|---|
| Supply voltage | $V_{DD}$ | | -0.5 to +6.5 | V |
| | $EV_{DD0}$, $EV_{DD1}$ | $EV_{DD0}$ = $EV_{DD1}$ | -0.5 to +6.5 | V |
| | $EV_{SS0}$, $EV_{SS1}$ | $EV_{SS0}$ = $EV_{SS1}$ | -0.5 to +0.3 | V |
| REGC pin input voltage | $V_{IREGC}$ | REGC | -0.3 to +2.8 and -0.3 to $V_{DD}$ +0.3 Note 1 | V |
| Input voltage | $V_{I1}$ | P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P140 to P147 | -0.3 to $EV_{DD0}$ +0.3 and -0.3 to $V_{DD}$ +0.3 Note 2 | V |
| | $V_{I2}$ | P60 to P63 (N-ch open-drain) | -0.3 to +6.5 | V |
| | $V_{I3}$ | P20 to P27, P121 to P124, P137, P150 to P156, EXCLK, EXCLKS, $\overline{\text{RESET}}$ | -0.3 to $V_{DD}$ +0.3 Note 2 | V |
| Output voltage | $V_{O1}$ | P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147 | -0.3 to $EV_{DD0}$ +0.3 and -0.3 to $V_{DD}$ +0.3 Note 2 | V |
| | $V_{O2}$ | P20 to P27, P150 to P156 | -0.3 to $V_{DD}$ +0.3 Note 2 | V |
| Analog input voltage | $V_{AI1}$ | ANI16 to ANI20 | -0.3 to $EV_{DD0}$ +0.3 and -0.3 to $AV_{REF}$(+) +0.3 Notes 2, 3 | V |
| | $V_{AI2}$ | ANI0 to ANI14 | -0.3 to $V_{DD}$ +0.3 and -0.3 to $AV_{REF}$(+) +0.3 Notes 2, 3 | V |

**Note 1.** Connect the REGC pin to $V_{SS}$ via a capacitor (0.47 to 1 μF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

**Note 2.** Must be 6.5 V or lower.

**Note 3.** Do not exceed $AV_{REF}$ (+) + 0.3 V in case of A/D conversion target pin.

**Caution** **Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

**Remark 1.** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**Remark 2.** $AV_{REF}$ (+): + side reference voltage of the A/D converter.

**Remark 3.** $V_{SS}$: Reference voltage

**Absolute Maximum Ratings** **(2/2)**

| Parameter | Symbols | Conditions | | Ratings | Unit |
|---|---|---|---|---|---|
| Output current, high | $I_{OH1}$ | Per pin | P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147 | -40 | mA |
| | | Total of all pins -170 mA | P00 to P04, P40 to P47, P102, P120, P130, P140 to P145 | -70 | mA |
| | | | P05, P06, P10 to P17, P30, P31, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100, P101, P110, P111, P146, P147 | -100 | mA |
| | $I_{OH2}$ | Per pin | P20 to P27, P150 to P156 | -0.5 | mA |
| | | Total of all pins | | -2 | mA |
| Output current, low | $I_{OL1}$ | Per pin | P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147 | 40 | mA |
| | | Total of all pins 170 mA | P00 to P04, P40 to P47, P102, P120, P130, P140 to P145 | 70 | mA |
| | | | P05, P06, P10 to P17, P30, P31, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P100, P101, P110, P111, P146, P147 | 100 | mA |
| | $I_{OL2}$ | Per pin | P20 to P27, P150 to P156 | 1 | mA |
| | | Total of all pins | | 5 | mA |
| Operating ambient temperature | $T_A$ | In normal operation mode | | -40 to +105 | °C |
| | | In flash memory programming mode | | | |
| Storage temperature | $T_{stg}$ | | | -65 to +150 | °C |

**Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

## 3.2 Oscillator Characteristics

### 3.2.1 X1, XT1 characteristics

**($T_A$ = -40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Resonator | Resonator | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| X1 clock oscillation frequency ($f_X$) Note | Ceramic resonator/ crystal resonator | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 1.0 | | 20.0 | MHz |
| | | 2.4 V ≤ $V_{DD}$ < 2.7 V | 1.0 | | 16.0 | |
| XT1 clock oscillation frequency ($f_{XT}$) Note | Crystal resonator | | 32 | 32.768 | 35 | kHz |

**Note** Indicates only permissible oscillator frequency ranges. Refer to **AC Characteristics** for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

**Caution Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.**

**Remark** When using the X1 oscillator and XT1 oscillator, refer to **5.4 System Clock Oscillator** in the RL78/G14 User's Manual.

### 3.2.2 On-chip oscillator characteristics

**($T_A$ = -40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Oscillators | Parameters | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| High-speed on-chip oscillator clock frequency Notes 1, 2 | $f_{IH}$ | | | 1 | | 32 | MHz |
| High-speed on-chip oscillator clock frequency accuracy | | -20 to +85°C | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | -1.0 | | +1.0 | % |
| | | -40 to -20°C | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | -1.5 | | +1.5 | % |
| | | +85 to +105°C | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | -2.0 | | +2.0 | % |
| Low-speed on-chip oscillator clock frequency | $f_{IL}$ | | | | 15 | | kHz |
| Low-speed on-chip oscillator clock frequency accuracy | | | | -15 | | +15 | % |

**Note 1.** High-speed on-chip oscillator frequency is selected with bits 0 to 4 of the option byte (000C2H) and bits 0 to 2 of the HOCODIV register.

**Note 2.** This only indicates the oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

## 3.3 DC Characteristics

### 3.3.1 Pin characteristics

**($T_A$ = -40 to +105°C, 2.4 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)** **(1/5)**

| Items | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Output current, high Note 1 | $I_{OH1}$ | Per pin for P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147 | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V | | | -3.0 Note 2 | mA |
| | | Total of P00 to P04, P40 to P47, P102, P120, P130, P140 to P145 (When duty ≤ 70% Note 3) | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V | | | -30.0 | mA |
| | | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V | | | -10.0 | mA |
| | | | 2.4 V ≤ $EV_{DD0}$ < 2.7 V | | | -5.0 | mA |
| | | Total of P05, P06, P10 to P17, P30, P31, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100, P101, P110, P111, P146, P147 (When duty ≤ 70% Note 3) | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V | | | -30.0 | mA |
| | | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V | | | -19.0 | mA |
| | | | 2.4 V ≤ $EV_{DD0}$ < 2.7 V | | | -10.0 | mA |
| | | Total of all pins (When duty ≤ 70% Note 3) | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V | | | -60.0 | mA |
| | $I_{OH2}$ | Per pin for P20 to P27, P150 to P156 | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | | | -0.1 Note 2 | mA |
| | | Total of all pins (When duty ≤ 70% Note 3) | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | | | -1.5 | mA |

**Note 1.** Value of current at which the device operation is guaranteed even if the current flows from the $EV_{DD0}$, $EV_{DD1}$, $V_{DD}$ pins to an output pin.

**Note 2.** Do not exceed the total current value.

**Note 3.** Specification under conditions where the duty factor ≤ 70%.
The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = ($I_{OH}$ × 0.7)/(n × 0.01)

<Example> Where n = 80% and $I_{OH}$ = -10.0 mA
Total output current of pins = (-10.0 × 0.7)/(80 × 0.01) ≈ -8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor.
A current higher than the absolute maximum rating must not flow into one pin.

**Caution P00, P02 to P04, P10, P11, P13 to P15, P17, P30, P43 to P45, P50 to P55, P71, P74, P80 to P82, and P142 to P144 do not output high level in N-ch open-drain mode.**

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**($T_A$ = -40 to +105°C, 2.4 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)** **(2/5)**

| Items | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Output current, low Note 1 | $I_{OL1}$ | Per pin for P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147 | | | | 8.5 Note 2 | mA |
| | | Per pin for P60 to P63 | | | | 15.0 Note 2 | mA |
| | | Total of P00 to P04, P40 to P47, P102, P120, P130, P140 to P145 (When duty ≤ 70% Note 3) | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V | | | 40.0 | mA |
| | | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V | | | 15.0 | mA |
| | | | 2.4 V ≤ $EV_{DD0}$ < 2.7 V | | | 9.0 | mA |
| | | Total of P05, P06, P10 to P17, P30, P31, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P100, P101, P110, P111, P146, P147 (When duty ≤ 70% Note 3) | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V | | | 40.0 | mA |
| | | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V | | | 35.0 | mA |
| | | | 2.4 V ≤ $EV_{DD0}$ < 2.7 V | | | 20.0 | mA |
| | | Total of all pins (When duty ≤ 70% Note 3) | | | | 80.0 | mA |
| | $I_{OL2}$ | Per pin for P20 to P27, P150 to P156 | | | | 0.4 Note 2 | mA |
| | | Total of all pins (When duty ≤ 70% Note 3) | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | | | 5.0 | mA |

**Note 1.** Value of current at which the device operation is guaranteed even if the current flows from an output pin to the $EV_{SS0}$, $EV_{SS1}$, and $V_{SS}$ pins.

**Note 2.** Do not exceed the total current value.

**Note 3.** Specification under conditions where the duty factor ≤ 70%.
The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = ($I_{OL}$ × 0.7)/(n × 0.01)

<Example> Where n = 80% and $I_{OL}$ = 10.0 mA
Total output current of pins = (10.0 × 0.7)/(80 × 0.01) ≈ 8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor.
A current higher than the absolute maximum rating must not flow into one pin.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**($T_A$ = -40 to +105°C, 2.4 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)** **(3/5)**

| Items | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Input voltage, high | $V_{IH1}$ | P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P140 to P147 | Normal input buffer | 0.8 $EV_{DD0}$ | | $EV_{DD0}$ | V |
| | $V_{IH2}$ | P01, P03, P04, P10, P14 to P17, P30, P43, P44, P50, P53 to P55, P80, P81, P142, P143 | TTL input buffer 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V | 2.2 | | $EV_{DD0}$ | V |
| | | | TTL input buffer 3.3 V ≤ $EV_{DD0}$ < 4.0 V | 2.0 | | $EV_{DD0}$ | V |
| | | | TTL input buffer 2.4 V ≤ $EV_{DD0}$ < 3.3 V | 1.5 | | $EV_{DD0}$ | V |
| | $V_{IH3}$ | P20 to P27, P150 to P156 | | 0.7 $V_{DD}$ | | $V_{DD}$ | V |
| | $V_{IH4}$ | P60 to P63 | | 0.7 $EV_{DD0}$ | | 6.0 | V |
| | $V_{IH5}$ | P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$ | | 0.8 $V_{DD}$ | | $V_{DD}$ | V |
| Input voltage, low | $V_{IL1}$ | P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P140 to P147 | Normal input buffer | 0 | | 0.2 $EV_{DD0}$ | V |
| | $V_{IL2}$ | P01, P03, P04, P10, P14 to P17, P30, P43, P44, P50, P53 to P55, P80, P81, P142, P143 | TTL input buffer 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V | 0 | | 0.8 | V |
| | | | TTL input buffer 3.3 V ≤ $EV_{DD0}$ < 4.0 V | 0 | | 0.5 | V |
| | | | TTL input buffer 2.4 V ≤ $EV_{DD0}$ < 3.3 V | 0 | | 0.32 | V |
| | $V_{IL3}$ | P20 to P27, P150 to P156 | | 0 | | 0.3 $V_{DD}$ | V |
| | $V_{IL4}$ | P60 to P63 | | 0 | | 0.3 $EV_{DD0}$ | V |
| | $V_{IL5}$ | P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$ | | 0 | | 0.2 $V_{DD}$ | V |

**Caution The maximum value of $V_{IH}$ of pins P00, P02 to P04, P10, P11, P13 to P15, P17, P30, P43 to P45, P50 to P55, P71, P74, P80 to P82, and P142 to P144 is $EV_{DD0}$, even in the N-ch open-drain mode.**

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**($T_A$ = -40 to +105°C, 2.4 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)** **(4/5)**

| Items | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Output voltage, high | $V_{OH1}$ | P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147 | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, $I_{OH1}$ = -3.0 mA | $EV_{DD0}$ - 0.7 | | | V |
| | | | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V, $I_{OH1}$ = -2.0 mA | $EV_{DD0}$ - 0.6 | | | V |
| | | | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V, $I_{OH1}$ = -1.5 mA | $EV_{DD0}$ - 0.5 | | | V |
| | $V_{OH2}$ | P20 to P27, P150 to P156 | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $I_{OH2}$ = -100 μA | $V_{DD}$ - 0.5 | | | V |
| Output voltage, low | $V_{OL1}$ | P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147 | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, $I_{OL1}$ = 8.5 mA | | | 0.7 | V |
| | | | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V, $I_{OL1}$ = 3.0 mA | | | 0.6 | V |
| | | | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V, $I_{OL1}$ = 1.5 mA | | | 0.4 | V |
| | | | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V, $I_{OL1}$ = 0.6 mA | | | 0.4 | V |
| | $V_{OL2}$ | P20 to P27, P150 to P156 | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $I_{OL2}$ = 400 μA | | | 0.4 | V |
| | $V_{OL3}$ | P60 to P63 | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, $I_{OL3}$ = 15.0 mA | | | 2.0 | V |
| | | | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, $I_{OL3}$ = 5.0 mA | | | 0.4 | V |
| | | | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V, $I_{OL3}$ = 3.0 mA | | | 0.4 | V |
| | | | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V, $I_{OL3}$ = 2.0 mA | | | 0.4 | V |

**Caution** **P00, P02 to P04, P10, P11, P13 to P15, P17, P30, P43 to P45, P50 to P55, P71, P74, P80 to P82, P142 to P144 do not output high level in N-ch open-drain mode.**

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**($T_A$ = -40 to +105°C, 2.4 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)** **(5/5)**

| Items | Symbol | Conditions | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|
| Input leakage current, high | $I_{LIH1}$ | P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P140 to P147 | $V_I$ = $EV_{DD0}$ | | | | 1 | μA |
| | $I_{LIH2}$ | P20 to P27, P137, P150 to P156, $\overline{\text{RESET}}$ | $V_I$ = $V_{DD}$ | | | | 1 | μA |
| | $I_{LIH3}$ | P121 to P124 (X1, X2, EXCLK, XT1, XT2, EXCLKS) | $V_I$ = $V_{DD}$ | In input port or external clock input | | | 1 | μA |
| | | | | In resonator connection | | | 10 | μA |
| Input leakage current, low | $I_{LIL1}$ | P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P140 to P147 | $V_I$ = $EV_{SS0}$ | | | | -1 | μA |
| | $I_{LIL2}$ | P20 to P27, P137, P150 to P156, $\overline{\text{RESET}}$ | $V_I$ = $V_{SS}$ | | | | -1 | μA |
| | $I_{LIL3}$ | P121 to P124 (X1, X2, EXCLK, XT1, XT2, EXCLKS) | $V_I$ = $V_{SS}$ | In input port or external clock input | | | -1 | μA |
| | | | | In resonator connection | | | -10 | μA |
| On-chip pull-up resistance | $R_U$ | P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P140 to P147 | $V_I$ = $EV_{SS0}$, In input port | | 10 | 20 | 100 | kΩ |

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

## 3.3.2 Supply current characteristics

**(1) Flash ROM: 16 to 64 KB of 30- to 64-pin products**

**($T_A$ = -40 to +105°C, 2.4 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = 0 V) (1/2)**

| Parameter | Symbol | Conditions | | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| Supply current Note 1 | IDD1 | Operating mode | HS (high-speed main) mode Note 5 | $f_{HOCO}$ = 64 MHz, $f_{IH}$ = 32 MHz Note 3 | Basic operation | $V_{DD}$ = 5.0 V | | 2.4 | | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 2.4 | | |
| | | | | $f_{HOCO}$ = 32 MHz, $f_{IH}$ = 32 MHz Note 3 | Basic operation | $V_{DD}$ = 5.0 V | | 2.1 | | |
| | | | | | | $V_{DD}$ = 3.0 V | | 2.1 | | |
| | | | HS (high-speed main) mode Note 5 | $f_{HOCO}$ = 64 MHz, $f_{IH}$ = 32 MHz Note 3 | Normal operation | $V_{DD}$ = 5.0 V | | 5.1 | 9.3 | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 5.1 | 9.3 | |
| | | | | $f_{HOCO}$ = 32 MHz, $f_{IH}$ = 32 MHz Note 3 | Normal operation | $V_{DD}$ = 5.0 V | | 4.8 | 8.7 | |
| | | | | | | $V_{DD}$ = 3.0 V | | 4.8 | 8.7 | |
| | | | | $f_{HOCO}$ = 48 MHz, $f_{IH}$ = 24 MHz Note 3 | Normal operation | $V_{DD}$ = 5.0 V | | 4.0 | 7.3 | |
| | | | | | | $V_{DD}$ = 3.0 V | | 4.0 | 7.3 | |
| | | | | $f_{HOCO}$ = 24 MHz, $f_{IH}$ = 24 MHz Note 3 | Normal operation | $V_{DD}$ = 5.0 V | | 3.8 | 6.7 | |
| | | | | | | $V_{DD}$ = 3.0 V | | 3.8 | 6.7 | |
| | | | | $f_{HOCO}$ = 16 MHz, $f_{IH}$ = 16 MHz Note 3 | Normal operation | $V_{DD}$ = 5.0 V | | 2.8 | 4.9 | |
| | | | | | | $V_{DD}$ = 3.0 V | | 2.8 | 4.9 | |
| | | | HS (high-speed main) mode Note 5 | $f_{MX}$ = 20 MHz Note 2, $V_{DD}$ = 5.0 V | Normal operation | Square wave input | | 3.3 | 5.7 | mA |
| | | | | | | Resonator connection | | 3.4 | 5.8 | |
| | | | | $f_{MX}$ = 20 MHz Note 2, $V_{DD}$ = 3.0 V | Normal operation | Square wave input | | 3.3 | 5.7 | |
| | | | | | | Resonator connection | | 3.4 | 5.8 | |
| | | | | $f_{MX}$ = 10 MHz Note 2, $V_{DD}$ = 5.0 V | Normal operation | Square wave input | | 2.0 | 3.4 | |
| | | | | | | Resonator connection | | 2.1 | 3.5 | |
| | | | | $f_{MX}$ = 10 MHz Note 2, $V_{DD}$ = 3.0 V | Normal operation | Square wave input | | 2.0 | 3.4 | |
| | | | | | | Resonator connection | | 2.1 | 3.5 | |
| | | | Subsystem clock operation | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = -40°C | Normal operation | Square wave input | | 4.7 | 6.1 | μA |
| | | | | | | Resonator connection | | 4.7 | 6.1 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +25°C | Normal operation | Square wave input | | 4.7 | 6.1 | |
| | | | | | | Resonator connection | | 4.7 | 6.1 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +50°C | Normal operation | Square wave input | | 4.8 | 6.7 | |
| | | | | | | Resonator connection | | 4.8 | 6.7 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +70°C | Normal operation | Square wave input | | 4.8 | 7.5 | |
| | | | | | | Resonator connection | | 4.8 | 7.5 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +85°C | Normal operation | Square wave input | | 5.4 | 8.9 | |
| | | | | | | Resonator connection | | 5.4 | 8.9 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +105°C | Normal operation | Square wave input | | 7.2 | 21.0 | |
| | | | | | | Resonator connection | | 7.3 | 21.1 | |

(**Notes** and **Remarks** are listed on the next page.)

**Note 1.** Total current flowing into $V_{DD}$ and $EV_{DD0}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$, $EV_{DD0}$ or $V_{SS}$, $EV_{SS0}$. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

**Note 2.** When high-speed on-chip oscillator and subsystem clock are stopped.

**Note 3.** When high-speed system clock and subsystem clock are stopped.

**Note 4.** When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.

**Note 5.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 32 MHz

2.4 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 16 MHz

**Remark 1.** $f_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

**Remark 2.** $f_{HOCO}$: High-speed on-chip oscillator clock frequency (64 MHz max.)

**Remark 3.** $f_{IH}$: High-speed on-chip oscillator clock frequency (32 MHz max.)

**Remark 4.** $f_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)

**Remark 5.** Except subsystem clock operation, temperature condition of the TYP. value is $T_A$ = 25°C

### (1) Flash ROM: 16 to 64 KB of 30- to 64-pin products

**($T_A$ = -40 to +105°C, 2.4 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = 0 V)** **(2/2)**

| Parameter | Symbol | Conditions | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|
| Supply current Note 1 | $I_{DD2}$ Note 2 | HALT mode | HS (high-speed main) mode Note 7 | $f_{HOCO}$ = 64 MHz, $f_{IH}$ = 32 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.80 | 4.36 | mA |
| | | | | | $V_{DD}$ = 3.0 V | | 0.80 | 4.36 | |
| | | | | $f_{HOCO}$ = 32 MHz, $f_{IH}$ = 32 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.49 | 3.67 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.49 | 3.67 | |
| | | | | $f_{HOCO}$ = 48 MHz, $f_{IH}$ = 24 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.62 | 3.42 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.62 | 3.42 | |
| | | | | $f_{HOCO}$ = 24 MHz, $f_{IH}$ = 24 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.4 | 2.85 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.4 | 2.85 | |
| | | | | $f_{HOCO}$ = 16 MHz, $f_{IH}$ = 16 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.37 | 2.08 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.37 | 2.08 | |
| | | | HS (high-speed main) mode Note 7 | $f_{MX}$ = 20 MHz Note 3, $V_{DD}$ = 5.0 V | Square wave input | | 0.28 | 2.45 | mA |
| | | | | | Resonator connection | | 0.40 | 2.57 | |
| | | | | $f_{MX}$ = 20 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 0.28 | 2.45 | |
| | | | | | Resonator connection | | 0.40 | 2.57 | |
| | | | | $f_{MX}$ = 10 MHz Note 3, $V_{DD}$ = 5.0 V | Square wave input | | 0.19 | 1.28 | |
| | | | | | Resonator connection | | 0.25 | 1.36 | |
| | | | | $f_{MX}$ = 10 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 0.19 | 1.28 | |
| | | | | | Resonator connection | | 0.25 | 1.36 | |
| | | | Subsystem clock operation | $f_{SUB}$ = 32.768 kHz Note 5, $T_A$ = -40°C | Square wave input | | 0.25 | 0.57 | μA |
| | | | | | Resonator connection | | 0.44 | 0.76 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 5, $T_A$ = +25°C | Square wave input | | 0.30 | 0.57 | |
| | | | | | Resonator connection | | 0.49 | 0.76 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 5, $T_A$ = +50°C | Square wave input | | 0.36 | 1.17 | |
| | | | | | Resonator connection | | 0.59 | 1.36 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 5, $T_A$ = +70°C | Square wave input | | 0.49 | 1.97 | |
| | | | | | Resonator connection | | 0.72 | 2.16 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 5, $T_A$ = +85°C | Square wave input | | 0.97 | 3.37 | |
| | | | | | Resonator connection | | 1.16 | 3.56 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 5, $T_A$ = +105°C | Square wave input | | 3.20 | 17.10 | |
| | | | | | Resonator connection | | 3.40 | 17.50 | |
| | $I_{DD3}$ Note 6 | STOP mode Note 8 | $T_A$ = -40°C | | | | 0.18 | 0.51 | μA |
| | | | $T_A$ = +25°C | | | | 0.24 | 0.51 | |
| | | | $T_A$ = +50°C | | | | 0.29 | 1.10 | |
| | | | $T_A$ = +70°C | | | | 0.41 | 1.90 | |
| | | | $T_A$ = +85°C | | | | 0.90 | 3.30 | |
| | | | $T_A$ = +105°C | | | | 3.10 | 17.00 | |

(**Notes** and **Remarks** are listed on the next page.)

**Note 1.** Total current flowing into $V_{DD}$ and $EV_{DD0}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$, $EV_{DD0}$ or $V_{SS}$, $EV_{SS0}$. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

**Note 2.** During HALT instruction execution by flash memory.

**Note 3.** When high-speed on-chip oscillator and subsystem clock are stopped.

**Note 4.** When high-speed system clock and subsystem clock are stopped.

**Note 5.** When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.

**Note 6.** Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.

**Note 7.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 32 MHz

2.4 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 16 MHz

**Note 8.** Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.

**Remark 1.** $f_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

**Remark 2.** $f_{HOCO}$: High-speed on-chip oscillator clock frequency (64 MHz max.)

**Remark 3.** $f_{IH}$: High-speed on-chip oscillator clock frequency (32 MHz max.)

**Remark 4.** $f_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)

**Remark 5.** Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is $T_A$ = 25°C

### (2) Flash ROM: 96 to 256 KB of 30- to 100-pin products

**($T_A$ = -40 to +105°C, 2.4 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)** **(1/2)**

| Parameter | Symbol | Conditions | | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| Supply current Note 1 | $I_{DD1}$ | Operating mode | HS (high-speed main) mode Note 5 | $f_{HOCO}$ = 64 MHz, $f_{IH}$ = 32 MHz Note 3 | Basic operation | $V_{DD}$ = 5.0 V | | 2.6 | | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 2.6 | | |
| | | | | $f_{HOCO}$ = 32 MHz, $f_{IH}$ = 32 MHz Note 3 | Basic operation | $V_{DD}$ = 5.0 V | | 2.3 | | |
| | | | | | | $V_{DD}$ = 3.0 V | | 2.3 | | |
| | | | HS (high-speed main) mode Note 5 | $f_{HOCO}$ = 64 MHz, $f_{IH}$ = 32 MHz Note 3 | Normal operation | $V_{DD}$ = 5.0 V | | 5.4 | 10.9 | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 5.4 | 10.9 | |
| | | | | $f_{HOCO}$ = 32 MHz, $f_{IH}$ = 32 MHz Note 3 | Normal operation | $V_{DD}$ = 5.0 V | | 5.0 | 10.3 | |
| | | | | | | $V_{DD}$ = 3.0 V | | 5.0 | 10.3 | |
| | | | | $f_{HOCO}$ = 48 MHz, $f_{IH}$ = 24 MHz Note 3 | Normal operation | $V_{DD}$ = 5.0 V | | 4.2 | 8.2 | |
| | | | | | | $V_{DD}$ = 3.0 V | | 4.2 | 8.2 | |
| | | | | $f_{HOCO}$ = 24 MHz, $f_{IH}$ = 24 MHz Note 3 | Normal operation | $V_{DD}$ = 5.0 V | | 4.0 | 7.8 | |
| | | | | | | $V_{DD}$ = 3.0 V | | 4.0 | 7.8 | |
| | | | | $f_{HOCO}$ = 16 MHz, $f_{IH}$ = 16 MHz Note 3 | Normal operation | $V_{DD}$ = 5.0 V | | 3.0 | 5.6 | |
| | | | | | | $V_{DD}$ = 3.0 V | | 3.0 | 5.6 | |
| | | | HS (high-speed main) mode Note 5 | $f_{MX}$ = 20 MHz Note 2, $V_{DD}$ = 5.0 V | Normal operation | Square wave input | | 3.4 | 6.6 | mA |
| | | | | | | Resonator connection | | 3.6 | 6.7 | |
| | | | | $f_{MX}$ = 20 MHz Note 2, $V_{DD}$ = 3.0 V | Normal operation | Square wave input | | 3.4 | 6.6 | |
| | | | | | | Resonator connection | | 3.6 | 6.7 | |
| | | | | $f_{MX}$ = 10 MHz Note 2, $V_{DD}$ = 5.0 V | Normal operation | Square wave input | | 2.1 | 3.9 | |
| | | | | | | Resonator connection | | 2.2 | 4.0 | |
| | | | | $f_{MX}$ = 10 MHz Note 2, $V_{DD}$ = 3.0 V | Normal operation | Square wave input | | 2.1 | 3.9 | |
| | | | | | | Resonator connection | | 2.2 | 4.0 | |
| | | | Subsystem clock operation | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = -40°C | Normal operation | Square wave input | | 4.9 | 7.1 | µA |
| | | | | | | Resonator connection | | 4.9 | 7.1 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +25°C | Normal operation | Square wave input | | 4.9 | 7.1 | |
| | | | | | | Resonator connection | | 4.9 | 7.1 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +50°C | Normal operation | Square wave input | | 5.1 | 8.8 | |
| | | | | | | Resonator connection | | 5.1 | 8.8 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +70°C | Normal operation | Square wave input | | 5.5 | 10.5 | |
| | | | | | | Resonator connection | | 5.5 | 10.5 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +85°C | Normal operation | Square wave input | | 6.5 | 14.5 | |
| | | | | | | Resonator connection | | 6.5 | 14.5 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +105°C | Normal operation | Square wave input | | 13.0 | 58.0 | |
| | | | | | | Resonator connection | | 13.0 | 58.0 | |

(**Notes** and **Remarks** are listed on the next page.)

**Note 1.** Total current flowing into $V_{DD}$, $EV_{DD0}$, and $EV_{DD1}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$, $EV_{DD0}$, and $EV_{DD1}$, or $V_{SS}$, $EV_{SS0}$, and $EV_{SS1}$. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, D/A converter, comparator, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

**Note 2.** When high-speed on-chip oscillator and subsystem clock are stopped.

**Note 3.** When high-speed system clock and subsystem clock are stopped.

**Note 4.** When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the 12-bit interval timer and watchdog timer.

**Note 5.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 32 MHz

2.4 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 16 MHz

**Remark 1.** $f_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

**Remark 2.** $f_{HOCO}$: High-speed on-chip oscillator clock frequency (64 MHz max.)

**Remark 3.** $f_{IH}$: High-speed on-chip oscillator clock frequency (32 MHz max.)

**Remark 4.** $f_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)

**Remark 5.** Except subsystem clock operation, temperature condition of the TYP. value is $T_A$ = 25°C

### (2) Flash ROM: 96 to 256 KB of 30- to 100-pin products

**($T_A$ = -40 to +105°C, 2.4 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)** **(2/2)**

| Parameter | Symbol | Conditions | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|
| Supply current Note 1 | $I_{DD2}$ Note 2 | HALT mode | HS (high-speed main) mode Note 7 | $f_{HOCO}$ = 64 MHz, $f_{IH}$ = 32 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.79 | 4.86 | mA |
| | | | | | $V_{DD}$ = 3.0 V | | 0.79 | 4.86 | |
| | | | | $f_{HOCO}$ = 32 MHz, $f_{IH}$ = 32 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.49 | 4.17 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.49 | 4.17 | |
| | | | | $f_{HOCO}$ = 48 MHz, $f_{IH}$ = 24 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.62 | 3.82 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.62 | 3.82 | |
| | | | | $f_{HOCO}$ = 24 MHz, $f_{IH}$ = 24 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.4 | 3.25 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.4 | 3.25 | |
| | | | | $f_{HOCO}$ = 16 MHz, $f_{IH}$ = 16 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.38 | 2.28 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.38 | 2.28 | |
| | | | HS (high-speed main) mode Note 7 | $f_{MX}$ = 20 MHz Note 3, $V_{DD}$ = 5.0 V | Square wave input | | 0.30 | 2.65 | mA |
| | | | | | Resonator connection | | 0.40 | 2.77 | |
| | | | | $f_{MX}$ = 20 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 0.30 | 2.65 | |
| | | | | | Resonator connection | | 0.40 | 2.77 | |
| | | | | $f_{MX}$ = 10 MHz Note 3, $V_{DD}$ = 5.0 V | Square wave input | | 0.20 | 1.36 | |
| | | | | | Resonator connection | | 0.25 | 1.46 | |
| | | | | $f_{MX}$ = 10 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 0.20 | 1.36 | |
| | | | | | Resonator connection | | 0.25 | 1.46 | |
| | | | Subsystem clock operation | $f_{SUB}$ = 32.768 kHz Note 5, $T_A$ = -40°C | Square wave input | | 0.28 | 0.66 | µA |
| | | | | | Resonator connection | | 0.47 | 0.85 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 5, $T_A$ = +25°C | Square wave input | | 0.34 | 0.66 | |
| | | | | | Resonator connection | | 0.53 | 0.85 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 5, $T_A$ = +50°C | Square wave input | | 0.37 | 2.35 | |
| | | | | | Resonator connection | | 0.56 | 2.54 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 5, $T_A$ = +70°C | Square wave input | | 0.61 | 4.08 | |
| | | | | | Resonator connection | | 0.80 | 4.27 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 5, $T_A$ = +85°C | Square wave input | | 1.55 | 8.09 | |
| | | | | | Resonator connection | | 1.74 | 8.28 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 5, $T_A$ = +105°C | Square wave input | | 6.00 | 51.00 | |
| | | | | | Resonator connection | | 6.00 | 51.00 | |
| | $I_{DD3}$ Note 6 | STOP mode Note 8 | $T_A$ = -40°C | | | | 0.19 | 0.57 | µA |
| | | | $T_A$ = +25°C | | | | 0.25 | 0.57 | |
| | | | $T_A$ = +50°C | | | | 0.33 | 2.26 | |
| | | | $T_A$ = +70°C | | | | 0.52 | 3.99 | |
| | | | $T_A$ = +85°C | | | | 1.46 | 8.00 | |
| | | | $T_A$ = +105°C | | | | 5.50 | 50.00 | |

(**Notes** and **Remarks** are listed on the next page.)

**Note 1.** Total current flowing into $V_{DD}$, $EV_{DD0}$, and $EV_{DD1}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$, $EV_{DD0}$, and $EV_{DD1}$, or $V_{SS}$, $EV_{SS0}$, and $EV_{SS1}$. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, D/A converter, comparator, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

**Note 2.** During HALT instruction execution by flash memory.

**Note 3.** When high-speed on-chip oscillator and subsystem clock are stopped.

**Note 4.** When high-speed system clock and subsystem clock are stopped.

**Note 5.** When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.

**Note 6.** Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.

**Note 7.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: $2.7\ V \leq V_{DD} \leq 5.5\ V$@1 MHz to 32 MHz

$2.4\ V \leq V_{DD} \leq 5.5\ V$@1 MHz to 16 MHz

**Note 8.** Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.

**Remark 1.** $f_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

**Remark 2.** $f_{HOCO}$: High-speed on-chip oscillator clock frequency (64 MHz max.)

**Remark 3.** $f_{IH}$: High-speed on-chip oscillator clock frequency (32 MHz max.)

**Remark 4.** $f_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)

**Remark 5.** Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is $T_A$ = 25°C

### (3) Flash ROM: 384 to 512 KB of 48- to 100-pin products

**($T_A$ = -40 to +105°C, 2.4 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)** **(1/2)**

| Parameter | Symbol | Conditions | | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| Supply current Note 1 | $I_{DD1}$ | Operating mode | HS (high-speed main) mode Note 5 | $f_{HOCO}$ = 64 MHz, $f_{IH}$ = 32 MHz Note 3 | Basic operation | $V_{DD}$ = 5.0 V | | 2.9 | | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 2.9 | | |
| | | | | $f_{HOCO}$ = 32 MHz, $f_{IH}$ = 32 MHz Note 3 | Basic operation | $V_{DD}$ = 5.0 V | | 2.5 | | |
| | | | | | | $V_{DD}$ = 3.0 V | | 2.5 | | |
| | | | HS (high-speed main) mode Note 5 | $f_{HOCO}$ = 64 MHz, $f_{IH}$ = 32 MHz Note 3 | Normal operation | $V_{DD}$ = 5.0 V | | 6.0 | 11.2 | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 6.0 | 11.2 | |
| | | | | $f_{HOCO}$ = 32 MHz, $f_{IH}$ = 32 MHz Note 3 | Normal operation | $V_{DD}$ = 5.0 V | | 5.5 | 10.6 | |
| | | | | | | $V_{DD}$ = 3.0 V | | 5.5 | 10.6 | |
| | | | | $f_{HOCO}$ = 48 MHz, $f_{IH}$ = 24 MHz Note 3 | Normal operation | $V_{DD}$ = 5.0 V | | 4.7 | 8.6 | |
| | | | | | | $V_{DD}$ = 3.0 V | | 4.7 | 8.6 | |
| | | | | $f_{HOCO}$ = 24 MHz, $f_{IH}$ = 24 MHz Note 3 | Normal operation | $V_{DD}$ = 5.0 V | | 4.4 | 8.2 | |
| | | | | | | $V_{DD}$ = 3.0 V | | 4.4 | 8.2 | |
| | | | | $f_{HOCO}$ = 16 MHz, $f_{IH}$ = 16 MHz Note 3 | Normal operation | $V_{DD}$ = 5.0 V | | 3.3 | 5.9 | |
| | | | | | | $V_{DD}$ = 3.0 V | | 3.3 | 5.9 | |
| | | | HS (high-speed main) mode Note 5 | $f_{MX}$ = 20 MHz Note 2, $V_{DD}$ = 5.0 V | Normal operation | Square wave input | | 3.7 | 6.8 | mA |
| | | | | | | Resonator connection | | 3.9 | 7.0 | |
| | | | | $f_{MX}$ = 20 MHz Note 2, $V_{DD}$ = 3.0 V | Normal operation | Square wave input | | 3.7 | 6.8 | |
| | | | | | | Resonator connection | | 3.9 | 7.0 | |
| | | | | $f_{MX}$ = 10 MHz Note 2, $V_{DD}$ = 5.0 V | Normal operation | Square wave input | | 2.3 | 4.1 | |
| | | | | | | Resonator connection | | 2.3 | 4.2 | |
| | | | | $f_{MX}$ = 10 MHz Note 2, $V_{DD}$ = 3.0 V | Normal operation | Square wave input | | 2.3 | 4.1 | |
| | | | | | | Resonator connection | | 2.3 | 4.2 | |
| | | | Subsystem clock operation | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = -40°C | Normal operation | Square wave input | | 5.2 | 7.7 | μA |
| | | | | | | Resonator connection | | 5.2 | 7.7 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +25°C | Normal operation | Square wave input | | 5.3 | 7.7 | |
| | | | | | | Resonator connection | | 5.3 | 7.7 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +50°C | Normal operation | Square wave input | | 5.5 | 10.6 | |
| | | | | | | Resonator connection | | 5.5 | 10.6 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +70°C | Normal operation | Square wave input | | 5.9 | 13.2 | |
| | | | | | | Resonator connection | | 6.0 | 13.2 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +85°C | Normal operation | Square wave input | | 6.8 | 17.5 | |
| | | | | | | Resonator connection | | 6.9 | 17.5 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 4 $T_A$ = +105°C | Normal operation | Square wave input | | 15.5 | 77.8 | |
| | | | | | | Resonator connection | | 15.5 | 77.8 | |

(**Notes** and **Remarks** are listed on the next page.)

**Note 1.** Total current flowing into $V_{DD}$, $EV_{DD0}$, and $EV_{DD1}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$, $EV_{DD0}$, and $EV_{DD1}$, or $V_{SS}$, $EV_{SS0}$, and $EV_{SS1}$. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, D/A converter, comparator, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

**Note 2.** When high-speed on-chip oscillator and subsystem clock are stopped.

**Note 3.** When high-speed system clock and subsystem clock are stopped.

**Note 4.** When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the 12-bit interval timer and watchdog timer.

**Note 5.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 32 MHz

2.4 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 16 MHz

**Remark 1.** $f_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

**Remark 2.** $f_{HOCO}$: High-speed on-chip oscillator clock frequency (64 MHz max.)

**Remark 3.** $f_{IH}$: High-speed on-chip oscillator clock frequency (32 MHz max.)

**Remark 4.** $f_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)

**Remark 5.** Except subsystem clock operation, temperature condition of the TYP. value is $T_A$ = 25°C

### (3) Flash ROM: 384 to 512 KB of 48- to 100-pin products

**($T_A$ = -40 to +105°C, 2.4 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)** **(2/2)**

| Parameter | Symbol | Conditions | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|
| Supply current Note 1 | $I_{DD2}$ Note 2 | HALT mode | HS (high-speed main) mode Note 7 | $f_{HOCO}$ = 64 MHz, $f_{IH}$ = 32 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.93 | 5.16 | mA |
| | | | | | $V_{DD}$ = 3.0 V | | 0.93 | 5.16 | |
| | | | | $f_{HOCO}$ = 32 MHz, $f_{IH}$ = 32 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.5 | 4.47 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.5 | 4.47 | |
| | | | | $f_{HOCO}$ = 48 MHz, $f_{IH}$ = 24 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.72 | 4.08 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.72 | 4.08 | |
| | | | | $f_{HOCO}$ = 24 MHz, $f_{IH}$ = 24 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.42 | 3.51 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.42 | 3.51 | |
| | | | | $f_{HOCO}$ = 16 MHz, $f_{IH}$ = 16 MHz Note 4 | $V_{DD}$ = 5.0 V | | 0.39 | 2.38 | |
| | | | | | $V_{DD}$ = 3.0 V | | 0.39 | 2.38 | |
| | | | HS (high-speed main) mode Note 7 | $f_{MX}$ = 20 MHz Note 3, $V_{DD}$ = 5.0 V | Square wave input | | 0.31 | 2.83 | mA |
| | | | | | Resonator connection | | 0.41 | 2.92 | |
| | | | | $f_{MX}$ = 20 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 0.31 | 2.83 | |
| | | | | | Resonator connection | | 0.41 | 2.92 | |
| | | | | $f_{MX}$ = 10 MHz Note 3, $V_{DD}$ = 5.0 V | Square wave input | | 0.21 | 1.46 | |
| | | | | | Resonator connection | | 0.26 | 1.57 | |
| | | | | $f_{MX}$ = 10 MHz Note 3, $V_{DD}$ = 3.0 V | Square wave input | | 0.21 | 1.46 | |
| | | | | | Resonator connection | | 0.26 | 1.57 | |
| | | | Subsystem clock operation | $f_{SUB}$ = 32.768 kHz Note 5, $T_A$ = -40°C | Square wave input | | 0.31 | 0.76 | μA |
| | | | | | Resonator connection | | 0.50 | 0.95 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 5, $T_A$ = +25°C | Square wave input | | 0.38 | 0.76 | |
| | | | | | Resonator connection | | 0.57 | 0.95 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 5, $T_A$ = +50°C | Square wave input | | 0.47 | 3.59 | |
| | | | | | Resonator connection | | 0.70 | 3.78 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 5, $T_A$ = +70°C | Square wave input | | 0.80 | 6.20 | |
| | | | | | Resonator connection | | 1.00 | 6.39 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 5, $T_A$ = +85°C | Square wave input | | 1.65 | 10.56 | |
| | | | | | Resonator connection | | 1.84 | 10.75 | |
| | | | | $f_{SUB}$ = 32.768 kHz Note 5, $T_A$ = +105°C | Square wave input | | 8.00 | 65.7 | |
| | | | | | Resonator connection | | 8.00 | 65.7 | |
| | $I_{DD3}$ Note 6 | STOP mode Note 8 | $T_A$ = -40°C | | | | 0.19 | 0.63 | μA |
| | | | $T_A$ = +25°C | | | | 0.30 | 0.63 | |
| | | | $T_A$ = +50°C | | | | 0.41 | 3.47 | |
| | | | $T_A$ = +70°C | | | | 0.80 | 6.08 | |
| | | | $T_A$ = +85°C | | | | 1.53 | 10.44 | |
| | | | $T_A$ = +105°C | | | | 6.50 | 67.14 | |

(**Notes** and **Remarks** are listed on the next page.)

**Note 1.** Total current flowing into $V_{DD}$, $EV_{DD0}$, and $EV_{DD1}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$, $EV_{DD0}$, and $EV_{DD1}$, or $V_{SS}$, $EV_{SS0}$, and $EV_{SS1}$. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, D/A converter, comparator, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

**Note 2.** During HALT instruction execution by flash memory.

**Note 3.** When high-speed on-chip oscillator and subsystem clock are stopped.

**Note 4.** When high-speed system clock and subsystem clock are stopped.

**Note 5.** When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.

**Note 6.** Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.

**Note 7.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: $2.7\ V \leq V_{DD} \leq 5.5\ V$@1 MHz to 32 MHz

$2.4\ V \leq V_{DD} \leq 5.5\ V$@1 MHz to 16 MHz

**Note 8.** Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.

**Remark 1.** $f_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

**Remark 2.** $f_{HOCO}$: High-speed on-chip oscillator clock frequency (64 MHz max.)

**Remark 3.** $f_{IH}$: High-speed on-chip oscillator clock frequency (32 MHz max.)

**Remark 4.** $f_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)

**Remark 5.** Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is $T_A$ = 25°C

### (4) Peripheral Functions (Common to all products)

**($T_A$ = -40 to +105°C, 2.4 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Low-speed on-chip oscillator operating current | $I_{FIL}$ Note 1 | | | | 0.20 | | μA |
| RTC operating current | $I_{RTC}$ Notes 1, 2, 3 | | | | 0.02 | | μA |
| 12-bit interval timer operating current | $I_{IT}$ Notes 1, 2, 4 | | | | 0.02 | | μA |
| Watchdog timer operating current | $I_{WDT}$ Notes 1, 2, 5 | $f_{IL}$ = 15 kHz | | | 0.22 | | μA |
| A/D converter operating current | $I_{ADC}$ Notes 1, 6 | When conversion at maximum speed | Normal mode, $AV_{REFP}$ = $V_{DD}$ = 5.0 V | | 1.3 | 1.7 | mA |
| | | | Low voltage mode, $AV_{REFP}$ = $V_{DD}$ = 3.0 V | | 0.5 | 0.7 | mA |
| A/D converter reference voltage current | $I_{ADREF}$ Note 1 | | | | 75.0 | | μA |
| Temperature sensor operating current | $I_{TMPS}$ Note 1 | | | | 75.0 | | μA |
| D/A converter operating current | $I_{DAC}$ Notes 1, 11, 13 | Per D/A converter channel | | | | 1.5 | mA |
| Comparator operating current | $I_{CMP}$ Notes 1, 12, 13 | $V_{DD}$ = 5.0 V, Regulator output voltage = 2.1 V | Window mode | | 12.5 | | μA |
| | | | Comparator high-speed mode | | 6.5 | | μA |
| | | | Comparator low-speed mode | | 1.7 | | μA |
| | | $V_{DD}$ = 5.0 V, Regulator output voltage = 1.8 V | Window mode | | 8.0 | | μA |
| | | | Comparator high-speed mode | | 4.0 | | μA |
| | | | Comparator low-speed mode | | 1.3 | | μA |
| LVD operating current | $I_{LVD}$ Notes 1, 7 | | | | 0.08 | | μA |
| Self-programming operating current | $I_{FSP}$ Notes 1, 9 | | | | 2.50 | 12.20 | mA |
| BGO operating current | $I_{BGO}$ Notes 1, 8 | | | | 2.50 | 12.20 | mA |
| SNOOZE operating current | $I_{SNOZ}$ Note 1 | ADC operation | The mode is performed Note 10 | | 0.50 | 1.10 | mA |
| | | | The A/D conversion operations are performed, Low voltage mode, $AV_{REFP}$ = $V_{DD}$ = 3.0 V | | 1.20 | 2.04 | |
| | | CSI/UART operation | | | 0.70 | 1.54 | |
| | | DTC operation | | | 3.10 | | |

**Note 1.** Current flowing to $V_{DD}$.

**Note 2.** When high speed on-chip oscillator and high-speed system clock are stopped.

**Note 3.** Current flowing only to the real-time clock (RTC) (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either $I_{DD1}$ or $I_{DD2}$, and $I_{RTC}$, when the real-time clock operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, $I_{FIL}$ should be added. $I_{DD2}$ subsystem clock operation includes the operational current of the real-time clock.

**Note 4.** Current flowing only to the 12-bit interval timer (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either $I_{DD1}$ or $I_{DD2}$, and $I_{IT}$, when the 12-bit interval timer operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, $I_{FIL}$ should be added.

**Note 5.** Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The supply current of the RL78 microcontrollers is the sum of $I_{DD1}$, $I_{DD2}$ or $I_{DD3}$ and $I_{WDT}$ when the watchdog timer is in operation.

**Note 6.** Current flowing only to the A/D converter. The supply current of the RL78 microcontrollers is the sum of $I_{DD1}$ or $I_{DD2}$ and $I_{ADC}$ when the A/D converter operates in an operation mode or the HALT mode.

**Note 7.** Current flowing only to the LVD circuit. The supply current of the RL78 microcontrollers is the sum of $I_{DD1}$, $I_{DD2}$ or $I_{DD3}$ and $I_{LVD}$ when the LVD circuit is in operation.

**Note 8.** Current flowing during programming of the data flash.

**Note 9.** Current flowing during self-programming.

**Note 10.** For shift time to the SNOOZE mode, see **23.3.3 SNOOZE mode** in the RL78/G14 User's Manual.

**Note 11.** Current flowing only to the D/A converter. The supply current of the RL78 microcontrollers is the sum of $I_{DD1}$ or $I_{DD2}$ and $I_{DAC}$ when the D/A converter operates in an operation mode or the HALT mode.

**Note 12.** Current flowing only to the comparator circuit. The supply current of the RL78 microcontrollers is the sum of $I_{DD1}$, $I_{DD2}$, or $I_{DD3}$ and $I_{CMP}$ when the comparator circuit is in operation.

**Note 13.** A comparator and D/A converter are provided in products with 96 KB or more code flash memory.

**Remark 1.** $f_{IL}$: Low-speed on-chip oscillator clock frequency

**Remark 2.** $f_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)

**Remark 3.** $f_{CLK}$: CPU/peripheral hardware clock frequency

**Remark 4.** Temperature condition of the TYP. value is $T_A$ = 25°C

## 3.4 AC Characteristics

**($T_A$ = -40 to +105°C, 2.4 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)** **(1/2)**

| Items | Symbol | Conditions | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|
| Instruction cycle (minimum instruction execution time) | $T_{CY}$ | Main system clock ($f_{MAIN}$) operation | HS (high-speed main) mode | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 0.03125 | | 1 | µs |
| | | | | 2.4 V ≤ $V_{DD}$ < 2.7 V | 0.0625 | | 1 | µs |
| | | Subsystem clock ($f_{SUB}$) operation | | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | 28.5 | 30.5 | 31.3 | µs |
| | | In the self-programming mode | HS (high-speed main) mode | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 0.03125 | | 1 | µs |
| | | | | 2.4 V ≤ $V_{DD}$ < 2.7 V | 0.0625 | | 1 | µs |
| External system clock frequency | $f_{EX}$ | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | | | 1.0 | | 20.0 | MHz |
| | | 2.4 V ≤ $V_{DD}$ ≤ 2.7 V | | | 1.0 | | 16.0 | MHz |
| | $f_{EXS}$ | | | | 32 | | 35 | kHz |
| External system clock input high-level width, low-level width | $t_{EXH}$, $t_{EXL}$ | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | | | 24 | | | ns |
| | | 2.4 V ≤ $V_{DD}$ ≤ 2.7 V | | | 30 | | | ns |
| | $t_{EXHS}$, $t_{EXLS}$ | | | | 13.7 | | | µs |
| TI00 to TI03, TI10 to TI13 input high-level width, low-level width | $t_{TIH}$, $t_{TIL}$ | | | | 1/$f_{MCK}$ + 10 Note | | | ns |
| Timer RJ input cycle | $f_C$ | TRJIO | | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | 100 | | | ns |
| | | | | 2.4 V ≤ $EV_{DD0}$ < 2.7 V | 300 | | | ns |
| Timer RJ input high-level width, low-level width | $t_{TJIH}$, $t_{TJIL}$ | TRJIO | | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | 40 | | | ns |
| | | | | 2.4 V ≤ $EV_{DD0}$ < 2.7 V | 120 | | | ns |

**Note** The following conditions are required for low voltage interface when $EV_{DD0}$ < $V_{DD}$
2.4 V ≤ $EV_{DD0}$ < 2.7 V: MIN. 125 ns

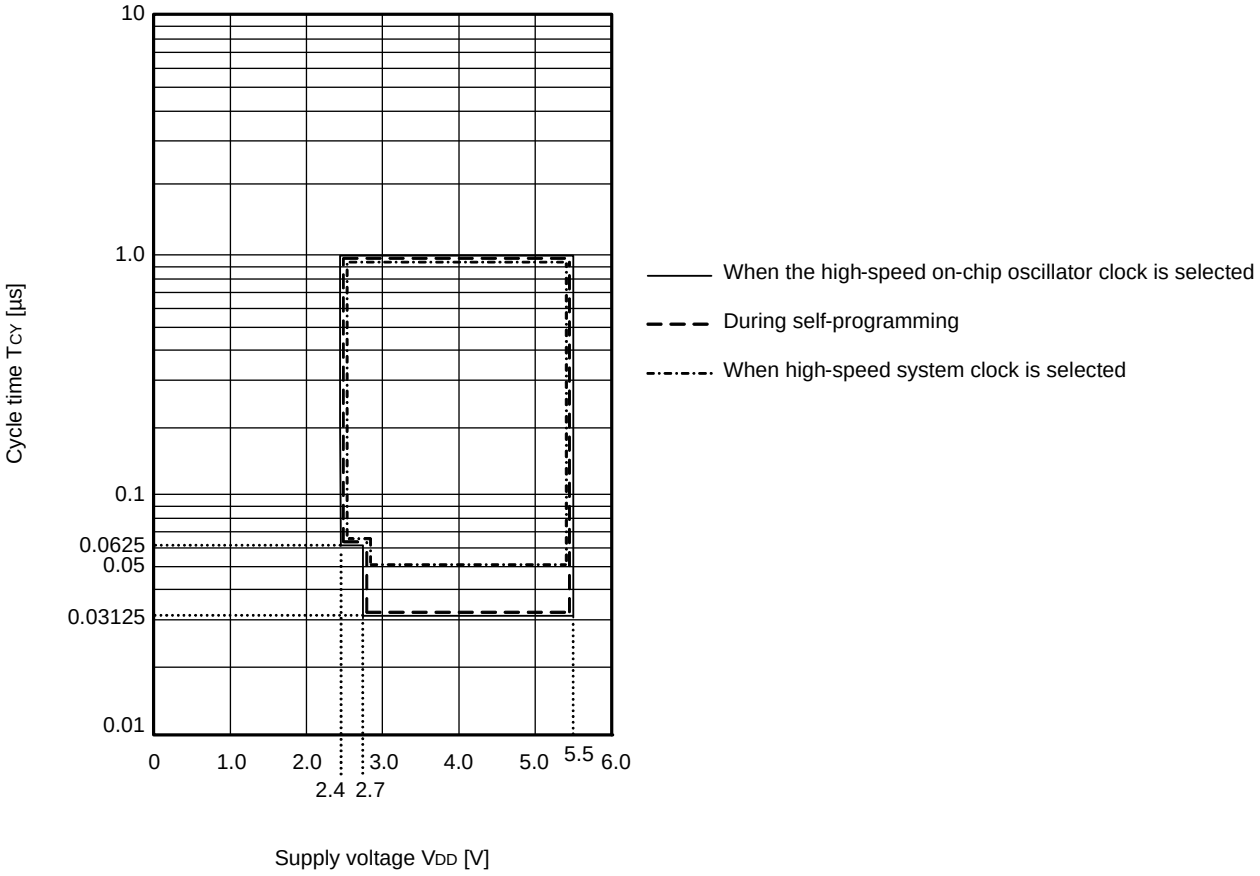
**Remark** $f_{MCK}$: Timer array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of timer mode register mn (TMRmn). m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3))

**($T_A$ = -40 to +105°C, 2.4 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)** **(2/2)**

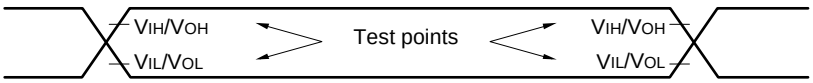
| Items | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Timer RD input high-level width, low-level width | $t_{TDIH}$, $t_{TDIL}$ | TRDIOA0, TRDIOA1, TRDIOB0, TRDIOB1, TRDIOC0, TRDIOC1, TRDIOD0, TRDIOD1 | | 3/$f_{CLK}$ | | | ns |
| Timer RD forced cutoff signal input low-level width | $t_{TDSIL}$ | P130/INTP0 | 2MHz < $f_{CLK}$ ≤ 32 MHz | 1 | | | µs |
| | | | $f_{CLK}$ ≤ 2 MHz | 1/$f_{CLK}$ + 1 | | | |
| Timer RG input high-level width, low-level width | $t_{TGIH}$, $t_{TGIL}$ | TRGIOA, TRGIOB | | 2.5/$f_{CLK}$ | | | ns |
| TO00 to TO03, TO10 to TO13, TRJIO0, TRJO0, TRDIOA0, TRDIOA1, TRDIOB0, TRDIOB1, TRDIOC0, TRDIOC1, TRDIOD0, TRDIOD1, TRGIOA, TRGIOB output frequency | $f_{TO}$ | HS (high-speed main) mode | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V | | | 16 | MHz |
| | | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V | | | 8 | MHz |
| | | | 2.4 V ≤ $EV_{DD0}$ < 2.7 V | | | 4 | MHz |
| PCLBUZ0, PCLBUZ1 output frequency | $f_{PCL}$ | HS (high-speed main) mode | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V | | | 16 | MHz |
| | | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V | | | 8 | MHz |
| | | | 2.4 V ≤ $EV_{DD0}$ < 2.7 V | | | 4 | MHz |
| Interrupt input high-level width, low-level width | $t_{INTH}$, $t_{INTL}$ | INTP0 | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | 1 | | | µs |
| | | INTP1 to INTP11 | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V | 1 | | | µs |
| Key interrupt input low-level width | $t_{KR}$ | KR0 to KR7 | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V | 250 | | | ns |
| $\overline{\text{RESET}}$ low-level width | $t_{RSL}$ | | | 10 | | | µs |

Minimum Instruction Execution Time during Main System Clock Operation

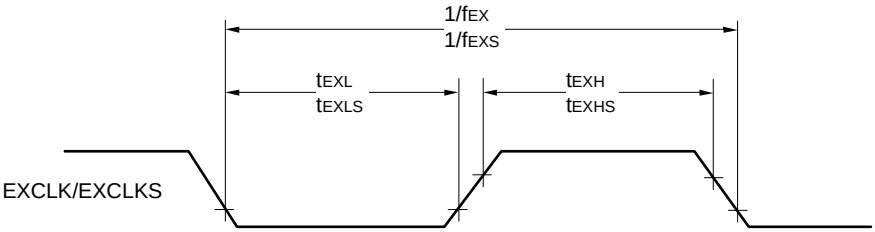
$T_{CY}$ vs $V_{DD}$ (HS (high-speed main) mode)



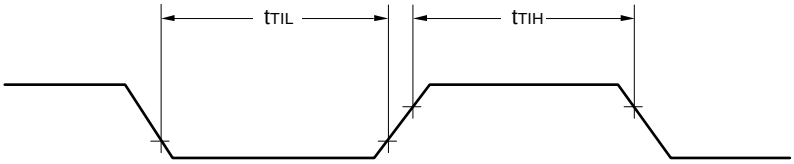
AC Timing Test Points



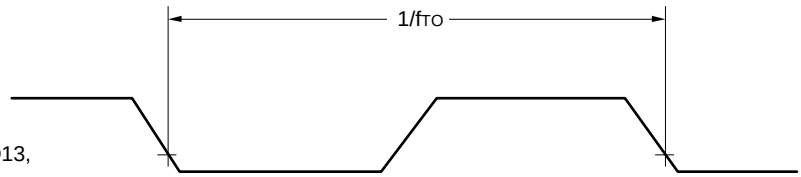

External System Clock Timing



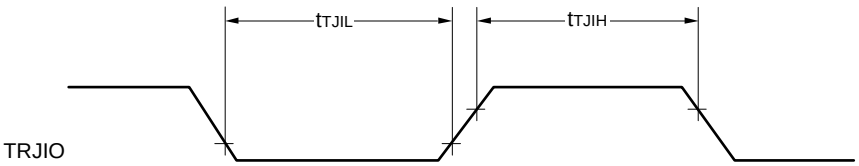

TI/TO Timing

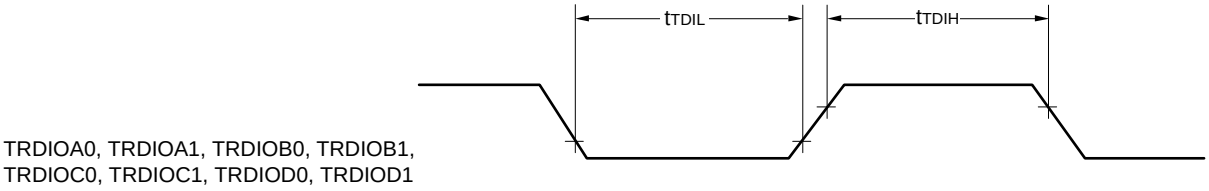


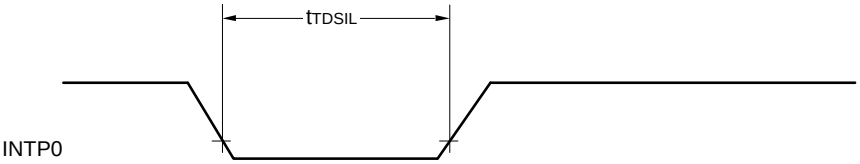

TI00 to TI03, TI10 to TI13

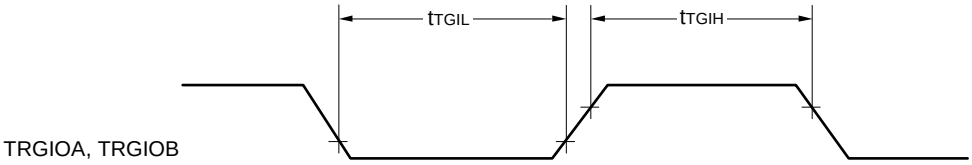



TO00 to TO03, TO10 to TO13,
TRJIO0, TRJO0,
TRDIOA0, TRDIOA1,
TRDIOB0, TRDIOB1,
TRDIOC0, TRDIOC1,
TRDIOD0, TRDIOD1,
TRGIOA, TRGIOB

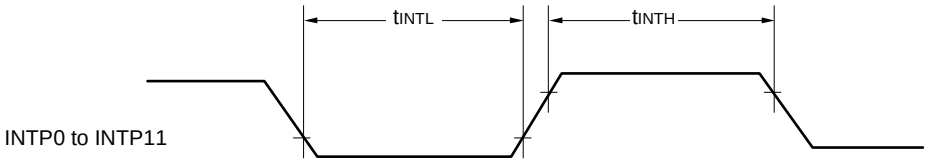

tTJIL
tTJIH
TRJIO


tTDIL
tTDIH
TRDIOA0, TRDIOA1, TRDIOB0, TRDIOB1,
TRDIOC0, TRDIOC1, TRDIOD0, TRDIOD1

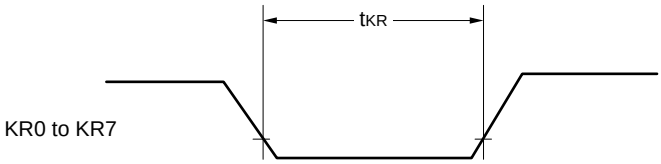

tTDSIL
INTP0


tTGIL
tTGIH
TRGIOA, TRGIOB

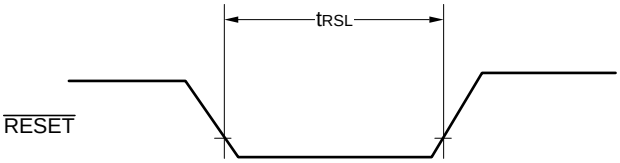
Interrupt Request Input Timing




Key Interrupt Input Timing

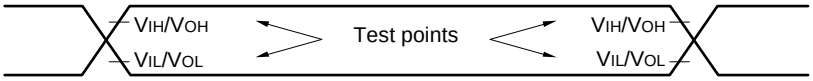



$\overline{\text{RESET}}$ Input Timing



## 3.5 Peripheral Functions Characteristics

AC Timing Test Points




### 3.5.1 Serial array unit

**(1) During communication at same potential (UART mode)**

**(TA = -40 to +105°C, 2.4 V ≤ EVDD0 = EVDD1 ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)**

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | Unit |
|---|---|---|---|---|---|
| | | | MIN. | MAX. | |
| Transfer rate Note 1 | | 2.4 V ≤ EVDD0 ≤ 5.5 V | | fMCK/12 Note 2 | bps |
| | | Theoretical value of the maximum transfer rate fMCK = fCLK Note 3 | | 2.6 | Mbps |

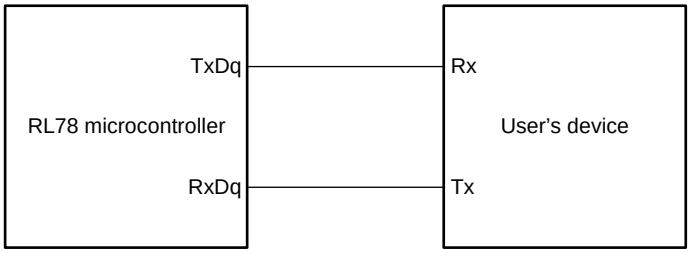
**Note 1.** Transfer rate in the SNOOZE mode is 4800 bps only.
However, the SNOOZE mode cannot be used when FRQSEL4 = 1.

**Note 2.** The following conditions are required for low voltage interface when EVDD0 < VDD.
2.4 V ≤ EVDD0 < 2.7 V: MAX. 1.3 Mbps

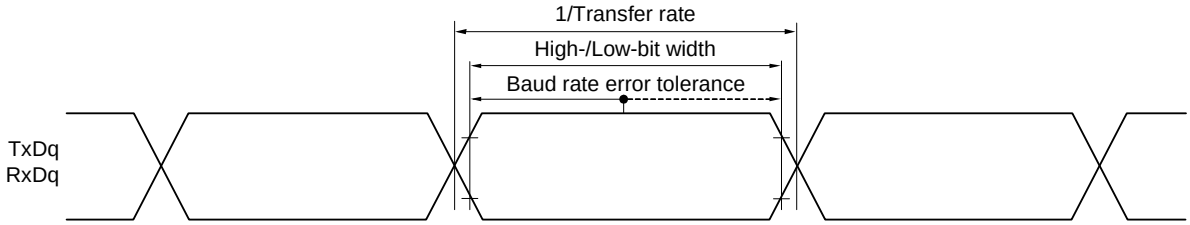
**Note 3.** The maximum operating frequencies of the CPU/peripheral hardware clock (fCLK) are:
HS (high-speed main) mode: 32 MHz (2.7 V ≤ VDD ≤ 5.5 V)
16 MHz (2.4 V ≤ VDD ≤ 5.5 V)

**Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

**UART mode connection diagram (during communication at same potential)**




**UART mode bit width (during communication at same potential) (reference)**




**Remark 1.** q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 5, 14)

**Remark 2.** fMCK: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

### (2) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)

**($T_A$ = -40 to +105°C, 2.4 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) mode | | Unit |
|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | |
| SCKp cycle time | $t_{KCY1}$ | $t_{KCY1}$ ≥ 4/$f_{CLK}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | 250 | | ns |
| | | | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V | 500 | | ns |
| SCKp high-/low-level width | $t_{KH1}$, $t_{KL1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V | | $t_{KCY1}$/2 - 24 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | $t_{KCY1}$/2 - 36 | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V | | $t_{KCY1}$/2 - 76 | | ns |
| SIp setup time (to SCKp↑) Note 1 | $t_{SIK1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 66 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 66 | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 113 | | ns |
| SIp hold time (from SCKp↑) Note 2 | $t_{KSI1}$ | | | 38 | | ns |
| Delay time from SCKp↓ to SOp output Note 3 | $t_{KSO1}$ | C = 30 pF Note 4 | | | 50 | ns |

**Note 1.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 2.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 3.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 4.** C is the load capacitance of the SCKp and SOp output lines.

**Caution Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

**Remark 1.** p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM number (g = 0, 1, 3 to 5, 14)

**Remark 2.** $f_{MCK}$: Serial array unit operation clock frequency (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

### (3) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)

**($T_A$ = -40 to +105°C, 2.4 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)** **(1/2)**

| Parameter | Symbol | Conditions | | HS (high-speed main) mode | | Unit |
|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | |
| SCKp cycle time Note 5 | $t_{KCY2}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V | 20 MHz < $f_{MCK}$ | 16/$f_{MCK}$ | | ns |
| | | | $f_{MCK}$ ≤ 20 MHz | 12/$f_{MCK}$ | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | 16 MHz < $f_{MCK}$ | 16/$f_{MCK}$ | | ns |
| | | | $f_{MCK}$ ≤ 16 MHz | 12/$f_{MCK}$ | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 12/$f_{MCK}$ and 1000 | | ns |
| SCKp high-/low-level width | $t_{KH2}$, $t_{KL2}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V | | $t_{KCY2}$/2 - 14 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | $t_{KCY2}$/2 - 16 | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V | | $t_{KCY2}$/2 - 36 | | ns |
| SIp setup time (to SCKp↑) Note 1 | $t_{SIK2}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 1/$f_{MCK}$ + 40 | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 1/$f_{MCK}$ + 60 | | ns |
| SIp hold time (from SCKp↑) Note 2 | $t_{KSI2}$ | | | 1/$f_{MCK}$ + 62 | | ns |
| Delay time from SCKp↓ to SOp output Note 3 | $t_{KSO2}$ | C = 30 pF Note 4 | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 2/$f_{MCK}$ + 66 | ns |
| | | | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 2/$f_{MCK}$ + 113 | ns |

**Note 1.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 2.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 3.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 4.** C is the load capacitance of the SOp output lines.

**Note 5.** The maximum transfer rate when using the SNOOZE mode is 1 Mbps.

**Caution Select the normal input buffer for the SIp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

**Remark 1.** p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31), m: Unit number (m = 0, 1),
n: Channel number (n = 0 to 3), g: PIM number (g = 0, 1, 3 to 5, 14)

**Remark 2.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,
n: Channel number (mn = 00 to 03, 10 to 13))

### (3) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)

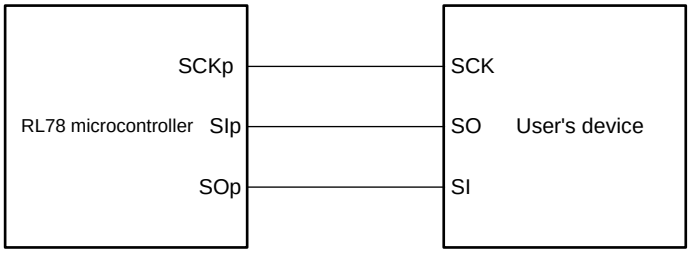
**($T_A$ = -40 to +105°C, 2.4 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)** **(2/2)**

| Parameter | Symbol | Conditions | | HS (high-speed main) mode | | Unit |
|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | |
| $\overline{SSI00}$ setup time | $t_{SSIK}$ | DAPmn = 0 | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | 240 | | ns |
| | | | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V | 400 | | ns |
| | | DAPmn = 1 | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | 1/$f_{MCK}$ + 240 | | ns |
| | | | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V | 1/$f_{MCK}$ + 400 | | ns |
| $\overline{SSI00}$ hold time | $t_{KSSI}$ | DAPmn = 0 | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | 1/$f_{MCK}$ + 240 | | ns |
| | | | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V | 1/$f_{MCK}$ + 400 | | ns |
| | | DAPmn = 1 | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | 240 | | ns |
| | | | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V | 400 | | ns |

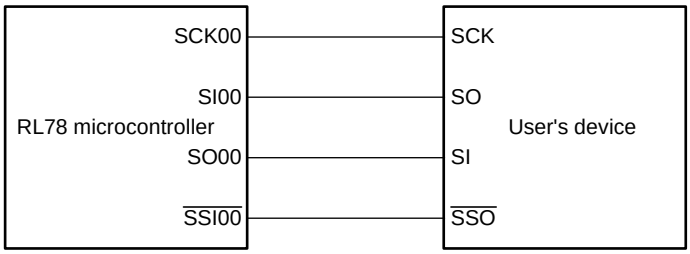
**Caution** **Select the normal input buffer for the SIp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

**Remark** p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM number (g = 3, 5)

**CSI mode connection diagram (during communication at same potential)**

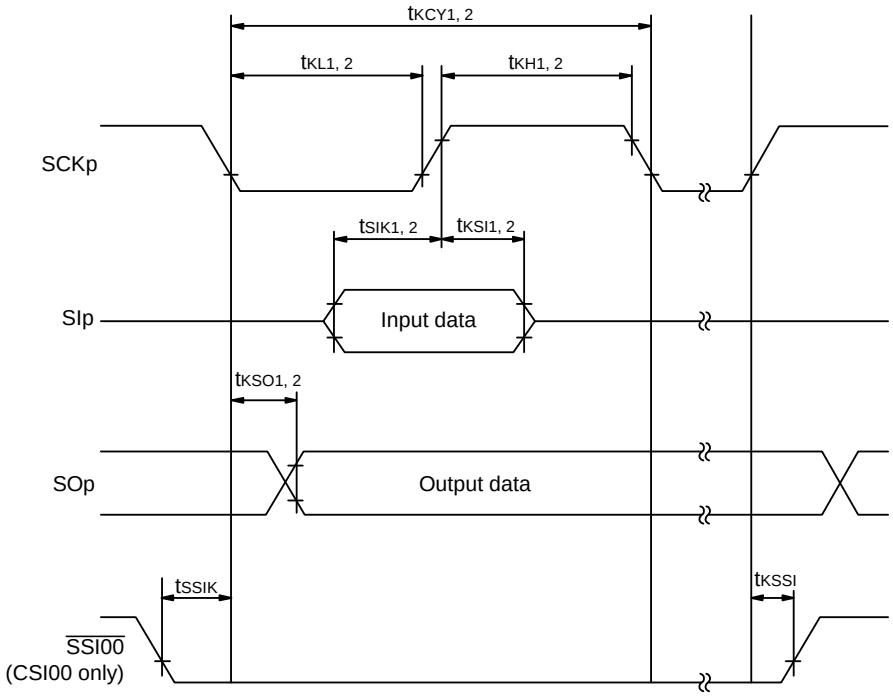



**CSI mode connection diagram (during communication at same potential)**
**(Slave Transmission of slave select input function (CSI00))**

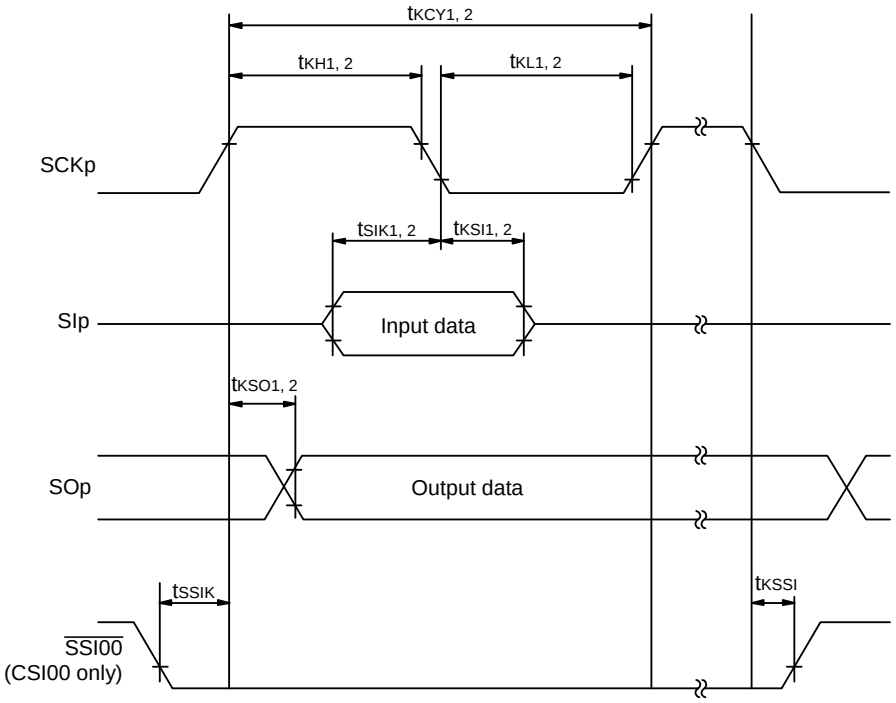



**Remark 1.** p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31)
**Remark 2.** m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13)

**CSI mode serial transfer timing (during communication at same potential)**
**(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)**




**CSI mode serial transfer timing (during communication at same potential)**
**(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**




**Remark 1.** p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31)
**Remark 2.** m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13)

### (4) During communication at same potential (simplified $I^2C$ mode)

**($T_A$ = -40 to +105°C, 2.4 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

| Parameter | Symbol | Conditions | HS (high-speed main) mode | | Unit |
|---|---|---|---|---|---|
| | | | MIN. | MAX. | |
| SCLr clock frequency | $f_{SCL}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | | 400 Note 1 | kHz |
| | | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V, $C_b$ = 100 pF, $R_b$ = 3 kΩ | | 100 Note 1 | kHz |
| Hold time when SCLr = “L” | $t_{LOW}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 1200 | | ns |
| | | 2.4V ≤ $EV_{DD0}$ ≤ 5.5 V, $C_b$ = 100 pF, $R_b$ = 3 kΩ | 4600 | | ns |
| Hold time when SCLr = “H” | $t_{HIGH}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 1200 | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V, $C_b$ = 100 pF, $R_b$ = 3 kΩ | 4600 | | ns |
| Data setup time (reception) | $t_{SU:DAT}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 1/$f_{MCK}$ + 220 Note 2 | | ns |
| | | 2.4V ≤ $EV_{DD0}$ ≤ 5.5 V, $C_b$ = 100 pF, $R_b$ = 3 kΩ | 1/$f_{MCK}$ + 580 Note 2 | | ns |
| Data hold time (transmission) | $t_{HD:DAT}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 0 | 770 | ns |
| | | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V, $C_b$ = 100 pF, $R_b$ = 3 kΩ | 0 | 1420 | ns |

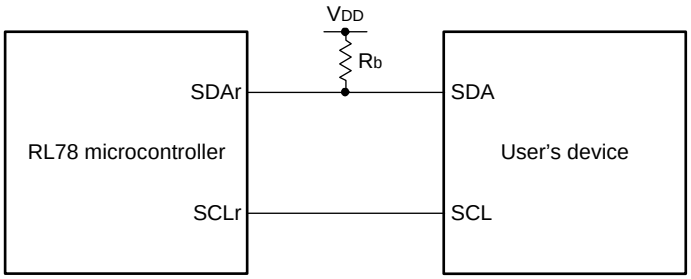
**Note 1.** The value must also be equal to or less than $f_{MCK}$/4.

**Note 2.** Set the $f_{MCK}$ value to keep the hold time of SCLr = “L” and SCLr = “H”.

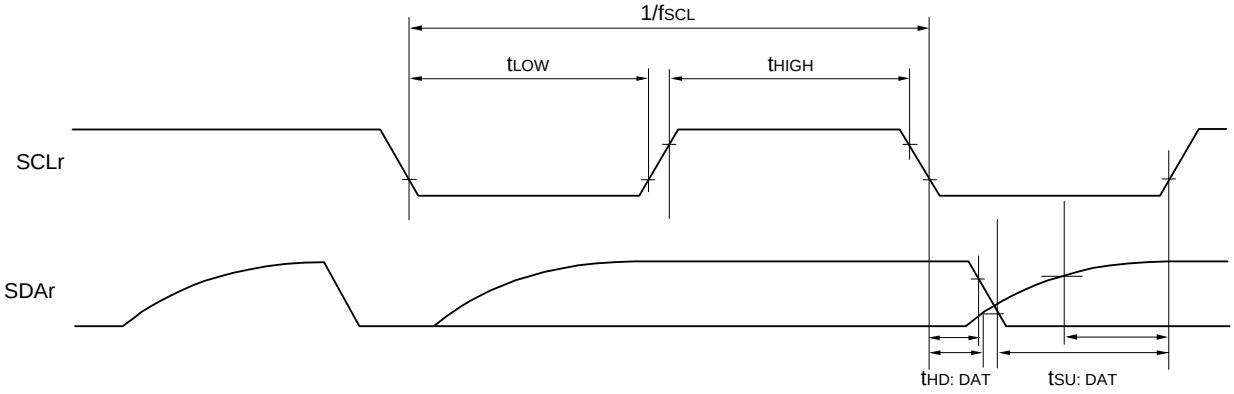
**Caution Select the normal input buffer and the N-ch open drain output ($V_{DD}$ tolerance (for the 30- to 52-pin products)/$EV_{DD}$ tolerance (for the 64- to 100-pin products)) mode for the SDAr pin and the normal output mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register h (POMh).**

(**Remarks** are listed on the next page.)

**Simplified I²C mode connection diagram (during communication at same potential)**




**Simplified I²C mode serial transfer timing (during communication at same potential)**




**Remark 1.** $R_b$[Ω]: Communication line (SDAr) pull-up resistance, $C_b$[F]: Communication line (SDAr, SCLr) load capacitance

**Remark 2.** r: IIC number (r = 00, 01, 10, 11, 20, 21, 30, 31), g: PIM number (g = 0, 1, 3 to 5, 14), h: POM number (h = 0, 1, 3 to 5, 7, 14)

**Remark 3.** $f_{MCK}$: Serial array unit operation clock frequency (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), mn = 00 to 03, 10 to 13)

### (5) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode)

**($T_A$ = -40 to +105°C, 2.4 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V) (1/2)**

| Parameter | Symbol | Conditions | | HS (high-speed main) mode | | Unit |
|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | |
| Transfer rate | | reception | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V | | $f_{MCK}$/12 Note 1 | bps |
| | | | Theoretical value of the maximum transfer rate $f_{MCK}$ = $f_{CLK}$ Note 3 | | 2.6 | Mbps |
| | | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | | $f_{MCK}$/12 Note 1 | bps |
| | | | Theoretical value of the maximum transfer rate $f_{MCK}$ = $f_{CLK}$ Note 3 | | 2.6 | Mbps |
| | | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V | | $f_{MCK}$/12 Notes 1, 2 | bps |
| | | | Theoretical value of the maximum transfer rate $f_{MCK}$ = $f_{CLK}$ Note 3 | | 2.6 | Mbps |

**Note 1.** Transfer rate in the SNOOZE mode is 4800 bps only.
However, the SNOOZE mode cannot be used when FRQSEL4 = 1.

**Note 2.** The following conditions are required for low voltage interface when $EV_{DD0}$ < $V_{DD}$.
2.4 V ≤ $EV_{DD0}$ < 2.7 V: MAX. 1.3 Mbps

**Note 3.** The maximum operating frequencies of the CPU/peripheral hardware clock ($f_{CLK}$) are:
HS (high-speed main) mode: 32 MHz (2.7 V ≤ $V_{DD}$ ≤ 5.5 V)
16 MHz (2.4 V ≤ $V_{DD}$ ≤ 5.5 V)

**Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output ($V_{DD}$ tolerance (for the 30- to 52-pin products)/$EV_{DD}$ tolerance (for the 64- to 100-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

**Remark 1.** $V_b$ [V]: Communication line voltage

**Remark 2.** q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 5, 14)

**Remark 3.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13)

**Remark 4.** UART2 cannot communicate at different potential when bit 1 (PIOR01) of peripheral I/O redirection register 0 (PIOR0) is 1.

### (5) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode)

**($T_A$ = -40 to +105°C, 2.4 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)** **(2/2)**

| Parameter | Symbol | Conditions | | HS (high-speed main) mode | | Unit |
|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | |
| Transfer rate | | transmission | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V | | Note 1 | bps |
| | | | Theoretical value of the maximum transfer rate $C_b$ = 50 pF, $R_b$ = 1.4 kΩ, $V_b$ = 2.7 V | | 2.6 Note 2 | Mbps |
| | | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | | Note 3 | bps |
| | | | Theoretical value of the maximum transfer rate $C_b$ = 50 pF, $R_b$ = 2.7 kΩ, $V_b$ = 2.3 V | | 1.2 Note 4 | Mbps |
| | | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V | | Note 5 | bps |
| | | | Theoretical value of the maximum transfer rate $C_b$ = 50 pF, $R_b$ = 5.5 kΩ, $V_b$ = 1.6 V | | 0.43 Note 6 | Mbps |

**Note 1.** The smaller maximum transfer rate derived by using $f_{MCK}$/12 or the following expression is the valid maximum transfer rate.
Expression for calculating the transfer rate when 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V and 2.7 V ≤ $V_b$ ≤ 4.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides

**Note 2.** This value as an example is calculated when the conditions described in the “Conditions” column are met.
Refer to **Note 1** above to calculate the maximum transfer rate under conditions of the customer.

**Note 3.** The smaller maximum transfer rate derived by using $f_{MCK}$/12 or the following expression is the valid maximum transfer rate.
Expression for calculating the transfer rate when 2.7 V ≤ $EV_{DD0}$ < 4.0 V and 2.3 V ≤ $V_b$ ≤ 2.7 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides

**Note 4.** This value as an example is calculated when the conditions described in the “Conditions” column are met.
Refer to **Note 3** above to calculate the maximum transfer rate under conditions of the customer.

**Note 5.** The smaller maximum transfer rate derived by using $f_{MCK}$/12 or the following expression is the valid maximum transfer rate.
Expression for calculating the transfer rate when 2.4 V ≤ $EV_{DD0}$ < 3.3 V and 1.6 V ≤ $V_b$ ≤ 2.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

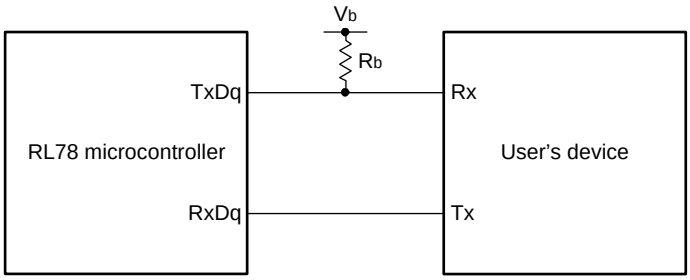
* This value is the theoretical value of the relative difference between the transmission and reception sides

**Note 6.** This value as an example is calculated when the conditions described in the “Conditions” column are met.
Refer to **Note 5** above to calculate the maximum transfer rate under conditions of the customer.

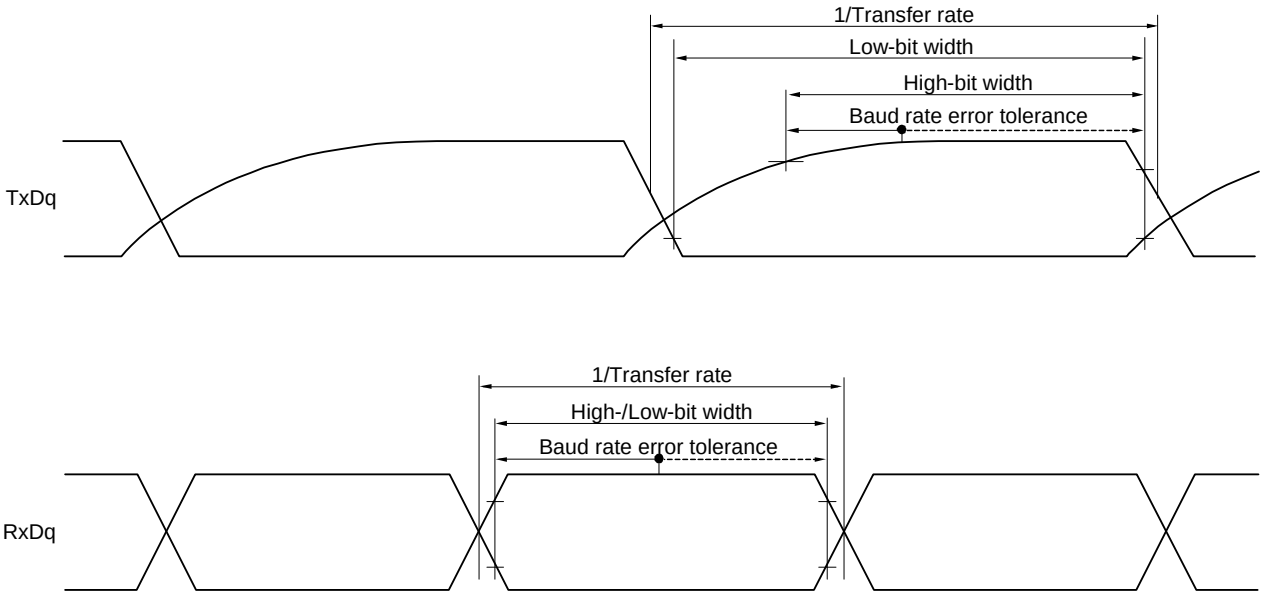
**Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output ($V_{DD}$ tolerance (for the 30- to 52-pin products)/$EV_{DD}$ tolerance (for the 64- to 100-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

(**Remarks** are listed on the next page.)

**UART mode connection diagram (during communication at different potential)**




**UART mode bit width (during communication at different potential) (reference)**




**Remark 1.** $R_b$[Ω]: Communication line (TxDq) pull-up resistance,
$C_b$[F]: Communication line (TxDq) load capacitance, $V_b$[V]: Communication line voltage

**Remark 2.** q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 5, 14)

**Remark 3.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

**Remark 4.** UART2 cannot communicate at different potential when bit 1 (PIOR01) of peripheral I/O redirection register 0 (PIOR0) is 1.

### (6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output)

**($T_A$ = -40 to +105°C, 2.4 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)** **(1/3)**

| Parameter | Symbol | Conditions | | HS (high-speed main) mode | | Unit |
|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | |
| SCKp cycle time | $t_{KCY1}$ | $t_{KCY1}$ ≥ 4/$f_{CLK}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | 600 | | ns |
| | | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | 1000 | | ns |
| | | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | 2300 | | ns |
| SCKp high-level width | $t_{KH1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | | $t_{KCY1}$/2 - 150 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | | $t_{KCY1}$/2 - 340 | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | | $t_{KCY1}$/2 - 916 | | ns |
| SCKp low-level width | $t_{KL1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | | $t_{KCY1}$/2 - 24 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | | $t_{KCY1}$/2 - 36 | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | | $t_{KCY1}$/2 - 100 | | ns |

**Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output ($V_{DD}$ tolerance (for the 30- to 52-pin products)/$EV_{DD}$ tolerance (for the 64- to 100-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

(**Remarks** are listed two pages after the next page.)

### (6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output)

**($T_A$ = -40 to +105°C, 2.4 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)** **(2/3)**

| Parameter | Symbol | Conditions | HS (high-speed main) mode | | Unit |
|---|---|---|---|---|---|
| | | | MIN. | MAX. | |
| SIp setup time (to SCKp↑) Note | $t_{SIK1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | 162 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | 354 | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | 958 | | ns |
| SIp hold time (from SCKp↑) Note | $t_{KSI1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | 38 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | 38 | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | 38 | | ns |
| Delay time from SCKp↓ to SOp output Note | $t_{KSO1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | | 200 | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | | 390 | ns |
| | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | | 966 | ns |

**Note** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

**Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output ($V_{DD}$ tolerance (for the 30- to 52-pin products)/$EV_{DD}$ tolerance (for the 64- to 100-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

(**Remarks** are listed on the page after the next page.)

### (6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output)

**($T_A$ = -40 to +105°C, 2.4 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)** **(3/3)**

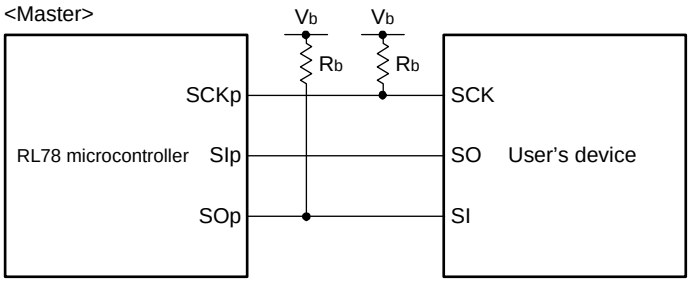
| Parameter | Symbol | Conditions | HS (high-speed main) mode | | Unit |
|---|---|---|---|---|---|
| | | | MIN. | MAX. | |
| SIp setup time (to SCKp↓) Note | $t_{SIK1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | 88 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | 88 | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | 220 | | ns |
| SIp hold time (from SCKp↓) Note | $t_{KSI1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | 38 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | 38 | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | 38 | | ns |
| Delay time from SCKp↑ to SOp output Note | $t_{KSO1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | | 50 | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | | 50 | ns |
| | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | | 50 | ns |

**Note** When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output ($V_{DD}$ tolerance (for the 30- to 52-pin products)/$EV_{DD}$ tolerance (for the 64- to 100-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

(**Remarks** are listed on the next page.)

**CSI mode connection diagram (during communication at different potential**



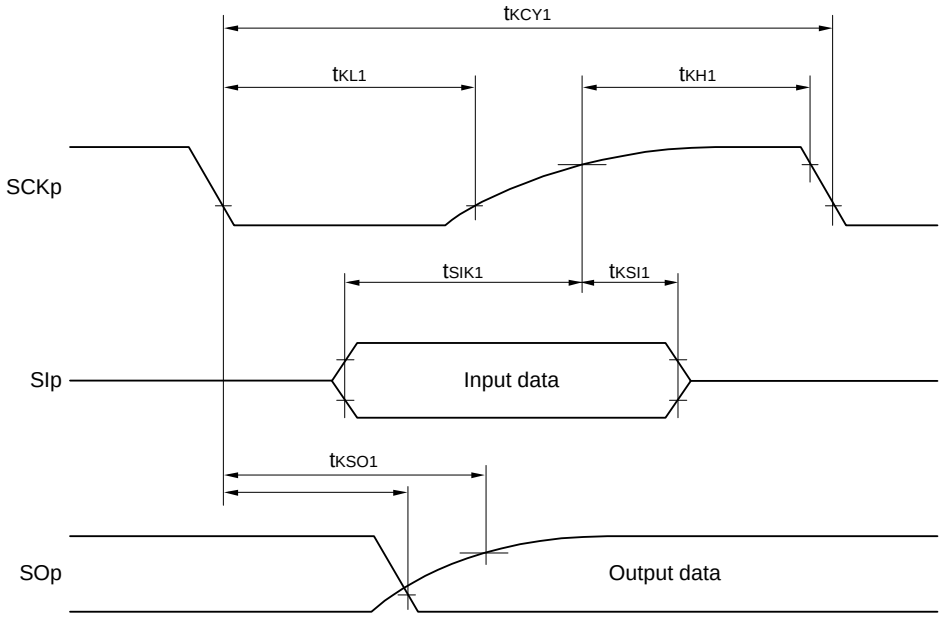

**Remark 5.** $R_b$[Ω]: Communication line (SCKp, SOp) pull-up resistance, $C_b$[F]: Communication line (SCKp, SOp) load capacitance, $V_b$[V]: Communication line voltage

**Remark 6.** p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM and POM number (g = 0, 1, 3 to 5, 14)

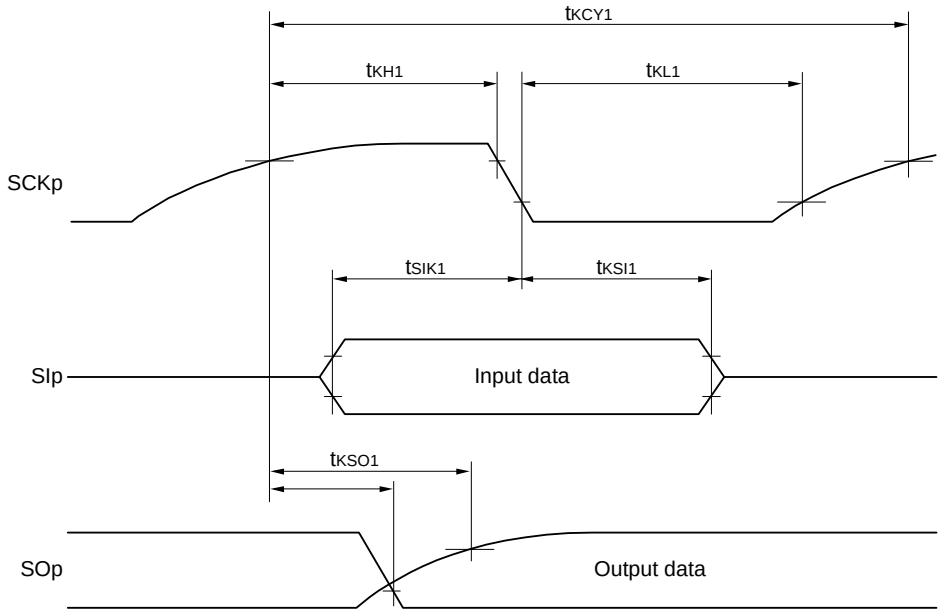
**Remark 7.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00))

**Remark 8.** CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

**CSI mode serial transfer timing (master mode) (during communication at different potential)**
**(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)**




**CSI mode serial transfer timing (master mode) (during communication at different potential)**
**(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**




**Remark 1.** p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM and POM number (g = 0, 1, 3 to 5, 14)

**Remark 2.** CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

### (7) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)

**($T_A$ = -40 to +105°C, 2.4 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) mode | | Unit |
|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | |
| SCKp cycle time Note 1 | $t_{KCY2}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V | 24 MHz < $f_{MCK}$ | 28/$f_{MCK}$ | | ns |
| | | | 20 MHz < $f_{MCK}$ ≤ 24 MHz | 24/$f_{MCK}$ | | ns |
| | | | 8 MHz < $f_{MCK}$ ≤ 20 MHz | 20/$f_{MCK}$ | | ns |
| | | | 4 MHz < $f_{MCK}$ ≤ 8 MHz | 16/$f_{MCK}$ | | ns |
| | | | $f_{MCK}$ ≤ 4 MHz | 12/$f_{MCK}$ | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | 24 MHz < $f_{MCK}$ | 40/$f_{MCK}$ | | ns |
| | | | 20 MHz < $f_{MCK}$ ≤ 24 MHz | 32/$f_{MCK}$ | | ns |
| | | | 16 MHz < $f_{MCK}$ ≤ 20 MHz | 28/$f_{MCK}$ | | ns |
| | | | 8 MHz < $f_{MCK}$ ≤ 16 MHz | 24/$f_{MCK}$ | | ns |
| | | | 4 MHz < $f_{MCK}$ ≤ 8 MHz | 16/$f_{MCK}$ | | ns |
| | | | $f_{MCK}$ ≤ 4 MHz | 12/$f_{MCK}$ | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V | 24 MHz < $f_{MCK}$ | 96/$f_{MCK}$ | | ns |
| | | | 20 MHz < $f_{MCK}$ ≤ 24 MHz | 72/$f_{MCK}$ | | ns |
| | | | 16 MHz < $f_{MCK}$ ≤ 20 MHz | 64/$f_{MCK}$ | | ns |
| | | | 8 MHz < $f_{MCK}$ ≤ 16 MHz | 52/$f_{MCK}$ | | ns |
| | | | 4 MHz < $f_{MCK}$ ≤ 8 MHz | 32/$f_{MCK}$ | | ns |
| | | | $f_{MCK}$ ≤ 4 MHz | 20/$f_{MCK}$ | | ns |
| SCKp high-/low-level width | $t_{KH2}$, $t_{KL2}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V | | $t_{KCY2}$/2 - 24 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | | $t_{KCY2}$/2 - 36 | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V | | $t_{KCY2}$/2 - 100 | | ns |
| SIp setup time (to SCKp↑) Note 2 | $t_{SIK2}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V | | 1/$f_{MCK}$ + 40 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | | 1/$f_{MCK}$ + 40 | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V | | 1/$f_{MCK}$ + 60 | | ns |
| SIp hold time (from SCKp↑) Note 3 | $t_{KSI2}$ | | | 1/$f_{MCK}$ + 62 | | ns |
| Delay time from SCKp↓ to SOp output Note 4 | $t_{KSO2}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | | | 2/$f_{MCK}$ + 240 | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | | | 2/$f_{MCK}$ + 428 | ns |
| | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 30 pF, $R_v$ = 5.5 kΩ | | | 2/$f_{MCK}$ + 1146 | ns |

(**Notes**, **Caution**, and **Remarks** are listed on the next page.)

**Note 1.** Transfer rate in the SNOOZE mode: MAX. 1 Mbps

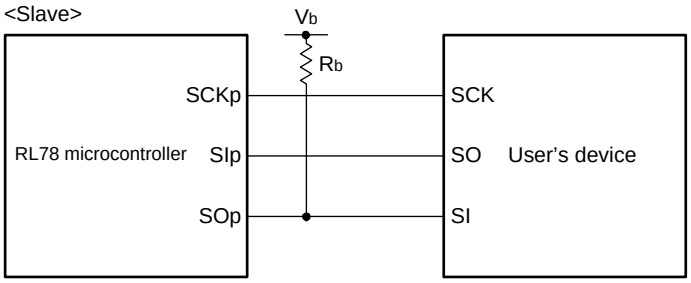
**Note 2.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 3.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 4.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Caution Select the TTL input buffer for the SIp pin and SCKp pin, and the N-ch open drain output ($V_{DD}$ tolerance (for the 30- to 52-pin products)/$EV_{DD}$ tolerance (for the 64- to 100-pin products)) mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

**CSI mode connection diagram (during communication at different potential)**



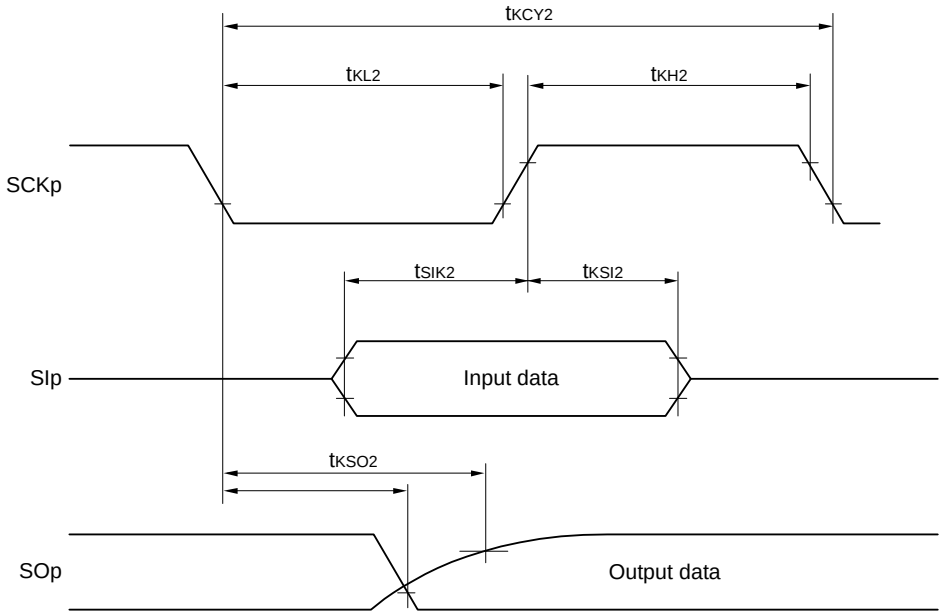

**Remark 1.** $R_b$[Ω]: Communication line (SOp) pull-up resistance, $C_b$[F]: Communication line (SOp) load capacitance, $V_b$[V]: Communication line voltage

**Remark 2.** p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM and POM number (g = 0, 1, 3 to 5, 14)

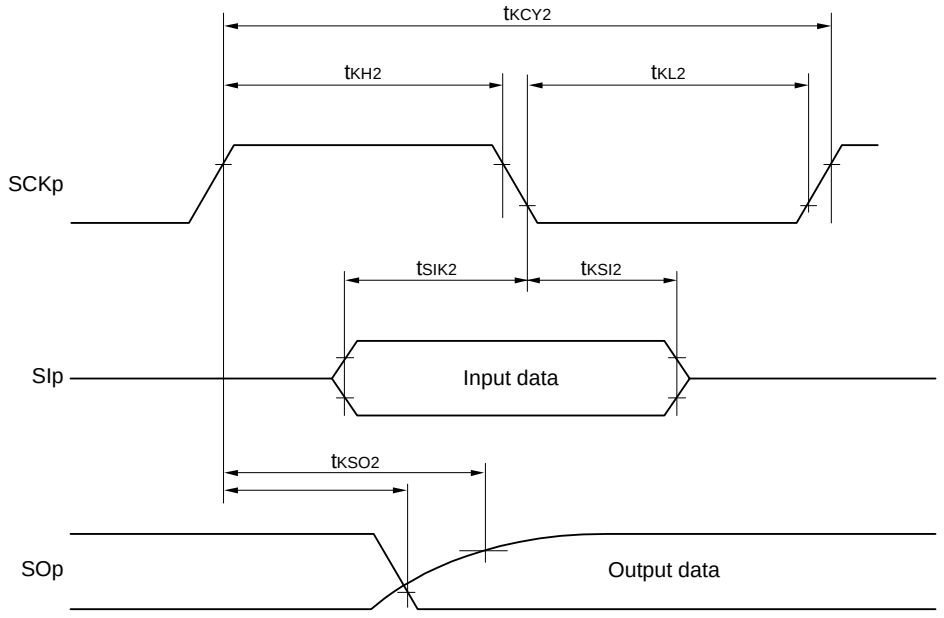
**Remark 3.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00, 01, 02, 10, 12, 13))

**Remark 4.** CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.
Also, communication at different potential cannot be performed during clock synchronous serial communication with the slave select function.

**CSI mode serial transfer timing (slave mode) (during communication at different potential)**
**(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)**




**CSI mode serial transfer timing (slave mode) (during communication at different potential)**
**(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**




**Remark 1.** p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM and POM number (g = 0, 1, 3 to 5, 14)

**Remark 2.** CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.
Also, communication at different potential cannot be performed during clock synchronous serial communication with the slave select function.

### (8) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified $I^2C$ mode)

**($T_A$ = -40 to +105°C, 2.4 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)** **(1/2)**

| Parameter | Symbol | Conditions | HS (high-speed main) mode | | Unit |
|---|---|---|---|---|---|
| | | | MIN. | MAX. | |
| SCLr clock frequency | $f_{SCL}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | | 400 Note 1 | kHz |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | | 400 Note 1 | kHz |
| | | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 100 pF, $R_b$ = 2.8 kΩ | | 100 Note 1 | kHz |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 100 pF, $R_b$ = 2.7 kΩ | | 100 Note 1 | kHz |
| | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 100 pF, $R_b$ = 5.5 kΩ | | 100 Note 1 | kHz |
| Hold time when SCLr = “L” | $t_{LOW}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 1200 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 1200 | | ns |
| | | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 100 pF, $R_b$ = 2.8 kΩ | 4600 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 100 pF, $R_b$ = 2.7 kΩ | 4600 | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 100 pF, $R_b$ = 5.5 kΩ | 4650 | | ns |
| Hold time when SCLr = “H” | $t_{HIGH}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 620 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 500 | | ns |
| | | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 100 pF, $R_b$ = 2.8 kΩ | 2700 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 100 pF, $R_b$ = 2.7 kΩ | 2400 | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 100 pF, $R_b$ = 5.5 kΩ | 1830 | | ns |

### (8) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified $I^2C$ mode)

**($T_A$ = -40 to +105°C, 2.4 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)** **(2/2)**

| Parameter | Symbol | Conditions | HS (high-speed main) mode | | Unit |
|---|---|---|---|---|---|
| | | | MIN. | MAX. | |
| Data setup time (reception) | $t_{SU:DAT}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 1/$f_{MCK}$ + 340 Note 2 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 1/$f_{MCK}$ + 340 Note 2 | | ns |
| | | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 100 pF, $R_b$ = 2.8 kΩ | 1/$f_{MCK}$ + 760 Note 2 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 100 pF, $R_b$ = 2.7 kΩ | 1/$f_{MCK}$ + 760 Note 2 | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 100 pF, $R_b$ = 5.5 kΩ | 1/$f_{MCK}$ + 570 Note 2 | | ns |
| Data hold time (transmission) | $t_{HD:DAT}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 0 | 770 | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 0 | 770 | ns |
| | | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 100 pF, $R_b$ = 2.8 kΩ | 0 | 1420 | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 100 pF, $R_b$ = 2.7 kΩ | 0 | 1420 | ns |
| | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 100 pF, $R_b$ = 5.5 kΩ | 0 | 1215 | ns |

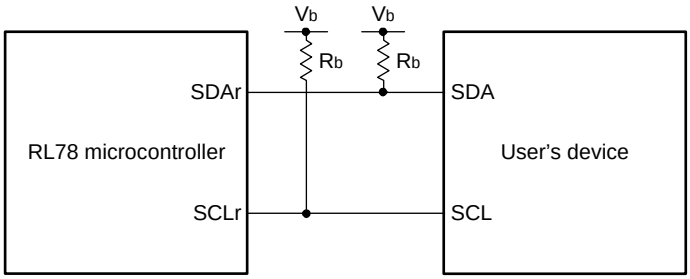
**Note 1.** The value must also be equal to or less than $f_{MCK}$/4.

**Note 2.** Set the $f_{MCK}$ value to keep the hold time of SCLr = "L" and SCLr = "H".

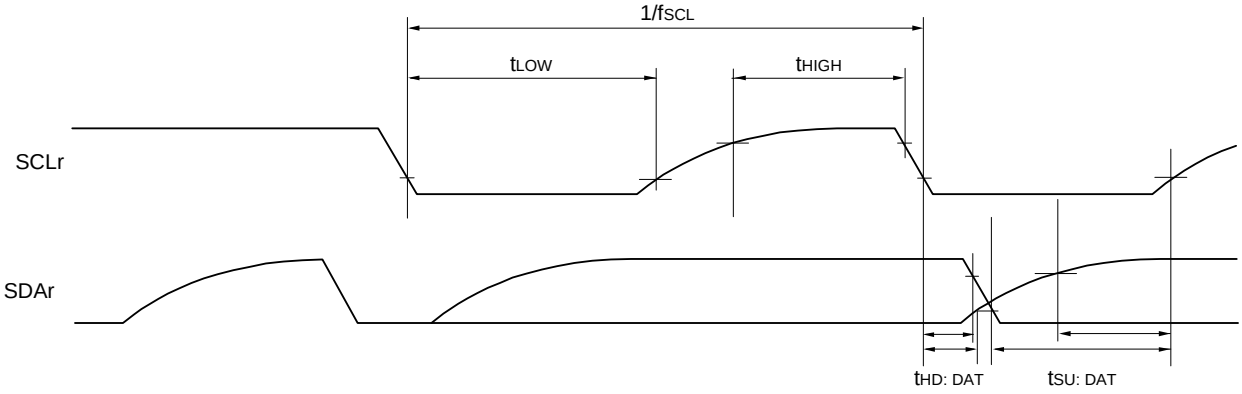
**Caution Select the TTL input buffer and the N-ch open drain output ($V_{DD}$ tolerance (for the 30- to 52-pin products)/$EV_{DD}$ tolerance (for the 64- to 100-pin products)) mode for the SDAr pin and the N-ch open drain output ($V_{DD}$ tolerance (for the 30- to 52-pin products)/$EV_{DD}$ tolerance (for the 64- to 100-pin products)) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

(**Remarks** are listed on the next page.)

**Simplified I²C mode connection diagram (during communication at different potential)**




**Simplified I²C mode serial transfer timing (during communication at different potential)**




**Remark 1.** $R_b$[Ω]: Communication line (SDAr, SCLr) pull-up resistance, $C_b$[F]: Communication line (SDAr, SCLr) load capacitance, $V_b$[V]: Communication line voltage

**Remark 2.** r: IIC number (r = 00, 01, 10, 11, 20, 30, 31), g: PIM, POM number (g = 0, 1, 3 to 5, 14)

**Remark 3.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), mn = 00, 01, 02, 10, 12, 13)

## 3.5.2 Serial interface IICA

**($T_A$ = -40 to +105°C, 2.4 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

| Parameter | Symbol | Conditions | HS (high-speed main) mode | | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Standard mode | | Fast mode | | |
| | | | MIN. | MAX. | MIN. | MAX. | |
| SCLA0 clock frequency | $f_{SCL}$ | Fast mode: $f_{CLK}$ ≥ 3.5 MHz | — | — | 0 | 400 | kHz |
| | | Standard mode: $f_{CLK}$ ≥ 1 MHz | 0 | 100 | — | — | kHz |
| Setup time of restart condition | $t_{SU: STA}$ | | 4.7 | | 0.6 | | µs |
| Hold time Note 1 | $t_{HD: STA}$ | | 4.0 | | 0.6 | | µs |
| Hold time when SCLA0 = "L" | $t_{LOW}$ | | 4.7 | | 1.3 | | µs |
| Hold time when SCLA0 = "H" | $t_{HIGH}$ | | 4.0 | | 0.6 | | µs |
| Data setup time (reception) | $t_{SU: DAT}$ | | 250 | | 100 | | ns |
| Data hold time (transmission) Note 2 | $t_{HD: DAT}$ | | 0 | 3.45 | 0 | 0.9 | µs |
| Setup time of stop condition | $t_{SU: STO}$ | | 4.0 | | 0.6 | | µs |
| Bus-free time | $t_{BUF}$ | | 4.7 | | 1.3 | | µs |

**Note 1.** The first clock pulse is generated after this period when the start/restart condition is detected.

**Note 2.** The maximum value (MAX.) of $t_{HD: DAT}$ is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

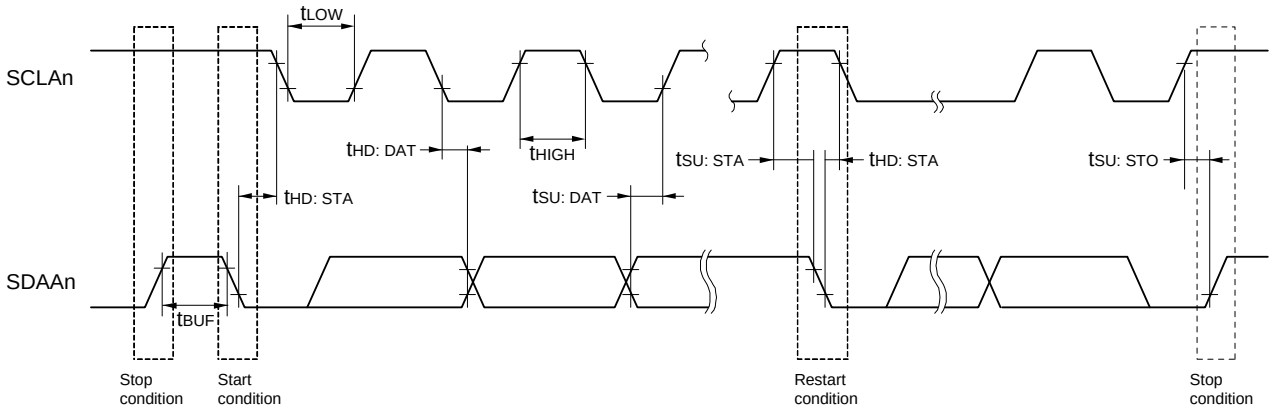
**Caution The values in the above table are applied even when bit 2 (PIOR02) in the peripheral I/O redirection register 0 (PIOR0) is 1. At this time, the pin characteristics ($I_{OH1}$, $I_{OL1}$, $V_{OH1}$, $V_{OL1}$) must satisfy the values in the redirect destination.**

**Remark** The maximum value of $C_b$ (communication line capacitance) and the value of $R_b$ (communication line pull-up resistor) at that time in each mode are as follows.

Standard mode: $C_b$ = 400 pF, $R_b$ = 2.7 kΩ

Fast mode: $C_b$ = 320 pF, $R_b$ = 1.1 kΩ

**IICA serial transfer timing**




**Remark** n = 0, 1

## 3.6 Analog Characteristics

### 3.6.1 A/D converter characteristics

**Classification of A/D converter characteristics**

| Reference Voltage / Input channel | Reference voltage (+) = $AV_{REFP}$<br>Reference voltage (-) = $AV_{REFM}$ | Reference voltage (+) = $V_{DD}$<br>Reference voltage (-) = $V_{SS}$ | Reference voltage (+) = $V_{BGR}$<br>Reference voltage (-)= $AV_{REFM}$ |
|---|---|---|---|
| ANI0 to ANI14 | Refer to **3.6.1 (1)**. | Refer to **3.6.1 (3)**. | Refer to **3.6.1 (4)**. |
| ANI16 to ANI20 | Refer to **3.6.1 (2)**. | | |
| Internal reference voltage<br>Temperature sensor output voltage | Refer to **3.6.1 (1)**. | | — |

**(1) When reference voltage (+) = $AV_{REFP}$/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = $AV_{REFM}$/ANI1 (ADREFM = 1), target pin: ANI2 to ANI14, internal reference voltage, and temperature sensor output voltage**

**($T_A$ = -40 to +105°C, 2.4 V ≤ $AV_{REFP}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V, Reference voltage (+) = $AV_{REFP}$, Reference voltage (-) = $AV_{REFM}$ = 0 V)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Resolution | RES | | | 8 | | 10 | bit |
| Overall error Note 1 | AINL | 10-bit resolution<br>$AV_{REFP}$ = $V_{DD}$ Note 3 | 2.4 V ≤ $AV_{REFP}$ ≤ 5.5 V | | 1.2 | ±3.5 | LSB |
| Conversion time | $t_{CONV}$ | 10-bit resolution<br>Target pin: ANI2 to ANI14 | 3.6 V ≤ $V_{DD}$ ≤ 5.5 V | 2.125 | | 39 | μs |
| | | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 3.1875 | | 39 | μs |
| | | | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | 17 | | 39 | μs |
| | | 10-bit resolution<br>Target pin: Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode) | 3.6 V ≤ $V_{DD}$ ≤ 5.5 V | 2.375 | | 39 | μs |
| | | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 3.5625 | | 39 | μs |
| | | | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | 17 | | 39 | μs |
| Zero-scale error Notes 1, 2 | $E_{ZS}$ | 10-bit resolution<br>$AV_{REFP}$ = $V_{DD}$ Note 3 | 2.4 V ≤ $AV_{REFP}$ ≤ 5.5 V | | | ±0.25 | %FSR |
| Full-scale error Notes 1, 2 | $E_{FS}$ | 10-bit resolution<br>$AV_{REFP}$ = $V_{DD}$ Note 3 | 2.4 V ≤ $AV_{REFP}$ ≤ 5.5 V | | | ±0.25 | %FSR |
| Integral linearity error Note 1 | ILE | 10-bit resolution<br>$AV_{REFP}$ = $V_{DD}$ Note 3 | 2.4 V ≤ $AV_{REFP}$ ≤ 5.5 V | | | ±2.5 | LSB |
| Differential linearity error Note 1 | DLE | 10-bit resolution<br>$AV_{REFP}$ = $V_{DD}$ Note 3 | 2.4 V ≤ $AV_{REFP}$ ≤ 5.5 V | | | ±1.5 | LSB |
| Analog input voltage | $V_{AIN}$ | ANI2 to ANI14 | | 0 | | $AV_{REFP}$ | V |
| | | Internal reference voltage output<br>(2.4 V ≤ $V_{DD}$ ≤ 5.5 V, HS (high-speed main) mode) | | $V_{BGR}$ Note 4 | | | V |
| | | Temperature sensor output voltage<br>(2.4 V ≤ $V_{DD}$ ≤ 5.5 V, HS (high-speed main) mode) | | $V_{TMPS25}$ Note 4 | | | V |

**Note 1.** Excludes quantization error (±1/2 LSB).

**Note 2.** This value is indicated as a ratio (%FSR) to the full-scale value.

**Note 3.** When $AV_{REFP}$ < $V_{DD}$, the MAX. values are as follows.

Overall error: Add ±1.0 LSB to the MAX. value when $AV_{REFP}$ = $V_{DD}$.

Zero-scale error/Full-scale error: Add ±0.05%FSR to the MAX. value when $AV_{REFP}$ = $V_{DD}$.

Integral linearity error/ Differential linearity error: Add ±0.5 LSB to the MAX. value when $AV_{REFP}$ = $V_{DD}$.

**Note 4.** Refer to **3.6.2 Temperature sensor characteristics/internal reference voltage characteristic**.

**(2) When reference voltage (+) = $AV_{REFP}$/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = $AV_{REFM}$/ANI1 (ADREFM = 1), target pin: ANI16 to ANI20**

**($T_A$ = -40 to +105°C, 2.4 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, 2.4 V ≤ $AV_{REFP}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V, Reference voltage (+) = $AV_{REFP}$, Reference voltage (-) = $AV_{REFM}$ = 0 V)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Resolution | RES | | | 8 | | 10 | bit |
| Overall error Note 1 | AINL | 10-bit resolution<br>$EV_{DD0}$ ≤ $AV_{REFP}$ = $V_{DD}$ Notes 3, 4 | 2.4 V ≤ $AV_{REFP}$ ≤ 5.5 V | | 1.2 | ±5.0 | LSB |
| Conversion time | $t_{CONV}$ | 10-bit resolution<br>Target ANI pin: ANI16 to ANI20 | 3.6 V ≤ $V_{DD}$ ≤ 5.5 V | 2.125 | | 39 | μs |
| | | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 3.1875 | | 39 | μs |
| | | | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | 17 | | 39 | μs |
| Zero-scale error Notes 1, 2 | $E_{ZS}$ | 10-bit resolution<br>$EV_{DD0}$ ≤ $AV_{REFP}$ = $V_{DD}$ Notes 3, 4 | 2.4 V ≤ $AV_{REFP}$ ≤ 5.5 V | | | ±0.35 | %FSR |
| Full-scale error Notes 1, 2 | $E_{FS}$ | 10-bit resolution<br>$EV_{DD0}$ ≤ $AV_{REFP}$ = $V_{DD}$ Notes 3, 4 | 2.4 V ≤ $AV_{REFP}$ ≤ 5.5 V | | | ±0.35 | %FSR |
| Integral linearity error Note 1 | ILE | 10-bit resolution<br>$EV_{DD0}$ ≤ $AV_{REFP}$ = $V_{DD}$ Notes 3, 4 | 2.4 V ≤ $AV_{REFP}$ ≤ 5.5 V | | | ±3.5 | LSB |
| Differential linearity error Note 1 | DLE | 10-bit resolution<br>$EV_{DD0}$ ≤ $AV_{REFP}$ = $V_{DD}$ Notes 3, 4 | 2.4 V ≤ $AV_{REFP}$ ≤ 5.5 V | | | ±2.0 | LSB |
| Analog input voltage | $V_{AIN}$ | ANI16 to ANI20 | | 0 | | $AV_{REFP}$ and $EV_{DD0}$ | V |

**Note 1.** Excludes quantization error (±1/2 LSB).

**Note 2.** This value is indicated as a ratio (%FSR) to the full-scale value.

**Note 3.** When $EV_{DD0}$ ≤ $AV_{REFP}$ ≤ $V_{DD}$, the MAX. values are as follows.

Overall error: Add ±1.0 LSB to the MAX. value when $AV_{REFP}$ = $V_{DD}$.

Zero-scale error/Full-scale error: Add ±0.05%FSR to the MAX. value when $AV_{REFP}$ = $V_{DD}$.

Integral linearity error/ Differential linearity error: Add ±0.5 LSB to the MAX. value when $AV_{REFP}$ = $V_{DD}$.

**Note 4.** When $AV_{REFP}$ < $EV_{DD0}$ ≤ $V_{DD}$, the MAX. values are as follows.

Overall error: Add ±4.0 LSB to the MAX. value when $AV_{REFP}$ = $V_{DD}$.

Zero-scale error/Full-scale error: Add ±0.20%FSR to the MAX. value when $AV_{REFP}$ = $V_{DD}$.

Integral linearity error/ Differential linearity error: Add ±2.0 LSB to the MAX. value when $AV_{REFP}$ = $V_{DD}$.

**(3) When reference voltage (+) = $V_{DD}$ (ADREFP1 = 0, ADREFP0 = 0), reference voltage (-) = $V_{SS}$ (ADREFM = 0), target pin: ANI0 to ANI14, ANI16 to ANI20, internal reference voltage, and temperature sensor output voltage**

**($T_A$ = -40 to +105°C, 2.4 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V, Reference voltage (+) = $V_{DD}$, Reference voltage (-) = $V_{SS}$)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Resolution | RES | | | 8 | | 10 | bit |
| Overall error Note 1 | AINL | 10-bit resolution | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | | 1.2 | ±7.0 | LSB |
| Conversion time | $t_{CONV}$ | 10-bit resolution<br>Target pin: ANI0 to ANI14, ANI16 to ANI20 | 3.6 V ≤ $V_{DD}$ ≤ 5.5 V | 2.125 | | 39 | µs |
| | | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 3.1875 | | 39 | µs |
| | | | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | 17 | | 39 | µs |
| | | 10-bit resolution<br>Target pin: internal reference voltage, and temperature sensor output voltage<br>(HS (high-speed main) mode) | 3.6 V ≤ $V_{DD}$ ≤ 5.5 V | 2.375 | | 39 | µs |
| | | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 3.5625 | | 39 | µs |
| | | | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | 17 | | 39 | µs |
| Zero-scale error Notes 1, 2 | $E_{ZS}$ | 10-bit resolution | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | | | ±0.60 | %FSR |
| Full-scale error Notes 1, 2 | $E_{FS}$ | 10-bit resolution | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | | | ±0.60 | %FSR |
| Integral linearity error Note 1 | ILE | 10-bit resolution | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | | | ±4.0 | LSB |
| Differential linearity error Note 1 | DLE | 10-bit resolution | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | | | ±2.0 | LSB |
| Analog input voltage | $V_{AIN}$ | ANI0 to ANI14 | | 0 | | $V_{DD}$ | V |
| | | ANI16 to ANI20 | | 0 | | $EV_{DD0}$ | V |
| | | Internal reference voltage<br>(2.4 V ≤ $V_{DD}$ ≤ 5.5 V, HS (high-speed main) mode) | | $V_{BGR}$ Note 3 | | | V |
| | | Temperature sensor output voltage<br>(2.4 V ≤ $V_{DD}$ ≤ 5.5 V, HS (high-speed main) mode) | | $V_{TMPS25}$ Note 3 | | | V |

**Note 1.** Excludes quantization error (±1/2 LSB).

**Note 2.** This value is indicated as a ratio (% FSR) to the full-scale value.

**Note 3.** Refer to **3.6.2 Temperature sensor characteristics/internal reference voltage characteristic**.

**(4) When reference voltage (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), reference voltage (-) = $AV_{REFM}$/ANI1 (ADREFM = 1), target pin: ANI0, ANI2 to ANI14, ANI16 to ANI20**

**($T_A$ = -40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, 1.6 V ≤ $EV_{DD}$ = $EV_{DD1}$ ≤ $V_{DD}$, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V,**
**Reference voltage (+) = $V_{BGR}$ Note 3, Reference voltage (-) = $AV_{REFM}$ = 0 V Note 4, HS (high-speed main) mode)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Resolution | RES | | | | 8 | | bit |
| Conversion time | $t_{CONV}$ | 8-bit resolution | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | 17 | | 39 | μs |
| Zero-scale error Notes 1, 2 | $E_{ZS}$ | 8-bit resolution | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | | | ±0.60 | % FSR |
| Integral linearity error Note 1 | ILE | 8-bit resolution | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | | | ±2.0 | LSB |
| Differential linearity error Note 1 | DLE | 8-bit resolution | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | | | ±1.0 | LSB |
| Analog input voltage | $V_{AIN}$ | | | 0 | | $V_{BGR}$ Note 3 | V |

**Note 1.** Excludes quantization error (±1/2 LSB).

**Note 2.** This value is indicated as a ratio (% FSR) to the full-scale value.

**Note 3.** Refer to **3.6.2 Temperature sensor characteristics/internal reference voltage characteristic**.

**Note 4.** When reference voltage (-) = $V_{SS}$, the MAX. values are as follows.

Zero-scale error: Add ±0.35%FSR to the MAX. value when reference voltage (-) = $AV_{REFM}$.

Integral linearity error: Add ±0.5 LSB to the MAX. value when reference voltage (-) = $AV_{REFM}$.

Differential linearity error: Add ±0.2 LSB to the MAX. value when reference voltage (-) = $AV_{REFM}$.

### 3.6.2 Temperature sensor characteristics/internal reference voltage characteristic

**($T_A$ = -40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V, HS (high-speed main) mode)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Temperature sensor output voltage | $V_{TMPS25}$ | Setting ADS register = 80H, $T_A$ = +25°C | | 1.05 | | V |
| Internal reference voltage | $V_{BGR}$ | Setting ADS register = 81H | 1.38 | 1.45 | 1.5 | V |
| Temperature coefficient | $F_{VTMPS}$ | Temperature sensor that depends on the temperature | | -3.6 | | mV/°C |
| Operation stabilization wait time | $t_{AMP}$ | | 5 | | | μs |

### 3.6.3 D/A converter characteristics

**($T_A$ = -40 to +105°C, 2.4 V ≤ $EV_{SS0}$ = $EV_{SS1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Resolution | RES | | | | | 8 | bit |
| Overall error | AINL | Rload = 4 MΩ | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | | | ±2.5 | LSB |
| | | Rload = 8 MΩ | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | | | ±2.5 | LSB |
| Settling time | $t_{SET}$ | Cload = 20 pF | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | | | 3 | μs |
| | | | 2.4 V ≤ $V_{DD}$ < 2.7 V | | | 6 | μs |

## 3.6.4 Comparator

**($T_A$ = -40 to +105°C, 2.4 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Input voltage range | Ivref | | | 0 | | $EV_{DD0}$ - 1.4 | V |
| | Ivcmp | | | -0.3 | | $EV_{DD0}$ + 0.3 | V |
| Output delay | td | $V_{DD}$ = 3.0 V<br>Input slew rate > 50 mV/µs | Comparator high-speed mode, standard mode | | | 1.2 | µs |
| | | | Comparator high-speed mode, window mode | | | 2.0 | µs |
| | | | Comparator low-speed mode, standard mode | | 3.0 | 5.0 | µs |
| High-electric-potential reference voltage | VTW+ | Comparator high-speed mode, window mode | | | 0.76 $V_{DD}$ | | V |
| Low-electric-potential reference voltage | VTW- | Comparator high-speed mode, window mode | | | 0.24 $V_{DD}$ | | V |
| Operation stabilization wait time | $t_{CMP}$ | | | 100 | | | µs |
| Internal reference voltage Note | $V_{BGR}$ | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, HS (high-speed main) mode | | 1.38 | 1.45 | 1.50 | V |

**Note** Not usable in sub-clock operation or STOP mode.

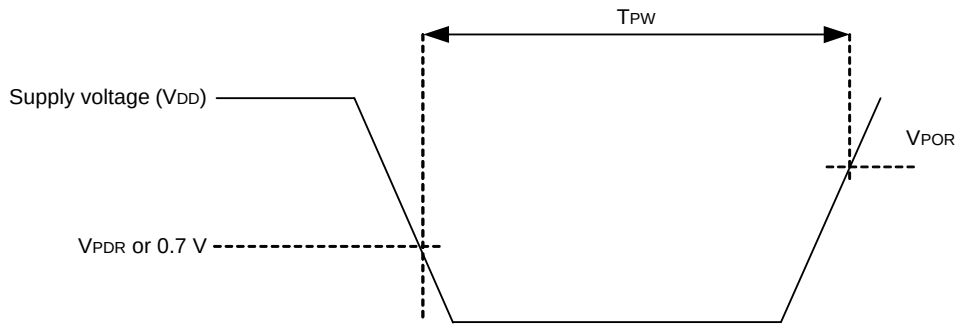
## 3.6.5 POR circuit characteristics

**($T_A$ = -40 to +105°C, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Power on/down reset threshold | $V_{POR}$ | Voltage threshold on $V_{DD}$ rising | 1.45 | 1.51 | 1.57 | V |
| | $V_{PDR}$ | Voltage threshold on $V_{DD}$ falling Note 1 | 1.44 | 1.50 | 1.56 | V |
| Minimum pulse width Note 2 | $T_{PW}$ | | 300 | | | µs |

**Note 1.** However, when the operating voltage falls while the LVD is off, enter STOP mode, or enable the reset status using the external reset pin before the voltage falls below the operating voltage range shown in 3.4 AC Characteristics.

**Note 2.** Minimum time required for a POR reset when $V_{DD}$ exceeds below $V_{PDR}$. This is also the minimum time required for a POR reset from when $V_{DD}$ exceeds below 0.7 V to when $V_{DD}$ exceeds $V_{POR}$ while STOP mode is entered or the main system clock is stopped through setting bit 0 (HIOSTOP) and bit 7 (MSTOP) in the clock operation status control register (CSC).



## 3.6.6 LVD circuit characteristics

**(1) Reset Mode and Interrupt Mode**

**($T_A$ = -40 to +105°C, $V_{PDR} \leq V_{DD} \leq$ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Voltage detection threshold | Supply voltage level | $V_{LVD0}$ | Rising edge | 3.90 | 4.06 | 4.22 | V |
| | | | Falling edge | 3.83 | 3.98 | 4.13 | V |
| | | $V_{LVD1}$ | Rising edge | 3.60 | 3.75 | 3.90 | V |
| | | | Falling edge | 3.53 | 3.67 | 3.81 | V |
| | | $V_{LVD2}$ | Rising edge | 3.01 | 3.13 | 3.25 | V |
| | | | Falling edge | 2.94 | 3.06 | 3.18 | V |
| | | $V_{LVD3}$ | Rising edge | 2.90 | 3.02 | 3.14 | V |
| | | | Falling edge | 2.85 | 2.96 | 3.07 | V |
| | | $V_{LVD4}$ | Rising edge | 2.81 | 2.92 | 3.03 | V |
| | | | Falling edge | 2.75 | 2.86 | 2.97 | V |
| | | $V_{LVD5}$ | Rising edge | 2.70 | 2.81 | 2.92 | V |
| | | | Falling edge | 2.64 | 2.75 | 2.86 | V |
| | | $V_{LVD6}$ | Rising edge | 2.61 | 2.71 | 2.81 | V |
| | | | Falling edge | 2.55 | 2.65 | 2.75 | V |
| | | $V_{LVD7}$ | Rising edge | 2.51 | 2.61 | 2.71 | V |
| | | | Falling edge | 2.45 | 2.55 | 2.65 | V |
| Minimum pulse width | | $t_{LW}$ | | 300 | | | µs |
| Detection delay time | | | | | | 300 | µs |

**(2) Interrupt & Reset Mode**

**($T_A$ = -40 to +105°C, $V_{PDR} \leq V_{DD} \leq$ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|
| Voltage detection threshold | $V_{LVDD0}$ | $V_{POC2}$, $V_{POC1}$, $V_{POC0}$ = 0, 1, 1, falling reset voltage | | | 2.64 | 2.75 | 2.86 | V |
| | $V_{LVDD1}$ | | LVIS1, LVIS0 = 1, 0 | Rising release reset voltage | 2.81 | 2.92 | 3.03 | V |
| | | | | Falling interrupt voltage | 2.75 | 2.86 | 2.97 | V |
| | $V_{LVDD2}$ | | LVIS1, LVIS0 = 0, 1 | Rising release reset voltage | 2.90 | 3.02 | 3.14 | V |
| | | | | Falling interrupt voltage | 2.85 | 2.96 | 3.07 | V |
| | $V_{LVDD3}$ | | LVIS1, LVIS0 = 0, 0 | Rising release reset voltage | 3.90 | 4.06 | 4.22 | V |
| | | | | Falling interrupt voltage | 3.83 | 3.98 | 4.13 | V |

## 3.6.7 Power supply voltage rising slope characteristics

**($T_A$ = -40 to +105°C, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Power supply voltage rising slope | $S_{VDD}$ | | | | 54 | V/ms |

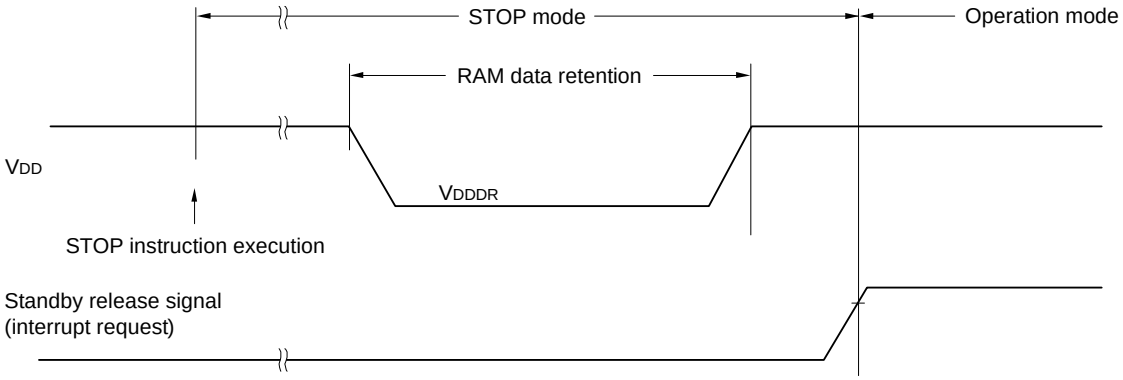
**Caution Make sure to keep the internal reset state by the LVD circuit or an external reset until $V_{DD}$ reaches the operating voltage range shown in 3.4 AC Characteristics.**

## 3.7 RAM Data Retention Characteristics

**($T_A$ = -40 to +105°C, $V_{SS}$ = 0V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Data retention supply voltage | $V_{DDDR}$ | | 1.44 Note | | 5.5 | V |

**Note** The value depends on the POR detection voltage. When the voltage drops, the RAM data is retained before a POR reset is effected, but RAM data is not retained when a POR reset is effected.




## 3.8 Flash Memory Programming Characteristics

**($T_A$ = -40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| System clock frequency | $f_{CLK}$ | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | 1 | | 32 | MHz |
| Number of code flash rewrites<br>Notes 1, 2, 3 | $C_{erwr}$ | Retained for 20 years<br>$T_A$ = 85°C Note 4 | 1,000 | | | Times |
| Number of data flash rewrites<br>Notes 1, 2, 3 | | Retained for 1 year<br>$T_A$ = 25°C | | 1,000,000 | | |
| | | Retained for 5 years<br>$T_A$ = 85°C Note 4 | 100,000 | | | |
| | | Retained for 20 years<br>$T_A$ = 85°C Note 4 | 10,000 | | | |

**Note 1.** 1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until next rewrite after the rewrite.

**Note 2.** When using flash memory programmer and Renesas Electronics self-programming library

**Note 3.** These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

**Note 4.** This temperature is the average value at which data are retained.

## 3.9 Dedicated Flash Memory Programmer Communication (UART)

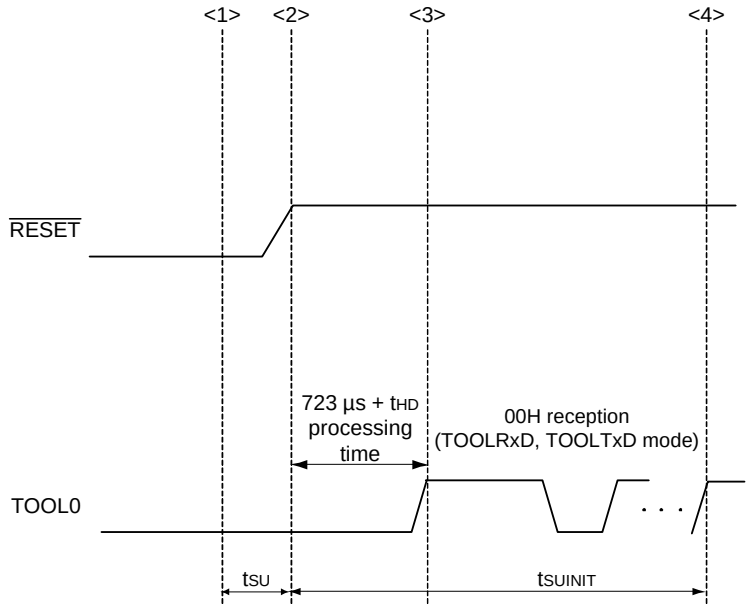
**($T_A$ = -40 to +105°C, 2.4 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Transfer rate | | During serial programming | 115,200 | | 1,000,000 | bps |

## 3.10 Timing of Entry to Flash Memory Programming Modes

**($T_A$ = -40 to +105°C, 2.4 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| How long from when an external reset ends until the initial communication settings are specified | $t_{SUINIT}$ | POR and LVD reset must end before the external reset ends. | | | 100 | ms |
| How long from when the TOOL0 pin is placed at the low level until an external reset ends | $t_{SU}$ | POR and LVD reset must end before the external reset ends. | 10 | | | μs |
| How long the TOOL0 pin must be kept at the low level after an external reset ends (excluding the processing time of the firmware to control the flash memory) | $t_{HD}$ | POR and LVD reset must end before the external reset ends. | 1 | | | ms |



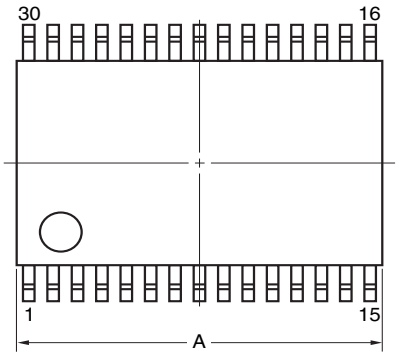

<1> The low level is input to the TOOL0 pin.
<2> The external reset ends (POR and LVD reset must end before the external reset ends).
<3> The TOOL0 pin is set to the high level.
<4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

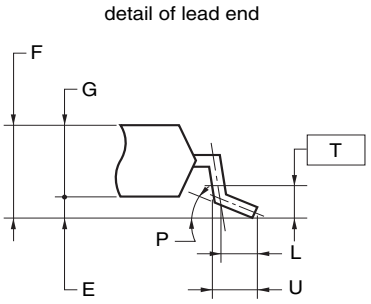
**Remark** $t_{SUINIT}$: The segment shows that it is necessary to finish specifying the initial communication settings within 100 ms from when the external resets end.
$t_{SU}$: How long from when the TOOL0 pin is placed at the low level until a pin reset ends
$t_{HD}$: How long to keep the TOOL0 pin at the low level from when the external resets end (excluding the processing time of the firmware to control the flash memory)

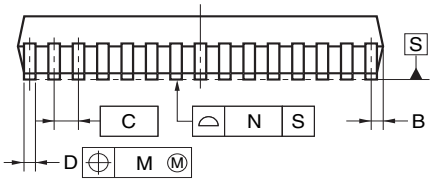
# 4. PACKAGE DRAWINGS

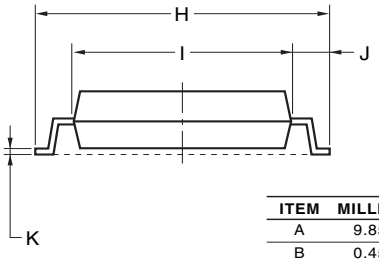
## <R> 4.1 30-pin Package

| JEITA Package Code | RENESAS Code | Previous Code | MASS (TYP.) [g] |
|---|---|---|---|
| P-LSSOP30-0300-0.65 | PLSP0030JB-B | S30MC-65-5A4-3 | 0.18 |




**NOTE**
Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

| ITEM | MILLIMETERS |
|---|---|
| A | 9.85±0.15 |
| B | 0.45 MAX. |
| C | 0.65 (T.P.) |
| D | $0.24^{+0.08}_{-0.07}$ |
| E | 0.1±0.05 |
| F | 1.3±0.1 |
| G | 1.2 |
| H | 8.1±0.2 |
| I | 6.1±0.2 |
| J | 1.0±0.2 |
| K | 0.17±0.03 |
| L | 0.5 |
| M | 0.13 |
| N | 0.10 |
| P | $3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$ |
| T | 0.25 |
| U | 0.6±0.15 |

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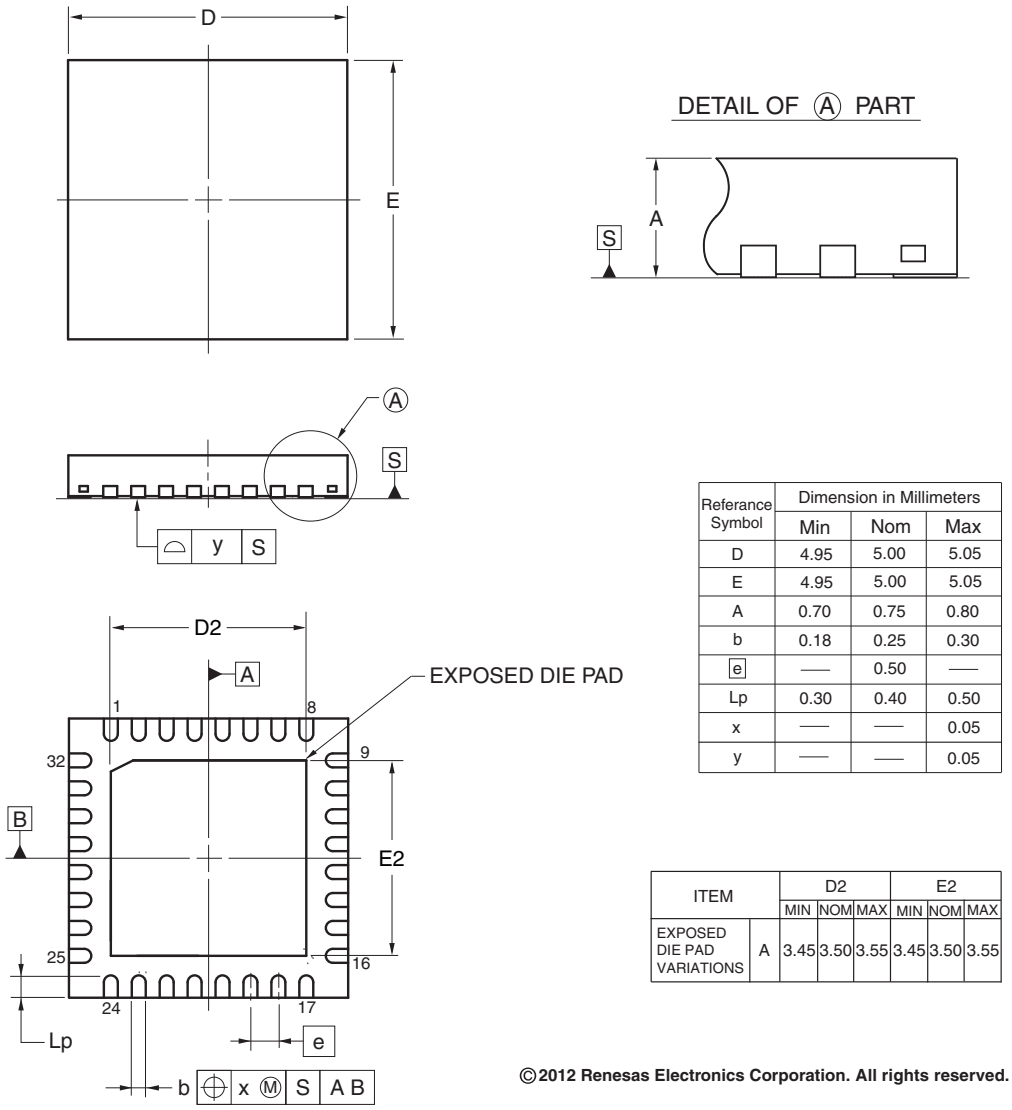
## <R> 4.2 32-pin Package

| JEITA Package Code | RENESAS Code | Previous Code | MASS (TYP.) [g] |
|---|---|---|---|
| P-HWQFN32-5x5-0.50 | PWQN0032KB-A | P32K8-50-3B4-4 | 0.06 |




| Referance Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 4.95 | 5.00 | 5.05 |
| E | 4.95 | 5.00 | 5.05 |
| A | 0.70 | 0.75 | 0.80 |
| b | 0.18 | 0.25 | 0.30 |
| e | — | 0.50 | — |
| Lp | 0.30 | 0.40 | 0.50 |
| x | — | — | 0.05 |
| y | — | — | 0.05 |

| ITEM | | D2 | | | E2 | | |
|---|---|---|---|---|---|---|---|
| | | MIN | NOM | MAX | MIN | NOM | MAX |
| EXPOSED DIE PAD VARIATIONS | A | 3.45 | 3.50 | 3.55 | 3.45 | 3.50 | 3.55 |

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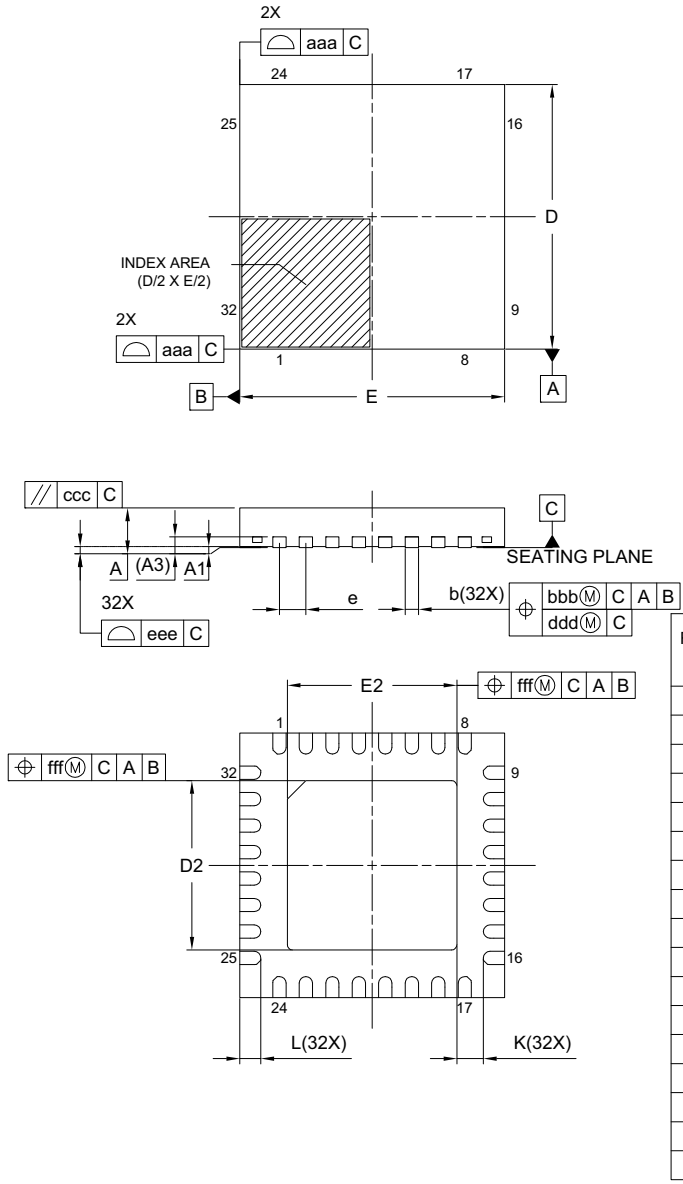
<R>

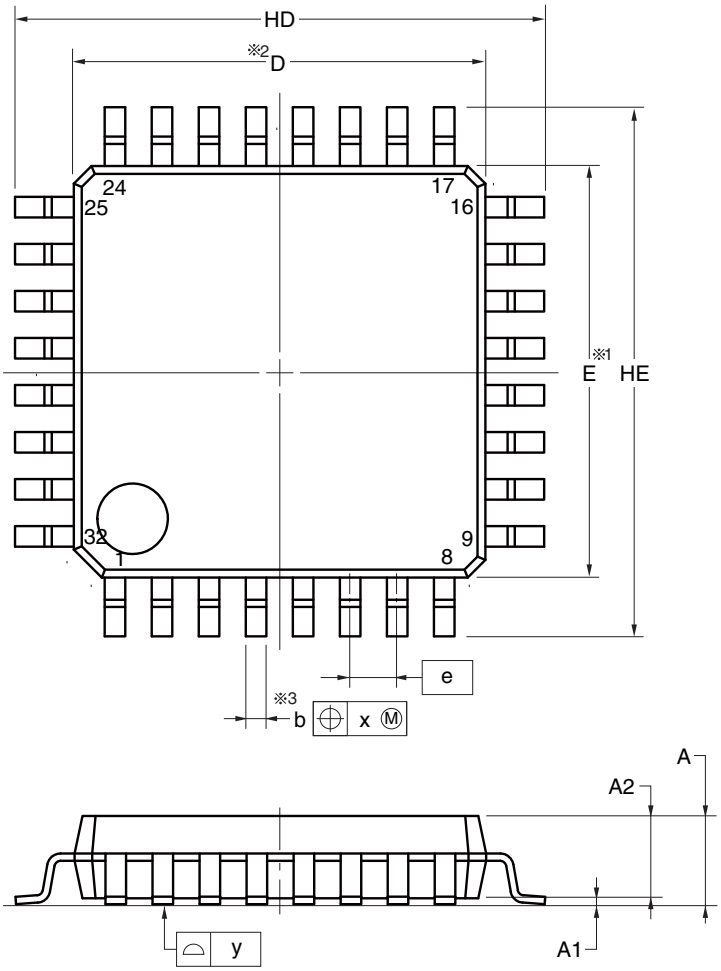
| JEITA Package code | RENESAS code | MASS(TYP.)[g] |
|---|---|---|
| P-HWQFN032-5x5-0.50 | PWQN0032KE-A | 0.06 |

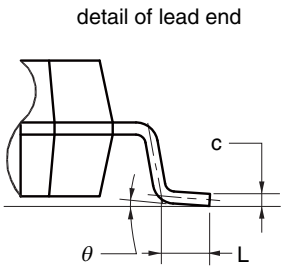



| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min. | Nom. | Max. |
| A | — | — | 0.80 |
| $A_1$ | 0.00 | 0.02 | 0.05 |
| $A_3$ | | 0.203 REF. | |
| b | 0.18 | 0.25 | 0.30 |
| D | | 5.00 BSC | |
| E | | 5.00 BSC | |
| e | | 0.50 BSC | |
| L | 0.35 | 0.40 | 0.45 |
| K | 0.20 | — | — |
| $D_2$ | 3.15 | 3.20 | 3.25 |
| $E_2$ | 3.15 | 3.20 | 3.25 |
| aaa | | 0.15 | |
| bbb | | 0.10 | |
| ccc | | 0.10 | |
| ddd | | 0.05 | |
| eee | | 0.08 | |
| fff | | 0.10 | |

<R>

| JEITA Package Code | RENESAS Code | Previous Code | MASS (TYP.) [g] |
|---|---|---|---|
| P-LQFP32-7x7-0.80 | PLQP0032GB-A | P32GA-80-GBT-1 | 0.2 |




(UNIT:mm)

| ITEM | DIMENSIONS |
|---|---|
| D | 7.00±0.10 |
| E | 7.00±0.10 |
| HD | 9.00±0.20 |
| HE | 9.00±0.20 |
| A | 1.70 MAX. |
| A1 | 0.10±0.10 |
| A2 | 1.40 |
| b | 0.37±0.05 |
| c | 0.145±0.055 |
| L | 0.50±0.20 |
| θ | 0° to 8° |
| e | 0.80 |
| x | 0.20 |
| y | 0.10 |

**NOTE**

1.Dimensions "※1" and "※2" do not include mold flash.

2.Dimension "※3" does not include trim offset.

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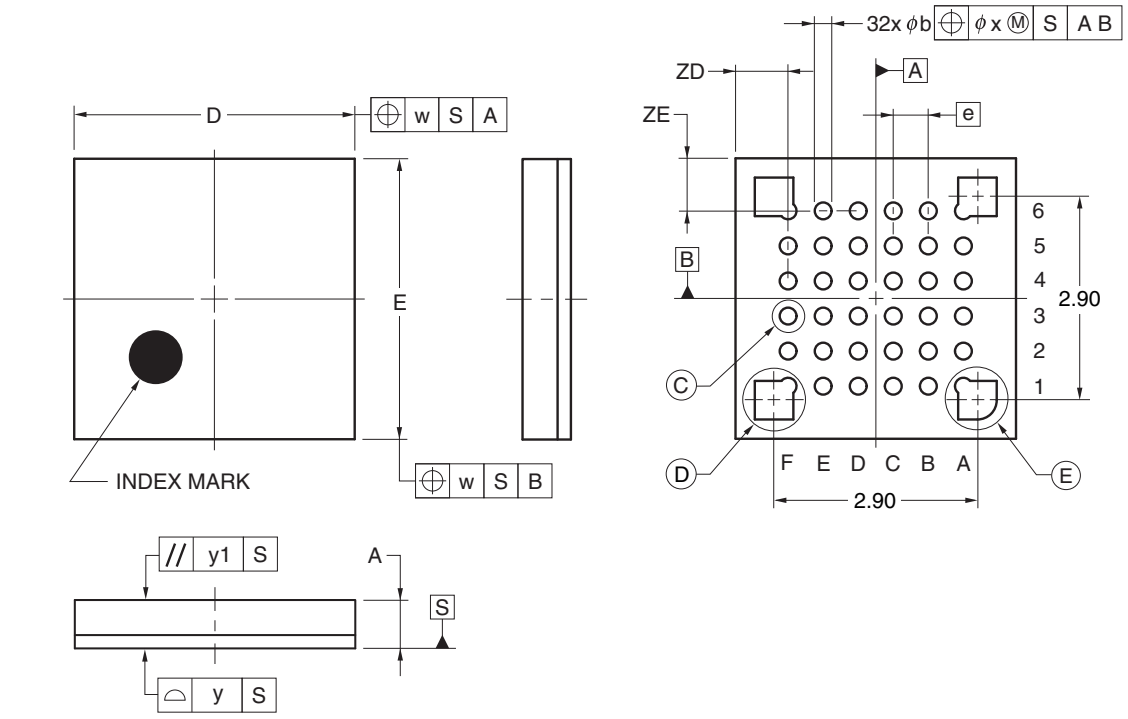
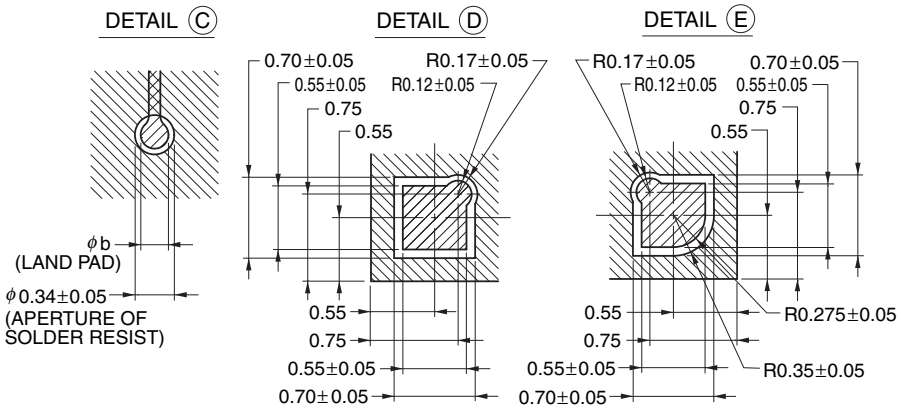
## <R> 4.3 36-pin Package

| JEITA Package Code | RENESAS Code | Previous Code | MASS (TYP.) [g] |
|---|---|---|---|
| P-WFLGA36-4x4-0.50 | PWLG0036KA-A | P36FC-50-AA4-2 | 0.023 |




(UNIT:mm)

| ITEM | DIMENSIONS |
|---|---|
| D | 4.00±0.10 |
| E | 4.00±0.10 |
| w | 0.20 |
| e | 0.50 |
| A | 0.69±0.07 |
| b | 0.24±0.05 |
| x | 0.05 |
| y | 0.08 |
| y1 | 0.20 |
| ZD | 0.75 |
| ZE | 0.75 |

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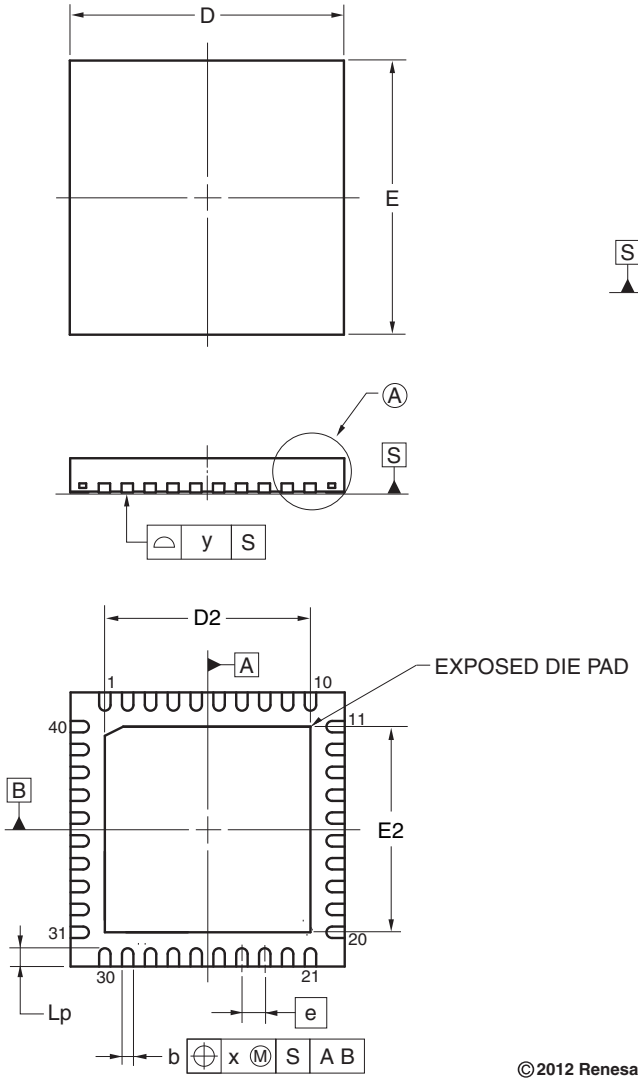
## <R> 4.4 40-pin Package

| JEITA Package Code | RENESAS Code | Previous Code | MASS (TYP.) [g] |
|---|---|---|---|
| P-HWQFN40-6x6-0.50 | PWQN0040KC-A | P40K8-50-4B4-4 | 0.09 |




| Referance Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 5.95 | 6.00 | 6.05 |
| E | 5.95 | 6.00 | 6.05 |
| A | 0.70 | 0.75 | 0.80 |
| b | 0.18 | 0.25 | 0.30 |
| e | — | 0.50 | — |
| Lp | 0.30 | 0.40 | 0.50 |
| x | — | — | 0.05 |
| y | — | — | 0.05 |

| ITEM | | D2 | | | E2 | | |
|---|---|---|---|---|---|---|---|
| | | MIN | NOM | MAX | MIN | NOM | MAX |
| EXPOSED DIE PAD VARIATIONS | A | 4.45 | 4.50 | 4.55 | 4.45 | 4.50 | 4.55 |

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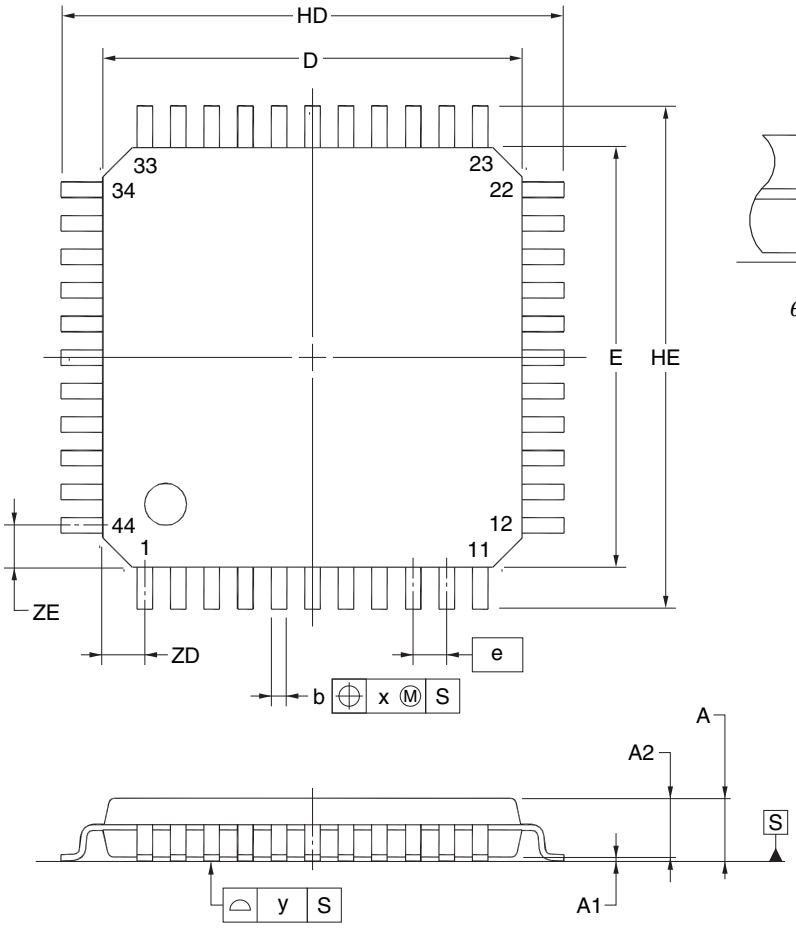
## <R> 4.5 44-pin Package

| JEITA Package Code | RENESAS Code | Previous Code | MASS (TYP.) [g] |
|---|---|---|---|
| P-LQFP44-10x10-0.80 | PLQP0044GC-A | P44GB-80-UES-2 | 0.36 |




(UNIT:mm)

| ITEM | DIMENSIONS |
|---|---|
| D | 10.00±0.20 |
| E | 10.00±0.20 |
| HD | 12.00±0.20 |
| HE | 12.00±0.20 |
| A | 1.60 MAX. |
| A1 | 0.10±0.05 |
| A2 | 1.40±0.05 |
| A3 | 0.25 |
| b | $0.37^{+0.08}_{-0.07}$ |
| c | $0.145^{+0.055}_{-0.045}$ |
| L | 0.50 |
| Lp | 0.60±0.15 |
| L1 | 1.00±0.20 |
| θ | $3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$ |
| e | 0.80 |
| x | 0.20 |
| y | 0.10 |
| ZD | 1.00 |
| ZE | 1.00 |

**NOTE**
Each lead centerline is located within 0.20 mm of its true position at maximum material condition.

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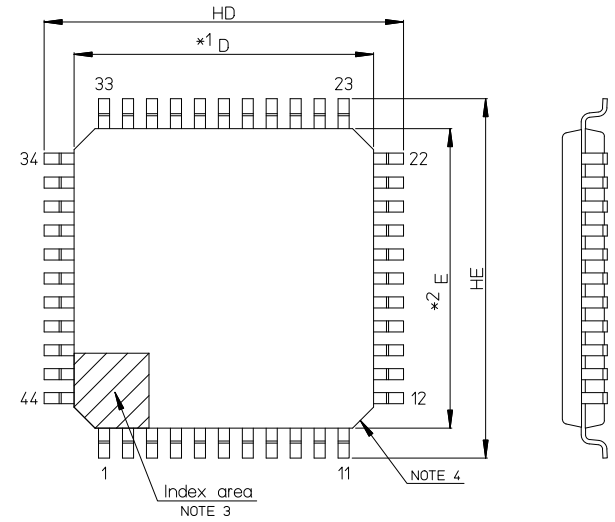
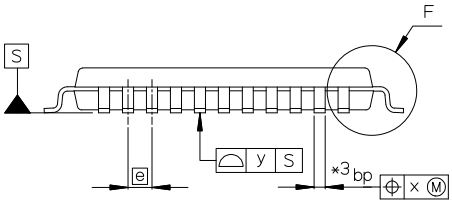
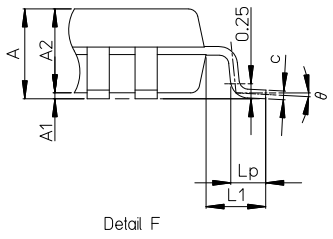
<R>

| JEITA Package Code | RENESAS Code | Previous Code | MASS[Typ.] |
|---|---|---|---|
| P-LQFP44-10x10-0.80 | PLQP0044GC-D | —— | 0.36g |




NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

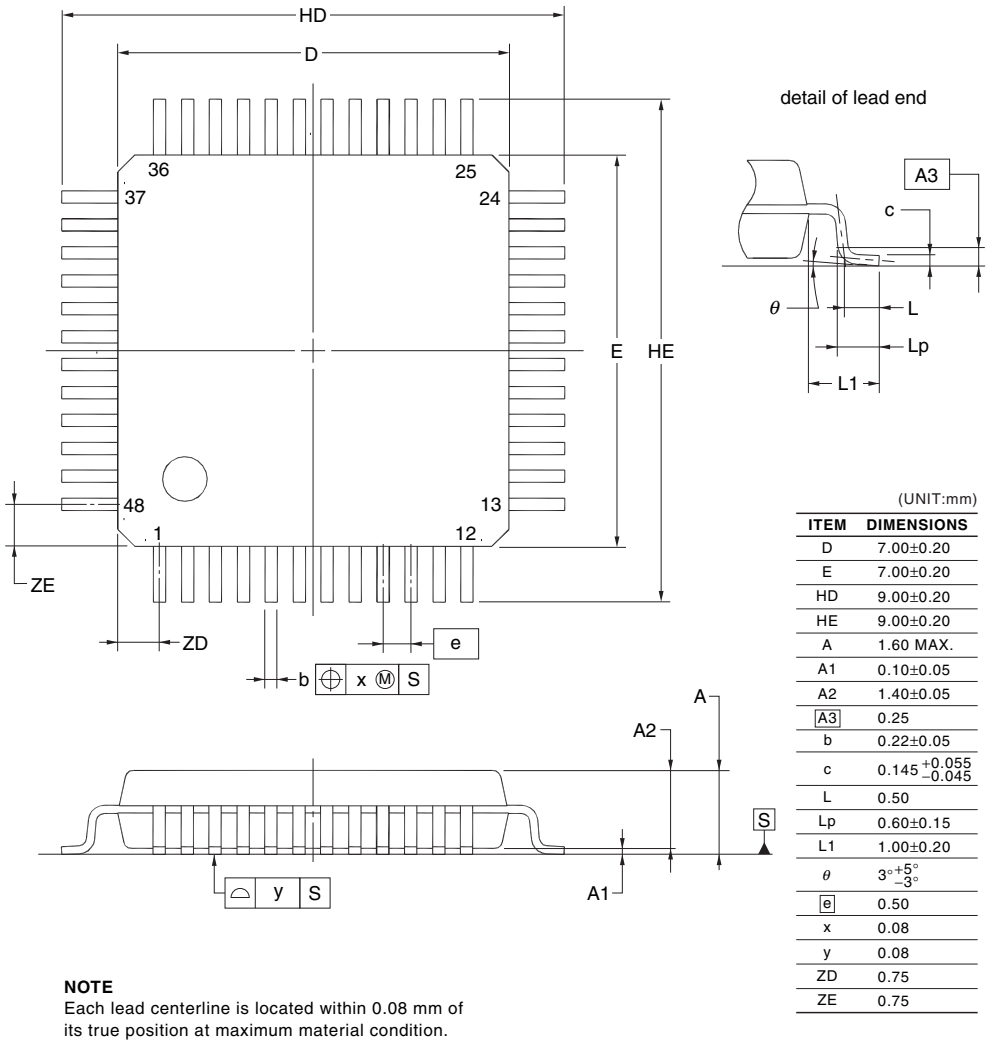



Detail F

| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 9.8 | 10.0 | 10.2 |
| E | 9.8 | 10.0 | 10.2 |
| A2 | —— | 1.4 | —— |
| HD | 11.8 | 12.0 | 12.2 |
| HE | 11.8 | 12.0 | 12.2 |
| A | —— | —— | 1.6 |
| A1 | 0.05 | —— | 0.15 |
| bp | 0.22 | 0.37 | 0.45 |
| c | 0.09 | —— | 0.20 |
| θ | 0° | 3.5° | 8° |
| e | —— | 0.80 | —— |
| x | —— | —— | 0.20 |
| y | —— | —— | 0.10 |
| Lp | 0.45 | 0.6 | 0.75 |
| L1 | —— | 1.0 | —— |

## <R> 4.6 48-pin Package

| JEITA Package Code | RENESAS Code | Previous Code | MASS (TYP.) [g] |
|---|---|---|---|
| P-LFQFP48-7x7-0.50 | PLQP0048KF-A | P48GA-50-8EU-1 | 0.16 |




(UNIT:mm)

| ITEM | DIMENSIONS |
|---|---|
| D | 7.00±0.20 |
| E | 7.00±0.20 |
| HD | 9.00±0.20 |
| HE | 9.00±0.20 |
| A | 1.60 MAX. |
| A1 | 0.10±0.05 |
| A2 | 1.40±0.05 |
| A3 | 0.25 |
| b | 0.22±0.05 |
| c | $0.145^{+0.055}_{-0.045}$ |
| L | 0.50 |
| Lp | 0.60±0.15 |
| L1 | 1.00±0.20 |
| θ | $3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$ |
| e | 0.50 |
| x | 0.08 |
| y | 0.08 |
| ZD | 0.75 |
| ZE | 0.75 |

**NOTE**
Each lead centerline is located within 0.08 mm of its true position at maximum material condition.

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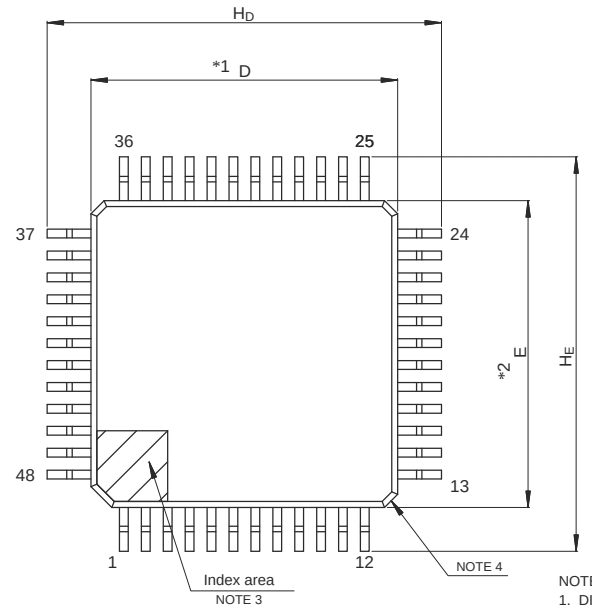
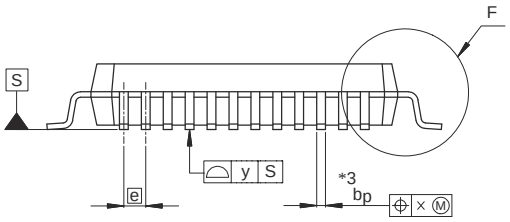
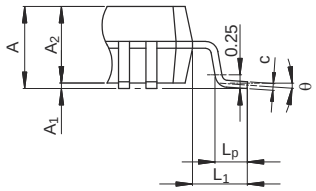
<R>

| JEITA Package Code | RENESAS Code | Previous Code | MASS (Typ) [g] |
|---|---|---|---|
| P-LFQFP48-7x7-0.50 | PLQP0048KB-B | — | 0.2 |

Unit: mm




Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

| Reference Symbol | Dimensions in millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 6.9 | 7.0 | 7.1 |
| E | 6.9 | 7.0 | 7.1 |
| $A_2$ | — | 1.4 | — |
| $H_D$ | 8.8 | 9.0 | 9.2 |
| $H_E$ | 8.8 | 9.0 | 9.2 |
| A | — | — | 1.7 |
| $A_1$ | 0.05 | — | 0.15 |
| $b_p$ | 0.17 | 0.20 | 0.27 |
| c | 0.09 | — | 0.20 |
| θ | 0° | 3.5° | 8° |
| e | — | 0.5 | — |
| x | — | — | 0.08 |
| y | — | — | 0.08 |
| $L_p$ | 0.45 | 0.6 | 0.75 |
| $L_1$ | — | 1.0 | — |

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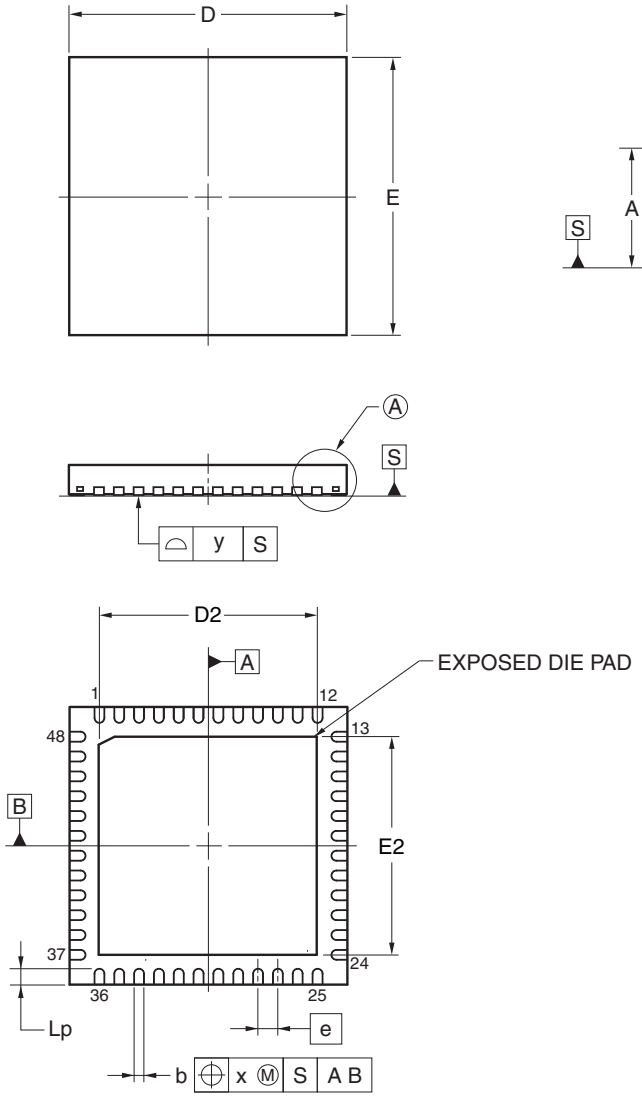
<R>

| JEITA Package Code | RENESAS Code | Previous Code | MASS (TYP.) [g] |
|---|---|---|---|
| P-HWQFN48-7x7-0.50 | PWQN0048KB-A | 48PJN-A<br>P48K8-50-5B4-5 | 0.13 |




| Referance Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 6.95 | 7.00 | 7.05 |
| E | 6.95 | 7.00 | 7.05 |
| A | 0.70 | 0.75 | 0.80 |
| b | 0.18 | 0.25 | 0.30 |
| e | — | 0.50 | — |
| Lp | 0.30 | 0.40 | 0.50 |
| x | — | — | 0.05 |
| y | — | — | 0.05 |

| ITEM | | D2 | | | E2 | | |
|---|---|---|---|---|---|---|---|
| | | MIN | NOM | MAX | MIN | NOM | MAX |
| EXPOSED DIE PAD VARIATIONS | A | 5.45 | 5.50 | 5.55 | 5.45 | 5.50 | 5.55 |

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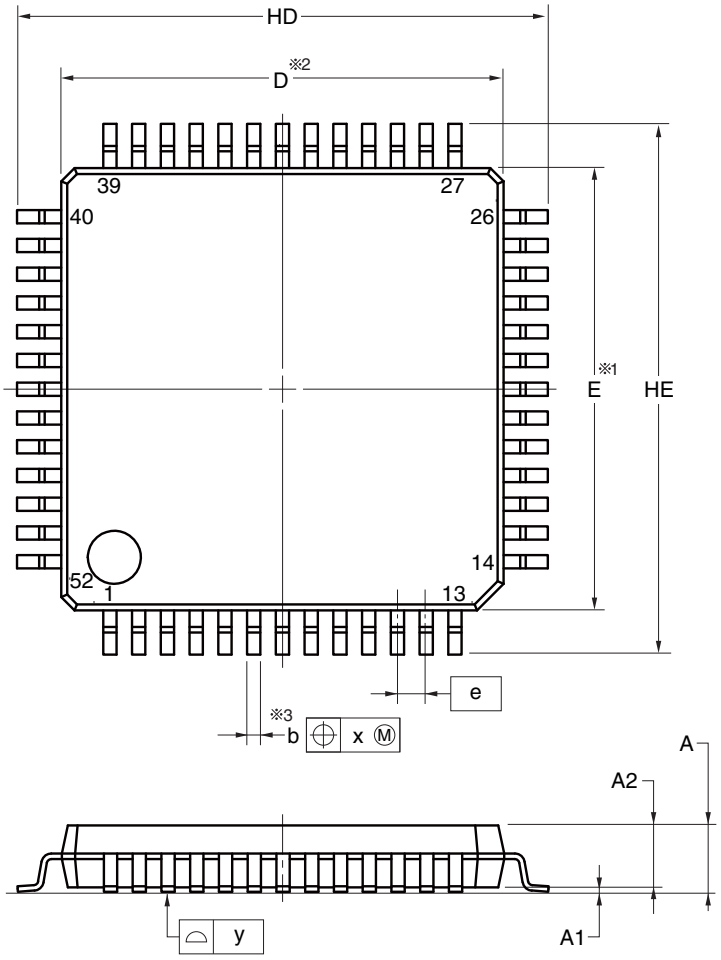
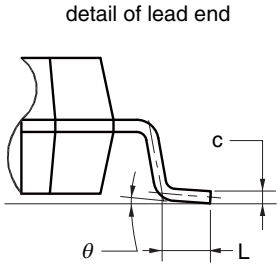
## <R> 4.7 52-pin Package

| JEITA Package Code | RENESAS Code | Previous Code | MASS (TYP.) [g] |
|---|---|---|---|
| P-LQFP52-10x10-0.65 | PLQP0052JA-A | P52GB-65-GBS-1 | 0.3 |




(UNIT:mm)

| ITEM | DIMENSIONS |
|---|---|
| D | 10.00±0.10 |
| E | 10.00±0.10 |
| HD | 12.00±0.20 |
| HE | 12.00±0.20 |
| A | 1.70 MAX. |
| A1 | 0.10±0.05 |
| A2 | 1.40 |
| b | 0.32±0.05 |
| c | 0.145±0.055 |
| L | 0.50±0.15 |
| θ | 0° to 8° |
| e | 0.65 |
| x | 0.13 |
| y | 0.10 |

**NOTE**

1.Dimensions "※1" and "※2" do not include mold flash.

2.Dimension "※3" does not include trim offset.

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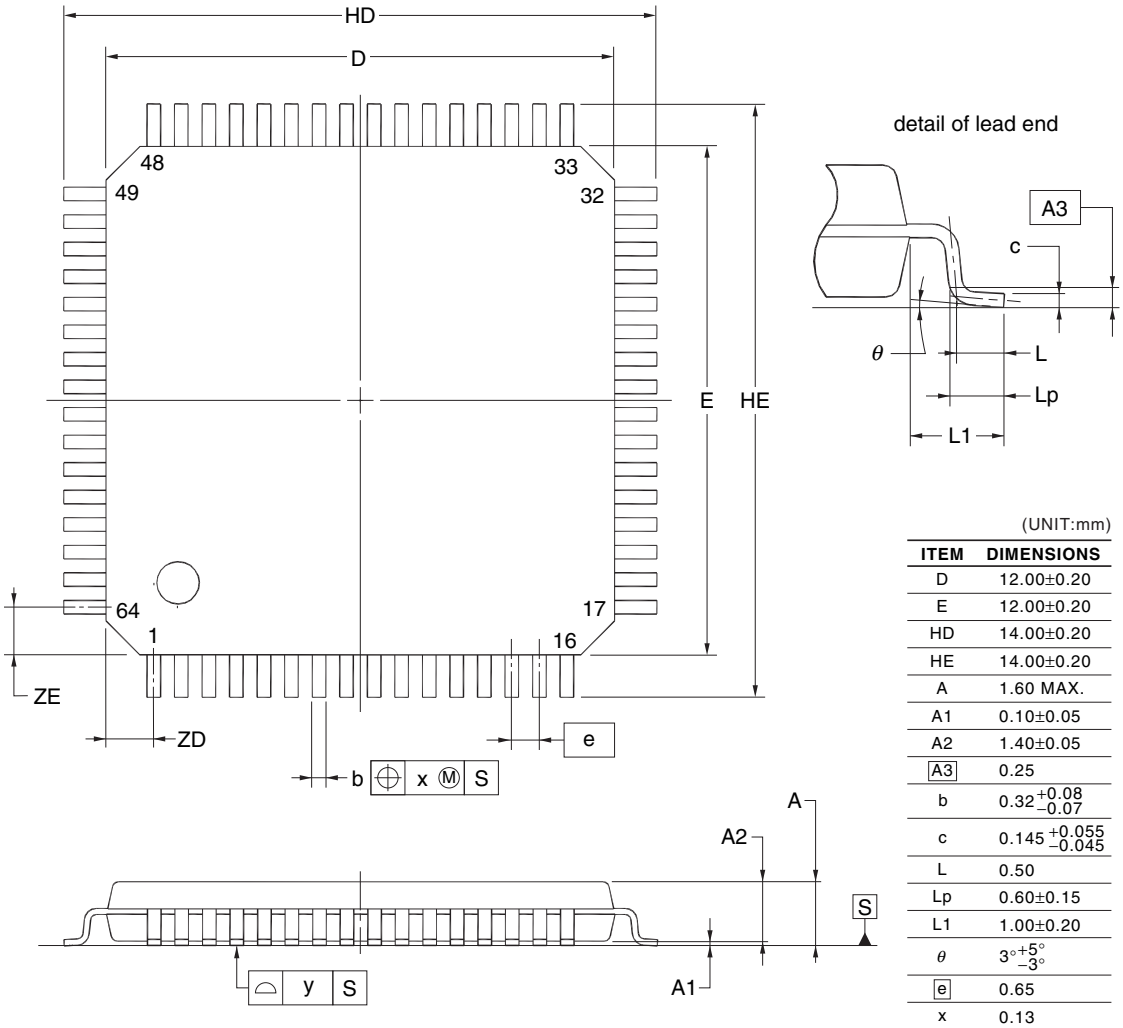
## <R> 4.8 64-pin Package

| JEITA Package Code | RENESAS Code | Previous Code | MASS (TYP.) [g] |
|---|---|---|---|
| P-LQFP64-12x12-0.65 | PLQP0064JA-A | P64GK-65-UET-2 | 0.51 |




(UNIT:mm)

| ITEM | DIMENSIONS |
|---|---|
| D | 12.00±0.20 |
| E | 12.00±0.20 |
| HD | 14.00±0.20 |
| HE | 14.00±0.20 |
| A | 1.60 MAX. |
| A1 | 0.10±0.05 |
| A2 | 1.40±0.05 |
| A3 | 0.25 |
| b | $0.32^{+0.08}_{-0.07}$ |
| c | $0.145^{+0.055}_{-0.045}$ |
| L | 0.50 |
| Lp | 0.60±0.15 |
| L1 | 1.00±0.20 |
| θ | $3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$ |
| e | 0.65 |
| x | 0.13 |
| y | 0.10 |
| ZD | 1.125 |
| ZE | 1.125 |

**NOTE**
Each lead centerline is located within 0.13 mm of its true position at maximum material condition.

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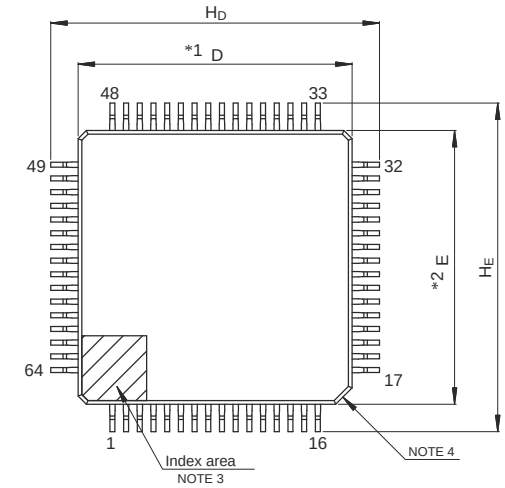
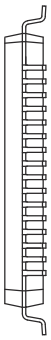
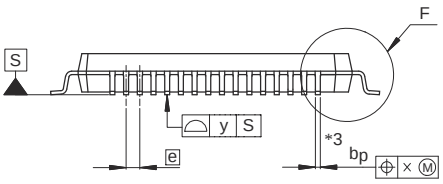
<R>

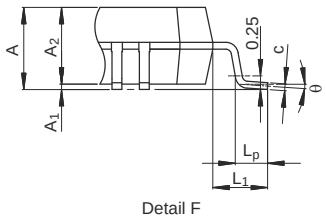
| JEITA Package Code | RENESAS Code | Previous Code | MASS (Typ) [g] |
|---|---|---|---|
| P-LFQFP64-10x10-0.50 | PLQP0064KB-C | — | 0.3 |

Unit: mm






Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

| Reference Symbol | Dimensions in millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 9.9 | 10.0 | 10.1 |
| E | 9.9 | 10.0 | 10.1 |
| $A_2$ | — | 1.4 | — |
| $H_D$ | 11.8 | 12.0 | 12.2 |
| $H_E$ | 11.8 | 12.0 | 12.2 |
| A | — | — | 1.7 |
| $A_1$ | 0.05 | — | 0.15 |
| $b_p$ | 0.15 | 0.20 | 0.27 |
| c | 0.09 | — | 0.20 |
| θ | 0° | 3.5° | 8° |
| e | — | 0.5 | — |
| x | — | — | 0.08 |
| y | — | — | 0.08 |
| $L_p$ | 0.45 | 0.6 | 0.75 |
| $L_1$ | — | 1.0 | — |

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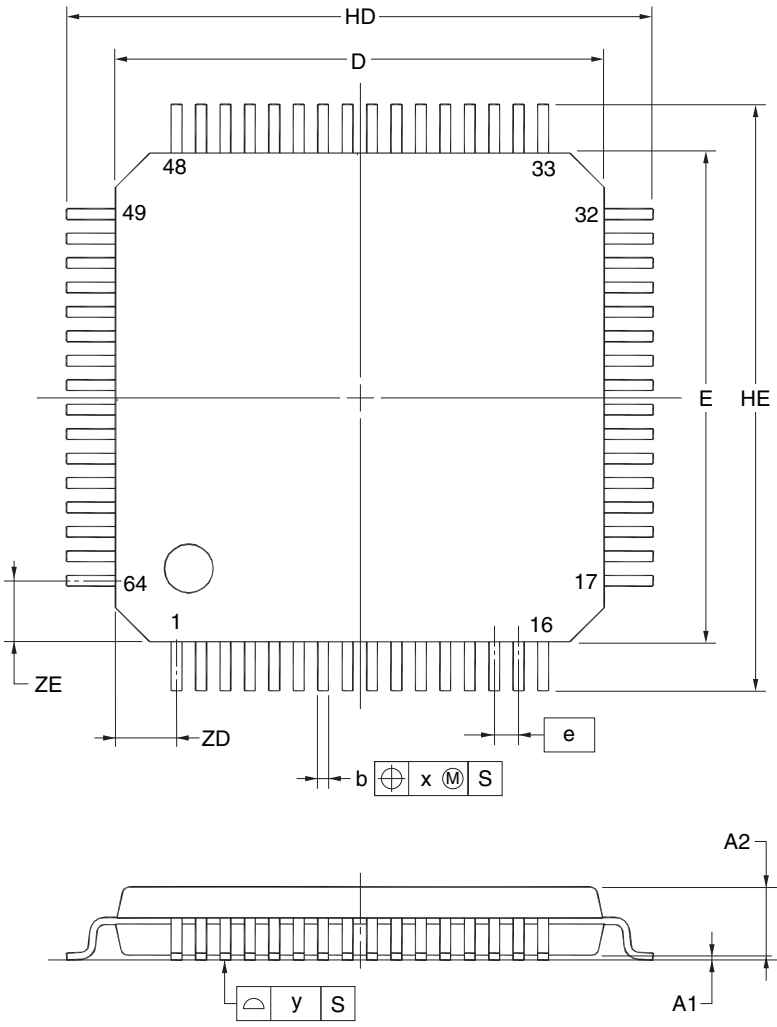
<R>

| JEITA Package Code | RENESAS Code | Previous Code | MASS (TYP.) [g] |
|---|---|---|---|
| P-LFQFP64-10x10-0.50 | PLQP0064KF-A | P64GB-50-UEU-2 | 0.35 |




(UNIT:mm)

| ITEM | DIMENSIONS |
|---|---|
| D | 10.00±0.20 |
| E | 10.00±0.20 |
| HD | 12.00±0.20 |
| HE | 12.00±0.20 |
| A | 1.60 MAX. |
| A1 | 0.10±0.05 |
| A2 | 1.40±0.05 |
| A3 | 0.25 |
| b | 0.22±0.05 |
| c | $0.145^{+0.055}_{-0.045}$ |
| L | 0.50 |
| Lp | 0.60±0.15 |
| L1 | 1.00±0.20 |
| θ | $3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$ |
| e | 0.50 |
| x | 0.08 |
| y | 0.08 |
| ZD | 1.25 |
| ZE | 1.25 |

**NOTE**
Each lead centerline is located within 0.08 mm of its true position at maximum material condition.

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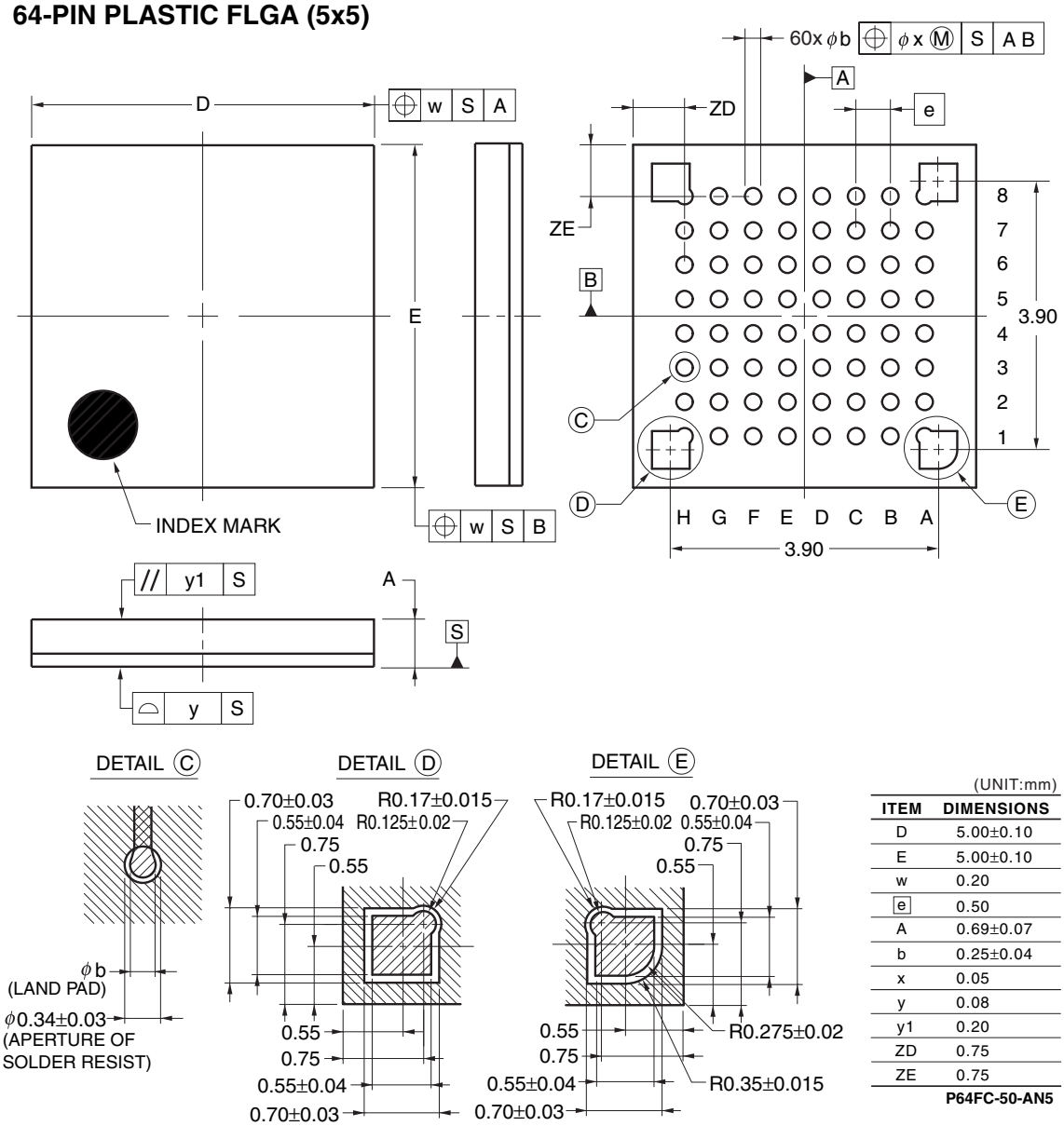
<R>

| JEITA Package Code | RENESAS Code | Previous Code | MASS (TYP.) [g] |
|---|---|---|---|
| P-WFLGA64-5x5-0.50 | PWLG0064KA-A | P64FC-50-AN5 | 0.037 |

## 64-PIN PLASTIC FLGA (5x5)




(UNIT:mm)

| ITEM | DIMENSIONS |
|---|---|
| D | 5.00±0.10 |
| E | 5.00±0.10 |
| w | 0.20 |
| e | 0.50 |
| A | 0.69±0.07 |
| b | 0.25±0.04 |
| x | 0.05 |
| y | 0.08 |
| y1 | 0.20 |
| ZD | 0.75 |
| ZE | 0.75 |

P64FC-50-AN5

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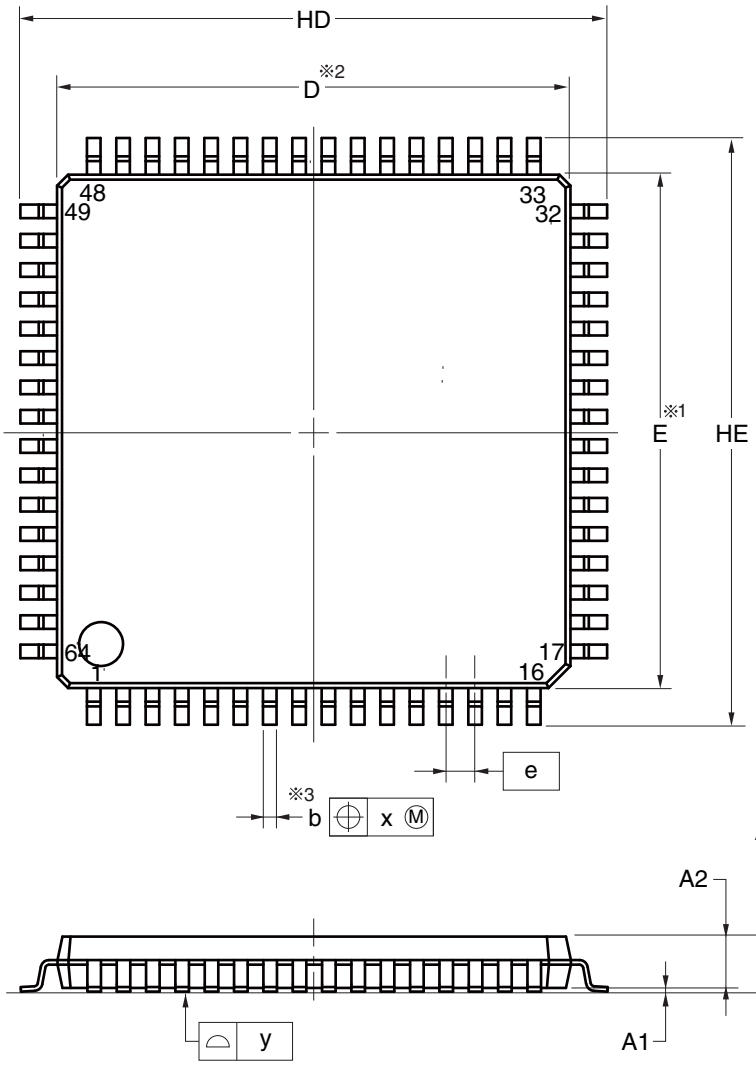
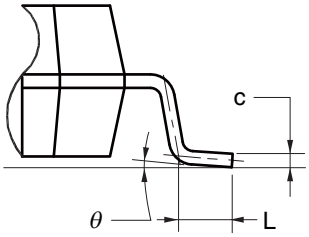
<R>

| JEITA Package Code | RENESAS Code | Previous Code | MASS (TYP.) [g] |
|---|---|---|---|
| P-LQFP64-14x14-0.80 | PLQP0064GA-A | P64GC-80-GBW-1 | 0.7 |




detail of lead end




(UNIT:mm)

| ITEM | DIMENSIONS |
|---|---|
| D | 14.00±0.10 |
| E | 14.00±0.10 |
| HD | 16.00±0.20 |
| HE | 16.00±0.20 |
| A | 1.70 MAX. |
| A1 | 0.10±0.10 |
| A2 | 1.40 |
| b | $0.37^{+0.08}_{-0.05}$ |
| c | $0.125^{+0.05}_{-0.02}$ |
| L | 0.50±0.20 |
| θ | 0° to 8° |
| e | 0.80 |
| x | 0.20 |
| y | 0.10 |

**NOTE**

1.Dimensions "※1" and "※2" do not include mold flash.

2.Dimension "※3" does not include trim offset.

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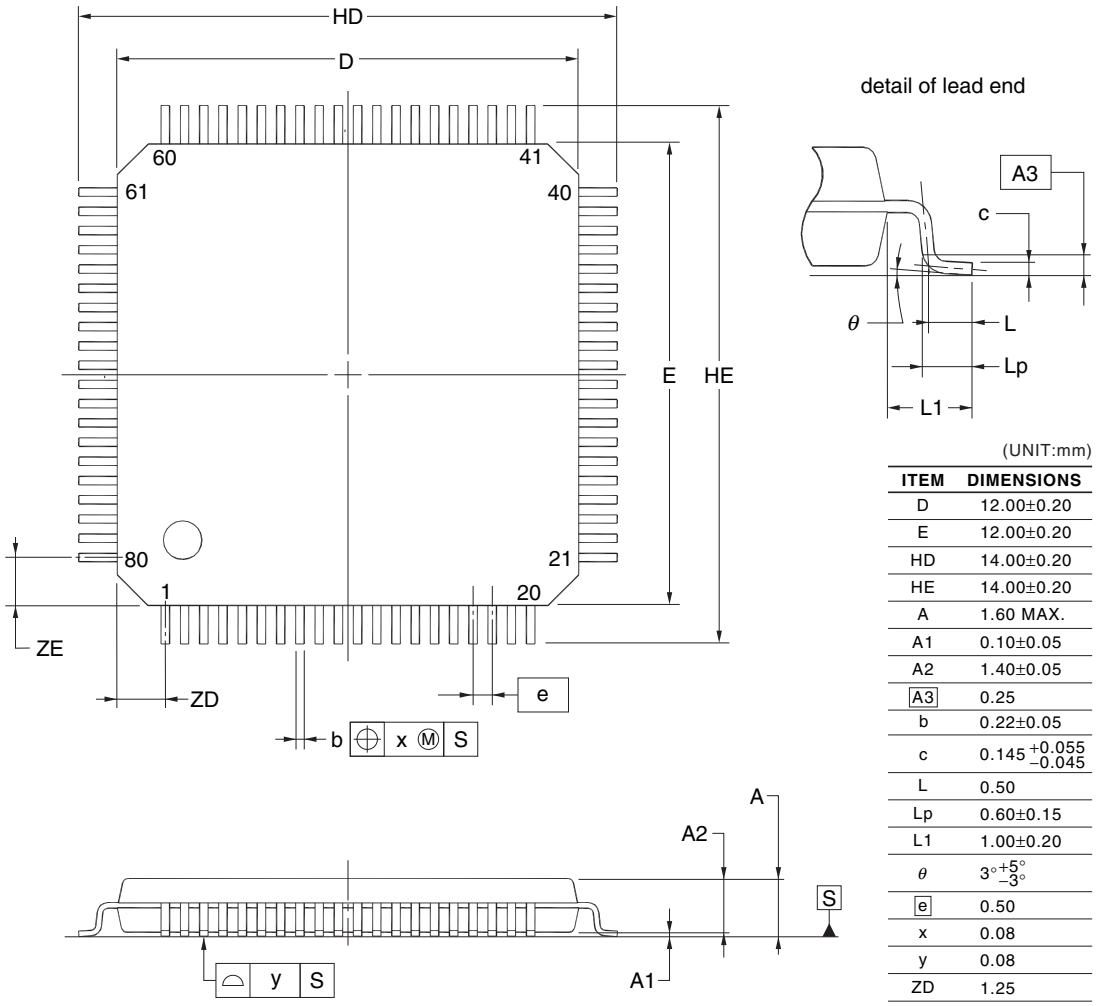
## <R> 4.9 80-pin Package

| JEITA Package Code | RENESAS Code | Previous Code | MASS (TYP.) [g] |
|---|---|---|---|
| P-LFQFP80-12x12-0.50 | PLQP0080KE-A | P80GK-50-8EU-2 | 0.53 |




(UNIT:mm)

| ITEM | DIMENSIONS |
|---|---|
| D | 12.00±0.20 |
| E | 12.00±0.20 |
| HD | 14.00±0.20 |
| HE | 14.00±0.20 |
| A | 1.60 MAX. |
| A1 | 0.10±0.05 |
| A2 | 1.40±0.05 |
| A3 | 0.25 |
| b | 0.22±0.05 |
| c | $0.145^{+0.055}_{-0.045}$ |
| L | 0.50 |
| Lp | 0.60±0.15 |
| L1 | 1.00±0.20 |
| θ | $3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$ |
| e | 0.50 |
| x | 0.08 |
| y | 0.08 |
| ZD | 1.25 |
| ZE | 1.25 |

**NOTE**
Each lead centerline is located within 0.08 mm of its true position at maximum material condition.

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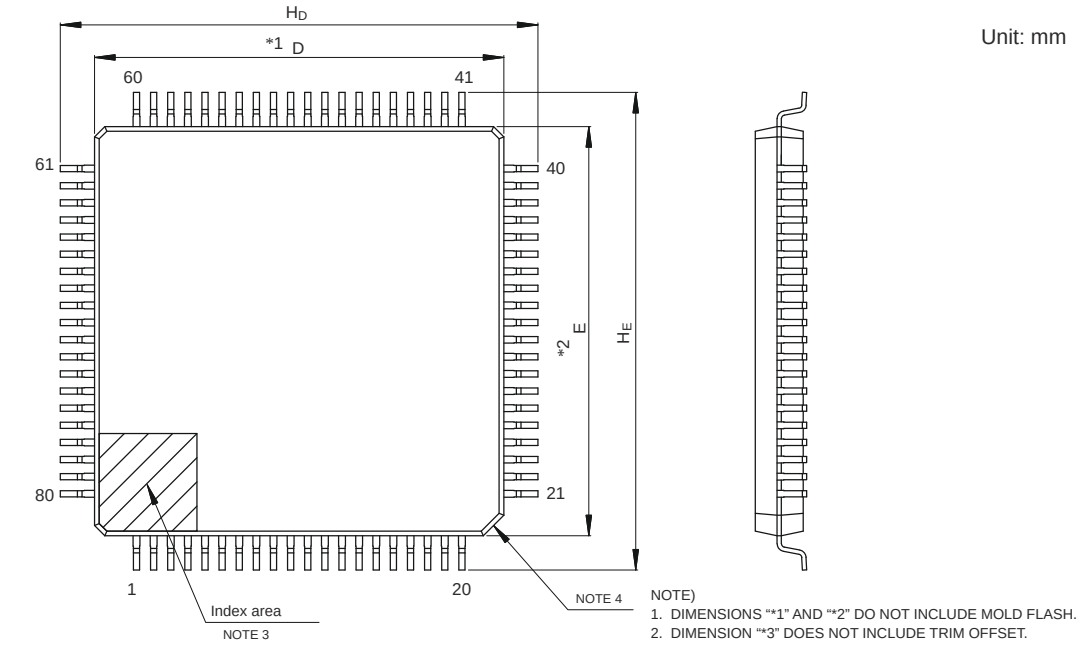
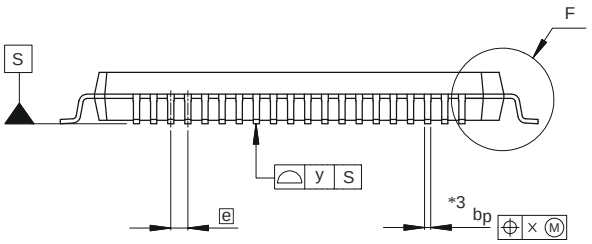
<R>

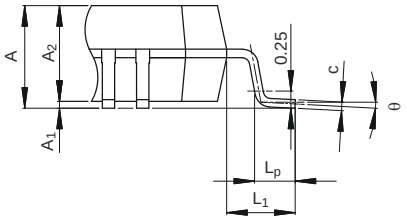
| JEITA Package Code | RENESAS Code | Previous Code | MASS (Typ) [g] |
|---|---|---|---|
| P-LFQFP80-12x12-0.50 | PLQP0080KB-B | — | 0.5 |

Unit: mm




NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.




Detail F

| Reference Symbol | Dimensions in millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 11.9 | 12.0 | 12.1 |
| E | 11.9 | 12.0 | 12.1 |
| $A_2$ | — | 1.4 | — |
| $H_D$ | 13.8 | 14.0 | 14.2 |
| $H_E$ | 13.8 | 14.0 | 14.2 |
| A | — | — | 1.7 |
| $A_1$ | 0.05 | — | 0.15 |
| $b_p$ | 0.15 | 0.20 | 0.27 |
| c | 0.09 | — | 0.20 |
| θ | 0° | 3.5° | 8° |
| e | — | 0.5 | — |
| x | — | — | 0.08 |
| y | — | — | 0.08 |
| $L_p$ | 0.45 | 0.6 | 0.75 |
| $L_1$ | — | 1.0 | — |

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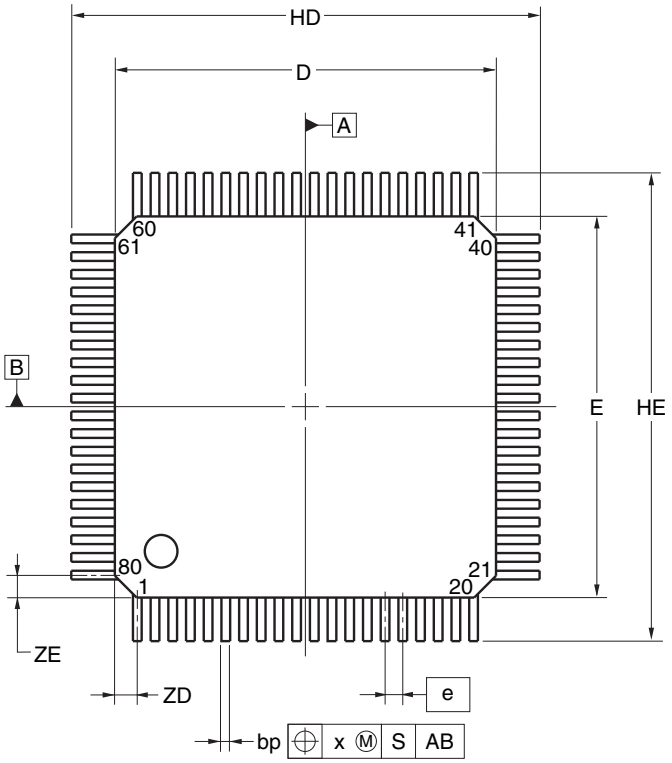
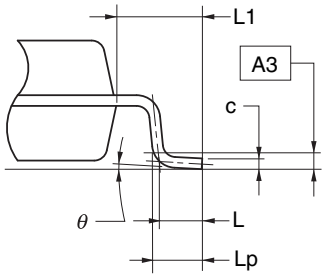
<R>

| JEITA Package Code | RENESAS Code | Previous Code | MASS (TYP.) [g] |
|---|---|---|---|
| P-LQFP80-14x14-0.65 | PLQP0080JB-E | P80GC-65-UBT-2 | 0.69 |




detail of lead end




| Referance Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 13.80 | 14.00 | 14.20 |
| E | 13.80 | 14.00 | 14.20 |
| HD | 17.00 | 17.20 | 17.40 |
| HE | 17.00 | 17.20 | 17.40 |
| A | — | — | 1.70 |
| A1 | 0.05 | 0.125 | 0.20 |
| A2 | 1.35 | 1.40 | 1.45 |
| A3 | — | 0.25 | — |
| bp | 0.26 | 0.32 | 0.38 |
| c | 0.10 | 0.145 | 0.20 |
| L | — | 0.80 | — |
| Lp | 0.736 | 0.886 | 1.036 |
| L1 | 1.40 | 1.60 | 1.80 |
| θ | 0° | 3° | 8° |
| e | — | 0.65 | — |
| x | — | — | 0.13 |
| y | — | — | 0.10 |
| ZD | — | 0.825 | — |
| ZE | — | 0.825 | — |

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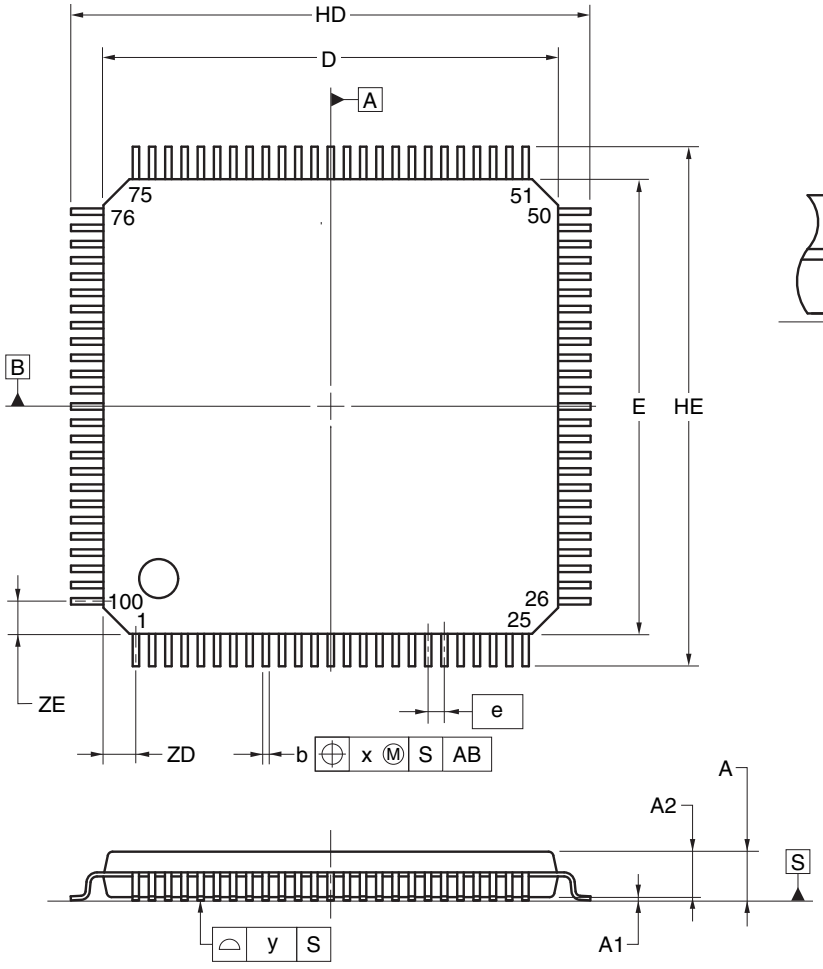
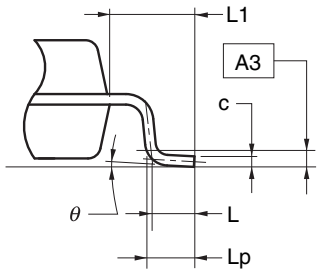
## <R> 4.10 100-pin Package

| JEITA Package Code | RENESAS Code | Previous Code | MASS (TYP.) [g] |
|---|---|---|---|
| P-LFQFP100-14x14-0.50 | PLQP0100KE-A | P100GC-50-GBR-1 | 0.69 |




detail of lead end




(UNIT:mm)

| ITEM | DIMENSIONS |
|---|---|
| D | 14.00±0.20 |
| E | 14.00±0.20 |
| HD | 16.00±0.20 |
| HE | 16.00±0.20 |
| A | 1.60 MAX. |
| A1 | 0.10±0.05 |
| A2 | 1.40±0.05 |
| A3 | 0.25 |
| b | 0.22±0.05 |
| c | $0.145^{+0.055}_{-0.045}$ |
| L | 0.50 |
| Lp | 0.60±0.15 |
| L1 | 1.00±0.20 |
| θ | $3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$ |
| e | 0.50 |
| x | 0.08 |
| y | 0.08 |
| ZD | 1.00 |
| ZE | 1.00 |

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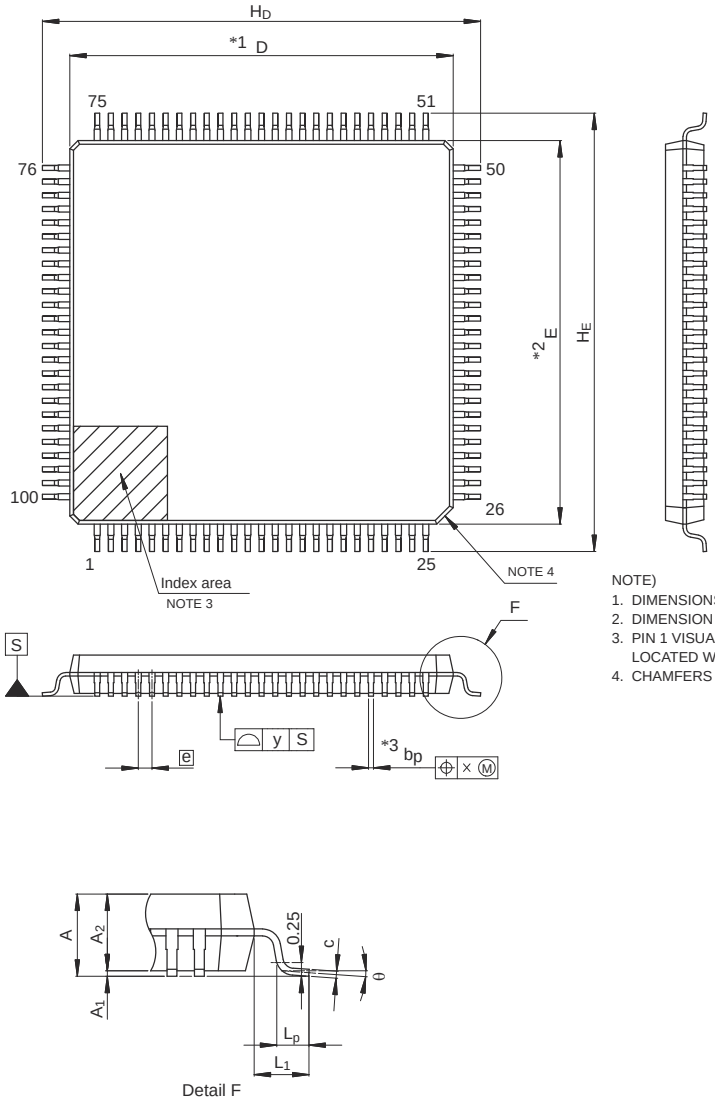
<R>

| JEITA Package Code | RENESAS Code | Previous Code | MASS (Typ) [g] |
|---|---|---|---|
| P-LFQFP100-14x14-0.50 | PLQP0100KB-B | — | 0.6 |

Unit: mm




NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

| Reference Symbol | Dimensions in millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 13.9 | 14.0 | 14.1 |
| E | 13.9 | 14.0 | 14.1 |
| $A_2$ | — | 1.4 | — |
| $H_D$ | 15.8 | 16.0 | 16.2 |
| $H_E$ | 15.8 | 16.0 | 16.2 |
| A | — | — | 1.7 |
| $A_1$ | 0.05 | — | 0.15 |
| $b_p$ | 0.15 | 0.20 | 0.27 |
| c | 0.09 | — | 0.20 |
| θ | 0° | 3.5° | 8° |
| e | — | 0.5 | — |
| x | — | — | 0.08 |
| y | — | — | 0.08 |
| $L_p$ | 0.45 | 0.6 | 0.75 |
| $L_1$ | — | 1.0 | — |

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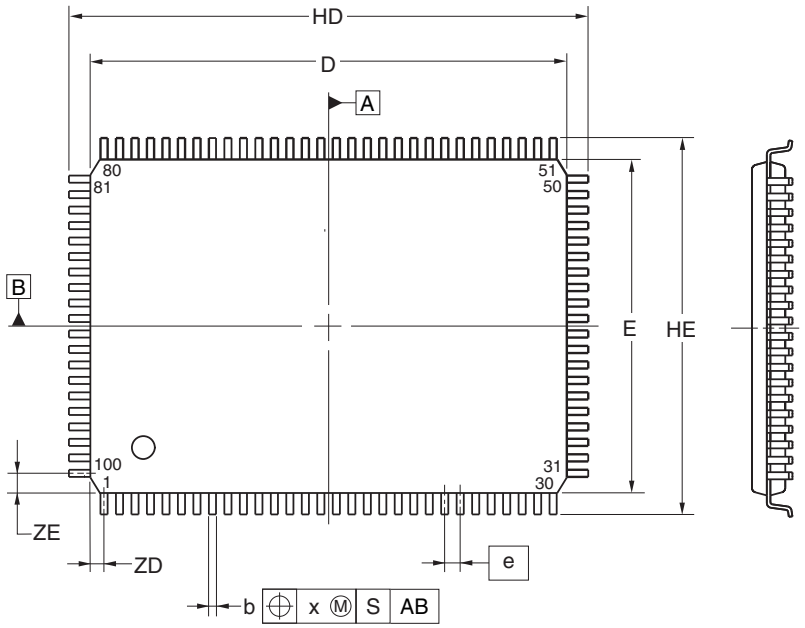
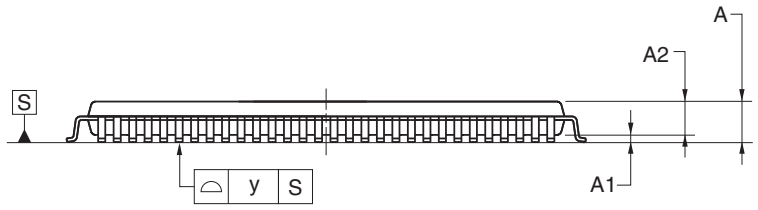
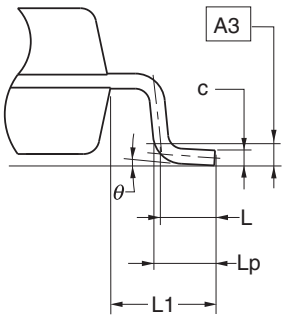
<R>

| JEITA Package Code | RENESAS Code | Previous Code | MASS (TYP.) [g] |
|---|---|---|---|
| P-LQFP100-14x20-0.65 | PLQP0100JC-A | P100GF-65-GBN-1 | 0.92 |




detail of lead end




(UNIT:mm)

| ITEM | DIMENSIONS |
|---|---|
| D | 20.00±0.20 |
| E | 14.00±0.20 |
| HD | 22.00±0.20 |
| HE | 16.00±0.20 |
| A | 1.60 MAX. |
| A1 | 0.10±0.05 |
| A2 | 1.40±0.05 |
| A3 | 0.25 |
| b | $0.32^{+0.08}_{-0.07}$ |
| c | $0.145^{+0.055}_{-0.045}$ |
| L | 0.50 |
| Lp | 0.60±0.15 |
| L1 | 1.00±0.20 |
| θ | $3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$ |
| e | 0.65 |
| x | 0.13 |
| y | 0.10 |
| ZD | 0.575 |
| ZE | 0.825 |

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| REVISION HISTORY | RL78/G14 Datasheet |
|---|---|

| Rev. | Date | Description | |
|---|---|---|---|
| | | Page | Summary |
| 0.01 | Feb 10, 2011 | — | First Edition issued |
| 0.02 | May 01, 2011 | 1 to 2 | 1.1 Features revised |
| | | 3 | 1.2 Ordering Information revised |
| | | 4 to 13 | 1.3 Pin Configuration (Top View) revised |
| | | 14 | 1.4 Pin Identification revised |
| | | 15 to 17 | 1.5.1 30-pin products to 1.5.3 36-pin products revised |
| | | 23 to 26 | 1.6 Outline of Functions revised |
| 0.03 | Jul 28, 2011 | 1 | 1.1 Features revised |
| 1.00 | Feb 21, 2012 | 1 to 40 | 1. OUTLINE revised |
| | | 41 to 97 | 2. ELECTRICAL SPECIFICATIONS added |
| 2.00 | Oct 25, 2013 | 1 | Modification of 1.1 Features |
| | | 3 to 8 | Modification of 1.2 Ordering Information |
| | | 9 to 22 | Modification of package type in 1.3 Pin Configuration (Top View) |
| | | 34 to 43 | Modification of description of subsystem clock in 1.6 Outline of Functions |
| | | 34 to 43 | Modification of description of timer output in 1.6 Outline of Functions |
| | | 34 to 43 | Modification of error of data transfer controller in 1.6 Outline of Functions |
| | | 34 to 43 | Modification of error of event link controller in 1.6 Outline of Functions |
| | | 45, 46 | Modification of description of Tables in 2.1 Absolute Maximum Ratings |
| | | 47 | Modification of Tables, notes, cautions, and remarks in 2.2 Oscillator Characteristics |
| | | 48 | Modification of error of conditions of high level input voltage in 2.3.1 Pin characteristics |
| | | 49 | Modification of error of conditions of low level output voltage in 2.3.1 Pin characteristics |
| | | 53 to 62 | Modification of Notes and Remarks in 2.3.2 Supply current characteristics |
| | | 65, 66 | Addition of Minimum Instruction Execution Time during Main System Clock Operation |
| | | 67 to 69 | Addition of AC Timing Test Points |
| | | 70 to 97 | Addition of LS mode and LV mode characteristics in 2.5.1 Serial array unit |
| | | 98 to 101 | Addition of LS mode and LV mode characteristics in 2.5.2 Serial interface IICA |
| | | 102 to 105 | Addition of characteristics about conversion of internal reference voltage and temperature sensor in 2.6.1 A/D converter characteristics |
| | | 107 | Addition of characteristic in 2.6.4 Comparator |
| | | 107 | Deletion of detection delay in 2.6.5 POR circuit characteristics |
| | | 109 | Modification of 2.6.7 Power supply voltage rising slope characteristics |
| | | 110 | Modification of 2.7 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics |
| | | 110 | Addition of characteristic in 2.8 Flash Memory Programming Characteristics |
| | | 111 | Addition of description in 2.10 Timing for Switching Flash Memory Programming Modes |

| REVISION HISTORY | RL78/G14 Datasheet |
|---|---|

| Rev. | Date | Description | |
|---|---|---|---|
| | | Page | Summary |
| 2.00 | Oct 25, 2013 | 112 to 169 | Addition of CHAPTER 3 ELECTRICAL SPECIFICATIONS |
| | | 171 to 187 | Modification of 4.1 30-pin products to 4.10 100-pin products |
| 3.00 | Feb 07, 2014 | All | Addition of products with maximum 512 KB flash ROM and 48 KB RAM |
| | | 1 | Modification of 1.1 Features |
| | | 2 | Modification of ROM, RAM capacities and addition of note 3 |
| | | 3 | Modification of Figure 1 - 1 Part Number, Memory Size, and Package of RL78/G14 |
| | | 6 to 8 | Addition of part number |
| | | 15, 16 | Modification of 1.3.6 48-pin products |
| | | 17 | Modification of 1.3.7 52-pin products |
| | | 18, 19 | Modification of 1.3.8 64-pin products |
| | | 20 | Modification of 1.3.9 80-pin products |
| | | 21, 22 | Modification of 1.3.10 100-pin products |
| | | 35, 37, 39, 41, 43, 45, 47 | Modification of operating ambient temperature in 1.6 Outline of Functions |
| | | 42, 43 | Addition of table of 48-pin, 52-pin, 64-pin products (code flash memory 384 KB to 512 KB) |
| | | 46, 47 | Addition of table of 80-pin, 100-pin products (code flash memory 384 KB to 512 KB) |
| | | 65 to 68 | Addition of (3) Flash ROM: 384 to 512 KB of 48- to 100-pin products |
| | | 118 | Modification of 2.7 Data Memory Retention Characteristics |
| | | 137 to 140 | Addition of (3) Flash ROM: 384 to 512 KB of 48- to 100-pin products |
| | | 180 | Modification of 3.7 Data Memory Retention Characteristics |
| | | 189, 190 | Addition and modification of 4.6 48-pin products |
| | | 191 | Modification of 4.7 52-pin products |
| | | 193 to 195 | Addition and modification of 4.8 64-pin products |
| | | 198, 199 | Addition and modification of 4.9 80-pin products |
| | | 201, 202 | Addition and modification of 4.10 100-pin products |
| 3.20 | Jan 05, 2015 | 2 | Deletion of R5F104JK and R5F104JL from the list of ROM and RAM capacities and modification of note |
| | | 6 | Deletion of ordering part numbers of R5F104JK and R5F104JL from 52-pin plastic LQFP package in 1.2 Ordering Information |
| | | 6 to 8 | Deletion of note 2 in 1.2 Ordering Information |
| | | 17 | Deletion of note 2 in 1.3.7 52-pin products |
| | | 36, 39, 42, 45, 48, 50, 52 | Modification of description in 1.6 Outline of Functions |
| | | 46, 48 | Deletion of description of 52-pin in 1.6 Outline of Functions |
| | | 47 | Modification of note of 1.6 Outline of Functions |
| | | 62, 64, 66, 68, 70, 72 | Modification of specifications in 2.3.2 Supply current characteristics |

| REVISION HISTORY | RL78/G14 Datasheet |
|---|---|

| Rev. | Date | Description | |
|---|---|---|---|
| | | Page | Summary |
| 3.20 | Jan 05, 2015 | 135, 137, 139, 141, 143, 145 | Modification of specifications in 3.3.2 Supply current characteristics |
| | | 197 | Modification of part number in 4.7 52-pin products |
| 3.30 | Aug 12, 2016 | 143, 145 | Addition of maximum values in (3) Flash ROM: 384 to 512 KB of 48- to 100-pin products of 3.3.2 Supply current characteristics |
| 3.31 | Feb 14, 2020 | 3 | Addition of packaging specifications in Figure 1 - 1 Part Number, Memory Size, and Package of RL78/G14 |
| | | 4 to 15 | Addition of ordering part numbers and RENESAS codes in Table 1 - 1 List of Ordering Part Numbers |
| | | 195, 196, 198 to 201, 203, 205 to 207, 209 to 212, 214, 215, 217 | Modification of the titles of the subchapters and deletion of product names in Chapter 4 |
| | | 197 | Addition of figure in 4.2 32-pin Package |
| | | 202 | Addition of figure in 4.5 44-pin Package |
| | | 204 | Modification of figure in 4.6 48-pin Package |
| | | 208 | Modification of figure in 4.8 64-pin Package |
| | | 213 | Modification of figure in 4.9 80-pin Package |
| | | 216 | Modification of figure in 4.10 100-pin Package |

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# General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between $V_{IL}$ (Max.) and $V_{IH}$ (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between $V_{IL}$ (Max.) and $V_{IH}$ (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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R5F104LDALA#W0 R5F104LKAFA#30 R5F104JGGFA#30 R5F104LEAFA#V0

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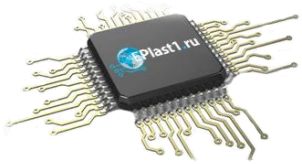


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