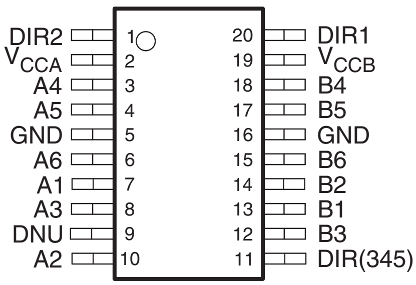
AUDIO CODEC AC'97 VOLTAGE-TRANSLATION TRANSCEIVER

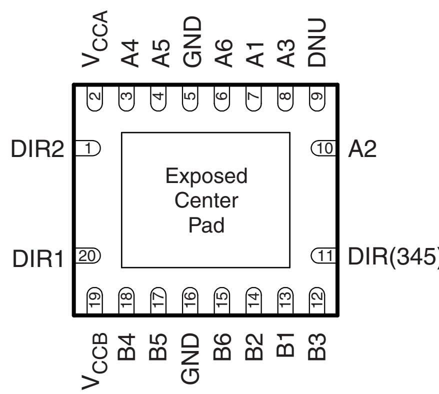
FEATURES

- **Voltage-Level Transceiver for Interfacing 1.8 V Audio Codec (AC'97) Controllers With 3.3 V AC'97 Codec Links**
- **Configurable I/O Switching Levels With Dual-Supply Pins Operating Over Full 1.2-V to 3.6-V Power-Supply Range**
- **For Low-Power Operation, A and B Ports Are Placed in High-Impedance State When Either Supply Voltage Is Switched Off**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **7000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1500-V Charged-Device Model (C101)**

PW PACKAGE
(TOP VIEW)

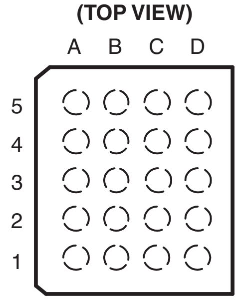


RGY PACKAGE
(BOTTOM VIEW)



The exposed center pad, if used, must be connected as a secondary ground or left electrically open.

ZXY PACKAGE
(TOP VIEW)



TERMINAL ASSIGNMENTS
(20-Ball ZXY Package)

	A	B	C	D
5	V_{CCA}	DIR2	DIR1	V_{CCB}
4	A5	A4	B4	B5
3	A6	GND	GND	B6
2	A3	A1	B2	B1
1	DNU(1)	A2	DIR(345)	B3

(1) DNU – Do not use; should be left unconnected

DESCRIPTION/ORDERING INFORMATION

The SN74AVC6T622 is a voltage-level transceiver for interfacing 1.8 V audio codec (AC'97) controllers, the audio/analog modem functionality found in personal computers, with 3.3V AC'97 codec links. With the digital switching levels of today's AC'97 codecs lowering to 1.8-V logic levels, the SN74AVC6T622 device can be used to bridge the gap between legacy 3.3-V AC'97 codecs and AC'97 controllers that are now operating at 1.8 V. The 6-bit wide SN74AVC6T622 device complies with the AC'97 electrical interface (both levels and timing) specification.

Two supply-voltage pins allow the A-port and B-port input switching thresholds to be configured separately. The A port is designed to track V_{CCA}, while the B port is designed to track V_{CCB}. V_{CCA} and V_{CCB} can accept any supply voltage from 1.2 V to 3.6 V.

If either V_{CC} is switched off (V_{CCA} = 0 V and/or V_{CCB} = 0 V), all outputs are placed in the high-impedance state to conserve power.

The SN74AVC6T622 is available in two 0.5-mm-pitch ball grid array (BGA) packages. The 20-ball package has dimensions of 3 mm × 2.5 mm, and the 24-ball package measures 3 mm × 3 mm. Memory cards are widely used in mobile phones, PDAs, digital cameras, personal media players, camcorders, set-top boxes, etc. Low static power consumption and small package size make the SN74AVC6T622 an ideal choice for these applications.

ORDERING INFORMATION

T_A	PACKAGE(1)(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QFN – RGY	Reel of 1000	SN74AVC6T622RGYR	WU622
	TSSOP – PW	Reel of 2000	SN74AVC6T622PWR	WU622
	UFBGA – ZXY (Pb-Free)	Reel of 2500	SN74AVC6T622ZXYR	WU622

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

REFERENCE DESIGN

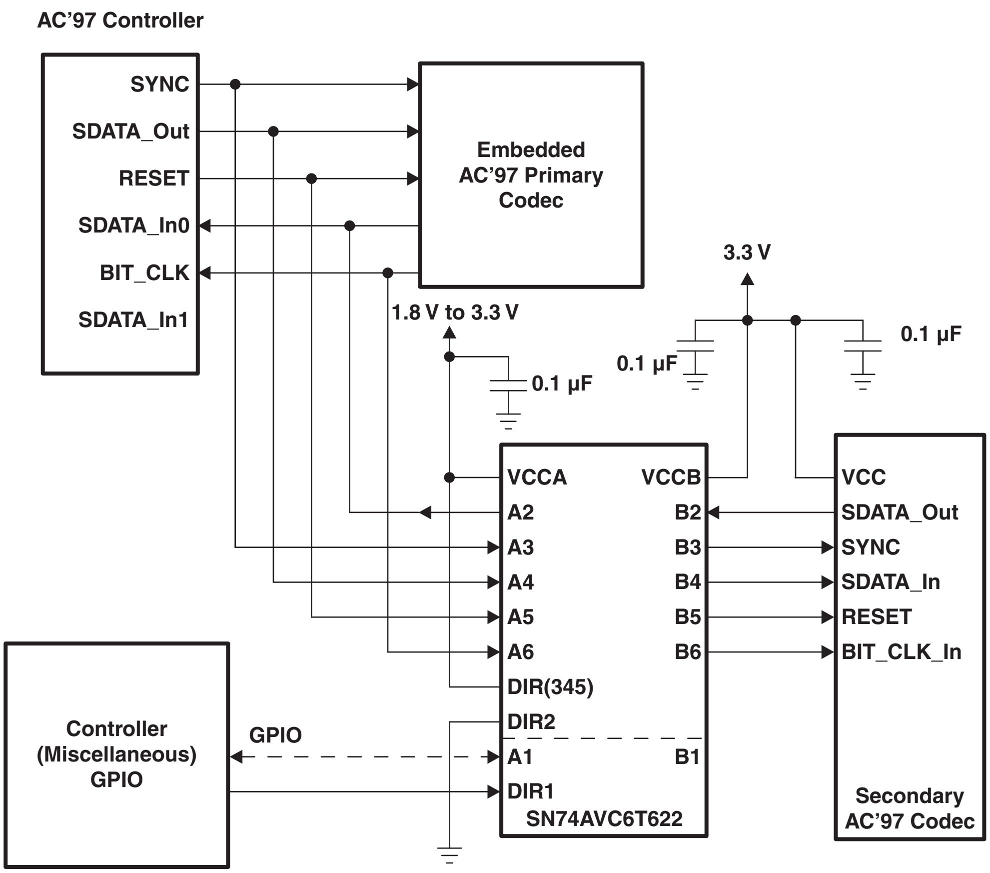


Figure 1. Interfacing 1.8 V AC'97 Controllers With 3.3 V AC'97 Controllers

TERMINAL FUNCTIONS

ZXY BALL NO.	RGY, PW PIN NO.	NAME	TYPE	DESCRIPTION
A1	9	DNU		Do not use; leave unconnected
A2	8	A3	I	AC'97 controller SYNC signal
A3	6	A6	I	AC'97 controller BIT_CLK signal
A4	4	A5	I	AC'97 controller RESET signal
A5	2	V_{CCA}	Pwr	A-port supply voltage. V_{CCA} powers all A-port I/Os and control pins.
B1	10	A2	O	AC'97 controller SDATA_In0 signal
B2	7	A1	I/O	GPIO to miscellaneous GPIO controller
B3, C3	5, 16	GND	–	Ground
B4	3	A4	I	AC'97 controller SDATA_Out signal
B5	1	DIR2	–	Should be tied to GND
C1	11	DIR(345)	–	Should be tied to V_{CCA}
C2	14	B2	I	Secondary AC'97 codec SDATA_Out signal
C4	18	B4	O	Secondary AC'97 codec SDATA_In signal
C5	20	DIR1	I	Direction control from miscellaneous GPIO controller
D1	12	B3	O	Secondary AC'97 codec SYNC signal
D2	13	B1	O	Optional GPIO signal if A1 is enabled
D3	15	B6	O	Secondary AC'97 codec BIT_CLK_In signal
D4	17	B5	O	Secondary AC'97 codec RESET signal
D5	19	V_{CCB}	Pwr	B-port supply voltage. V_{CCB} powers all B-port I/Os and control pins.

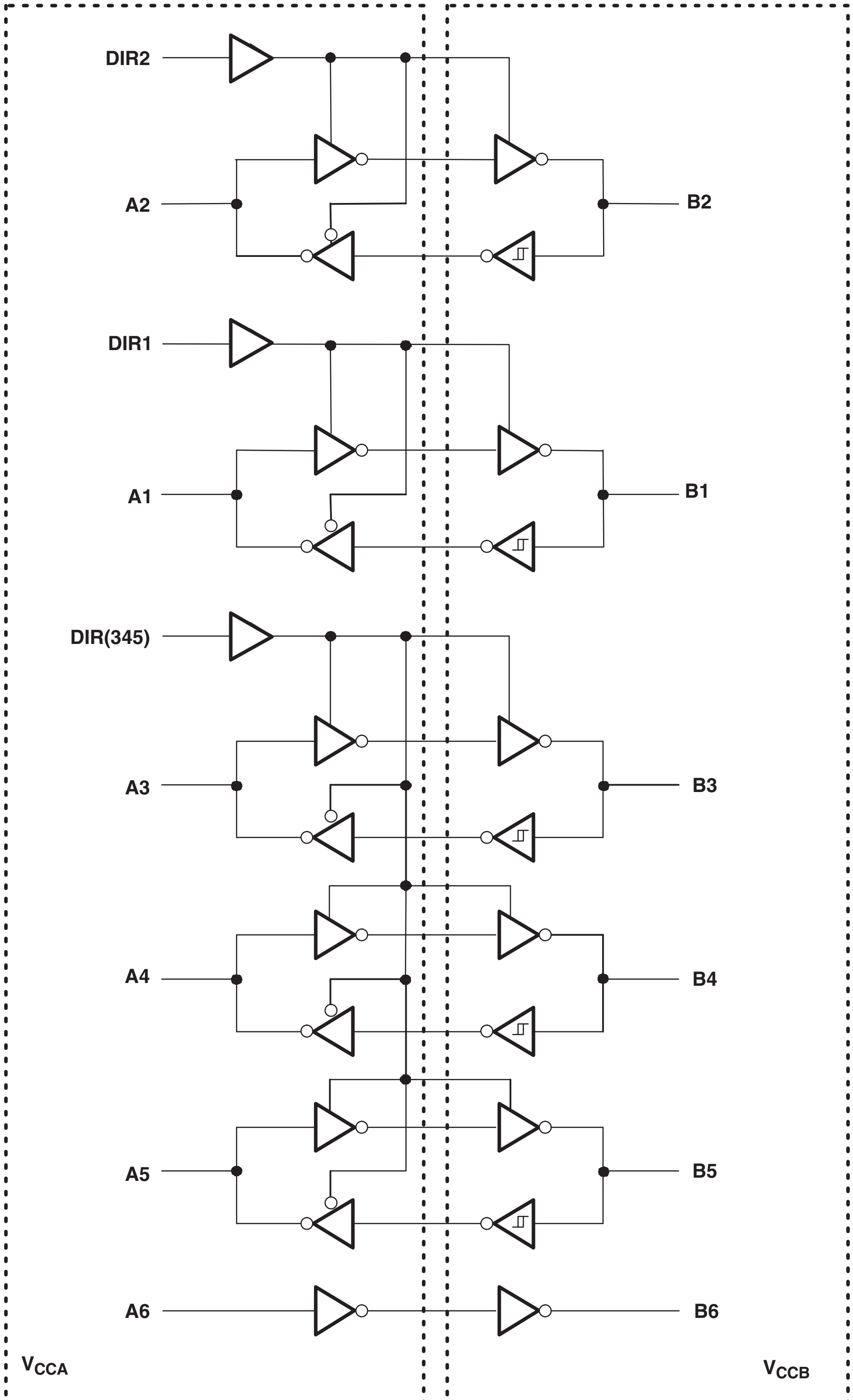
FUNCTION TABLES

CONTROL INPUT DIR2	OUTPUT CIRCUITS		OPERATION
	A2	B2	
High	Hi-Z	Enabled	A2 to B2
Low	Enabled	Hi-Z	B2 to A2

CONTROL INPUT DIR1	OUTPUT CIRCUITS		FUNCTION
	A1	B1	
High	Hi-Z	Enabled	A1 to B1
Low	Enabled	Hi-Z	B1 to A1

CONTROL INPUT DIR(345)	OUTPUT CIRCUITS		FUNCTION
	A3, A4, A5	B3, B4, B5	
High	Hi-Z	Enabled	A3 to B3
			A4 to B4
			A5 to B5
Low	Enabled	Hi-Z	B3 to A3
			B4 to A4
			B5 to A5

LOGIC DIAGRAM (POSITIVE LOGIC)



ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CCA} V_{CCB}	Supply voltage range		–0.5	4.6	V
V_I	Input voltage range(2)	I/O ports (A port)	–0.5	4.6	V
		I/O ports (B port)	–0.5	4.6	
		Control inputs	–0.5	4.6	
V_O	Voltage range applied to any output in the high-impedance or power-off state(2)	A port	–0.5	4.6	V
		B port	–0.5	4.6	
V_O	Voltage range applied to any output in the high or low state(2)(3)	A port	–0.5	V_{CCA} + 0.5	V
		B port	–0.5	V_{CCB} + 0.5	
I_{IK}	Input clamp current	V_I < 0		–50	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CCA}, V_{CCB}, or GND			±100	mA
θ_{JA}	Package thermal impedance	PW package(4)		83	°C/W
		RGY package(5)		37	
		ZXY package(4)		193	
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input voltage and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The output positive-voltage rating may be exceeded up to 4.6 V maximum if the output current rating is observed.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.
(5) The package thermal impedance is calculated in accordance with JESD 51-5.

RECOMMENDED OPERATING CONDITIONS[1][2][3]

			V_{CCI}	V_{CCO}	MIN	MAX	UNIT
V_{CCA}	Supply voltage				1.2	3.6	V
V_{CCB}	Supply voltage				1.2	3.6	V
V_{IH}	High-level input voltage	All inputs[4]	1.2 V to 1.95 V		V_{CCI} × 0.65		V
			1.95 V to 2.7 V		1.7		
			2.7 V to 3.6 V		2		
V_{IL}	Low-level input voltage	All inputs[4]	1.2 V to 1.95 V			V_{CCI} × 0.35	V
			1.95 V to 2.7 V			0.7	
			2.7 V to 3.6 V			0.8	
V_I	Input voltage	Control inputs			0	3.6	V
$V_{I/O}$	Input/output voltage	Active state			0	V_{CCO}	V
		3-state			0	3.6	
I_{OH}	High-level output current (A port)			1.2 V		–1	mA
				1.4 V to 1.6 V		–1	
				1.65 V to 1.95 V		–2	
				2.3 V to 2.7 V		–4	
				3 V to 3.6 V		–8	
I_{OL}	Low-level output current (A port)			1.2 V		1	mA
				1.4 V to 1.6 V		1	
				1.65 V to 1.95 V		2	
				2.3 V to 2.7 V		4	
				3 V to 3.6 V		8	
I_{OH}	High-level output current (B port)			1.2 V		–1	mA
				1.4 V to 1.6 V		–2	
				1.65 V to 1.95 V		–4	
				2.3 V to 2.7 V		–8	
				3 V to 3.6 V		–16	
I_{OL}	Low-level output current (B port)			1.2 V		1	mA
				1.4 V to 1.6 V		2	
				1.65 V to 1.95 V		4	
				2.3 V to 2.7 V		8	
				3 V to 3.6 V		16	
Δt/Δv	Input transition rise or fall rate					5	ns/V
T_A	Operating free-air temperature				–40	85	°C

(1) V_{CCI} is the V_{CC} associated with the input port.
(2) V_{CCO} is the V_{CC} associated with the output port.
(3) All unused data inputs of the device must be held at V_{CCI} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
(4) DIR2, DIR1, and DIR(345) are referenced to V_{CCA}.

ELECTRICAL CHARACTERISTICS[1][2]

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CCA}	V_{CCB}	T_A = 25°C MIN	TYP[3]	MAX	UNIT
V_{OH}	A port	I_{OH} = –100 µA	$V_I = V_{IH}$	1.2 V to 3.6 V	1.2 V to 3.6 V	V_{CCO} – 0.2			V
		I_{OH} = –1 mA		1.2 V	1.2 V		1.1		
				1.4 V	1.4 V	1.05			
		I_{OH} = –2 mA		1.65 V	1.65 V	1.2			
		I_{OH} = –4 mA		2.3 V	2.3 V	1.75			
		I_{OH} = –8 mA		3 V	3 V	2.3			
V_{OL}	A port	I_{OL} = 100 µA	$V_I = V_{IL}$	1.2 V to 3.6 V	1.2 V to 3.6 V			0.2	V
		I_{OL} = 1 mA		1.2 V	1.2 V		0.07		
				1.4 V	1.4 V			0.35	
		I_{OL} = 2 mA		1.65 V	1.65 V			0.45	
		I_{OL} = 4 mA		2.3 V	2.3 V			0.55	
		I_{OL} = 8 mA		3 V	3 V			0.7	
V_{OH}	B port	I_{OH} = –100 µA	$V_I = V_{IH}$	1.2 V to 3.6 V	1.2 V to 3.6 V	V_{CCO} – 0.2			V
		I_{OH} = –1 mA		1.2 V	1.2 V		1.1		
		I_{OH} = –2 mA		1.4 V	1.4 V	1.05			
		I_{OH} = –4 mA		1.65 V	1.65 V	1.2			
		I_{OH} = –8 mA		2.3 V	2.3 V	1.75			
		I_{OH} = –16 mA		3 V	3 V	2.3			
V_{OL}	B port	I_{OL} = 100 µA	$V_I = V_{IL}$	1.2 V to 3.6 V	1.2 V to 3.6 V			0.2	V
		I_{OL} = 1 mA		1.2 V	1.2 V		0.07		
		I_{OL} = 2 mA		1.4 V	1.4 V			0.35	
		I_{OL} = 4 mA		1.65 V	1.65 V			0.45	
		I_{OL} = 8 mA		2.3 V	2.3 V			0.55	
		I_{OL} = 16 mA		3 V	3 V			0.7	
I_I	Control inputs	$V_I = V_{CCA}$ or GND		1.2 V to 3.6 V	1.2 V to 3.6 V			±1	µA
I_{off}	A or B port	V_I or V_O = 0 to 3.6 V		0 V	0 V to 3.6 V			±5	µA
				0 V to 3.6 V	0 V			±5	
I_{OZ}[4]	A or B port	$V_O = V_{CCO}$ or GND, $V_I = V_{CCI}$ or GND	See function table for input states when outputs are Hi Z	3.6 V	3.6 V			±5	µA
I_{CCA}		$V_I = V_{CCI}$ or GND,	$I_O = 0$	1.2 V to 3.6 V	1.2 V to 3.6 V			10	µA
				3.6 V	0 V			10	
				0 V	3.6 V			–1	
I_{CCB}		$V_I = V_{CCI}$ or GND,	$I_O = 0$	1.2 V to 3.6 V	1.2 V to 3.6 V			10	µA
				3.6 V	0 V			–1	
				0 V	3.6 V			10	
$I_{CCA} + I_{CCB}$		$V_I = V_{CCI}$ or GND,	$I_O = 0$	1.2 V to 3.6 V	1.2 V to 3.6 V			15	µA
C_i	Control inputs	$V_I = V_{CCA}$ or GND		1.8 V	3 V		1.5	2	pF
	Clock input						2	2.5	
C_{io}	A port	$V_O = V_{CCA}$ or GND		1.8 V	3 V		2.5	3	pF
	B port	$V_O = V_{CCB}$ or GND					2.5	3	

(1) V_{CCO} is the V_{CC} associated with the output port.
(2) V_{CCI} is the V_{CC} associated with the input port.
(3) All typical values are at T_A = 25°C.
(4) For I/O ports, the parameter I_{OZ} includes the input leakage current.

OUTPUT SLEW RATES[1]

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM	TO	V_{CCA} = 1.8 V ± 0.15 V, V_{CCB} = 3 V ± 0.3 V MIN	MAX	UNIT
t_r	10%	90%		3[2]	ns
t_f	90%	10%		3[2]	ns

(1) Values are characterized, but not production tested.
(2) Using C_L = 15 pF on the B side and C_L = 7 pF on the A side

TYPICAL SWITCHING CHARACTERISTICS

T_A = 25°C, V_{CCA} = 1.2 V (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.2 V TYP	V_{CCB} = 1.5 V TYP	V_{CCB} = 1.8 V TYP	V_{CCB} = 2.5 V TYP	V_{CCB} = 3 V TYP	V_{CCB} = 3.3 V TYP	UNIT
t_{pd}	A	B	3.8	3	2.6	2.5	2.5	2.6	ns
	B	A	4.6	4.2	4	3.9	3.9	3.8	
	A6	B6	3.8	3	2.6	2.5	2.5	2.6	
	A2	B2	3.8	3	2.6	2.5	2.5	2.6	
	B2	A2	4.6	4.2	4	3.9	3.9	3.8	
t_{en}[1]	DIR	B	4.8	4	3.7	3.4	3.4	3.4	ns
		A	4.5	4.4	5	5.4	5.4	5.4	
t_{dis}[1]	DIR	B	6.3	5.2	5.6	4.8	4.8	6.1	ns
		A	4.8	4.6	5.3	5.4	5.4	5.3	

(1) DIR refers to DIR2, DIR1, and DIR(345).

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, V_{CCA} = 1.5 V ± 0.1 V (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.2 V	V_{CCB} = 1.5 V ± 0.1 V		V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3 V ± 0.3 V		V_{CCB} = 3.3 V ± 0.3 V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	B	3.4	1.1	5.6	1	4.8	1	3.9	0.9	3.9	0.9	3.8	ns
	B	A	3.8	1.4	6	1.3	5.6	1.3	5.2	0.5	5.2	0.3	5.2	
	A6	B6	3.4	1.1	5.6	1	4.8	1	3.9	0.9	3.9	0.9	3.8	
	A2	B2	3.4	1.1	5.6	1	4.8	1	3.9	0.9	3.9	0.9	3.8	
	B2	A2	3.8	1.4	6	1.3	5.6	1.3	5.2	0.5	5.2	0.3	5.2	
t_{en}[1]	DIR	B	4	1.3	7.7	1.1	6.9	0.8	6.1	0.8	6	0.8	5.9	ns
		A	3.5	1.4	7	1.5	7.4	1.7	8.2	1.7	8.2	1.7	7.7	
t_{dis}[1]	DIR	B	5.7	1.9	8.9	2.1	10.4	1.8	8.7	1.7	8.5	2.4	11.4	ns
		A	3.4	1.2	7	1.2	6.8	1.2	6.9	1.2	6.5	1.2	6.6	

(1) DIR refers to DIR2, DIR1, and DIR(345).

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, V_{CCA} = 1.8 V ± 0.15 V (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.2 V	V_{CCB} = 1.5 V ± 0.1 V		V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3 V ± 0.3 V		V_{CCB} = 3.3 V ± 0.3 V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	B	3.2	1	5.2	0.8	4.4	0.7	3.5	0.6	3.4	0.7	3.1	ns
	B	A	3.4	1.1	5.2	1	4.8	0.9	4.3	0.3	4.3	0.2	4.3	
	A6	B6	3.2	1	5.2	0.8	4.4	0.7	3.5	0.6	3.4	0.7	3.1	
	A2	B2	3.2	1	5.2	0.8	4.4	0.7	3.5	0.6	3.4	0.7	3.1	
	B2	A2	3.4	1.1	5.2	1	4.8	0.9	4.3	0.3	4.3	0.2	4.3	
t_{en} (1)	DIR	B	3.5	1.2	6.8	0.9	6	0.7	5.1	0.7	5	0.7	4.8	ns
		A	2.9	1.1	4.7	1.1	5.2	1.4	5.1	1.4	5.1	1.4	5.3	
t_{dis} (1)	DIR	B	5.3	1.6	8.4	2	9.5	1.6	8.2	1.4	8.1	2.2	8.2	ns
		A	3.6	1.3	7.7	1.2	7.9	1.3	7.5	1.3	7.5	1.3	7.6	

(1) DIR refers to DIR2, DIR1, and DIR(345).

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, V_{CCA} = 2.5 V ± 0.2 V (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.2 V	V_{CCB} = 1.5 V ± 0.1 V		V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3 V ± 0.3 V		V_{CCB} = 3.3 V ± 0.3 V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	B	3	0.8	4.7	0.7	3.8	0.6	2.9	0.4	2.7	0.5	2.5	ns
	B	A	3	0.9	4.4	0.7	3.9	0.6	3.3	0.3	3.2	0.3	3.2	
	A6	B6	3	0.8	4.7	0.7	3.8	0.6	2.9	0.4	2.7	0.5	2.5	
	A2	B2	3	0.8	4.7	0.7	3.8	0.6	2.9	0.4	2.7	0.5	2.5	
	B2	A2	3	0.9	4.4	0.7	3.9	0.6	3.3	0.3	3.2	0.3	3.2	
t_{en} (1)	DIR	B	3.1	1	5.7	0.8	4.8	0.5	3.9	0.5	3.7	0.5	3.6	ns
		A	2.2	0.7	3.5	0.6	4.3	1.2	4.4	0.7	4.6	0.4	4.7	
t_{dis}	DIR	B	4.6	1.4	7.6	1.8	8.4	1.3	7.2	1.3	7.1	2	7.5	ns
		A	2.6	0.9	5.6	0.9	5.4	1	5.5	0.9	5.5	0.9	5.8	

(1) DIR refers to DIR2, DIR1, and DIR(345).

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, V_{CCA} = 3.3 V ± 0.3 V (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.2 V	V_{CCB} = 1.5 V ± 0.1 V		V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3 V ± 0.3 V		V_{CCB} = 3.3 V ± 0.3 V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	B	2.8	0.8	4.5	0.6	3.6	0.4	2.7	0.4	2.7	0.3	2.3	ns
	B	A	2.9	0.8	4.3	0.6	3.7	0.5	3	0.5	3	0.1	2.7	
	A6	B6	2.8	0.8	4.5	0.6	3.6	0.4	2.7	0.4	2.7	0.3	2.3	
	A2	B2	2.8	0.8	4.5	0.6	3.6	0.4	2.7	0.4	2.7	0.3	2.3	
	B2	A2	2.9	0.8	4.3	0.6	3.7	0.5	3	0.5	3	0.1	2.7	
t_{en} (1)	DIR	B	3	1	5.1	0.6	4.3	0.5	3.4	0.5	3.4	0.4	3	ns
		A	2	0.6	3.1	0.6	5.4	0.7	5.4	0.7	5.4	0.5	5.4	
t_{dis} (1)	DIR	B	4.4	1.4	7.4	1.8	8.3	1.2	7	1.2	7	2	7.3	ns
		A	3.7	1.5	8.1	1.5	7.9	1.5	7.9	1.5	7.9	1.5	8	

(1) DIR refers to DIR2, DIR1, and DIR(345).

TYPICAL FREQUENCY AND OUTPUT SKEW

T_A = 25°C, V_{CCA} = 1.2 V (see Figure 2)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.2 V	V_{CCB} = 1.5 V	V_{CCB} = 1.8 V	V_{CCB} = 2.5 V	V_{CCB} = 3 V	V_{CCB} = 3.3 V	UNIT
				TYP	TYP	TYP	TYP	TYP	TYP	
t_{max}	Clock	A6	B6	95	95	95	95	95	95	MHz
	Data	A	B	95	95	95	95	95	95	
		B	A	95	95	95	95	95	95	
$t_{sk(o)}$	Channel-to-channel	A	B	0.5	0.4	0.4	0.3	0.5	0.5	ns

MAXIMUM FREQUENCY AND OUTPUT SKEW

over recommended operating free-air temperature range, V_{CCA} = 1.5 V ± 0.1 V (see Figure 2)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.2 V	V_{CCB} = 1.5 V ± 0.1 V		V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3 V ± 0.3 V		V_{CCB} = 3.3 V ± 0.3 V		UNIT
				TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}	Clock	A6	B6	95	95		95		95		95		95		MHz
	Data	A	B	95	95		95		95		95		95		
		B	A	95	95		95		95		95		95		
$t_{sk(o)}$	Channel-to-channel	DIR	B	0.3		0.3		0.3		0.3		0.5		0.4	ns

MAXIMUM FREQUENCY AND OUTPUT SKEW

over recommended operating free-air temperature range, V_{CCA} = 1.8 V ± 0.15 V (see Figure 2)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.2 V	V_{CCB} = 1.5 V ± 0.1 V		V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3 V ± 0.3 V		V_{CCB} = 3.3 V ± 0.3 V		UNIT
				TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}	Clock	A6	B6	95	95		95		95		95		95		MHz
	Data	A	B	95	95		95		95		95		95		
		B	A	95	95		95		95		95		95		
$t_{sk(o)}$	Channel-to-channel	DIR	B	0.3		0.3		0.3		0.3		0.5		0.3	ns

MAXIMUM FREQUENCY AND OUTPUT SKEW

over recommended operating free-air temperature range, V_{CCA} = 2.5 V ± 0.2 V (see Figure 2)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.2 V	V_{CCB} = 1.5 V ± 0.1 V		V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3 V ± 0.3 V		V_{CCB} = 3.3 V ± 0.3 V		UNIT
				TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}	Clock	A6	B6	95	95		95		95		95		95		MHz
	Data	A	B	95	95		95		95		95		95		
		B	A	95	95		95		95		95		95		
$t_{sk(o)}$	Channel-to-channel	DIR	B	0.3		0.3		0.3		0.2		0.6		0.3	ns

MAXIMUM FREQUENCY AND OUTPUT SKEW

over recommended operating free-air temperature range, V_{CCA} = 3.3 V ± 0.3 V (see Figure 2)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.2 V	V_{CCB} = 1.5 V ± 0.1 V		V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3 V ± 0.3 V		V_{CCB} = 3.3 V ± 0.3 V		UNIT
				TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}	Clock	A6	B6	95	95		95		95		95		95		MHz
	Data	A	B	95	95		95		95		95		95		
		B	A	95	95		95		95		95		95		
$t_{sk(o)}$	Channel-to-channel	DIR	B	0.3		0.3		0.4		0.3		0.6		0.4	ns

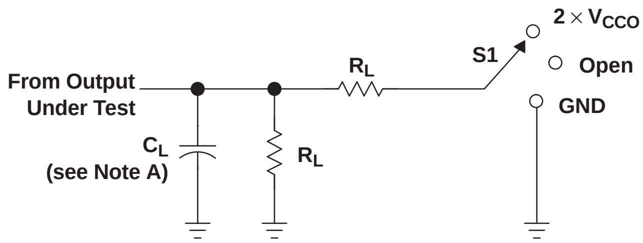
OPERATING CHARACTERISTICS

T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CCA} = V_{CCB} = 1.2 V	V_{CCA} = V_{CCB} = 1.5 V	V_{CCA} = V_{CCB} = 1.8 V	V_{CCA} = V_{CCB} = 2.5 V	V_{CCA} = V_{CCB} = 3 V	V_{CCA} = V_{CCB} = 3.3 V	UNIT
			TYP	TYP	TYP	TYP	TYP	TYP	
C_{pdA} (1)	A-port input, B-port output	C_L = 0, f = 10 MHz, t_r = t_f = 1 ns	1.9	2	2.1	2.4	2.7	2.9	pF
	B-port input, A-port output		4.4	4.5	4.6	4.7	4.8	4.9	
C_{pdB} (1)	A-port input, B-port output	C_L = 0, f = 10 MHz, t_r = t_f = 1 ns	5.3	5.4	5.4	5.7	5.8	5.9	pF
	B-port input, A-port output		0.3	0.3	0.4	0.5	0.6	0.6	

(1) Power dissipation capacitance per transceiver

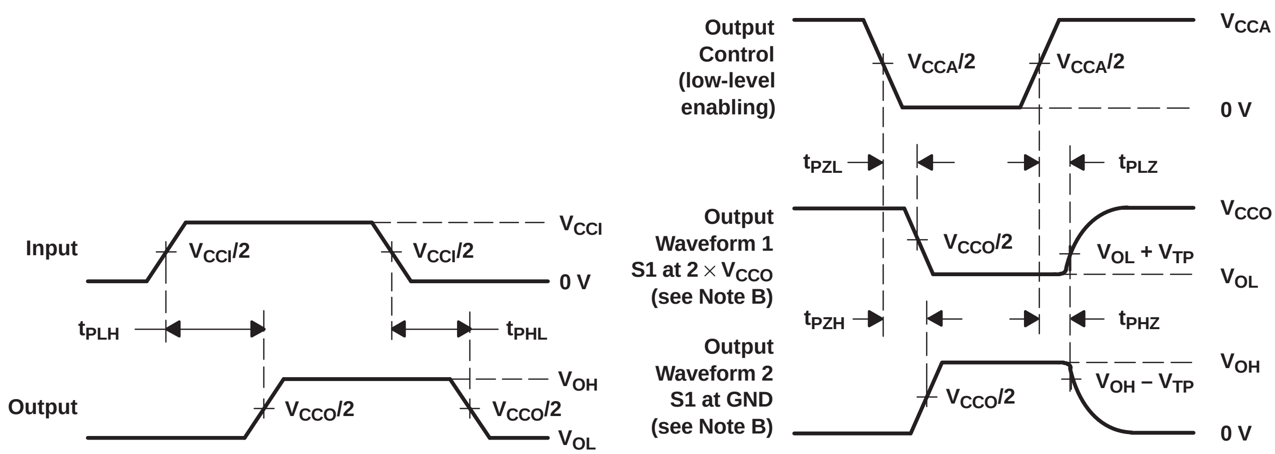
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CCO}$
t_{PHZ}/t_{PZH}	GND

V_{CCO}	C_L	R_L	V_{TP}
1.5 V ± 0.1 V	15 pF	2 kΩ	0.1 V
1.8 V ± 0.15 V	15 pF	2 kΩ	0.15 V
2.5 V ± 0.2 V	15 pF	2 kΩ	0.15 V
3.3 V ± 0.3 V	15 pF	2 kΩ	0.3 V



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, dv/dt ≥ 1 V/ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. V_{CCI} is the V_{CC} associated with the input port.
I. V_{CCO} is the V_{CC} associated with the output port.

Figure 2. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
SN74AVC6T622PWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	WU622	Samples
SN74AVC6T622PWRG4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	WU622	Samples
SN74AVC6T622RGYR	ACTIVE	VQFN	RGY	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	WU622	Samples
SN74AVC6T622RGYR4	ACTIVE	VQFN	RGY	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	WU622	Samples
SN74AVC6T622ZXYR	ACTIVE	BGA MICROSTAR JUNIOR	ZXY	20	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	WU622	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

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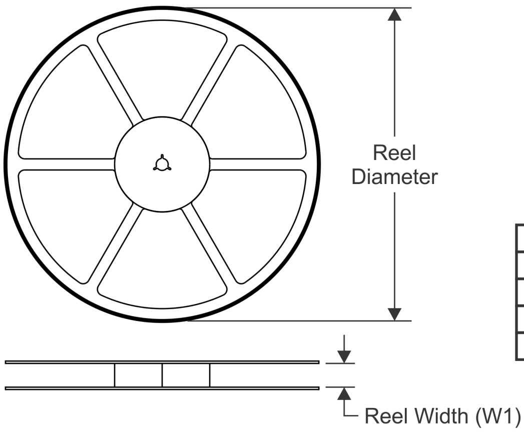
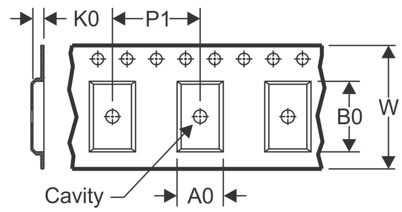
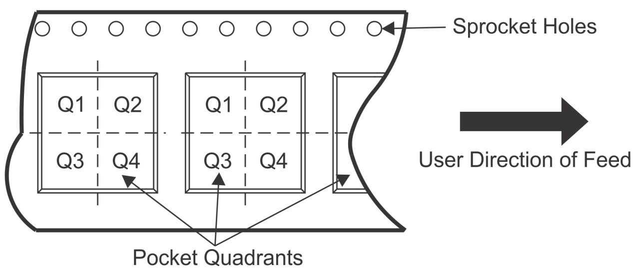
TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

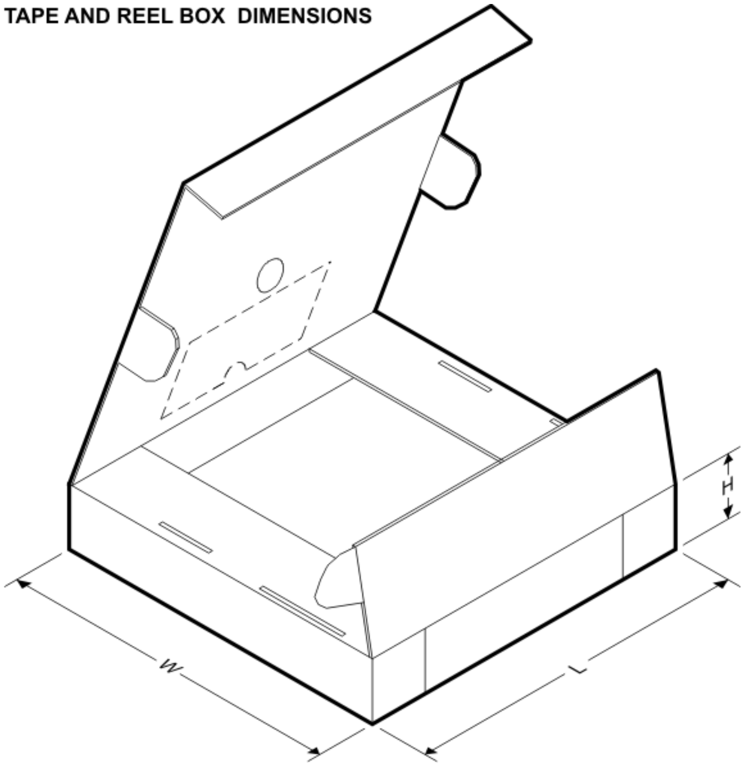
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AVC6T622PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
SN74AVC6T622RGYR	VQFN	RGY	20	3000	330.0	12.4	3.8	4.8	1.6	8.0	12.0	Q1
SN74AVC6T622ZXYR	BGA MI CROSTA R JUNI OR	ZXY	20	2500	330.0	12.4	2.8	3.3	1.0	4.0	12.0	Q2

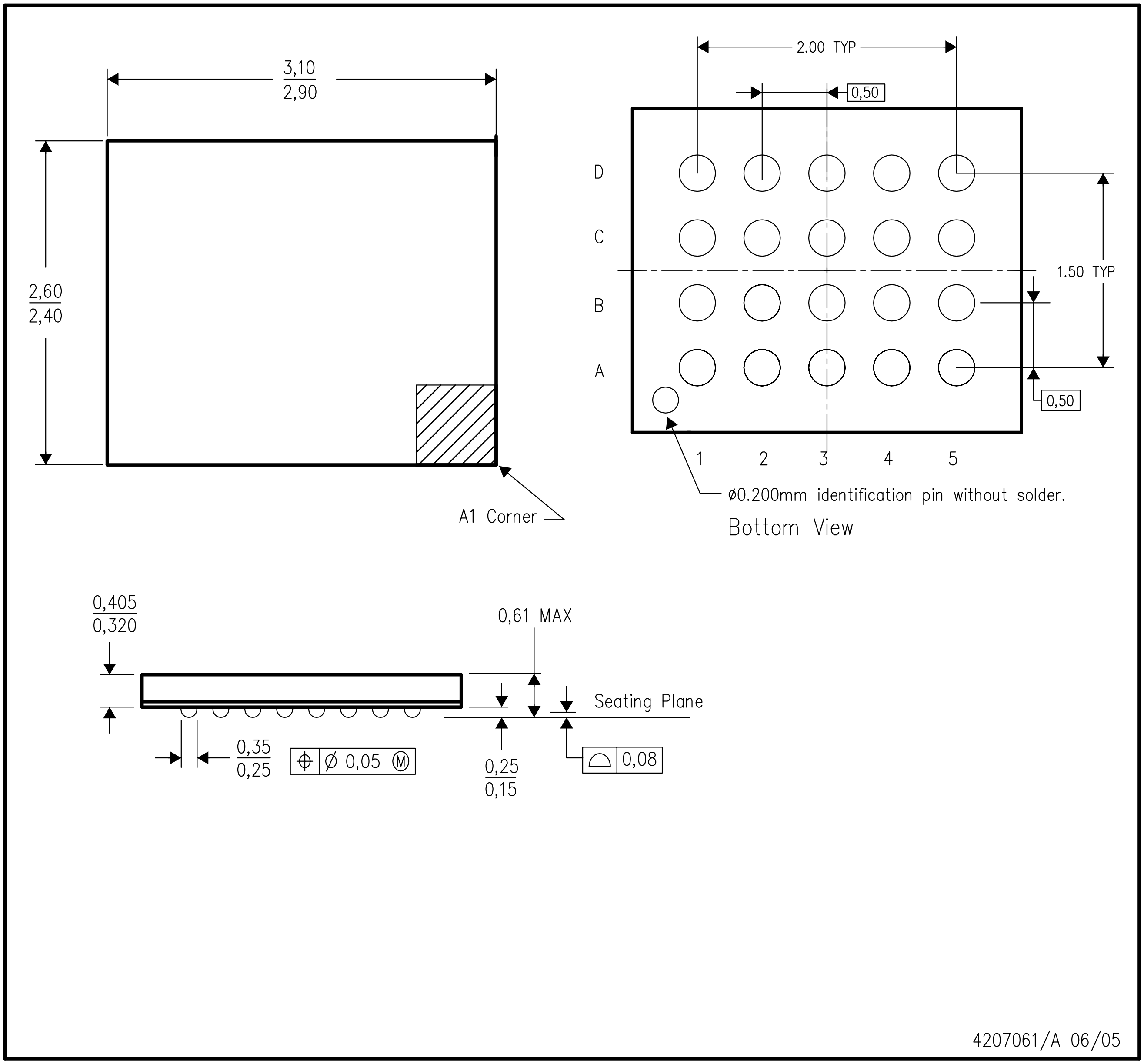
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

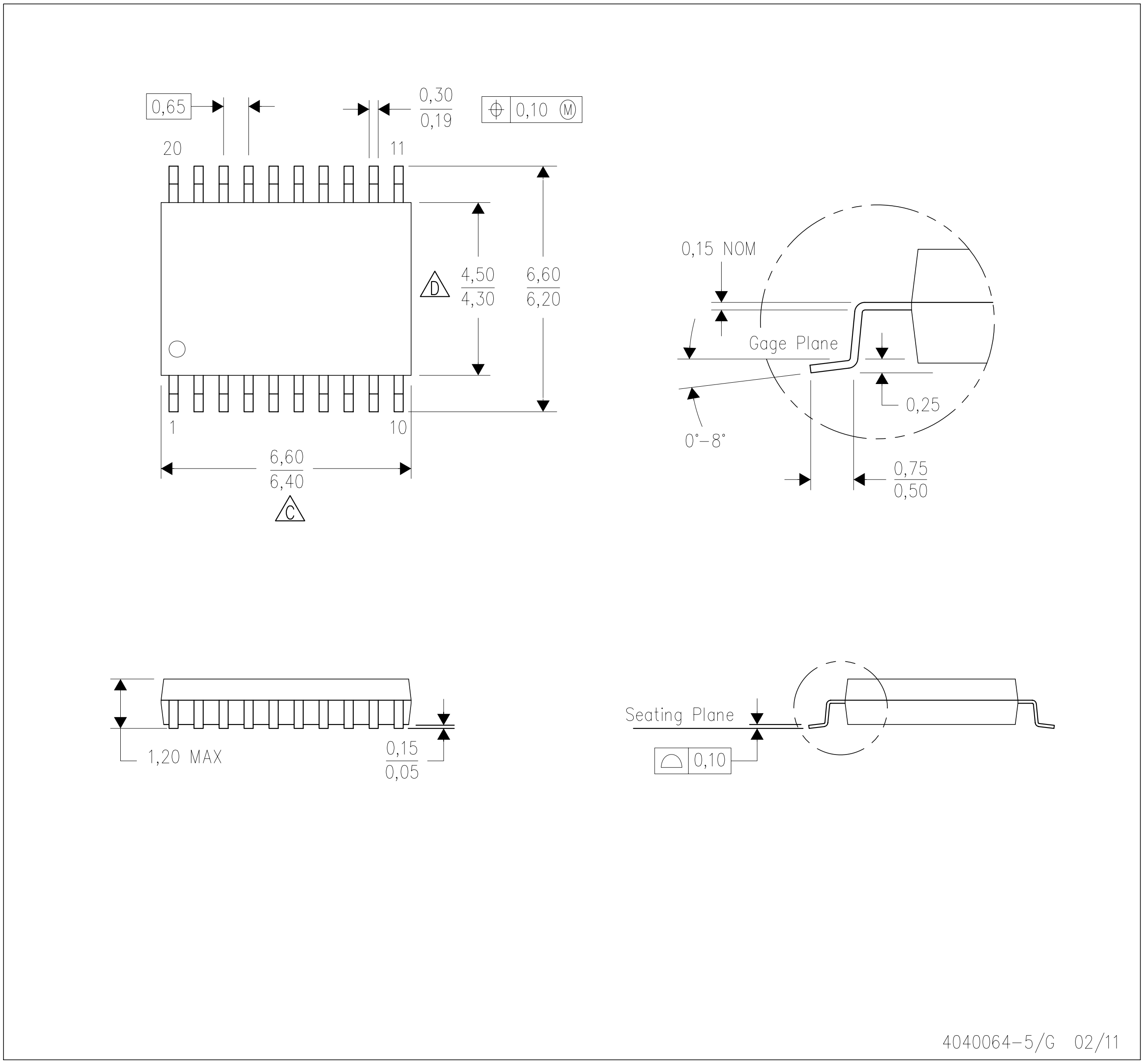
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AVC6T622PWR	TSSOP	PW	20	2000	367.0	367.0	38.0
SN74AVC6T622RGYR	VQFN	RGY	20	3000	367.0	367.0	35.0
SN74AVC6T622ZXYR	BGA MICROSTAR JUNIOR	ZXY	20	2500	338.1	338.1	20.6

ZXY (S–PBGA–N20) PLASTIC BALL GRID ARRAY



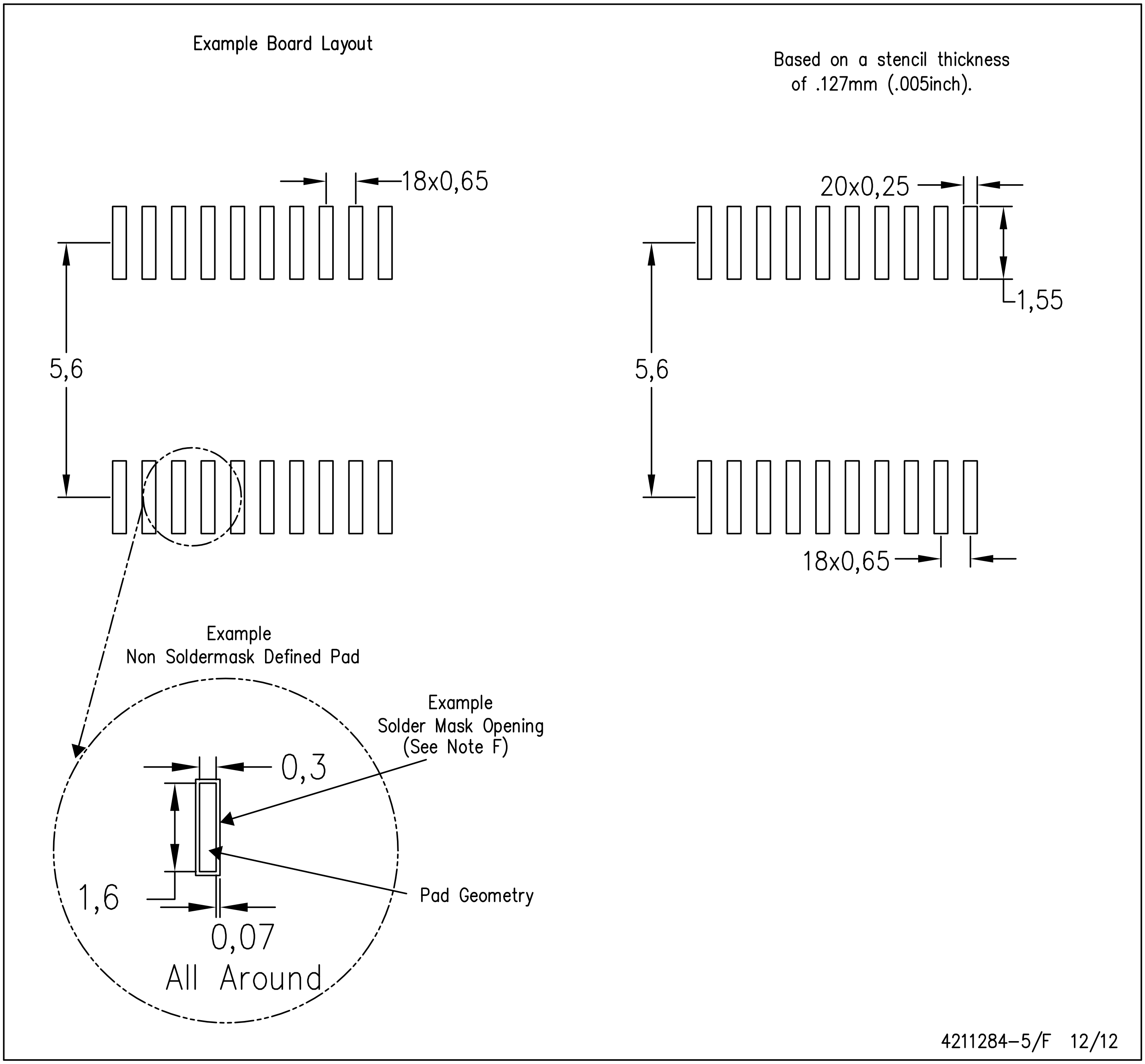
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. This package is a lead–free solder ball design.

PW (R-PDSO-G20) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G20) PLASTIC SMALL OUTLINE



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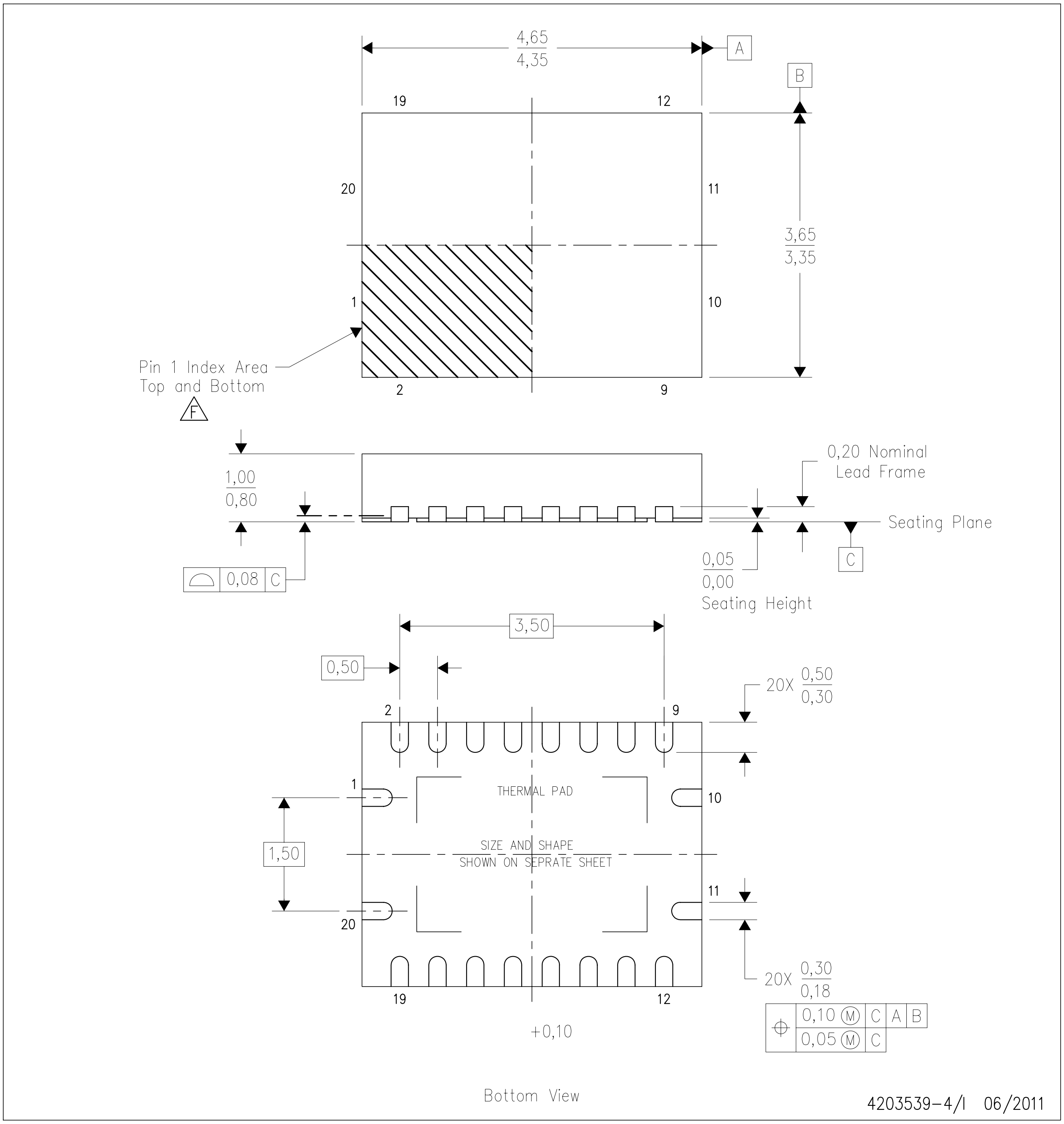
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate design.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

RGY (R-PVQFN-N20) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:

A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

B. This drawing is subject to change without notice.

C. QFN (Quad Flatpack No-Lead) package configuration.

D. The package thermal pad must be soldered to the board for thermal and mechanical performance.

E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.

G. Package complies to JEDEC MO-241 variation BA.

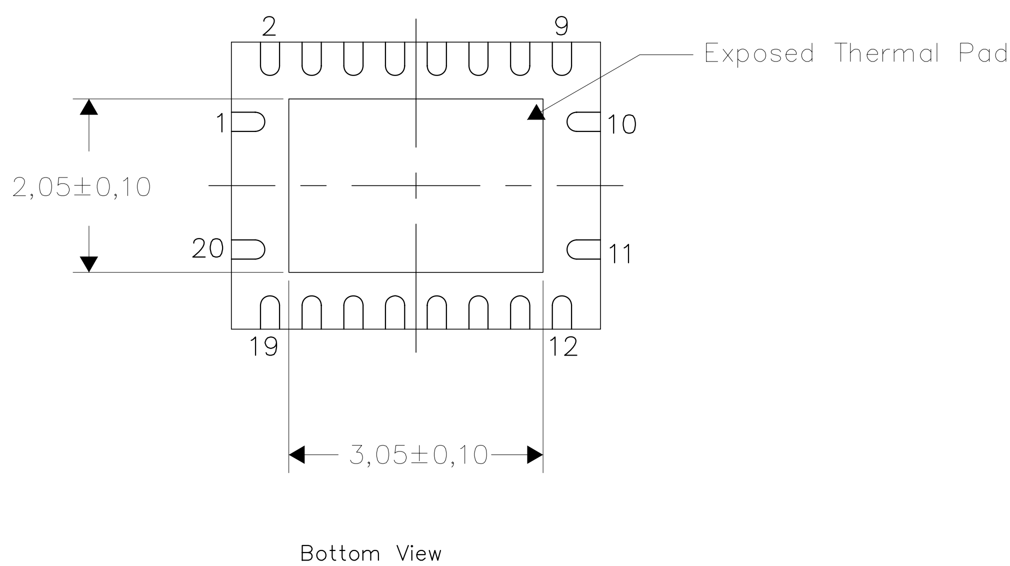
RGY (R–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Exposed Thermal Pad Dimensions

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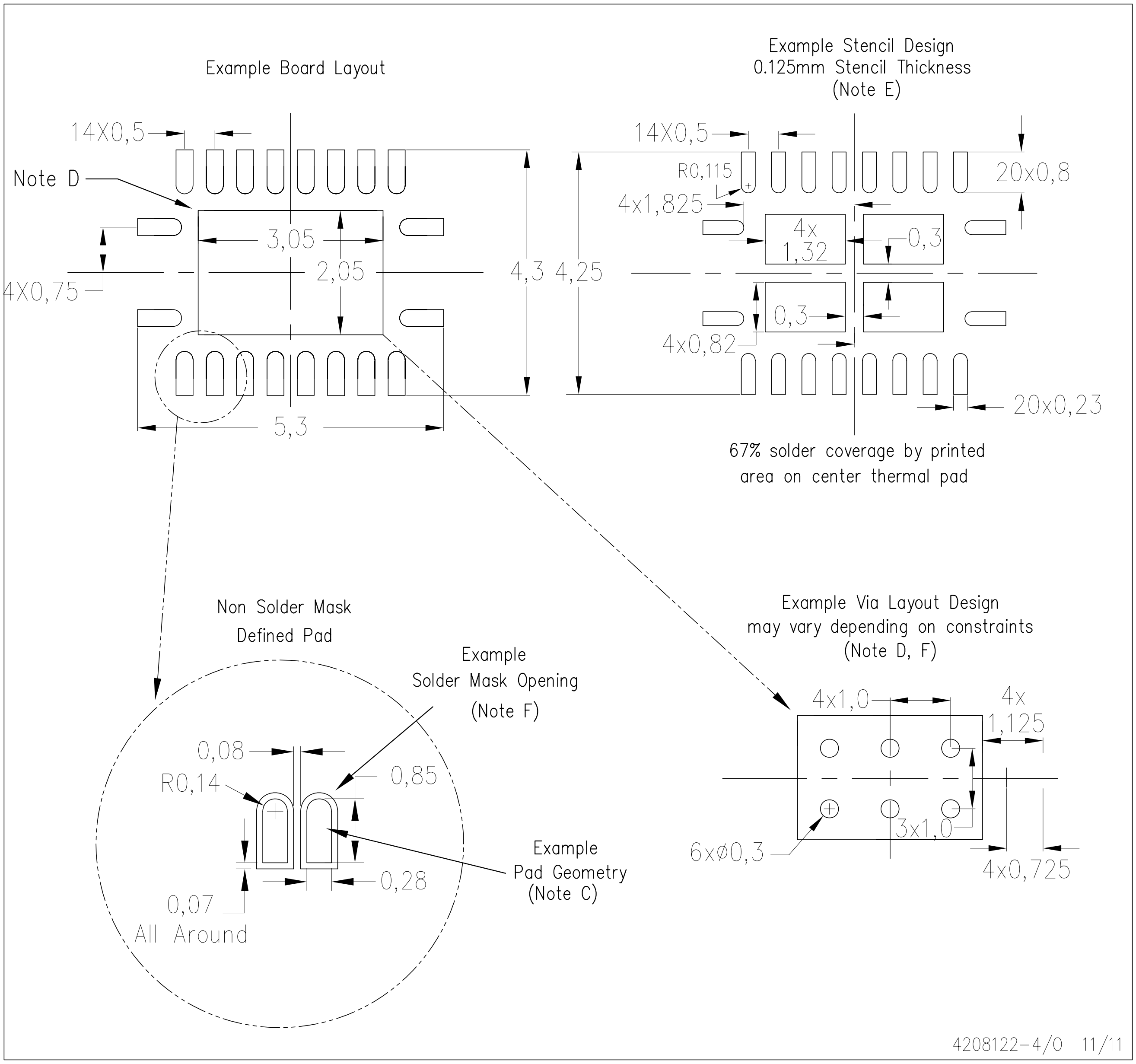
NOTE: All linear dimensions are in millimeters

RGY (R–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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