74AVC16374-Q100

16-bit edge triggered D-type flip-flop; 3.6 V tolerant; 3-state

Rev. 2 — 16 March 2015 | Product data sheet

1. General description

The 74AVC16374-Q100 is a 16-bit edge triggered flip-flop featuring separate D-type inputs for each flip-flop and 3-state outputs for bus-oriented applications. The 74AVC16374-Q100 consist of 2 sections of 8 edge-triggered flip-flops. A clock input (CP) and an output enable ($\overline{OE}$) are provided per 8-bit section.

The 74AVC16374-Q100 is designed to have an extremely fast propagation delay and a minimum amount of power consumption.

To ensure the high-impedance output state during power-up or power-down, n$\overline{OE}$ should be tied to VCC through a pull-up resistor (Live Insertion).

A Dynamic Controlled Output (DCO) circuitry is implemented to support termination line drive during transient (see Figure 5 and Figure 6).

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 3) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 3)
  - Specified from –40 °C to +85 °C
- Wide supply voltage range from 1.2 V to 3.6 V
- Complies with JEDEC standards:
  - JESD8-7 (1.2 V to 1.95 V)
  - JESD8-5 (1.8 V to 2.7 V)
  - JESD8-1A (2.7 V to 3.6 V)
- ESD protection:
  - MIL-STD-883, method 3015 exceeds 1000 V
  - HBM JESD22-A114F exceeds 1000 V
  - MM JESD22-A115-A exceeds 200 V (C = 200 pF, R = 0 Ω)
- CMOS low power consumption
- Input/output tolerant up to 3.6 V
- Dynamic Controlled Output (DCO) circuit dynamically changes output impedance, resulting in noise reduction without speed degradation
- Low inductance multiple V_{CC} and GND pins to minimize noise and ground bounce
- Supports Live Insertion

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3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74AVC16374DGG-Q100	–40 °C to +85 °C	TSSOP48	plastic thin shrink small outline package; 48 leads; body width 6.1 mm	SOT362-1

4. Functional diagram

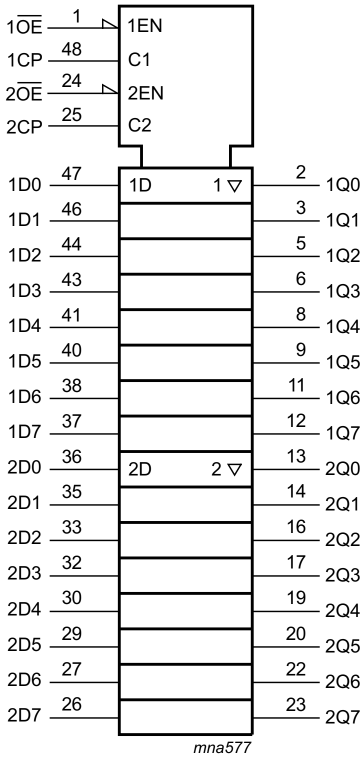


Fig 1. IEC logic symbol

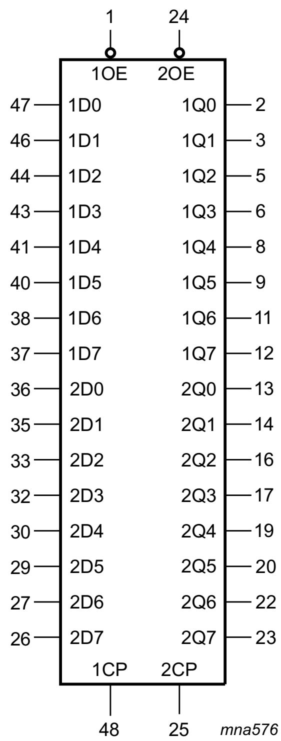


Fig 2. Logic symbol

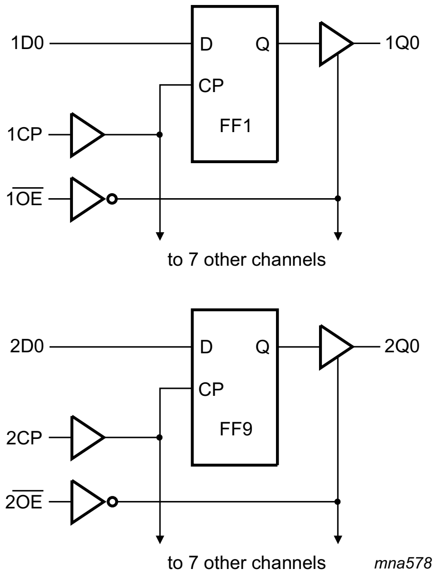


Fig 3. Logic diagram

5. Pinning information

5.1 Pinning

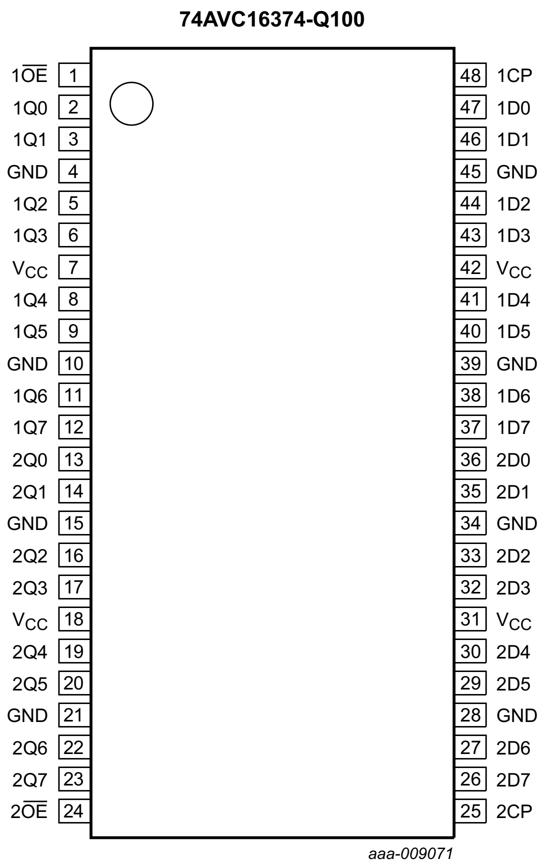


Fig 4. Pin configuration

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
$1\overline{OE}$	1	output enable input (active LOW)
1Q0 to 1Q7	2, 3, 5, 6, 8, 9, 11, 12	3-state flip-flop outputs
GND	4, 10, 15, 21, 28, 34, 39, 45	ground (0 V)
V_{CC}	7, 18, 31, 42	supply voltage
2Q0 to 2Q7	13, 14, 16, 17, 19, 20, 22, 23	3-state flip-flop outputs
$2\overline{OE}$	24	output enable input (active LOW)
2CP	25	clock input
2D0 to 2D7	36, 35, 33, 32, 30, 29, 27, 26	data input/output
1D0 to 1D7	47, 46, 44, 43, 41, 40, 38, 37	data input/output
1CP	48	clock input

6. Functional description

Table 3. Function table[1]

Operating modes	Inputs			Internal flip-flops	Outputs
	$\overline{nOE}$	nCp	nDn		nQn
Load and read register	L	↑	l	L	L
	L	↑	h	H	H
Load register and disable outputs	H	↑	l	L	Z
	H	↑	h	H	Z

[1] H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
Z = high-impedance OFF-state
↑ = LOW-to-HIGH CP transition

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		–0.5	+4.6	V
I_{IK}	input clamping current	$V_I < 0$ V	-	–50	mA
V_I	input voltage	[1]	–0.5	+4.6	V
I_{OK}	output clamping current	$V_O < 0$ V	–50	-	mA
V_O	output voltage	output HIGH or LOW [1]	–0.5	V_{CC} + 0.5	V
		output 3-state [1]	–0.5	+4.6	V
I_O	output current	V_O = 0 V to V_{CC}	-	±50	mA
I_{CC}	supply current		-	+100	mA
I_{GND}	ground current		–100	-	mA
T_{stg}	storage temperature		–65	+150	°C
P_{tot}	total power dissipation	T_{amb} = –40 °C to +85 °C [2]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] Above 60 °C, the value of P_{tot} derates linearly with 5.5 mW/K.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage	according to JEDEC Low Voltage Standards	1.4	-	1.6	V
			1.65	-	1.95	V
			2.3	-	2.7	V
			3.0	-	3.6	V
		for low-voltage applications	1.2	-	3.6	V
V_I	input voltage		0	-	3.6	V
V_O	output voltage	output HIGH or LOW	0	-	V_{CC}	V
		output 3-state	0	-	3.6	V
T_{amb}	ambient temperature	in free air	–40	-	+85	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 1.4 V to 1.6 V	0	-	40	ns/V
		V_{CC} = 1.65 V to 2.3 V	0	-	30	ns/V
		V_{CC} = 2.3 V to 3.0 V	0	-	20	ns/V
		V_{CC} = 3.0 V to 3.6 V	0	-	10	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
T_{amb} = –40 °C to +85 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 1.2 V	V_{CC}	-	-	V
		V_{CC} = 1.4 V to 1.6 V	0.65 × V_{CC}	0.9	-	V
		V_{CC} = 1.65 V to 1.95 V	0.65 × V_{CC}	0.9	-	V
		V_{CC} = 2.3 V to 2.7 V	1.7	1.2	-	V
		V_{CC} = 3.0 V to 3.6 V	2.0	1.5	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 1.2 V	-	-	GND	V
		V_{CC} = 1.4 V to 1.6 V	-	0.9	0.35 × V_{CC}	V
		V_{CC} = 1.65 V to 1.95 V	-	0.9	0.35 × V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V	-	1.2	0.7	V
		V_{CC} = 3.0 V to 3.6 V	-	1.5	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = –100 μA; V_{CC} = 1.65 V to 3.6 V	V_{CC} – 0.20	V_{CC}	-	V
		I_O = –3 mA; V_{CC} = 1.4 V	V_{CC} – 0.35	V_{CC} – 0.23	-	V
		I_O = –4 mA; V_{CC} = 1.65 V	V_{CC} – 0.45	V_{CC} – 0.25	-	V
		I_O = –8 mA; V_{CC} = 2.3 V	V_{CC} – 0.55	V_{CC} – 0.38	-	V
		I_O = –12 mA; V_{CC} = 3.0 V	V_{CC} – 0.70	V_{CC} – 0.48	-	V

Table 6. Static characteristics *...continued*

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = 100 μA; V_{CC} = 1.65 V to 3.6 V	-	GND	0.20	V
		I_O = 3 mA; V_{CC} = 1.4 V	-	0.10	0.35	V
		I_O = 4 mA; V_{CC} = 1.65 V	-	0.10	0.45	V
		I_O = 8 mA; V_{CC} = 2.3 V	-	0.26	0.55	V
		I_O = 12 mA; V_{CC} = 3.0 V	-	0.36	0.70	V
I_I	input leakage current	per pin; $V_I = V_{CC}$ or GND; V_{CC} = 1.4 V to 3.6 V	-	0.1	2.5	μA
I_{OFF}	power-off leakage current	V_I or V_O = 3.6 V; V_{CC} = 0.0 V	-	±0.1	±10	μA
I_{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL}; $V_O = V_{CC}$ or GND				
		V_{CC} = 1.4 V to 2.7 V	-	0.1	5	μA
		V_{CC} = 3.0 V to 3.6 V	-	0.1	10	μA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; I_O = 0 A				
		V_{CC} = 1.4 V to 2.7 V	-	0.1	20	μA
		V_{CC} = 3.0 V to 3.6 V	-	0.2	40	μA
C_I	input capacitance		-	5	-	pF

[1] All typical values are measured at T_{amb} = 25 °C.

9.1 Graphs

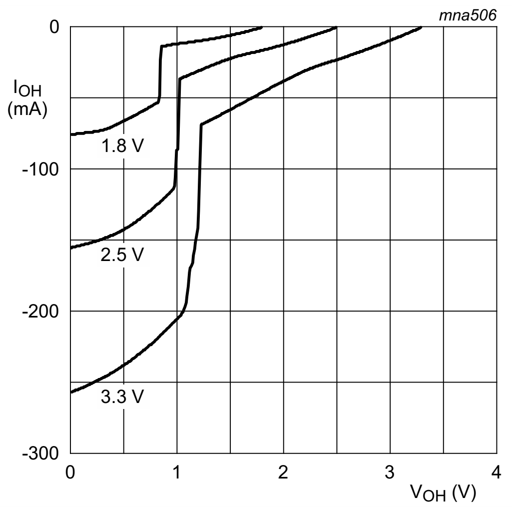


Fig 5. Output voltage as a function of the HIGH-level output current.

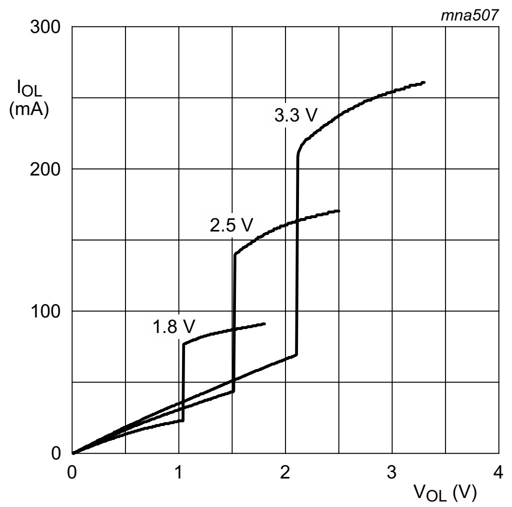


Fig 6. Output voltage as a function of the LOW-level output current.

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). t_r = t_f ≤ 2 ns. For test circuit, see Figure 10.

Symbol	Parameter	Conditions	–40 °C to +85 °C			Unit
			Min	Typ[2]	Max	
t_{pd}	propagation delay	nCP to nQn; see Figure 7 [1]				
		V_{CC} = 1.2 V	-	3.1	-	ns
		V_{CC} = 1.4 V to 1.6 V	1.2	2.4	8.4	ns
		V_{CC} = 1.65 V to 1.95 V	1.0	2.0	6.7	ns
		V_{CC} = 2.3 V to 2.7 V	0.8	1.5	4.1	ns
		V_{CC} = 3.0 V to 3.6 V	0.7	1.3	3.3	ns
t_{en}	enable time	n$\overline{OE}$ to nQn, nBn; see Figure 8 [1]				
		V_{CC} = 1.2 V	-	5.4	-	ns
		V_{CC} = 1.4 V to 1.6 V	1.6	3.9	8.5	ns
		V_{CC} = 1.65 V to 1.95 V	2.3	3.3	6.7	ns
		V_{CC} = 2.3 V to 2.7 V	0.9	2.3	4.3	ns
		V_{CC} = 3.0 V to 3.6 V	0.7	2.0	3.4	ns
t_{dis}	disable time	n$\overline{OE}$ to nQn; see Figure 8 [1]				
		V_{CC} = 1.2 V	-	5.6	-	ns
		V_{CC} = 1.4 V to 1.6 V	2.5	4.5	9.4	ns
		V_{CC} = 1.65 V to 1.95 V	1.8	3.3	7.8	ns
		V_{CC} = 2.3 V to 2.7 V	1.0	1.8	4.2	ns
		V_{CC} = 3.0 V to 3.6 V	1.2	2.0	3.9	ns
t_W	pulse width	HIGH; nCP; see Figure 7				
		V_{CC} = 1.2 V	-	0.8	-	ns
		V_{CC} = 1.4 V to 1.6 V	-	0.5	-	ns
		V_{CC} = 1.65 V to 1.95 V	3.1	0.3	-	ns
		V_{CC} = 2.3 V to 2.7 V	2.5	0.2	-	ns
		V_{CC} = 3.0 V to 3.6 V	2.5	0.2	-	ns
t_{su}	set-up time	nDn to nCP; see Figure 8				
		V_{CC} = 1.2 V	-	–0.6	-	ns
		V_{CC} = 1.4 V to 1.6 V	2.7	–0.3	-	ns
		V_{CC} = 1.65 V to 1.95 V	1.9	–0.3	-	ns
		V_{CC} = 2.3 V to 2.7 V	1.4	–0.2	-	ns
		V_{CC} = 3.0 V to 3.6 V	1.4	–0.1	-	ns
t_h	hold time	nDn to nCP; see Figure 8				
		V_{CC} = 1.2 V	-	0.8	-	ns
		V_{CC} = 1.4 V to 1.6 V	1.3	0.7	-	ns
		V_{CC} = 1.65 V to 1.95 V	1.2	0.6	-	ns
		V_{CC} = 2.3 V to 2.7 V	1.1	0.5	-	ns
		V_{CC} = 3.0 V to 3.6 V	1.1	0.4	-	ns

Table 7. Dynamic characteristics *...continued*

Voltages are referenced to GND (ground = 0 V). $t_r = t_f \leq 2$ ns. For test circuit, see Figure 10.

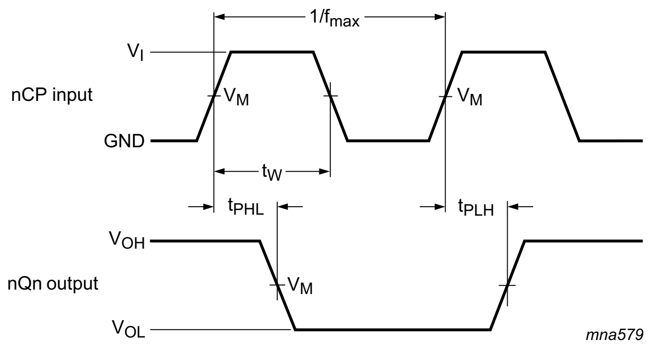
Symbol	Parameter	Conditions	–40 °C to +85 °C			Unit
			Min	Typ[2]	Max	
f_{max}	maximum frequency	see Figure 8				
		V_{CC} = 1.2 V	-	250	-	MHz
		V_{CC} = 1.4 V to 1.6 V	-	300	-	MHz
		V_{CC} = 1.65 V to 1.95 V	160	320	-	MHz
		V_{CC} = 2.3 V to 2.7 V	200	350	-	MHz
		V_{CC} = 3.0 V to 3.6 V	200	350	-	MHz
C_{PD}	power dissipation capacitance	per input; V_I = GND to V_{CC} [3]				
		outputs enabled	-	66	-	pF
		outputs disabled	-	1	-	pF

[1] t_{pd} is the same as t_{PLH} and t_{PHL}.
t_{en} is the same as t_{PZL} and t_{PZH}.
t_{dis} is the same as t_{PLZ} and t_{PHZ}.

[2] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.2 V, 1.5 V, 1.8 V, 2.5 V and 3.3 V respectively.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz; f_o = output frequency in MHz
C_L = output load capacitance in pF
V_{CC} = supply voltage in Volts
N = number of inputs switching
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

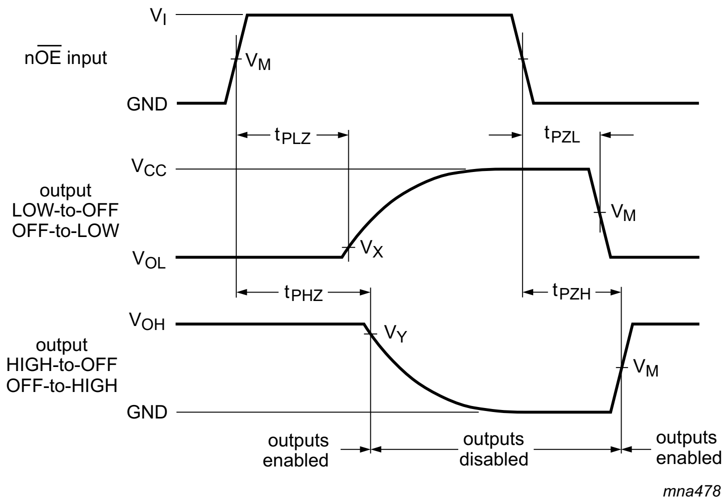
11. Waveforms



Measurement points are given in Table 9.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

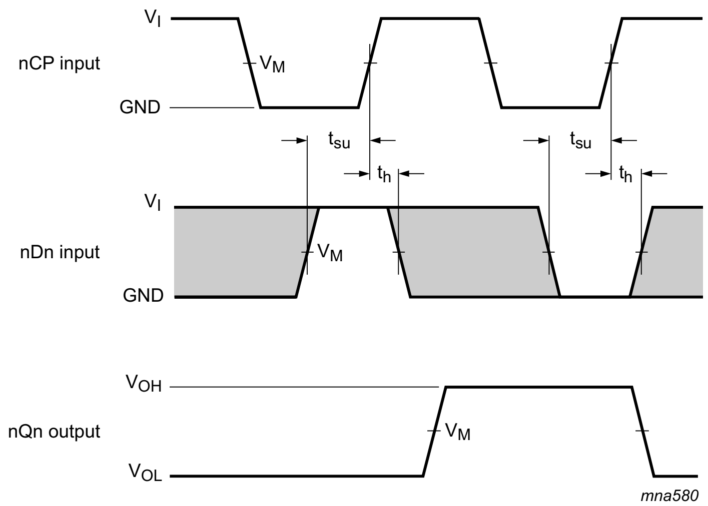
Fig 7. Clock input (nCP) to output (nQn) propagation delays



Measurement points are given in Table 9.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 8. 3-state enable and disable times



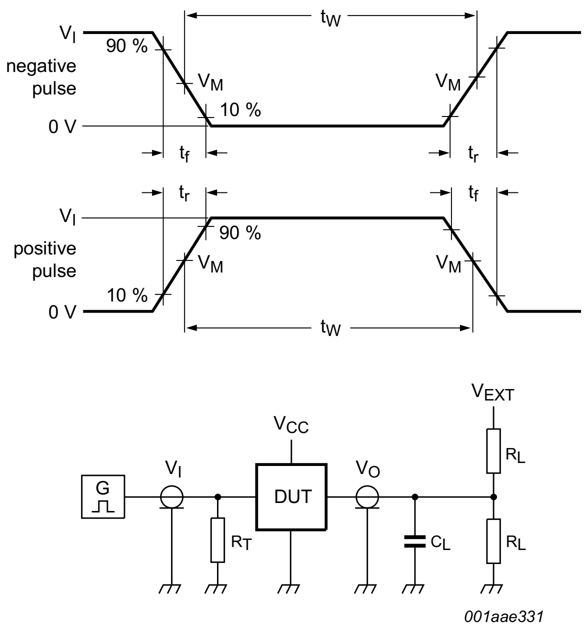
Measurement points are given in Table 9.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 9. Data set-up and hold times for nDn input to nCP input

Table 8. Measurement points

Supply voltage	V_M	Input			
V_{CC}		V_I	$t_r = t_f$	V_X	V_Y
1.2 V	0.5 × V_{CC}	V_{CC}	≤ 2 ns	V_{OL} + 0.15 V	V_{OH} − 0.15 V
1.4 V to 1.6 V	0.5 × V_{CC}	V_{CC}	≤ 2 ns	V_{OL} + 0.15 V	V_{OH} − 0.15 V
1.65 V to 1.95 V	0.5 × V_{CC}	V_{CC}	≤ 2 ns	V_{OL} + 0.15 V	V_{OH} − 0.15 V
2.3 V to 2.7 V	0.5 × V_{CC}	V_{CC}	≤ 2 ns	V_{OL} + 0.15 V	V_{OH} − 0.15 V
3.0 V to 3.6 V	0.5 × V_{CC}	V_{CC}	≤ 2 ns	V_{OL} + 0.3 V	V_{OH} − 0.3 V



Test data is given in Table 9.

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

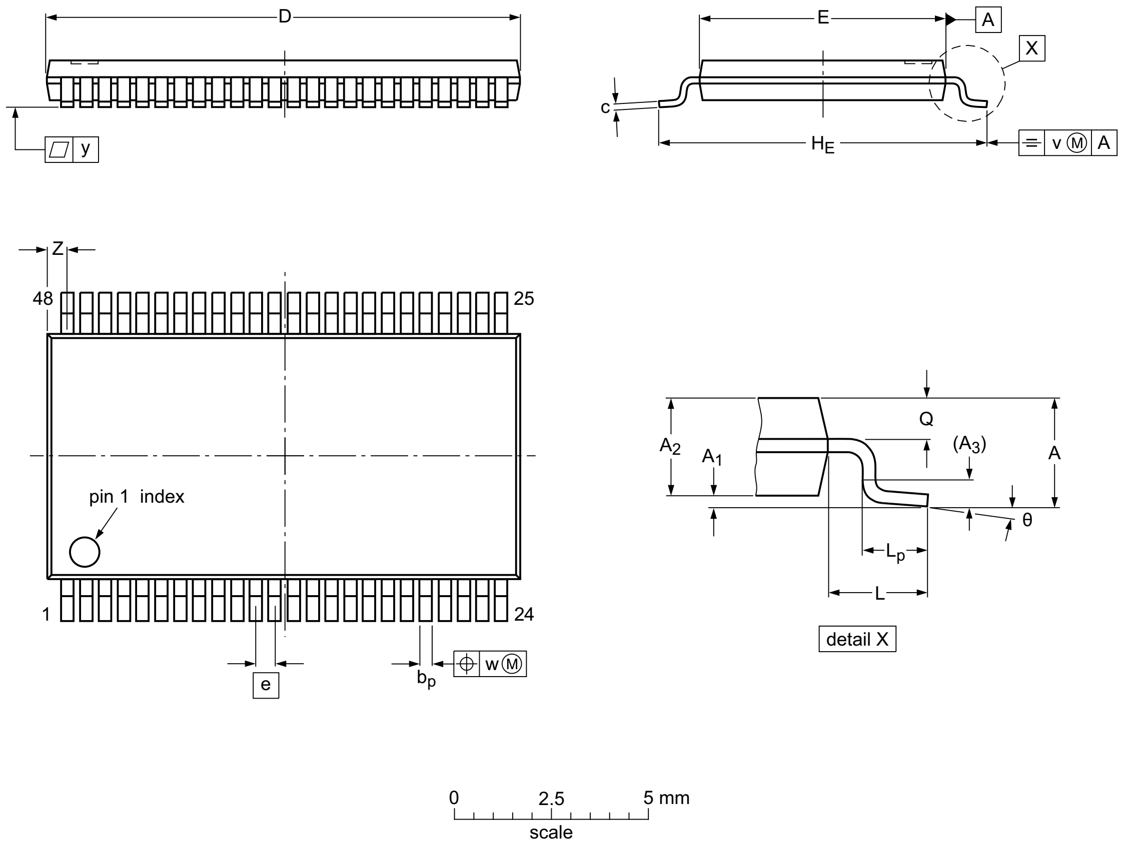
Fig 10. Test circuit for measuring switching times

Table 9. Test data

Supply voltage	Input		Load		V_{EXT}		
	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PLZ}, t_{PZL}	t_{PHZ}, t_{PZH}
1.2 V	V_{CC}	≤ 2 ns	15 pF	2 kΩ	open	2 × V_{CC}	GND
1.4 V to 1.6 V	V_{CC}	≤ 2 ns	15 pF	2 kΩ	open	2 × V_{CC}	GND
1.65 V to 1.95 V	V_{CC}	≤ 2 ns	30 pF	1 kΩ	open	2 × V_{CC}	GND
2.3 V to 2.7 V	V_{CC}	≤ 2 ns	30 pF	500 Ω	open	2 × V_{CC}	GND
3.0 V to 3.6 V	V_{CC}	≤ 2 ns	30 pF	500 Ω	open	2 × V_{CC}	GND

12. Package outline

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm **SOT362-1**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	A_3	b_p	c	D(1)	E(2)	e	H_E	L	L_p	Q	v	w	y	Z	θ
mm	max		0.15	1.05		0.28	0.2	12.6	6.2		8.3		0.8	0.50				0.8	8°
	nom	1.2			0.25					0.5		1			0.25	0.08	0.1		
	min		0.05	0.85		0.17	0.1	12.4	6.0		7.9		0.4	0.35				0.4	0°

Note
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

sot362-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT362-1		MO-153				~~03-02-19~~ 13-08-05

Fig 11. Package outline SOT362-1 (TSSOP48)

13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
MIL	Military
TTL	Transistor-Transistor Logic

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AVC16374_Q100 v.2	20150316	Product data sheet	-	74AVC16374_Q100 v.1
Modifications:	• Section 2: ESD protection; for MIL-STD-883 (method 3015) and HBM JESD22-A114F the value is changed from 2000 V to 1000 V.			
74AVC16374_Q100 v.1	20130916	Product data sheet	-	-

15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nexperia.com.

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16. Contact information

For more information, please visit: **http://www.nexperia.com**

For sales office addresses, please send an email to: **salesaddresses@nexperia.com**

17. Contents

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Date of release: 16 March 2015

Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов;
- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits,General Dynamics и др.);

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- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.

Как с нами связаться

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