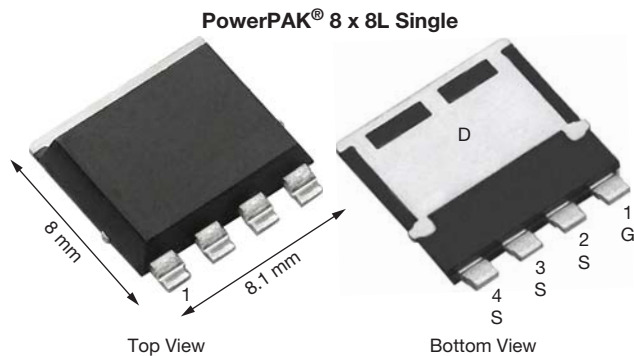


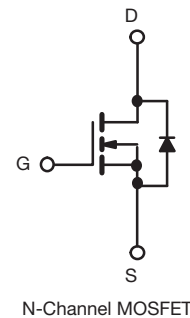
Automotive N-Channel 40 V (D-S) 175 °C MOSFET



FEATURES

- TrenchFET® power MOSFET
- AEC-Q101 qualified
- 100 % R_G and UIS tested
- Fully lead (Pb)-free device
- Thin 1.9 mm height
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

PRODUCT SUMMARY	
V _{DS} (V)	40
R _{DS(on)} (Ω) at V _{GS} = 10 V	0.0012
R _{DS(on)} (Ω) at V _{GS} = 4.5 V	0.0015
I _D (A)	200
Configuration	Single
Package	PowerPAK 8 x 8L



ABSOLUTE MAXIMUM RATINGS (T _C = 25 °C, unless otherwise noted)				
PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-source voltage	V _{DS}	40	V	
Gate-source voltage	V _{GS}	± 20		
Continuous drain current	I _D	T _C = 25 °C ^a	200	
		T _C = 125 °C	141	
Continuous source current (diode conduction)	I _S	136	A	
Pulsed drain current ^b	I _{DM}	600		
Single pulse avalanche current	I _{AS}	50		
Single pulse avalanche energy	E _{AS}	L = 0.1 mH	125	mJ
Maximum power dissipation			T _C = 25 °C	
		T _C = 125 °C	50	W
Operating junction and storage temperature range	T _J , T _{stg}	-55 to +175	°C	
Soldering recommendations (peak temperature) ^{d, e}		260		

THERMAL RESISTANCE RATINGS			
PARAMETER	SYMBOL	LIMIT	UNIT
Junction-to-ambient	R _{thJA}	50	°C/W
Junction-to-case (drain)	R _{thJC}	1	

Notes

- Package limited
- Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %
- When mounted on 1" square PCB (FR4 material)
- See solder profile (www.vishay.com/doc?73257). The PowerPAK 8 x 8L is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components



SPECIFICATIONS (T _C = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0, I _D = 250 μA	40	-	-	V
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	1.5	2	2.5	
Gate-source leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V	-	-	± 100	nA
Zero gate voltage drain current	I _{DSS}	V _{GS} = 0 V, V _{DS} = 40 V	-	-	1	μA
		V _{GS} = 0 V, V _{DS} = 40 V, T _J = 125 °C	-	-	50	
		V _{GS} = 0 V, V _{DS} = 40 V, T _J = 175 °C	-	-	500	
On-state drain current ^a	I _{D(on)}	V _{GS} = 10 V, V _{DS} ≥ 5 V	100	-	-	A
Drain-source on-state resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 20 A	-	0.0009	0.0012	Ω
		V _{GS} = 4.5 V, I _D = 10 A	-	0.0011	0.0015	
		V _{GS} = 10 V, I _D = 20 A, T _J = 125 °C	-	-	0.0018	
		V _{GS} = 10 V, I _D = 20 A, T _J = 175 °C	-	-	0.0022	
Forward transconductance ^b	g _{fs}	V _{DS} = 15 V, I _D = 15 A	-	122	-	S
Dynamic^b						
Input capacitance	C _{iSS}	V _{GS} = 0 V, V _{DS} = 25 V, f = 1 MHz	-	10 810	14 500	pF
Output capacitance	C _{oss}		-	6500	8500	
Reverse transfer capacitance	C _{rSS}		-	700	950	
Total gate charge ^c	Q _g	V _{GS} = 10 V, V _{DS} = 20 V, I _D = 10 A	-	140	220	nC
Gate-source charge ^c	Q _{gs}		-	30	-	
Gate-drain charge ^c	Q _{gd}		-	20	-	
Gate resistance	R _g	f = 1 MHz	0.45	0.99	1.50	Ω
Turn-on delay time ^c	t _{d(on)}	V _{DD} = 20 V, R _L = 2 Ω I _D ≅ 10 A, V _{GEN} = 10 V, R _g = 1 Ω	-	24	40	ns
Rise time ^c	t _r		-	60	100	
Turn-off delay time ^c	t _{d(off)}		-	60	100	
Fall time ^c	t _f		-	30	50	
Source-Drain Diode Ratings and Characteristics^b						
Pulsed current ^a	I _{SM}		-	-	200	A
Forward voltage	V _{SD}	I _F = 50 A, V _{GS} = 0	-	0.8	1.2	V

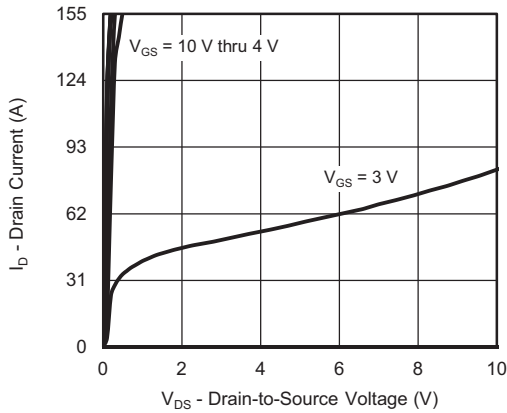
Notes

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %
b. Guaranteed by design, not subject to production testing
c. Independent of operating temperature

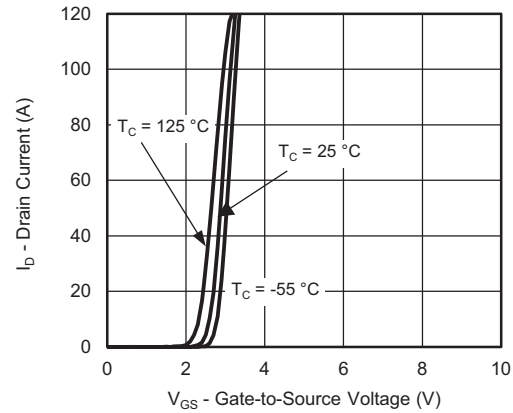
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



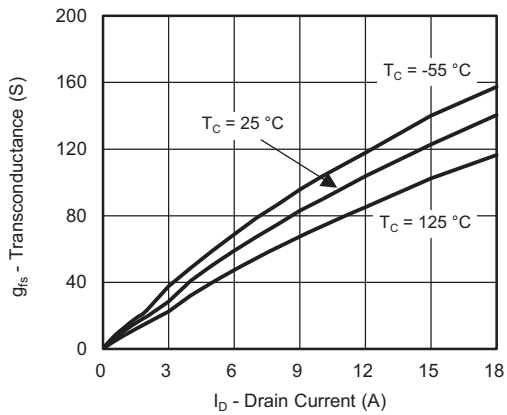
TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



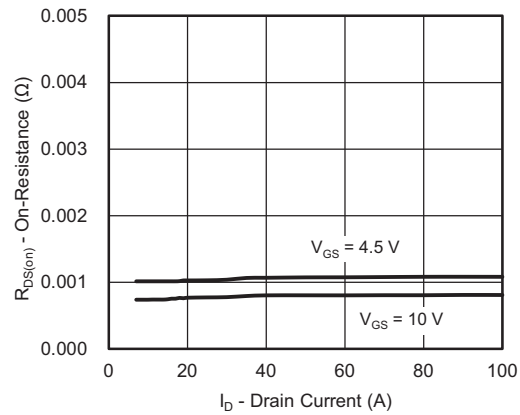
Output Characteristics



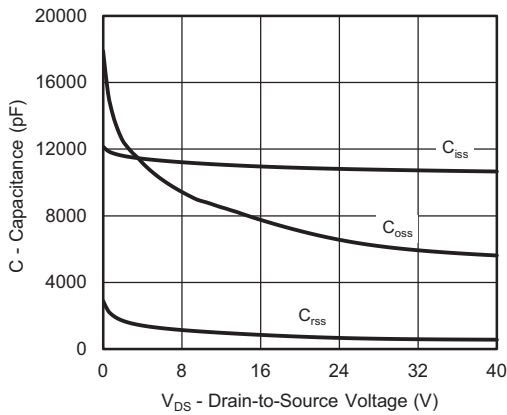
Transfer Characteristics



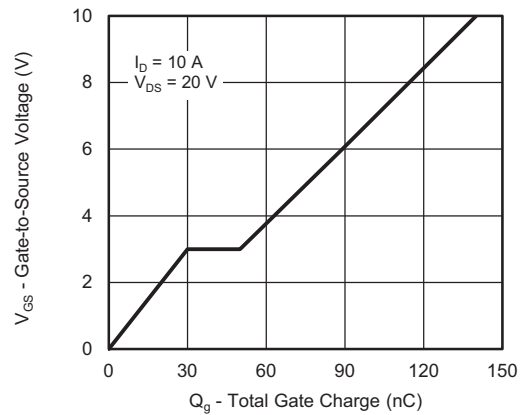
Transconductance



On-Resistance vs. Drain Current



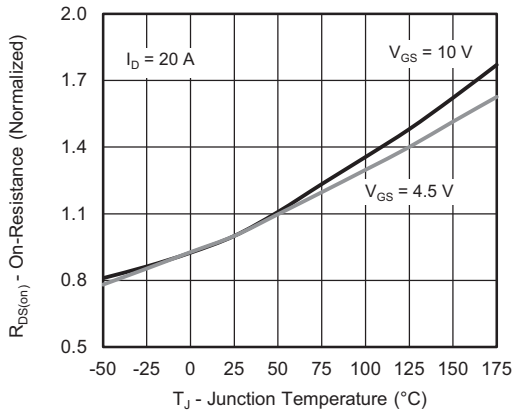
Capacitance



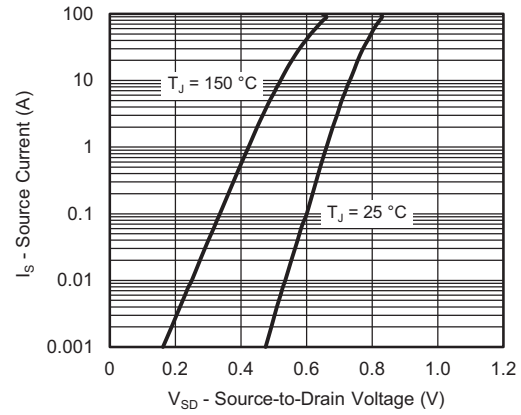
Gate Charge



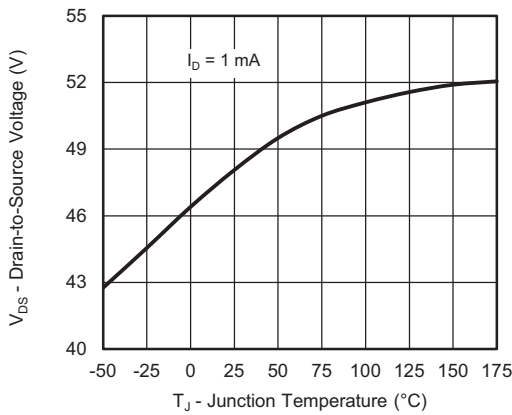
TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



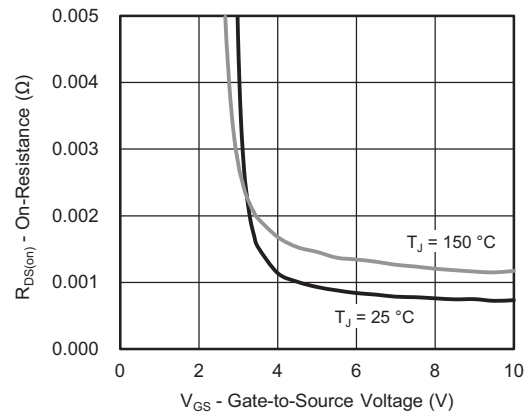
On-Resistance vs. Junction Temperature



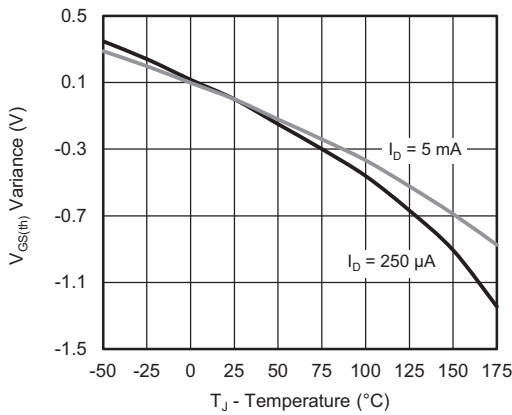
Source Drain Diode Forward Voltage



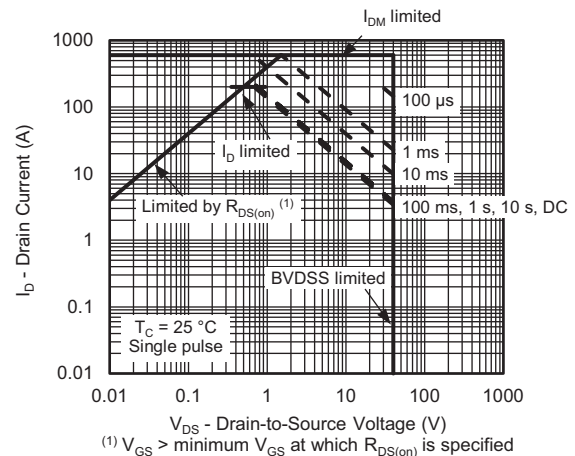
Drain Source Breakdown vs. Junction Temperature



On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

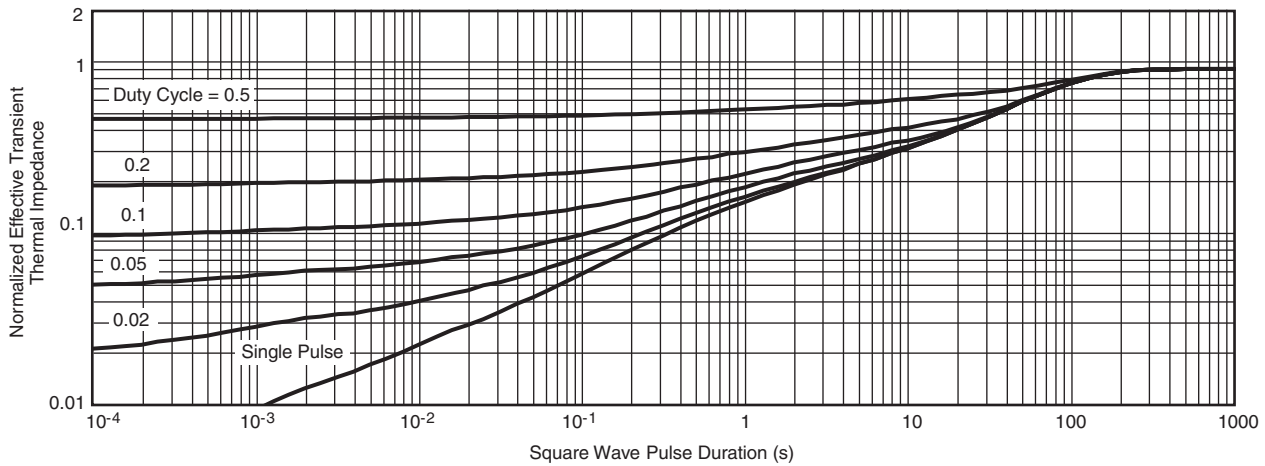


⁽¹⁾ $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

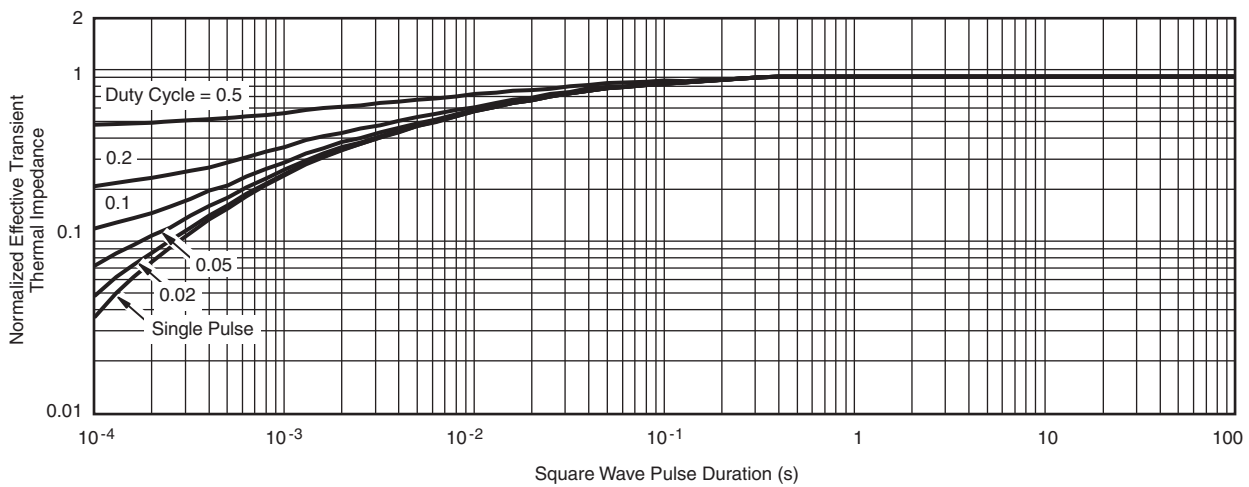
Safe Operating Area



THERMAL RATINGS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient

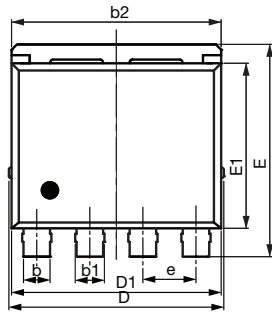


Normalized Thermal Transient Impedance, Junction-to-Case

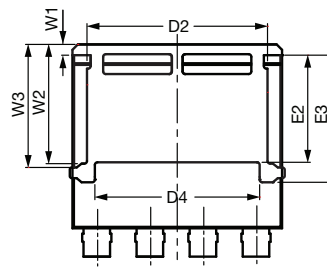
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?68443.



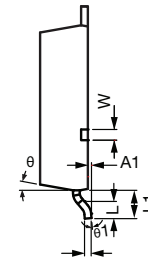
PowerPAK[®] 8 x 8L Case Outline



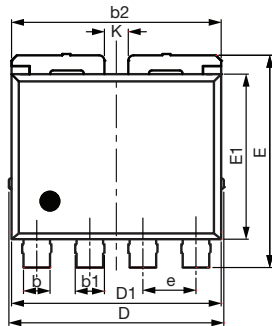
Top view (single)



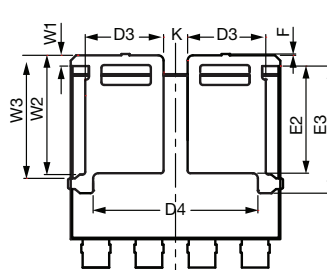
Bottom view (single)



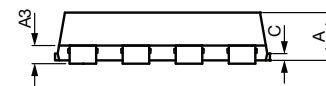
0.25 gauge line



Top view (dual)



Bottom view (dual)

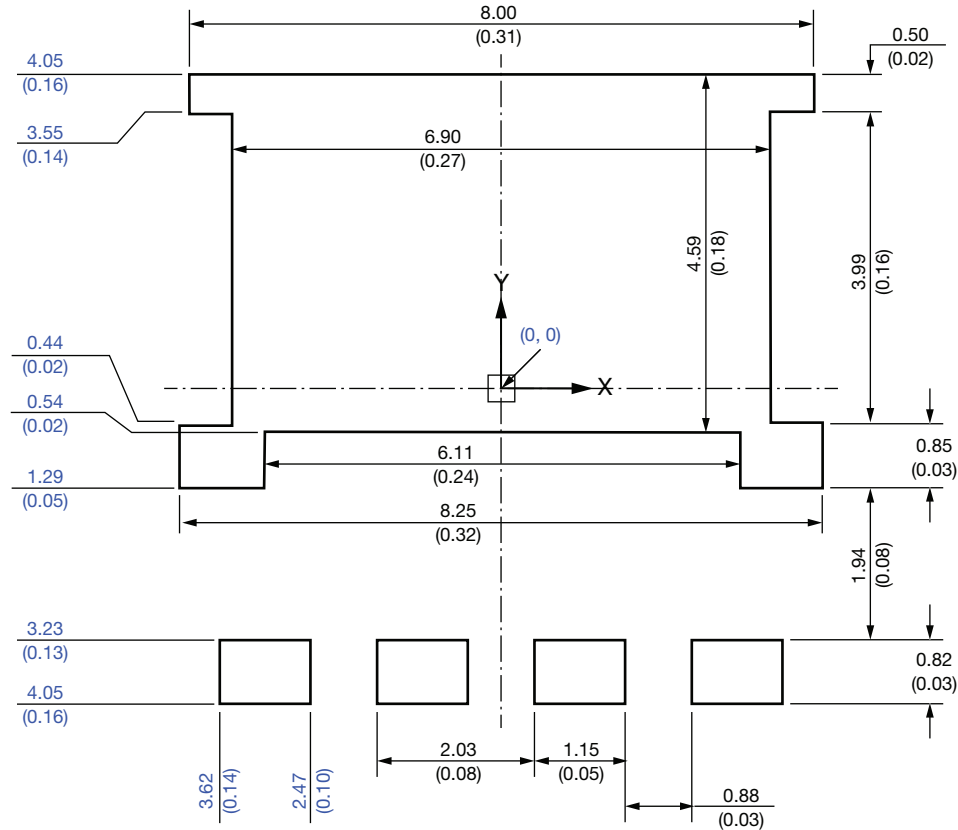


DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.70	1.80	1.90	0.067	0.071	0.075
A1	0.00	0.08	0.13	0.000	0.003	0.005
A3	0.55	0.62	0.70	0.022	0.024	0.028
b	0.92	1.00	1.08	0.036	0.039	0.043
b1	1.02	1.10	1.18	0.040	0.043	0.046
b2	7.80	7.90	8.00	0.307	0.311	0.315
c	0.20	0.25	0.30	0.008	0.010	0.012
D	8.00	8.10	8.25	0.315	0.319	0.325
D1	7.80	7.90	8.00	0.307	0.311	0.315
D2	6.70	6.80	6.90	0.264	0.268	0.272
D3	2.85	2.95	3.05	0.112	0.116	0.120
D4	6.11	6.21	6.31	0.241	0.244	0.248
e	1.95	2.00	2.05	0.077	0.079	0.081
E	7.90	8.00	8.10	0.311	0.315	0.319
E1	6.12	6.22	6.32	0.241	0.245	0.249
E2	3.94	4.04	4.14	0.140	0.159	0.163
E3	4.69	4.79	4.89	0.185	0.189	0.193
F	0.05	0.10	0.15	0.002	0.004	0.006
L	0.62	0.72	0.82	0.024	0.028	0.032
L1	0.92	1.07	1.22	0.036	0.042	0.048
K	0.80	0.90	1.00	0.031	0.035	0.039
W	0.30	0.40	0.50	0.012	0.016	0.020
W1	0.30	0.40	0.50	0.012	0.016	0.020
W2	4.39	4.49	4.59	0.173	0.177	0.181
W3	4.54	4.64	4.74	0.179	0.183	0.187
θ	6°	10°	14°	6°	10°	14°
θ1	0°	3°	8°	0°	3°	8°

C14-0891-Rev. A, 06-Oct-14
DWG: 6026



Recommended Minimum PADS for PowerPAK[®] 8 x 8L Single



Dimensions in millimeters (inches)

Note

- Linear dimensions are in black, the same information is provided in ordinate dimensions which are in blue.



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- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



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