

Ultra Low Power BLE 4.1 SoC

PRELIMINARY DATASHEET

Description

The SAM B11 is an ultra-low power Bluetooth® SMART (BLE 4.1) System on a Chip with Integrated MCU, Transceiver, Modem, MAC, PA, TR Switch, and Power Management Unit (PMU). It is a standalone Cortex®-M0 applications processor with embedded Flash memory and BLE connectivity.

The qualified Bluetooth Smart protocol stack is stored in dedicated ROM, the firmware includes L2CAP service layer protocols, Security Manager, Attribute protocol (ATT), Generic Attribute Profile (GATT) and the Generic Access Profile (GAP). Additionally, application profiles such as Proximity, Thermometer, Heart Rate, Blood Pressure, and many others are supported and included in the protocol stack.

Features

- Complies with Bluetooth® V4.1, ETSI EN 300 328 and EN 300 440 Class 2, FCC CFR47 Part 15 and ARIB STD-T66
- 2.4GHz transceiver and Modem
 - -96dBm/ -93dBm programmable receiver sensitivity
 - -20 to +4dBm programmable TX output power
 - Integrated T/R switch
 - Single wire antenna connection
- ARM® Cortex®-M0 32-bit processor
 - Single wire Debug (SWD) interface
 - 4-channel DMA controller
 - Brown out detector and Power On Reset
 - Watch Dog Timer
- Memory
 - 128kB embedded RAM (96kB available for application)
 - 128kB embedded ROM
 - 256kB Flash
- Hardware Security Accelerators
 - AES-128
 - SHA-256
- Peripherals
 - 23 digital and 3 wakeup GPIOs with 96kΩ internal pull-up resistors, 4 Mixed Signal GPIO
 - 2x SPI Master/Slave
 - 2x I²C Master/Slave and 1x I²C Slave
 - 2x UART
 - Three-axis quadrature decoder
 - 4x Pulse Width Modulation (PWM), 3 General Purpose Timers, and one Wakeup Timer
 - 4-channel 11-bit ADC

- Clock
 - Integrated 26MHz RC oscillator
 - 26MHz crystal oscillator
 - Integrated 2MHz sleep RC oscillator
 - 32.768kHz RTC crystal oscillator
- Ultra Low power
 - 1.1µA sleep current (8K RAM retention and RTC running)
 - 2.9mA peak TX current (0dBm, 3.6V)
 - 4.0mA peak RX current (3.6V, -93dBm sensitivity)
 - 9.7µA average advertisement current (3 channels, 1s interval)
- Integrated Power management
 - 2.3-4.3V battery voltage range (limited by Flash memory)
 - Fully integrated Buck DC/DC converter

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1 Ordering Information

Ordering Code	Package	Description
ATSAMB11G18A-MU-T	6x6mm QFN 48	SAM B11 Tape & Reel
ATSAMB11G18A-MU-Y	6x6mm QFN 48	SAM B11 Tray

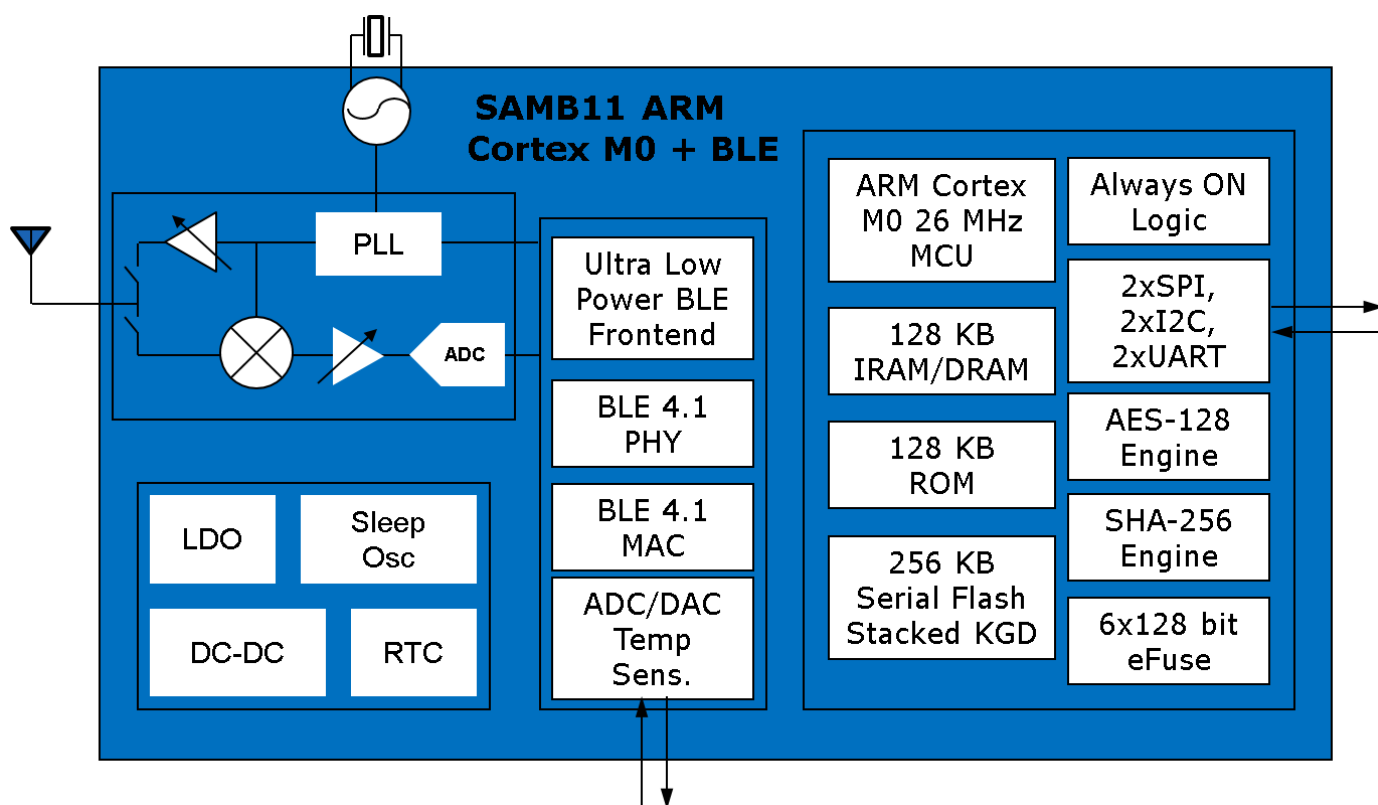
2 Package Information

Table 2-1. SAM B11 6x6 QFN 48 Package Information

Parameter	Value	Units	Tolerance
Package Size	6x6	mm	± 0.1 mm
QFN Pad Count	48		
Total Thickness	0.85	mm	+0.15 /- 0.05mm
QFN Pad Pitch	0.4		
Pad Width	0.2		
Exposed Pad size	4.2x4.2		

3 Block Diagram

Figure 3-1. SAM B11 Block Diagram



4 Pinout Information

SAM B11 is offered in an exposed pad 48-pin QFN package. This package has an exposed paddle that must be connected to the system board ground. The QFN package pin assignment is shown in [Figure 4-1](#). The color shading is used to indicate the pin type as follows:

- Red – analog
- Green – digital I/O (switchable power domain)
- Blue – digital I/O (always-on power domain)
- Yellow – digital I/O power
- Purple – PMU
- Shaded green/red – configurable mixed-signal GPIO (digital/analog)

The SAM B11 pins are described in [Table 4-1](#).

Figure 4-1. SAM B11 Pin Assignment

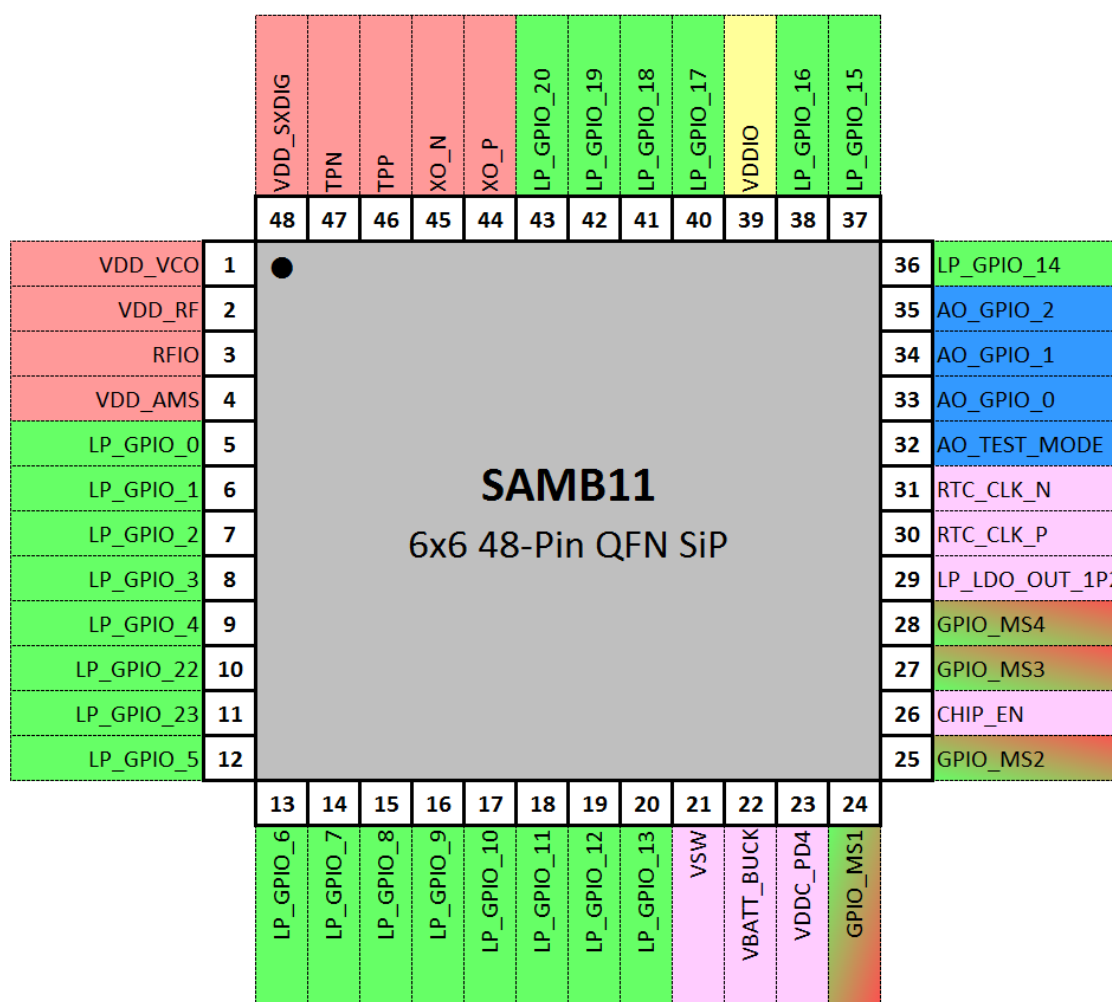


Table 4-1. SAM B11 Pin Description with Default Peripheral Mapping

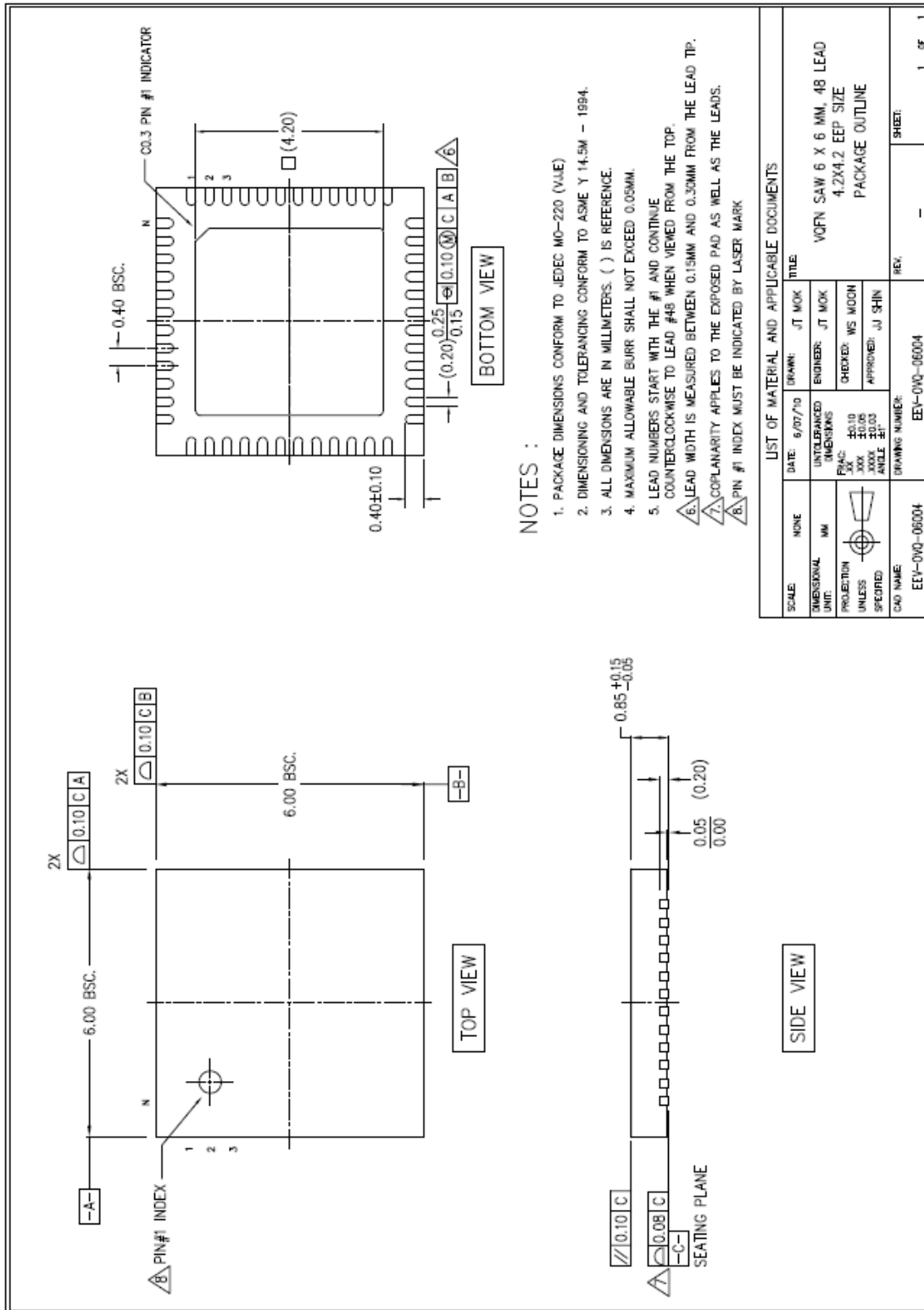
Pin #	Pin Name	Pin Type	Description / Default Function
1	VDD_VCO	Analog/RF	RF Supply 1.2V
2	VDD_RF	Analog/RF	RF Supply 1.2V
3	RFIO	Analog/RF	Rx input and Tx output
4	VDD_AMS	Analog/RF	AMS Supply 1.2V
5	LP_GPIO_0	Digital I/O	SWD Clock
6	LP_GPIO_1	Digital I/O	SWD I/O
7	LP_GPIO_2	Digital I/O	UART1 RXD
8	LP_GPIO_3	Digital I/O	UART1 TXD
9	LP_GPIO_4	Digital I/O	UART1 CTS
10	LP_GPIO_22	Digital I/O	GPIO
11	LP_GPIO_23	Digital I/O	GPIO
12	LP_GPIO_5	Digital I/O	UART1 RTS
13	LP_GPIO_6	Digital I/O	UART2 RXD
14	LP_GPIO_7	Digital I/O	UART2 TXD
15	LP_GPIO_8	Digital I/O	I2C0 SDA (high-drive pad, see Table 13-3)
16	LP_GPIO_9	Digital I/O	I2C0 SCL (high-drive pad, see Table 13-3)
17	LP_GPIO_10	Digital I/O	SPI0 SCK
18	LP_GPIO_11	Digital I/O	SPI0 MOSI
19	LP_GPIO_12	Digital I/O	SPI0 SSN
20	LP_GPIO_13	Digital I/O	SPI0 MISO
21	VSW	PMU	DC/DC Converter Switching Node
22	VBATT_BUCK	PMU	DC/DC Converter Supply & General Battery Connection
23	VDDC_PD4	PMU	DC/DC Converter 1.2V output and feedback node
24	GPIO_MS1	Mixed Signal I/O	Configurable to be a GPIO Mixed Signal only (ADC interface)
25	GPIO_MS2	Mixed Signal I/O	Configurable to be a GPIO Mixed Signal only (ADC interface)
26	CHIP_EN	PMU	Master Enable for chip
27	GPIO_MS3	Mixed Signal I/O	Configurable to be a GPIO Mixed Signal only (ADC interface)
28	GPIO_MS4	Mixed Signal I/O	Configurable to be a GPIO Mixed Signal only (ADC interface)
29	LP_LDO_OUT_1P2	PMU	Low Power LDO output (connect to 1uF decoupling cap)
30	RTC_CLK_P	PMU	RTC terminal + / 32.768kHz Xtal +
31	RTC_CLK_N	PMU	RTC terminal - / 32.768kHz Xtal +
32	AO_TEST_MODE	Digital Input	Test Mode Selection (SCAN ATE) /GND for normal operation
33	AO_GPIO_0	Digital I/O	Always On External Wakeup
34	AO_GPIO_1	Digital I/O	Always On External Wakeup
35	AO_GPIO_2	Digital I/O	Always On External Wakeup
36	LP_GPIO_14	Digital I/O	UART2 CTS

Pin #	Pin Name	Pin Type	Description / Default Function
37	LP_GPIO_15	Digital I/O	UART2 RTS
38	LP_GPIO_16	Digital I/O	GPIO
39	VDDIO	I/O Power	I/O Supply, can be less than or equal to VBATT_BUCK
40	LP_GPIO_17	Digital I/O	GPIO
41	LP_GPIO_18	Digital I/O	GPIO
42	LP_GPIO_19	Digital I/O	GPIO
43	LP_GPIO_20	Digital I/O	GPIO
44	XO_P	Analog/RF	XO Crystal +
45	XO_N	Analog/RF	XO Crystal -
46	TPP	Analog/RF	Test Mux + output
47	TPN	Analog/RF	Test Mux – output
48	VDD_SXDIG	Analog/RF	RF Supply 1.2V

5 Package drawing

The SAM B11 QFN package is RoHS/green compliant.

Figure 5-1. SAM B11 6x6 QFN 48 Package Outline Drawing



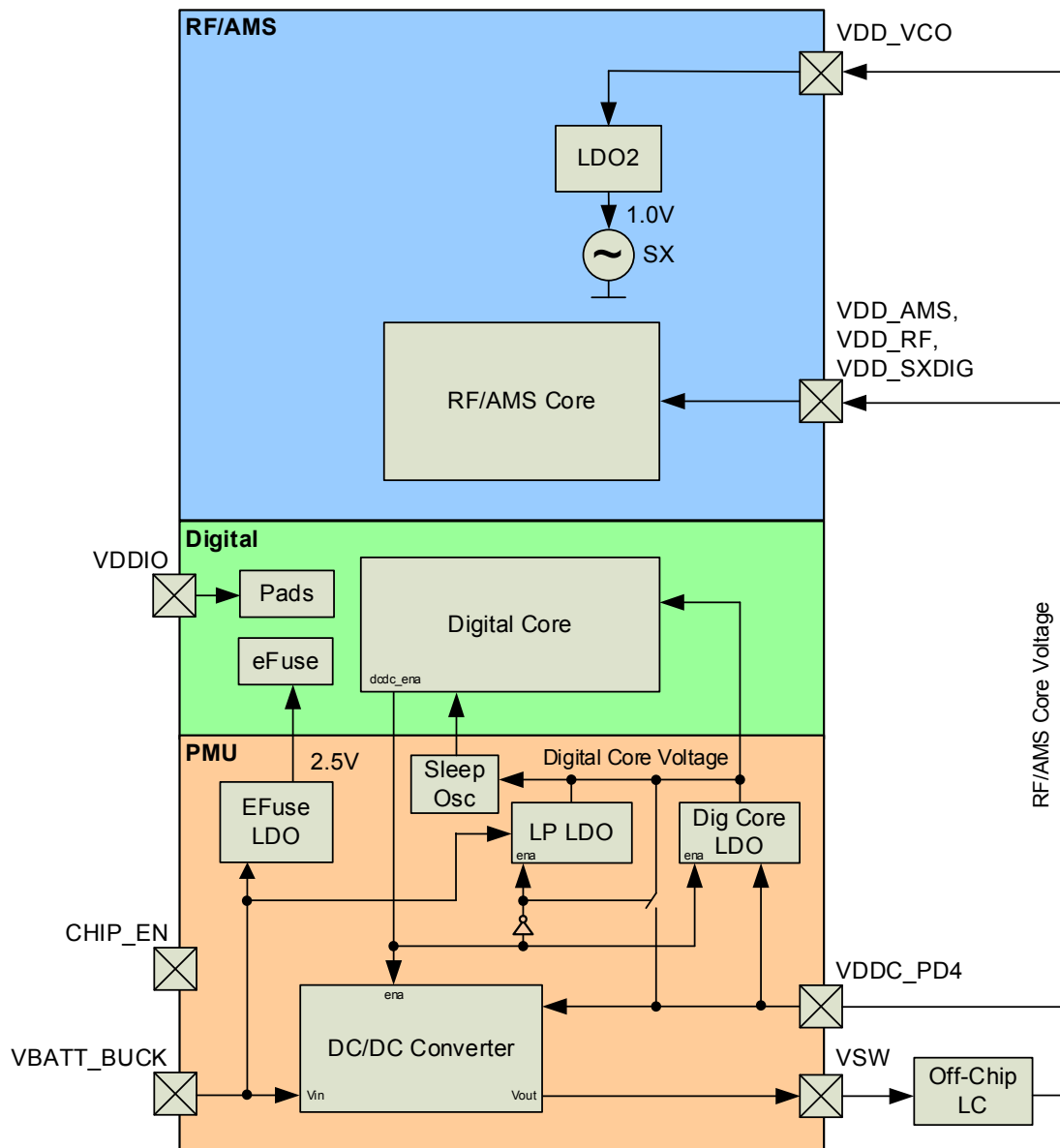
6 Power Management

6.1 Power Architecture

SAM B11 uses an innovative power architecture to eliminate the need for external regulators and reduce the number of off-chip components. The integrated power management block includes a DC/DC buck converter and separate Low Drop out (LDO) regulators for different power domains. The DCDC buck converter converts battery voltage to a lower internal voltage for the different circuit blocks and does this with high efficiency. The DCDC requires three external components for proper operation (two inductors L 4.7 μ H and 9.1nH, and one capacitor C 4.7 μ F).

The stacked Flash has a supply pin that is internally connected to the VDDIO pin.

Figure 6-1. SAM B11 Power Architecture



6.2 DC/DC Converter

The DC/DC Converter is intended to supply current to the BLE digital core and the RF transceiver core. The DC/DC consists of a power switch, 26MHz RC oscillator, controller, external inductor, and external capacitor. The DCDC is utilizing pulse skipping discontinuous mode as its control scheme. The DC/DC specifications are shown in the following tables and charts.

Table 6-1. DC/DC Converter Specifications (performance is guaranteed for 4.7μF L and 4.7μF C)

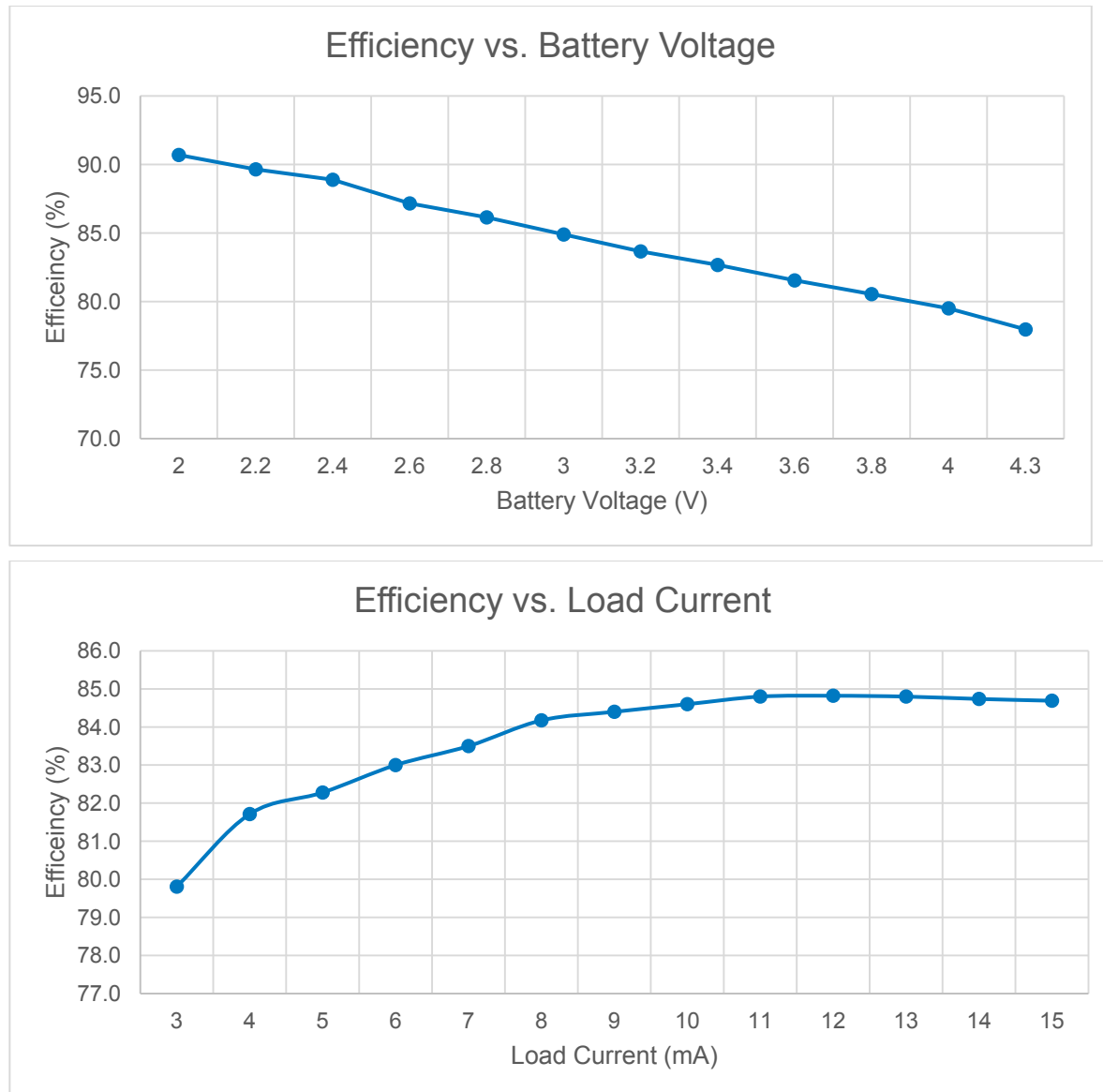
Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Output current capability	I_{REG}	0	10	30	mA	Dependent on external component values and DC/DC settings with acceptable efficiency
External capacitor range	C_{EXT}	2	4.7	20	μF	External capacitance range
External inductor range	L_{EXT}	2	4.7	10	μH	External inductance range
Battery voltage	V_{BAT}	1.8	3	4.3	V	Functionality and stability given
Output voltage range	V_{REG}	1.05	1.2	1.47		25 mV step size
Current consumption	I_{DD}		125		μA	DC/DC quiescent current
Startup time	$t_{startup}$	20		600	μs	Dependent on external component values and DC/DC settings
Voltage ripple	ΔV_{REG}	5	10	30	mV	Dependent on external component values and DC/DC settings
Efficiency	η		85		%	Measured at 3V VBATT, at load of 10mA
Overshoot at startup	V_{OS}		0		mV	No overshoot, no output pre-charge
Line Regulation	ΔV_{REG}		10			From 1.8 - 4.3V
Load regulation	ΔV_{REG}		5			From 0 - 10mA

Table 6-2. DC/DC Converter Allowable Onboard Inductor and Capacitor Values (VBATT=3V)

Inductor (μH)	Efficiency (%)	Vripple (mV)			Rx Sensitivity* (dBm)
		C=1uF	C=2.2uF	C=4.7uF	
1	81	13	7	3	~2.5 dB degrade
2.2	83	13	7	3	~1.5 dB degrade
4.7	85	17	9	5	~0.7 dB degrade

Note: Degradation relative to design powered by external LDO and DC/DC disabled.

Figure 6-2. DC/DC Converter Efficiency



6.3 Power Consumption

6.3.1 Description of Device States

SAM B11 has multiple device states, depending on the state of the ARM processor and BLE subsystem.

Note: The ARM is required to be powered on if the BLE subsystem is active.

- BLE_On_Transmit – Device is actively transmitting a BLE signal (Application may or may not be active)
- BLE_On_Receive – Device is actively receiving a BLE signal (Application may or may not be active)
- MCU_Only – Device has ARM processor powered on and BLE subsystem powered down
- Ultra_Low_Power – BLE is powered down and Application is powered down (with or without RAM retention)
- Power_Down – Device core supply off

6.3.2 Controlling the Device States

The following pins are used to switch between the main device states:

- CHIP_EN – used to enable PMU
- VDDIO – I/O supply voltage from external supply

In Power_Down state, VDDIO is on and CHIP_EN is low (at GND level). To switch between Power_Down state and MCU_Only state CHIP_EN has to change between low and high (VDDIO voltage level). Once the device is MCU_Only state, all other state transitions are controlled entirely by software. When VDDIO is off and CHIP_EN is low, the chip is powered off with no leakage.

When no power is supplied to the device (the DC/DC Converter output and VDDIO are both off and at ground potential), a voltage cannot be applied to the SAM B11 pins because each pin contains an ESD diode from the pin to supply. This diode will turn on when voltage higher than one diode-drop is supplied to the pin.

If a voltage must be applied to the signal pads while the chip is in a low power state, the VDDIO supply must be on, so the Power_Down state must be used. Similarly, to prevent the pin-to-ground diode from turning on, do not apply a voltage that is more than one diode-drop below ground to any pin.

6.3.3 Current Consumption in Various Device States

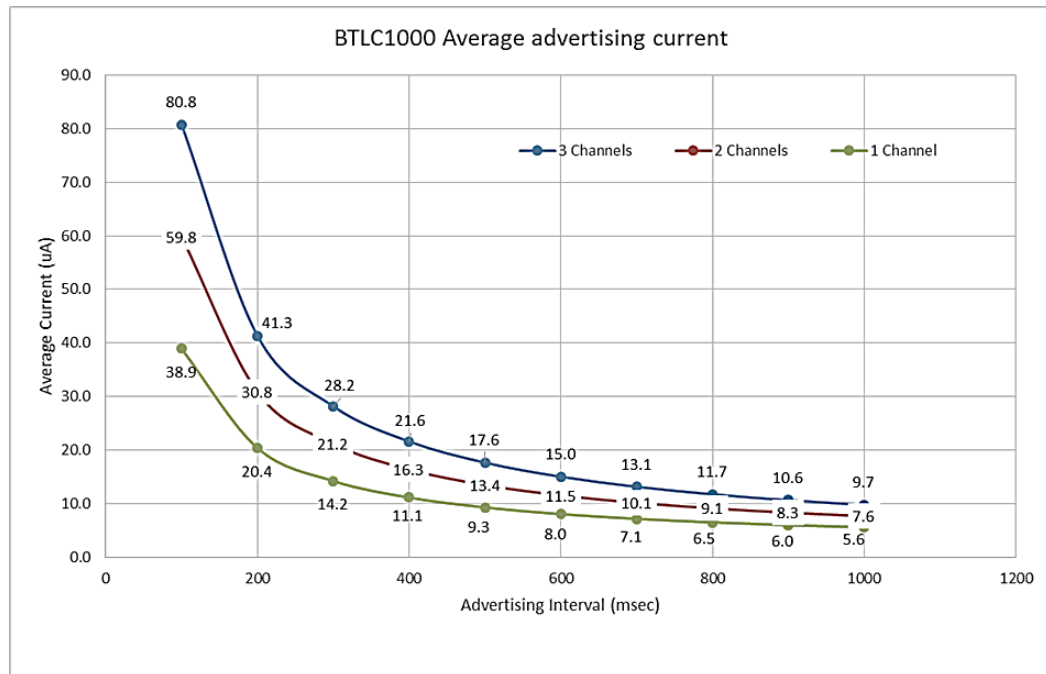
Table 6-3. SAM B11 Device Current Consumption at VBATT=3.6V

Condition	Min	Typ	Max	Unit
Power_Down		50		nA
Ultra_Low_Power Standby		900		
Ultra_Low_Power with 8KB retention, BLE timer, no RTC ¹		1.1		μA
Ultra_Low_Power with 8KB retention, BLE timer, with RTC ²		1.25		
MCU_Only, idle (waiting for interrupt)		0.85		mA
BLE_On_Receive		4.0		
BLE_On_Transmit, 0dBm output power		2.9		
BLE_On_Transmit, 3.5dBm output power		3.7		

¹ Sleep clock derived from internal 32kHz RC oscillator

² Sleep clock derived from external crystal

Figure 6-3. SAM B11 Average Advertising Current



6.4 Power-Up Sequence

The power-up sequence for SAM B11 is shown in Figure 6-4. The timing parameters are provided in Table 6-4.

Figure 6-4. SAM B11 Power-Up Sequence

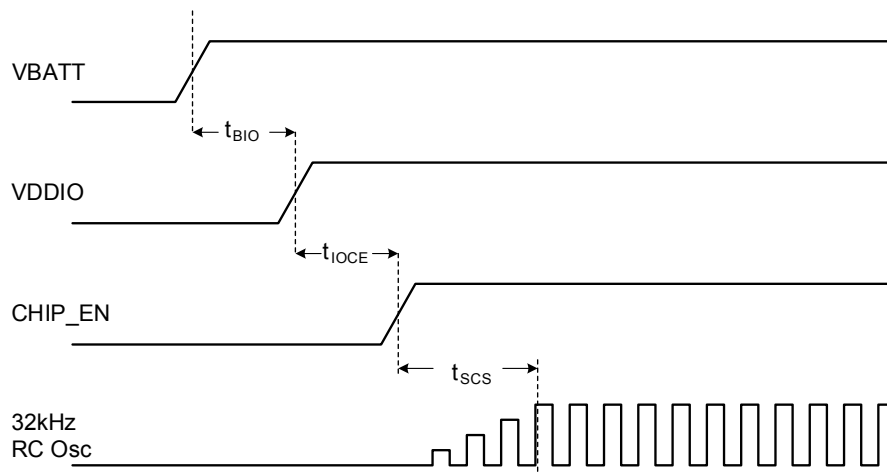


Table 6-4. SAM B11 Power-Up Sequence Timing

Parameter	Min.	Max.	Units	Description	Notes
t_{BIO}	0		ms	VBATT rise to VDDIO rise	VBATT and VDDIO can rise simultaneously or can be tied together.
t_{IOCE}	0			VDDIO rise to CHIP_EN rise	CHIP_EN must not rise before VDDIO. CHIP_EN must be driven high or low, not left floating.

Parameter	Min.	Max.	Units	Description	Notes
t _{scs}	10		μs	CHIP_EN rise to 31.25kHz (2MHz/64) oscillator stabilizing	

6.5 Power On Reset (POR) and Brown Out Detector (BOD)

The SAM B11 has a POR circuit for proper system power bring up and a brown out detector to reset the system's operation when a drop in battery voltage is detected.

- POR is a power on reset circuit that outputs a HI logic value when the VBATT_BUCK is below a voltage threshold. The POR output becomes a LO logic value when the VBATT_BUCK is above a voltage threshold.
- BOD is a brown out detector that outputs a HI logic value when the bandgap reference (BGR) voltage falls below a programmable voltage threshold. When the bandgap voltage reference voltage level is restored above a voltage threshold, the BOD output becomes a LO logic value.
- The counter creates a pulse that is HI for $256 \cdot (64 \cdot T_{2MHz}) \sim 8.2ms$

The system block diagram and timing are illustrated in [Figure 6-5](#) and [Figure 6-6](#).

Figure 6-5. SAM B11 POR and BOD Block Diagram

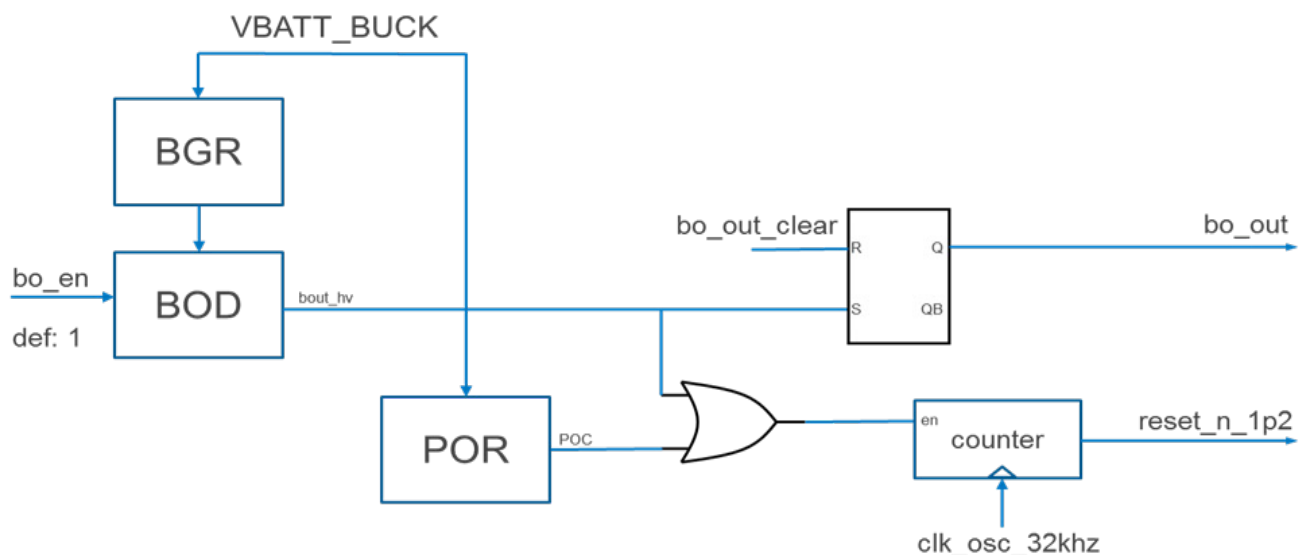
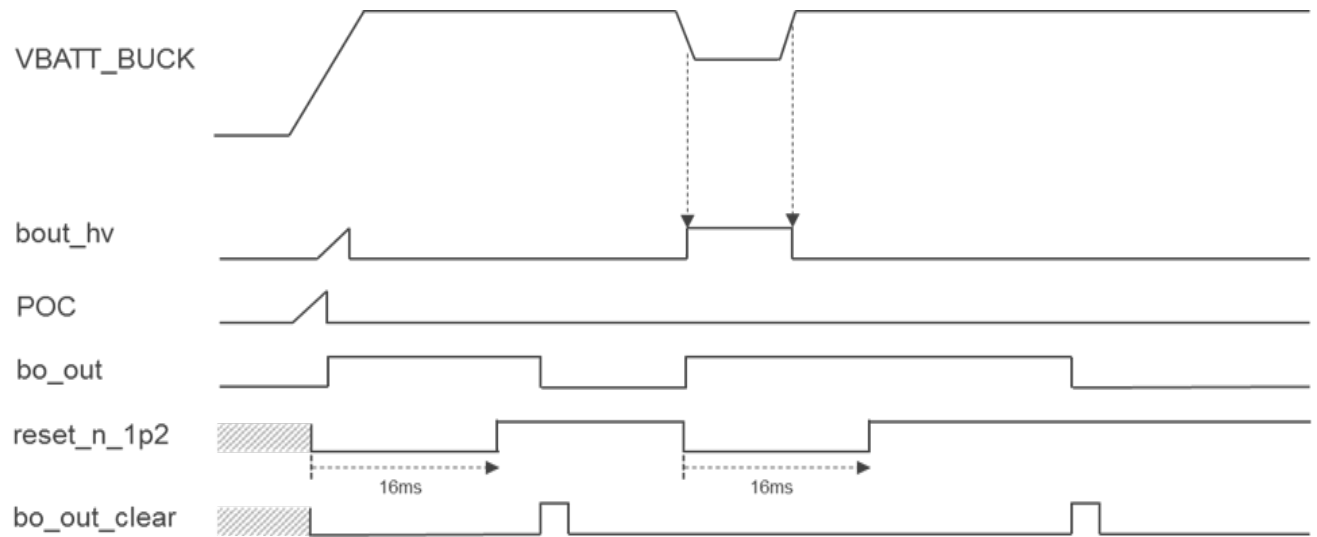


Figure 6-6. SAM B11 POR and BOD Timing Sequence



7 Clocking

7.1 Overview

Figure 7-1. SAM B11 Clock Architecture

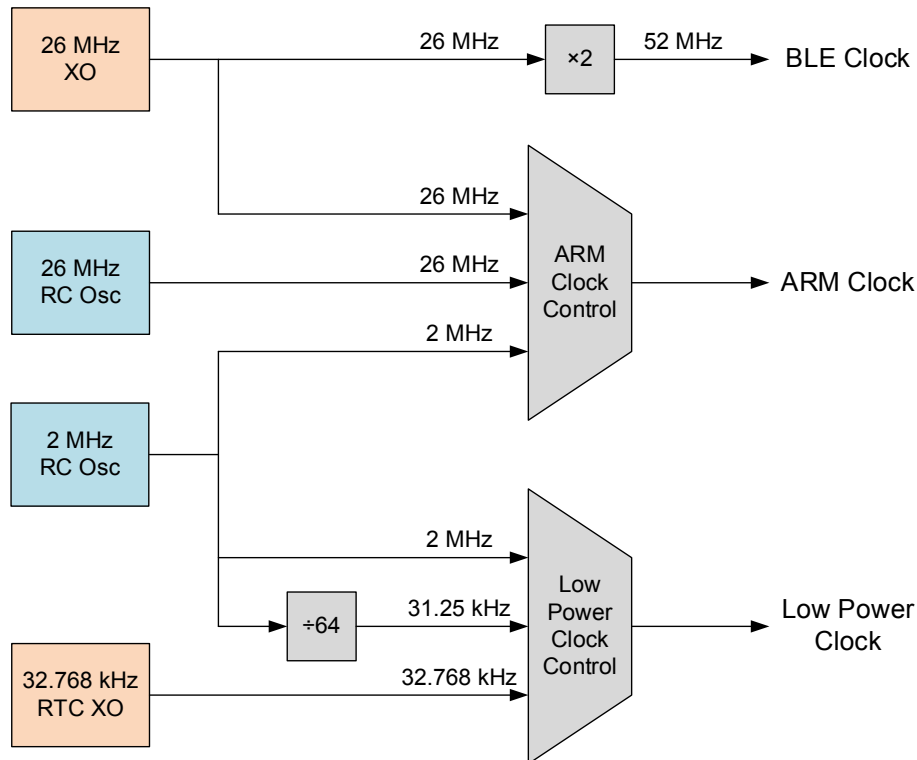


Figure 7-1 provides an overview of the clock tree and clock management blocks.

The BLE Clock is used to drive the BLE subsystem. The ARM clock is used to drive the Cortex-M0 MCU and its interfaces (UART, SPI, and I²C), the nominal MCU clock speed is 26MHz. The Low Power Clock is used to drive all the low power applications like BLE sleep timer, always-on power sequencer, always-on timer, and others.

The 26MHz Crystal Oscillator (XO) must be used for the BLE operations or in the event a very accurate clock is required for the ARM subsystem operations.

The 26MHz integrated RC Oscillator is used for most general purpose operations on the MCU and its peripherals. In cases when the BLE subsystem is not used, the RC oscillator can be used for lower power consumption. The frequency variation of this RC oscillator is up to $\pm 40\%$ over process, voltage, and temperature.

The 2MHz integrated RC Oscillator can be used as the Low Power Clock for applications that require fast wakeup of the ARM or for generating a ~ 31.25 kHz clock for slower wakeup but lowest power in sleep mode. This 2MHz oscillator can also be used as the ARM Clock for low-power applications where the MCU needs to remain on but run at a reduced clock speed. The frequency variation of this RC oscillator is up to $\pm 40\%$ over process, voltage, and temperature.

The 32.768kHz RTC Crystal Oscillator (RTC XO) is recommended to be used for BLE operations (although optional) as it will reduce power consumption by providing the best timing for wakeup precision, allowing circuits to be in low power sleep mode for as long as possible until they need to wake up and connect during the BLE connection event. The ~ 31.25 kHz clock derived from the 2MHz integrated RC Oscillator can be used instead of RTC XO but it has low accuracy over process, voltage and temperature variations (up to $\pm 40\%$) and thus needs to

be frequently calibrated to within $\pm 500\text{ppm}$ if the RC oscillator is used for BLE timing during a connection event. Because this clock is less accurate than RTC XO, it will require waking up earlier to prepare for a connection event and this will increase the average power consumption. Calibration of the RC Oscillator is described in the application note.

7.2 26MHz Crystal Oscillator (XO)

Table 7-1. SAM B11 26MHz Crystal Oscillator Parameters

Parameter	Min	Typ	Max	Units
Crystal Resonant Frequency	N/A	26	N/A	MHz
Crystal Equivalent Series Resistance		50	150	Ω
Stability - Initial Offset*	-50		50	ppm
Stability - Temperature and Aging	-40		40	ppm

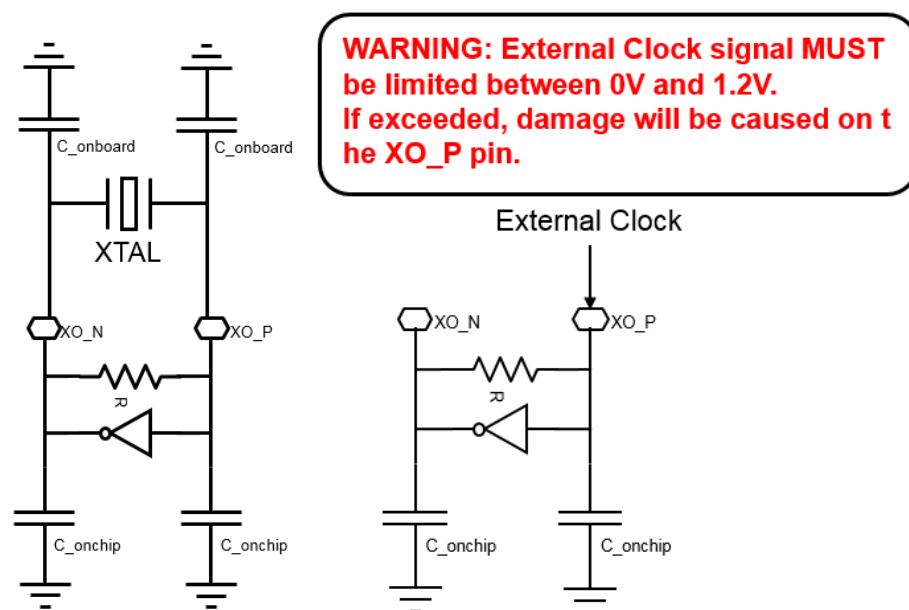
Note: * Initial offset must be calibrated to maintain $\pm 25\text{ppm}$ in all operating conditions. This calibration is performed during final production testing and calibration offset values are stored in eFuse. More details are provided in the calibration application note.

The block diagram in [Figure 7-2](#) (a) shows how the internal Crystal Oscillator (XO) is connected to the external crystal.

The XO has up to 10pF internal capacitance on each terminal XO_P and XO_N (programmable in steps of 1.25pF). To bypass the crystal oscillator, an external Signal capable of driving 10pF can be applied to the XO_P terminal as shown in [Figure 7-2](#)(b).

The needed external bypass capacitors depend on the chosen crystal characteristics. Please refer to the datasheet of the preferred crystal and take into account the on chip capacitance. When bypassing XO_P from an external clock, XO_N is required to be floating.

Figure 7-2. SAM B11 Connections to XO



(a) Crystal oscillator is used

(b) crystal oscillator is bypassed

Table 7-2. SAM B11 26MHz XTAL C_onchip programming

Register	Cl_onchip	[pF]
rx_xo_regs[7,6,15] = 000	1.00	
rx_xo_regs[7,6,15] = 001	2.25	
rx_xo_regs[7,6,15] = 010	3.50	
rx_xo_regs[7,6,15] = 011	4.75	
rx_xo_regs[7,6,15] = 100	6.00	
rx_xo_regs[7,6,15] = 101	7.25	
rx_xo_regs[7,6,15] = 110	8.50	
rx_xo_regs[7,6,15] = 111	9.75	
If rx_reg7[1] = 1 add 5pF to above value		

Table 7-3 specifies the electrical and performance requirements for the external clock.

Table 7-3. SAM B11 Bypass Clock Specification

Parameter	Min.	Max.	Unit	Comments
Oscillation frequency	26	26	MHz	Must be able to drive 5pF load @ desired frequency
Voltage swing	0.75	1.2	Vpp	
Stability – Temperature and Aging	-25	+25	ppm	
Phase Noise		-130	dBc/Hz	At 10kHz offset
Jitter (RMS)		<1psec		Based on integrated phase noise spectrum from 1kHz to 1MHz

7.3 32.768kHz RTC Crystal Oscillator (RTC XO)

7.3.1 General Information

SAM B11 has a 32.768 kHz RTC oscillator that is preferably used for BLE activities involving connection events. To be compliant with the BLE specifications for connection events, the frequency accuracy of this clock has to be within ± 500 ppm. Because of the high accuracy of the 32.768kHz crystal oscillator clock, the power consumption can be minimized by leaving radio circuits in low power sleep mode for as long as possible until they need to wake up for the next connection timed event.

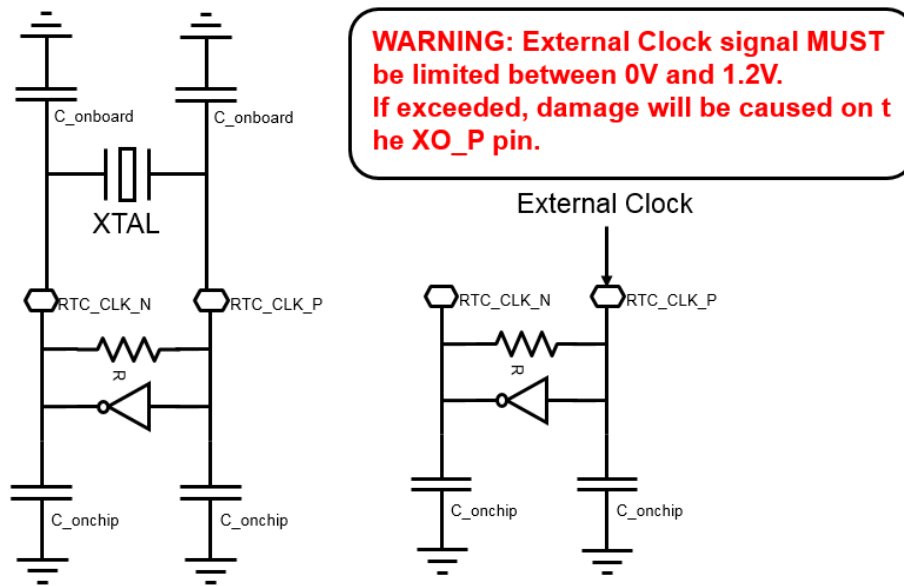
The block diagram in Figure 7-3 (a) shows how the internal low frequency Crystal Oscillator (XO) is connected to the external crystal.

The RTC XO has a programmable internal capacitance with a maximum of 15pF on each terminal, RTC_CLK_P and RTC_CLK_N. When bypassing the crystal oscillator with an external signal, one can program down the internal capacitance to its minimum value (~ 1 pF) for easier driving capability. The driving signal can be applied to the RTC_CLK_P terminal as shown in Figure 7-3 (b).

The needed external bypass capacitors depend on the chosen crystal characteristics. Please refer to the datasheet of the preferred crystal and take into account the on chip capacitance.

When bypassing RTC_CLK_P from an external clock, RTC_CLK_N is required to be floating.

Figure 7-3. SAM B11 Connections to RTC XO



(a) Crystal oscillator is used (b) Crystal oscillator is bypassed

Table 7-4. 32.768kHz XTAL C_onchip programming

Register: pierce_cap_ctrl[3:0]	Cl_onchip	[pF]
0000	0.0	
0001	1.0	
0010	2.0	
0011	3.0	
0100	4.0	
0101	5.0	
0110	6.0	
0111	7.0	
1000	8.0	
1001	9.0	
1010	10.0	
1011	11.0	
1100	12.0	
1101	13.0	
1110	14.0	
1111	15.0	

7.3.2 RTC XO Design and Interface Specification

The RTC consists of 2 main blocks: The Programmable Gm stage and tuning capacitors. The programmable Gm stage is used to maintain a phase shift of 360° with the motional arm and keep total negative resistance to sustain oscillation. Tuning capacitors are used to adjust the XO center frequency and control the XO precision for different crystal models. The output of the XO is driven to the digital domain via a digital buffer stage with supply voltage of 1.2V.

Table 7-5. RTC XO Interface

Pin Name	Function	Register Default
Digital Control Pins		
Pierce_res_ctrl	Control feedback resistance value: 0 = 20MΩ Feedback resistance 1 = 30MΩ Feedback resistance	0X4000F404<15>='1'
Pierce_cap_ctrl<3:0>	Control the internal tuning capacitors with step of 700fF: 0000=700fF 1111=11.2pF Refer to crystal datasheet to check for optimum tuning cap value	0X4000F404<23:20>="1000"
Pierce_gm_ctrl<3:0>	Controls the Gm stage gain for different crystal mode: 0011= for crystal with shunt cap of 1.2pF 1000= for crystal with shunt cap >3pF	0X4000F404<19:16>="1000"
Supply Pins		
VDD_XO	1.2V	

7.3.3 RTC Characterization with Gm Code Variation at Supply 1.2V and Temp=25°C

This section shows the RTC total drawn current and the XO accuracy versus different tuning capacitors and different GM codes, at supply voltage of 1.2V and temp=25°C.

Figure 7-4. RTC Drawn Current vs Tuning Caps at 25°C

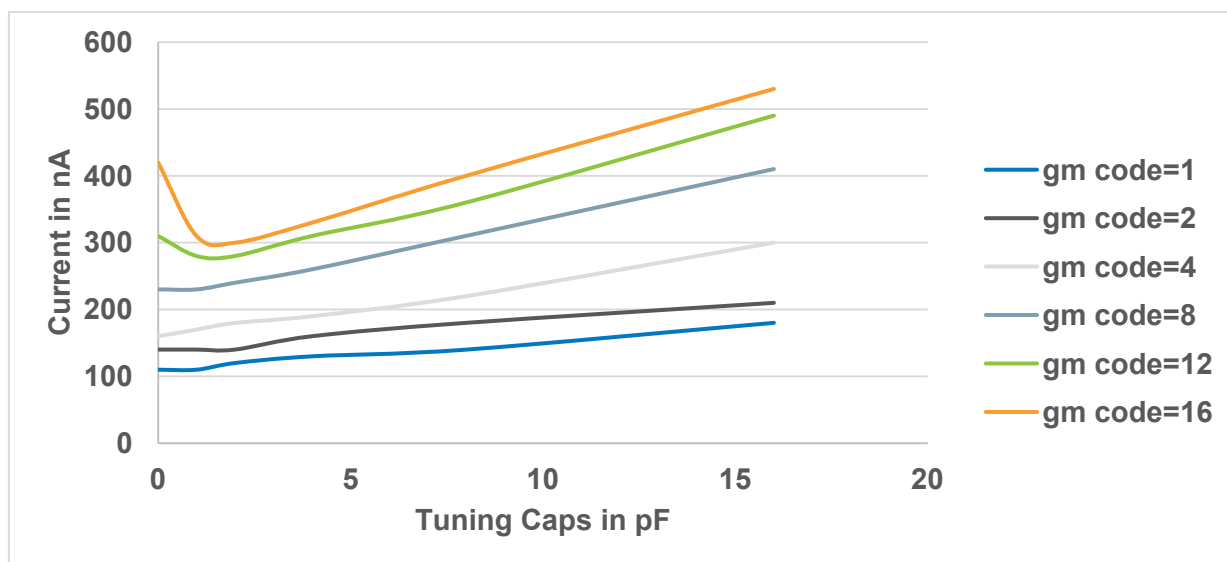
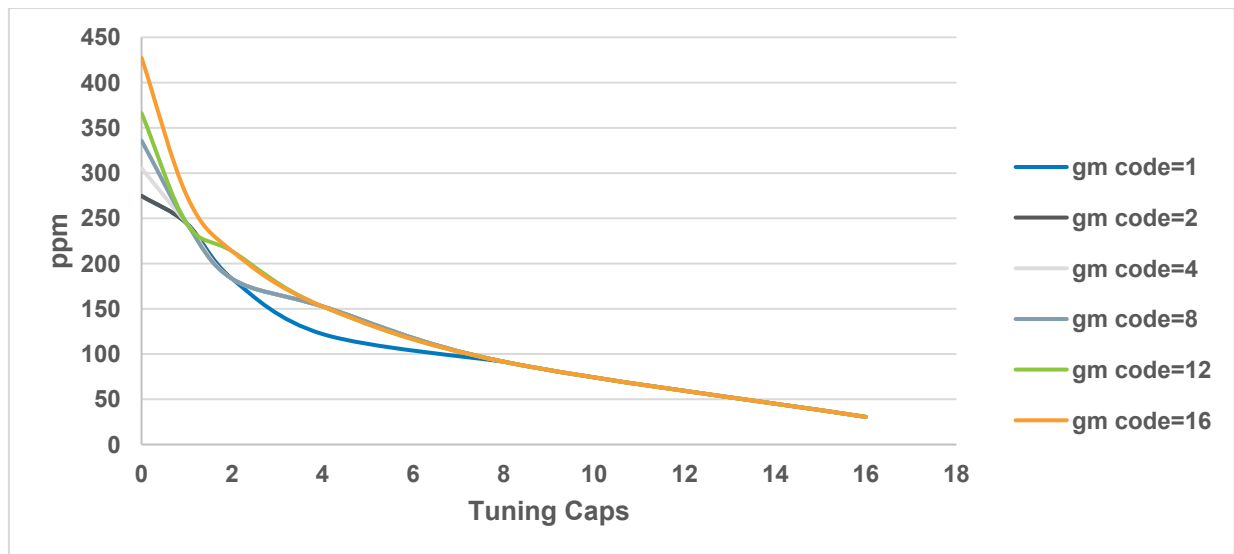


Figure 7-5. RTC Oscillation Frequency Deviation vs Tuning Caps at 25°C



7.3.4 RTC Characterization with Supply Variation and Temp=25°C

Figure 7-6. RTC Drawn Current vs Supply variation

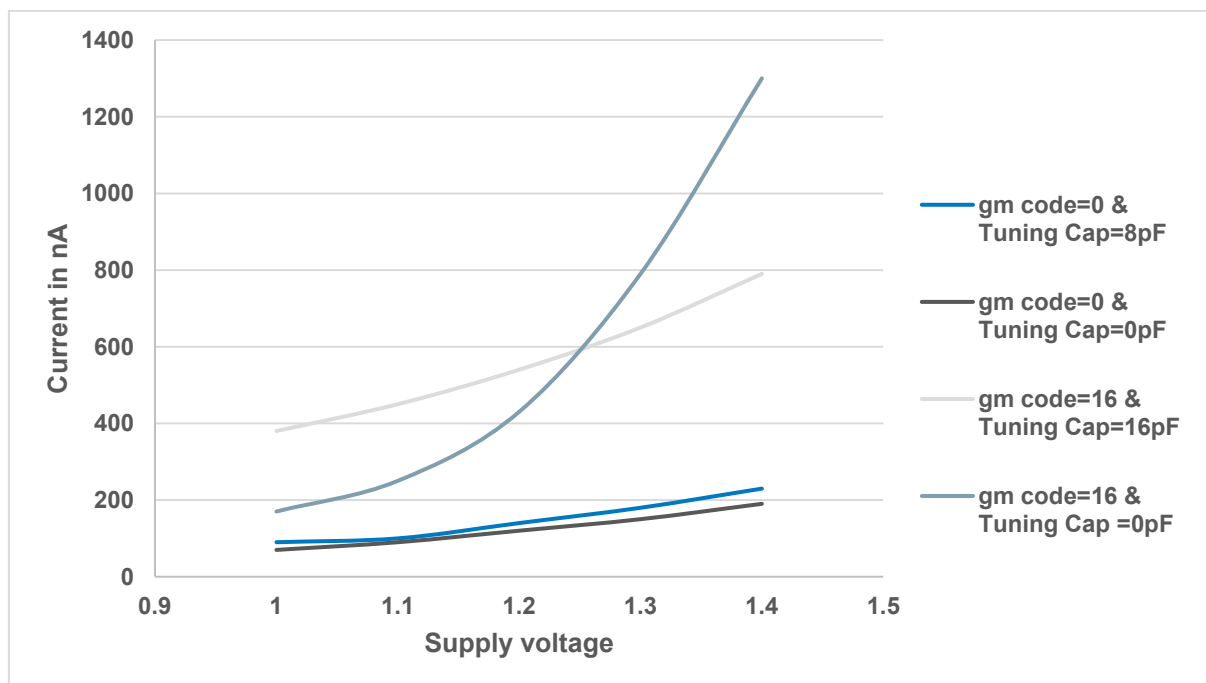
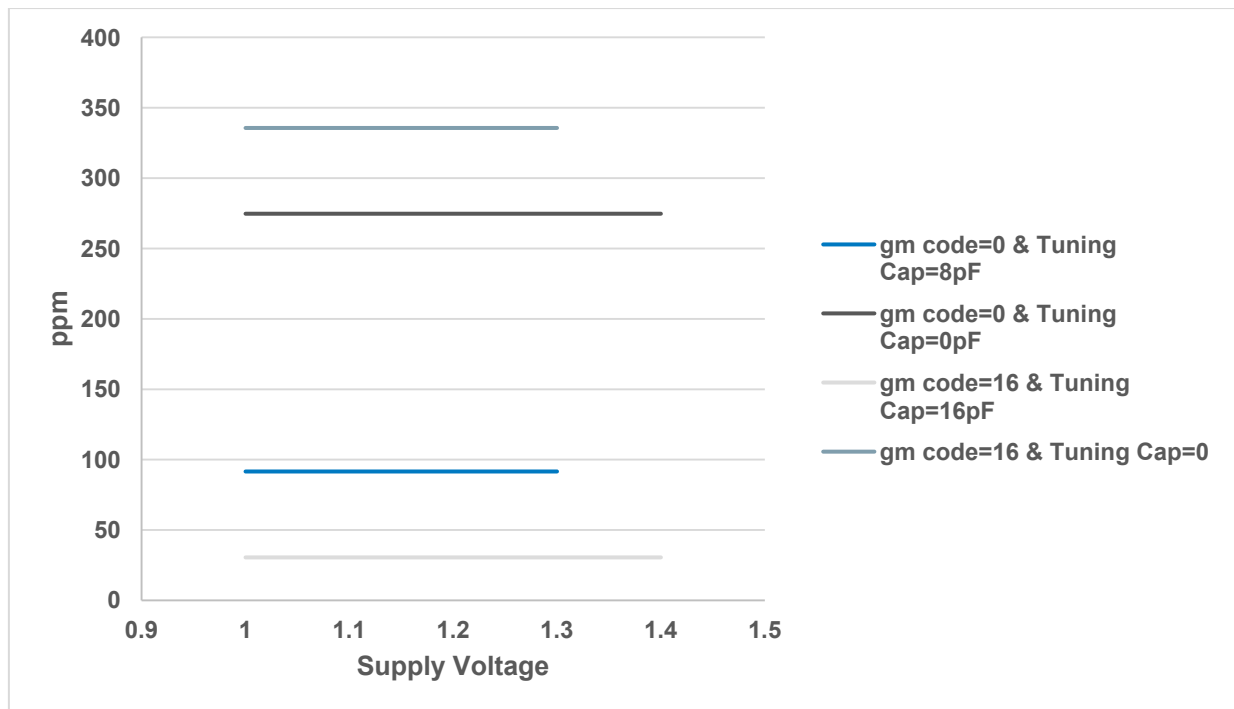


Figure 7-7. RTC Frequency Deviation vs Supply Voltage



7.4 2MHz and 26MHz Integrated RC Oscillator

The 2MHz integrated RC Oscillator circuit without calibration has a frequency variation of 40% over process, temperature and voltage variation. The ~31.25kHz clock is derived from the 2MHz clock by dividing by 64 and provides for lowest sleep power mode with a real time clock running. As described above, calibration over process, temperature and voltage is required to maintain the accuracy of this clock.

Figure 7-8. 32kHz RC Oscillator PPM Variation vs. Calibration Time at Room Temperature

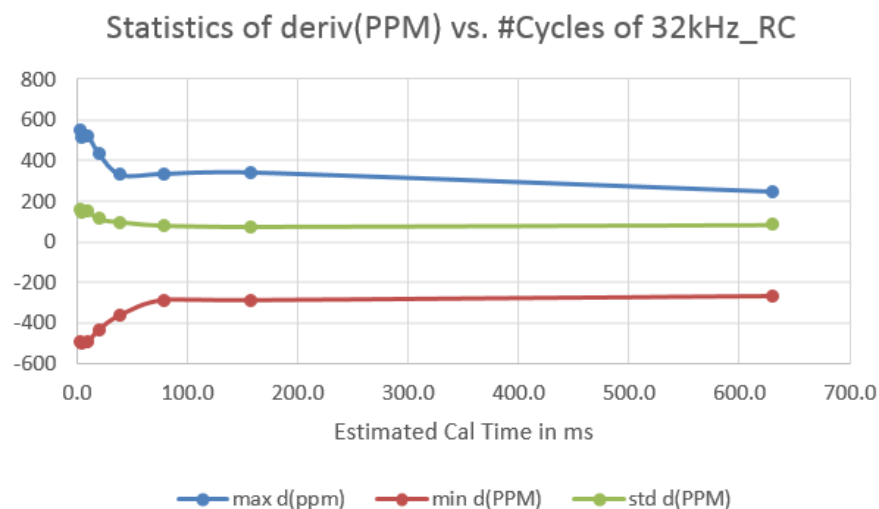
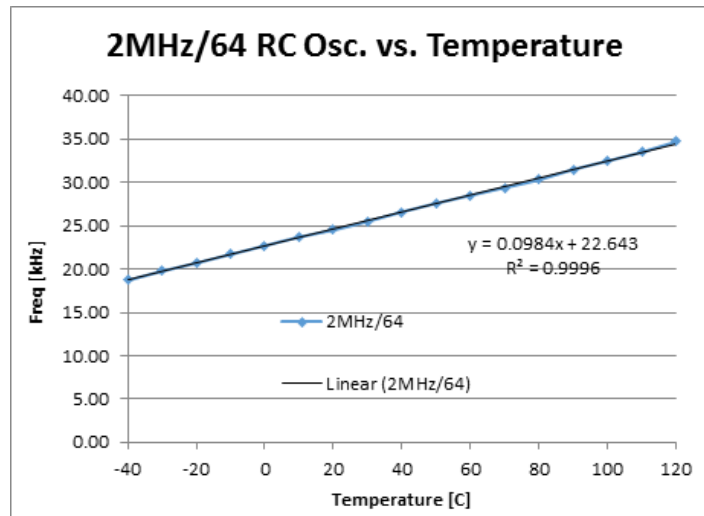


Figure 7-9. 32kHz RC Oscillator Frequency Variation over Temperature



The 26MHz integrated RC Oscillator circuit has a frequency variation of 40% over process, temperature, and voltage variation.

8 CPU and Memory Subsystem

8.1 ARM Subsystem

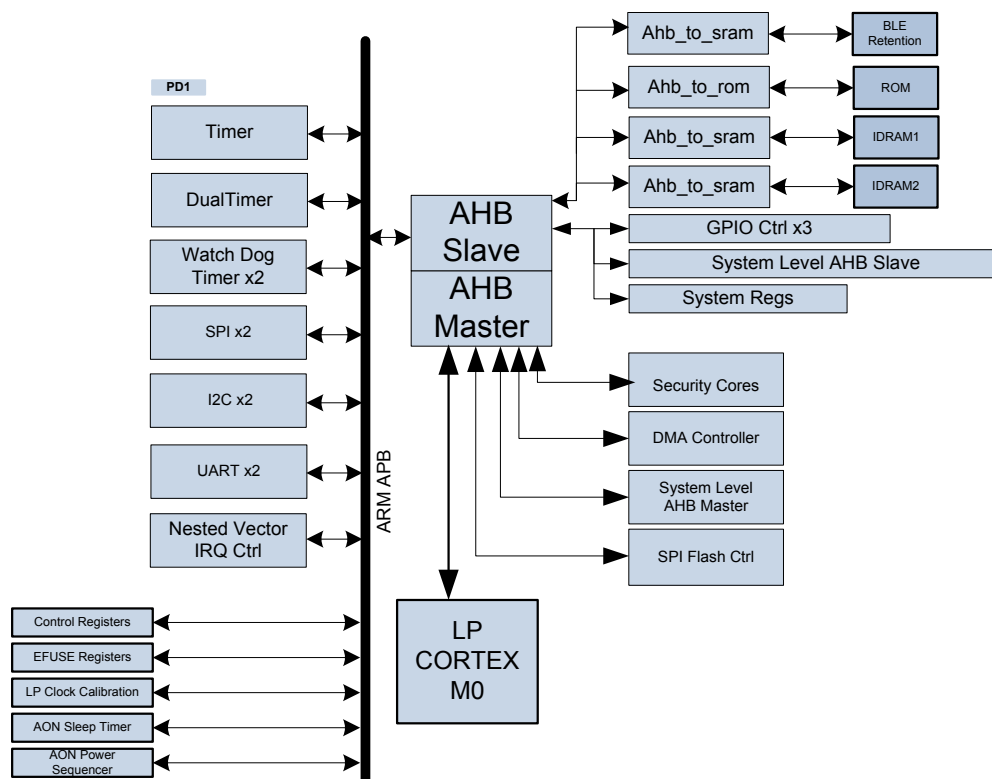
SAM B11 has an ARM Cortex-M0 32-bit processor. It is responsible for controlling the BLE Subsystem and handling all application features.

The Cortex-M0 Micro Controller consists of a full 32-bit processor capable of addressing 4GB of memory. It has a RISC-like load/store instruction set and internal 3-stage Pipeline Von Neumann architecture.

The Cortex-M0 processor provides a single system-level interface using AMBA technology to provide high speed, low latency memory accesses.

The Cortex-M0 processor implements a complete hardware debug solution, with 4 hardware breakpoint and 2 watch point options. This provides high system visibility of the processor, memory and peripherals through a 2-pin Serial Wire Debug (SWD) port that is ideal for microcontrollers and other small package devices.

Figure 8-1. SAM B11 ARM Cortex-M0 Subsystem



8.1.1 Features

The processor features and benefits are:

- Tight integration with the system peripherals to reduce area and development costs
- Thumb instruction set combines high code density with 32-bit performance
- Integrated sleep modes using a Wakeup Interrupt Controller for low power consumption
- Deterministic, high-performance interrupt handling via Nested Vector Interrupt Controller for time-critical applications
- Serial Wire Debug reduces the number of pins required for debugging
- DMA engine for Peripheral-to-Memory, Memory-to-Memory and Memory-to-Peripheral operation

8.1.2 Module Descriptions

8.1.2.1 Timer

The 32 bit timer block allows the CPU to generate a time tick at a programmed interval. This feature can be used for a wide variety of functions such as counting, interrupt generation and time tracking.

8.1.2.2 Dual Timer

The APB dual-input timer module is an APB slave module consisting of two programmable 32-bit down-counters that can generate interrupts when they expire. The timer can be used in a Free-running, Periodic, or One-shot mode.

8.1.2.3 Watchdog

The two watchdog blocks allow the CPU to be interrupted if it has not interacted with the watch dog timer before it expires. In addition, this interrupt will be an output of the core so that it can be used to reset the CPU in the event that a direct interrupt to the CPU is not useful. This will allow the CPU to get back to a known state in the event a program is no longer executing as expected. The watchdog module applies a reset to a system in the event of a software failure, providing a way to recover from software crashes.

8.1.2.4 Wake up Timer

This timer is a 32-bit count down timer that operates on the 32kHz sleep clock. It can be used as a general purpose timer for the ARM or as a wakeup source for the chip. It has the ability to be a one time programmable timer, as it will generate an interrupt/wakeup on expiration and stop operation. It also has the ability to be programmed in an auto reload fashion where it will generate an interrupt/wakeup and then proceed to start another count down sequence.

8.1.2.5 SPI Controller

See Section [10.3](#).

8.1.2.6 I2C Controller

See Section [10.2](#).

8.1.2.7 SPI-Flash Controller

The AHB SPI-Flash Controller is used to access the internal stacked Flash memory to access various instruction/data code needed for storing application code, code patches, and OTA images. Supports several SPI modes including 0, 1, 2, and 3.

8.1.2.8 UART

See Section [10.4](#).

8.1.2.9 DMA Controller

Direct memory access (DMA) allows certain hardware subsystems to access main system memory independently of the Cortex-M0 Processor.

The DMA features and benefits are:

- Supports any address alignment
- Supports any buffer size alignment
- Peripheral flow control, including peripheral block transfer
- The following modes are supported:
 - Peripheral to peripheral transfer
 - Memory to memory
 - Memory to peripheral
 - Peripheral to memory
 - Register to memory

- Interrupts for both TX done and RX done in memory and peripheral mode
- Scheduled transfers
- Endianness byte swapping
- Watchdog timer
- 4 Channel operation
- 32-bit Data width
- AHB mux (on read and write buses)
- Command lists support
- Usage of tokens

8.1.2.10 Nested Vector Interrupt Controller

External interrupt signals connect to the NVIC, and the NVIC prioritizes the interrupts. Software can set the priority of each interrupt. The NVIC and the Cortex-M0 processor core are closely coupled, providing low latency interrupt processing and efficient processing of late arriving interrupts.

All NVIC registers are accessible via word transfers and are little-endian. Any attempt to read or write a half-word or byte individually is Unpredictable.

The NVIC allows for the CPU to be able to individually enable, disable each interrupt source and hold each interrupt until it has been serviced and cleared by the CPU.

Table 8-1. NVIC Register Summary

Name	Description
ISER	Interrupt Set-Enable Register
ICER	Interrupt Clear-Enable Register
ISPR	Interrupt Set-Pending Register
ICPR	Interrupt Clear-Pending Register
IPR0-IPR7	Interrupt Priority Registers

For a description of each register, please see the Cortex-M0 documentation from ARM.

8.1.2.11 GPIO Controller

The AHB GPIO is a general-purpose I/O interface unit allowing the CPU to independently control all input or output signals on SAM B11. These can be used for a wide variety of functions pertaining to the application.

The AHB GPIO provides a 16-bit I/O interface with the following features:

- Programmable interrupt generation capability.
- Programmable masking support.
- Thread safe operation by providing separate set and clear addresses for control registers.
- Inputs are sampled using a double flip-flop to avoid metastability issues.

8.2 Memory Subsystem

The Cortex-M0 core uses a 128 KB instruction/boot ROM along with a 128 KB shared instruction & data RAM.

8.2.1 Shared Instruction and Data Memory

The Instruction and Data Memory (IDRAM1 and IDRAM2) contains instructions and data used by the ARM. The size of IDRAM1 and IDRAM2 is 128KB that can be used for BLE subsystem as well as for the user application.

IDRAM1 contains the three 32KB and IDRAM2 contains two 16KB memories that are accessible to the ARM and used for instruction/data storage.

8.2.2 ROM

The ROM is used to store the boot code and BLE firmware, stack and selected user profiles. ROM contains the 128KB memory that is accessible to the ARM.

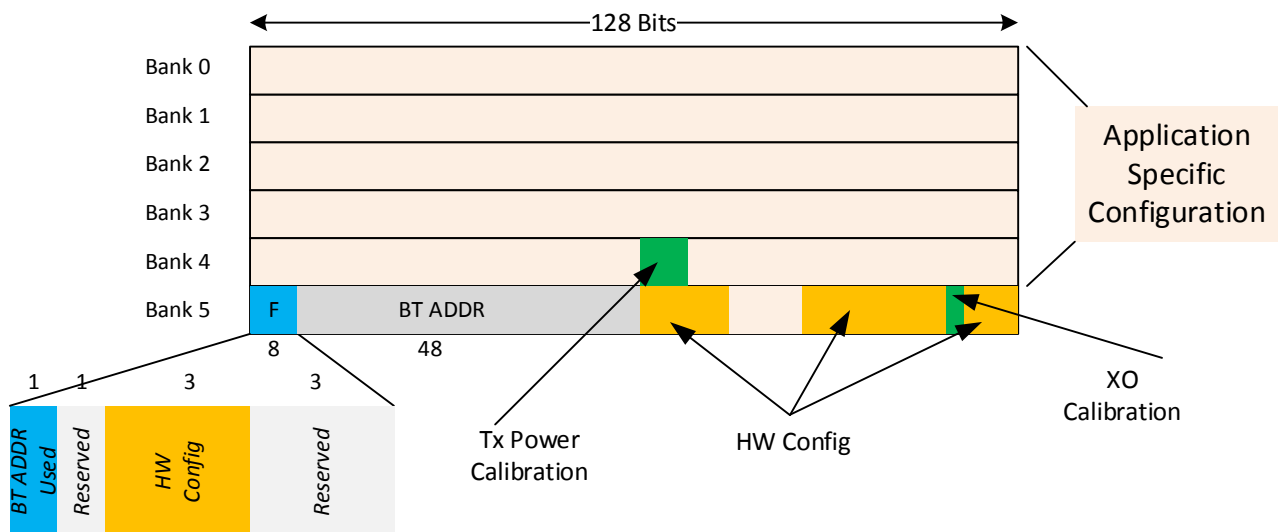
8.2.3 BLE Retention Memory

The BLE functionality requires 8KB (or more depending on the application) state, instruction and data to be retained in memory when the processor either goes into Sleep Mode or Power Off Mode. The RAM is separated into specific power domains to allow tradeoff in power consumption with retention memory size.

8.3 Non-Volatile Memory

SAM B11 has 768 bits of non-volatile eFuse memory that can be read by the CPU after device reset. This non-volatile one-time-programmable memory can be used to store customer-specific parameters, such as BLE address, XO calibration information, TX power, crystal frequency offset, etc., as well as other software-specific configuration parameters. The eFuse is partitioned into six 128-bit banks. The bit map of the first bank is shown in Figure 8-2. The purpose of the first 80 bits in bank 0 is fixed, and the remaining bits are general-purpose software dependent bits, or reserved for future use. Since each bank and each bit can be programmed independently, this allows for several updates of the device parameters following the initial programming, e.g. updating BLE address (this can be done by invalidating the last programmed bank and programming a new bank). Please refer to SAM B11 Programming Guide for the eFuse programming instructions.

Figure 8-2. SAM B11 eFuse Bit Map



8.4 Flash Memory

SAM B11 has 256KB of Flash memory, stacked on top of the MCU+BLE System on Chip. It is accessed through the SPI Flash controller and uses the 26MHz clock.

Flash memory features are:

- 256-bytes per programmable page
- Uniform 4KB Sectors, 32KB & 64KB Blocks
- Sector Erase (4K-byte)

- Block Erase (32K or 64K-byte)
- Page program up to 256 bytes <1ms
- More than 100,000 erase/write cycles and more than 20-year data retention
- 2.3V to 3.6V supply range
- 1mA active current, <1μA Power-down

9 Bluetooth Low Energy (BLE) Subsystem

The BLE subsystem implements all the critical real-time functions required for full compliance with Specification of the Bluetooth System, v4.1, Bluetooth SIG.

It consists of a Bluetooth 4.1 baseband controller (core), Radio transceiver and the Atmel® Bluetooth Smart Stack, the BLE Software Platform.

9.1 BLE core

The baseband controller consists of modem and Medium Access Controller (MAC) and it encodes and decodes HCI packets, constructs baseband data packages, schedules frames and manages and monitors connection status, slot usage, data flow, routing, segmentation, and buffer control.

The core performs Link Control Layer management supporting the main BLE states, including advertising and connection.

9.1.1 Features

- Broadcaster, Central, Observer, Peripheral
- Simultaneous Master and Slave operation, connect up to 8 slaves
- Frequency Hopping
- Advertising / Data / Control packet types
- Encryption (AES-128, SHA-256)
- Bit stream processing (CRC, whitening)
- Operating clock 52MHz

9.2 BLE Radio

The radio consists of a fully integrated transceiver, including Low Noise Amplifier, Receive (RX) down converter and analog baseband processing as well as Phase Locked Loop (PLL), Transmit (TX) Power Amplifier and Transmit/Receive switch. At the RF front end, no external RF components on the PCB are required other than the antenna and a matching component.

The RX sensitivity and TX output power of the radio together with the 4.1 PHY core provide a 100dB RF link budget for superior range and link reliability

9.2.1 Receiver Performance

Table 9-1. SAM B11 BLE Receiver Performance

Parameter	Minimum	Typical	Maximum	Unit
Frequency	2,402		2,480	MHz
Sensitivity (maximum RX gain setting)		-96		dBm

Parameter	Minimum	Typical	Maximum	Unit
Sensitivity with on-chip DC/DC		-95		
Maximum receive signal level		+5		
CCI		12.5		dB
ACI (N±1)		0		
N+2 Blocker (Image)		-22		
N-2 Blocker		-38		
N+3 Blocker (Adj. Image)		-35		
N-3 Blocker		-43		
N±4 or greater		-45		dB
Intermod (N+3, N+6)		-32		dBm
OOB (2GHz<f<2.399GHz)		-15		
OOB (f<2GHz)		-10		
RX peak current draw		4.0*		mA

All measurements performed at 3.6V VBATT and 25°C, with tests following Bluetooth V4.1 standard tests

There are two gain settings for Sensitivity, high gain (-96dBm) and low gain (-93dBm). Low gain has lower current consumption.

* At -93dBm sensitivity setting. Add 0.2mA at 3.3V for best sensitivity setting.

9.2.2 Transmitter Performance

The transmitter has fine step power control with P_{out} variable in <3dB steps below 0dBm and in <0.5dB steps above 0dBm.

Table 9-2. SAM B11 BLE Transmitter Performance

Parameter	Minimum	Typical	Maximum	Unit
Frequency	2,402		2,480	MHz
Output power range	-20	0	3.5	dBm
Maximum output power		3.5		
In-band Spurious (N±2)		-45		
In-band Spurious (N±3)		-55		
2 nd harmonic P_{out}	-41			
3 rd harmonic P_{out}	-41			
4 th harmonic P_{out}	-41			
5 th harmonic P_{out}	-41			
Frequency deviation		±250		kHz
TX peak current draw		2.9*		mA

All measurements performed at 3.6V VBATT and 25°C, with tests following Bluetooth V4.1 standard tests.

* At 0dBm TX output power.

9.3 Atmel Bluetooth SmartConnect Stack

The SAM B11 has a completely integrated Bluetooth Low Energy stack on chip, fully qualified, mature and Bluetooth V4.1 compliant.

Customer applications interface with the BLE protocol stack through the Atmel BLE API which supports direct access to the GAP, SMP, ATT, GATT client / server, and L2CAP service layer protocols in the embedded firmware.

The stack includes numerous BLE profiles for applications like:

- Smart Energy
- Consumer Wellness
- Home Automation
- Security
- Proximity Detection
- Entertainment
- Sports and Fitness
- Automotive

Together with the Atmel Studio Software Development environment, additional customer profiles can be easily developed.

The Atmel Bluetooth SmartConnect software development kit is based on Keil and IAR™ compiler tools and contains numerous application code examples for embedded and hosted modes.

In addition to the protocol stack, drivers for each peripheral hardware block are provided.

10 External Interfaces

10.1 Overview

SAM B11 external interfaces include: 2xSPI Master/Slave (SPI0 & SPI1), 2xI²C Master/Slave (I²C0 & I²C1), 2xI²C Slave-only (I²C2), 2xUART (UART1 & UART2), 1xSWD, and General Purpose Input/Output (GPIO) pins. For specific programming instructions please refer to SAM B11 Programming Guide.

Table 10-1 illustrates the different peripheral functions that are Software selectable on a per pin basis. This allows for maximum flexibility of mapping desired interfaces on GPIO pins. MUX1 option allows for any MEGAMUX option from Table 10-2 to be assigned to a GPIO.

Table 10-1. SAM B11 Pin-MUX Matrix of External Interfaces

Pin Name	Pin #	Pull	MUX0	MUX1	MUX2	MUX3	MUX4	MUX5	MUX6	MUX7
LP_GPIO_0	5	Up	GPIO 0	MEGAMUX 0	SWD CLK					TEST OUT 0
LP_GPIO_1	6	Up	GPIO 1	MEGAMUX 1	SWD IO					TEST OUT 1
LP_GPIO_2	7	Up	GPIO 2	MEGAMUX 2	UART1 RXD		SPI1 SCK	SPI0 SCK		TEST OUT 2
LP_GPIO_3	8	Up	GPIO 3	MEGAMUX 3	UART1 TXD		SPI1 MOSI	SPI0 MOSI		TEST OUT 3
LP_GPIO_4	9	Up	GPIO 4	MEGAMUX 4	UART1 CTS		SPI1 SSN	SPI0 SSN		TEST OUT 4
LP_GPIO_5	12	Up	GPIO 5	MEGAMUX 5	UART1 RTS		SPI1 MISO	SPI0 MISO		TEST OUT 5
LP_GPIO_6	13	Up	GPIO 6	MEGAMUX 6	UART2 RXD			SPI0 SCK		TEST OUT 6
LP_GPIO_7	14	Up	GPIO 7	MEGAMUX 7	UART2 TXD			SPI0 MOSI		TEST OUT 7
LP_GPIO_8	15	Up	GPIO 8	MEGAMUX 8	I ² C0 SDA	I ² C2 SDA		SPI0 SSN		TEST OUT 8
LP_GPIO_9	16	Up	GPIO 9	MEGAMUX 9	I ² C0 SCL	I ² C2 SCL		SPI0 MISO		TEST OUT 9
LP_GPIO_10	17	Up	GPIO 10	MEGAMUX 10	SPI0 SCK					TEST OUT 10
LP_GPIO_11	18	Up	GPIO 11	MEGAMUX 11	SPI0 MOSI					TEST OUT 11
LP_GPIO_12	19	Up	GPIO 12	MEGAMUX 12	SPI0 SSN					TEST OUT 12
LP_GPIO_13	20	Up	GPIO 13	MEGAMUX 13	SPI0 MISO					TEST OUT 13
LP_GPIO_14	36	Up	GPIO 14	MEGAMUX 14	UART2 CTS		I ² C1 SDA			TEST OUT 14
LP_GPIO_15	37	Up	GPIO 15	MEGAMUX 15	UART2 RTS		I ² C1 SCL			TEST OUT 15
LP_GPIO_16	38	Up	GPIO 16	MEGAMUX 16			SPI1 SSN	SPI0 SCK		TEST OUT 16
LP_GPIO_17	40	Up	GPIO 17	MEGAMUX 17		I ² C2 SDA	SPI1 SCK	SPI0 MOSI		TEST OUT 17
LP_GPIO_18	41	Up	GPIO 18	MEGAMUX 18		I ² C2 SCL	SPI1 MISO	SPI0 SSN		TEST OUT 18
LP_GPIO_19	42	Up	GPIO 19	MEGAMUX 19			SPI1 MOSI	SPI0 MISO		TEST OUT 19
LP_GPIO_20	43	Up	GPIO 20	MEGAMUX 20						TEST OUT 20
LP_GPIO_22	10	Up	GPIO 22	MEGAMUX 22						
LP_GPIO_23	11	Up	GPIO 23	MEGAMUX 23						
AO_GPIO_0	33	Up	GPIO 31	WAKEUP	RTC CLK IN	32KHZ CLKOUT				
AO_GPIO_1	34	Up	GPIO 30	WAKEUP	RTC CLK IN	32KHZ CLKOUT				
AO_GPIO_2	35	Up	GPIO 29	WAKEUP	RTC CLK IN	32KHZ CLKOUT				

Pin Name	Pin #	Pull	MUX0	MUX1	MUX2	MUX3	MUX4	MUX5	MUX6	MUX7
GPIO_MS1	24	Up	GPIO 47							
GPIO_MS2	25	Up	GPIO 46							
GPIO_MS3	27	Up	GPIO 45							
GPIO_MS4	28	Up	GPIO 44							

Table 10-2 shows the various software selectable MEGAMUX options that correspond to specific peripheral functionality. Several MEGAMUX options provides an interface to manage Wi-Fi BLE coexistence issues.

Table 10-2. SAM B11 Software Selectable MEGAMUX Options

MUX_Sel	Function	Notes
0	UART1 RXD	
1	UART1 TXD	
2	UART1 CTS	
3	UART1 RTS	
4	UART2 RXD	
5	UART2 TXD	
6	UART2 CTS	
7	UART2 RTS	
8	I2C0 SDA	
9	I2C0 SCL	
10	I2C1 SDA	
11	I2C1 SCL	
12	PWM 1	
13	PWM 2	
14	PWM 3	
15	PWM 4	
16	LP CLOCK OUT	32kHz clock output (RC Osc or RTC XO)
17	WLAN TX ACTIVE	Coexistence: WiFi is currently transmitting
18	WLAN RX ACTIVE	Coexistence: WiFi is currently receiving
19	BLE TX ACTIVE	Coexistence: BLE is currently transmitting
20	BLE RX ACTIVE	Coexistence: BLE is currently receiving
21	BLE IN PROCESS	Coexistence Signal
22	BLE MBSY	Coexistence Signal
23	BLE SYNC	Coexistence Signal
24	BLE RXNTX	Coexistence Signal
25	BLE PTI 0	Coexistence: BLE Priority

MUX_Sel	Function	Notes
26	BLE PTI 1	Coexistence: BLE Priority
27	BLE PTI 2	Coexistence: BLE Priority
28	BLE PTI 3	Coexistence: BLE Priority
29	QUAD DEC X IN A	
30	QUAD DEC X IN B	
31	QUAD DEC Y IN A	
32	QUAD DEC Y IN B	
33	QUAD DEC Z IN A	
34	QUAD DEC Z IN B	

An example of peripheral assignment using these MEGAMUX options is as follows:

- I²C0 pin-muxed on LP_GPIO_10 and LP_GPIO_11 via MUX1 and MEGAMUX=8 and 9
- I²C1 pin-muxed on LP_GPIO_0 and LP_GPIO_1 via MUX1 and MEGAMUX=10 and 11
- PWM pin-muxed on LP_GPIO_16 via MUX1 and MEGAMUX=12

Another example is to illustrate the available options for pin LP_GPIO_3, depending on the pin-MUX option selected:

- MUX0: the pin will function as bit 3 of the GPIO bus and is controlled by the GPIO controller in the ARM subsystem
- MUX1: any option from the MEGAMUX table can be selected, for example it can be a quad_dec, pwm, or any of the other functions listed in the MEGAMUX table
- MUX2: the pin will function as UART1 TXD; this can be also achieved with the MUX1 option via MEGAMUX, but the MUX2 option allows a shortcut for the recommended pinout
- MUX3: this option is not used and thus defaults to the GPIO option (same as MUX0)
- MUX4: the pin will function as SPI1 MOSI (this option is not available through MEGAMUX)
- MUX5: the pin will function as SPI0 MOSI (this option is not available through MEGAMUX)
- MUX6: the pin will function as SPI FLASH SCK (this option is not available through MEGAMUX)
- MUX7: the pin will function as bit 3 of the test output bus, giving access to various debug signals

10.2 I²C Master/Slave Interface

10.2.1 Description

SAM B11 provides I²C Interface that can be configured as Slave or Master. I²C Interface is a two-wire serial interface consisting of a serial data line (SDA) and a serial clock line (SCL). SAM B11 I²C supports I²C bus Version 2.1 - 2000 and can operate in the following speed modes:

- Standard mode (100kb/s)
- Fast mode (400kb/s)
- High-speed mode (3.4Mb/s)

The I²C is a synchronous serial interface. The SDA line is a bidirectional signal and changes only while the SCL line is low, except for STOP, START, and RESTART conditions. The output drivers are open-drain to perform wire-AND functions on the bus. The maximum number of devices on the bus is limited by only the maximum capacitance specification of 400pF. Data is transmitted in byte packages.

For specific information, refer to the Philips Specification entitled “The I²C -Bus Specification, Ver2.1”.

10.2.2 I²C Interface Timing

The I²C Interface timing (common to Slave and Master) is provided in Figure 10-1. The timing parameters for Slave and Master modes are specified in Table 10-3 and Table 10-4 respectively.

Figure 10-1. SAM B11 I²C Slave Timing Diagram

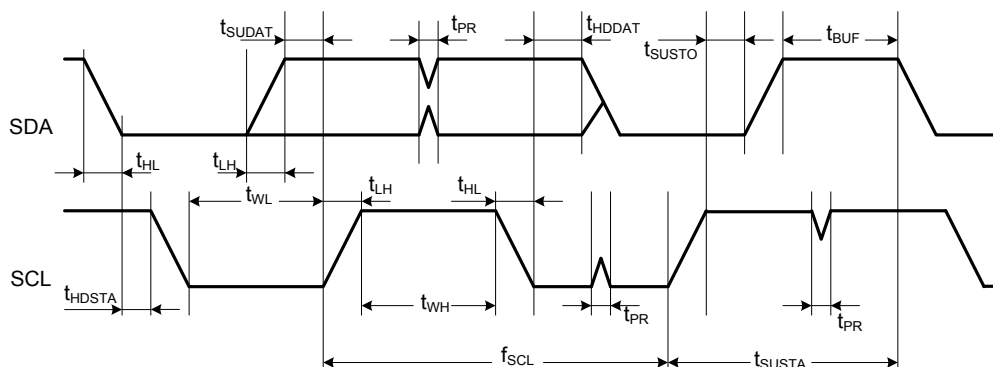


Table 10-3. SAM B11 I²C Slave Timing Parameters

Parameter	Symbol	Min.	Max.	Units	Remarks
SCL Clock Frequency	f_{SCL}	0	400	kHz	
SCL Low Pulse Width	t_{WL}	1.3		μs	
SCL High Pulse Width	t_{WH}	0.6			
SCL, SDA Fall Time	t_{HL}		300	ns	
SCL, SDA Rise Time	t_{LH}		300		This is dictated by external components
START Setup Time	t_{SUSTA}	0.6		μs	
START Hold Time	t_{HDSTA}	0.6			
SDA Setup Time	t_{SUDAT}	100		ns	
SDA Hold Time	t_{HDDAT}	0 40			Slave and Master Default Master Programming Option
STOP Setup time	t_{SUSTO}	0.6		μs	
Bus Free Time Between STOP and START	t_{BUF}	1.3			
Glitch Pulse Reject	t_{PR}	0	50	ns	

Table 10-4. SAM B11 I²C Master Timing Parameters

Parameter	Symbol	Standard Mode		Fast Mode		High-speed Mode		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
SCL Clock Frequency	f_{SCL}	0	100	0	400	0	3400	kHz
SCL Low Pulse Width	t_{WL}	4.7		1.3		0.16		μs
SCL High Pulse Width	t_{WH}	4		0.6		0.06		
SCL Fall Time	t_{HLSCL}		300		300	10	40	ns

Parameter	Symbol	Standard Mode		Fast Mode		High-speed Mode		Units
SDA Fall Time	t_{HLSDA}		300		300	10	80	
SCL Rise Time	t_{LHSCl}		1000		300	10	40	
SDA Rise Time	t_{LHSDA}		1000		300	10	80	
START Setup Time	t_{SUSTA}	4.7		0.6		0.16		μs
START Hold Time	t_{HDSTA}	4		0.6		0.16		
SDA Setup Time	t_{SUDAT}	250		100		10		ns
SDA Hold Time	t_{HDDAT}	5		40		0	70	
STOP Setup time	t_{SUSTO}	4		0.6		0.16		μs
Bus Free Time Between STOP and START	t_{BUF}	4.7		1.3				
Glitch Pulse Reject	t_{PR}			0	50			ns

10.3 SPI Master/Slave Interface

10.3.1 Description

SAM B11 provides a Serial Peripheral Interface (SPI) that can be configured as Master or Slave. The SPI Interface pins are mapped as shown in [Table 10-5](#). The SPI Interface is a full-duplex slave-synchronous serial interface. When the SPI is not selected, i.e., when SSN is high, the SPI interface will not interfere with data transfers between the serial-master and other serial-slave devices. When the serial slave is not selected, its transmitted data output is buffered, resulting in a high impedance drive onto the serial master receive line. The SPI Slave interface responds to a protocol that allows an external host to read or write any register in the chip as well as initiate DMA transfers. For the details of the SPI protocol and more specific instructions, refer to SAM B11 Programming Guide.

Table 10-5. SAM B11 SPI Interface Pin Mapping

Pin Name	SPI Function
SSN	Active Low Slave Select
SCK	Serial Clock
MOSI	Master Out Slave In (Data)
MISO	Master In Slave Out (Data)

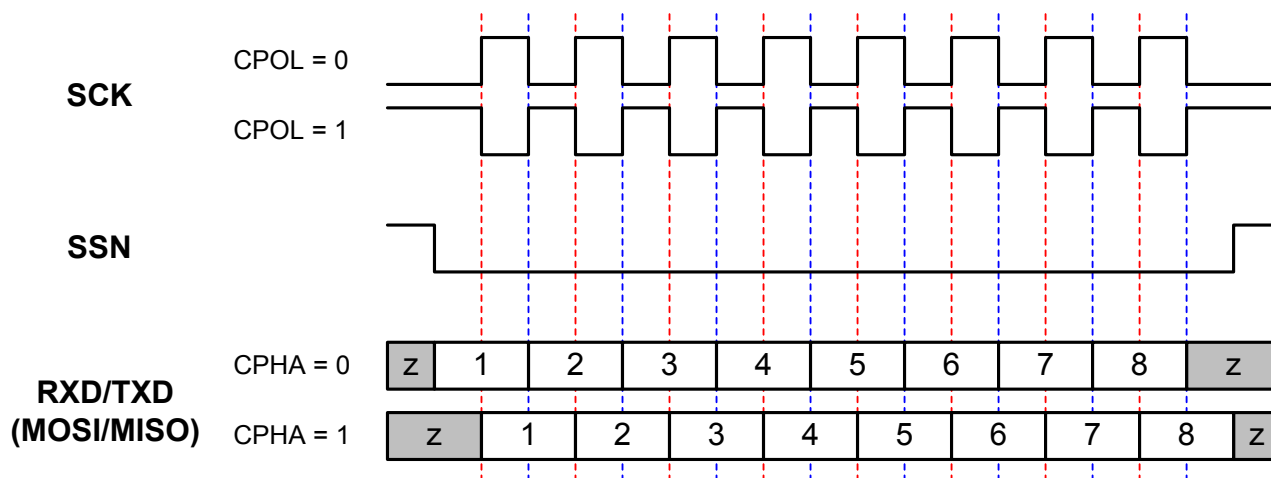
10.3.2 SPI Interface Modes

The SPI Interface supports four standard modes as determined by the Clock Polarity (CPOL) and Clock Phase (CPHA) settings. These modes are illustrated in Table 10-6 and Figure 10-2. The red lines in Figure 10-2 correspond to Clock Phase = 0 and the blue lines correspond to Clock Phase = 1.

Table 10-6. SAM B11 SPI Modes

Mode	CPOL	CPHA
0	0	0
1	0	1
2	1	0
3	1	1

Figure 10-2. SAM B11 SPI Clock Polarity and Clock Phase Timing



10.3.3 SPI Slave Timing

The SPI Slave timing is provided in [Figure 10-3](#) and [Table 10-7](#).

Figure 10-3. SAM B11 SPI Slave Timing Diagram

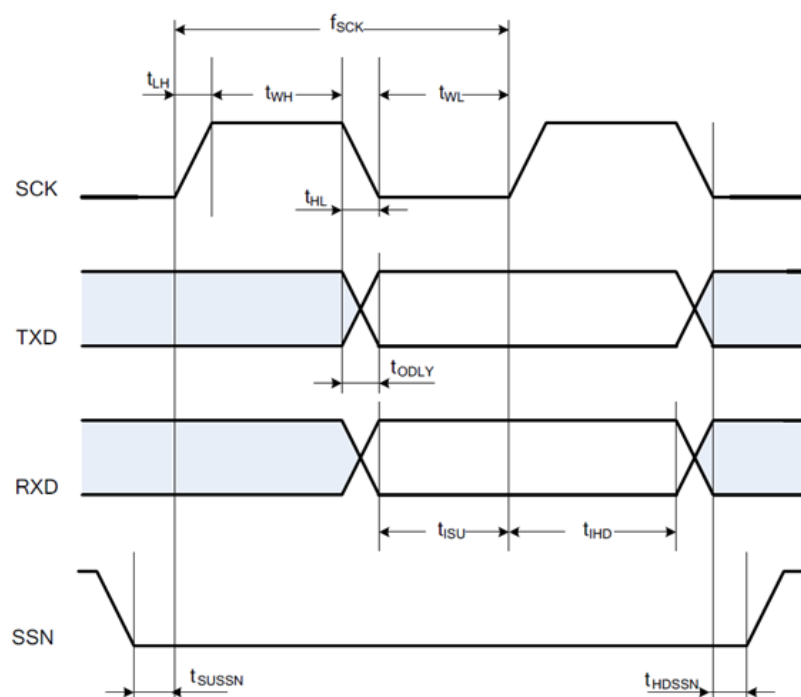


Table 10-7. SAM B11 SPI Slave Timing Parameters

Parameter	Symbol	Min.	Max.	Units
Clock Input Frequency	f_{SCK}		2	MHz
Clock Low Pulse Width	t_{WL}	240		ns
Clock High Pulse Width	t_{WH}	240		
Clock Rise Time	t_{LH}		10	
Clock Fall Time	t_{HL}		10	
Input Setup Time	t_{ISU}	5		
Input Hold Time	t_{IHD}	5		
Output Delay	t_{ODLY}	0	20	
Slave Select Setup Time	t_{SUSSN}	5		
Slave Select Hold Time	t_{HDSSN}	5		

10.3.4 SPI Master Timing

The SPI Master Timing is provided in [Figure 10-4](#) and [Table 10-8](#).

Figure 10-4. SAM B11 SPI Master Timing Diagram

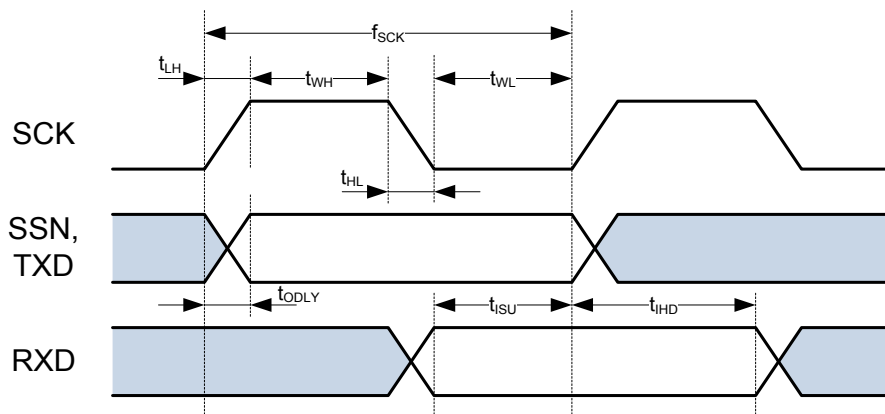


Table 10-8. SAM B11 SPI Master Timing Parameters

Parameter	Symbol	Min.	Max.	Units
Clock Output Frequency	f_{SCK}		4	MHz
Clock Low Pulse Width	t_{WL}	120		ns
Clock High Pulse Width	t_{WH}	120		
Clock Rise Time	t_{LH}		5	
Clock Fall Time	t_{HL}		5	
Input Setup Time	t_{ISU}	5		
Input Hold Time	t_{IHD}	5		
Output Delay	t_{ODLY}	0	5	

10.4 UART Interface

SAM B11 provides Universal Asynchronous Receiver/Transmitter (UART) interfaces for serial communication. The Bluetooth subsystem has two UART interfaces: a 4-pin interface for control and data transfer. The UART interfaces are compatible with the RS-232 standard, where SAM B11 operates as Data Terminal Equipment (DTE). The 2-pin UART has the receive and transmit pins (RXD and TXD), and the 4-pin UART has two additional pins used for flow control/handshaking: Request To Send (RTS) and Clear To Send (CTS). The pins associated with each UART interfaces can be enabled on several alternative pins by programming their corresponding pin MUX control registers (see [Table 10-1](#) and [Table 10-2](#) for available options).

The UART features programmable baud rate generation with fractional clock division, which allows transmission and reception at a wide variety of standard and non-standard baud rates. The Bluetooth UART input clock is selectable between 26MHz, 13MHz, 6.5MHz, and 3.25MHz. The clock divider value is programmable as 13 integer bits and three fractional bits (with 8.0 being the smallest recommended value for normal operation). This results in the maximum supported baud rate of $26\text{MHz} / 8.0 = 3.25\text{MBd}$.

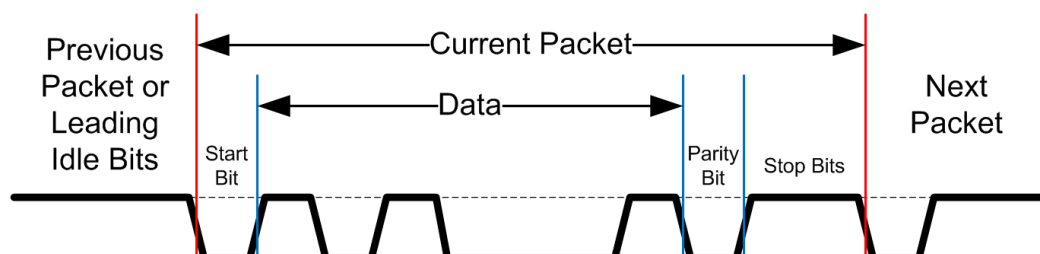
The UART can be configured for seven or eight bit operation, with or without parity, with four different parity types (odd, even, mark, or space), and with one or two stop bits. It also has RX and TX FIFOs, which ensure reliable high speed reception and low software overhead transmission. FIFO size is 4 x 8 for both RX and TX direction.

The UART also has status registers showing the number of received characters available in the FIFO and various error conditions, as well the ability to generate interrupts based on these status bits.

An example of UART receiving or transmitting a single packet is shown in [Figure 10-5](#). This example shows 7-bit data (0x45), odd parity, and two stop bits.

For more specific instructions please refer to SAM B11 Programming Guide.

Figure 10-5. Example of UART Rx or Tx packet



10.5 GPIOs

30 General Purpose Input/Output (GPIO) pins total, labeled LP_GPIO, GPIO_MS, and AO_GPIO, are available to allow for application specific functions. Each GPIO pin can be programmed as an input (the value of the pin can be read by the host or internal processor) or as an output (the output values can be programmed by the host or internal processor).

LP_GPIO are digital interface pins, GPIO_MS are mixed signal/analog interface pins and AO_GPIO are always-on digital interface pins that can detect interrupt signals while in deep sleep mode for wake up purposes.

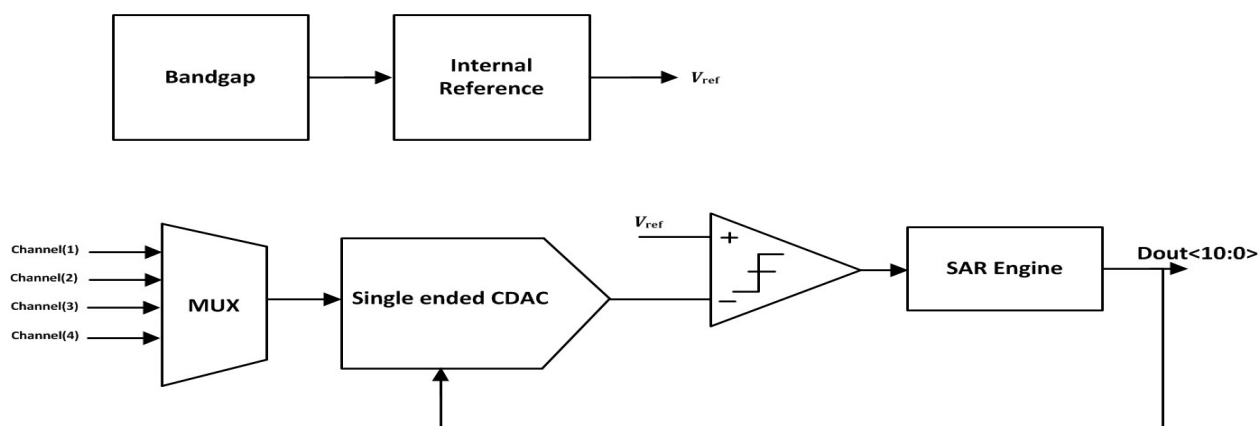
The LP_GPIO have interrupt capability but only when in active / standby mode. In sleep mode, they are turned off to save power consumption.

10.6 Analog to Digital Converter (ADC)

10.6.1 Overview

The SAM B11 has an integrated Successive Approximation (SAR) ADC with 11-bit resolution and variable conversion speed up to 1MS/s. The key building blocks are the capacitive DAC, comparator, and synchronous SAR engine as shown in [Figure 10-6](#).

Figure 10-6. SAM B11 SAR ADC Block Diagram



The ADC reference voltage can be either generated internally or set externally via one of the four available Mixed Signal GPIO pins on the SAM B11.

There are two modes of operation:

- A. High resolution (11-bit): Set the reference voltage to half the supply voltage or below. In this condition the input signal dynamic range is equal to twice the reference voltage (ENOB=10bit)
- B. Medium Resolution (10-bit) : Set the reference voltage to any value below supply voltage (up to supply voltage - 300mV) and in this condition the input dynamic range is from zero to reference voltage (ENOB = 9bit)

There are four input channels that are time multiplexed to the input of the SAR ADC.

In power saving mode, the internal reference voltage is completely off and the reference voltage is set externally.

The ADC characteristics are summarized in [Table 10-9](#).

Table 10-9. SAR ADC Characteristics

Conversion rate	1ks → 1MS
Selectable Resolution	10 → 11bit
Power consumption	13.5μA (at 100KS/s)*

* With external reference

10.6.2 Timing

The ADC timing is shown in [Figure 10-7](#). The input signal is sampled twice, in the first sampling cycle the input range is defined either to be above reference voltage or below it and in the 2nd sampling instant the ADC start its normal operation.

The ADC takes two sampling instants and N-1 conversion cycle (N=ADC resolution) and one cycle to sample the data out. So for 11-bit resolution it takes 13 clock cycles to do one Sample conversion.

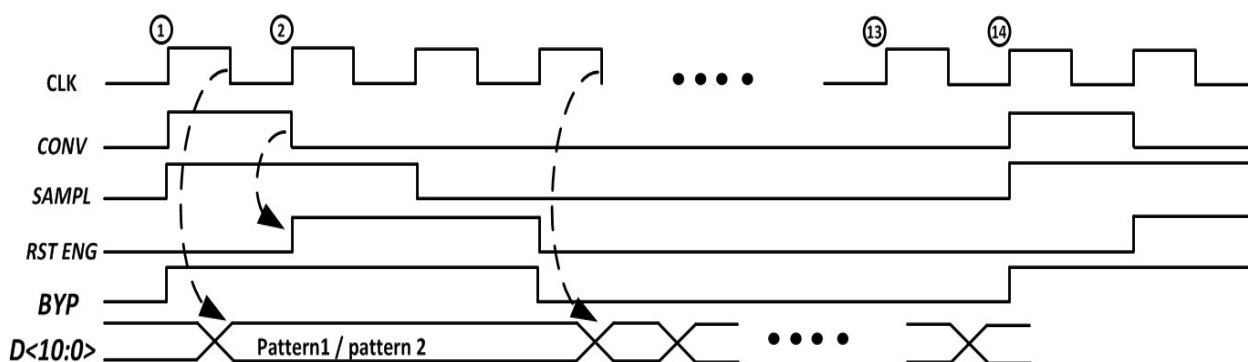
The Input clock equals N+2 the sampling clock frequency (N is the ADC resolution).

CONV signal: Gives indication about end of conversion.

SAMPL: The input signal is sampled when this signal is high.

RST ENG: When High SAR Engine is in reset mode (SAR engine output is set to mid-scale).

Figure 10-7. SAR ADC Timing



10.6.3 Performance

Table 10-10. Static Performance of SAR ADC

Parameter	Condition	Min	Typ	Max	Unit
Input voltage range		0		VBAT	V
Resolution			11		bits
Sample rate			100	1000	KSPS
Input offset	Internal VREF	-10		+10	mV
Gain error	Internal VREF	-4		+4	%
DNL	100KSPS. Internal VREF=1.6V. Same result for external VREF.	-0.75		+1.75	LSB
INL	100KSPS. Internal VREF=1.6V. Same result for external VREF.	-2		+2.5	LSB
THD	1.1.1.1 1kHz sine input at 100KSPS		73		dB
SINAD	1kHz sine input at 100KSPS		62.5		dB
SFDR	1kHz sine input at 100KSPS		73.7		dB
Conversion time			13		cycles
Current consumption	Using external VREF, at 100KSPS.		13.5		uA
	Using internal VREF, at 100KSPS.		25.0		uA
	Using external VREF, at 1MSPS		94		uA
	Using internal VREF, at 1MSPS		150		uA
	Using internal VREF, during VBAT monitoring		100		uA
	Using internal VREF, during temperature monitoring		50		uA
Internal reference voltage	Mean value using VBAT=2.5V		1.026*		V
	Standard deviation across parts		10.5		mV
VBAT Sensor Accuracy	Without calibration	-55		+55	mV
	With offset & gain calibration	-17		+17	mV
Temperature Sensor Accuracy	Without calibration	-9		+9	C
	With offset calibration	-4		+4	C

$T_c = 25^{\circ}\text{C}$ $V_{BAT} = 3.0\text{ V}$, unless otherwise noted

* Effective VREF is 2xInternal Reference Voltage

Figure 10-8. INL of SAR ADC

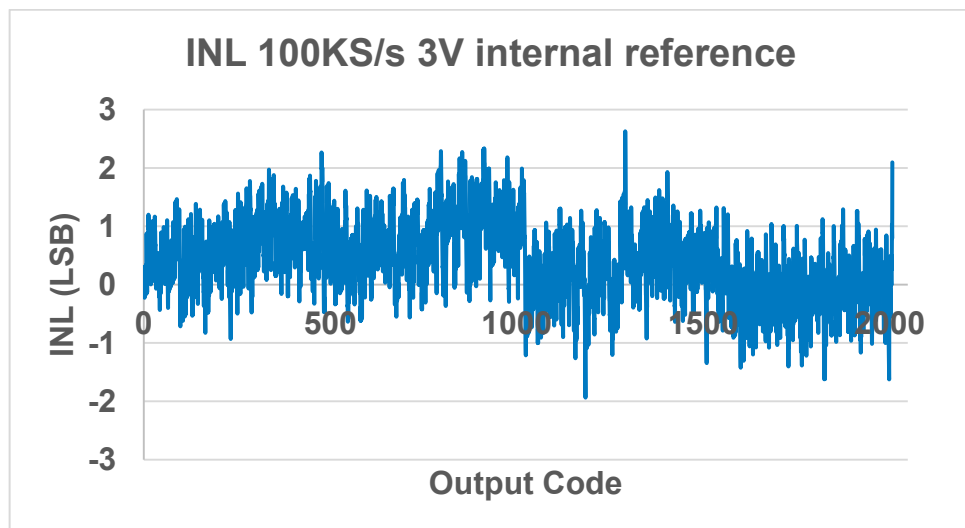


Figure 10-9. DNL of SAR ADC

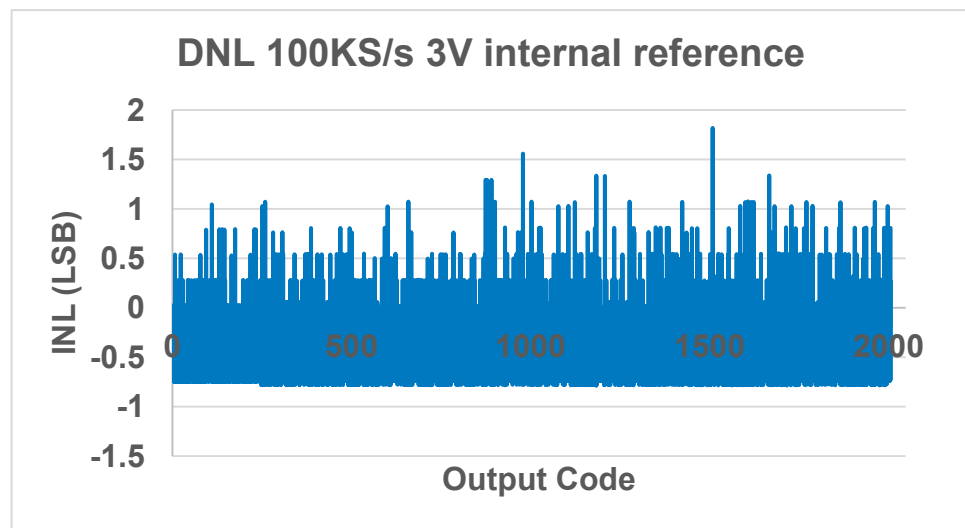


Figure 10-10. Sensor ADC dynamic measurement with sinusoidal input

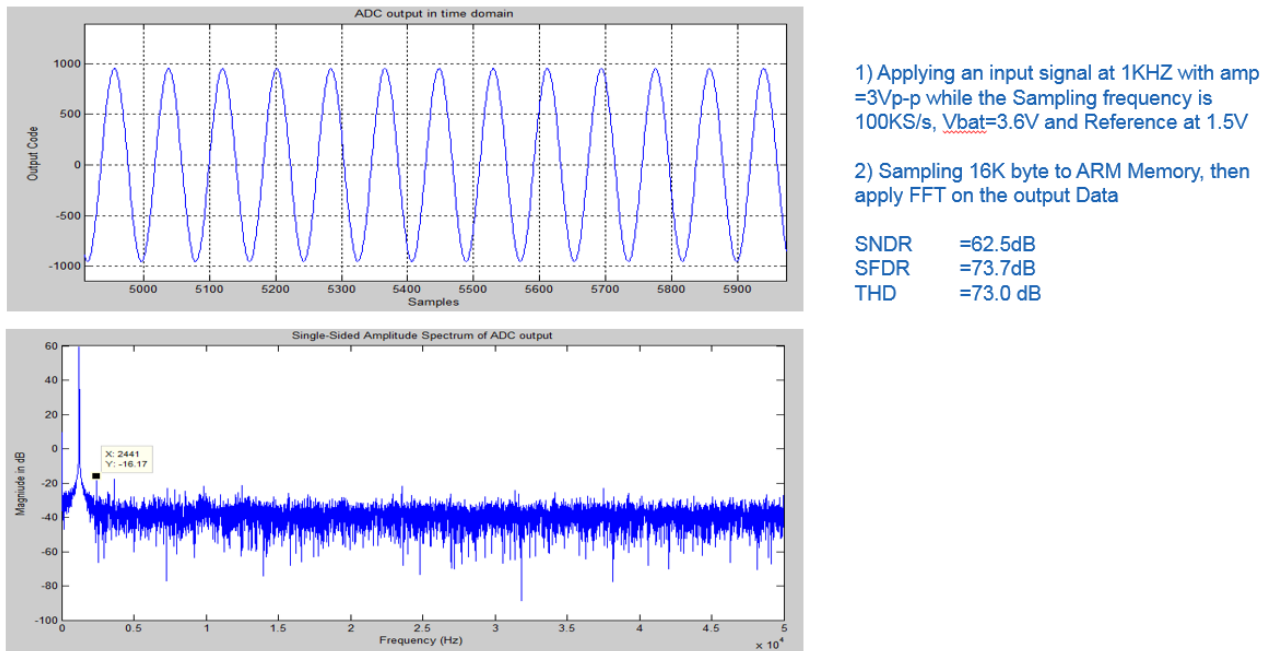
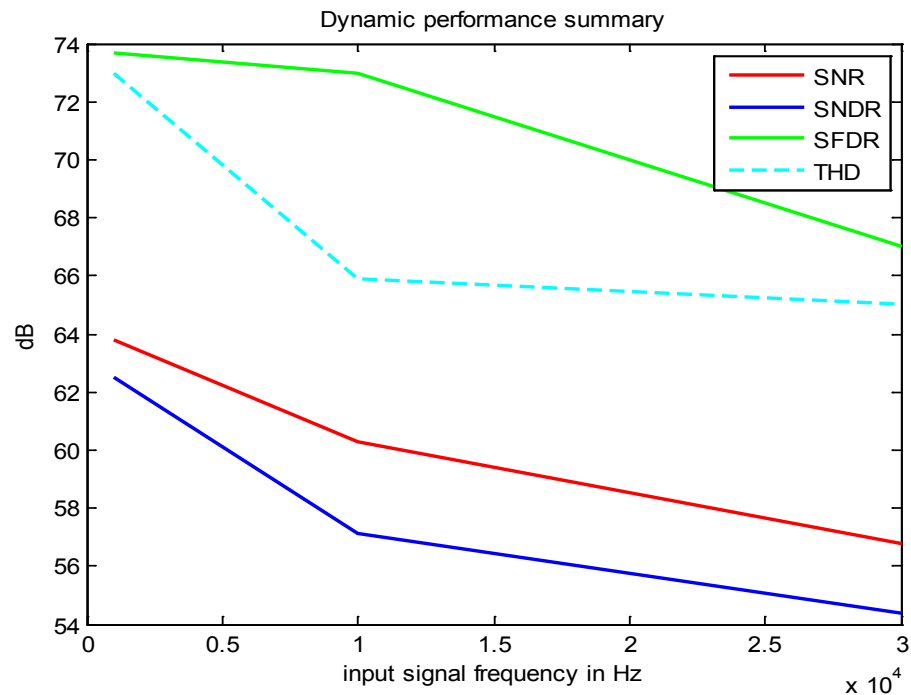


Figure 10-11. Sensor ADC dynamic performance summary at 100KSPS



10.7 Software Programmable Timer and Pulse Width Modulator

SAM B11 contains four individually configurable pulse width modulator (PWM) blocks to provide external control voltages. The base frequency of the PWM block (f_{PWM_base}) is derived from the XO clock (26MHz) or the RC oscillator followed by a programmable divider.

The frequency of each PWM pulse (f_{PWM}) is programmable in steps according to the following relationship:

$$f_{PWM} = \frac{f_{PWM_base}}{64 * 2^i} \quad i = 0, 1, 2, \dots, 8$$

The duty cycle of each PWM signal is configurable with 10-bit resolution (minimum duty cycle is 1/1024 and maximum is 1023/1024).

f_{PWM_base} can be selected to have different values according to the following table. Minimum and maximum frequencies supported for each clock selection is listed in the table as well.

Table 10-11. f_{PWM} Range for Different f_{PWM} Base Frequencies

f_{PWM_base}	f_{PWM} max	f_{PWM} min
26MHz	406.25kHz	6.347kHz
13MHz	203.125kHz	3.173kHz
6.5MHz	101.562kHz	1.586kHz
3.25MHz	50.781kHz	793.25Hz

10.8 Clock Output

SAM B11 has an ability to output a clock. The clock can be output to any GPIO pin via the test MUX. Note that this feature requires that the ARM and BLE power domains stay on. If BLE is not used, the clocks to the BLE core are gated off, resulting in small leakage. The following two methods can be used to output a clock.

10.8.1 Variable Frequency Clock Output Using Fractional Divider

SAM B11 can output the variable frequency ADC clock using a fractional divider off the 26MHz oscillator. This clock needs to be enabled using bit 10 of the `lpmcu_clock_enables_1` register. The clock frequency can be controlled by the divider ratio using the `sens_adc_clk_ctrl` register (12-bits integer part, 8-bit fractional part). The division ratio can vary from 2 to 4096 delivering output frequency between 6.35kHz to 13MHz. This is a digital divider with pulse swallowing implementation so the clock edges may not be at exact intervals for the fractional ratios. However, it is exact for integer division ratios.

10.8.2 Fixed Frequency Clock Output

SAM B11 can output the following fixed-frequency clocks:

- 52MHz derived from XO
- 26MHz derived from XO
- 2MHz derived from the 2MHz RC Osc
- 31.25kHz derived from the 2MHz RC Osc
- 32.768kHz derived from the RTC XO
- 26MHz derived from 26MHz RC Osc
- 6.5MHz derived from XO
- 3.25MHz derived from 26MHz RC Osc

For clocks 26MHz and above ensure that external pad load on the board is minimized to get a clean waveform.

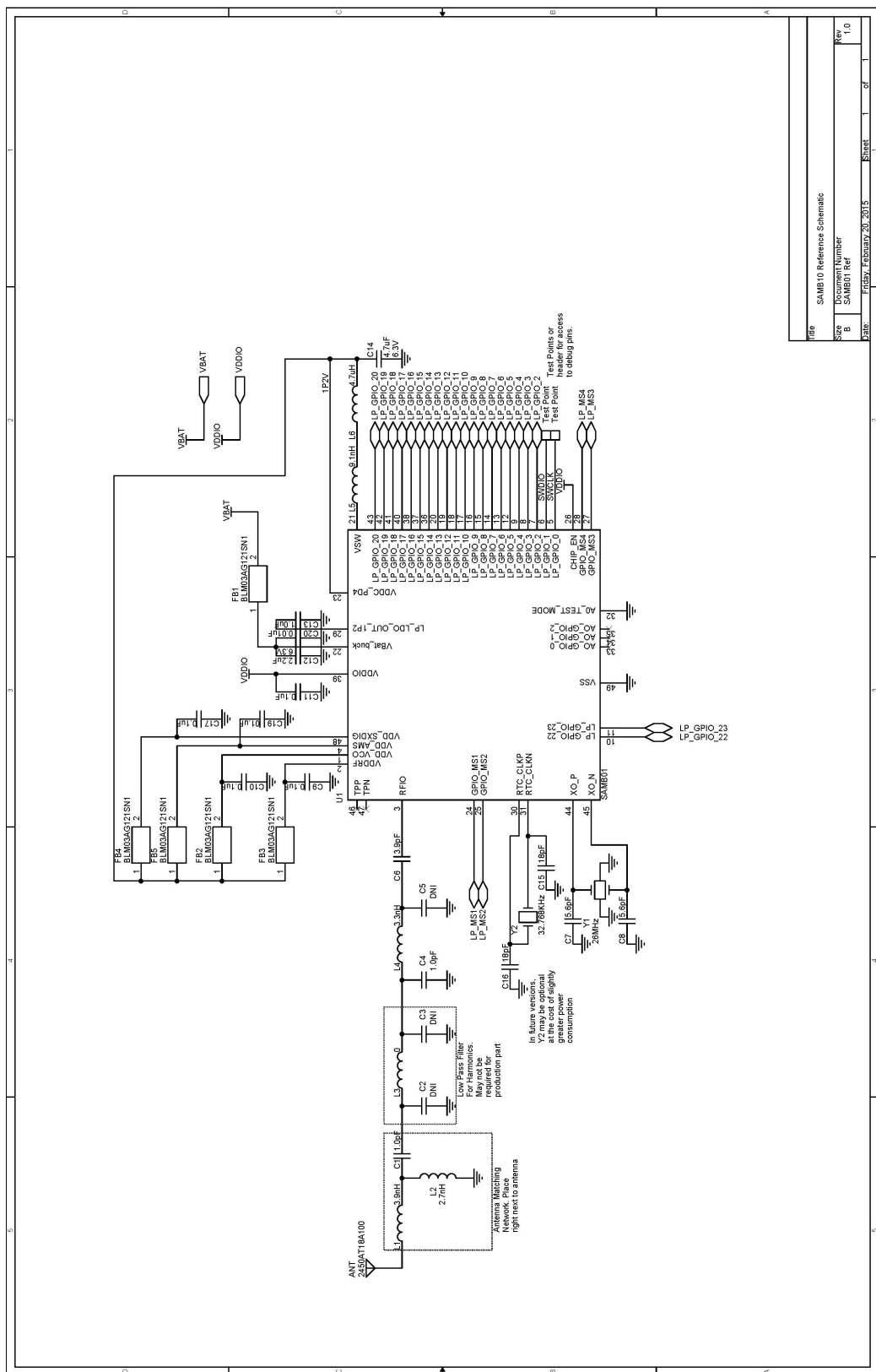
10.9 Three-Axis Quadrature Decoder

SAM B11 has a three-axis Quadrature decoder (X, Y, and Z) that can determine the direction and speed of movement on three axes, requiring in total six GPIO pins to interface with the sensors. The sensors are expected to provide pulse trains as inputs to the quadrature decoder.

Each axis channel input will have two pulses with ± 90 degrees phase shift depending on the direction of movement. The decoder counts the edges of the two waveforms to determine the speed and uses the phase relationship between the two inputs to determine the direction of motion.

The decoder is configured to interrupt ARM based on independent thresholds for each direction. Each quadrature clock counter (X, Y, and Z) is an unsigned 16-bit counter and the system clock uses a programmable sampling clock ranging from 26MHz, 13, 6.5 to 3.25MHz.

If wakeup is desired from threshold detection on an axis input, the always on GPIO needs to be used.



12 Bill of Material (BOM)

SAMB10 Reference Schematic Revised: Friday, February 20, 2015							
SAMB01 Ref Revision: 1.0							
Bill Of Materials February 20,2015 15:49:00							
Item	Qty	Reference	Value	Description	Manufacturer	Part Number	Footprint
1	1	ANT	Antenna	Antenna			ANT_2450AT18A100
2	2	C1,C4	1.0pF	CAP,CER,1.0pF,+/-0.1pF,NPO,0201,25V,-55-125C	Murata	GRM0335C1E1R0BA01J	CS0201
3	3	C2,C3,C5	DNI	CAP,CER,1.0pF,+/-0.1pF,NPO,0201,25V,-55-125C	Murata	GRM0335C1E1R0BA01J	CS0201
4	1	C6	3.9pF	CAP,CER,3.9pF,+/-0.1pF,NPO,0201,25V,-55-125C	Samsung	CL03C3R9BA3GNNC	CS0201
5	2	C7,C8	5.6pF	CAP,CER,5.6pF,+/-0.5pF,NPO,0201,25V,-55-125C	TDK	C0603C0G1E5R6D030BA	CS0201
6	4	C9,C10,C11,C17	0.1uF	CAP,CER,0.1uF,10%,X5R,0201,6.3V,-55-125C	Murata	GRM033R60J104KE19D	CS0201
7	1	C12	2.2uF	CAP,CER,2.2uF,10%,X5R,0402,6.3V,-55-85C	TDK	C1005X5R0J225K	CS0402
8	1	C13	1.0uF	CAP,CER,1.0uF,20%,X5R,0201,6.3V,-55-85C	TDK	C0603X5R0J105M030BC	CS0201
9	1	C14	4.7uF	CAP,CER,4.7uF,10%,X5R,0402,6.3V,-55-85C	TDK	C1005X5R0J475K050BC	CS0402
10	2	C15,C16	18pF	CAP,CER,18pF,5%,NPO,0201,50V	Murata	GRM1555C1H180JA01D	CS0201
11	1	C19	01.uF	CAP,CER,0.1uF,10%,X5R,0201,6.3V,-55-125C	Murata	GRM033R60J104KE19D	CS0201
12	1	C20	0.01uF	CAP,CER,0.01uF,10%,X5R,0201,10V,-55-125C	Murata	GRM033R61A103KA01D	CS0201
13	5	FB1,FB2,FB3,FB4,FB5	BLM03AG121SN1	FERRITE,120 OHM @100MHz,200mA,0201,-55-125C	Murata	BLM03AG121SN1	FBS0201
14	1	L1	3.9nH	Inductor,3.9nH,+/-0.2nH,Q=13@500MHz,SRF=8.1GHz,0201,-55-125C	Taiyo Yuden	HKQ0603S3N9C-T	LS0201
15	1	L2	2.7nH	Inductor,2.7nH,+/-0.2nH,Q=13@500MHz,SRF=8.1GHz,0201,-55-125C	Taiyo Yuden	HKQ0603S2N7C-T	LS0201
16	1	L3	0	Inductor,3.3nH,+/-0.2nH,Q=13@500MHz,SRF=8.1GHz,0201,-55-125C	Taiyo Yuden	HKQ0603S3N3C-T	LS0201
17	1	L4	3.3nH	Inductor,3.3nH,+/-0.2nH,Q=13@500MHz,SRF=8.1GHz,0201,-55-125C	Taiyo Yuden	HKQ0603S3N3C-T	LS0201
18	1	L5	9.1nH	INDUCTOR,Multilayer,9.1nH,5%,300mA,0.26 ohmsQ=8@100MHz,-55C-125C,0402	Murata	LQG15HS15NJ02D	LS0402
19	1	L6	4.7uH	INDUCTOR,unshielded,4.7uH,20%,145mA Saturation,0.312ohms,0603,-40-105C	Taiyo Yuden	CBMF1608T4R7M	LS0603
20							
21	1	U1	SAMB01	IC, BLE, 48QFN	Atmel	SAMB01	48QFN
22	1	Y1	26MHz	CRYSTAL,26MHz,CL=8pF,15ppm,-30-85C,ESR=60,2.5x2mm	NDK	CX2520DB26000D0FLICC	KYOCERA_CX2520DB
23	1	Y2	32.768KHz	Crystal, 32.768KHz,+/-20ppm,-40-+85C,CL=12.5pF, 2 lead, SM	ECS	ECS-.327-12.5-39-TR	OSC_ECX-39

13 Electrical Characteristics

13.1 Absolute Maximum Ratings

Table 13-1. SAM B11 Absolute Maximum Ratings

Symbol	Characteristic	Min	Max	Unit
VDDIO	I/O Supply Voltage	-0.3	5.0	V
VBATT	Battery Supply Voltage	-0.3	5.0	
V _{IN} ⁽¹⁾	Digital Input Voltage	-0.3	VDDIO	
V _{AIN} ⁽²⁾	Analog Input Voltage	-0.3	1.5	
V _{ESDHBM} ⁽³⁾	ESD Human Body Model	-1000, -2000 (see notes below)	+1000, +2000 (see notes below)	°C
T _A	Storage Temperature	-65	150	
	Junction Temperature		125	

- Note:
1. V_{IN} corresponds to all the digital pins
 2. V_{AIN} corresponds to all the analog pins
 3. For V_{ESDHBM}, each pin is classified as Class 1, or Class 2, or both:
 - The Class 1 pins include all the pins (both analog and digital)
 - The Class 2 pins include all digital pins only
 - V_{ESDHBM} is ±1kV for Class1 pins. V_{ESDHBM} is ±2kV for Class2 pins

13.2 Recommended Operating Conditions

Table 13-2. SAM B11 Recommended Operating Conditions

Symbol	Characteristic	Min	Typ	Max	Units
VDDIO	I/O Supply Voltage*	2.3	3	4.3	V
VBATT	Battery Supply Voltage*	2.3	3	4.3	V
	Operating Temperature	-40		85	°C

Note: * VBATT must not be less than VDDIO

13.3 DC Characteristics

Table 13-3 provides the DC characteristics for the SAM B11 digital pads.

Table 13-3. SAM B11 DC Electrical Characteristics

Characteristic	Min	Typ	Max	Unit
Input Low Voltage VIL	-0.30		0.60	V
Input High Voltage VIH	VDDIO-0.60		VDDIO+0.30	
Output Low Voltage VOL			0.45	
Output High Voltage VOH	VDDIO-0.50			
Output Loading			20	pF
Digital Input Load			6	
Pad drive strength (regular pads*)	5	11		mA
Pad drive strength (high-drive pads*)	10	22		

Note: * The following are high-drive pads: GPIO_8, GPIO_9; all other pads are regular.

14 Document Revision History

Doc Rev.	Date	Comments
42426A	09/2015	

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