Spartan-3A DSP FPGA Family Data Sheet

DS610 October 4, 2010 **Product Specification**

Module 1: Introduction and Ordering Information

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The functionality of the Spartan®-3A DSP FPGA family is described in the following documents.

- UG331: *Spartan-3 Generation FPGA User Guide*
  - Clocking Resources
  - Digital Clock Managers (DCMs)
  - Block RAM
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  - Design Authentication using Device DNA
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Spartan-3A DSP FPGA Family: Introduction and Ordering Information

DS610 (v3.0) October 4, 2010 **Product Specification**

Introduction

The Spartan®-3A DSP family of Field-Programmable Gate Arrays (FPGAs) solves the design challenges in most high- volume, cost-sensitive, high-performance DSP applications. The two-member family offers densities ranging from 1.8 to 3.4 million system gates, as shown in Table 1.

The Spartan-3A DSP family builds on the success of the Spartan-3A FPGA family by increasing the amount of memory per logic and adding XtremeDSP™ DSP48A slices. New features improve system performance and reduce the cost of configuration. These Spartan-3A DSP FPGA enhancements, combined with proven 90 nm process technology, deliver more functionality and bandwidth per dollar than ever before, setting the new standard in the programmable logic and DSP processing industry.

The Spartan-3A DSP FPGAs extend and enhance the Spartan-3A FPGA family. The XC3SD1800A and the XC3SD3400A devices are tailored for DSP applications and have additional block RAM and XtremeDSP DSP48A slices. The XtremeDSP DSP48A slices replace the 18x18 multipliers found in the Spartan-3A devices and are based on the DSP48 blocks found in the Virtex®-4 devices. The block RAMs are also enhanced to run faster by adding an output register. Both the block RAM and DSP48A slices in the Spartan-3A DSP devices run at 250 MHz in the lowest cost, standard -4 speed grade.

Because of their exceptional DSP price/performance ratio, Spartan-3A DSP FPGAs are ideally suited to a wide range of consumer electronics applications, such as broadband access, home networking, display/projection, and digital television.

The Spartan-3A DSP family is a superior alternative to mask programmed ASICs. FPGAs avoid the high initial cost, lengthy development cycles, and the inherent inflexibility of conventional ASICs. Also, FPGA programmability permits design upgrades in the field with no hardware replacement necessary, an impossibility with ASICs.

Features

- Very low cost, high-performance DSP solution for high-volume, cost-conscious applications
- 250 MHz XtremeDSP DSP48A Slices
  - Dedicated 18-bit by 18-bit multiplier
  - Available pipeline stages for enhanced performance of at least 250 MHz in the standard -4 speed grade
  - 48-bit accumulator for multiply-accumulate (MAC) operation
  - Integrated adder for complex multiply or multiply-add operation
  - Integrated 18-bit pre-adder
  - Optional cascaded Multiply or MAC
- Hierarchical SelectRAM™ memory architecture
  - Up to 2268 Kbits of fast block RAM with byte write enables for processor applications
  - Up to 373 Kbits of efficient distributed RAM
  - Registered outputs on the block RAM with operation of at least 280 MHz in the standard -4 speed grade
- Dual-range V_{CCAUX} supply simplifies 3.3V-only design
- Suspend, Hibernate modes reduce system power
- Low-power option reduces quiescent current
- Multi-voltage, multi-standard SelectIO™ interface pins
  - Up to 519 I/O pins or 227 differential signal pairs
  - LVCMOS, LVTTL, HSTL, and SSTL single-ended I/O
  - 3.3V, 2.5V, 1.8V, 1.5V, and 1.2V signaling
  - Selectable output drive, up to 24 mA per pin
  - QUIETIO standard reduces I/O switching noise
  - Full 3.3V ± 10% compatibility and hot swap compliance
  - 622+ Mb/s data transfer rate per differential I/O
  - LVDS, RSDS, mini-LVDS, HSTL/SSTL differential I/O with integrated differential termination resistors
  - Enhanced Double Data Rate (DDR) support
  - DDR/DDR2 SDRAM support up to 333 Mb/s
  - Fully compliant 32-/64-bit, 33/66 MHz PCI support
- Abundant, flexible logic resources
  - Densities up to 53712 logic cells, including optional shift register
  - Efficient wide multiplexers, wide logic, fast carry logic
  - IEEE 1149.1/1532 JTAG programming/debug port
- Eight Digital Clock Managers (DCMs)
  - Clock skew elimination (delay locked loop)
  - Frequency synthesis, multiplication, division
  - High-resolution phase shifting
  - Wide frequency range (5 MHz to over 320 MHz)
- Eight low-skew global clock networks, eight additional clocks per half device, plus abundant low-skew routing
- Configuration interface to industry-standard PROMs
  - Low-cost, space-saving SPI serial Flash PROM
  - x8 or x8/x16 BPI parallel NOR Flash PROM
  - Low-cost Xilinx® Platform Flash with JTAG
  - Unique Device DNA identifier for design authentication
  - Load multiple bitstreams under FPGA control
  - Post-configuration CRC checking
- MicroBlaze™ and PicoBlaze™ embedded processor cores
- BGA and CSP packaging with Pb-free options
  - Common footprints support easy density migration
- XA Automotive version available

Table 1: **Summary of Spartan-3A DSP FPGA Attributes**

Device	System Gates	Equivalent Logic Cells	CLB Array (One CLB = Four Slices)				Distributed RAM Bits(1)	Block RAM Bits(1)	DSP48As	DCMs	Maximum User I/O	Maximum Differential I/O Pairs
			Rows	Columns	Total CLBs	Total Slices						
XC3SD1800A	1800K	37,440	88	48	4,160	16,640	260K	1512K	84	8	519	227
XC3SD3400A	3400K	53,712	104	58	5,968	23,872	373K	2268K	126	8	469	213

Notes:
1. By convention, one Kb is equivalent to 1,024 bits.

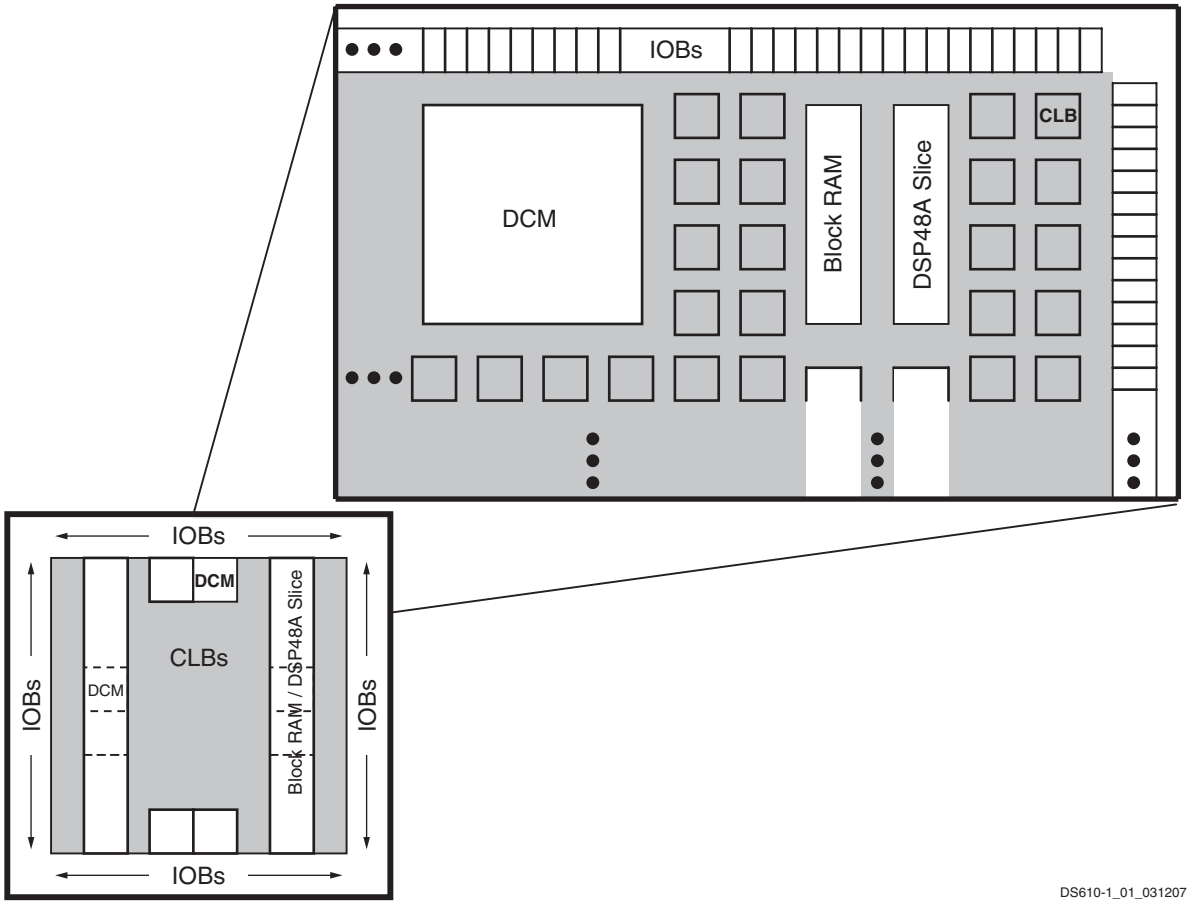
Architectural Overview

The Spartan-3A DSP family architecture consists of five fundamental programmable functional elements:

- **XtremeDSP™ DSP48A Slice** provides an 18-bit x 18-bit multiplier, 18-bit pre-adder, 48-bit post-adder/accumulator, and cascade capabilities for various DSP applications.
- **Block RAM** provides data storage in the form of 18-Kbit dual-port blocks.
- **Configurable Logic Blocks (CLBs)** contain flexible Look-Up Tables (LUTs) that implement logic plus storage elements used as flip-flops or latches. CLBs perform a wide variety of logical functions as well as store data.
- **Input/Output Blocks (IOBs)** control the flow of data between the I/O pins and the internal logic of the device. IOBs support bidirectional data flow plus 3-state operation. Supports a variety of signal standards, including several high-performance differential standards. Double Data-Rate (DDR) registers are included.
- **Digital Clock Manager (DCM) Blocks** provide self-calibrating, fully digital solutions for distributing, delaying, multiplying, dividing, and phase-shifting clock signals.

These elements are organized as shown in Figure 1. A dual ring of staggered IOBs surrounds a regular array of CLBs. The XC3SD1800A has four columns of DSP48As, and the XC3SD3400A has five columns of DSP48As. Each DSP48A has an associated block RAM. The DCMs are positioned in the center with two at the top and two at the bottom of the device and in the two outer columns of the 4 or 5 columns of block RAM and DSP48As.

The Spartan-3A DSP family features a rich network of routing that interconnect all five functional elements, transmitting signals among them. Each functional element has an associated switch matrix that permits multiple connections to the routing.



Notes:

1. The XC3SD1800A and XC3SD3400A have two DCMs on both the left and right sides, as well as the two DCMs at the top and bottom of the devices. The two DCMs on the left and right of the chips are in the middle of the outer Block RAM/DSP48A columns of the 4 or 5 columns in the selected device, as shown in the diagram above.
2. A detailed diagram of the DSP48A can be found in UG431: *XtremeDSP DSP48A for Spartan-3A DSP FPGAs User Guide.*

Figure 1: **Spartan-3A DSP Family Architecture**

Configuration

Spartan-3A DSP FPGAs are programmed by loading configuration data into robust, reprogrammable, static CMOS configuration latches (CCLs) that collectively control all functional elements and routing resources. The FPGA's configuration data is stored externally in a PROM or some other non-volatile medium, either on or off the board. After applying power, the configuration data is written to the FPGA using any of seven different modes:

- Master Serial from a Xilinx Platform Flash PROM
- Serial Peripheral Interface (SPI) from an industry-standard SPI serial Flash
- Byte Peripheral Interface (BPI) Up from an industry-standard x8 or x8/x16 parallel NOR Flash
- Slave Serial, typically downloaded from a processor
- Slave Parallel, typically downloaded from a processor
- Boundary Scan (JTAG), typically downloaded from a processor or system tester

Furthermore, Spartan-3A DSP FPGAs support MultiBoot configuration, allowing two or more FPGA configuration bitstreams to be stored in a single SPI serial Flash or a BPI parallel NOR Flash. The FPGA application controls which configuration to load next and when to load it.

Additionally, each Spartan-3A DSP FPGA contains a unique, factory-programmed Device DNA identifier useful for tracking purposes, anti-cloning designs, or IP protection.

I/O Capabilities

The Spartan-3A DSP FPGA SelectIO interface supports many popular single-ended and differential standards. Table 2 shows the number of user I/Os as well as the number of differential I/O pairs available for each device/package combination. Some of the user I/Os are unidirectional input-only pins as indicated in Table 2.

Spartan-3A DSP FPGAs support the following single-ended standards:

- 3.3V low-voltage TTL (LVTTL)
- Low-voltage CMOS (LVCMOS) at 3.3V, 2.5V, 1.8V, 1.5V, or 1.2V
- 3.3V PCI at 33 MHz or 66 MHz
- HSTL I, II, and III at 1.5V and 1.8V, commonly used in memory applications
- SSTL I and II at 1.8V, 2.5V, and 3.3V, commonly used for memory applications
- Spartan-3A DSP FPGAs support the following differential standards:
- LVDS, mini-LVDS, RSDS, and PPDS I/O at 2.5V or 3.3V
- Bus LVDS I/O at 2.5V
- TMDS I/O at 3.3V
- Differential HSTL and SSTL I/O
- LVPECL inputs at 2.5V or 3.3V

Table 2: **Available User I/Os and Differential (Diff) I/O Pairs**

Device	CS484 CSG484		FG676 FGG676	
	User	**Diff**	**User**	**Diff**
XC3SD1800A	**309**(1) *(60)*	**140** *(78)*	**519** *(110)*	**227** *(131)*
XC3SD3400A	**309** *(60)*	**140** *(78)*	**469** *(60)*	**213** *(117)*

Notes:

1. The number shown in **bold** indicates the maximum number of I/O and input-only pins. The number shown in (*italics*) indicates the number of input-only pins. The differential (Diff) input-only pin count includes both differential pairs on input-only pins and differential pairs on I/O pins within I/O banks that are restricted to differential inputs.

Package Marking

Figure 2 shows the top marking for Spartan-3A DSP FPGAs. The "5C" and "4I" Speed Grade/Temperature Range part combinations may be dual marked as "5C/4I". Devices with the dual mark can be used as either -5C or -4I devices. Devices with a single mark are only guaranteed for the marked speed grade and temperature range.

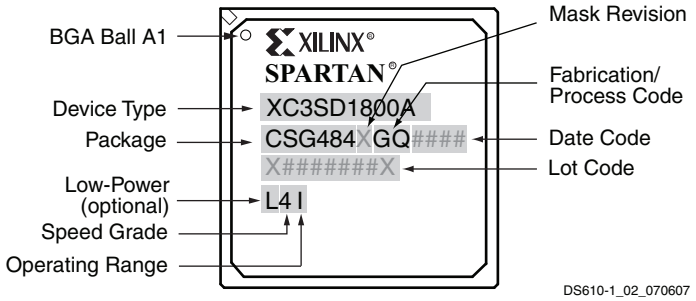
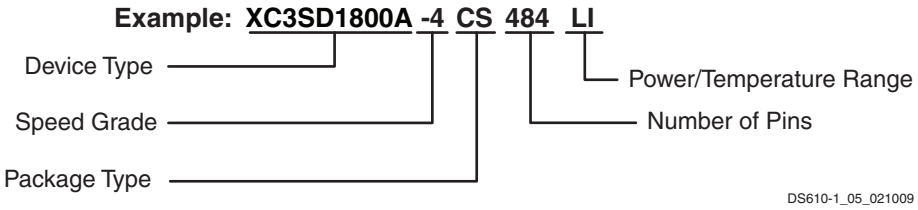


Figure 2: **Spartan-3A DSP FPGA Package Marking Example**

Ordering Information

Spartan-3A DSP FPGAs are available in both standard and Pb-free packaging options for all device/package combinations. The Pb-free packages include a 'G' character in the ordering code.



Device	Speed Grade		Package Type / Number of Pins		Power/Temperature Range (T_J)	
XC3SD1800A	-4	Standard Performance	CS484/ CSG484	484-ball Chip-Scale Ball Grid Array (CSBGA)	C	Commercial (0°C to 85°C)
XC3SD3400A	-5	High Performance(1)	FG676/ FGG676	676-ball Fine-Pitch Ball Grid Array (FBGA)	I	Industrial (–40°C to 100°C)
					LI	Low-power Industrial (–40°C to 100°C)(2)

Notes:

1. The -5 speed grade is exclusively available in the Commercial temperature range.
2. The low-power option (LI) is exclusively available in the CS(G)484 package and industrial temperature range.
3. See DS705, *XA Spartan-3A DSP Automotive FPGA Family Data Sheet* for the XA Automotive Spartan-3A DSP FPGAs.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
04/02/07	1.0	Initial Xilinx release.
05/25/07	1.0.1	Minor edits.
06/18/07	1.2	Updated for Production release.
07/16/07	2.0	Added Low-power options.
06/02/08	2.1	Added reference to SCD 4103 for 750 Mbps performance. Add dual mark clarification to Package Marking. Updated links.
03/11/09	2.2	Simplified ordering information. Removed reference to SCD 4103.
10/04/10	3.0	Updated the Notice of Disclaimer section.

Notice of Disclaimer

Spartan-3A DSP FPGA Design Documentation

The functionality of the Spartan®-3A DSP FPGA family is described in the following documents. The topics covered in each guide are listed.

- DS706: E*xtended Spartan-3A Family Overview*
- UG331**:** *Spartan-3 Generation FPGA User Guide*
  - Clocking Resources
  - Digital Clock Managers (DCMs)
  - Block RAM
  - Configurable Logic Blocks (CLBs)
    - Distributed RAM
    - SRL16 Shift Registers
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  - ISE iMPACT Programming Examples
  - MultiBoot Reconfiguration
  - Design Authentication using Device DNA
- UG431: *XtremeDSP DSP48A for Spartan-3A DSP FPGAs User Guide*
  - XtremeDSP DSP48A Slices
  - XtremeDSP DSP48A Pre-Adder

For specific hardware examples, please see the Spartan-3A DSP FPGA Starter Kit board web pages.

- **XtremeDSP Starter Platform—Spartan-3A DSP 1800A Edition**
  http://www.xilinx.com/products/devkits/HW-SD1800A-DSP-SB-UNI-G.htm
- **XtremeDSP Starter Kit—Spartan-3A DSP 1800A Edition**
  http://www.xilinx.com/products/devkits/DO-SD1800A-DSP-SK-UNI-G.htm
- **XtremeDSP Video Starter Kit—Spartan-3A DSP Edition**
  http://www.xilinx.com/products/devkits/DO-S3ADSP-VIDEO-SK-UNI-G.htm
- **Embedded Development HW/SW Kit—Spartan-3A DSP S3D1800A MicroBlaze Processor Edition**
  http://www.xilinx.com/products/devkits/DO-SD1800A-EDK-DK-UNI-G.htm

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04/02/07	1.0	Initial Xilinx release.
05/25/07	1.0.1	Minor edits.
06/18/07	1.2	Updated for Production release.
07/16/07	2.0	Added Low-power options; no changes to this module.
06/02/08	2.1	Updated links.
03/11/09	2.2	Added link to DS706 on Extended Spartan-3A family.
10/04/10	3.0	Updated link to sign up for Alerts and updated Notice of Disclaimer.

Notice of Disclaimer

DC Electrical Characteristics

In this section, specifications may be designated as Advance, Preliminary, or Production. These terms are defined as follows:

Advance: Initial estimates are based on simulation, early characterization, and/or extrapolation from the characteristics of other families. Values are subject to change. Use as estimates, not for production.

Preliminary: Based on characterization. Further changes are not expected.

Production: These specifications are approved once the silicon has been characterized over numerous production lots. Parameter values are considered stable with no future changes expected.

All parameter limits are representative of worst-case supply voltage and junction temperature conditions. **Unless otherwise noted, the published parameter values apply to all Spartan®-3A DSP devices. AC and DC characteristics are specified using the same numbers for both commercial and industrial grades.**

Absolute Maximum Ratings

Stresses beyond those listed under Table 3: Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions is not implied. Exposure to absolute maximum conditions for extended periods of time adversely affects device reliability.

Table 3: **Absolute Maximum Ratings**

Symbol	Description	Conditions	Min	Max	Units
V_{CCINT}	Internal supply voltage		–0.5	1.32	V
V_{CCAUX}	Auxiliary supply voltage		–0.5	3.75	V
V_{CCO}	Output driver supply voltage		–0.5	3.75	V
V_{REF}	Input reference voltage		–0.5	V_{CCO} + 0.5	V
V_{IN}	Voltage applied to all User I/O pins and Dual-Purpose pins	Driver in a high-impedance state	–0.95	4.6	V
	Voltage applied to all Dedicated pins		–0.5	4.6	V
I_{IK}	Input clamp current per I/O pin	$-0.5V < V_{IN} < (V_{CCO} + 0.5V)$ (1)	–	±100	mA
V_{ESD}	Electrostatic Discharge Voltage	Human body model	–	±2000	V
		Charged device model	–	±500	V
		Machine model	–	±200	V
T_J	Junction temperature		–	125	°C
T_{STG}	Storage temperature		–65	150	°C

Notes:

1. Upper clamp applies only when using PCI IOSTANDARDs.
2. For soldering guidelines, see UG112: *Device Packaging and Thermal Characteristics* and XAPP427: *Implementation and Solder Reflow Guidelines for Pb-Free Packages*.

Power Supply Specifications

Table 4: **Supply Voltage Thresholds for Power-On Reset**

Symbol	Description	Min	Max	Units
V_{CCINTT}	Threshold for the V_{CCINT} supply	0.4	1.0	V
V_{CCAUXT}	Threshold for the V_{CCAUX} supply	1.0	2.0	V
V_{CCO2T}	Threshold for the V_{CCO} Bank 2 supply	1.0	2.0	V

Notes:

1. V_{CCINT}, V_{CCAUX}, and V_{CCO} supplies to the FPGA can be applied in any order. However, the FPGA configuration source (Platform Flash, SPI Flash, parallel NOR Flash, microcontroller) might have specific requirements. Check the data sheet for the attached configuration source. Apply V_{CCINT} last for lowest overall power consumption (see the UG331 chapter titled "Powering Spartan-3 Generation FPGAs" for more information).
2. To ensure successful power-on, V_{CCINT}, V_{CCO} Bank 2, and V_{CCAUX} supplies must rise through their respective threshold-voltage ranges with no dips at any point.

Table 5: **Supply Voltage Ramp Rate**

Symbol	Description	Min	Max	Units
V_{CCINTR}	Ramp rate from GND to valid V_{CCINT} supply level	0.2	100	ms
V_{CCAUXR}	Ramp rate from GND to valid V_{CCAUX} supply level	0.2	100	ms
V_{CCO2R}	Ramp rate from GND to valid V_{CCO} Bank 2 supply level	0.2	100	ms

Notes:

1. V_{CCINT}, V_{CCAUX}, and V_{CCO} supplies to the FPGA can be applied in any order. However, the FPGA configuration source (Platform Flash, SPI Flash, parallel NOR Flash, microcontroller) might have specific requirements. Check the data sheet for the attached configuration source. Apply V_{CCINT} last for lowest overall power consumption (see the UG331 chapter titled "Powering Spartan-3 Generation FPGAs" for more information).
2. To ensure successful power-on, V_{CCINT}, V_{CCO} Bank 2, and V_{CCAUX} supplies must rise through their respective threshold-voltage ranges with no dips at any point.

Table 6: **Supply Voltage Levels Necessary for Preserving CMOS Configuration Latch (CCL) Contents and RAM Data**

Symbol	Description	Min	Units
V_{DRINT}	V_{CCINT} level required to retain CMOS Configuration Latch (CCL) and RAM data	1.0	V
V_{DRAUX}	V_{CCAUX} level required to retain CMOS Configuration Latch (CCL) and RAM data	2.0	V

General Recommended Operating Conditions

Table 7: **General Recommended Operating Conditions**

Symbol	Description			Min	Nominal	Max	Units
T_J	Junction temperature	Commercial		0	–	85	°C
		Industrial		–40	–	100	°C
V_{CCINT}	Internal supply voltage			1.14	1.20	1.26	V
V_{CCO} (1)	Output driver supply voltage			1.10	–	3.60	V
V_{CCAUX}	Auxiliary supply voltage (2)	V_{CCAUX} = 2.5		2.25	2.50	2.75	V
		V_{CCAUX} = 3.3		3.00	3.30	3.60	V
V_{IN} (3)	Input voltage	PCI™ IOSTANDARD		–0.5	–	V_{CCO}+0.5	V
		All other IOSTANDARDs	IP or IO_#	–0.5	–	4.10	V
			IO_Lxxy_# (4)	–0.5	–	4.10	V
T_{IN}	Input signal transition time (5)			–	–	500	ns

Notes:

1. This V_{CCO} range spans the lowest and highest operating voltages for all supported I/O standards. Table 10 lists the recommended V_{CCO} range specific to each of the single-ended I/O standards, and Table 12 lists that specific to the differential standards.
2. Define V_{CCAUX} selection using CONFIG VCCAUX constraint.
3. See XAPP459, *Eliminating I/O Coupling Effects when Interfacing Large-Swing Single-Ended Signals to User I/O Pins on Spartan-3 Families*.
4. For single-ended signals that are placed on a differential-capable I/O, V_{IN} of –0.2V to –0.5V is supported but can cause increased leakage between the two pins. See *Parasitic Leakage* in UG331, *Spartan-3 Generation FPGA User Guide*.
5. Measured between 10% and 90% V_{CCO}. Follow Signal Integrity recommendations.

General DC Characteristics for I/O Pins

Table 8: **General DC Characteristics of User I/O, Dual-Purpose, and Dedicated Pins** (1)

Symbol	Description	Test Conditions		Min	Typ	Max	Units
I_L (2)	Leakage current at User I/O, Input-only, Dual-Purpose, and Dedicated pins, FPGA powered	Driver is in a high-impedance state, V_{IN} = 0V or V_{CCO} max, sample-tested		–10	–	+10	µA
I_{HS}	Leakage current on pins during hot socketing, FPGA unpowered	All pins except INIT_B, PROG_B, DONE, and JTAG pins when PUDC_B = 1.		–10	–	+10	µA
		INIT_B, PROG_B, DONE, and JTAG pins or other pins when PUDC_B = 0.		Add I_{HS} + I_{RPU}			µA
I_{RPU} (3)	Current through pull-up resistor at User I/O, Dual-Purpose, Input-only, and Dedicated pins. Dedicated pins are powered by V_{CCAUX}.	V_{IN} = GND	V_{CCO} or V_{CCAUX} = 3.0V to 3.6V	–151	–315	–710	µA
			V_{CCO} or V_{CCAUX} = 2.3V to 2.7V	–82	–182	–437	µA
			V_{CCO} = 1.7V to 1.9V	–36	–88	–226	µA
			V_{CCO} = 1.4V to 1.6V	–22	–56	–148	µA
			V_{CCO} = 1.14V to 1.26V	–11	–31	–83	µA
R_{PU} (3)	Equivalent pull-up resistor value at User I/O, Dual-Purpose, Input-only, and Dedicated pins (based on I_{RPU} per Note 2)	V_{IN} = GND	V_{CCO} = 3.0V to 3.6V	5.1	11.4	23.9	kΩ
			V_{CCO} = 2.3V to 2.7V	6.2	14.8	33.1	kΩ
			V_{CCO} = 1.7V to 1.9V	8.4	21.6	52.6	kΩ
			V_{CCO} = 1.4V to 1.6V	10.8	28.4	74.0	kΩ
			V_{CCO} = 1.14V to 1.26V	15.3	41.1	119.4	kΩ
I_{RPD} (3)	Current through pull-down resistor at User I/O, Dual-Purpose, Input-only, and Dedicated pins	V_{IN} = V_{CCO}	V_{CCAUX} = 3.0V to 3.6V	167	346	659	µA
			V_{CCAUX} = 2.25V to 2.75V	100	225	457	µA
R_{PD} (3)	Equivalent pull-down resistor value at User I/O, Dual-Purpose, Input-only, and Dedicated pins (based on I_{RPD} per Note 2)	V_{CCAUX} = 3.0V to 3.6V	V_{IN} = 3.0V to 3.6V	5.5	10.4	20.8	kΩ
			V_{IN} = 2.3V to 2.7V	4.1	7.8	15.7	kΩ
			V_{IN} = 1.7V to 1.9V	3.0	5.7	11.1	kΩ
			V_{IN} = 1.4V to 1.6V	2.7	5.1	9.6	kΩ
			V_{IN} = 1.14V to 1.26V	2.4	4.5	8.1	kΩ
		V_{CCAUX} = 2.25V to 2.75V	V_{IN} = 3.0V to 3.6V	7.9	16.0	35.0	kΩ
			V_{IN} = 2.3V to 2.7V	5.9	12.0	26.3	kΩ
			V_{IN} = 1.7V to 1.9V	4.2	8.5	18.6	kΩ
			V_{IN} = 1.4V to 1.6V	3.6	7.2	15.7	kΩ
			V_{IN} = 1.14V to 1.26V	3.0	6.0	12.5	kΩ
I_{REF}	V_{REF} current per pin	All V_{CCO} levels		–10	–	+10	µA
C_{IN}	Input capacitance	–		–	–	10	pF
R_{DT}	Resistance of optional differential termination circuit within a differential I/O pair. Not available on Input-only pairs.	V_{CCO} = 3.3V ± 10%	LVDS_33, MINI_LVDS_33, RSDS_33	90	100	115	Ω
		V_{CCO} = 2.5V ± 10%	LVDS_25, MINI_LVDS_25, RSDS_25	90	110	–	Ω

Notes:

1. The numbers in this table are based on the conditions set forth in Table 7.
2. For single-ended signals that are placed on a differential-capable I/O, V_{IN} of –0.2V to –0.5V is supported but can cause increased leakage between the two pins. See *Parasitic Leakage* in UG331, *Spartan-3 Generation FPGA User Guide*.
3. This parameter is based on characterization. The pull-up resistance R_{PU} = V_{CCO}/I_{RPU}. The pull-down resistance R_{PD} = V_{IN} / I_{RPD}.

Quiescent Current Requirements

Table 9: **Quiescent Supply Current Characteristics**(1)

Symbol	Description	Device	Power	Typical(2)	Commercial Maximum(2)	Industrial Maximum(2)	Units
I_{CCINTQ}	Quiescent V_{CCINT} supply current	XC3SD1800A	C,I	41	390	500	mA
			LI	36	–	175	mA
		XC3SD3400A	C,I	64	550	725	mA
			LI	55	–	300	mA
I_{CCOQ}	Quiescent V_{CCO} supply current	XC3SD1800A	C,I	0.4	4	5	mA
			LI	0.2	–	5	mA
		XC3SD3400A	C,I	0.4	4	5	mA
			LI	0.2	–	5	mA
I_{CCAUXQ}	Quiescent V_{CCAUX} supply current	XC3SD1800A	C,I	25	90	110	mA
			LI	24	–	72	mA
		XC3SD3400A	C,I	39	130	160	mA
			LI	38	–	105	mA

Notes:

1. The numbers in this table are based on the conditions set forth in Table 7.
2. Quiescent supply current is measured with all I/O drivers in a high-impedance state and with all pull-up/pull-down resistors at the I/O pads disabled. Typical values are characterized using typical devices at room temperature (T_J of 25°C at V_{CCINT} = 1.2V, V_{CCO} = 3.3V, and V_{CCAUX} = 2.5V). The maximum limits are tested for each device at the respective maximum specified junction temperature and at maximum voltage limits with V_{CCINT} = 1.26V, V_{CCO} = 3.6V, and V_{CCAUX} = 3.6V. The FPGA is programmed with a "blank" configuration data file (that is, a design with no functional elements instantiated). For conditions other than those described above (for example, a design including functional elements), measured quiescent current levels will be different than the values in the table.
3. For more accurate estimates for a specific design, use the Xilinx XPower tools. There are two recommended ways to estimate the total power consumption (quiescent plus dynamic) for a specific design: a) The Spartan-3A DSP FPGA XPower Estimator provides quick, approximate, typical estimates, and does not require a netlist of the design. b) XPower Analyzer uses a netlist as input to provide maximum estimates as well as more accurate typical estimates.
4. The maximum numbers in this table indicate the minimum current each power rail requires in order for the FPGA to power-on successfully.
5. For information on the power-saving Suspend mode, see XAPP480: *Using Suspend Mode in Spartan-3 Generation FPGAs*. Suspend mode typically saves 40% total power consumption compared to quiescent current.

Single-Ended I/O Standards

Table 10: **Recommended Operating Conditions for User I/Os Using Single-Ended Standards**

IOSTANDARD Attribute	V_{CCO} for Drivers[2]			V_{REF}			V_{IL}	V_{IH}[3]
	Min (V)	Nom (V)	Max (V)	Min (V)	Nom (V)	Max (V)	Max (V)	Min (V)
LVTTL	3.0	3.3	3.6	V_{REF} is not used for these I/O standards			0.8	2.0
LVCMOS33[4]	3.0	3.3	3.6				0.8	2.0
LVCMOS25[4,5]	2.3	2.5	2.7				0.7	1.7
LVCMOS18	1.65	1.8	1.95				0.4	0.8
LVCMOS15	1.4	1.5	1.6				0.4	0.8
LVCMOS12	1.1	1.2	1.3				0.4	0.7
PCI33_3[6]	3.0	3.3	3.6				0.3 • V_{CCO}	0.5 • V_{CCO}
PCI66_3[6]	3.0	3.3	3.6				0.3 • V_{CCO}	0.5 • V_{CCO}
HSTL_I	1.4	1.5	1.6	0.68	0.75	0.9	V_{REF} – 0.1	V_{REF} + 0.1
HSTL_III	1.4	1.5	1.6	–	0.9	–	V_{REF} – 0.1	V_{REF} + 0.1
HSTL_I_18	1.7	1.8	1.9	0.8	0.9	1.1	V_{REF} – 0.1	V_{REF} + 0.1
HSTL_II_18	1.7	1.8	1.9	–	0.9	–	V_{REF} – 0.1	V_{REF} + 0.1
HSTL_III_18	1.7	1.8	1.9	–	1.1	–	V_{REF} – 0.1	V_{REF} + 0.1
SSTL18_I	1.7	1.8	1.9	0.833	0.900	0.969	V_{REF} – 0.125	V_{REF} + 0.125
SSTL18_II	1.7	1.8	1.9	0.833	0.900	0.969	V_{REF} – 0.125	V_{REF} + 0.125
SSTL2_I	2.3	2.5	2.7	1.13	1.25	1.38	V_{REF} – 0.150	V_{REF} + 0.150
SSTL2_II	2.3	2.5	2.7	1.13	1.25	1.38	V_{REF} – 0.150	V_{REF} + 0.150
SSTL3_I	3.0	3.3	3.6	1.3	1.5	1.7	V_{REF} – 0.2	V_{REF} + 0.2
SSTL3_II	3.0	3.3	3.6	1.3	1.5	1.7	V_{REF} – 0.2	V_{REF} + 0.2

Notes:

1. Descriptions of the symbols used in this table are as follows:
   V_{CCO}—the supply voltage for output drivers
   V_{REF}—the reference voltage for setting the input switching threshold
   V_{IL}—the input voltage that indicates a Low logic level
   V_{IH}—the input voltage that indicates a High logic level
2. In general, the V_{CCO} rails supply only output drivers, not input circuits. The exceptions are for LVCMOS25 inputs when V_{CCAUX} = 3.3V range and for PCI I/O standards.
3. For device operation, the maximum signal voltage (V_{IH} max) can be as high as V_{IN} max. See Table 7.
4. There is approximately 100 mV of hysteresis on inputs using LVCMOS33 and LVCMOS25 I/O standards.
5. All Dedicated pins (PROG_B, DONE, SUSPEND, TCK, TDI, TDO, and TMS) draw power from the V_{CCAUX} rail and use the LVCMOS25 or LVCMOS33 standard depending on V_{CCAUX}. The Dual-Purpose configuration pins use the LVCMOS standard before the User mode. When using these pins as part of a standard 2.5V configuration interface, apply 2.5V to the V_{CCO} lines of Banks 0, 1, and 2 at power-on as well as throughout configuration.
6. For information on PCI IP solutions, see www.xilinx.com/pci. The PCI IOSTANDARD is not supported on input-only pins. The PCIX IOSTANDARD is available and has equivalent characteristics but no PCI-X IP is supported.

Table 11: **DC Characteristics of User I/Os Using Single-Ended Standards**

IOSTANDARD Attribute		Test Conditions		Logic Level Characteristics	
		I_{OL} (mA)	I_{OH} (mA)	V_{OL} Max (V)	V_{OH} Min (V)
LVTTL(3)	2	2	–2	0.4	2.4
	4	4	–4		
	6	6	–6		
	8	8	–8		
	12	12	–12		
	16	16	–16		
	24	24	–24		
LVCMOS33(3)	2	2	–2	0.4	V_{CCO} – 0.4
	4	4	–4		
	6	6	–6		
	8	8	–8		
	12	12	–12		
	16	16	–16		
	24(5)	24	–24		
LVCMOS25(3)	2	2	–2	0.4	V_{CCO} – 0.4
	4	4	–4		
	6	6	–6		
	8	8	–8		
	12	12	–12		
	16(5)	16	–16		
	24(5)	24	–24		
LVCMOS18(3)	2	2	–2	0.4	V_{CCO} – 0.4
	4	4	–4		
	6	6	–6		
	8	8	–8		
	12(5)	12	–12		
	16(5)	16	–16		
LVCMOS15(3)	2	2	–2	0.4	V_{CCO} – 0.4
	4	4	–4		
	6	6	–6		
	8(5)	8	–8		
	12(5)	12	–12		
LVCMOS12(3)	2	2	–2	0.4	V_{CCO} – 0.4
	4(5)	4	–4		
	6(5)	6	–6		

Table 11: **DC Characteristics of User I/Os Using Single-Ended Standards *(Cont'd)***

IOSTANDARD Attribute	Test Conditions		Logic Level Characteristics	
	I_{OL} (mA)	I_{OH} (mA)	V_{OL} Max (V)	V_{OH} Min (V)
PCI33_3(4)	1.5	–0.5	10% V_{CCO}	90% V_{CCO}
PCI66_3(4)	1.5	–0.5	10% V_{CCO}	90% V_{CCO}
HSTL_I (5)	8	–8	0.4	V_{CCO} – 0.4
HSTL_III (5)	24	–8	0.4	V_{CCO} – 0.4
HSTL_I_18	8	–8	0.4	V_{CCO} – 0.4
HSTL_II_18(5)	16	–16	0.4	V_{CCO} – 0.4
HSTL_III_18	24	–8	0.4	V_{CCO} – 0.4
SSTL18_I	6.7	–6.7	V_{TT} – 0.475	V_{TT} + 0.475
SSTL18_II(5)	13.4	–13.4	V_{TT} – 0.603	V_{TT} + 0.603
SSTL2_I	8.1	–8.1	V_{TT} – 0.61	V_{TT} + 0.61
SSTL2_II(5)	16.2	–16.2	V_{TT} – 0.81	V_{TT} + 0.81
SSTL3_I	8	–8	V_{TT} – 0.6	V_{TT} + 0.6
SSTL3_II(5)	16	–16	V_{TT} – 0.8	V_{TT} + 0.8

Notes:

1. The numbers in this table are based on the conditions set forth in Table 7 and Table 10.
2. Descriptions of the symbols used in this table are as follows:
   I_{OL}—the output current condition under which VOL is tested
   I_{OH}—the output current condition under which VOH is tested
   V_{OL}— the output voltage that indicates a Low logic level
   V_{OH}—the output voltage that indicates a High logic level
   V_{CCO}—the supply voltage for output drivers
   V_{TT}—the voltage applied to a resistor termination
3. For the LVCMOS and LVTTL standards: the same V_{OL} and V_{OH} limits apply for the Fast, Slow, and QUIETIO slew attributes.
4. Tested according to the relevant PCI specifications. For information on PCI IP solutions, see www.xilinx.com/products/design_resources/conn_central/protocols/pci_pcix.htm. The PCIX IOSTANDARD is available and has equivalent characteristics but no PCI-X IP is supported.
5. These higher-drive output standards are supported only on FPGA banks 1 and 3. Inputs are unrestricted. See the *Using I/O Resources* chapter in UG331.

Differential I/O Standards

Differential Input Pairs

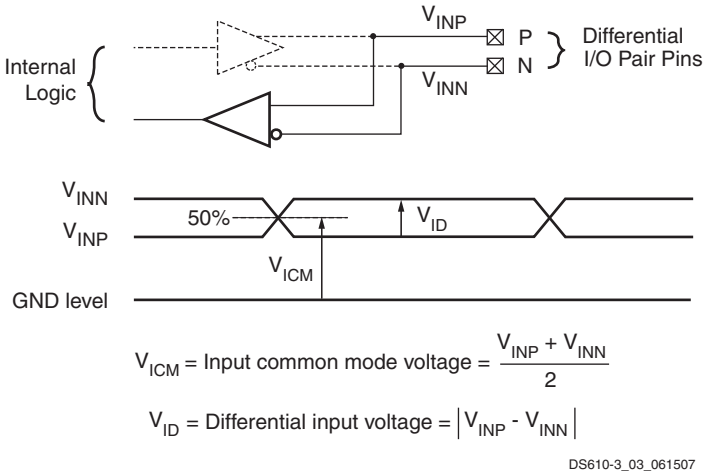


Figure 3: **Differential Input Voltages**

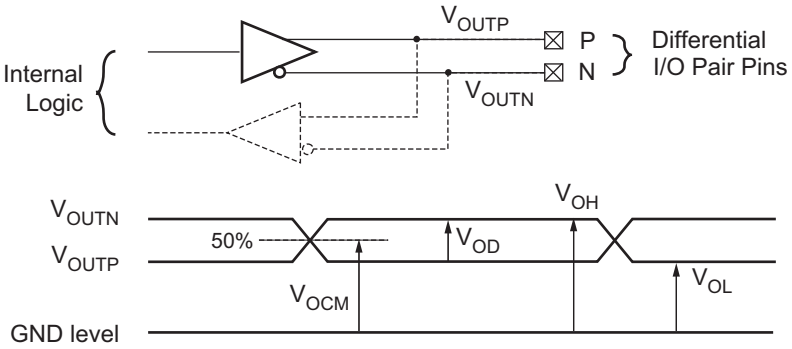
Table 12: **Recommended Operating Conditions for User I/Os Using Differential Signal Standards**

IOSTANDARD Attribute	V_{CCO} for Drivers[1]			V_{ID}			V_{ICM}[2]		
	Min (V)	Nom (V)	Max (V)	Min (mV)	Nom (mV)	Max (mV)	Min (V)	Nom (V)	Max (V)
LVDS_25[3]	2.25	2.5	2.75	100	350	600	0.3	1.25	2.35
LVDS_33[3]	3.0	3.3	3.6	100	350	600	0.3	1.25	2.35
BLVDS_25[4]	2.25	2.5	2.75	100	300	–	0.3	1.3	2.35
MINI_LVDS_25[3]	2.25	2.5	2.75	200	–	600	0.3	1.2	1.95
MINI_LVDS_33[3]	3.0	3.3	3.6	200	–	600	0.3	1.2	1.95
LVPECL_25[5]	Inputs Only			100	800	1000	0.3	1.2	1.95
LVPECL_33[5]	Inputs Only			100	800	1000	0.3	1.2	2.8[6]
RSDS_25[3]	2.25	2.5	2.75	100	200	–	0.3	1.2	1.5
RSDS_33[3]	3.0	3.3	3.6	100	200	–	0.3	1.2	1.5
TMDS_33[3,4,7]	3.14	3.3	3.47	150	–	1200	2.7	–	3.23
PPDS_25[3]	2.25	2.5	2.75	100	–	400	0.2	–	2.3
PPDS_33[3]	3.0	3.3	3.6	100	–	400	0.2	–	2.3
DIFF_HSTL_I_18	1.7	1.8	1.9	100	–	–	0.8	–	1.1
DIFF_HSTL_II_18[8]	1.7	1.8	1.9	100	–	–	0.8	–	1.1
DIFF_HSTL_III_18	1.7	1.8	1.9	100	–	–	0.8	–	1.1
DIFF_HSTL_I	1.4	1.5	1.6	100	–	–	0.68	–	0.9
DIFF_HSTL_III	1.4	1.5	1.6	100	–	–	–	0.9	–
DIFF_SSTL18_I	1.7	1.8	1.9	100	–	–	0.7	–	1.1
DIFF_SSTL18_II[8]	1.7	1.8	1.9	100	–	–	0.7	–	1.1
DIFF_SSTL2_I	2.3	2.5	2.7	100	–	–	1.0	–	1.5
DIFF_SSTL2_II[8]	2.3	2.5	2.7	100	–	–	1.0	–	1.5
DIFF_SSTL3_I	3.0	3.3	3.6	100	–	–	1.1	–	1.9
DIFF_SSTL3_II	3.0	3.3	3.6	100	–	–	1.1	–	1.9

Notes:

1. The V_{CCO} rails supply only differential output drivers, not input circuits.
2. V_{ICM} must be less than V_{CCAUX}.
3. These true differential output standards are supported only on FPGA banks 0 and 2. Inputs are unrestricted. See the chapter "Using I/O Resources" in UG331.
4. See "External Termination Requirements for Differential I/O."
5. LVPECL is supported on inputs only, not outputs. LVPECL_33 requires V_{CCAUX} = 3.3V ± 10%.
6. LVPECL_33 maximum V_{ICM} = the lower of 2.8V or $V_{CCAUX} - (V_{ID}/2)$.
7. Requires V_{CCAUX} = 3.3V ±10%. (V_{CCAUX} - 300 mV) ≤ V_{ICM} ≤ (V_{CCAUX} - 37 mV).
8. These higher-drive output standards are supported only on FPGA banks 1 and 3. Inputs are unrestricted. See the chapter "Using I/O Resources" in UG331.
9. All standards except for LVPECL and TMDS can have VCCAUX at either 2.5V or 3.3V. Define your VCCAUX level using the CONFIG VCCAUX constraint.

Differential Output Pairs



V_{OCM} = Output common mode voltage = $\frac{V_{OUTP} + V_{OUTN}}{2}$

V_{OD} = Output differential voltage = $|V_{OUTP} - V_{OUTN}|$

V_{OH} = Output voltage indicating a High logic level

V_{OL} = Output voltage indicating a Low logic level

DS312-3_03_090510

Figure 4: **Differential Output Voltages**

Table 13: **DC Characteristics of User I/Os Using Differential Signal Standards**

IOSTANDARD Attribute	V_{OD}			V_{OCM}			V_{OH}	V_{OL}
	Min (mV)	Typ (mV)	Max (mV)	Min (V)	Typ (V)	Max (V)	Min (V)	Max (V)
LVDS_25	247	350	454	1.125	–	1.375	–	–
LVDS_33	247	350	454	1.125	–	1.375	–	–
BLVDS_25	240	350	460	–	1.30	–	–	–
MINI_LVDS_25	300	–	600	1.0	–	1.4	–	–
MINI_LVDS_33	300	–	600	1.0	–	1.4	–	–
RSDS_25	100	–	400	1.0	–	1.4	–	–
RSDS_33	100	–	400	1.0	–	1.4	–	–
TMDS_33	400	–	800	V_{CCO} – 0.405	–	V_{CCO} – 0.190	–	–
PPDS_25	100	–	400	0.5	0.8	1.4	–	–
PPDS_33	100	–	400	0.5	0.8	1.4	–	–
DIFF_HSTL_I_18	–	–	–	–	–	–	V_{CCO} – 0.4	0.4
DIFF_HSTL_II_18	–	–	–	–	–	–	V_{CCO} – 0.4	0.4
DIFF_HSTL_III_18	–	–	–	–	–	–	V_{CCO} – 0.4	0.4
DIFF_HSTL_I	–	–	–	–	–	–	V_{CCO} – 0.4	0.4
DIFF_HSTL_III	–	–	–	–	–	–	V_{CCO} – 0.4	0.4
DIFF_SSTL18_I	–	–	–	–	–	–	V_{TT} + 0.475	V_{TT} – 0.475
DIFF_SSTL18_II	–	–	–	–	–	–	V_{TT} + 0.603	V_{TT} – 0.603
DIFF_SSTL2_I	–	–	–	–	–	–	V_{TT} + 0.61	V_{TT} – 0.61
DIFF_SSTL2_II	–	–	–	–	–	–	V_{TT} + 0.81	V_{TT} – 0.81
DIFF_SSTL3_I	–	–	–	–	–	–	V_{TT} + 0.6	V_{TT} - 0.6
DIFF_SSTL3_II	–	–	–	–	–	–	V_{TT} + 0.8	V_{TT} - 0.8

Notes:

1. The numbers in this table are based on the conditions set forth in Table 7 and Table 12.
2. See "External Termination Requirements for Differential I/O."
3. Output voltage measurements for all differential standards are made with a termination resistor (R_T) of 100Ω across the N and P pins of the differential signal pair.
4. At any given time, no more than two of the following differential output standards can be assigned to an I/O bank: LVDS_25, RSDS_25, MINI_LVDS_25, PPDS_25 when V_{CCO}=2.5V, or LVDS_33, RSDS_33, MINI_LVDS_33, TMDS_33, PPDS_33 when V_{CCO} = 3.3V

External Termination Requirements for Differential I/O

LVDS, RSDS, MINI_LVDS, and PPDS I/O Standards

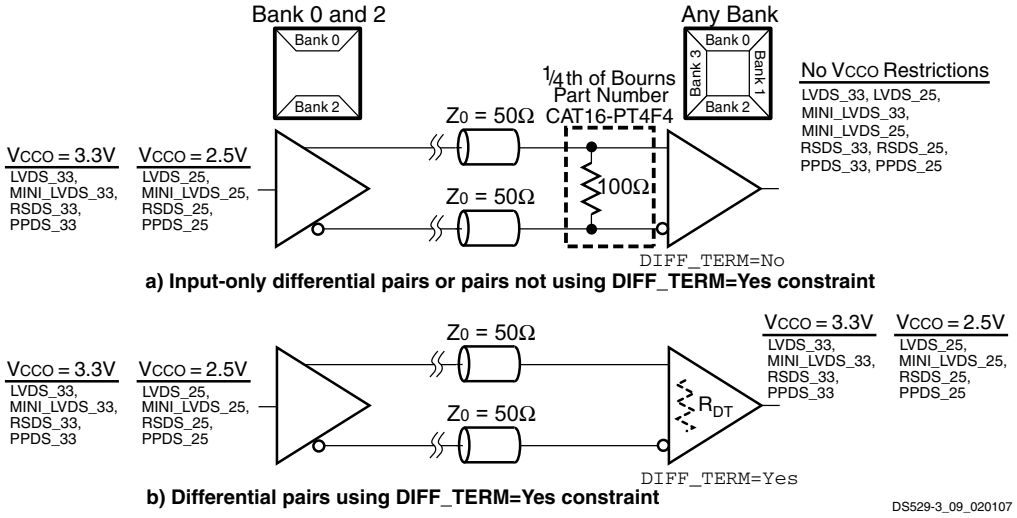


Figure 5: **External Input Termination for LVDS, RSDS, MINI_LVDS, and PPDS I/O Standards**

BLVDS_25 I/O Standard

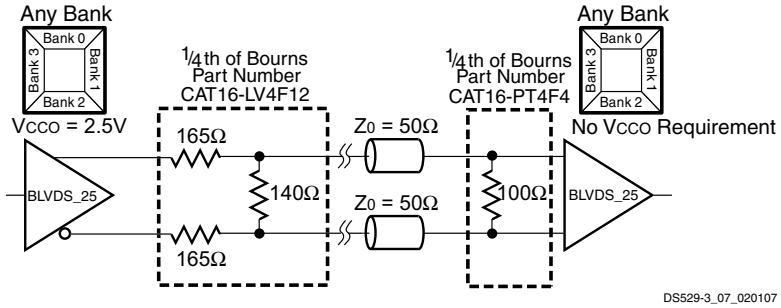


Figure 6: **External Output and Input Termination Resistors for BLVDS_25 I/O Standard**

TMDS_33 I/O Standard

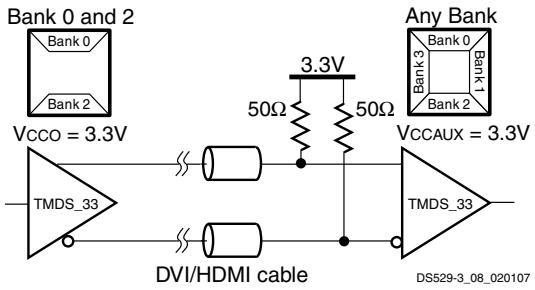


Figure 7: **External Input Resistors Required for TMDS_33 I/O Standard**

Device DNA Read Endurance

Table 14: **Device DNA Identifier Memory Characteristics**

Symbol	Description	Minimum	Units
DNA_CYCLES	Number of READ operations or JTAG ISC_DNA read operations. Unaffected by HOLD or SHIFT operations.	30,000,000	Read cycles

Switching Characteristics

All Spartan-3A DSP FPGAs ship in two speed grades: –4 and the higher performance –5. Switching characteristics in this document are designated as Advance, Preliminary, or Production, as shown in Table 15. Each category is defined as follows:

Advance: These specifications are based on simulations only and are typically available soon after establishing FPGA specifications. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary: These specifications are based on complete early silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting preliminary delays is greatly reduced compared to Advance data.

Production: These specifications are approved once enough production silicon of a particular device family member has been characterized to provide full correlation between speed files and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

Software Version Requirements

Production-quality systems must use FPGA designs compiled using a speed file designated as PRODUCTION status. FPGAs designs using a less mature speed file designation should only be used during system prototyping or pre-production qualification. FPGA designs with speed files designated as Preview, Advance, or Preliminary should not be used in a production-quality system.

Whenever a speed file designation changes, as a device matures toward Production status, rerun the latest Xilinx® ISE® software on the FPGA design to ensure that the FPGA design incorporates the latest timing information and software updates.

Production designs will require updating the Xilinx ISE development software with a future version and/or Service Pack.

All parameter limits are representative of worst-case supply voltage and junction temperature conditions. **Unless otherwise noted, the published parameter values apply to all Spartan-3A DSP devices. AC and DC characteristics are specified using the same numbers for both commercial and industrial grades.**

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Timing parameters and their representative values are selected for inclusion below either because they are important as general design requirements or they indicate fundamental device performance characteristics. The Spartan-3A DSP FPGA speed files (v1.32), part of the Xilinx Development Software, are the original source for many but not all of the values. The speed grade designations for these files are shown in Table 15. For more complete, more precise, and worst-case data, use the values reported by the Xilinx static timing analyzer (TRACE in the Xilinx development software) and back-annotated to the simulation netlist.

Table 15: **Spartan-3A DSP v1.32 Speed Grade Designations**

Device	Advance	Preliminary	Production
XC3SD1800A			-4, -5
XC3SD3400A			-4, -5

Table 16 provides the recent history of the Spartan-3A DSP FPGA speed files.

Table 16: **Spartan-3A DSP Speed File Version History**

Version	ISE Release	Description
1.32	ISE 10.1.02	Updated DSP timing model to reflect higher performance for some implementations
1.31	ISE 10.1	Added Automotive support
1.30	ISE 9.2.03i	Added absolute minimum values
1.29	ISE 9.2.01i	Production Speed Files for -4 and -5 speed grades
1.28	ISE 9.2i	Minor updates
1.27	ISE 9.1.03i	Advance Speed Files for -4 speed grade

I/O Timing

Pin-to-Pin Clock-to-Output Times

Table 17: **Pin-to-Pin Clock-to-Output Times for the IOB Output Path**

Symbol	Description	Conditions	Device	Speed Grade		Units
				-5	-4	
				Max	Max	
Clock-to-Output Times						
$T_{ICKOFDCM}$	When reading from the Output Flip-Flop (OFF), the time from the active transition on the Global Clock pin to data appearing at the Output pin. The DCM is in use.	LVCMOS25(2), 12 mA output drive, Fast slew rate, with DCM(3)	XC3SD1800A	3.28	3.51	ns
			XC3SD3400A	3.36	3.82	ns
T_{ICKOF}	When reading from OFF, the time from the active transition on the Global Clock pin to data appearing at the Output pin. The DCM is not in use.	LVCMOS25(2), 12 mA output drive, Fast slew rate, without DCM	XC3SD1800A	5.23	5.58	ns
			XC3SD3400A	5.51	6.13	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 26 and are based on the operating conditions set forth in Table 7 and Table 10.
2. This clock-to-output time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the Global Clock Input or a standard other than LVCMOS25 with 12 mA drive and Fast slew rate is assigned to the data Output. If the former is true, *add* the appropriate Input adjustment from Table 22. If the latter is true, *add* the appropriate Output adjustment from Table 25.
3. DCM output jitter is included in all measurements.

Pin-to-Pin Setup and Hold Times

Table 18: **Pin-to-Pin Setup and Hold Times for the IOB Input Path (System Synchronous)**

Symbol	Description	Conditions	Device	Speed Grade		Units
				-5	-4	
				Max	Max	
Setup Times						
T_{PSDCM}	When writing to the Input Flip-Flop (IFF), the time from the setup of data at the Input pin to the active transition at a Global Clock pin. The DCM is in use. No Input Delay is programmed.	LVCMOS25(2), IFD_DELAY_VALUE = 0, with DCM(4)	XC3SD1800A	2.65	3.11	ns
			XC3SD3400A	2.25	2.49	ns
T_{PSFD}	When writing to IFF, the time from the setup of data at the Input pin to an active transition at the Global Clock pin. The DCM is not in use. The Input Delay is programmed.	LVCMOS25(2), IFD_DELAY_VALUE = 6, without DCM	XC3SD1800A	2.98	3.39	ns
			XC3SD3400A	2.78	3.08	ns
Hold Times						
T_{PHDCM}	When writing to IFF, the time from the active transition at the Global Clock pin to the point when data must be held at the Input pin. The DCM is in use. No Input Delay is programmed.	LVCMOS25(3), IFD_DELAY_VALUE = 0, with DCM(4)	XC3SD1800A	–0.38	–0.38	ns
			XC3SD3400A	–0.26	–0.26	ns
T_{PHFD}	When writing to IFF, the time from the active transition at the Global Clock pin to the point when data must be held at the Input pin. The DCM is not in use. The Input Delay is programmed.	LVCMOS25(3), IFD_DELAY_VALUE = 6, without DCM	XC3SD1800A	–0.71	–0.71	ns
			XC3SD3400A	–0.65	–0.65	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 26 and are based on the operating conditions set forth in Table 7 and Table 10.
2. This setup time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the Global Clock Input or the data Input. If this is true of the Global Clock Input, subtract the appropriate adjustment from Table 22. If this is true of the data Input, add the appropriate Input adjustment from the same table.
3. This hold time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the Global Clock Input or the data Input. If this is true of the Global Clock Input, add the appropriate Input adjustment from Table 22. If this is true of the data Input, subtract the appropriate Input adjustment from the same table. When the hold time is negative, it is possible to change the data before the clock's active edge.
4. DCM output jitter is included in all measurements.

Input Setup and Hold Times

Table 19: **Setup and Hold Times for the IOB Input Path**

Symbol	Description	Conditions	DELAY_ VALUE	Device	Speed		Units
					-5	-4	
					Min	Min	
Setup Times							
T_{IOPICK}	Time from the setup of data at the Input pin to the active transition at the ICLK input of the Input Flip-Flop (IFF). No Input Delay is programmed.	LVCMOS25(2)	IFD_DELAY_VALUE=0	XC3SD1800A	1.65	1.81	ns
				XC3SD3400A	1.51	1.88	ns
$T_{IOPICKD}$	Time from the setup of data at the Input pin to the active transition at the ICLK input of the Input Flip-Flop (IFF). The Input Delay is programmed.	LVCMOS25(2)	1	XC3SD1800A	2.09	2.24	ns
			2		2.67	2.83	ns
			3		3.25	3.64	ns
			4		3.75	4.20	ns
			5		3.69	4.16	ns
			6		4.47	5.09	ns
			7		5.27	6.02	ns
			8		5.79	6.63	ns
			1	XC3SD3400A	2.07	2.44	ns
			2		2.57	3.02	ns
			3		3.44	3.81	ns
			4		4.01	4.39	ns
			5		3.89	4.26	ns
			6		4.43	5.08	ns
			7		5.20	5.95	ns
			8		5.70	6.55	ns
Hold Times							
T_{IOICKP}	Time from the active transition at the ICLK input of the Input Flip-Flop (IFF) to the point where data must be held at the Input pin. No Input Delay is programmed.	LVCMOS25(3)	0	XC3SD1800A	–0.63	–0.52	ns
				XC3SD3400A	–0.56	–0.56	ns

Table 19: **Setup and Hold Times for the IOB Input Path *(Cont'd)***

Symbol	Description	Conditions	DELAY_ VALUE	Device	Speed		Units
					-5	-4	
					Min	Min	
$T_{IOICKPD}$	Time from the active transition at the ICLK input of the Input Flip-Flop (IFF) to the point where data must be held at the Input pin. The Input Delay is programmed.	LVCMOS25(3)	1	XC3SD1800A	–1.40	–1.40	ns
			2		–2.11	–2.11	ns
			3		–2.48	–2.48	ns
			4		–2.77	–2.77	ns
			5		–2.62	–2.62	ns
			6		–3.06	–3.06	ns
			7		–3.42	–3.42	ns
			8		–3.65	–3.65	ns
			1	XC3SD3400A	–1.31	–1.31	ns
			2		–1.88	–1.88	ns
			3		–2.44	–2.44	ns
			4		–2.89	–2.89	ns
			5		–2.83	–2.83	ns
			6		–3.33	–3.33	ns
			7		–3.63	–3.63	ns
			8		–3.96	–3.96	ns
Set/Reset Pulse Width							
T_{RPW_IOB}	Minimum pulse width to SR control input on IOB	–	–	All	1.33	1.61	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 26 and are based on the operating conditions set forth in Table 7 and Table 10.
2. This setup time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the data Input. If this is true, add the appropriate Input adjustment from Table 22.
3. These hold times require adjustment whenever a signal standard other than LVCMOS25 is assigned to the data Input. If this is true, subtract the appropriate Input adjustment from Table 22. When the hold time is negative, it is possible to change the data before the clock's active edge.

Table 20: **Sample Window (Source Synchronous)**

Symbol	Description	Max	Units
T_{SAMP}	Setup and hold capture window of an IOB flip-flop.	The input capture sample window value is highly specific to a particular application, device, package, I/O standard, I/O placement, DCM usage, and clock buffer. Please consult the appropriate Xilinx Answer Record for application-specific values. • Answer Record 30879	ps

Input Propagation Times

Table 21: **Propagation Times for the IOB Input Path**

Symbol	Description	Conditions	DELAY_VALUE	Device	Speed Grade		Units
					-5	-4	
					Max	Max	
Propagation Times							
T_{IOPI}	The time it takes for data to travel from the Input pin to the I output with no input delay programmed	LVCMOS25[2]	IBUF_DELAY_VALUE=0	XC3SD1800A	0.51	0.53	ns
				XC3SD3400A	0.73	0.93	ns
T_{IOPID}	The time it takes for data to travel from the Input pin to the I output with the input delay programmed	LVCMOS25[2]	1	XC3SD1800A	1.29	1.62	ns
			2		1.67	2.08	ns
			3		1.92	2.36	ns
			4		2.38	2.89	ns
			5		2.61	3.17	ns
			6		2.98	3.55	ns
			7		3.30	3.92	ns
			8		3.63	4.37	ns
			9		3.31	4.02	ns
			10		3.69	4.47	ns
			11		3.94	4.77	ns
			12		4.41	5.27	ns
			13		4.67	5.56	ns
			14		5.03	5.94	ns
			15		5.36	6.31	ns
			16		5.64	6.73	ns
			1	XC3SD3400A	1.56	1.99	ns
			2		1.92	2.44	ns
			3		2.18	2.72	ns
			4		2.66	3.19	ns
			5		2.91	3.43	ns
			6		3.27	3.81	ns
			7		3.59	4.17	ns
			8		3.87	4.58	ns
			9		3.52	4.22	ns
			10		3.87	4.65	ns
			11		4.14	4.94	ns
			12		4.68	5.40	ns
			13		4.93	5.66	ns
			14		5.29	6.06	ns
			15		5.61	6.43	ns
			16		5.88	6.80	ns

Table 21: **Propagation Times for the IOB Input Path *(Cont'd)***

Symbol	Description	Conditions	DELAY_VALUE	Device	Speed Grade		Units
					-5	-4	
					Max	Max	
T_{IOPLI}	The time it takes for data to travel from the Input pin through the IFF latch to the I output with no input delay programmed	LVCMOS25(2)	0	XC3SD1800A	1.79	2.04	ns
				XC3SD3400A	1.65	2.11	ns
T_{IOPLID}	The time it takes for data to travel from the Input pin through the IFF latch to the I output with the input delay programmed	LVCMOS25(2)	1	XC3SD1800A	2.23	2.47	ns
			2		2.81	3.06	ns
			3		3.39	3.86	ns
			4		3.89	4.43	ns
			5		3.83	4.39	ns
			6		4.61	5.32	ns
			7		5.40	6.24	ns
			8		5.93	6.86	ns
			1	XC3SD3400A	2.21	2.67	ns
			2		2.71	3.25	ns
			3		3.58	4.04	ns
			4		4.15	4.62	ns
			5		4.03	4.49	ns
			6		4.57	5.31	ns
			7		5.34	6.18	ns
			8		5.84	6.78	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 26 and are based on the operating conditions set forth in Table 7 and Table 10.
2. This propagation time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the data Input. When this is true, *add* the appropriate Input adjustment from Table 22.

Input Timing Adjustments

Table 22: **Input Timing Adjustments by IOSTANDARD**

Convert Input Time from LVCMOS25 to the Following Signal Standard (IOSTANDARD)	Add the Adjustment Below		Units
	Speed Grade		
	-5	-4	
Single-Ended Standards			
LVTTL	0.62	0.62	ns
LVCMOS33	0.54	0.54	ns
LVCMOS25	0.00	0.00	ns
LVCMOS18	0.83	0.83	ns
LVCMOS15	0.60	0.60	ns
LVCMOS12	0.31	0.31	ns
PCI33_3	0.41	0.41	ns
PCI66_3	0.41	0.41	ns
HSTL_I	0.72	0.72	ns
HSTL_III	0.77	0.77	ns
HSTL_I_18	0.69	0.69	ns
HSTL_II_18	0.69	0.69	ns
HSTL_III_18	0.79	0.79	ns
SSTL18_I	0.71	0.71	ns
SSTL18_II	0.71	0.71	ns
SSTL2_I	0.68	0.68	ns
SSTL2_II	0.68	0.68	ns
SSTL3_I	0.78	0.78	ns
SSTL3_II	0.78	0.78	ns

Table 22: **Input Timing Adjustments by IOSTANDARD**

Convert Input Time from LVCMOS25 to the Following Signal Standard (IOSTANDARD)	Add the Adjustment Below		Units
	Speed Grade		
	-5	-4	
Differential Standards			
LVDS_25	0.76	0.76	ns
LVDS_33	0.79	0.79	ns
BLVDS_25	0.79	0.79	ns
MINI_LVDS_25	0.78	0.78	ns
MINI_LVDS_33	0.79	0.79	ns
LVPECL_25	0.78	0.78	ns
LVPECL_33	0.79	0.79	ns
RSDS_25	0.79	0.79	ns
RSDS_33	0.77	0.77	ns
TMDS_33	0.79	0.79	ns
PPDS_25	0.79	0.79	ns
PPDS_33	0.79	0.79	ns
DIFF_HSTL_I_18	0.74	0.74	ns
DIFF_HSTL_II_18	0.72	0.72	ns
DIFF_HSTL_III_18	1.05	1.05	ns
DIFF_HSTL_I	0.72	0.72	ns
DIFF_HSTL_III	1.05	1.05	ns
DIFF_SSTL18_I	0.71	0.71	ns
DIFF_SSTL18_II	0.71	0.71	ns
DIFF_SSTL2_I	0.74	0.74	ns
DIFF_SSTL2_II	0.75	0.75	ns
DIFF_SSTL3_I	1.06	1.06	ns
DIFF_SSTL3_II	1.06	1.06	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 26 and are based on the operating conditions set forth in Table 7, Table 10, and Table 12.
2. These adjustments are used to convert input path times originally specified for the LVCMOS25 standard to times that correspond to other signal standards.

Output Propagation Times

Table 23: **Timing for the IOB Output Path**

Symbol	Description	Conditions	Device	Speed Grade		Units
				-5	-4	
				Max	Max	
Clock-to-Output Times						
T_{IOCKP}	When reading from the Output Flip-Flop (OFF), the time from the active transition at the OCLK input to data appearing at the Output pin	LVCMOS25(2), 12 mA output drive, Fast slew rate	All	2.87	3.13	ns
Propagation Times						
T_{IOOP}	The time it takes for data to travel from the IOB's O input to the Output pin	LVCMOS25(2), 12 mA output drive, Fast slew rate	All	2.78	2.91	ns
Set/Reset Times						
T_{IOSRP}	Time from asserting the OFF's SR input to setting/resetting data at the Output pin	LVCMOS25(2), 12 mA output drive, Fast slew rate	All	3.63	3.89	ns
T_{IOGSRQ}	Time from asserting the Global Set Reset (GSR) input on the STARTUP_SPARTAN3A primitive to setting/resetting data at the Output pin			8.62	9.65	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 26 and are based on the operating conditions set forth in Table 7 and Table 10.
2. This time requires adjustment whenever a signal standard other than LVCMOS25 with 12 mA drive and Fast slew rate is assigned to the data Output. When this is true, *add* the appropriate Output adjustment from Table 25.

Three-State Output Propagation Times

Table 24: **Timing for the IOB Three-State Path**

Symbol	Description	Conditions	Device	Speed Grade		Units
				-5	-4	
				Max	Max	
Synchronous Output Enable/Disable Times						
T_{IOCKHZ}	Time from the active transition at the OTCLK input of the Three-state Flip-Flop (TFF) to when the Output pin enters the high-impedance state	LVCMOS25, 12 mA output drive, Fast slew rate	All	1.13	1.39	ns
T_{IOCKON} (2)	Time from the active transition at TFF's OTCLK input to when the Output pin drives valid data		All	3.08	3.35	ns
Asynchronous Output Enable/Disable Times						
T_{GTS}	Time from asserting the Global Three State (GTS) input on the STARTUP_SPARTAN3A primitive to when the Output pin enters the high-impedance state	LVCMOS25, 12 mA output drive, Fast slew rate	All	9.47	10.36	ns
Set/Reset Times						
T_{IOSRHZ}	Time from asserting TFF's SR input to when the Output pin enters a high-impedance state	LVCMOS25, 12 mA output drive, Fast slew rate	All	1.61	1.86	ns
T_{IOSRON} (2)	Time from asserting TFF's SR input at TFF to when the Output pin drives valid data		All	3.57	3.82	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 26 and are based on the operating conditions set forth in Table 7 and Table 10.
2. This time requires adjustment whenever a signal standard other than LVCMOS25 with 12 mA drive and Fast slew rate is assigned to the data Output. When this is true, *add* the appropriate Output adjustment from Table 25.

Output Timing Adjustments

Table 25: **Output Timing Adjustments for IOB**

Convert Output Time from LVCMOS25 with 12mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD)			Add the Adjustment Below		Units
			Speed Grade		
			-5	-4	
Single-Ended Standards					
LVTTL	Slow	2 mA	5.58	5.58	ns
		4 mA	3.16	3.16	ns
		6 mA	3.17	3.17	ns
		8 mA	2.09	2.09	ns
		12 mA	1.62	1.62	ns
		16 mA	1.24	1.24	ns
		24 mA	2.74(3)	2.74(3)	ns
	Fast	2 mA	3.03	3.03	ns
		4 mA	1.71	1.71	ns
		6 mA	1.71	1.71	ns
		8 mA	0.53	0.53	ns
		12 mA	0.53	0.53	ns
		16 mA	0.59	0.59	ns
		24 mA	0.60	0.60	ns
	QuietIO	2 mA	27.67	27.67	ns
		4 mA	27.67	27.67	ns
		6 mA	27.67	27.67	ns
		8 mA	16.71	16.71	ns
		12 mA	16.67	16.67	ns
		16 mA	16.22	16.22	ns
		24 mA	12.11	12.11	ns

Table 25: **Output Timing Adjustments for IOB *(Cont'd)***

Convert Output Time from LVCMOS25 with 12mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD)			Add the Adjustment Below		Units
			Speed Grade		
			-5	-4	
LVCMOS33	Slow	2 mA	5.58	5.58	ns
		4 mA	3.17	3.17	ns
		6 mA	3.17	3.17	ns
		8 mA	2.09	2.09	ns
		12 mA	1.24	1.24	ns
		16 mA	1.15	1.15	ns
		24 mA	2.55(3)	2.55(3)	ns
	Fast	2 mA	3.02	3.02	ns
		4 mA	1.71	1.71	ns
		6 mA	1.72	1.72	ns
		8 mA	0.53	0.53	ns
		12 mA	0.59	0.59	ns
		16 mA	0.59	0.59	ns
		24 mA	0.51	0.51	ns
	QuietIO	2 mA	27.67	27.67	ns
		4 mA	27.67	27.67	ns
		6 mA	27.67	27.67	ns
		8 mA	16.71	16.71	ns
		12 mA	16.29	16.29	ns
		16 mA	16.18	16.18	ns
		24 mA	12.11	12.11	ns

Table 25: **Output Timing Adjustments for IOB *(Cont'd)***

Convert Output Time from LVCMOS25 with 12mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD)			Add the Adjustment Below		Units
			Speed Grade		
			-5	-4	
LVCMOS25	Slow	2 mA	5.33	5.33	ns
		4 mA	2.81	2.81	ns
		6 mA	2.82	2.82	ns
		8 mA	1.14	1.14	ns
		12 mA	1.10	1.10	ns
		16 mA	0.83	0.83	ns
		24 mA	2.26(3)	2.26(3)	ns
	Fast	2 mA	4.36	4.36	ns
		4 mA	1.76	1.76	ns
		6 mA	1.25	1.25	ns
		8 mA	0.38	0.38	ns
		12 mA	0.00	0.00	ns
		16 mA	0.01	0.01	ns
		24 mA	0.01	0.01	ns
	QuietIO	2 mA	25.92	25.92	ns
		4 mA	25.92	25.92	ns
		6 mA	25.92	25.92	ns
		8 mA	15.57	15.57	ns
		12 mA	15.59	15.59	ns
		16 mA	14.27	14.27	ns
		24 mA	11.37	11.37	ns

Table 25: **Output Timing Adjustments for IOB *(Cont'd)***

Convert Output Time from LVCMOS25 with 12mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD)			Add the Adjustment Below		Units
			Speed Grade		
			-5	-4	
LVCMOS18	Slow	2 mA	4.48	4.48	ns
		4 mA	3.69	3.69	ns
		6 mA	2.91	2.91	ns
		8 mA	1.99	1.99	ns
		12 mA	1.57	1.57	ns
		16 mA	1.19	1.19	ns
	Fast	2 mA	3.96	3.96	ns
		4 mA	2.57	2.57	ns
		6 mA	1.90	1.90	ns
		8 mA	1.06	1.06	ns
		12 mA	0.83	0.83	ns
		16 mA	0.63	0.63	ns
	QuietIO	2 mA	24.97	24.97	ns
		4 mA	24.97	24.97	ns
		6 mA	24.08	24.08	ns
		8 mA	16.43	16.43	ns
		12 mA	14.52	14.52	ns
		16 mA	13.41	13.41	ns
LVCMOS15	Slow	2 mA	5.82	5.82	ns
		4 mA	3.97	3.97	ns
		6 mA	3.21	3.21	ns
		8 mA	2.53	2.53	ns
		12 mA	2.06	2.06	ns
	Fast	2 mA	5.23	5.23	ns
		4 mA	3.05	3.05	ns
		6 mA	1.95	1.95	ns
		8 mA	1.60	1.60	ns
		12 mA	1.30	1.30	ns
	QuietIO	2 mA	34.11	34.11	ns
		4 mA	25.66	25.66	ns
		6 mA	24.64	24.64	ns
		8 mA	22.06	22.06	ns
		12 mA	20.64	20.64	ns

Table 25: **Output Timing Adjustments for IOB *(Cont'd)***

Convert Output Time from LVCMOS25 with 12mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD)			Add the Adjustment Below		Units
			Speed Grade		
			-5	-4	
LVCMOS12	Slow	2 mA	7.14	7.14	ns
		4 mA	4.87	4.87	ns
		6 mA	5.67	5.67	ns
	Fast	2 mA	6.77	6.77	ns
		4 mA	5.02	5.02	ns
		6 mA	4.09	4.09	ns
	QuietIO	2 mA	50.76	50.76	ns
		4 mA	43.17	43.17	ns
		6 mA	37.31	37.31	ns
PCI33_3			0.34	0.34	ns
PCI66_3			0.34	0.34	ns
HSTL_I			0.78	0.78	ns
HSTL_III			1.16	1.16	ns
HSTL_I_18			0.35	0.35	ns
HSTL_II_18			0.30	0.30	ns
HSTL_III_18			0.47	0.47	ns
SSTL18_I			0.40	0.40	ns
SSTL18_II			0.30	0.30	ns
SSTL2_I			0.00	0.00	ns
SSTL2_II			–0.05	–0.05	ns
SSTL3_I			0.00	0.00	ns
SSTL3_II			0.17	0.17	ns

Table 25: **Output Timing Adjustments for IOB *(Cont'd)***

Convert Output Time from LVCMOS25 with 12mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD)	Add the Adjustment Below		Units
	Speed Grade		
	-5	-4	
Differential Standards			
LVDS_25	1.16	1.16	ns
LVDS_33	0.46	0.46	ns
BLVDS_25	0.11	0.11	ns
MINI_LVDS_25	0.75	0.75	ns
MINI_LVDS_33	0.40	0.40	ns
LVPECL_25	Inputs Only		
LVPECL_33			
RSDS_25	1.42	1.42	ns
RSDS_33	0.58	0.58	ns
TMDS_33	0.46	0.46	ns
PPDS_25	1.07	1.07	ns
PPDS_33	0.63	0.63	ns
DIFF_HSTL_I_18	0.43	0.43	ns
DIFF_HSTL_II_18	0.41	0.41	ns
DIFF_HSTL_III_18	0.36	0.36	ns
DIFF_HSTL_I	1.01	1.01	ns
DIFF_HSTL_III	0.54	0.54	ns
DIFF_SSTL18_I	0.49	0.49	ns
DIFF_SSTL18_II	0.41	0.41	ns
DIFF_SSTL2_I	0.82	0.82	ns
DIFF_SSTL2_II	0.09	0.09	ns
DIFF_SSTL3_I	1.16	1.16	ns
DIFF_SSTL3_II	0.28	0.28	ns

Notes:

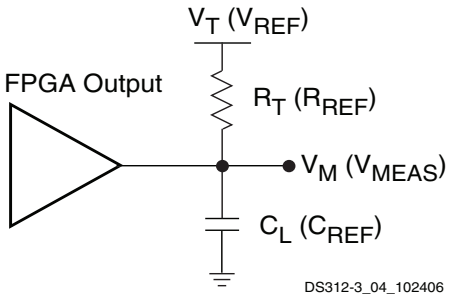
1. The numbers in this table are tested using the methodology presented in Table 26 and are based on the operating conditions set forth in Table 7, Table 10, and Table 12.
2. These adjustments are used to convert output- and three-state-path times originally specified for the LVCMOS25 standard with 12 mA drive and Fast slew rate to times that correspond to other signal standards. Do not adjust times that measure when outputs go into a high-impedance state.
3. Note that 16 mA drive is faster than 24 mA drive for the Slow slew rate.

Timing Measurement Methodology

When measuring timing parameters at the programmable I/Os, different signal standards call for different test conditions. Table 26 lists the conditions to use for each standard.

The method for measuring Input timing is as follows: A signal that swings between a Low logic level of V_L and a High logic level of V_H is applied to the Input under test. Some standards also require the application of a bias voltage to the V_{REF} pins of a given bank to properly set the input-switching threshold. The measurement point of the Input signal (V_M) is commonly located halfway between V_L and V_H.

The Output test setup is shown in Figure 8. A termination voltage V_T is applied to the termination resistor R_T, the other end of which is connected to the Output. For each standard, R_T and V_T generally take on the standard values recommended for minimizing signal reflections. If the standard does not ordinarily use terminations (for example, LVCMOS, LVTTL), then R_T is set to 1MΩ to indicate an open connection, and V_T is set to zero. The same measurement point (V_M) that was used at the Input is also used at the Output.



Notes:

1. The names shown in parentheses are used in the IBIS file.

Figure 8: **Output Test Setup**

Table 26: **Test Methods for Timing Measurement at I/Os**

Signal Standard (IOSTANDARD)		Inputs			Outputs[2]		Inputs and Outputs
		V_{REF} (V)	V_L (V)	V_H (V)	R_T (Ω)	V_T (V)	V_M (V)
Single-Ended							
LVTTL		–	0	3.3	1M	0	1.4
LVCMOS33		–	0	3.3	1M	0	1.65
LVCMOS25		–	0	2.5	1M	0	1.25
LVCMOS18		–	0	1.8	1M	0	0.9
LVCMOS15		–	0	1.5	1M	0	0.75
LVCMOS12		–	0	1.2	1M	0	0.6
PCI33_3	Rising	–	Note 3	Note 3	25	0	0.94
	Falling				25	3.3	2.03
PCI66_3	Rising	–	Note 3	Note 3	25	0	0.94
	Falling				25	3.3	2.03
HSTL_I		0.75	V_{REF} – 0.5	V_{REF} + 0.5	50	0.75	V_{REF}
HSTL_III		0.9	V_{REF} – 0.5	V_{REF} + 0.5	50	1.5	V_{REF}
HSTL_I_18		0.9	V_{REF} – 0.5	V_{REF} + 0.5	50	0.9	V_{REF}
HSTL_II_18		0.9	V_{REF} – 0.5	V_{REF} + 0.5	25	0.9	V_{REF}
HSTL_III_18		1.1	V_{REF} – 0.5	V_{REF} + 0.5	50	1.8	V_{REF}
SSTL18_I		0.9	V_{REF} – 0.5	V_{REF} + 0.5	50	0.9	V_{REF}
SSTL18_II		0.9	V_{REF} – 0.5	V_{REF} + 0.5	25	0.9	V_{REF}
SSTL2_I		1.25	V_{REF} – 0.75	V_{REF} + 0.75	50	1.25	V_{REF}
SSTL2_II		1.25	V_{REF} – 0.75	V_{REF} + 0.75	25	1.25	V_{REF}
SSTL3_I		1.5	V_{REF} – 0.75	V_{REF} + 0.75	50	1.5	V_{REF}
SSTL3_II		1.5	V_{REF} – 0.75	V_{REF} + 0.75	25	1.5	V_{REF}

Table 26: **Test Methods for Timing Measurement at I/Os *(Cont'd)***

Signal Standard (IOSTANDARD)	Inputs			Outputs[2]		Inputs and Outputs
	V_{REF} (V)	V_L (V)	V_H (V)	R_T (Ω)	V_T (V)	V_M (V)
Differential						
LVDS_25	–	V_{ICM} – 0.125	V_{ICM} + 0.125	50	1.2	V_{ICM}
LVDS_33	–	V_{ICM} – 0.125	V_{ICM} + 0.125	50	1.2	V_{ICM}
BLVDS_25	–	V_{ICM} – 0.125	V_{ICM} + 0.125	1M	0	V_{ICM}
MINI_LVDS_25	–	V_{ICM} – 0.125	V_{ICM} + 0.125	50	1.2	V_{ICM}
MINI_LVDS_33	–	V_{ICM} – 0.125	V_{ICM} + 0.125	50	1.2	V_{ICM}
LVPECL_25	–	V_{ICM} – 0.3	V_{ICM} + 0.3	N/A	N/A	V_{ICM}
LVPECL_33	–	V_{ICM} – 0.3	V_{ICM} + 0.3	N/A	N/A	V_{ICM}
RSDS_25	–	V_{ICM} – 0.1	V_{ICM} + 0.1	50	1.2	V_{ICM}
RSDS_33	–	V_{ICM} – 0.1	V_{ICM} + 0.1	50	1.2	V_{ICM}
TMDS_33	–	V_{ICM} – 0.1	V_{ICM} + 0.1	50	3.3	V_{ICM}
PPDS_25	–	V_{ICM} – 0.1	V_{ICM} + 0.1	50	0.8	V_{ICM}
PPDS_33	–	V_{ICM} – 0.1	V_{ICM} + 0.1	50	0.8	V_{ICM}
DIFF_HSTL_I_18	–	V_{ICM} – 0.5	V_{ICM} + 0.5	50	0.9	V_{ICM}
DIFF_HSTL_II_18	–	V_{ICM} – 0.5	V_{ICM} + 0.5	50	0.9	V_{ICM}
DIFF_HSTL_III_18	–	V_{ICM} – 0.5	V_{ICM} + 0.5	50	1.8	V_{ICM}
DIFF_HSTL_I	–	V_{ICM} – 0.5	V_{ICM} + 0.5	50	0.9	V_{ICM}
DIFF_HSTL_III	–	V_{ICM} – 0.5	V_{ICM} + 0.5	50	0.9	V_{ICM}
DIFF_SSTL18_I	–	V_{ICM} – 0.5	V_{ICM} + 0.5	50	0.9	V_{ICM}
DIFF_SSTL18_II	–	V_{ICM} – 0.5	V_{ICM} + 0.5	50	0.9	V_{ICM}
DIFF_SSTL2_I	–	V_{ICM} – 0.5	V_{ICM} + 0.5	50	1.25	V_{ICM}
DIFF_SSTL2_II	–	V_{ICM} – 0.5	V_{ICM} + 0.5	50	1.25	V_{ICM}
DIFF_SSTL3_I	–	V_{ICM} – 0.5	V_{ICM} + 0.5	50	1.5	V_{ICM}
DIFF_SSTL3_II	–	V_{ICM} – 0.5	V_{ICM} + 0.5	50	1.5	V_{ICM}

Notes:

1. Descriptions of the relevant symbols are:
   V_{REF} – The reference voltage for setting the input switching threshold
   V_{ICM} – The common mode input voltage
   V_M – Voltage of measurement point on signal transition
   V_L – Low-level test voltage at Input pin
   V_H – High-level test voltage at Input pin
   R_T – Effective termination resistance, which takes on a value of 1 MΩ when no parallel termination is required
   V_T – Termination voltage
2. The load capacitance (C_L) at the Output pin is 0 pF for all signal standards.
3. According to the PCI specification. For information on PCI IP solutions, see www.xilinx.com/pci. The PCIX IOSTANDARD is available and has equivalent characteristics but no PCI-X IP is supported.

The capacitive load (C_L) is connected between the output and GND. *The Output timing for all standards, as published in the speed files and the data sheet, is always based on a C_L value of zero.* High-impedance probes (less than 1 pF) are used for all measurements. Any delay that the test fixture might contribute to test measurements is subtracted from those measurements to produce the final timing numbers as published in the speed files and data sheet.

Using IBIS Models to Simulate Load Conditions in Application

IBIS models permit the most accurate prediction of timing delays for a given application. The parameters found in the IBIS model (V_{REF}, R_{REF}, and V_{MEAS}) correspond directly with the parameters used in Table 26 (V_T, R_T, and V_M). Do not confuse V_{REF} (the termination voltage) from the IBIS model with V_{REF} (the input-switching threshold) from the table. A fourth parameter, C_{REF}, is always zero. The four parameters describe all relevant output test conditions. IBIS models are found in the Xilinx development software as well as at the following link:

www.xilinx.com/support/download/index.htm

Delays for a given application are simulated according to its specific load conditions as follows:

1. Simulate the desired signal standard with the output driver connected to the test setup shown in Figure 8. Use parameter values V_T, R_T, and V_M from Table 26. C_{REF} is zero.
2. Record the time to V_M.
3. Simulate the same signal standard with the output driver connected to the PCB trace with load. Use the appropriate IBIS model (including V_{REF}, R_{REF}, C_{REF}, and V_{MEAS} values) or capacitive value to represent the load.
4. Record the time to V_{MEAS}.
5. Compare the results of steps 2 and 4. Add (or subtract) the increase (or decrease) in delay to (or from) the appropriate Output standard adjustment (Table 25) to yield the worst-case delay of the PCB trace.

Simultaneously Switching Output Guidelines

This section provides guidelines for the recommended maximum allowable number of Simultaneous Switching Outputs (SSOs). These guidelines describe the maximum number of user I/O pins of a given output signal standard that should simultaneously switch in the same direction, while maintaining a safe level of switching noise. Meeting these guidelines for the stated test conditions ensures that the FPGA operates free from the adverse effects of ground and power bounce.

Ground or power bounce occurs when a large number of outputs simultaneously switch in the same direction. The output drive transistors all conduct current to a common voltage rail. Low-to-High transitions conduct to the V_{CCO} rail; High-to-Low transitions conduct to the GND rail. The resulting cumulative current transient induces a voltage difference across the inductance that exists between the die pad and the power supply or ground return. The inductance is associated with bonding wires, the package lead frame, and any other signal routing inside the package. Other variables contribute to SSO noise levels, including stray inductance on the PCB as well as capacitive loading at receivers. Any SSO-induced voltage consequently affects internal switching noise margins and ultimately signal quality.

Table 27 and Table 28 provide the essential SSO guidelines. For each device/package combination, Table 27 provides the number of equivalent V_{CCO}/GND pairs. The equivalent number of pairs is based on characterization and may not match the physical number of pairs. For each output signal standard and drive strength, Table 28 recommends the maximum number of SSOs, switching in the same direction, allowed per V_{CCO}/GND pair within an I/O bank. The guidelines in Table 28 are categorized by package style, slew rate, and output drive current. Furthermore, the number of SSOs is specified by I/O bank. Generally, the left and right I/O banks (Banks 1 and 3) support higher output drive current.

Multiply the appropriate numbers from Table 27 and Table 28 to calculate the maximum number of SSOs allowed within an I/O bank. Exceeding these SSO guidelines might result in increased power or ground bounce, degraded signal integrity, or increased system jitter.

SSO_{MAX}/IO Bank = Table 27 x Table 28

The recommended maximum SSO values assumes that the FPGA is soldered on the printed circuit board and that the board uses sound design practices. The SSO values do not apply for FPGAs mounted in sockets, due to the lead inductance introduced by the socket.

The SSO values assume that the V_{CCAUX} is powered at 3.3V. Setting V_{CCAUX} to 2.5V provides better SSO characteristics.

Table 27: **Equivalent V_{CCO}/GND Pairs per Bank**

Device	Package Style *(including Pb-free)*	
	CS484	FG676
XC3SD1800A	6	9
XC3SD3400A	6	10

Table 28: **Recommended Simultaneously Switching Outputs per V_{CCO}/GND Pair (V_{CCAUX} = 3.3V)**

Signal Standard (IOSTANDARD)			Package Type	
			CS484, FG676	
			Top, Bottom (Banks 0, 2)	Left, Right (Banks 1, 3)
Single-Ended Standards				
LVTTL	Slow	2	60	60
		4	41	41
		6	29	29
		8	22	22
		12	13	13
		16	11	11
		24	9	9
	Fast	2	10	10
		4	6	6
		6	5	5
		8	3	3
		12	3	3
		16	3	3
		24	2	2
	QuietIO	2	80	80
		4	48	48
		6	36	36
		8	27	27
		12	16	16
		16	13	13
		24	12	12

Table 28: **Recommended Simultaneously Switching Outputs per V_{CCO}/GND Pair (V_{CCAUX} = 3.3V) *(Cont'd)***

Signal Standard (IOSTANDARD)			Package Type	
			CS484, FG676	
			Top, Bottom (Banks 0, 2)	Left, Right (Banks 1, 3)
LVCMOS33	Slow	2	76	76
		4	46	46
		6	27	27
		8	20	20
		12	13	13
		16	10	10
		24	–	9
	Fast	2	10	10
		4	8	8
		6	5	5
		8	4	4
		12	4	4
		16	2	2
		24	–	2
	QuietIO	2	76	76
		4	46	46
		6	32	32
		8	26	26
		12	18	18
		16	14	14
		24	–	10

Table 28: **Recommended Simultaneously Switching Outputs per V_{CCO}/GND Pair (V_{CCAUX} = 3.3V) *(Cont'd)***

Signal Standard (IOSTANDARD)			Package Type	
			CS484, FG676	
			Top, Bottom (Banks 0, 2)	Left, Right (Banks 1, 3)
LVCMOS25	Slow	2	76	76
		4	46	46
		6	33	33
		8	24	24
		12	18	18
		16	–	11
		24	–	7
	Fast	2	18	18
		4	14	14
		6	6	6
		8	6	6
		12	3	3
		16	–	3
		24	–	2
	QuietIO	2	76	76
		4	60	60
		6	48	48
		8	36	36
		12	36	36
		16	–	36
		24	–	8

Table 28: **Recommended Simultaneously Switching Outputs per V_{CCO}/GND Pair (V_{CCAUX} = 3.3V) *(Cont'd)***

Signal Standard (IOSTANDARD)			Package Type	
			CS484, FG676	
			Top, Bottom (Banks 0, 2)	Left, Right (Banks 1, 3)
LVCMOS18	Slow	2	64	64
		4	34	34
		6	22	22
		8	18	18
		12	–	13
		16	–	10
	Fast	2	18	18
		4	9	9
		6	7	7
		8	4	4
		12	–	4
		16	–	3
	QuietIO	2	64	64
		4	64	64
		6	48	48
		8	36	36
		12	–	36
		16	–	24
LVCMOS15	Slow	2	55	55
		4	31	31
		6	18	18
		8	–	15
		12	–	10
	Fast	2	25	25
		4	10	10
		6	6	6
		8	–	4
		12	–	3
	QuietIO	2	70	70
		4	40	40
		6	31	31
		8	–	31
		12	–	20

Table 28: **Recommended Simultaneously Switching Outputs per V_{CCO}/GND Pair (V_{CCAUX} = 3.3V) *(Cont'd)***

Signal Standard (IOSTANDARD)			Package Type	
			CS484, FG676	
			Top, Bottom (Banks 0, 2)	Left, Right (Banks 1, 3)
LVCMOS12	Slow	2	40	40
		4	–	25
		6	–	18
	Fast	2	31	31
		4	–	13
		6	–	9
	QuietIO	2	55	55
		4	–	36
		6	–	36
PCI33_3			16	16
PCI66_3			–	13
HSTL_I			–	20
HSTL_III			–	8
HSTL_I_18			17	17
HSTL_II_18			–	5
HSTL_III_18			10	8
SSTL18_I			7	15
SSTL18_II			–	9
SSTL2_I			18	18
SSTL2_II			–	9
SSTL3_I			8	10
SSTL3_II			6	7

Table 28: **Recommended Simultaneously Switching Outputs per V_{CCO}/GND Pair (V_{CCAUX} = 3.3V) *(Cont'd)***

Signal Standard (IOSTANDARD)	Package Type	
	CS484, FG676	
	Top, Bottom (Banks 0, 2)	Left, Right (Banks 1, 3)
Differential Standards (Number of I/O Pairs or Channels)		
LVDS_25	22	–
LVDS_33	27	–
BLVDS_25	4	4
MINI_LVDS_25	22	–
MINI_LVDS_33	27	–
LVPECL_25	Inputs Only	
LVPECL_33	Inputs Only	
RSDS_25	22	–
RSDS_33	27	–
TMDS_33	27	–
PPDS_25	22	–
PPDS_33	27	–
DIFF_HSTL_I_18	8	8
DIFF_HSTL_II_18	–	2
DIFF_HSTL_III_18	5	4
DIFF_HSTL_I	–	10
DIFF_HSTL_III	–	4
DIFF_SSTL18_I	3	7
DIFF_SSTL18_II	–	4
DIFF_SSTL2_I	9	9
DIFF_SSTL2_II	–	4
DIFF_SSTL3_I	4	5
DIFF_SSTL3_II	3	3

Notes:

1. Not all I/O standards are supported on all I/O banks. The left and right banks (I/O banks 1 and 3) support higher output drive current than the top and bottom banks (I/O banks 0 and 2). Similarly, true differential output standards, such as LVDS, RSDS, PPDS, miniLVDS, and TMDS, are only supported in top or bottom banks (I/O banks 0 and 2). Refer to UG331: *Spartan-3 Generation FPGA User Guide* for additional information.
2. The numbers in this table are recommendations that assume sound board lay out practice. This table assumes the following parasitic factors: combined PCB trace and land inductance per V_{CCO} and GND pin of 1.0 nH, receiver capacitive load of 15 pF. Test limits are the V_{IL}/V_{IH} voltage limits for the respective I/O standard.
3. If more than one signal standard is assigned to the I/Os of a given bank, refer to XAPP689: *Managing Ground Bounce in Large FPGAs* for information on how to perform weighted average SSO calculations.

Configurable Logic Block (CLB) Timing

Table 29: **CLB (SLICEM) Timing**

Symbol	Description	Speed Grade				Units
		-5		-4		
		Min	Max	Min	Max	
Clock-to-Output Times						
T_{CKO}	When reading from the FFX (FFY) Flip-Flop, the time from the active transition at the CLK input to data appearing at the XQ (YQ) output	–	0.60	–	0.68	ns
Setup Times						
T_{AS}	Time from the setup of data at the F or G input to the active transition at the CLK input of the CLB	0.18	–	0.36	–	ns
T_{DICK}	Time from the setup of data at the BX or BY input to the active transition at the CLK input of the CLB	1.58	–	1.88	–	ns
Hold Times						
T_{AH}	Time from the active transition at the CLK input to the point where data is last held at the F or G input	0.00	–	0.00	–	ns
T_{CKDI}	Time from the active transition at the CLK input to the point where data is last held at the BX or BY input	0.00	–	0.00	–	ns
Clock Timing						
T_{CH}	The High pulse width of the CLB's CLK signal	0.63	–	0.75	–	ns
T_{CL}	The Low pulse width of the CLK signal	0.63	–	0.75	–	ns
F_{TOG}	Toggle frequency (for export control)	0	770	0	667	MHz
Propagation Times						
T_{ILO}	The time it takes for data to travel from the CLB's F (G) input to the X (Y) output	–	0.62	–	0.71	ns
Set/Reset Pulse Width						
T_{RPW_CLB}	The minimum allowable pulse width, High or Low, to the CLB's SR input	1.33	–	1.61	–	ns

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 7.

Table 30: **CLB Distributed RAM Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-5		-4		
		Min	Max	Min	Max	
Clock-to-Output Times						
T_{SHCKO}	Time from the active edge at the CLK input to data appearing on the distributed RAM output	–	1.44	–	1.72	ns
Setup Times						
T_{DS}	Setup time of data at the BX or BY input before the active transition at the CLK input of the distributed RAM	–0.07	–	–0.02	–	ns
T_{AS}	Setup time of the F/G address inputs before the active transition at the CLK input of the distributed RAM	0.18	–	0.36	–	ns
T_{WS}	Setup time of the write enable input before the active transition at the CLK input of the distributed RAM	0.30	–	0.59	–	ns
Hold Times						
T_{DH}	Hold time of the BX and BY data inputs after the active transition at the CLK input of the distributed RAM	0.13	–	0.13	–	ns
T_{AH}, T_{WH}	Hold time of the F/G address inputs or the write enable input after the active transition at the CLK input of the distributed RAM	0.01	–	0.01	–	ns
Clock Pulse Width						
T_{WPH}, T_{WPL}	Minimum High or Low pulse width at CLK input	0.88	–	1.01	–	ns

Table 31: **CLB Shift Register Switching Characteristics**

Symbol	Description	Speed Grade				Units
		-5		-4		
		Min	Max	Min	Max	
Clock-to-Output Times						
T_{REG}	Time from the active edge at the CLK input to data appearing on the shift register output	–	4.11	–	4.82	ns
Setup Times						
T_{SRLDS}	Setup time of data at the BX or BY input before the active transition at the CLK input of the shift register	0.13	–	0.18	–	ns
Hold Times						
T_{SRLDH}	Hold time of the BX or BY data input after the active transition at the CLK input of the shift register	0.16	–	0.16	–	ns
Clock Pulse Width						
T_{WPH}, T_{WPL}	Minimum High or Low pulse width at CLK input	0.90	–	1.01	–	ns

Clock Buffer/Multiplexer Switching Characteristics

Table 32: **Clock Distribution Switching Characteristics**

Symbol	Description	Minimum	Maximum		Units
			Speed Grade		
			-5	-4	
T_{GIO}	Global clock buffer (BUFG, BUFGMUX, BUFGCE) I input to O-output delay	–	0.22	0.23	ns
T_{GSI}	Global clock multiplexer (BUFGMUX) select S-input setup to I0 and I1 inputs. Same as BUFGCE enable CE-input	–	0.56	0.63	ns
F_{BUFG}	Frequency of signals distributed on global buffers (all sides)	0	350	334	MHz

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 7.

Block RAM Timing

Table 33: **Block RAM Timing**

Symbol	Description	Speed Grade				Units
		-5		-4		
		Min	Max	Min	Max	
Clock-to-Output Times						
$T_{RCKO\_DOA\_NC}$	When reading from block RAM, the delay from the active transition at the CLK input to data appearing at the DOUT output	–	2.38	–	2.80	ns
T_{RCKO_DOA}	Clock CLK to DOUT output (with output register)	–	1.24	–	1.45	ns
Setup Times						
T_{RCCK_ADDR}	Setup time for the ADDR inputs before the active transition at the CLK input of the block RAM	0.40	–	0.46	–	ns
T_{RDCK_DIB}	Setup time for data at the DIN inputs before the active transition at the CLK input of the block RAM	0.29	–	0.33	–	ns
T_{RCCK_ENB}	Setup time for the EN input before the active transition at the CLK input of the block RAM	0.51	–	0.60	–	ns
T_{RCCK_WEB}	Setup time for the WE input before the active transition at the CLK input of the block RAM	0.64	–	0.75	–	ns
T_{RCCK_REGCE}	Setup time for the CE input before the active transition at the CLK input of the block RAM	0.34	–	0.40	–	ns
T_{RCCK_RST}	Setup time for the RST input before the active transition at the CLK input of the block RAM	0.22	–	0.25	–	ns
Hold Times						
T_{RCKC_ADDR}	Hold time on the ADDR inputs after the active transition at the CLK input	0.09	–	0.10	–	ns
T_{RCKC_DIB}	Hold time on the DIN inputs after the active transition at the CLK input	0.09	–	0.10	–	ns
T_{RCKC_ENB}	Hold time on the EN input after the active transition at the CLK input	0.09	–	0.10	–	ns
T_{RCKC_WEB}	Hold time on the WE input after the active transition at the CLK input	0.09	–	0.10	–	ns
T_{RCKC_REGCE}	Hold time on the CE input after the active transition at the CLK input	0.09	–	0.10	–	ns
T_{RCKC_RST}	Hold time on the RST input after the active transition at the CLK input	0.09	–	0.10	–	ns
Clock Timing						
T_{BPWH}	High pulse width of the CLK signal	1.56	–	1.79	–	ns
T_{BPWL}	Low pulse width of the CLK signal	1.56	–	1.79	–	ns
Clock Frequency						
F_{BRAM}	Block RAM clock frequency	0	320	0	280	MHz

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 7.

DSP48A Timing

To reference the DSP48A block diagram, see UG431: *XtremeDSP DSP48A for Spartan-3A DSP FPGA User Guide*.

Table 34: **Setup Times for the DSP48A**

Symbol	Description	Pre-adder	Multiplier	Post-adder	Speed Grade		Units
					-5	-4	
					Min	Min	
Setup Times of Data/Control Pins to the Input Register Clock							
T_{DSPDCK_AA}	A input to A register CLK	–	–	–	0.04	0.04	ns
T_{DSPDCK_DB}	D input to B register CLK	Yes	–	–	1.64	1.88	ns
T_{DSPDCK_CC}	C input to C register CLK	–	–	–	0.05	0.05	ns
T_{DSPDCK_DD}	D input to D register CLK	–	–	–	0.04	0.04	ns
T_{DSPDCK_OPB}	OPMODE input to B register CLK	Yes	–	–	0.37	0.42	ns
T_{DSPDCK_OPOP}	OPMODE input to OPMODE register CLK	–	–	–	0.06	0.06	ns
Setup Times of Data Pins to the Pipeline Register Clock							
T_{DSPDCK_AM}	A input to M register CLK	–	Yes	–	3.30	3.79	ns
T_{DSPDCK_BM}	B input to M register CLK	Yes	Yes	–	4.33	4.97	ns
		No	Yes	–	3.30	3.79	ns
T_{DSPDCK_DM}	D input to M register CLK	Yes	Yes	–	4.41	5.06	ns
T_{DSPDCK_OPM}	OPMODE to M register CLK	Yes	Yes	–	4.72	5.42	ns
Setup Times of Data/Control Pins to the Output Register Clock							
T_{DSPDCK_AP}	A input to P register CLK	–	Yes	Yes	4.78	5.49	ns
T_{DSPDCK_BP}	B input to P register CLK	Yes	Yes	Yes	5.87	6.74	ns
		No	Yes	Yes	4.77	5.48	ns
T_{DSPDCK_DP}	D input to P register CLK	Yes	Yes	Yes	5.95	6.83	ns
T_{DSPDCK_CP}	C input to P register CLK	–	–	Yes	1.90	2.18	ns
T_{DSPDCK_OPP}	OPMODE input to P register CLK	Yes	Yes	Yes	6.25	7.18	ns

Notes:

1. "Yes" means that the component is in the path. "No" means that the component is being bypassed. "–" means that no path exists, so it is not applicable.
2. The numbers in this table are based on the operating conditions set forth in Table 7.

Table 35: **Clock to Out, Propagation Delays, and Maximum Frequency for the DSP48A**

Symbol	Description	Pre-adder	Multiplier	Post-adder	Speed Grade		Units
					-5	-4	
					Max	Max	
Clock to Out from Output Register Clock to Output Pin							
T_{DSPCKO_PP}	CLK (PREG) to P output	–	–	–	1.26	1.44	ns
Clock to Out from Pipeline Register Clock to Output Pins							
T_{DSPCKO_PM}	CLK (MREG) to P output	–	Yes	Yes	3.16	3.63	ns
		–	Yes	No	1.94	2.23	ns
Clock to Out from Input Register Clock to Output Pins							
T_{DSPCKO_PA}	CLK (AREG) to P output	–	Yes	Yes	6.33	7.27	ns
T_{DSPCKO_PB}	CLK (BREG) to P output	Yes	Yes	Yes	7.45	8.56	ns
T_{DSPCKO_PC}	CLK (CREG) to P output	–	–	Yes	3.37	3.87	ns
T_{DSPCKO_PD}	CLK (DREG) to P output	Yes	Yes	Yes	7.33	8.42	ns
Combinatorial Delays from Input Pins to Output Pins							
T_{DSPDO_AP} T_{DSPDO_BP}	A or B input to P output	–	No	Yes	2.78	3.19	ns
		–	Yes	No	4.60	5.28	ns
		–	Yes	Yes	5.65	6.49	ns
T_{DSPDO_BP}	B input to P output	Yes	No	No	3.49	4.01	ns
		Yes	Yes	No	5.79	6.65	ns
		Yes	Yes	Yes	6.74	7.74	ns
T_{DSPDO_CP}	C input to P output	–	–	Yes	2.76	3.17	ns
T_{DSPDO_DP}	D input to P output	Yes	Yes	Yes	6.81	7.82	ns
T_{DSPDO_OPP}	OPMODE input to P output	Yes	Yes	Yes	7.12	8.18	ns
Maximum Frequency							
F_{MAX}	All registers used	Yes	Yes	Yes	287	250	MHz

Notes:

1. To reference the DSP48A block diagram, see UG431: *XtremeDSP DSP48A for Spartan-3A DSP FPGA User Guide*.
2. "Yes" means that the component is in the path. "No" means that the component is being bypassed. "–" means that no path exists, so it is not applicable.
3. The numbers in this table are based on the operating conditions set forth in Table 7.

Digital Clock Manager (DCM) Timing

For specification purposes, the DCM consists of three key components: the Delay-Locked Loop (DLL), the Digital Frequency Synthesizer (DFS), and the Phase Shifter (PS).

Aspects of DLL operation play a role in all DCM applications. All such applications inevitably use the CLKIN and the CLKFB inputs connected to either the CLK0 or the CLK2X feedback, respectively. Thus, specifications in the DLL tables (Table 36 and Table 37) apply to any application that only employs the DLL component. When the DFS and/or the PS components are used together with the DLL, then the specifications listed in the DFS and PS tables (Table 38 through Table 41) supersede any corresponding ones in the DLL tables. DLL specifications that do not change with the addition of DFS or PS functions are presented in Table 36 and Table 37.

Period jitter and cycle-cycle jitter are two of many different ways of specifying clock jitter. Both specifications describe statistical variation from a mean value.

Period jitter is the worst-case deviation from the ideal clock period over a collection of millions of samples. In a histogram of period jitter, the mean value is the clock period.

Cycle-cycle jitter is the worst-case difference in clock period between adjacent clock cycles in the collection of clock periods sampled. In a histogram of cycle-cycle jitter, the mean value is zero.

Spread Spectrum

DCMs accept typical spread spectrum clocks as long as they meet the input requirements. The DLL will track the frequency changes created by the spread spectrum clock to drive the global clocks to the FPGA logic. See XAPP469: *Spread-Spectrum Clocking Reception for Displays* for details.

Delay-Locked Loop (DLL)

Table 36: **Recommended Operating Conditions for the DLL**

Symbol		Description		Speed Grade				Units
				-5		-4		
				Min	Max	Min	Max	
Input Frequency Ranges								
F_{CLKIN}	CLKIN_FREQ_DLL	Frequency of the CLKIN clock input		5(2)	280(3)	5(2)	250(3)	MHz
Input Pulse Requirements								
CLKIN_PULSE		CLKIN pulse width as a percentage of the CLKIN period	$F_{CLKIN} \le 150$ MHz	40%	60%	40%	60%	–
			$F_{CLKIN} > 150$ MHz	45%	55%	45%	55%	–
Input Clock Jitter Tolerance and Delay Path Variation(4)								
CLKIN_CYC_JITT_DLL_LF		Cycle-to-cycle jitter at the CLKIN input	$F_{CLKIN} \le 150$ MHz	–	±300	–	±300	ps
CLKIN_CYC_JITT_DLL_HF			$F_{CLKIN} > 150$ MHz	–	±150	–	±150	ps
CLKIN_PER_JITT_DLL		Period jitter at the CLKIN input		–	±1	–	±1	ns
CLKFB_DELAY_VAR_EXT		Allowable variation of off-chip feedback delay from the DCM output to the CLKFB input		–	±1	–	±1	ns

Notes:

1. DLL specifications apply when any of the DLL outputs (CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, or CLKDV) are in use.
2. The DFS, when operating independently of the DLL, supports lower FCLKIN frequencies. See Table 38.
3. To support double the maximum effective FCLKIN limit, set the CLKIN_DIVIDE_BY_2 attribute to TRUE. This attribute divides the incoming clock frequency by two as it enters the DCM. The CLK2X output reproduces the clock frequency provided on the CLKIN input.
4. CLKIN input jitter beyond these limits might cause the DCM to lose lock.
5. The DCM specifications are guaranteed when both adjacent DCMs are locked.

Table 37: **Switching Characteristics for the DLL**

Symbol	Description		Device	Speed Grade				Units
				-5		-4		
				Min	Max	Min	Max	
Output Frequency Ranges								
CLKOUT_FREQ_CLK0	Frequency for the CLK0 and CLK180 outputs		All	5	280	5	250	MHz
CLKOUT_FREQ_CLK90	Frequency for the CLK90 and CLK270 outputs			5	200	5	200	MHz
CLKOUT_FREQ_2X	Frequency for the CLK2X and CLK2X180 outputs			10	334	10	334	MHz
CLKOUT_FREQ_DV	Frequency for the CLKDV output			0.3125	186	0.3125	166	MHz
Output Clock Jitter (2)(3)(4)								
CLKOUT_PER_JITT_0	Period jitter at the CLK0 output		All	–	±100	–	±100	ps
CLKOUT_PER_JITT_90	Period jitter at the CLK90 output			–	±150	–	±150	ps
CLKOUT_PER_JITT_180	Period jitter at the CLK180 output			–	±150	–	±150	ps
CLKOUT_PER_JITT_270	Period jitter at the CLK270 output			–	±150	–	±150	ps
CLKOUT_PER_JITT_2X	Period jitter at the CLK2X and CLK2X180 outputs			–	±[0.5% of CLKIN period + 100]	–	±[0.5% of CLKIN period + 100]	ps
CLKOUT_PER_JITT_DV1	Period jitter at the CLKDV output when performing integer division			–	±150	–	±150	ps
CLKOUT_PER_JITT_DV2	Period jitter at the CLKDV output when performing non-integer division			–	±[0.5% of CLKIN period + 100]	–	±[0.5% of CLKIN period + 100]	ps
Duty Cycle (4)								
CLKOUT_DUTY_CYCLE_DLL	Duty cycle variation for the CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV outputs, including the BUFGMUX and clock tree duty-cycle distortion		All	–	±[1% of CLKIN period + 350]	–	±[1% of CLKIN period + 350]	ps
Phase Alignment (4)								
CLKIN_CLKFB_PHASE	Phase offset between the CLKIN and CLKFB inputs		All	–	±150	–	±150	ps
CLKOUT_PHASE_DLL	Phase offset between DLL outputs	CLK0 to CLK2X (not CLK2X180)		–	±[1% of CLKIN period + 100]	–	±[1% of CLKIN period + 100]	ps
		All others		–	±[1% of CLKIN period + 150]	–	±[1% of CLKIN period + 150]	ps
Lock Time								
LOCK_DLL(3)	When using the DLL alone: The time from deassertion at the DCM's Reset input to the rising transition at its LOCKED output. When the DCM is locked, the CLKIN and CLKFB signals are in phase	5 MHz < FCLKIN < 15 MHz	All	–	5	–	5	ms
		FCLKIN > 15 MHz		–	600	–	600	µs

Table 37: **Switching Characteristics for the DLL *(Cont'd)***

Symbol	Description	Device	Speed Grade				Units
			-5		-4		
			Min	Max	Min	Max	
Delay Lines							
DCM_DELAY_STEP(5)	Finest delay resolution, averaged over all steps	All	15	35	15	35	ps

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 7 and Table 36.
2. Indicates the maximum amount of output jitter that the DCM adds to the jitter on the CLKIN input.
3. For optimal jitter tolerance and faster lock time, use the CLKIN_PERIOD attribute.
4. Some jitter and duty-cycle specifications include 1% of input clock period or 0.01 UI. For example, the data sheet specifies a maximum jitter of ±[1% of CLKIN period + 150]. Assume the CLKIN frequency is 100 MHz. The equivalent CLKIN period is 10 ns and 1% of 10 ns is 0.1 ns or 100 ps. According to the data sheet, the maximum jitter is ±[100 ps + 150 ps] = ±250 ps, averaged over all steps.
5. The typical delay step size is 23 ps.

Digital Frequency Synthesizer (DFS)

Table 38: **Recommended Operating Conditions for the DFS**

Symbol		Description		Speed Grade				Units
				-5		-4		
				Min	Max	Min	Max	
Input Frequency Ranges(2)								
F_{CLKIN}	CLKIN_FREQ_FX	Frequency for the CLKIN input		0.2	333(5)	0.2	333(5)	MHz
Input Clock Jitter Tolerance(3)								
CLKIN_CYC_JITT_FX_LF		Cycle-to-cycle jitter at the CLKIN input, based on CLKFX output frequency	$F_{CLKFX} \leq 150$ MHz	–	±300	–	±300	ps
CLKIN_CYC_JITT_FX_HF			$F_{CLKFX} > 150$ MHz	–	±150	–	±150	ps
CLKIN_PER_JITT_FX		Period jitter at the CLKIN input		–	±1	–	±1	ns

Notes:

1. DFS specifications apply when either of the DFS outputs (CLKFX or CLKFX180) are used.
2. If both DFS and DLL outputs are used on the same DCM, follow the more restrictive CLKIN_FREQ_DLL specifications in Table 36.
3. CLKIN input jitter beyond these limits may cause the DCM to lose lock.
4. The DCM specifications are guaranteed when both adjacent DCMs are locked.
5. To support double the maximum effective F_{CLKIN} limit, set the CLKIN_DIVIDE_BY_2 attribute to TRUE. This attribute divides the incoming clock frequency by two as it enters the DCM.

Table 39: **Switching Characteristics for the DFS**

Symbol	Description		Device	Speed Grade				Units
				-5		-4		
				Min	Max	Min	Max	
Output Frequency Ranges								
CLKOUT_FREQ_FX[2]	Frequency for the CLKFX and CLKFX180 outputs		All	5	350	5	311	MHz
Output Clock Jitter [3][4]								
CLKOUT_PER_JITT_FX	Period jitter at the CLKFX and CLKFX180 outputs.	CLKIN ≤ 20 MHz	All	Typ	Max	Typ	Max	
				Use the Spartan-3A Jitter Calculator: www.xilinx.com/support/documentation/data_sheets/s3a_jitter_calc.zip				ps
		CLKIN > 20 MHz		±[1% of CLKFX period + 100]	±[1% of CLKFX period + 200]	±[1% of CLKFX period + 100]	±[1% of CLKFX period + 200]	ps
Duty Cycle[5][6]								
CLKOUT_DUTY_CYCLE_FX	Duty cycle precision for the CLKFX and CLKFX180 outputs, including the BUFGMUX and clock tree duty-cycle distortion		All	–	±[1% of CLKFX period + 350]	–	±[1% of CLKFX period + 350]	ps
Phase Alignment[6]								
CLKOUT_PHASE_FX	Phase offset between the DFS CLKFX output and the DLL CLK0 output when both the DFS and DLL are used		All	–	±200	–	±200	ps
CLKOUT_PHASE_FX180	Phase offset between the DFS CLKFX180 output and the DLL CLK0 output when both the DFS and DLL are used		All	–	±[1% of CLKFX period + 200]	–	±[1% of CLKFX period + 200]	ps
Lock Time								
LOCK_FX[2][3]	The time from deassertion at the DCM's Reset input to the rising transition at its LOCKED output. The DFS asserts LOCKED when the CLKFX and CLKFX180 signals are valid. If using both the DLL and the DFS, use the longer locking time.	5 MHz ≤ F_{CLKIN} ≤ 15 MHz	All	–	5	–	5	ms
		F_{CLKIN} > 15 MHz		–	450	–	450	µs

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 7 and Table 38.
2. DFS performance requires the additional logic automatically added by ISE 9.1i and later software revisions.
3. For optimal jitter tolerance and faster lock time, use the CLKIN_PERIOD attribute.
4. Maximum output jitter is characterized within a reasonable noise environment (150 ps input period jitter, 40 SSOs and 25% CLB switching) on an FPGA. Output jitter strongly depends on the environment, including the number of SSOs, the output drive strength, CLB utilization, CLB switching activities, switching frequency, power supply and PCB design. The actual maximum output jitter depends on the system application.
5. The CLKFX and CLKFX180 outputs always have an approximate 50% duty cycle.
6. Some duty-cycle and alignment specifications include a percentage of the CLKFX output period. For example, the data sheet specifies a maximum CLKFX jitter of "±[1% of CLKFX period + 200]". Assume the CLKFX output frequency is 100 MHz. The equivalent CLKFX period is 10 ns and 1% of 10 ns is 0.1 ns or 100 ps. According to the data sheet, the maximum jitter is ±[100 ps + 200 ps] = ±300 ps.

Phase Shifter (PS)

Table 40: **Recommended Operating Conditions for the PS in Variable Phase Mode**

Symbol	Description	Speed Grade				Units
		-5		-4		
		Min	Max	Min	Max	
Operating Frequency Ranges						
PSCLK_FREQ (FPSCLK)	Frequency for the PSCLK input	1	167	1	167	MHz
Input Pulse Requirements						
PSCLK_PULSE	PSCLK pulse width as a percentage of the PSCLK period	40%	60%	40%	60%	–

Table 41: **Switching Characteristics for the PS in Variable Phase Mode**

Symbol	Description		Phase Shift Amount	Units
Phase Shifting Range				
MAX_STEPS(2,3)	Maximum allowed number of DCM_DELAY_STEP steps for a given CLKIN clock period, where T = CLKIN clock period in ns. If using CLKIN_DIVIDE_BY_2 = TRUE, double the effective clock period.	CLKIN < 60 MHz	±[INTEGER(10 • (T_{CLKIN} – 3 ns))]	steps
		CLKIN ≥ 60 MHz	±[INTEGER(15 • (T_{CLKIN} – 3 ns))]	
FINE_SHIFT_RANGE_MIN	Minimum guaranteed delay for variable phase shifting		±[MAX_STEPS • DCM_DELAY_STEP_MIN]	ns
FINE_SHIFT_RANGE_MAX	Maximum guaranteed delay for variable phase shifting		±[MAX_STEPS • DCM_DELAY_STEP_MAX]	ns

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 7 and Table 40.
2. The maximum variable phase shift range, MAX_STEPS, is only valid when the DCM is has no initial fixed phase shifting, that is, the PHASE_SHIFT attribute is set to 0.
3. The DCM_DELAY_STEP values are provided at the bottom of Table 37.

Miscellaneous DCM Timing

Table 42: **Miscellaneous DCM Timing**

Symbol	Description	Min	Max	Units
DCM_RST_PW_MIN	Minimum duration of a RST pulse width	3	–	CLKIN cycles

DNA Port Timing

Table 43: **DNA_PORT Interface Timing**

Symbol	Description	Min	Max	Units
T_{DNASSU}	Setup time on SHIFT before the rising edge of CLK	1.0	–	ns
T_{DNASH}	Hold time on SHIFT after the rising edge of CLK	0.5	–	ns
T_{DNADSU}	Setup time on DIN before the rising edge of CLK	1.0	–	ns
T_{DNADH}	Hold time on DIN after the rising edge of CLK	0.5	–	ns
T_{DNARSU}	Setup time on READ before the rising edge of CLK	5.0	10,000	ns
T_{DNARH}	Hold time on READ after the rising edge of CLK	0.0	–	ns
$T_{DNADCKO}$	Clock-to-output delay on DOUT after rising edge of CLK	0.5	1.5	ns
$T_{DNACLKF}$	CLK frequency	0.0	100	MHz
$T_{DNACLKH}$	CLK High time	1.0	∞	ns
$T_{DNACLKL}$	CLK Low time	1.0	∞	ns

Notes:

1. The minimum READ pulse width is 5 ns, and the maximum READ pulse width is 10 µs.

Suspend Mode Timing

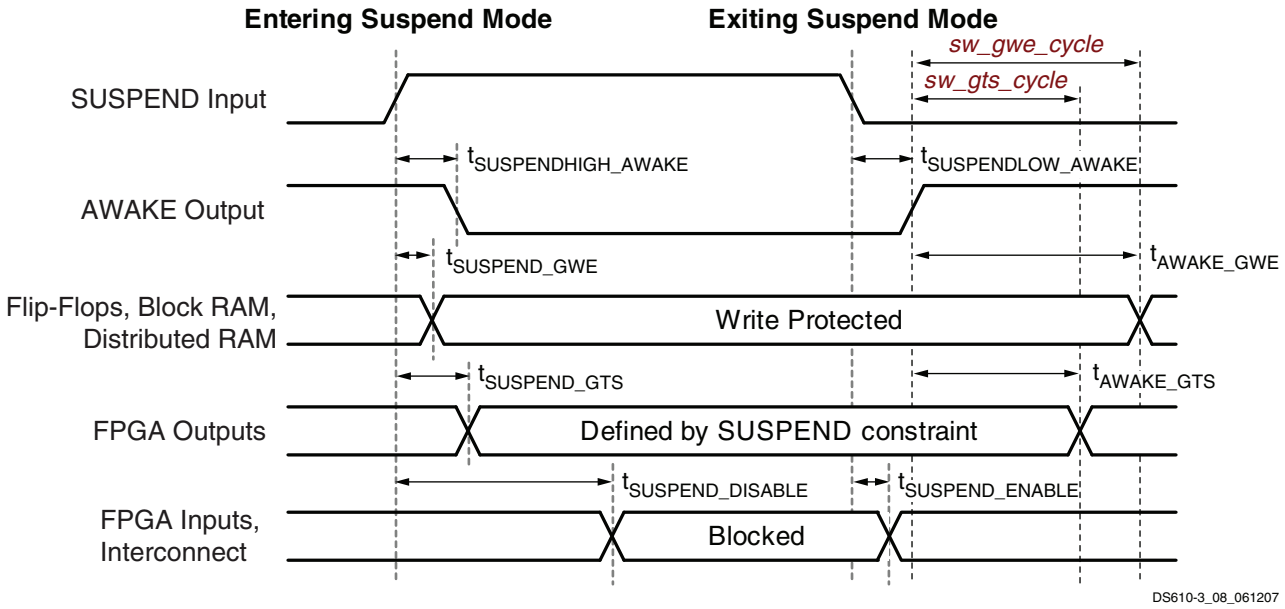


Figure 9: **Suspend Mode Timing**

Table 44: **Suspend Mode Timing Parameters**

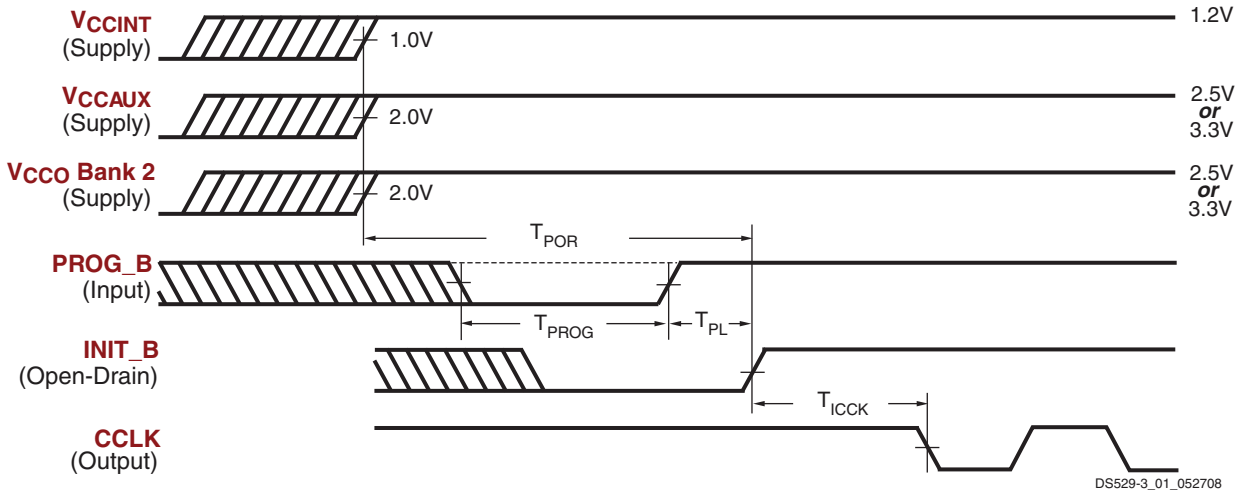
Symbol	Description	Min	Typ	Max	Units
Entering Suspend Mode					
$T_{SUSPENDHIGH\_AWAKE}$	Rising edge of SUSPEND pin to falling edge of AWAKE pin without glitch filter (***suspend_filter:No***)	–	7	–	ns
$T_{SUSPENDFILTER}$	Adjustment to SUSPEND pin rising edge parameters when glitch filter enabled (***suspend_filter:Yes***)	+160	+300	+600	ns
$T_{SUSPEND\_GTS}$	Rising edge of SUSPEND pin until FPGA output pins drive their defined SUSPEND constraint behavior	–	10	–	ns
$T_{SUSPEND\_GWE}$	Rising edge of SUSPEND pin to write-protect lock on all writable clocked elements	–	<5	–	ns
$T_{SUSPEND\_DISABLE}$	Rising edge of the SUSPEND pin to FPGA input pins and interconnect disabled	–	340	–	ns
Exiting Suspend Mode					
$T_{SUSPENDLOW\_AWAKE}$	Falling edge of the SUSPEND pin to rising edge of the AWAKE pin. Does not include DCM lock time.	–	4 to 108	–	µs
$T_{SUSPEND\_ENABLE}$	Falling edge of the SUSPEND pin to FPGA input pins and interconnect re-enabled	–	3.7 to 109	–	µs
T_{AWAKE_GWE1}	Rising edge of the AWAKE pin until write-protect lock released on all writable clocked elements, using ***sw_clk:InternalClock*** and ***sw_gwe_cycle:1***.	–	67	–	ns
T_{AWAKE_GWE512}	Rising edge of the AWAKE pin until write-protect lock released on all writable clocked elements, using ***sw_clk:InternalClock*** and ***sw_gwe_cycle:512***.	–	14	–	µs
T_{AWAKE_GTS1}	Rising edge of the AWAKE pin until outputs return to the behavior described in the FPGA application, using ***sw_clk:InternalClock*** and ***sw_gts_cycle:1***.	–	57	–	ns
T_{AWAKE_GTS512}	Rising edge of the AWAKE pin until outputs return to the behavior described in the FPGA application, using ***sw_clk:InternalClock*** and ***sw_gts_cycle:512***.	–	14	–	µs

Notes:

1. These parameters based on characterization.
2. For information on using the Spartan-3A DSP Suspend feature, see XAPP480: *Using Suspend Mode in Spartan-3 Generation FPGAs*.

Configuration and JTAG Timing

General Configuration Power-On/Reconfigure Timing



Notes:

1. The V_{CCINT}, V_{CCAUX}, and V_{CCO} supplies can be applied in any order.
2. The Low-going pulse on PROG_B is optional after power-on but necessary for reconfiguration without a power cycle.
3. The rising edge of INIT_B samples the voltage levels applied to the mode pins (M0 - M2).

Figure 10: **Waveforms for Power-On and the Beginning of Configuration**

Table 45: **Power-On Timing and the Beginning of Configuration**

Symbol	Description	Device	All Speed Grades		Units
			Min	Max	
T_{POR}(2)	The time from the application of V_{CCINT}, V_{CCAUX}, and V_{CCO} Bank 2 supply voltage ramps (whichever occurs last) to the rising transition of the INIT_B pin	All	–	18	ms
T_{PROG}	The width of the low-going pulse on the PROG_B pin	All	0.5	–	µs
T_{PL}(2)	The time from the rising edge of the PROG_B pin to the rising transition on the INIT_B pin	All	–	2	ms
T_{INIT}	Minimum Low pulse width on INIT_B output	All	300	–	ns
T_{ICCK}(3)	The time from the rising edge of the INIT_B pin to the generation of the configuration clock signal at the CCLK output pin	All	0.5	4	µs

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 7. This means power must be applied to all V_{CCINT}, V_{CCO}, and V_{CCAUX} lines.
2. Power-on reset and the clearing of configuration memory occurs during this period.
3. This specification applies only to the Master Serial, SPI, and BPI modes.
4. For details on configuration, see UG332 *Spartan-3 Generation Configuration User Guide*.

Configuration Clock (CCLK) Characteristics

Table 46: **Master Mode CCLK Output Period by *ConfigRate* Option Setting**

Symbol	Description	*ConfigRate* Setting[1]	Temperature Range	Minimum	Maximum	Units
T_{CCLK1}	CCLK clock period by ***ConfigRate*** setting	1 *(power-on value)*	Commercial	1,254	2,500	ns
			Industrial	1,180		ns
T_{CCLK3}		3	Commercial	413	833	ns
			Industrial	390		ns
T_{CCLK6}		6 (default)	Commercial	207	417	ns
			Industrial	195		ns
T_{CCLK7}		7	Commercial	178	357	ns
			Industrial	168		ns
T_{CCLK8}		8	Commercial	156	313	ns
			Industrial	147		ns
T_{CCLK10}		10	Commercial	123	250	ns
			Industrial	116		ns
T_{CCLK12}		12	Commercial	103	208	ns
			Industrial	97		ns
T_{CCLK13}		13	Commercial	93	192	ns
			Industrial	88		ns
T_{CCLK17}		17	Commercial	72	147	ns
			Industrial	68		ns
T_{CCLK22}		22	Commercial	54	114	ns
			Industrial	51		ns
T_{CCLK25}		25	Commercial	47	100	ns
			Industrial	45		ns
T_{CCLK27}		27	Commercial	44	93	ns
			Industrial	42		ns
T_{CCLK33}		33	Commercial	36	76	ns
			Industrial	34		ns
T_{CCLK44}		44	Commercial	26	57	ns
			Industrial	25		ns
T_{CCLK50}		50	Commercial	22	50	ns
			Industrial	21		ns
$T_{CCLK100}$		100	Commercial	11.2	25	ns
			Industrial	10.6		ns

Notes:

1. Set the ***ConfigRate*** option value when generating a configuration bitstream.

Table 47: **Master Mode CCLK Output Frequency by *ConfigRate* Option Setting**

Symbol	Description	*ConfigRate* Setting	Temperature Range	Minimum	Maximum	Units
F_{CCLK1}	Equivalent CCLK clock frequency by ***ConfigRate*** setting	1 *(power-on value)*	Commercial	0.400	0.797	MHz
			Industrial		0.847	MHz
F_{CCLK3}		3	Commercial	1.20	2.42	MHz
			Industrial		2.57	MHz
F_{CCLK6}		6 (default)	Commercial	2.40	4.83	MHz
			Industrial		5.13	MHz
F_{CCLK7}		7	Commercial	2.80	5.61	MHz
			Industrial		5.96	MHz
F_{CCLK8}		8	Commercial	3.20	6.41	MHz
			Industrial		6.81	MHz
F_{CCLK10}		10	Commercial	4.00	8.12	MHz
			Industrial		8.63	MHz
F_{CCLK12}		12	Commercial	4.80	9.70	MHz
			Industrial		10.31	MHz
F_{CCLK13}		13	Commercial	5.20	10.69	MHz
			Industrial		11.37	MHz
F_{CCLK17}		17	Commercial	6.80	13.74	MHz
			Industrial		14.61	MHz
F_{CCLK22}		22	Commercial	8.80	18.44	MHz
			Industrial		19.61	MHz
F_{CCLK25}		25	Commercial	10.00	20.90	MHz
			Industrial		22.23	MHz
F_{CCLK27}		27	Commercial	10.80	22.39	MHz
			Industrial		23.81	MHz
F_{CCLK33}		33	Commercial	13.20	27.48	MHz
			Industrial		29.23	MHz
F_{CCLK44}		44	Commercial	17.60	37.60	MHz
			Industrial		40.00	MHz
F_{CCLK50}		50	Commercial	20.00	44.80	MHz
			Industrial		47.66	MHz
$F_{CCLK100}$		100	Commercial	40.00	88.68	MHz
			Industrial		94.34	MHz

Table 48: **Master Mode CCLK Output Minimum Low and High Time**

Symbol	Description		*ConfigRate* Setting															Units
			1	3	6	7	8	10	12	13	17	22	25	27	33	44	50	100	
T_{MCCL}, T_{MCCH}	Master Mode CCLK Minimum Low and High Time	Commercial	595	196	98.3	84.5	74.1	58.4	48.9	44.1	34.2	25.6	22.3	20.9	17.1	12.3	10.4	5.3	ns
		Industrial	560	185	92.6	79.8	69.8	55.0	46.0	41.8	32.3	24.2	21.4	20.0	16.2	11.9	10.0	5.0	ns

Table 49: **Slave Mode CCLK Input Low and High Time**

Symbol	Description	Min	Max	Units
T_{SCCL} T_{SCCH}	CCLK Low and High time	5	∞	ns

Master Serial and Slave Serial Mode Timing

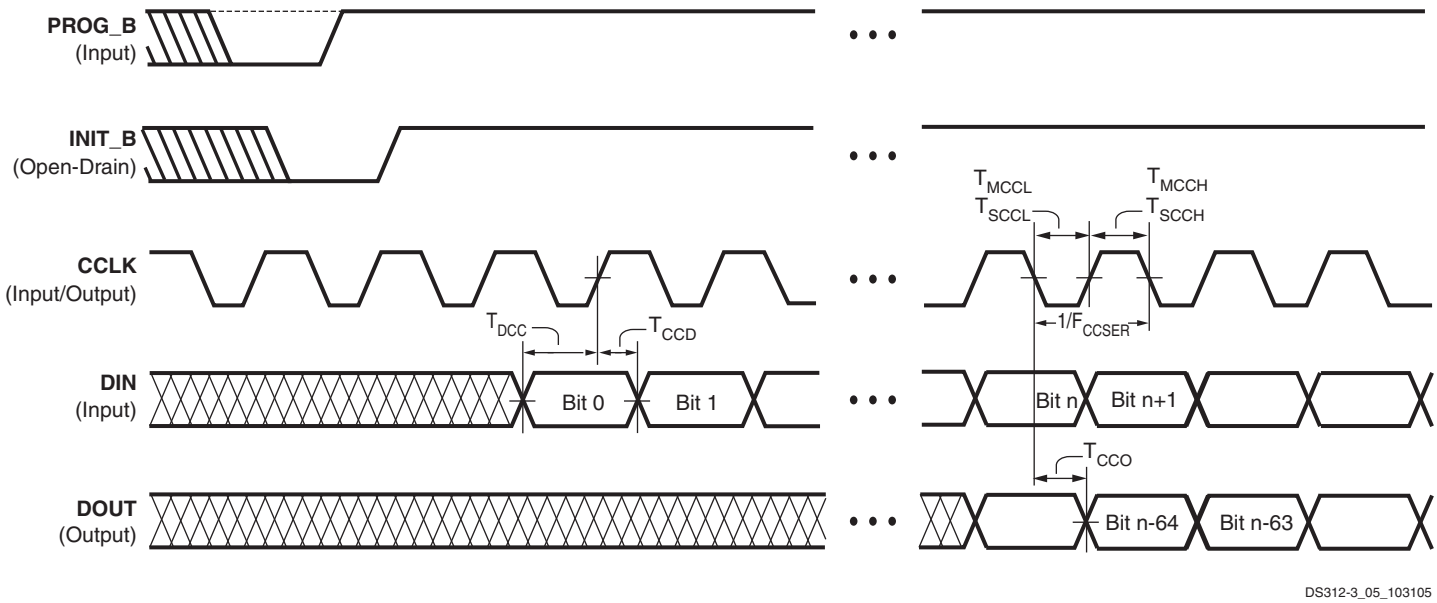


Figure 11: **Waveforms for Master Serial and Slave Serial Configuration**

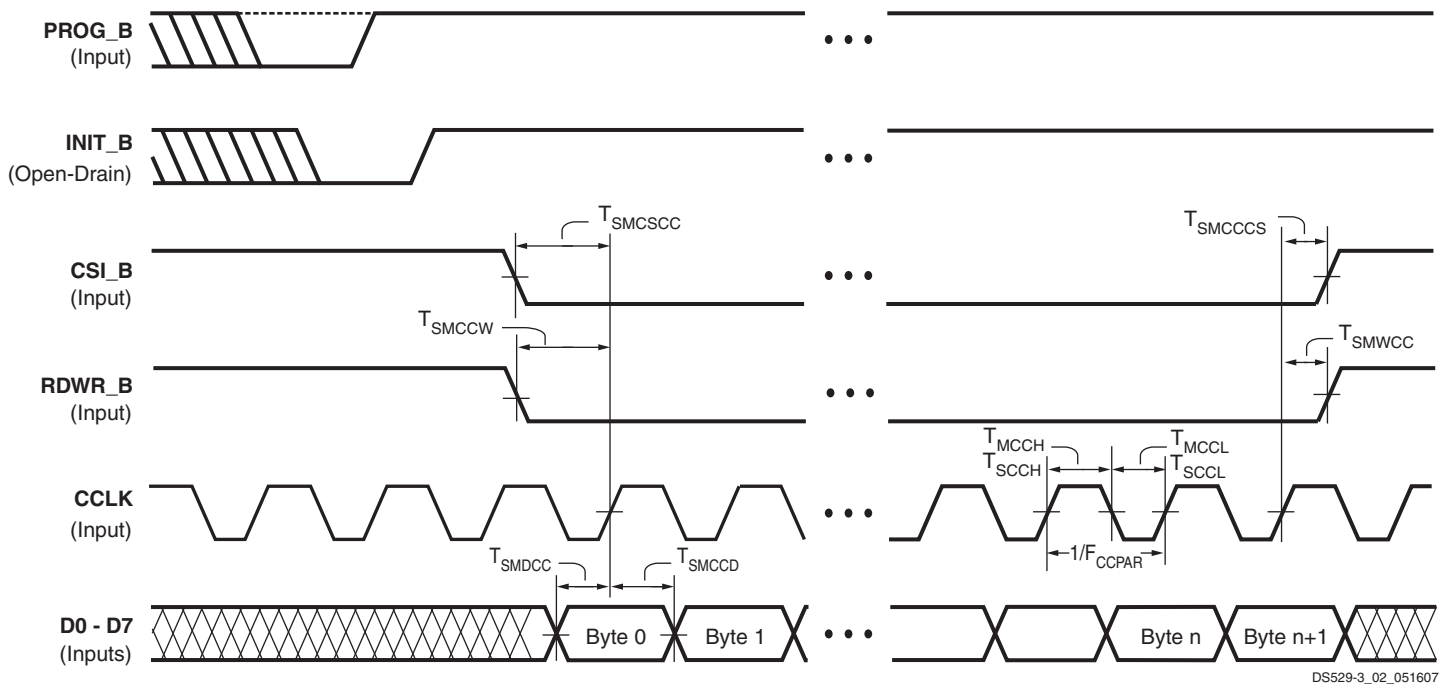
Table 50: **Timing for the Master Serial and Slave Serial Configuration Modes**

Symbol	Description		Slave/ Master	All Speed Grades		Units
				Min	Max	
Clock-to-Output Times						
T_{CCO}	The time from the falling transition on the CCLK pin to data appearing at the DOUT pin		Both	1.5	10	ns
Setup Times						
T_{DCC}	The time from the setup of data at the DIN pin to the rising transition at the CCLK pin		Both	7	–	ns
Hold Times						
T_{CCD}	The time from the rising transition at the CCLK pin to the point when data is last held at the DIN pin		Master	0.0	–	ns
			Slave	1.0	–	ns
Clock Timing						
T_{CCH}	High pulse width at the CCLK input pin		Master	See Table 48		
			Slave	See Table 49		
T_{CCL}	Low pulse width at the CCLK input pin		Master	See Table 48		
			Slave	See Table 49		
F_{CCSER}	Frequency of the clock signal at the CCLK input pin(2)	No bitstream compression	Slave	0	100	MHz
		With bitstream compression		0	100	MHz

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 7.
2. For serial configuration with a daisy-chain of multiple FPGAs, the maximum limit is 25 MHz.

Slave Parallel Mode Timing



Notes:

1. It is possible to abort configuration by pulling CSI_B Low in a given CCLK cycle, then switching RDWR_B Low or High in any subsequent cycle for which CSI_B remains Low. The RDWR_B pin asynchronously controls the driver impedance of the D0–D7 bus. When RDWR_B switches High, be careful to avoid contention on the D0–D7 bus.
2. To pause configuration, pause CCLK instead of de-asserting CSI_B. See UG332, Chapter 7, section “Non-Continuous SelectMAP Data Loading” for more details.

Figure 12: **Waveforms for Slave Parallel Configuration**

Table 51: **Timing for the Slave Parallel Configuration Mode**

Symbol	Description		All Speed Grades		Units
			Min	Max	
Setup Times					
T_{SMDCC}(2)	The time from the setup of data at the D0-D7 pins to the rising transition at the CCLK pin		7	–	ns
T_{SMCSCC}	Setup time on the CSI_B pin before the rising transition at the CCLK pin		7	–	ns
T_{SMCCW}	Setup time on the RDWR_B pin before the rising transition at the CCLK pin		17	–	ns
Hold Times					
T_{SMCCD}	The time from the rising transition at the CCLK pin to the point when data is last held at the D0-D7 pins		1	–	ns
T_{SMCCCS}	The time from the rising transition at the CCLK pin to the point when a logic level is last held at the CSO_B pin		0	–	ns
T_{SMWCC}	The time from the rising transition at the CCLK pin to the point when a logic level is last held at the RDWR_B pin		0	–	ns
Clock Timing					
T_{CCH}	The High pulse width at the CCLK input pin		5	–	ns
T_{CCL}	The Low pulse width at the CCLK input pin		5	–	ns
F_{CCPAR}	Frequency of the clock signal at the CCLK input pin	No bitstream compression	0	80	MHz
		With bitstream compression	0	80	MHz

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 7.
2. Some Xilinx documents refer to Parallel modes as “SelectMAP” modes.

Serial Peripheral Interface (SPI) Configuration Timing

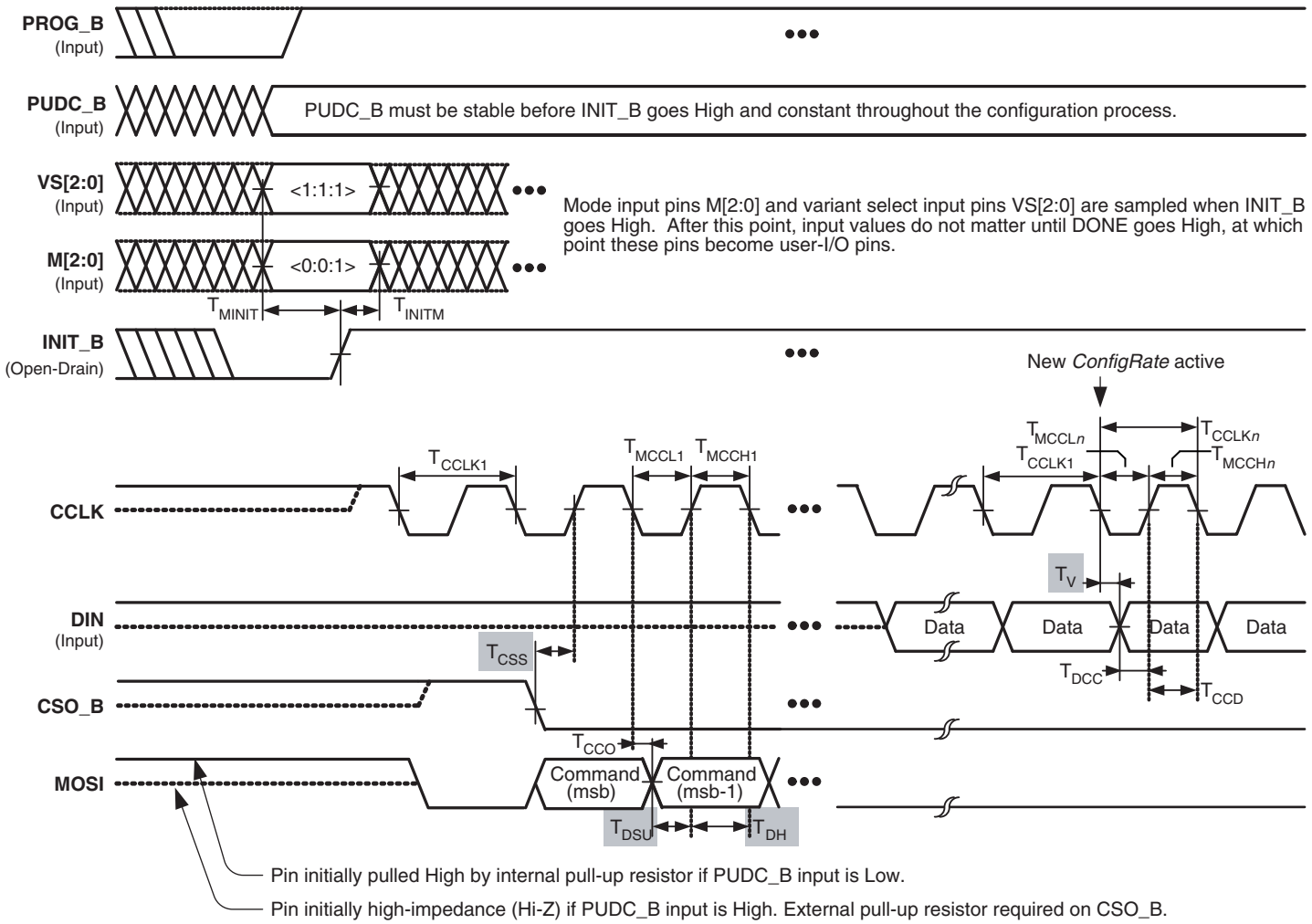


Figure 13: **Waveforms for Serial Peripheral Interface (SPI) Configuration**

Table 52: **Timing for Serial Peripheral Interface (SPI) Configuration Mode**

Symbol	Description	Minimum	Maximum	Units
T_{CCLK1}	Initial CCLK clock period	See Table 46		
T_{CCLKn}	CCLK clock period after FPGA loads ConfigRate setting	See Table 46		
T_{MINIT}	Setup time on VS[2:0] variant-select pins and M[2:0] mode pins before the rising edge of INIT_B	50	–	ns
T_{INITM}	Hold time on VS[2:0] variant-select pins and M[2:0] mode pins after the rising edge of INIT_B	0	–	ns
T_{CCO}	MOSI output valid delay after CCLK falling edge	See Table 50		
T_{DCC}	Setup time on DIN data input before CCLK rising edge	See Table 50		
T_{CCD}	Hold time on DIN data input after CCLK rising edge	See Table 50		

Table 53: **Configuration Timing Requirements for Attached SPI Serial Flash**

Symbol	Description	Requirement	Units
T_{CCS}	SPI serial Flash PROM chip-select time	$T_{CCS} \leq T_{MCCL1} - T_{CCO}$	ns
T_{DSU}	SPI serial Flash PROM data input setup time	$T_{DSU} \leq T_{MCCL1} - T_{CCO}$	ns
T_{DH}	SPI serial Flash PROM data input hold time	$T_{DH} \leq T_{MCCH1}$	ns
T_V	SPI serial Flash PROM data clock-to-output time	$T_V \leq T_{MCCLn} - T_{DCC}$	ns
f_C or f_R	Maximum SPI serial Flash PROM clock frequency (also depends on specific read command used)	$f_C \geq \frac{1}{T_{CCLKn(min)}}$	MHz

Notes:

1. These requirements are for successful FPGA configuration in SPI mode, where the FPGA generates the CCLK signal. The post-configuration timing can be different to support the specific needs of the application loaded into the FPGA.
2. Subtract additional printed circuit board routing delay as required by the application.

Byte Peripheral Interface (BPI) Configuration Timing

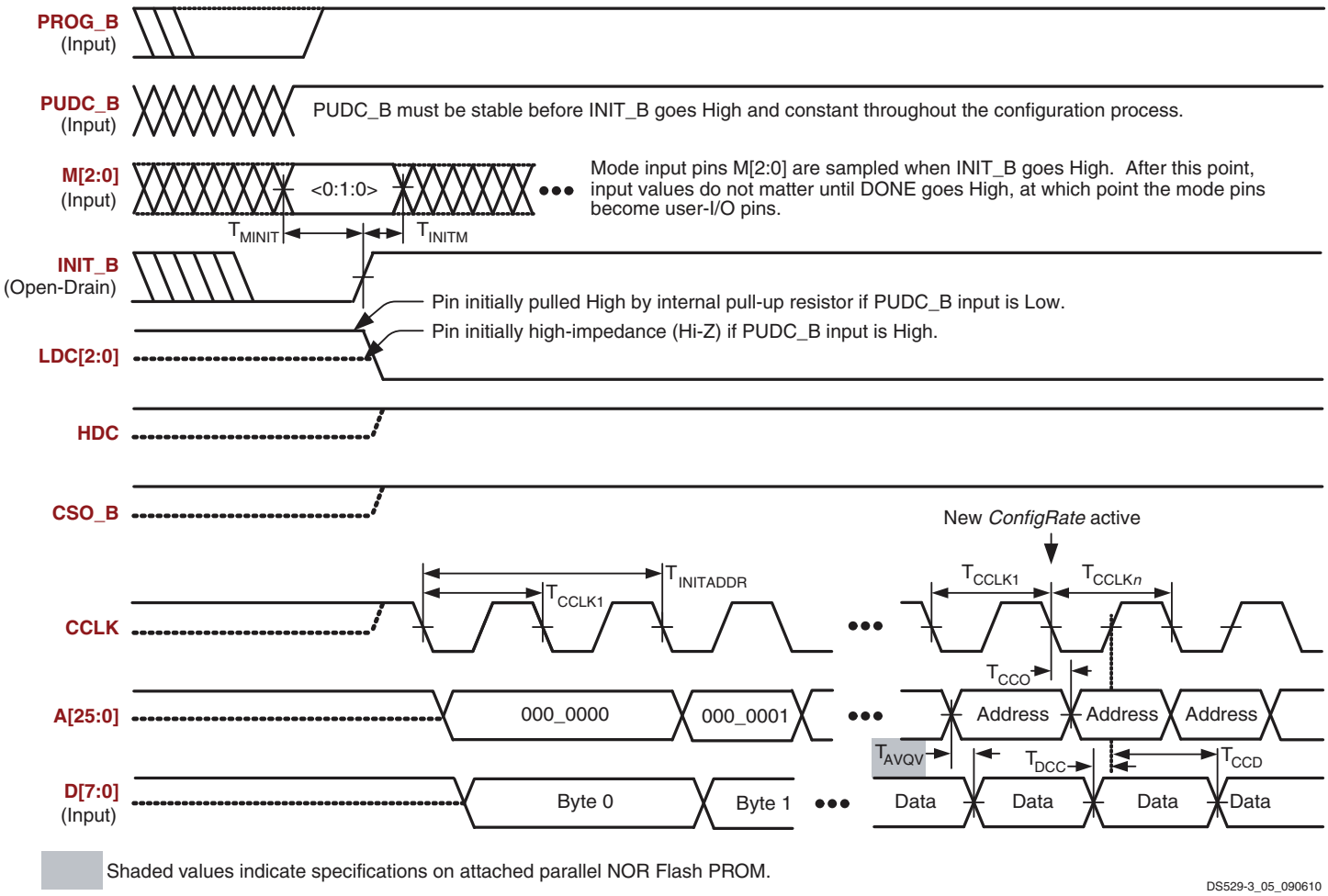


Figure 14: **Waveforms for Byte-wide Peripheral Interface (BPI) Configuration**

Table 54: **Timing for Byte-wide Peripheral Interface (BPI) Configuration Mode**

Symbol	Description	Minimum	Maximum	Units
T_{CCLK1}	Initial CCLK clock period	See Table 46		
T_{CCLKn}	CCLK clock period after FPGA loads ConfigRate setting	See Table 46		
T_{MINIT}	Setup time on M[2:0] mode pins before the rising edge of INIT_B	50	–	ns
T_{INITM}	Hold time on M[2:0] mode pins after the rising edge of INIT_B	0	–	ns
$T_{INITADDR}$	Minimum period of initial A[25:0] address cycle; LDC[2:0] and HDC are asserted and valid	5	5	T_{CCLK1} cycles
T_{CCO}	Address A[25:0] outputs valid after CCLK falling edge	See Table 50		
T_{DCC}	Setup time on D[7:0] data inputs before CCLK rising edge	See T_{SMDCC} in Table 51		
T_{CCD}	Hold time on D[7:0] data inputs after CCLK rising edge	0	–	ns

Table 55: **Configuration Timing Requirements for Attached Parallel NOR BPI Flash**

Symbol	Description	Requirement	Units
T_{CE} (t_{ELQV})	Parallel NOR Flash PROM chip-select time	$T_{CE} \leq T_{INITADDR}$	ns
T_{OE} (t_{GLQV})	Parallel NOR Flash PROM output-enable time	$T_{OE} \leq T_{INITADDR}$	ns
T_{ACC} (t_{AVQV})	Parallel NOR Flash PROM read access time	$T_{ACC} \leq 50\% T_{CCLKn(min)} - T_{CCO} - T_{DCC} - PCB$	ns
T_{BYTE} (t_{FLQV}, t_{FHQV})	For x8/x16 PROMs only: BYTE# to output valid time(3)	$T_{BYTE} \leq T_{INITADDR}$	ns

Notes:

1. These requirements are for successful FPGA configuration in BPI mode, where the FPGA generates the CCLK signal. The post-configuration timing can be different to support the specific needs of the application loaded into the FPGA.
2. Subtract additional printed circuit board routing delay as required by the application.
3. The initial BYTE# timing can be extended using an external, appropriately sized pull-down resistor on the FPGA's LDC2 pin. The resistor value also depends on whether the FPGA's PUDC_B pin is High or Low.

IEEE 1149.1/1532 JTAG Test Access Port Timing

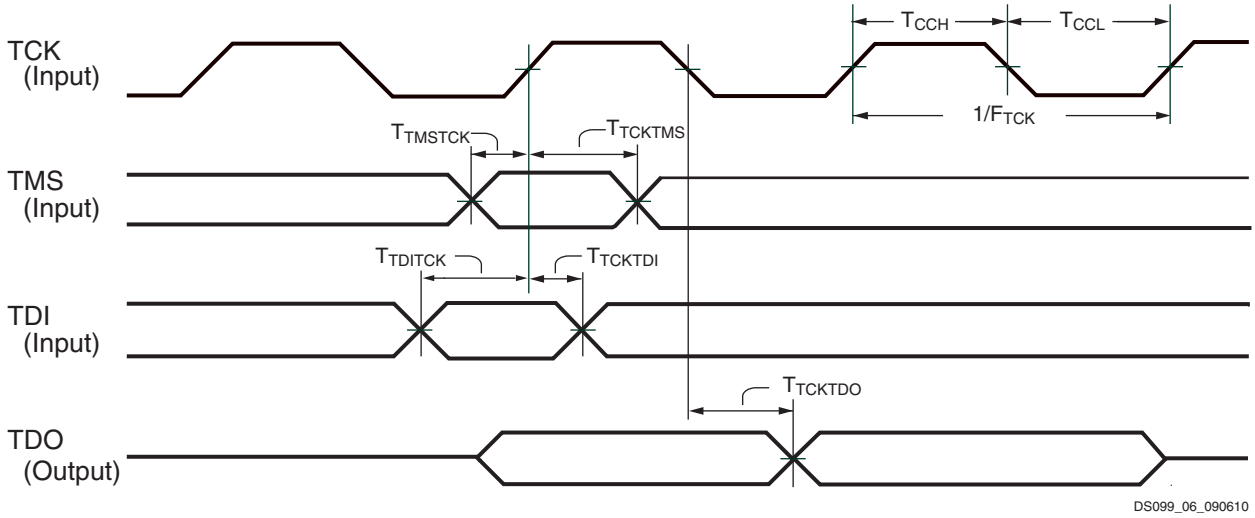


Figure 15: **JTAG Waveforms**

Table 56: **Timing for the JTAG[2] Test Access Port**

Symbol	Description		All Speed Grades		Units
			Min	Max	
Clock-to-Output Times					
T_{TCKTDO}	The time from the falling transition on the TCK pin to data appearing at the TDO pin		1.0	11.0	ns
Setup Times					
T_{TDITCK}	The time from the setup of data at the TDI pin to the rising transition at the TCK pin	All functions except those shown below	7.0	–	ns
		Boundary scan commands (INTEST, EXTEST, SAMPLE)	13.0		
T_{TMSTCK}	The time from the setup of a logic level at the TMS pin to the rising transition at the TCK pin		7.0	–	ns
Hold Times					
T_{TCKTDI}	The time from the rising transition at the TCK pin to the point when data is last held at the TDI pin	All functions except those shown below	0	–	ns
		Configuration commands (CFG_IN, ISC_PROGRAM)	3.5		
T_{TCKTMS}	The time from the rising transition at the TCK pin to the point when a logic level is last held at the TMS pin		0	–	ns
Clock Timing					
T_{CCH}	The High pulse width at the TCK pin	All functions except ISC_DNA command	5	–	ns
T_{CCL}	The Low pulse width at the TCK pin		5	–	ns
T_{CCHDNA}	The High pulse width at the TCK pin	During ISC_DNA command	10	10,000	ns
T_{CCLDNA}	The Low pulse width at the TCK pin		10	10,000	ns
F_{TCK}	Frequency of the TCK signal	BYPASS or HIGHZ instructions	0	33	MHz
		All operations except for BYPASS or HIGHZ instructions		20	

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 7.
2. For details on JTAG, see Chapter 9, “JTAG Configuraton Mode and Boundary-Scan” in UG332: *Spartan-3 Generation Configuration User Guide*.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
04/02/07	1.0	Initial Xilinx release.
05/25/07	1.0.1	Minor edits.
06/18/07	1.2	Updated for v1.29 production speed files. Noted banking rules in Table 11 and Table 12. Added DIFF_HSTL_I and DIFF_HSTL_III to Table 12, Table 13, and Table 26. Updated TMDS DC characteristics in Table 13. Updated I/O Test Method values in Table 26. Added Simultaneously Switching Output limits in Table 28. Updated DSP48A timing symbols, descriptions, and values in Table 34. Added power-on timing in Table 45. Added CCLK specifications for Commercial in Table 46 through Table 48. Updated Slave Parallel timing in Table 51. Updated JTAG specifications in Table 56.
07/16/07	2.0	Added Low-power options and updated typical values for quiescent current in Table 9. Updated DSP48A timing in Table 34 and Table 35.
06/02/08	2.1	Improved V_{CCAUXT} and V_{CCO2T} POR minimum in Table 4 and updated V_{CCO} POR levels in Figure 10. Added V_{IN} to Recommended Operating Conditions in Table 7 and added reference to XAPP459, "Eliminating I/O Coupling Effects when Interfacing Large-Swing Single-Ended Signals to User I/O Pins." Reduced typical I_{CCINTQ} and I_{CCAUXQ} quiescent current values by 20%-44% in Table 9. Increased V_{IL} max to 0.4V for LVCMOS12/15/18 and improved V_{IH} min to 0.7V for LVCMOS12 in Table 10. Changed V_{OL} max to 0.4V and V_{OH} min to V_{CCO}–0.4V for LVCMOS15/18 in Table 11. Added reference to V_{CCAUX} in Simultaneously Switching Output Guidelines. Removed DNA_RETENTION limit of 10 years in Table 14 since number of Read cycles is the only unique limit. Updated speed files to v1.31 in Table 16 and elsewhere. Updated IOB Setup and Hold times with device-specific values in Table 19. Added reference to Sample Window in Table 20. Updated IOB Propagation times with device-specific values in Table 21. Improved SSTL_18_II SSO value in Table 28. Improved F_{BUFG} for -4 to 334 MHz in Table 32. Added references to 375 MHz performance via SCD 4103 in Table 32,Table 37, Table 38, and Table 39. Added explanatory footnotes to DSP48A Timing tables. Simplified DSP48A F_{MAX} to value with all registers used in Table 35. Improved FBUFG in Table 32 for -4 speed grade. Updated CCLK output maximum period in Table 46 to match minimum frequency in Table 47. Replaced BPI with SPI specification descriptions in Table 52. Corrected BPI Figure 14 and Table 54 from falling edge to rising edge. Added references to Spartan-3 Generation User Guides. Updated links.
03/11/09	2.2	Changed typical quiescent current temperature from ambient to quiescent. Updated selected I/O standard DC characteristics. Removed PCIX IOSTANDARD due to limited PCIX interface support. Added T_{IOPI} and T_{IOPID} to Table 21. Updated BPI configuration waveforms in Figure 14 and updated Table 55. Removed references to SCD 4103.
10/04/10	3.0	Added I_{IK} to Table 3. Updated description for V_{IN} in Table 7 including adding note 4. Also, added note 2 to I_L in Table 8 to note potential leakage between pins of a differential pair. Added note 6 to Table 10. Updated notes 5 and 6 in Table 12. Corrected symbols for $T_{SUSPEND\_GTS}$ and $T_{SUSPEND\_GWE}$ in Table 44.

Introduction

This section describes how the various pins on a Spartan®-3A DSP FPGA connect within the supported component packages and provides device-specific thermal characteristics. For general information on the pin functions and the package characteristics, see the *Packaging* section in UG331: *Spartan-3 Generation FPGA User Guide.*

Spartan-3A DSP FPGAs are available in both standard and Pb-free, RoHS versions of each package, with the Pb-free version adding a “G” to the middle of the package code. Except for the thermal characteristics, all information for the standard package applies equally to the Pb-free package.

Pin Types

Most pins on a Spartan-3A DSP FPGA are general-purpose, user-defined I/O pins. There are, however, up to 12 different functional types of pins on Spartan-3A DSP packages, as outlined in Table 57. In the package footprint drawings that follow, the individual pins are color-coded according to pin type as in the table.

Table 57: **Types of Pins on Spartan-3A DSP FPGAs**

Type/Color Code	Description	Pin Name(s) in Type
I/O	Unrestricted, general-purpose user-I/O pin. Most pins can be paired together to form differential I/Os.	IO_# IO_Lxxy_#
INPUT	Unrestricted, general-purpose input-only pin. This pin does not have an output structure, differential termination resistor, or PCI clamp diode.	IP_# IP_Lxxy_#
DUAL	Dual-purpose pin used in some configuration modes during the configuration process and then usually available as a user I/O after configuration. If the pin is not used during configuration, this pin behaves as an I/O-type pin. See UG332: *Spartan-3 Generation Configuration User Guide* for additional information on these signals.	M[2:0] PUDC_B CCLK MOSI/CSI_B D[7:1] D0/DIN CSO_B RDWR_B INIT_B A[25:0] VS[2:0] LDC[2:0] HDC
VREF	Dual-purpose pin that is either a user-I/O pin or Input-only pin, or, along with all other VREF pins in the same bank, provides a reference voltage input for certain I/O standards. If used for a reference voltage within a bank, all VREF pins within the bank must be connected.	IP/VREF_# IP_Lxxy_#/VREF_# IO/VREF_# IO_Lxxy_#/VREF_#
CLK	Either a user-I/O pin or an input to a specific clock buffer driver. Packages have 16 global clock inputs that optionally clock the entire device. The RHCLK inputs optionally clock the right half of the device. The LHCLK inputs optionally clock the left half of the device. See the Using Global Clock Resources chapter in UG331: *Spartan-3 Generation FPGA User Guide* for additional information on these signals.	IO_Lxxy_#/GCLK[15:0], IO_Lxxy_#/LHCLK[7:0], IO_Lxxy_#/RHCLK[7:0]
CONFIG	Dedicated configuration pin, two per device. Not available as a user-I/O pin. Every package has two dedicated configuration pins. These pins are powered by VCCAUX. See the UG332: *Spartan-3 Generation Configuration User Guide* for additional information on the DONE and PROG_B signals.	DONE, PROG_B

Table 57: **Types of Pins on Spartan-3A DSP FPGAs *(Cont'd)***

Type/Color Code	Description	Pin Name(s) in Type
PWR MGMT	Control and status pins for the power-saving Suspend mode. SUSPEND is a dedicated pin and is powered by VCCAUX. AWAKE is a dual-purpose pin. Unless Suspend mode is enabled in the application, AWAKE is available as a user-I/O pin.	SUSPEND, AWAKE
JTAG	Dedicated JTAG pin - 4 per device. Not available as a user-I/O pin. Every package has four dedicated JTAG pins. These pins are powered by VCCAUX.	TDI, TMS, TCK, TDO
GND	Dedicated ground pin. The number of GND pins depends on the package used. All must be connected.	GND
VCCAUX	Dedicated auxiliary power supply pin. The number of VCCAUX pins depends on the package used. All must be connected. Set on board and using CONFIG VCCAUX constraint.	VCCAUX
VCCINT	Dedicated internal core logic power supply pin. The number of VCCINT pins depends on the package used. All must be connected to +1.2V.	VCCINT
VCCO	Along with all the other VCCO pins in the same bank, this pin supplies power to the output buffers within the I/O bank and sets the input threshold voltage for some I/O standards. All must be connected.	VCCO_#
N.C.	This package pin is not connected in this specific device/package combination but may be connected in larger devices in the same package.	N.C.

Notes:

1. # = I/O bank number, an integer between 0 and 3.

Package Pins by Type

Each package has three separate voltage supply inputs—VCCINT, VCCAUX, and VCCO—and a common ground return, GND. The numbers of pins dedicated to these functions vary by package, as shown in Table 58.

Table 58: **Power and Ground Supply Pins by Package**

Package	Device	VCCINT	VCCAUX	VCCO	GND
CS484	XC3SD1800A	36	24	24	84
	XC3SD3400A	36	24	24	84
FG676	XC3SD1800A	23	14	36	77
	XC3SD3400A	36	24	40	100

A majority of package pins are user-defined I/O or input pins. However, the numbers and characteristics of these I/O depend on the device type and the package in which it is available, as shown in Table 59. The table shows the maximum number of single-ended I/O pins available, assuming that all I/O-, INPUT-, DUAL-, VREF-, and CLK-type pins are used as general-purpose I/O. AWAKE is counted here as a dual-purpose I/O pin. Likewise, the table shows the maximum number of differential pin-pairs available on the package. Finally, the table shows how the total maximum user-I/Os are distributed by pin type, including the number of unconnected—N.C.—pins on the device.

Not all I/O standards are supported on all I/O banks. The left and right banks (I/O banks 1 and 3) support higher output drive current than the top and bottom banks (I/O banks 0 and 2). Similarly, true differential output standards, such as LVDS, RSDS, PPDS, miniLVDS, and TMDS, are only supported in the top or bottom banks (I/O banks 0 and 2). Inputs are unrestricted. For more details, see the *Using I/O Resources* chapter in UG331.

Table 59: **Maximum User I/O by Package**

Package	Device	Maximum User I/Os and Input-Only	Maximum Input-Only	Maximum Differential Pairs	All Possible I/Os by Type					
					I/O	INPUT	DUAL	VREF[1]	CLK	N.C.
CS484	XC3SD1800A	309	60	140	156	41	52	28	32	0
	XC3SD3400A	309	60	140	156	41	52	28	32	0
FG676	XC3SD1800A	519	110	227	314	82	52	39	32	0
	XC3SD3400A	469	60	213	314	34	52	37	32	0

Notes:

1. Some VREFs are on INPUT pins. See pinout tables for details.

Electronic versions of the package pinout tables and foot- prints are available for download from the Xilinx® website. Using a spreadsheet program, the data can be sorted and reformatted according to any specific needs. Similarly, the ASCII-text file is easily parsed by most scripting programs. www.xilinx.com/support/documentation/data_sheets/s3a_pin.zip

Package Overview

Table 60 shows the two low-cost, space-saving production package styles for the Spartan-3A DSP family.

Table 60: **Spartan-3A DSP Family Package Options**

Package	Leads	Type	Maximum I/O	Lead Pitch (mm)	Footprint Area (mm)	Height (mm)	Mass(1) (g)
CS484 / CSG484	484	Chip-Scale Ball Grid Array (CS)	309	0.8	19 x 19	1.80	1.4
FG676 / FGG676	676	Fine-pitch Ball Grid Array (FBGA)	519	1.0	27 x 27	2.60	3.4

Notes:

1. Package mass is ±10%.

Each package style is available as a standard and an environmentally friendly lead-free (Pb-free) option. The Pb-free packages include an extra 'G' in the package style name. For example, the standard "CS484" package becomes "CSG484" when ordered as the Pb-free option. The mechanical dimensions of the standard and Pb-free packages are similar, as shown in the mechanical drawings provided in Table 61.

For additional package information, see UG112: *Device Package User Guide*.

Mechanical Drawings

Detailed mechanical drawings for each package type are available from the Xilinx web site at the specified location in Table 61.

Material Declaration Data Sheets (MDDS) are also available on the Xilinx web site for each package.

Table 61: **Xilinx Package Documentation**

Package	Drawing	MDDS
CS484	Package Drawing	PK230_CS484
CSG484		PK231_CSG484
FG676	Package Drawing	PK155_FG676
FGG676		PK111_FGG676

Package Thermal Characteristics

The power dissipated by an FPGA application has implications on package selection and system design. The power consumed by a Spartan-3A DSP FPGA is reported using either the XPower Power Estimator or the XPower Analyzer calculator integrated in the Xilinx ISE® development software. Table 62 provides the thermal characteristics for the various Spartan-3A DSP device package offerings. This information is also available using the Thermal Query tool.

The junction-to-case thermal resistance (θ_{JC}) indicates the difference between the temperature measured on the package body (case) and the die junction temperature per watt of power consumption. The junction-to-board (θ_{JB}) value similarly reports the difference between the board and junction temperature. The junction-to-ambient (θ_{JA}) value reports the temperature difference between the ambient environment and the junction temperature. The θ_{JA} value is reported at different air velocities, measured in linear feet per minute (LFM). The "Still Air (0 LFM)" column shows the θ_{JA} value in a system without a fan. The thermal resistance drops with increasing air flow.

Table 62: **Spartan-3A DSP FPGA Package Thermal Characteristics**

Package	Device	Junction-to-Case (θ_{JC})	Junction-to-Board (θ_{JB})	Junction-to-Ambient (θ_{JA}) at Different Air Flows				Units
				Still Air (0 LFM)	250 LFM	500 LFM	750 LFM	
CS484 CSG484	XC3SD1800A	4.1	6.8	18.0	13.3	12.3	11.5	°C/W
	XC3SD3400A	3.5	5.6	16.9	12.2	11.0	10.4	°C/W
FG676 FGG676	XC3SD1800A	4.7	7.8	15.9	11.6	10.6	10.0	°C/W
	XC3SD3400A	3.8	6.4	14.7	10.5	9.4	8.9	°C/W

CS484: 484-Ball Chip-Scale Ball Grid Array

The 484-ball chip-scale ball grid array, CS484, supports both the XC3SD1800A and XC3SD3400A FPGAs. There are no pinout differences between the two devices.

Table 63 lists all the CS484 package pins. They are sorted by bank number and then by pin name. Pairs of pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at www.xilinx.com/support/documentation/data_sheets/s3a_pin.zip

Pinout Table

Table 63: **Spartan-3A DSP CS484 Pinout**

Bank	Pin Name	CS484 Ball	Type
0	IO_L30N_0	A3	I/O
0	IO_L28N_0	A4	I/O
0	IO_L25N_0	A5	I/O
0	IO_L25P_0	A6	I/O
0	IO_L24N_0/VREF_0	A7	VREF
0	IO_L20P_0/GCLK10	A8	GCLK
0	IO_L18P_0/GCLK6	A9	GCLK
0	IP_0	A10	INPUT
0	IO_L15N_0	A11	I/O
0	IP_0	A12	INPUT
0	IO_L11P_0	A13	I/O
0	IO_L10P_0	A14	I/O
0	IP_0	A15	INPUT
0	IO_L06P_0/VREF_0	A16	VREF
0	IO_L06N_0	A17	I/O
0	IP_0	A18	INPUT
0	IO_L07N_0	A19	I/O
0	IO_0	A20	I/O
0	IO_L30P_0	B3	I/O
0	IO_L28P_0	B4	I/O
0	IO_L24P_0	B6	I/O
0	IO_L20N_0/GCLK11	B8	GCLK
0	IO_L18N_0/GCLK7	B9	GCLK
0	IO_L15P_0	B11	I/O
0	IO_L11N_0	B13	I/O
0	IO_L10N_0	B15	I/O
0	IO_L03P_0	B17	I/O
0	IO_L02N_0	B19	I/O

Table 63: **Spartan-3A DSP CS484 Pinout *(Cont'd)***

Bank	Pin Name	CS484 Ball	Type
0	IO_L07P_0	B20	I/O
0	IO_L29N_0	C4	I/O
0	IP_0	C5	INPUT
0	IO_L21P_0	C6	I/O
0	IO_L26P_0	C7	I/O
0	IO_L22P_0	C8	I/O
0	IO_L16P_0	C9	I/O
0	IP_0	C10	INPUT
0	IP_0/VREF_0	C11	VREF
0	IO_L14N_0	C12	I/O
0	IO_L14P_0	C13	I/O
0	IP_0	C14	INPUT
0	IO_L12N_0/VREF_0	C15	VREF
0	IO_L08N_0	C16	I/O
0	IO_L03N_0	C17	I/O
0	IO_L02P_0/VREF_0	C18	VREF
0	IO_L01N_0	C19	I/O
0	IO_L29P_0	D5	I/O
0	IO_L21N_0	D6	I/O
0	IO_L26N_0	D7	I/O
0	IO_L22N_0	D9	I/O
0	IO_L16N_0	D10	I/O
0	IO_L09N_0	D13	I/O
0	IO_L12P_0	D14	I/O
0	IO_L08P_0	D15	I/O
0	IP_0	D17	INPUT
0	IP_0	D18	INPUT
0	IO_L01P_0	D19	I/O
0	IP_0	E6	INPUT
0	IO_L31P_0/VREF_0	E7	VREF
0	IO_L27N_0	E8	I/O
0	IP_0	E10	INPUT
0	IO_L19N_0/GCLK9	E11	GCLK
0	IO_L17P_0/GCLK4	E12	GCLK
0	IO_L09P_0	E13	I/O
0	IO_L05P_0	E15	I/O
0	IO_L04P_0	E16	I/O
0	IP_0	E17	INPUT
0	IO_L31N_0/PUDC_B	F7	DUAL
0	IO_L27P_0	F8	I/O
0	IO_L23N_0	F9	I/O

Table 63: **Spartan-3A DSP CS484 Pinout *(Cont'd)***

Bank	Pin Name	CS484 Ball	Type
0	IO_L19P_0/GCLK8	F10	GCLK
0	IO_L17N_0/GCLK5	F11	GCLK
0	IP_0	F12	INPUT
0	IO_L13N_0	F13	I/O
0	IO_L13P_0	F14	I/O
0	IO_L05N_0	F15	I/O
0	IO_L04N_0	F16	I/O
0	IO_L23P_0	G8	I/O
0	VCCO_0	B5	VCCO
0	VCCO_0	B10	VCCO
0	VCCO_0	B14	VCCO
0	VCCO_0	B18	VCCO
0	VCCO_0	E9	VCCO
0	VCCO_0	E14	VCCO
1	IO_L02N_1/LDC0	AA22	DUAL
1	IP_L39N_1	C21	INPUT
1	IP_L39P_1/VREF_1	C22	VREF
1	IO_L36P_1/A20	D20	DUAL
1	IO_L37P_1/A22	D21	DUAL
1	IO_L37N_1/A23	D22	DUAL
1	IO_L36N_1/A21	E19	DUAL
1	IO_L35N_1	E20	I/O
1	IO_L33N_1	E22	I/O
1	IO_L38N_1/A25	F18	DUAL
1	IO_L38P_1/A24	F19	DUAL
1	IO_L30N_1/A19	F20	DUAL
1	IO_L35P_1	F21	I/O
1	IO_L33P_1	F22	I/O
1	IO_L34P_1	G17	I/O
1	IO_L34N_1	G18	I/O
1	IO_L30P_1/A18	G19	DUAL
1	IP_L31N_1	G20	INPUT
1	IO_L28N_1	G22	I/O
1	IO_L26P_1/A14	H17	DUAL
1	IO_L26N_1/A15	H18	DUAL
1	IO_L32N_1	H20	I/O
1	IP_L31P_1/VREF_1	H21	VREF
1	IO_L28P_1	H22	I/O
1	IO_L29N_1/A17	J17	DUAL
1	IO_L32P_1	J19	I/O
1	IO_L25N_1/A13	J20	DUAL
1	IP_L27P_1	J21	INPUT

Table 63: **Spartan-3A DSP CS484 Pinout *(Cont'd)***

Bank	Pin Name	CS484 Ball	Type
1	IP_L27N_1	J22	INPUT
1	IO_L29P_1/A16	K16	DUAL
1	IP_L23N_1	K17	INPUT
1	IO_L24N_1	K18	I/O
1	IO_L24P_1	K19	I/O
1	IO_L25P_1/A12	K20	DUAL
1	IO_L22N_1/A11	K22	DUAL
1	IO_L21N_1/RHCLK7	L17	RHCLK
1	IP_L23P_1/VREF_1	L18	VREF
1	IO_L20N_1/RHCLK5	L20	RHCLK
1	IO_L20P_1/RHCLK4	L21	RHCLK
1	IO_L22P_1/A10	L22	DUAL
1	IO_L18N_1/RHCLK1	M17	RHCLK
1	IO_L21P_1/IRDY1/RHCLK6	M18	RHCLK
1	IO_L19N_1/TRDY1/RHCLK3	M20	RHCLK
1	IO_L17N_1/A9	M22	DUAL
1	IO_L13P_1/A2	N17	DUAL
1	IO_L18P_1/RHCLK0	N18	RHCLK
1	IO_L15N_1/A7	N19	DUAL
1	IO_L15P_1/A6	N20	DUAL
1	IO_L19P_1/RHCLK2	N21	RHCLK
1	IO_L17P_1/A8	N22	DUAL
1	IO_L13N_1/A3	P16	DUAL
1	IP_L12N_1/VREF_1	P17	VREF
1	IO_L10P_1	P19	I/O
1	IP_L16N_1	P20	INPUT
1	IO_L14N_1/A5	P22	DUAL
1	IP_L12P_1	R17	INPUT
1	IO_L10N_1	R18	I/O
1	IO_L07P_1	R19	I/O
1	IO_L07N_1	R20	I/O
1	IP_L16P_1/VREF_1	R21	VREF
1	IO_L14P_1/A4	R22	DUAL
1	IO_L05N_1	T17	I/O
1	IO_L05P_1	T18	I/O
1	IO_L09N_1	T20	I/O
1	IO_L11N_1/VREF_1	T22	VREF
1	IO_L01P_1/HDC	U18	DUAL
1	IO_L01N_1/LDC2	U19	DUAL
1	IO_L09P_1	U20	I/O
1	IP_L08N_1/VREF_1	U21	VREF
1	IO_L11P_1	U22	I/O

Table 63: **Spartan-3A DSP CS484 Pinout *(Cont'd)***

Bank	Pin Name	CS484 Ball	Type
1	IO_L03N_1/A1	V20	DUAL
1	IP_L08P_1	V22	INPUT
1	IO_L03P_1/A0	W19	DUAL
1	IP_L04N_1/VREF_1	W20	VREF
1	IP_L04P_1	W21	INPUT
1	IO_L06P_1	W22	I/O
1	IO_L02P_1/LDC1	Y21	DUAL
1	IO_L06N_1	Y22	I/O
1	VCCO_1	E21	VCCO
1	VCCO_1	J18	VCCO
1	VCCO_1	K21	VCCO
1	VCCO_1	P18	VCCO
1	VCCO_1	P21	VCCO
1	VCCO_1	V21	VCCO
2	IO_L01P_2/M1	AA3	DUAL
2	IO_L04N_2	AA4	I/O
2	IP_2	AA6	INPUT
2	IO_L08N_2	AA8	I/O
2	IO_L12N_2/D6	AA10	DUAL
2	IO_L16P_2/GCLK14	AA12	GCLK
2	IO_L18N_2/GCLK3	AA14	GCLK
2	IO_L19P_2	AA15	I/O
2	IO_L22P_2/AWAKE	AA17	PWRMGMT
2	IO_L27N_2	AA19	I/O
2	IO_L30P_2	AA20	I/O
2	IP_2/VREF_2	AB2	VREF
2	IO_L01N_2/M0	AB3	DUAL
2	IO_L04P_2	AB4	I/O
2	IO_L05P_2	AB5	I/O
2	IO_L05N_2	AB6	I/O
2	IO_L08P_2	AB7	I/O
2	IO_L09P_2/VS1	AB8	DUAL
2	IO_L09N_2/VS0	AB9	DUAL
2	IO_L12P_2/D7	AB10	DUAL
2	IP_2/VREF_2	AB11	VREF
2	IO_L16N_2/GCLK15	AB12	GCLK
2	IO_L18P_2/GCLK2	AB13	GCLK
2	IO_L19N_2	AB14	I/O
2	IP_2	AB15	INPUT
2	IO_L22N_2/DOUT	AB16	DUAL
2	IO_L23P_2	AB17	I/O
2	IO_L23N_2	AB18	I/O

Table 63: **Spartan-3A DSP CS484 Pinout *(Cont'd)***

Bank	Pin Name	CS484 Ball	Type
2	IO_L27P_2	AB19	I/O
2	IO_L30N_2	AB20	I/O
2	IO_L02N_2/CSO_B	U7	DUAL
2	IO_L11N_2	U8	I/O
2	IO_L10N_2	U9	I/O
2	IO_L14N_2/D4	U10	DUAL
2	IO_L17P_2/GCLK0	U12	GCLK
2	IO_L20P_2	U13	I/O
2	IO_L25P_2	U14	I/O
2	IO_L25N_2	U15	I/O
2	IO_L28P_2	U16	I/O
2	IO_L02P_2/M2	V6	DUAL
2	IO_L11P_2	V7	I/O
2	IO_L06N_2	V8	I/O
2	IO_L10P_2	V10	I/O
2	IO_L14P_2/D5	V11	DUAL
2	IO_L17N_2/GCLK1	V12	GCLK
2	IO_L20N_2/MOSI/CSI_B	V13	DUAL
2	IP_2/VREF_2	V15	VREF
2	IO_L28N_2	V16	I/O
2	IO_L31N_2/CCLK	V17	DUAL
2	IP_2/VREF_2	W4	VREF
2	IO_L03P_2	W5	I/O
2	IO_L07N_2/VS2	W6	DUAL
2	IO_L06P_2	W8	I/O
2	IP_2/VREF_2	W9	VREF
2	IP_2	W10	INPUT
2	IP_2/VREF_2	W13	VREF
2	IO_L21N_2	W14	I/O
2	IO_L24P_2/INIT_B	W15	DUAL
2	IO_L31P_2/D0/DIN/MISO	W17	DUAL
2	IP_2/VREF_2	W18	VREF
2	IO_L03N_2	Y4	I/O
2	IO_L07P_2/RDWR_B	Y5	DUAL
2	IP_2	Y6	INPUT
2	IP_2	Y7	INPUT
2	IO_L13P_2	Y8	I/O
2	IO_L13N_2	Y9	I/O
2	IO_L15N_2/GCLK13	Y10	GCLK
2	IO_L15P_2/GCLK12	Y11	GCLK
2	IP_2	Y12	INPUT
2	IO_L21P_2	Y13	I/O

Table 63: **Spartan-3A DSP CS484 Pinout *(Cont'd)***

Bank	Pin Name	CS484 Ball	Type
2	IP_2/VREF_2	Y14	VREF
2	IO_L24N_2/D3	Y15	DUAL
2	IO_L29N_2	Y16	I/O
2	IO_L29P_2	Y17	I/O
2	IO_L26P_2/D2	Y18	DUAL
2	IO_L26N_2/D1	Y19	DUAL
2	VCCO_2	AA5	VCCO
2	VCCO_2	AA9	VCCO
2	VCCO_2	AA13	VCCO
2	VCCO_2	AA18	VCCO
2	VCCO_2	V9	VCCO
2	VCCO_2	V14	VCCO
3	IP_L39N_3/VREF_3	AA1	VREF
3	IO_L02N_3	C1	I/O
3	IO_L02P_3	C2	I/O
3	IP_L04P_3	D1	INPUT
3	IP_L08P_3	D3	INPUT
3	IP_L08N_3	D4	INPUT
3	IP_L04N_3/VREF_3	E1	VREF
3	IO_L09P_3	E3	I/O
3	IO_L09N_3	E4	I/O
3	IO_L06N_3	F1	I/O
3	IO_L06P_3	F2	I/O
3	IO_L01P_3	F3	I/O
3	IO_L03P_3	F4	I/O
3	IO_L03N_3	F5	I/O
3	IO_L11P_3	G1	I/O
3	IO_L01N_3	G3	I/O
3	IO_L07P_3	G5	I/O
3	IO_L07N_3	G6	I/O
3	IO_L11N_3	H1	I/O
3	IO_L14P_3	H2	I/O
3	IO_L05P_3	H3	I/O
3	IO_L05N_3	H4	I/O
3	IO_L10P_3	H5	I/O
3	IO_L10N_3	H6	I/O
3	IO_L14N_3/VREF_3	J1	VREF
3	IP_L16P_3	J3	INPUT
3	IP_L16N_3	J4	INPUT
3	IP_L12P_3	J6	INPUT
3	IP_L12N_3/VREF_3	J7	VREF
3	IO_L19P_3/LHCLK2	K1	LHCLK

Table 63: **Spartan-3A DSP CS484 Pinout *(Cont'd)***

Bank	Pin Name	CS484 Ball	Type
3	IO_L17P_3	K2	I/O
3	IO_L17N_3	K3	I/O
3	IO_L13P_3	K4	I/O
3	IO_L13N_3	K5	I/O
3	IO_L15P_3	K6	I/O
3	IO_L19N_3/IRDY2/LHCLK3	L1	LHCLK
3	IO_L20P_3/LHCLK4	L3	LHCLK
3	IO_L15N_3	L5	I/O
3	IO_L18P_3/LHCLK0	L6	LHCLK
3	IO_L22P_3/VREF_3	M1	VREF
3	IO_L20N_3/LHCLK5	M2	LHCLK
3	IP_L23P_3	M3	INPUT
3	IO_L18N_3/LHCLK1	M5	LHCLK
3	IO_L21P_3/TRDY2/LHCLK6	M6	LHCLK
3	IO_L22N_3	N1	I/O
3	IP_L31P_3	N3	INPUT
3	IP_L23N_3	N4	INPUT
3	IO_L24N_3	N5	I/O
3	IO_L24P_3	N6	I/O
3	IO_L21N_3/LHCLK7	N7	LHCLK
3	IO_L25P_3	P1	I/O
3	IO_L25N_3	P2	I/O
3	IP_L31N_3	P3	INPUT
3	IO_L32P_3/VREF_3	P4	VREF
3	IO_L26P_3	P6	I/O
3	IO_L28N_3	R1	I/O
3	IO_L28P_3	R2	I/O
3	IO_L34P_3	R3	I/O
3	IO_L32N_3	R5	I/O
3	IO_L26N_3	R6	I/O
3	IO_L30P_3	T1	I/O
3	IP_L27P_3	T3	INPUT
3	IO_L34N_3	T4	I/O
3	IO_L29N_3	T5	I/O
3	IO_L29P_3	T6	I/O
3	IO_L30N_3	U1	I/O
3	IO_L33P_3	U2	I/O
3	IP_L27N_3	U3	INPUT
3	IO_L38P_3	U4	I/O
3	IO_L38N_3	U5	I/O
3	IO_L33N_3	V1	I/O
3	IO_L36N_3	V3	I/O

Table 63: **Spartan-3A DSP CS484 Pinout *(Cont'd)***

Bank	Pin Name	CS484 Ball	Type
3	IO_L36P_3	V4	I/O
3	IO_L35N_3	W1	I/O
3	IO_L37N_3	W2	I/O
3	IO_L37P_3	W3	I/O
3	IO_L35P_3	Y1	I/O
3	IP_L39P_3	Y2	INPUT
3	VCCO_3	E2	VCCO
3	VCCO_3	J2	VCCO
3	VCCO_3	J5	VCCO
3	VCCO_3	N2	VCCO
3	VCCO_3	P5	VCCO
3	VCCO_3	V2	VCCO
GND	GND	A1	GND
GND	GND	A22	GND
GND	GND	AA7	GND
GND	GND	AA11	GND
GND	GND	AA16	GND
GND	GND	AB1	GND
GND	GND	AB22	GND
GND	GND	B7	GND
GND	GND	B12	GND
GND	GND	B16	GND
GND	GND	C3	GND
GND	GND	C20	GND
GND	GND	D8	GND
GND	GND	D11	GND
GND	GND	D16	GND
GND	GND	F6	GND
GND	GND	F17	GND
GND	GND	G2	GND
GND	GND	G4	GND
GND	GND	G9	GND
GND	GND	G11	GND
GND	GND	G13	GND
GND	GND	G15	GND
GND	GND	G21	GND
GND	GND	H7	GND
GND	GND	H8	GND
GND	GND	H10	GND
GND	GND	H12	GND
GND	GND	H14	GND
GND	GND	H16	GND

Table 63: **Spartan-3A DSP CS484 Pinout *(Cont'd)***

Bank	Pin Name	CS484 Ball	Type
GND	GND	H19	GND
GND	GND	J9	GND
GND	GND	J11	GND
GND	GND	J13	GND
GND	GND	J15	GND
GND	GND	K8	GND
GND	GND	K10	GND
GND	GND	K12	GND
GND	GND	K14	GND
GND	GND	L2	GND
GND	GND	L7	GND
GND	GND	L9	GND
GND	GND	L11	GND
GND	GND	L13	GND
GND	GND	L15	GND
GND	GND	L19	GND
GND	GND	M4	GND
GND	GND	M8	GND
GND	GND	M10	GND
GND	GND	M12	GND
GND	GND	M14	GND
GND	GND	M16	GND
GND	GND	M21	GND
GND	GND	N9	GND
GND	GND	N11	GND
GND	GND	N13	GND
GND	GND	N15	GND
GND	GND	P8	GND
GND	GND	P10	GND
GND	GND	P12	GND
GND	GND	P14	GND
GND	GND	R4	GND
GND	GND	R7	GND
GND	GND	R9	GND
GND	GND	R11	GND
GND	GND	R13	GND
GND	GND	R15	GND
GND	GND	R16	GND
GND	GND	T2	GND
GND	GND	T8	GND
GND	GND	T10	GND
GND	GND	T12	GND

Table 63: **Spartan-3A DSP CS484 Pinout *(Cont'd)***

Bank	Pin Name	CS484 Ball	Type
GND	GND	T14	GND
GND	GND	T15	GND
GND	GND	T19	GND
GND	GND	T21	GND
GND	GND	U6	GND
GND	GND	U11	GND
GND	GND	U17	GND
GND	GND	W7	GND
GND	GND	W12	GND
GND	GND	W16	GND
GND	GND	Y3	GND
GND	GND	Y20	GND
VCCAUX	SUSPEND	V19	PWRMGMT
VCCAUX	PROG_B	A2	CONFIG
VCCAUX	DONE	AB21	CONFIG
VCCAUX	TCK	A21	JTAG
VCCAUX	TMS	B1	JTAG
VCCAUX	TDO	B22	JTAG
VCCAUX	TDI	D2	JTAG
VCCAUX	VCCAUX	AA2	VCCAUX
VCCAUX	VCCAUX	AA21	VCCAUX
VCCAUX	VCCAUX	B2	VCCAUX
VCCAUX	VCCAUX	B21	VCCAUX
VCCAUX	VCCAUX	D12	VCCAUX
VCCAUX	VCCAUX	E5	VCCAUX
VCCAUX	VCCAUX	E18	VCCAUX
VCCAUX	VCCAUX	G10	VCCAUX
VCCAUX	VCCAUX	G12	VCCAUX
VCCAUX	VCCAUX	G14	VCCAUX
VCCAUX	VCCAUX	J16	VCCAUX
VCCAUX	VCCAUX	K7	VCCAUX
VCCAUX	VCCAUX	L4	VCCAUX
VCCAUX	VCCAUX	L16	VCCAUX
VCCAUX	VCCAUX	M7	VCCAUX
VCCAUX	VCCAUX	M19	VCCAUX
VCCAUX	VCCAUX	N16	VCCAUX
VCCAUX	VCCAUX	P7	VCCAUX
VCCAUX	VCCAUX	T9	VCCAUX
VCCAUX	VCCAUX	T11	VCCAUX
VCCAUX	VCCAUX	T13	VCCAUX
VCCAUX	VCCAUX	V5	VCCAUX
VCCAUX	VCCAUX	V18	VCCAUX

Table 63: **Spartan-3A DSP CS484 Pinout *(Cont'd)***

Bank	Pin Name	CS484 Ball	Type
VCCAUX	VCCAUX	W11	VCCAUX
VCCINT	VCCINT	G7	VCCINT
VCCINT	VCCINT	G16	VCCINT
VCCINT	VCCINT	H9	VCCINT
VCCINT	VCCINT	H11	VCCINT
VCCINT	VCCINT	H13	VCCINT
VCCINT	VCCINT	H15	VCCINT
VCCINT	VCCINT	J8	VCCINT
VCCINT	VCCINT	J10	VCCINT
VCCINT	VCCINT	J12	VCCINT
VCCINT	VCCINT	J14	VCCINT
VCCINT	VCCINT	K9	VCCINT
VCCINT	VCCINT	K11	VCCINT
VCCINT	VCCINT	K13	VCCINT
VCCINT	VCCINT	K15	VCCINT
VCCINT	VCCINT	L8	VCCINT
VCCINT	VCCINT	L10	VCCINT
VCCINT	VCCINT	L12	VCCINT
VCCINT	VCCINT	L14	VCCINT
VCCINT	VCCINT	M9	VCCINT
VCCINT	VCCINT	M11	VCCINT
VCCINT	VCCINT	M13	VCCINT
VCCINT	VCCINT	M15	VCCINT
VCCINT	VCCINT	N8	VCCINT
VCCINT	VCCINT	N10	VCCINT
VCCINT	VCCINT	N12	VCCINT
VCCINT	VCCINT	N14	VCCINT
VCCINT	VCCINT	P9	VCCINT
VCCINT	VCCINT	P11	VCCINT
VCCINT	VCCINT	P13	VCCINT
VCCINT	VCCINT	P15	VCCINT
VCCINT	VCCINT	R8	VCCINT
VCCINT	VCCINT	R10	VCCINT
VCCINT	VCCINT	R12	VCCINT
VCCINT	VCCINT	R14	VCCINT
VCCINT	VCCINT	T7	VCCINT
VCCINT	VCCINT	T16	VCCINT

User I/Os by Bank

Table 64 and Table 65 indicates how the user-I/O pins are distributed between the four I/O banks on the CS484 package. The AWAKE pin is counted as a dual-purpose I/O.

Table 64: **User I/Os Per Bank for the XC3SD1800A in the CS484 Package**

Package Edge	I/O Bank	Maximum I/Os and Input-Only	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF[1]	CLK
Top	0	77	49	13	1	6	8
Right	1	78	23	9	30	8	8
Bottom	2	76	33	6	21	8	8
Left	3	78	51	13	0	6	8
TOTAL		**309**	**156**	**41**	**52**	**28**	**32**

Notes:

1. 19 VREF are on INPUT pins.

Table 65: **User I/Os Per Bank for the XC3SD3400A in the CS484 Package**

Package Edge	I/O Bank	Maximum I/O and Input-Only	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF[1]	CLK
Top	0	77	49	13	1	6	8
Right	1	78	23	9	30	8	8
Bottom	2	76	33	6	21	8	8
Left	3	78	51	13	0	6	8
TOTAL		**309**	**156**	**41**	**52**	**28**	**32**

Notes:

1. 19 VREF are on INPUT pins.

Footprint Migration Differences

There are no migration footprint differences between the XC3SD1800A and the XC3SD3400A in the CS484 package.

CS484 Footprint

Left Half of Package (Top View)

156 **I/O:** Unrestricted, general-purpose user I/O.

41 **INPUT:** Unrestricted, general-purpose input pin.

51 **DUAL:** Configuration pins, then possible user I/O.

28 **VREF:** User I/O or input voltage reference for bank.

32 **CLK:** User I/O, input, or clock buffer input.

2 **CONFIG:** Dedicated configuration pins.

2 **SUSPEND:** Dedicated SUSPEND and dual-purpose AWAKE Power Management pins.

4 **JTAG:** Dedicated JTAG port pins.

84 **GND:** Ground.

24 **VCCO:** Output voltage supply for bank.

36 **VCCINT:** Internal core supply voltage (+1.2V).

24 **VCCAUX:** Auxiliary supply voltage

Bank 0

	1	2	3	4	5	6	7	8	9	10	11
A	GND	PROG_B	I/O L30N_0	I/O L28N_0	I/O L25N_0	I/O L25P_0	I/O L24N_0 VREF_0	I/O L20P_0 GCLK10	I/O L18P_0 GCLK6	INPUT	I/O L15N_0
B	TMS	VCCAUX	I/O L30P_0	I/O L28P_0	VCCO_0	I/O L24P_0	GND	I/O L20N_0 GCLK11	I/O L18N_0 GCLK7	VCCO_0	I/O L15P_0
C	I/O L02N_3	I/O L02P_3	GND	I/O L29N_0	INPUT	I/O L21P_0	I/O L26P_0	I/O L22P_0	I/O L16P_0	INPUT	INPUT 0 VREF_0
D	INPUT L04P_3	TDI	INPUT L08P_3	INPUT L08N_3	I/O L29P_0	I/O L21N_0	I/O L26N_0	GND	I/O L22N_0	I/O L16N_0	GND
E	INPUT L04N_3 VREF_3	VCCO_3	I/O L09P_3	I/O L09N_3	VCCAUX	INPUT	I/O L31P_0 VREF_0	I/O L27N_0	VCCO_0	INPUT	I/O L19N_0 GCLK9
F	I/O L06N_3	I/O L06P_3	I/O L01P_3	I/O L03P_3	I/O L03N_3	GND	I/O L31N_0 PUDC_B	I/O L27P_0	I/O L23N_0	I/O L19P_0 GCLK8	I/O L17N_0 GCLK5
G	I/O L11P_3	GND	I/O L01N_3	GND	I/O L07P_3	I/O L07N_3	VCCINT	I/O L23P_0	GND	VCCAUX	GND
H	I/O L11N_3	I/O L14P_3	I/O L05P_3	I/O L05N_3	I/O L10P_3	I/O L10N_3	GND	GND	VCCINT	GND	VCCINT
J	I/O L14N_3 VREF_3	VCCO_3	INPUT L16P_3	INPUT L16N_3	VCCO_3	INPUT L12P_3	INPUT L12N_3 VREF_3	VCCINT	GND	VCCINT	GND
K	I/O L19P_3 LHCLK2	I/O L17P_3	I/O L17N_3	I/O L13P_3	I/O L13N_3	I/O L15P_3	VCCAUX	GND	VCCINT	GND	VCCINT
L	I/O L19N_3 IRDY2 LHCLK3	GND	I/O L20P_3 LHCLK4	VCCAUX	I/O L15N_3	I/O L18P_3 LHCLK0	GND	VCCINT	GND	VCCINT	GND
M	I/O L22P_3 VREF_3	I/O L20N_3 LHCLK5	INPUT L23P_3	GND	I/O L18N_3 LHCLK1	I/O L21P_3 TRDY2 LHCLK6	VCCAUX	GND	VCCINT	GND	VCCINT
N	I/O L22N_3	VCCO_3	INPUT L31P_3	INPUT L23N_3	I/O L24N_3	I/O L24P_3	I/O L21N_3 LHCLK7	VCCINT	GND	VCCINT	GND
P	I/O L25P_3	I/O L25N_3	INPUT L31N_3	I/O L32P_3 VREF_3	VCCO_3	I/O L26P_3	VCCAUX	GND	VCCINT	GND	VCCINT
R	I/O L28N_3	I/O L28P_3	I/O L34P_3	GND	I/O L32N_3	I/O L26N_3	GND	VCCINT	GND	VCCINT	GND
T	I/O L30P_3	GND	INPUT L27P_3	I/O L34N_3	I/O L29N_3	I/O L29P_3	VCCINT	GND	VCCAUX	GND	VCCAUX
U	I/O L30N_3	I/O L33P_3	INPUT L27N_3	I/O L38P_3	I/O L38N_3	GND	I/O L02N_2 CSO_B	I/O L11N_2	I/O L10N_2	I/O L14N_2 D4	GND
V	I/O L33N_3	VCCO_3	I/O L36N_3	I/O L36P_3	VCCAUX	I/O L02P_2 M2	I/O L11P_2	I/O L06N_2	VCCO_2	I/O L10P_2	I/O L14P_2 D5
W	I/O L35N_3	I/O L37N_3	I/O L37P_3	INPUT 2 VREF_2	I/O L03P_2	I/O L07N_2 VS2	GND	I/O L06P_2	INPUT 2 VREF_2	INPUT	VCCAUX
Y	I/O L35P_3	INPUT L39P_3	GND	I/O L03N_2	I/O L07P_2 RDWR_B	INPUT	INPUT	I/O L13P_2	I/O L13N_2	I/O L15N_2 GCLK13	I/O L15P_2 GCLK12
AA	INPUT L39N_3 VREF_3	VCCAUX	I/O L01P_2 M1	I/O L04N_2	VCCO_2	INPUT	GND	I/O L08N_2	VCCO_2	I/O L12N_2 D6	GND
AB	GND	INPUT 2 VREF_2	I/O L01N_2 M0	I/O L04P_2	I/O L05P_2	I/O L05N_2	I/O L08P_2	I/O L09P_2 VS1	I/O L09N_2 VS0	I/O L12P_2 D7	INPUT 2 VREF_2

Bank 3 (left) **Bank 2** (bottom)

Figure 15: **CS484 Package Footprint (Top View–Left Half)**

Right Half of CS484 Package (Top View)

Figure 16: CS484 Package Footprint (Top View–Right Half)

FG676: 676-Ball Fine-Pitch Ball Grid Array

The 676-ball fine-pitch ball grid array, FG676, supports both the XC3SD1800A and the XC3SD3400A FPGAs. There are multiple pinout differences between the two devices. For a list of differences and migration advice, see the Footprint Migration Differences section.

XC3SD1800A FPGA

Table 66 lists all the FG676 package pins for the XC3SD1800A FPGA. They are sorted by bank number and then by pin name. Pairs of pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type, as defined earlier.

Pinout Table

Note: The grayed boxes denote a difference between the XC3SD1800A and the XC3SD3400A devices.

Table 66: **Spartan-3A DSP FG676 Pinout for XC3SD1800A FPGA**

Bank	XC3SD1800A Pin Name	FG676 Ball	Type
0	IO_L43N_0	K11	I/O
0	IO_L39N_0	K12	I/O
0	IO_L25P_0/GCLK4	K14	GCLK
0	IO_L12N_0	K16	I/O
0	IP_0	J10	INPUT
0	IO_L43P_0	J11	I/O
0	IO_L39P_0	J12	I/O
0	IP_0	J13	INPUT
0	IO_L25N_0/GCLK5	J14	GCLK
0	IP_0	J15	INPUT
0	IO_L12P_0	J16	I/O
0	IP_0/VREF_0	J17	VREF
0	IO_L47N_0	H9	I/O
0	IO_L46N_0	H10	I/O
0	IO_L35N_0	H12	I/O
0	IP_0	H13	INPUT
0	IO_L16N_0	H15	I/O
0	IO_L08P_0	H17	I/O
0	IP_0	H18	INPUT
0	IO_L52N_0/PUDC_B	G8	DUAL
0	IO_L47P_0	G9	I/O
0	IO_L46P_0	G10	I/O
0	IP_0/VREF_0	G11	VREF
0	IO_L35P_0	G12	I/O
0	IO_L27N_0/GCLK9	G13	GCLK
0	IP_0	G14	INPUT
0	IO_L16P_0	G15	I/O
0	IO_L08N_0	G17	I/O

Table 66: **Spartan-3A DSP FG676 Pinout for XC3SD1800A FPGA *(Cont'd)***

Bank	XC3SD1800A Pin Name	FG676 Ball	Type
0	IO_L02P_0/VREF_0	G19	VREF
0	IO_L01P_0	G20	I/O
0	IO_L48P_0	F7	I/O
0	IO_L52P_0/VREF_0	F8	VREF
0	IO_L31N_0	F12	I/O
0	IO_L27P_0/GCLK8	F13	GCLK
0	IO_L24N_0	F14	I/O
0	IO_L20P_0	F15	I/O
0	IO_L13P_0	F17	I/O
0	IO_L02N_0	F19	I/O
0	IO_L01N_0	F20	I/O
0	IO_L48N_0	E7	I/O
0	IO_L37P_0	E10	I/O
0	IP_0	E11	INPUT
0	IO_L31P_0	E12	I/O
0	IO_L24P_0	E14	I/O
0	IO_L20N_0/VREF_0	E15	VREF
0	IO_L13N_0	E17	I/O
0	IP_0	E18	INPUT
0	IO_L10P_0	E21	I/O
0	IO_L44N_0	D6	I/O
0	IP_0/VREF_0	D7	VREF
0	IO_L40N_0	D8	I/O
0	IO_L37N_0	D9	I/O
0	IO_L34N_0	D10	I/O
0	IO_L32N_0/VREF_0	D11	VREF
0	IP_0	D12	INPUT
0	IO_L30P_0	D13	I/O

Table 66: **Spartan-3A DSP FG676 Pinout for XC3SD1800A FPGA *(Cont'd)***

Bank	XC3SD1800A Pin Name	FG676 Ball	Type
0	IP_0/VREF_0	D14	VREF
0	IO_L22P_0	D16	I/O
0	IO_L21P_0	D17	I/O
0	IO_L17P_0	D18	I/O
0	IO_L11P_0	D20	I/O
0	IO_L10N_0	D21	I/O
0	IO_L05P_0	D22	I/O
0	IO_L06P_0	D23	I/O
0	IO_L44P_0	C5	I/O
0	IO_L41N_0	C6	I/O
0	IO_L42N_0	C7	I/O
0	IO_L40P_0	C8	I/O
0	IO_L34P_0	C10	I/O
0	IO_L32P_0	C11	I/O
0	IO_L30N_0	C12	I/O
0	IO_L28N_0/GCLK11	C13	GCLK
0	IO_L22N_0	C15	I/O
0	IO_L21N_0	C16	I/O
0	IO_L19P_0	C17	I/O
0	IO_L17N_0	C18	I/O
0	IO_L11N_0	C20	I/O
0	IO_L09P_0	C21	I/O
0	IO_L05N_0	C22	I/O
0	IO_L06N_0	C23	I/O
0	IO_L51N_0	B3	I/O
0	IO_L45N_0	B4	I/O
0	IO_L41P_0	B6	I/O
0	IO_L42P_0	B7	I/O
0	IO_L38N_0	B8	I/O
0	IO_L36N_0	B9	I/O
0	IO_L33N_0	B10	I/O
0	IO_L29N_0	B12	I/O
0	IO_L28P_0/GCLK10	B13	GCLK
0	IO_L26P_0/GCLK6	B14	GCLK
0	IO_L23P_0	B15	I/O
0	IO_L19N_0	B17	I/O
0	IO_L18P_0	B18	I/O
0	IO_L15P_0	B19	I/O
0	IO_L14P_0/VREF_0	B20	VREF

Table 66: **Spartan-3A DSP FG676 Pinout for XC3SD1800A FPGA *(Cont'd)***

Bank	XC3SD1800A Pin Name	FG676 Ball	Type
0	IO_L09N_0	B21	I/O
0	IO_L07P_0	B23	I/O
0	IO_L51P_0	A3	I/O
0	IO_L45P_0	A4	I/O
0	IP_0	A7	INPUT
0	IO_L38P_0	A8	I/O
0	IO_L36P_0	A9	I/O
0	IO_L33P_0	A10	I/O
0	IO_L29P_0	A12	I/O
0	IP_0	A13	INPUT
0	IO_L26N_0/GCLK7	A14	GCLK
0	IO_L23N_0	A15	I/O
0	IP_0	A17	INPUT
0	IO_L18N_0	A18	I/O
0	IO_L15N_0	A19	I/O
0	IO_L14N_0	A20	I/O
0	IO_L07N_0	A22	I/O
0	IP_0	G16	INPUT
0	IP_0	E9	INPUT
0	IP_0	D15	INPUT
0	IP_0	D19	INPUT
0	IP_0	B24	INPUT
0	IP_0	A5	INPUT
0	IP_0	A23	INPUT
0	IP_0	F9	INPUT
0	IP_0	E20	INPUT
0	IP_0	A24	INPUT
0	IP_0	G18	INPUT
0	IP_0	F10	INPUT
0	IP_0	F18	INPUT
0	IP_0	E6	INPUT
0	IP_0	D5	INPUT
0	IP_0	C4	INPUT
0	VCCO_0	H11	VCCO
0	VCCO_0	H16	VCCO
0	VCCO_0	E8	VCCO
0	VCCO_0	E13	VCCO
0	VCCO_0	E19	VCCO
0	VCCO_0	B5	VCCO

Table 66: **Spartan-3A DSP FG676 Pinout for XC3SD1800A FPGA *(Cont'd)***

Bank	XC3SD1800A Pin Name	FG676 Ball	Type
0	VCCO_0	B11	VCCO
0	VCCO_0	B16	VCCO
0	VCCO_0	B22	VCCO
1	IO_L01P_1/HDC	Y20	DUAL
1	IO_L01N_1/LDC2	Y21	DUAL
1	IO_L13P_1	Y22	I/O
1	IO_L13N_1	Y23	I/O
1	IO_L15P_1	Y24	I/O
1	IO_L15N_1	Y25	I/O
1	IP_L16N_1	Y26	INPUT
1	IO_L04P_1	W20	I/O
1	IO_L04N_1	W21	I/O
1	IO_L18P_1	W23	I/O
1	IO_L08P_1	V18	I/O
1	IO_L08N_1	V19	I/O
1	IO_L10P_1	V21	I/O
1	IO_L18N_1	V22	I/O
1	IO_L21P_1	V23	I/O
1	IO_L19P_1	V24	I/O
1	IO_L19N_1	V25	I/O
1	IP_L20N_1/VREF_1	V26	VREF
1	IO_L12N_1	U18	I/O
1	IO_L12P_1	U19	I/O
1	IO_L10N_1	U20	I/O
1	IO_L14P_1	U21	I/O
1	IO_L21N_1	U22	I/O
1	IO_L23P_1	U23	I/O
1	IO_L23N_1/VREF_1	U24	VREF
1	IP_L24N_1/VREF_1	U26	VREF
1	IO_L17N_1	T17	I/O
1	IO_L17P_1	T18	I/O
1	IO_L14N_1	T20	I/O
1	IO_L26P_1/A4	T23	DUAL
1	IO_L26N_1/A5	T24	DUAL
1	IO_L27N_1/A7	R17	DUAL
1	IO_L27P_1/A6	R18	DUAL
1	IO_L22P_1	R19	I/O
1	IO_L22N_1	R20	I/O
1	IO_L25P_1/A2	R21	DUAL

Table 66: **Spartan-3A DSP FG676 Pinout for XC3SD1800A FPGA *(Cont'd)***

Bank	XC3SD1800A Pin Name	FG676 Ball	Type
1	IO_L25N_1/A3	R22	DUAL
1	IP_L28P_1/VREF_1	R23	VREF
1	IP_L28N_1	R24	INPUT
1	IO_L29P_1/A8	R25	DUAL
1	IO_L29N_1/A9	R26	DUAL
1	IO_L34P_1/IRDY1/RHCLK6	P18	RHCLK
1	IO_L30N_1/RHCLK1	P20	RHCLK
1	IO_L30P_1/RHCLK0	P21	RHCLK
1	IO_L37P_1	P22	I/O
1	IO_L33P_1/RHCLK4	P23	RHCLK
1	IO_L31N_1/TRDY1/RHCLK3	P25	RHCLK
1	IO_L31P_1/RHCLK2	P26	RHCLK
1	IO_L39N_1/A15	N17	DUAL
1	IO_L39P_1/A14	N18	DUAL
1	IO_L34N_1/RHCLK7	N19	RHCLK
1	IO_L42P_1/A16	N20	DUAL
1	IO_L37N_1	N21	I/O
1	IP_L36N_1	N23	INPUT
1	IO_L33N_1/RHCLK5	N24	RHCLK
1	IP_L32N_1	N25	INPUT
1	IP_L32P_1	N26	INPUT
1	IO_L47N_1	M18	I/O
1	IO_L47P_1	M19	I/O
1	IO_L42N_1/A17	M20	DUAL
1	IO_L45P_1	M21	I/O
1	IO_L45N_1	M22	I/O
1	IO_L38N_1/A13	M23	DUAL
1	IP_L36P_1/VREF_1	M24	VREF
1	IO_L35N_1/A11	M25	DUAL
1	IO_L35P_1/A10	M26	DUAL
1	IO_L55N_1	L17	I/O
1	IO_L55P_1	L18	I/O
1	IO_L53P_1	L20	I/O
1	IO_L50P_1	L22	I/O
1	IP_L40N_1	L23	INPUT
1	IO_L38P_1/A12	L24	DUAL
1	IO_L57N_1	K18	I/O
1	IO_L57P_1	K19	I/O
1	IO_L53N_1	K20	I/O

Table 66: **Spartan-3A DSP FG676 Pinout for XC3SD1800A FPGA *(Cont'd)***

Bank	XC3SD1800A Pin Name	FG676 Ball	Type
1	IO_L50N_1	K21	I/O
1	IO_L46N_1	K22	I/O
1	IO_L46P_1	K23	I/O
1	IP_L40P_1	K24	INPUT
1	IO_L41P_1	K25	I/O
1	IO_L41N_1	K26	I/O
1	IO_L59P_1	J19	I/O
1	IO_L59N_1	J20	I/O
1	IO_L62P_1/A20	J21	DUAL
1	IO_L49N_1	J22	I/O
1	IO_L49P_1	J23	I/O
1	IO_L43N_1/A19	J25	DUAL
1	IO_L43P_1/A18	J26	DUAL
1	IO_L64P_1/A24	H20	DUAL
1	IO_L62N_1/A21	H21	DUAL
1	IP_L48N_1	H24	INPUT
1	IP_L44N_1	H25	INPUT
1	IP_L44P_1/VREF_1	H26	VREF
1	IO_L64N_1/A25	G21	DUAL
1	IO_L58N_1	G22	I/O
1	IO_L51P_1	G23	I/O
1	IO_L51N_1	G24	I/O
1	IP_L52N_1/VREF_1	G25	VREF
1	IO_L58P_1/VREF_1	F22	VREF
1	IO_L56N_1	F23	I/O
1	IO_L54N_1	F24	I/O
1	IO_L54P_1	F25	I/O
1	IO_L56P_1	E24	I/O
1	IO_L60P_1	E26	I/O
1	IO_L61N_1	D24	I/O
1	IO_L61P_1	D25	I/O
1	IO_L60N_1	D26	I/O
1	IO_L63N_1/A23	C25	DUAL
1	IO_L63P_1/A22	C26	DUAL
1	IP_L65P_1/VREF_1	B26	VREF
1	IO_L02P_1/LDC1	AE26	DUAL
1	IO_L02N_1/LDC0	AD25	DUAL
1	IO_L05P_1	AD26	I/O
1	IO_L03P_1/A0	AC23	DUAL

Table 66: **Spartan-3A DSP FG676 Pinout for XC3SD1800A FPGA *(Cont'd)***

Bank	XC3SD1800A Pin Name	FG676 Ball	Type
1	IO_L03N_1/A1	AC24	DUAL
1	IO_L05N_1	AC25	I/O
1	IO_L06P_1	AC26	I/O
1	IO_L07P_1	AB23	I/O
1	IO_L07N_1/VREF_1	AB24	VREF
1	IO_L06N_1	AB26	I/O
1	IO_L09P_1	AA22	I/O
1	IO_L09N_1	AA23	I/O
1	IO_L11P_1	AA24	I/O
1	IO_L11N_1	AA25	I/O
1	IP_L16P_1	W25	INPUT
1	IP_L24P_1	U25	INPUT
1	IP_L65N_1	B25	INPUT
1	IP_L20P_1	W26	INPUT
1	IP_L48P_1	H23	INPUT
1	IP_L52P_1	G26	INPUT
1	VCCO_1	W22	VCCO
1	VCCO_1	T19	VCCO
1	VCCO_1	T25	VCCO
1	VCCO_1	N22	VCCO
1	VCCO_1	L19	VCCO
1	VCCO_1	L25	VCCO
1	VCCO_1	H22	VCCO
1	VCCO_1	E25	VCCO
1	VCCO_1	AB25	VCCO
2	IO_L02P_2/M2	Y7	DUAL
2	IO_L05N_2	Y9	I/O
2	IO_L12P_2	Y10	I/O
2	IO_L17P_2/RDWR_B	Y12	DUAL
2	IO_L25N_2/GCLK13	Y13	GCLK
2	IO_L27P_2/GCLK0	Y14	GCLK
2	IO_L34N_2/D3	Y15	DUAL
2	IP_2/VREF_2	Y16	VREF
2	IO_L43N_2	Y17	I/O
2	IO_L05P_2	W9	I/O
2	IO_L09N_2	W10	I/O
2	IO_L16N_2	W12	I/O
2	IO_L20N_2	W13	I/O
2	IO_L31N_2	W15	I/O

Table 66: **Spartan-3A DSP FG676 Pinout for XC3SD1800A FPGA *(Cont'd)***

Bank	XC3SD1800A Pin Name	FG676 Ball	Type
2	IO_L46P_2	W17	I/O
2	IO_L09P_2	V10	I/O
2	IO_L13P_2	V11	I/O
2	IO_L16P_2	V12	I/O
2	IO_L20P_2	V13	I/O
2	IO_L31P_2	V14	I/O
2	IO_L35P_2	V15	I/O
2	IO_L42P_2	V16	I/O
2	IO_L46N_2	V17	I/O
2	IO_L13N_2	U11	I/O
2	IO_L35N_2	U15	I/O
2	IO_L42N_2	U16	I/O
2	IO_L06N_2	AF3	I/O
2	IO_L07N_2	AF4	I/O
2	IO_L10P_2	AF5	I/O
2	IP_2	AF7	INPUT
2	IO_L18N_2	AF8	I/O
2	IO_L19N_2/VS0	AF9	DUAL
2	IO_L22N_2/D6	AF10	DUAL
2	IO_L24P_2/D5	AF12	DUAL
2	IO_L26P_2/GCLK14	AF13	GCLK
2	IO_L28P_2/GCLK2	AF14	GCLK
2	IP_2/VREF_2	AF15	VREF
2	IP_2/VREF_2	AF17	VREF
2	IO_L36P_2/D2	AF18	DUAL
2	IO_L37P_2	AF19	I/O
2	IO_L39P_2	AF20	I/O
2	IP_2/VREF_2	AF22	VREF
2	IO_L48P_2	AF23	I/O
2	IO_L52P_2/D0/DIN/MISO	AF24	DUAL
2	IO_L51P_2	AF25	I/O
2	IO_L06P_2	AE3	I/O
2	IO_L07P_2	AE4	I/O
2	IO_L10N_2	AE6	I/O
2	IO_L11N_2	AE7	I/O
2	IO_L18P_2	AE8	I/O
2	IO_L19P_2/VS1	AE9	DUAL
2	IO_L22P_2/D7	AE10	DUAL
2	IO_L24N_2/D4	AE12	DUAL

Table 66: **Spartan-3A DSP FG676 Pinout for XC3SD1800A FPGA *(Cont'd)***

Bank	XC3SD1800A Pin Name	FG676 Ball	Type
2	IO_L26N_2/GCLK15	AE13	GCLK
2	IO_L28N_2/GCLK3	AE14	GCLK
2	IO_L32N_2/DOUT	AE15	DUAL
2	IO_L33P_2	AE17	I/O
2	IO_L36N_2/D1	AE18	DUAL
2	IO_L37N_2	AE19	I/O
2	IO_L39N_2	AE20	I/O
2	IO_L44P_2	AE21	I/O
2	IO_L48N_2	AE23	I/O
2	IO_L52N_2/CCLK	AE24	DUAL
2	IO_L51N_2	AE25	I/O
2	IO_L01N_2/M0	AD4	DUAL
2	IO_L08N_2	AD6	I/O
2	IO_L11P_2	AD7	I/O
2	IP_2	AD9	INPUT
2	IP_2	AD10	INPUT
2	IO_L23P_2	AD11	I/O
2	IP_2/VREF_2	AD12	VREF
2	IO_L29P_2	AD14	I/O
2	IO_L32P_2/AWAKE	AD15	PWRMGMT
2	IP_2	AD16	INPUT
2	IO_L33N_2	AD17	I/O
2	IO_L40P_2	AD19	I/O
2	IO_L41P_2	AD20	I/O
2	IO_L44N_2	AD21	I/O
2	IO_L45P_2	AD22	I/O
2	IO_L01P_2/M1	AC4	DUAL
2	IO_L08P_2	AC6	I/O
2	IO_L14P_2	AC8	I/O
2	IO_L15N_2	AC9	I/O
2	IP_2/VREF_2	AC10	VREF
2	IO_L23N_2	AC11	I/O
2	IO_L21N_2	AC12	I/O
2	IP_2	AC13	INPUT
2	IO_L29N_2	AC14	I/O
2	IO_L30P_2	AC15	I/O
2	IO_L38P_2	AC16	I/O
2	IP_2	AC17	INPUT
2	IO_L40N_2	AC19	I/O

Table 66: **Spartan-3A DSP FG676 Pinout for XC3SD1800A FPGA *(Cont'd)***

Bank	XC3SD1800A Pin Name	FG676 Ball	Type
2	IO_L41N_2	AC20	I/O
2	IO_L45N_2	AC21	I/O
2	IO_2	AC22	I/O
2	IP_2/VREF_2	AB6	VREF
2	IO_L14N_2	AB7	I/O
2	IO_L15P_2	AB9	I/O
2	IO_L21P_2	AB12	I/O
2	IP_2	AB13	INPUT
2	IO_L30N_2/MOSI/CSI_B	AB15	DUAL
2	IO_L38N_2	AB16	I/O
2	IO_L47P_2	AB18	I/O
2	IO_L02N_2/CSO_B	AA7	DUAL
2	IP_2/VREF_2	AA9	VREF
2	IO_L12N_2	AA10	I/O
2	IO_L17N_2/VS2	AA12	DUAL
2	IO_L25P_2/GCLK12	AA13	GCLK
2	IO_L27N_2/GCLK1	AA14	GCLK
2	IO_L34P_2/INIT_B	AA15	DUAL
2	IO_L43P_2	AA17	I/O
2	IO_L47N_2	AA18	I/O
2	IP_2/VREF_2	AA20	VREF
2	IP_2	AD5	INPUT
2	IP_2	AD23	INPUT
2	IP_2	AC5	INPUT
2	IP_2	AC7	INPUT
2	IP_2	AC18	INPUT
2	IP_2/VREF_2	AB10	VREF
2	IP_2	AB20	INPUT
2	IP_2	AA19	INPUT
2	IP_2	AF2	INPUT
2	IP_2	AB17	INPUT
2	IP_2	Y8	INPUT
2	IP_2	Y11	INPUT
2	IP_2	Y18	INPUT
2	IP_2/VREF_2	Y19	VREF
2	IP_2	W18	INPUT
2	IP_2	AA8	INPUT
2	VCCO_2	W11	VCCO
2	VCCO_2	W16	VCCO

Table 66: **Spartan-3A DSP FG676 Pinout for XC3SD1800A FPGA *(Cont'd)***

Bank	XC3SD1800A Pin Name	FG676 Ball	Type
2	VCCO_2	AE5	VCCO
2	VCCO_2	AE11	VCCO
2	VCCO_2	AE16	VCCO
2	VCCO_2	AE22	VCCO
2	VCCO_2	AB8	VCCO
2	VCCO_2	AB14	VCCO
2	VCCO_2	AB19	VCCO
3	IO_L53P_3	Y1	I/O
3	IO_L53N_3	Y2	I/O
3	IP_L54P_3	Y3	INPUT
3	IO_L57P_3	Y5	I/O
3	IO_L57N_3	Y6	I/O
3	IP_L50P_3	W1	INPUT
3	IP_L50N_3/VREF_3	W2	VREF
3	IO_L52P_3	W3	I/O
3	IO_L52N_3	W4	I/O
3	IO_L63N_3	W6	I/O
3	IO_L63P_3	W7	I/O
3	IO_L47P_3	V1	I/O
3	IO_L47N_3	V2	I/O
3	IP_L46N_3	V4	INPUT
3	IO_L49N_3	V5	I/O
3	IO_L59N_3	V6	I/O
3	IO_L59P_3	V7	I/O
3	IO_L61N_3	V8	I/O
3	IO_L44P_3	U1	I/O
3	IO_L44N_3	U2	I/O
3	IP_L46P_3	U3	INPUT
3	IO_L42N_3	U4	I/O
3	IO_L49P_3	U5	I/O
3	IO_L51N_3	U6	I/O
3	IO_L56P_3	U7	I/O
3	IO_L56N_3	U8	I/O
3	IO_L61P_3	U9	I/O
3	IO_L38P_3	T3	I/O
3	IO_L38N_3	T4	I/O
3	IO_L42P_3	T5	I/O
3	IO_L51P_3	T7	I/O
3	IO_L48N_3	T9	I/O

Table 66: **Spartan-3A DSP FG676 Pinout for XC3SD1800A FPGA *(Cont'd)***

Bank	XC3SD1800A Pin Name	FG676 Ball	Type
3	IO_L48P_3	T10	I/O
3	IO_L36P_3/VREF_3	R1	VREF
3	IO_L36N_3	R2	I/O
3	IO_L37P_3	R3	I/O
3	IO_L37N_3	R4	I/O
3	IO_L40P_3	R5	I/O
3	IO_L40N_3	R6	I/O
3	IO_L45N_3	R7	I/O
3	IO_L45P_3	R8	I/O
3	IO_L43N_3	R9	I/O
3	IO_L43P_3/VREF_3	R10	VREF
3	IO_L33P_3/LHCLK2	P1	LHCLK
3	IO_L33N_3/IRDY2/LHCLK3	P2	LHCLK
3	IO_L34N_3/LHCLK5	P3	LHCLK
3	IO_L34P_3/LHCLK4	P4	LHCLK
3	IO_L39N_3	P6	I/O
3	IO_L39P_3	P7	I/O
3	IO_L41P_3	P8	I/O
3	IO_L41N_3	P9	I/O
3	IO_L35N_3/LHCLK7	P10	LHCLK
3	IO_L31P_3	N1	I/O
3	IO_L31N_3	N2	I/O
3	IO_L30N_3	N4	I/O
3	IO_L30P_3	N5	I/O
3	IO_L32P_3/LHCLK0	N6	LHCLK
3	IO_L32N_3/LHCLK1	N7	LHCLK
3	IO_L35P_3/TRDY2/LHCLK6	N9	LHCLK
3	IO_L29N_3/VREF_3	M1	VREF
3	IO_L29P_3	M2	I/O
3	IO_L27N_3	M3	I/O
3	IO_L27P_3	M4	I/O
3	IO_L28P_3	M5	I/O
3	IO_L28N_3	M6	I/O
3	IO_L26N_3	M7	I/O
3	IO_L26P_3	M8	I/O
3	IO_L21N_3	M9	I/O
3	IO_L21P_3	M10	I/O
3	IO_L25N_3	L3	I/O
3	IO_L25P_3	L4	I/O

Table 66: **Spartan-3A DSP FG676 Pinout for XC3SD1800A FPGA *(Cont'd)***

Bank	XC3SD1800A Pin Name	FG676 Ball	Type
3	IO_L18N_3	L7	I/O
3	IO_L15N_3	L9	I/O
3	IO_L15P_3	L10	I/O
3	IP_L24N_3	K1	INPUT
3	IO_L23N_3	K2	I/O
3	IO_L23P_3	K3	I/O
3	IO_L22N_3	K4	I/O
3	IO_L22P_3	K5	I/O
3	IO_L18P_3	K6	I/O
3	IO_L13P_3	K7	I/O
3	IO_L05N_3	K8	I/O
3	IO_L05P_3	K9	I/O
3	IP_L24P_3	J1	INPUT
3	IP_L20N_3/VREF_3	J2	VREF
3	IP_L20P_3	J3	INPUT
3	IO_L19N_3	J4	I/O
3	IO_L19P_3	J5	I/O
3	IO_L13N_3	J6	I/O
3	IO_L10P_3	J7	I/O
3	IO_L01P_3	J8	I/O
3	IO_L01N_3	J9	I/O
3	IO_L17N_3	H1	I/O
3	IO_L17P_3	H2	I/O
3	IP_L12N_3/VREF_3	H4	VREF
3	IO_L10N_3	H6	I/O
3	IO_L03N_3	H7	I/O
3	IP_L16N_3	G1	INPUT
3	IO_L14P_3	G3	I/O
3	IO_L09N_3	G4	I/O
3	IO_L03P_3	G6	I/O
3	IO_L11N_3	F2	I/O
3	IO_L14N_3	F3	I/O
3	IO_L07N_3	F4	I/O
3	IO_L09P_3	F5	I/O
3	IO_L11P_3	E1	I/O
3	IO_L07P_3	E3	I/O
3	IO_L06N_3	E4	I/O
3	IO_L06P_3	D3	I/O
3	IP_L04N_3/VREF_3	C1	VREF

Table 66: **Spartan-3A DSP FG676 Pinout for XC3SD1800A FPGA *(Cont'd)***

Bank	XC3SD1800A Pin Name	FG676 Ball	Type
3	IP_L04P_3	C2	INPUT
3	IO_L02N_3	B1	I/O
3	IO_L02P_3	B2	I/O
3	IP_L66P_3	AE1	INPUT
3	IP_L66N_3/VREF_3	AE2	VREF
3	IO_L65P_3	AD1	I/O
3	IO_L65N_3	AD2	I/O
3	IO_L60N_3	AC1	I/O
3	IO_L64P_3	AC2	I/O
3	IO_L64N_3	AC3	I/O
3	IO_L60P_3	AB1	I/O
3	IO_L55P_3	AA2	I/O
3	IO_L55N_3	AA3	I/O
3	IP_L58N_3/VREF_3	AA5	VREF
3	IP_L16P_3	G2	INPUT
3	IP_L12P_3	G5	INPUT
3	IP_L08P_3	D2	INPUT
3	IP_L62P_3	AB3	INPUT
3	IP_L58P_3	AA4	INPUT
3	IP_L08N_3	D1	INPUT
3	IP_L62N_3	AB4	INPUT
3	IP_L54N_3	Y4	INPUT
3	VCCO_3	W5	VCCO
3	VCCO_3	T2	VCCO
3	VCCO_3	T8	VCCO
3	VCCO_3	P5	VCCO
3	VCCO_3	L2	VCCO
3	VCCO_3	L8	VCCO
3	VCCO_3	H5	VCCO
3	VCCO_3	E2	VCCO
3	VCCO_3	AB2	VCCO
GND	GND	W8	GND
GND	GND	W14	GND
GND	GND	W19	GND
GND	GND	W24	GND
GND	GND	V3	GND
GND	GND	U10	GND
GND	GND	U13	GND
GND	GND	U17	GND

Table 66: **Spartan-3A DSP FG676 Pinout for XC3SD1800A FPGA *(Cont'd)***

Bank	XC3SD1800A Pin Name	FG676 Ball	Type
GND	GND	T1	GND
GND	GND	T6	GND
GND	GND	T12	GND
GND	GND	T14	GND
GND	GND	T16	GND
GND	GND	T21	GND
GND	GND	T26	GND
GND	GND	R11	GND
GND	GND	R13	GND
GND	GND	R15	GND
GND	GND	P12	GND
GND	GND	P16	GND
GND	GND	P19	GND
GND	GND	P24	GND
GND	GND	N3	GND
GND	GND	N8	GND
GND	GND	N11	GND
GND	GND	N15	GND
GND	GND	M12	GND
GND	GND	M14	GND
GND	GND	M16	GND
GND	GND	L1	GND
GND	GND	L6	GND
GND	GND	L11	GND
GND	GND	L13	GND
GND	GND	L15	GND
GND	GND	L21	GND
GND	GND	L26	GND
GND	GND	K10	GND
GND	GND	K17	GND
GND	GND	J24	GND
GND	GND	H3	GND
GND	GND	H8	GND
GND	GND	H14	GND
GND	GND	H19	GND
GND	GND	F1	GND
GND	GND	F6	GND
GND	GND	F11	GND
GND	GND	F16	GND

Table 66: **Spartan-3A DSP FG676 Pinout for XC3SD1800A FPGA *(Cont'd)***

Bank	XC3SD1800A Pin Name	FG676 Ball	Type
GND	GND	F21	GND
GND	GND	F26	GND
GND	GND	C3	GND
GND	GND	C9	GND
GND	GND	C14	GND
GND	GND	C19	GND
GND	GND	C24	GND
GND	GND	AF1	GND
GND	GND	AF6	GND
GND	GND	AF11	GND
GND	GND	AF16	GND
GND	GND	AF21	GND
GND	GND	AF26	GND
GND	GND	AD3	GND
GND	GND	AD8	GND
GND	GND	AD13	GND
GND	GND	AD18	GND
GND	GND	AD24	GND
GND	GND	AA1	GND
GND	GND	AA6	GND
GND	GND	AA11	GND
GND	GND	AA16	GND
GND	GND	AA21	GND
GND	GND	AA26	GND
GND	GND	A1	GND
GND	GND	A6	GND
GND	GND	A11	GND
GND	GND	A16	GND
GND	GND	A21	GND
GND	GND	A26	GND
VCCAUX	SUSPEND	V20	PWRMGMT
VCCAUX	DONE	AB21	CONFIG
VCCAUX	PROG_B	A2	CONFIG
VCCAUX	TDI	G7	JTAG
VCCAUX	TDO	E23	JTAG
VCCAUX	TMS	D4	JTAG
VCCAUX	TCK	A25	JTAG
VCCAUX	VCCAUX	V9	VCCAUX
VCCAUX	VCCAUX	U14	VCCAUX

Table 66: **Spartan-3A DSP FG676 Pinout for XC3SD1800A FPGA *(Cont'd)***

Bank	XC3SD1800A Pin Name	FG676 Ball	Type
VCCAUX	VCCAUX	T22	VCCAUX
VCCAUX	VCCAUX	P17	VCCAUX
VCCAUX	VCCAUX	N10	VCCAUX
VCCAUX	VCCAUX	L5	VCCAUX
VCCAUX	VCCAUX	K13	VCCAUX
VCCAUX	VCCAUX	J18	VCCAUX
VCCAUX	VCCAUX	E5	VCCAUX
VCCAUX	VCCAUX	E16	VCCAUX
VCCAUX	VCCAUX	E22	VCCAUX
VCCAUX	VCCAUX	AB5	VCCAUX
VCCAUX	VCCAUX	AB11	VCCAUX
VCCAUX	VCCAUX	AB22	VCCAUX
VCCINT	VCCINT	U12	VCCINT
VCCINT	VCCINT	T11	VCCINT
VCCINT	VCCINT	T13	VCCINT
VCCINT	VCCINT	T15	VCCINT
VCCINT	VCCINT	R12	VCCINT
VCCINT	VCCINT	R14	VCCINT
VCCINT	VCCINT	R16	VCCINT
VCCINT	VCCINT	P11	VCCINT
VCCINT	VCCINT	P13	VCCINT
VCCINT	VCCINT	P14	VCCINT
VCCINT	VCCINT	P15	VCCINT
VCCINT	VCCINT	N12	VCCINT
VCCINT	VCCINT	N13	VCCINT
VCCINT	VCCINT	N14	VCCINT
VCCINT	VCCINT	N16	VCCINT
VCCINT	VCCINT	M11	VCCINT
VCCINT	VCCINT	M13	VCCINT
VCCINT	VCCINT	M15	VCCINT
VCCINT	VCCINT	M17	VCCINT
VCCINT	VCCINT	L12	VCCINT
VCCINT	VCCINT	L14	VCCINT
VCCINT	VCCINT	L16	VCCINT
VCCINT	VCCINT	K15	VCCINT

User I/Os by Bank

Table 67 indicates how the available user-I/O pins are distributed between the four I/O banks on the FG676 package. The AWAKE pin is counted as a dual-purpose I/O.

Table 67: **User I/Os Per Bank for the XC3SD1800A in the FG676 Package**

Package Edge	I/O Bank	Maximum I/Os and Input-Only	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF[1]	CLK
Top	0	128	82	28	1	9	8
Right	1	130	67	15	30	10	8
Bottom	2	129	68	21	21	11	8
Left	3	132	97	18	0	9	8
TOTAL		**519**	**314**	**82**	**52**	**39**	**32**

Notes:

1. 28 VREF are on INPUT pins.

FG676 Footprint – XC3SD1800A FPGA

Left Half of Package (Top View)

314 **I/O:** Unrestricted, general-purpose user I/O.

82 **INPUT:** Unrestricted, general-purpose input pin.

51 **DUAL:** Configuration pins, then possible user I/O.

39 **VREF:** User I/O or input voltage reference for bank.

32 **CLK:** User I/O, input, or clock buffer input.

2 **CONFIG:** Dedicated configuration pins.

4 **JTAG:** Dedicated JTAG port pins.

2 **SUSPEND:** Dedicated SUSPEND and dual-purpose AWAKE Power Management pins

77 **GND:** Ground

36 **VCCO:** Output voltage supply for bank.

23 **VCCINT:** Internal core supply voltage (+1.2V).

14 **VCCAUX:** Auxiliary supply voltage.

Note: The boxes with triangles inside indicate pin differences from the XC3SD3400A device. Please see the Footprint Migration Differences section for more information.

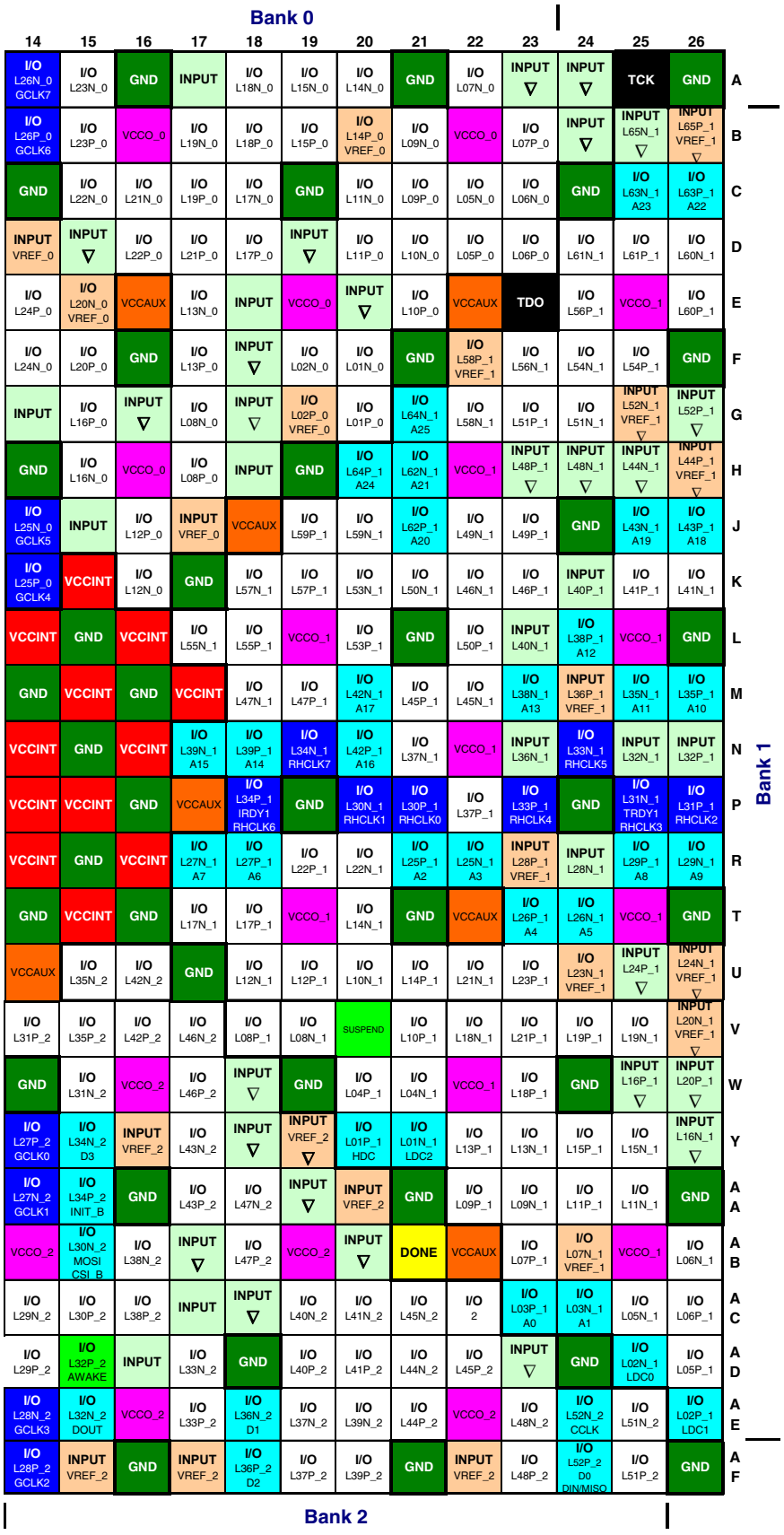
Bank 0

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	GND	PROG_B	I/O L51P_0	I/O L45P_0	INPUT ▽	GND	INPUT ▽	I/O L38P_0	I/O L36P_0	I/O L33P_0	GND	I/O L29P_0	INPUT
B	I/O L02N_3	I/O L02P_3	I/O L51N_0	I/O L45N_0	VCCO_0	I/O L41P_0	I/O L42P_0	I/O L38N_0	I/O L36N_0	I/O L33N_0	VCCO_0	I/O L29N_0	I/O L28P_0 GCLK10
C	INPUT L04N_3 VREF_3 ▽	INPUT L04P_3 ▽	GND	INPUT ▽	I/O L44P_0	I/O L41N_0	I/O L42N_0	I/O L40P_0	GND	I/O L34P_0	I/O L32P_0	I/O L30N_0	I/O L28N_0 GCLK11
D	INPUT L08N_3 ▽	INPUT L08P_3 ▽	I/O L06P_3	TMS	INPUT ▽	I/O L44N_0	INPUT VREF_0	I/O L40N_0	I/O L37N_0	I/O L34N_0	I/O L32N_0 VREF_0	INPUT	I/O L30P_0
E	I/O L11P_3	VCCO_3	I/O L07P_3	I/O L06N_3	VCCAUX	INPUT ▽	I/O L48N_0	VCCO_0	INPUT ▽	I/O L37P_0	INPUT	I/O L31P_0	VCCO_0
F	GND	I/O L11N_3	I/O L14N_3	I/O L07N_3	I/O L09P_3	GND	I/O L48P_0	I/O L52P_0 VREF_0	INPUT ▽	INPUT ▽	GND	I/O L31N_0	I/O L27P_0 GCLK8
G	INPUT L16N_3 ▽	INPUT L16P_3 ▽	I/O L14P_3	I/O L09N_3	INPUT L12P_3 ▽	I/O L03P_3	TDI	I/O L52N_0 PUDC_B	I/O L47P_0	I/O L46P_0	INPUT VREF_0	I/O L35P_0	I/O L27N_0 GCLK9
H	I/O L17N_3	I/O L17P_3	GND	INPUT L12N_3 VREF_3 ▽	VCCO_3	I/O L10N_3	I/O L03N_3	GND	I/O L47N_0	I/O L46N_0	VCCO_0	I/O L35N_0	INPUT
J	INPUT L24P_3	INPUT L20N_3 VREF_3	INPUT L20P_3	I/O L19N_3	I/O L19P_3	I/O L13N_3	I/O L10P_3	I/O L01P_3	I/O L01N_3	INPUT	I/O L43P_0	I/O L39P_0	INPUT
K	INPUT L24N_3	I/O L23N_3	I/O L23P_3	I/O L22N_3	I/O L22P_3	I/O L18P_3	I/O L13P_3	I/O L05N_3	I/O L05P_3	GND	I/O L43N_0	I/O L39N_0	VCCAUX
L	GND	VCCO_3	I/O L25N_3	I/O L25P_3	VCCAUX	GND	I/O L18N_3	VCCO_3	I/O L15N_3	I/O L15P_3	GND	VCCINT	GND
M	I/O L29N_3 VREF_3	I/O L29P_3	I/O L27N_3	I/O L27P_3	I/O L28P_3	I/O L28N_3	I/O L26N_3	I/O L26P_3	I/O L21N_3	I/O L21P_3	VCCINT	GND	VCCINT
N	I/O L31P_3	I/O L31N_3	GND	I/O L30N_3	I/O L30P_3	I/O L32P_3 LHCLK0	I/O L32N_3 LHCLK1	GND	I/O L35P_3 TRDY2 LHCLK6	VCCAUX	GND	VCCINT	VCCINT
P	I/O L33P_3 LHCLK2	I/O L33N_3 IRDY2 LHCLK3	I/O L34N_3 LHCLK5	I/O L34P_3 LHCLK4	VCCO_3	I/O L39N_3	I/O L39P_3	I/O L41P_3	I/O L41N_3	I/O L35N_3 LHCLK7	VCCINT	GND	VCCINT
R	I/O L36P_3 VREF_3	I/O L36N_3	I/O L37P_3	I/O L37N_3	I/O L40P_3	I/O L40N_3	I/O L45N_3	I/O L45P_3	I/O L43N_3	I/O L43P_3 VREF_3	GND	VCCINT	GND
T	GND	VCCO_3	I/O L38P_3	I/O L38N_3	I/O L42P_3	GND	I/O L51P_3	VCCO_3	I/O L48N_3	I/O L48P_3	VCCINT	GND	VCCINT
U	I/O L44P_3	I/O L44N_3	INPUT L46P_3	I/O L42N_3	I/O L49P_3	I/O L51N_3	I/O L56P_3	I/O L56N_3	I/O L61P_3	GND	I/O L13N_2	VCCINT	GND
V	I/O L47P_3	I/O L47N_3	GND	INPUT L46N_3	I/O L49N_3	I/O L59N_3	I/O L59P_3	I/O L61N_3	VCCAUX	I/O L09P_2	I/O L13P_2	I/O L16P_2	I/O L20P_2
W	INPUT L50P_3	INPUT L50N_3 VREF_3	I/O L52P_3	I/O L52N_3	VCCO_3	I/O L63N_3	I/O L63P_3	GND	I/O L05P_2	I/O L09N_2	VCCO_2	I/O L16N_2	I/O L20N_2
Y	I/O L53P_3	I/O L53N_3	INPUT L54P_3 ▽	INPUT L54N_3 ▽	I/O L57P_3	I/O L57N_3	I/O L02P_2 M2	INPUT ▽	I/O L05N_2	I/O L12P_2	INPUT ▽	I/O L17P_2 RDWR_B	I/O L25N_2 GCLK13
AA	GND	I/O L55P_3	I/O L55N_3	INPUT L58P_3 ▽	INPUT L58N_3 VREF_3 ▽	GND	I/O L02N_2 CSO_B	INPUT ▽	INPUT VREF_2	I/O L12N_2	GND	I/O L17N_2 VS2	I/O L25P_2 GCLK12
AB	I/O L60P_3	VCCO_3	INPUT L62P_3 ▽	INPUT L62N_3 ▽	VCCAUX	INPUT VREF_2	I/O L14N_2	VCCO_2	I/O L15P_2	INPUT VREF_2 ▽	VCCAUX	I/O L21P_2	INPUT
AC	I/O L60N_3	I/O L64P_3	I/O L64N_3	I/O L01P_2 M1	INPUT ▽	I/O L08P_2	INPUT ▽	I/O L14P_2	I/O L15N_2	INPUT VREF_2	I/O L23N_2	I/O L21N_2	INPUT
AD	I/O L65P_3	I/O L65N_3	GND	I/O L01N_2 M0	INPUT ▽	I/O L08N_2	I/O L11P_2	GND	INPUT	INPUT	I/O L23P_2	INPUT VREF_2	GND
AE	INPUT L66P_3	INPUT L66N_3 VREF_3	I/O L06P_2	I/O L07P_2	VCCO_2	I/O L10N_2	I/O L11N_2	I/O L18P_2	I/O L19P_2 VS1	I/O L22P_2 D7	VCCO_2	I/O L24N_2 D4	I/O L26N_2 GCLK15
AF	GND	INPUT ▽	I/O L06N_2	I/O L07N_2	I/O L10P_2	GND	INPUT ▽	I/O L18N_2	I/O L19N_2 VS0	I/O L22N_2 D6	GND	I/O L24P_2 D5	I/O L26P_2 GCLK14

Bank 3

Bank 2

Figure 16: **FG676 Package Footprint for XC3SD1800A FPGA (Top View–Left Half)**



Right Half of FG676 Package (Top View)

Figure 17: FG676 Package Footprint for XC3SD1800A FPGA (Top View–Right Half)

XC3SD3400A FPGA

Table 68 lists all the FG676 package pins for the XC3SD3400A FPGA. They are sorted by bank number and then by pin name. Pairs of pins that form a differential I/O pair appear together in the table. Table 68 also shows the pin number for each pin and the pin type, as defined earlier.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at: www.xilinx.com/support/documentation/data_sheets/s3a_pin.zip.

Pinout Table

Note: The grayed boxes denote a difference between the XC3SD1800A and the XC3SD3400A devices.

Table 68: **Spartan-3A DSP FG676 Pinout for XC3SD3400A FPGA**

Bank	XC3SD3400A Pin Name	FG676 Ball	Type
0	IO_L43N_0	K11	I/O
0	IO_L39N_0	K12	I/O
0	IO_L25P_0/GCLK4	K14	GCLK
0	IO_L12N_0	K16	I/O
0	IP_0	J10	INPUT
0	IO_L43P_0	J11	I/O
0	IO_L39P_0	J12	I/O
0	IP_0	J13	INPUT
0	IO_L25N_0/GCLK5	J14	GCLK
0	IP_0	J15	INPUT
0	IO_L12P_0	J16	I/O
0	IP_0/VREF_0	J17	VREF
0	IO_L47N_0	H9	I/O
0	IO_L46N_0	H10	I/O
0	IO_L35N_0	H12	I/O
0	IP_0	H13	INPUT
0	IO_L16N_0	H15	I/O
0	IO_L08P_0	H17	I/O
0	IP_0	H18	INPUT
0	IO_L52N_0/PUDC_B	G8	DUAL
0	IO_L47P_0	G9	I/O
0	IO_L46P_0	G10	I/O
0	IP_0/VREF_0	G11	VREF
0	IO_L35P_0	G12	I/O
0	IO_L27N_0/GCLK9	G13	GCLK
0	IP_0	G14	INPUT
0	IO_L16P_0	G15	I/O
0	IO_L08N_0	G17	I/O
0	IO_L02P_0/VREF_0	G19	VREF
0	IO_L01P_0	G20	I/O

Table 68: **Spartan-3A DSP FG676 Pinout for XC3SD3400A FPGA *(Cont'd)***

Bank	XC3SD3400A Pin Name	FG676 Ball	Type
0	IO_L48P_0	F7	I/O
0	IO_L52P_0/VREF_0	F8	VREF
0	IO_L31N_0	F12	I/O
0	IO_L27P_0/GCLK8	F13	GCLK
0	IO_L24N_0	F14	I/O
0	IO_L20P_0	F15	I/O
0	IO_L13P_0	F17	I/O
0	IO_L02N_0	F19	I/O
0	IO_L01N_0	F20	I/O
0	IO_L48N_0	E7	I/O
0	IO_L37P_0	E10	I/O
0	IP_0	E11	INPUT
0	IO_L31P_0	E12	I/O
0	IO_L24P_0	E14	I/O
0	IO_L20N_0/VREF_0	E15	VREF
0	IO_L13N_0	E17	I/O
0	IP_0	E18	INPUT
0	IO_L10P_0	E21	I/O
0	IO_L44N_0	D6	I/O
0	IP_0/VREF_0	D7	VREF
0	IO_L40N_0	D8	I/O
0	IO_L37N_0	D9	I/O
0	IO_L34N_0	D10	I/O
0	IO_L32N_0/VREF_0	D11	VREF
0	IP_0	D12	INPUT
0	IO_L30P_0	D13	I/O
0	IP_0/VREF_0	D14	VREF
0	IO_L22P_0	D16	I/O
0	IO_L21P_0	D17	I/O
0	IO_L17P_0	D18	I/O
0	IO_L11P_0	D20	I/O

Table 68: **Spartan-3A DSP FG676 Pinout for XC3SD3400A FPGA *(Cont'd)***

Bank	XC3SD3400A Pin Name	FG676 Ball	Type
0	IO_L10N_0	D21	I/O
0	IO_L05P_0	D22	I/O
0	IO_L06P_0	D23	I/O
0	IO_L44P_0	C5	I/O
0	IO_L41N_0	C6	I/O
0	IO_L42N_0	C7	I/O
0	IO_L40P_0	C8	I/O
0	IO_L34P_0	C10	I/O
0	IO_L32P_0	C11	I/O
0	IO_L30N_0	C12	I/O
0	IO_L28N_0/GCLK11	C13	GCLK
0	IO_L22N_0	C15	I/O
0	IO_L21N_0	C16	I/O
0	IO_L19P_0	C17	I/O
0	IO_L17N_0	C18	I/O
0	IO_L11N_0	C20	I/O
0	IO_L09P_0	C21	I/O
0	IO_L05N_0	C22	I/O
0	IO_L06N_0	C23	I/O
0	IO_L51N_0	B3	I/O
0	IO_L45N_0	B4	I/O
0	IO_L41P_0	B6	I/O
0	IO_L42P_0	B7	I/O
0	IO_L38N_0	B8	I/O
0	IO_L36N_0	B9	I/O
0	IO_L33N_0	B10	I/O
0	IO_L29N_0	B12	I/O
0	IO_L28P_0/GCLK10	B13	GCLK
0	IO_L26P_0/GCLK6	B14	GCLK
0	IO_L23P_0	B15	I/O
0	IO_L19N_0	B17	I/O
0	IO_L18P_0	B18	I/O
0	IO_L15P_0	B19	I/O
0	IO_L14P_0/VREF_0	B20	VREF
0	IO_L09N_0	B21	I/O
0	IO_L07P_0	B23	I/O
0	IO_L51P_0	A3	I/O
0	IO_L45P_0	A4	I/O
0	IO_L38P_0	A8	I/O

Table 68: **Spartan-3A DSP FG676 Pinout for XC3SD3400A FPGA *(Cont'd)***

Bank	XC3SD3400A Pin Name	FG676 Ball	Type
0	IO_L36P_0	A9	I/O
0	IO_L33P_0	A10	I/O
0	IO_L29P_0	A12	I/O
0	IP_0	A13	INPUT
0	IO_L26N_0/GCLK7	A14	GCLK
0	IO_L23N_0	A15	I/O
0	IP_0	A17	INPUT
0	IO_L18N_0	A18	I/O
0	IO_L15N_0	A19	I/O
0	IO_L14N_0	A20	I/O
0	IO_L07N_0	A22	I/O
0	VCCO_0	H11	VCCO
0	VCCO_0	H16	VCCO
0	VCCO_0	E8	VCCO
0	VCCO_0	E13	VCCO
0	VCCO_0	E19	VCCO
0	VCCO_0	B5	VCCO
0	VCCO_0	B11	VCCO
0	VCCO_0	B16	VCCO
0	VCCO_0	B22	VCCO
0	VCCO_0	A7	VCCO
1	IO_L01P_1/HDC	Y20	DUAL
1	IO_L01N_1/LDC2	Y21	DUAL
1	IO_L13P_1	Y22	I/O
1	IO_L13N_1	Y23	I/O
1	IO_L15P_1	Y24	I/O
1	IO_L15N_1	Y25	I/O
1	IP_1	Y26	INPUT
1	IO_L04P_1	W20	I/O
1	IO_L04N_1	W21	I/O
1	IO_L18P_1	W23	I/O
1	IO_L08P_1	V18	I/O
1	IO_L08N_1	V19	I/O
1	IO_L10P_1	V21	I/O
1	IO_L18N_1	V22	I/O
1	IO_L21P_1	V23	I/O
1	IO_L19P_1	V24	I/O
1	IO_L19N_1	V25	I/O
1	IP_1/VREF_1	V26	VREF

Table 68: **Spartan-3A DSP FG676 Pinout for XC3SD3400A FPGA *(Cont'd)***

Bank	XC3SD3400A Pin Name	FG676 Ball	Type
1	IO_L12N_1	U18	I/O
1	IO_L12P_1	U19	I/O
1	IO_L10N_1	U20	I/O
1	IO_L14P_1	U21	I/O
1	IO_L21N_1	U22	I/O
1	IO_L23P_1	U23	I/O
1	IO_L23N_1/VREF_1	U24	VREF
1	IP_1/VREF_1	U26	VREF
1	IO_L17N_1	T17	I/O
1	IO_L17P_1	T18	I/O
1	IO_L14N_1	T20	I/O
1	IO_L26P_1/A4	T23	DUAL
1	IO_L26N_1/A5	T24	DUAL
1	IO_L27N_1/A7	R17	DUAL
1	IO_L27P_1/A6	R18	DUAL
1	IO_L22P_1	R19	I/O
1	IO_L22N_1	R20	I/O
1	IO_L25P_1/A2	R21	DUAL
1	IO_L25N_1/A3	R22	DUAL
1	IP_L28P_1/VREF_1	R23	VREF
1	IP_L28N_1	R24	INPUT
1	IO_L29P_1/A8	R25	DUAL
1	IO_L29N_1/A9	R26	DUAL
1	IO_L34P_1/IRDY1/RHCLK6	P18	RHCLK
1	IO_L30N_1/RHCLK1	P20	RHCLK
1	IO_L30P_1/RHCLK0	P21	RHCLK
1	IO_L37P_1	P22	I/O
1	IO_L33P_1/RHCLK4	P23	RHCLK
1	IO_L31N_1/TRDY1/RHCLK3	P25	RHCLK
1	IO_L31P_1/RHCLK2	P26	RHCLK
1	IO_L39N_1/A15	N17	DUAL
1	IO_L39P_1/A14	N18	DUAL
1	IO_L34N_1/RHCLK7	N19	RHCLK
1	IO_L42P_1/A16	N20	DUAL
1	IO_L37N_1	N21	I/O
1	IP_L36N_1	N23	INPUT
1	IO_L33N_1/RHCLK5	N24	RHCLK
1	IP_L32N_1	N25	INPUT
1	IP_L32P_1	N26	INPUT

Table 68: **Spartan-3A DSP FG676 Pinout for XC3SD3400A FPGA *(Cont'd)***

Bank	XC3SD3400A Pin Name	FG676 Ball	Type
1	IO_L47N_1	M18	I/O
1	IO_L47P_1	M19	I/O
1	IO_L42N_1/A17	M20	DUAL
1	IO_L45P_1	M21	I/O
1	IO_L45N_1	M22	I/O
1	IO_L38N_1/A13	M23	DUAL
1	IP_L36P_1/VREF_1	M24	VREF
1	IO_L35N_1/A11	M25	DUAL
1	IO_L35P_1/A10	M26	DUAL
1	IO_L55N_1	L17	I/O
1	IO_L55P_1	L18	I/O
1	IO_L53P_1	L20	I/O
1	IO_L50P_1	L22	I/O
1	IP_L40N_1	L23	INPUT
1	IO_L38P_1/A12	L24	DUAL
1	IO_L57N_1	K18	I/O
1	IO_L57P_1	K19	I/O
1	IO_L53N_1	K20	I/O
1	IO_L50N_1	K21	I/O
1	IO_L46N_1	K22	I/O
1	IO_L46P_1	K23	I/O
1	IP_L40P_1	K24	INPUT
1	IO_L41P_1	K25	I/O
1	IO_L41N_1	K26	I/O
1	IO_L59P_1	J19	I/O
1	IO_L59N_1	J20	I/O
1	IO_L62P_1/A20	J21	DUAL
1	IO_L49N_1	J22	I/O
1	IO_L49P_1	J23	I/O
1	IO_L43N_1/A19	J25	DUAL
1	IO_L43P_1/A18	J26	DUAL
1	IO_L64P_1/A24	H20	DUAL
1	IO_L62N_1/A21	H21	DUAL
1	IP_1	H24	INPUT
1	IP_1/VREF_1	H26	VREF
1	IO_L64N_1/A25	G21	DUAL
1	IO_L58N_1	G22	I/O
1	IO_L51P_1	G23	I/O
1	IO_L51N_1	G24	I/O

Table 68: **Spartan-3A DSP FG676 Pinout for XC3SD3400A FPGA *(Cont'd)***

Bank	XC3SD3400A Pin Name	FG676 Ball	Type
1	IP_1/VREF_1	G25	VREF
1	IO_L58P_1/VREF_1	F22	VREF
1	IO_L56N_1	F23	I/O
1	IO_L54N_1	F24	I/O
1	IO_L54P_1	F25	I/O
1	IO_L56P_1	E24	I/O
1	IO_L60P_1	E26	I/O
1	IO_L61N_1	D24	I/O
1	IO_L61P_1	D25	I/O
1	IO_L60N_1	D26	I/O
1	IO_L63N_1/A23	C25	DUAL
1	IO_L63P_1/A22	C26	DUAL
1	IP_1/VREF_1	B26	VREF
1	IO_L02P_1/LDC1	AE26	DUAL
1	IO_L02N_1/LDC0	AD25	DUAL
1	IO_L05P_1	AD26	I/O
1	IO_L03P_1/A0	AC23	DUAL
1	IO_L03N_1/A1	AC24	DUAL
1	IO_L05N_1	AC25	I/O
1	IO_L06P_1	AC26	I/O
1	IO_L07P_1	AB23	I/O
1	IO_L07N_1/VREF_1	AB24	VREF
1	IO_L06N_1	AB26	I/O
1	IO_L09P_1	AA22	I/O
1	IO_L09N_1	AA23	I/O
1	IO_L11P_1	AA24	I/O
1	IO_L11N_1	AA25	I/O
1	VCCO_1	W22	VCCO
1	VCCO_1	T19	VCCO
1	VCCO_1	T25	VCCO
1	VCCO_1	N22	VCCO
1	VCCO_1	L19	VCCO
1	VCCO_1	L25	VCCO
1	VCCO_1	H22	VCCO
1	VCCO_1	H25	VCCO
1	VCCO_1	E25	VCCO
1	VCCO_1	AB25	VCCO
2	IO_L02P_2/M2	Y7	DUAL
2	IO_L05N_2	Y9	I/O

Table 68: **Spartan-3A DSP FG676 Pinout for XC3SD3400A FPGA *(Cont'd)***

Bank	XC3SD3400A Pin Name	FG676 Ball	Type
2	IO_L12P_2	Y10	I/O
2	IO_L17P_2/RDWR_B	Y12	DUAL
2	IO_L25N_2/GCLK13	Y13	GCLK
2	IO_L27P_2/GCLK0	Y14	GCLK
2	IO_L34N_2/D3	Y15	DUAL
2	IP_2/VREF_2	Y16	VREF
2	IO_L43N_2	Y17	I/O
2	IO_L05P_2	W9	I/O
2	IO_L09N_2	W10	I/O
2	IO_L16N_2	W12	I/O
2	IO_L20N_2	W13	I/O
2	IO_L31N_2	W15	I/O
2	IO_L46P_2	W17	I/O
2	IO_L09P_2	V10	I/O
2	IO_L13P_2	V11	I/O
2	IO_L16P_2	V12	I/O
2	IO_L20P_2	V13	I/O
2	IO_L31P_2	V14	I/O
2	IO_L35P_2	V15	I/O
2	IO_L42P_2	V16	I/O
2	IO_L46N_2	V17	I/O
2	IO_L13N_2	U11	I/O
2	IO_L35N_2	U15	I/O
2	IO_L42N_2	U16	I/O
2	IO_L06N_2	AF3	I/O
2	IO_L07N_2	AF4	I/O
2	IO_L10P_2	AF5	I/O
2	IO_L18N_2	AF8	I/O
2	IO_L19N_2/VS0	AF9	DUAL
2	IO_L22N_2/D6	AF10	DUAL
2	IO_L24P_2/D5	AF12	DUAL
2	IO_L26P_2/GCLK14	AF13	GCLK
2	IO_L28P_2/GCLK2	AF14	GCLK
2	IP_2/VREF_2	AF15	VREF
2	IP_2/VREF_2	AF17	VREF
2	IO_L36P_2/D2	AF18	DUAL
2	IO_L37P_2	AF19	I/O
2	IO_L39P_2	AF20	I/O
2	IP_2/VREF_2	AF22	VREF

Table 68: **Spartan-3A DSP FG676 Pinout for XC3SD3400A FPGA *(Cont'd)***

Bank	XC3SD3400A Pin Name	FG676 Ball	Type
2	IO_L48P_2	AF23	I/O
2	IO_L52P_2/D0/DIN/MISO	AF24	DUAL
2	IO_L51P_2	AF25	I/O
2	IO_L06P_2	AE3	I/O
2	IO_L07P_2	AE4	I/O
2	IO_L10N_2	AE6	I/O
2	IO_L11N_2	AE7	I/O
2	IO_L18P_2	AE8	I/O
2	IO_L19P_2/VS1	AE9	DUAL
2	IO_L22P_2/D7	AE10	DUAL
2	IO_L24N_2/D4	AE12	DUAL
2	IO_L26N_2/GCLK15	AE13	GCLK
2	IO_L28N_2/GCLK3	AE14	GCLK
2	IO_L32N_2/DOUT	AE15	DUAL
2	IO_L33P_2	AE17	I/O
2	IO_L36N_2/D1	AE18	DUAL
2	IO_L37N_2	AE19	I/O
2	IO_L39N_2	AE20	I/O
2	IO_L44P_2	AE21	I/O
2	IO_L48N_2	AE23	I/O
2	IO_L52N_2/CCLK	AE24	DUAL
2	IO_L51N_2	AE25	I/O
2	IO_L01N_2/M0	AD4	DUAL
2	IO_L08N_2	AD6	I/O
2	IO_L11P_2	AD7	I/O
2	IP_2	AD9	INPUT
2	IP_2	AD10	INPUT
2	IO_L23P_2	AD11	I/O
2	IP_2/VREF_2	AD12	VREF
2	IO_L29P_2	AD14	I/O
2	IO_L32P_2/AWAKE	AD15	PWRMGMT
2	IP_2	AD16	INPUT
2	IO_L33N_2	AD17	I/O
2	IO_L40P_2	AD19	I/O
2	IO_L41P_2	AD20	I/O
2	IO_L44N_2	AD21	I/O
2	IO_L45P_2	AD22	I/O
2	IO_L01P_2/M1	AC4	DUAL
2	IO_L08P_2	AC6	I/O

Table 68: **Spartan-3A DSP FG676 Pinout for XC3SD3400A FPGA *(Cont'd)***

Bank	XC3SD3400A Pin Name	FG676 Ball	Type
2	IO_L14P_2	AC8	I/O
2	IO_L15N_2	AC9	I/O
2	IP_2/VREF_2	AC10	VREF
2	IO_L23N_2	AC11	I/O
2	IO_L21N_2	AC12	I/O
2	IP_2	AC13	INPUT
2	IO_L29N_2	AC14	I/O
2	IO_L30P_2	AC15	I/O
2	IO_L38P_2	AC16	I/O
2	IP_2	AC17	INPUT
2	IO_L40N_2	AC19	I/O
2	IO_L41N_2	AC20	I/O
2	IO_L45N_2	AC21	I/O
2	IO_2	AC22	I/O
2	IP_2/VREF_2	AB6	VREF
2	IO_L14N_2	AB7	I/O
2	IO_L15P_2	AB9	I/O
2	IO_L21P_2	AB12	I/O
2	IP_2	AB13	INPUT
2	IO_L30N_2/MOSI/CSI_B	AB15	DUAL
2	IO_L38N_2	AB16	I/O
2	IO_L47P_2	AB18	I/O
2	IO_L02N_2/CSO_B	AA7	DUAL
2	IP_2/VREF_2	AA9	VREF
2	IO_L12N_2	AA10	I/O
2	IO_L17N_2/VS2	AA12	DUAL
2	IO_L25P_2/GCLK12	AA13	GCLK
2	IO_L27N_2/GCLK1	AA14	GCLK
2	IO_L34P_2/INIT_B	AA15	DUAL
2	IO_L43P_2	AA17	I/O
2	IO_L47N_2	AA18	I/O
2	IP_2/VREF_2	AA20	VREF
2	VCCO_2	W11	VCCO
2	VCCO_2	W16	VCCO
2	VCCO_2	AF7	VCCO
2	VCCO_2	AE5	VCCO
2	VCCO_2	AE11	VCCO
2	VCCO_2	AE16	VCCO
2	VCCO_2	AE22	VCCO

Table 68: **Spartan-3A DSP FG676 Pinout for XC3SD3400A FPGA *(Cont'd)***

Bank	XC3SD3400A Pin Name	FG676 Ball	Type
2	VCCO_2	AB8	VCCO
2	VCCO_2	AB14	VCCO
2	VCCO_2	AB19	VCCO
3	IO_L53P_3	Y1	I/O
3	IO_L53N_3	Y2	I/O
3	IP_3	Y3	INPUT
3	IO_L57P_3	Y5	I/O
3	IO_L57N_3	Y6	I/O
3	IP_L50P_3	W1	INPUT
3	IP_L50N_3/VREF_3	W2	VREF
3	IO_L52P_3	W3	I/O
3	IO_L52N_3	W4	I/O
3	IO_L63N_3	W6	I/O
3	IO_L63P_3	W7	I/O
3	IO_L47P_3	V1	I/O
3	IO_L47N_3	V2	I/O
3	IP_L46N_3	V4	INPUT
3	IO_L49N_3	V5	I/O
3	IO_L59N_3	V6	I/O
3	IO_L59P_3	V7	I/O
3	IO_L61N_3	V8	I/O
3	IO_L44P_3	U1	I/O
3	IO_L44N_3	U2	I/O
3	IP_L46P_3	U3	INPUT
3	IO_L42N_3	U4	I/O
3	IO_L49P_3	U5	I/O
3	IO_L51N_3	U6	I/O
3	IO_L56P_3	U7	I/O
3	IO_L56N_3	U8	I/O
3	IO_L61P_3	U9	I/O
3	IO_L38P_3	T3	I/O
3	IO_L38N_3	T4	I/O
3	IO_L42P_3	T5	I/O
3	IO_L51P_3	T7	I/O
3	IO_L48N_3	T9	I/O
3	IO_L48P_3	T10	I/O
3	IO_L36P_3/VREF_3	R1	VREF
3	IO_L36N_3	R2	I/O
3	IO_L37P_3	R3	I/O

Table 68: **Spartan-3A DSP FG676 Pinout for XC3SD3400A FPGA *(Cont'd)***

Bank	XC3SD3400A Pin Name	FG676 Ball	Type
3	IO_L37N_3	R4	I/O
3	IO_L40P_3	R5	I/O
3	IO_L40N_3	R6	I/O
3	IO_L45N_3	R7	I/O
3	IO_L45P_3	R8	I/O
3	IO_L43N_3	R9	I/O
3	IO_L43P_3/VREF_3	R10	VREF
3	IO_L33P_3/LHCLK2	P1	LHCLK
3	IO_L33N_3/IRDY2/LHCLK3	P2	LHCLK
3	IO_L34N_3/LHCLK5	P3	LHCLK
3	IO_L34P_3/LHCLK4	P4	LHCLK
3	IO_L39N_3	P6	I/O
3	IO_L39P_3	P7	I/O
3	IO_L41P_3	P8	I/O
3	IO_L41N_3	P9	I/O
3	IO_L35N_3/LHCLK7	P10	LHCLK
3	IO_L31P_3	N1	I/O
3	IO_L31N_3	N2	I/O
3	IO_L30N_3	N4	I/O
3	IO_L30P_3	N5	I/O
3	IO_L32P_3/LHCLK0	N6	LHCLK
3	IO_L32N_3/LHCLK1	N7	LHCLK
3	IO_L35P_3/TRDY2/LHCLK6	N9	LHCLK
3	IO_L29N_3/VREF_3	M1	VREF
3	IO_L29P_3	M2	I/O
3	IO_L27N_3	M3	I/O
3	IO_L27P_3	M4	I/O
3	IO_L28P_3	M5	I/O
3	IO_L28N_3	M6	I/O
3	IO_L26N_3	M7	I/O
3	IO_L26P_3	M8	I/O
3	IO_L21N_3	M9	I/O
3	IO_L21P_3	M10	I/O
3	IO_L25N_3	L3	I/O
3	IO_L25P_3	L4	I/O
3	IO_L18N_3	L7	I/O
3	IO_L15N_3	L9	I/O
3	IO_L15P_3	L10	I/O
3	IP_L24N_3	K1	INPUT

Table 68: **Spartan-3A DSP FG676 Pinout for XC3SD3400A FPGA *(Cont'd)***

Bank	XC3SD3400A Pin Name	FG676 Ball	Type
3	IO_L23N_3	K2	I/O
3	IO_L23P_3	K3	I/O
3	IO_L22N_3	K4	I/O
3	IO_L22P_3	K5	I/O
3	IO_L18P_3	K6	I/O
3	IO_L13P_3	K7	I/O
3	IO_L05N_3	K8	I/O
3	IO_L05P_3	K9	I/O
3	IP_L24P_3	J1	INPUT
3	IP_L20N_3/VREF_3	J2	VREF
3	IP_L20P_3	J3	INPUT
3	IO_L19N_3	J4	I/O
3	IO_L19P_3	J5	I/O
3	IO_L13N_3	J6	I/O
3	IO_L10P_3	J7	I/O
3	IO_L01P_3	J8	I/O
3	IO_L01N_3	J9	I/O
3	IO_L17N_3	H1	I/O
3	IO_L17P_3	H2	I/O
3	IP_3/VREF_3	H4	VREF
3	IO_L10N_3	H6	I/O
3	IO_L03N_3	H7	I/O
3	IP_3	G1	INPUT
3	IO_L14P_3	G3	I/O
3	IO_L09N_3	G4	I/O
3	IO_L03P_3	G6	I/O
3	IO_L11N_3	F2	I/O
3	IO_L14N_3	F3	I/O
3	IO_L07N_3	F4	I/O
3	IO_L09P_3	F5	I/O
3	IO_L11P_3	E1	I/O
3	IO_L07P_3	E3	I/O
3	IO_L06N_3	E4	I/O
3	IO_L06P_3	D3	I/O
3	IP_3/VREF_3	C1	VREF
3	IO_L02N_3	B1	I/O
3	IO_L02P_3	B2	I/O
3	IP_L66P_3	AE1	INPUT
3	IP_L66N_3/VREF_3	AE2	VREF

Table 68: **Spartan-3A DSP FG676 Pinout for XC3SD3400A FPGA *(Cont'd)***

Bank	XC3SD3400A Pin Name	FG676 Ball	Type
3	IO_L65P_3	AD1	I/O
3	IO_L65N_3	AD2	I/O
3	IO_L60N_3	AC1	I/O
3	IO_L64P_3	AC2	I/O
3	IO_L64N_3	AC3	I/O
3	IO_L60P_3	AB1	I/O
3	IO_L55P_3	AA2	I/O
3	IO_L55N_3	AA3	I/O
3	IP_3/VREF_3	AA5	VREF
3	VCCO_3	W5	VCCO
3	VCCO_3	T2	VCCO
3	VCCO_3	T8	VCCO
3	VCCO_3	P5	VCCO
3	VCCO_3	L2	VCCO
3	VCCO_3	L8	VCCO
3	VCCO_3	H5	VCCO
3	VCCO_3	E2	VCCO
3	VCCO_3	C2	VCCO
3	VCCO_3	AB2	VCCO
GND	GND	W8	GND
GND	GND	W14	GND
GND	GND	W19	GND
GND	GND	W24	GND
GND	GND	W25	GND
GND	GND	V3	GND
GND	GND	U10	GND
GND	GND	U13	GND
GND	GND	U17	GND
GND	GND	U25	GND
GND	GND	T1	GND
GND	GND	T6	GND
GND	GND	T12	GND
GND	GND	T14	GND
GND	GND	T16	GND
GND	GND	T21	GND
GND	GND	T26	GND
GND	GND	R11	GND
GND	GND	R13	GND
GND	GND	R15	GND

Table 68: **Spartan-3A DSP FG676 Pinout for XC3SD3400A FPGA *(Cont'd)***

Bank	XC3SD3400A Pin Name	FG676 Ball	Type
GND	GND	P12	GND
GND	GND	P16	GND
GND	GND	P19	GND
GND	GND	P24	GND
GND	GND	N3	GND
GND	GND	N8	GND
GND	GND	N11	GND
GND	GND	N15	GND
GND	GND	M12	GND
GND	GND	M14	GND
GND	GND	M16	GND
GND	GND	L1	GND
GND	GND	L6	GND
GND	GND	L11	GND
GND	GND	L13	GND
GND	GND	L15	GND
GND	GND	L21	GND
GND	GND	L26	GND
GND	GND	K10	GND
GND	GND	K17	GND
GND	GND	J24	GND
GND	GND	H3	GND
GND	GND	H8	GND
GND	GND	H14	GND
GND	GND	H19	GND
GND	GND	G2	GND
GND	GND	G5	GND
GND	GND	G16	GND
GND	GND	F1	GND
GND	GND	F6	GND
GND	GND	F11	GND
GND	GND	F16	GND
GND	GND	F21	GND
GND	GND	F26	GND
GND	GND	E9	GND
GND	GND	D2	GND
GND	GND	D15	GND
GND	GND	D19	GND
GND	GND	C3	GND

Table 68: **Spartan-3A DSP FG676 Pinout for XC3SD3400A FPGA *(Cont'd)***

Bank	XC3SD3400A Pin Name	FG676 Ball	Type
GND	GND	C9	GND
GND	GND	C14	GND
GND	GND	C19	GND
GND	GND	C24	GND
GND	GND	B24	GND
GND	GND	B25	GND
GND	GND	AF1	GND
GND	GND	AF6	GND
GND	GND	AF11	GND
GND	GND	AF16	GND
GND	GND	AF21	GND
GND	GND	AF26	GND
GND	GND	AD3	GND
GND	GND	AD5	GND
GND	GND	AD8	GND
GND	GND	AD13	GND
GND	GND	AD18	GND
GND	GND	AD23	GND
GND	GND	AD24	GND
GND	GND	AC5	GND
GND	GND	AC7	GND
GND	GND	AC18	GND
GND	GND	AB3	GND
GND	GND	AB10	GND
GND	GND	AB20	GND
GND	GND	AA1	GND
GND	GND	AA4	GND
GND	GND	AA6	GND
GND	GND	AA11	GND
GND	GND	AA16	GND
GND	GND	AA19	GND
GND	GND	AA21	GND
GND	GND	AA26	GND
GND	GND	A1	GND
GND	GND	A5	GND
GND	GND	A6	GND
GND	GND	A11	GND
GND	GND	A16	GND
GND	GND	A21	GND

Table 68: **Spartan-3A DSP FG676 Pinout for XC3SD3400A FPGA *(Cont'd)***

Bank	XC3SD3400A Pin Name	FG676 Ball	Type
GND	GND	A23	GND
GND	GND	A26	GND
VCCAUX	SUSPEND	V20	PWRMGMT
VCCAUX	DONE	AB21	CONFIG
VCCAUX	PROG_B	A2	CONFIG
VCCAUX	TDI	G7	JTAG
VCCAUX	TDO	E23	JTAG
VCCAUX	TMS	D4	JTAG
VCCAUX	TCK	A25	JTAG
VCCAUX	VCCAUX	W26	VCCAUX
VCCAUX	VCCAUX	V9	VCCAUX
VCCAUX	VCCAUX	U14	VCCAUX
VCCAUX	VCCAUX	T22	VCCAUX
VCCAUX	VCCAUX	P17	VCCAUX
VCCAUX	VCCAUX	N10	VCCAUX
VCCAUX	VCCAUX	L5	VCCAUX
VCCAUX	VCCAUX	K13	VCCAUX
VCCAUX	VCCAUX	J18	VCCAUX
VCCAUX	VCCAUX	H23	VCCAUX
VCCAUX	VCCAUX	G26	VCCAUX
VCCAUX	VCCAUX	F9	VCCAUX
VCCAUX	VCCAUX	E5	VCCAUX
VCCAUX	VCCAUX	E16	VCCAUX
VCCAUX	VCCAUX	E20	VCCAUX
VCCAUX	VCCAUX	E22	VCCAUX
VCCAUX	VCCAUX	D1	VCCAUX
VCCAUX	VCCAUX	AF2	VCCAUX
VCCAUX	VCCAUX	AB4	VCCAUX
VCCAUX	VCCAUX	AB5	VCCAUX
VCCAUX	VCCAUX	AB11	VCCAUX
VCCAUX	VCCAUX	AB17	VCCAUX
VCCAUX	VCCAUX	AB22	VCCAUX
VCCAUX	VCCAUX	A24	VCCAUX
VCCINT	VCCINT	Y4	VCCINT
VCCINT	VCCINT	Y8	VCCINT
VCCINT	VCCINT	Y11	VCCINT
VCCINT	VCCINT	Y18	VCCINT
VCCINT	VCCINT	Y19	VCCINT
VCCINT	VCCINT	W18	VCCINT

Table 68: **Spartan-3A DSP FG676 Pinout for XC3SD3400A FPGA *(Cont'd)***

Bank	XC3SD3400A Pin Name	FG676 Ball	Type
VCCINT	VCCINT	U12	VCCINT
VCCINT	VCCINT	T11	VCCINT
VCCINT	VCCINT	T13	VCCINT
VCCINT	VCCINT	T15	VCCINT
VCCINT	VCCINT	R12	VCCINT
VCCINT	VCCINT	R14	VCCINT
VCCINT	VCCINT	R16	VCCINT
VCCINT	VCCINT	P11	VCCINT
VCCINT	VCCINT	P13	VCCINT
VCCINT	VCCINT	P14	VCCINT
VCCINT	VCCINT	P15	VCCINT
VCCINT	VCCINT	N12	VCCINT
VCCINT	VCCINT	N13	VCCINT
VCCINT	VCCINT	N14	VCCINT
VCCINT	VCCINT	N16	VCCINT
VCCINT	VCCINT	M11	VCCINT
VCCINT	VCCINT	M13	VCCINT
VCCINT	VCCINT	M15	VCCINT
VCCINT	VCCINT	M17	VCCINT
VCCINT	VCCINT	L12	VCCINT
VCCINT	VCCINT	L14	VCCINT
VCCINT	VCCINT	L16	VCCINT
VCCINT	VCCINT	K15	VCCINT
VCCINT	VCCINT	G18	VCCINT
VCCINT	VCCINT	F10	VCCINT
VCCINT	VCCINT	F18	VCCINT
VCCINT	VCCINT	E6	VCCINT
VCCINT	VCCINT	D5	VCCINT
VCCINT	VCCINT	C4	VCCINT
VCCINT	VCCINT	AA8	VCCINT

User I/Os by Bank

Table 69 indicates how the available user-I/O pins are distributed between the four I/O banks on the FG676 package. The AWAKE pin is counted as a dual-purpose I/O.

Table 69: **User I/Os Per Bank for the XC3SD3400A in the FG676 Package**

Package Edge	I/O Bank	Maximum I/Os and Input-Only	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF[1]	CLK
Top	0	111	82	11	1	9	8
Right	1	123	67	8	30	10	8
Bottom	2	112	68	6	21	9	8
Left	3	123	97	9	0	9	8
TOTAL		**469**	**314**	**34**	**52**	**37**	**32**

Notes:

1. 26 VREF are on INPUT pins.

FG676 Footprint – XC3SD3400A FPGA

Left Half of Package (Top View)

314 **I/O:** Unrestricted, general-purpose user I/O.

34 **INPUT:** Unrestricted, general-purpose input pin.

51 **DUAL:** Configuration pins, then possible user I/O.

37 **VREF:** User I/O or input voltage reference for bank.

32 **CLK:** User I/O, input, or clock buffer input.

2 **CONFIG:** Dedicated configuration pins.

2 **SUSPEND:** Dedicated SUSPEND and dual-purpose AWAKE Power Management pins

4 **JTAG:** Dedicated JTAG port pins.

100 **GND:** Ground

40 **VCCO:** Output voltage supply for bank.

36 **VCCINT:** Internal core supply voltage (+1.2V).

24 **VCCAUX:** Auxiliary supply voltage.

Note: The boxes with question marks inside indicate pin differences from the XC3SD1800A device. Please see the Footprint Migration Differences section for more information.

	Bank 0												
	1	2	3	4	5	6	7	8	9	10	11	12	13
A	GND	PROG_B	I/O L51P_0	I/O L45P_0	GND ▽	GND	VCCO_0 ▽	I/O L38P_0	I/O L36P_0	I/O L33P_0	GND	I/O L29P_0	INPUT
B	I/O L02N_3	I/O L02P_3	I/O L51N_0	I/O L45N_0	VCCO_0	I/O L41P_0	I/O L42P_0	I/O L38N_0	I/O L36N_0	I/O L33N_0	VCCO_0	I/O L29N_0	I/O L28P_0 GCLK10
C	INPUT VREF_3 ▽	VCCO_3 ▽	GND	VCCINT ▽	I/O L44P_0	I/O L41N_0	I/O L42N_0	I/O L40P_0	GND	I/O L34P_0	I/O L32P_0	I/O L30N_0	I/O L28N_0 GCLK11
D	VCCAUX ▽	GND ▽	I/O L06P_3	TMS	VCCINT ▽	I/O L44N_0	INPUT VREF_0	I/O L40N_0	I/O L37N_0	I/O L34N_0	I/O L32N_0 VREF_0	INPUT	I/O L30P_0
E	I/O L11P_3	VCCO_3	I/O L07P_3	I/O L06N_3	VCCAUX	VCCINT ▽	I/O L48N_0	VCCO_0	GND ▽	I/O L37P_0	INPUT	I/O L31P_0	VCCO_0
F	GND	I/O L11N_3	I/O L14N_3	I/O L07N_3	I/O L09P_3	GND	I/O L48P_0	I/O L52P_0 VREF_0	VCCAUX ▽	VCCINT ▽	GND	I/O L31N_0	I/O L27P_0 GCLK8
G	INPUT ▽	GND ▽	I/O L14P_3	I/O L09N_3	GND ▽	I/O L03P_3	TDI	I/O L52N_0 PUDC_B	I/O L47P_0	I/O L46P_0	INPUT VREF_0	I/O L35P_0	I/O L27N_0 GCLK9
H	I/O L17N_3	I/O L17P_3	GND	INPUT VREF_3 ▽	VCCO_3	I/O L10N_3	I/O L03N_3	GND	I/O L47N_0	I/O L46N_0	VCCO_0	I/O L35N_0	INPUT
J	INPUT L24P_3	INPUT L20N_3 VREF_3	INPUT L20P_3	I/O L19N_3	I/O L19P_3	I/O L13N_3	I/O L10P_3	I/O L01P_3	I/O L01N_3	INPUT	I/O L43P_0	I/O L39P_0	INPUT
K	INPUT L24N_3	I/O L23N_3	I/O L23P_3	I/O L22N_3	I/O L22P_3	I/O L18P_3	I/O L13P_3	I/O L05N_3	I/O L05P_3	GND	I/O L43N_0	I/O L39N_0	VCCAUX
L	GND	VCCO_3	I/O L25N_3	I/O L25P_3	VCCAUX	GND	I/O L18N_3	VCCO_3	I/O L15N_3	I/O L15P_3	GND	VCCINT	GND
M	I/O L29N_3 VREF_3	I/O L29P_3	I/O L27N_3	I/O L27P_3	I/O L28P_3	I/O L28N_3	I/O L26N_3	I/O L26P_3	I/O L21N_3	I/O L21P_3	VCCINT	GND	VCCINT
N	I/O L31P_3	I/O L31N_3	GND	I/O L30N_3	I/O L30P_3	I/O L32P_3 LHCLK0	I/O L32N_3 LHCLK1	GND	I/O L35P_3 TRDY2 LHCLK6	VCCAUX	GND	VCCINT	VCCINT
P	I/O L33P_3 LHCLK2	I/O L33N_3 IRDY2 LHCLK3	I/O L34N_3 LHCLK5	I/O L34P_3 LHCLK4	VCCO_3	I/O L39N_3	I/O L39P_3	I/O L41P_3	I/O L41N_3	I/O L35N_3 LHCLK7	VCCINT	GND	VCCINT
R	I/O L36P_3 VREF_3	I/O L36N_3	I/O L37P_3	I/O L37N_3	I/O L40P_3	I/O L40N_3	I/O L45N_3	I/O L45P_3	I/O L43N_3	I/O L43P_3 VREF_3	GND	VCCINT	GND
T	GND	VCCO_3	I/O L38P_3	I/O L38N_3	I/O L42P_3	GND	I/O L51P_3	VCCO_3	I/O L48N_3	I/O L48P_3	VCCINT	GND	VCCINT
U	I/O L44P_3	I/O L44N_3	INPUT L46P_3	I/O L42N_3	I/O L49P_3	I/O L51N_3	I/O L56P_3	I/O L56N_3	I/O L61P_3	GND	I/O L13N_2	VCCINT	GND
V	I/O L47P_3	I/O L47N_3	GND	INPUT L46N_3	I/O L49N_3	I/O L59N_3	I/O L59P_3	I/O L61N_3	VCCAUX	I/O L09P_2	I/O L13P_2	I/O L16P_2	I/O L20P_2
W	INPUT L50P_3	INPUT L50N_3 VREF_3	I/O L52P_3	I/O L52N_3	VCCO_3	I/O L63N_3	I/O L63P_3	GND	I/O L05P_2	I/O L09N_2	VCCO_2	I/O L16N_2	I/O L20N_2
Y	I/O L53P_3	I/O L53N_3	INPUT ▽	VCCINT ▽	I/O L57P_3	I/O L57N_3	I/O L02P_2 M2	VCCINT ▽	I/O L05N_2	I/O L12P_2	VCCINT ▽	I/O L17P_2 RDWR_B	I/O L25N_2 GCLK13
AA	GND	I/O L55P_3	I/O L55N_3	GND ▽	INPUT VREF_3 ▽	GND	I/O L02N_2 CSO_B	VCCINT ▽	INPUT VREF_2	I/O L12N_2	GND	I/O L17N_2 VS2	I/O L25P_2 GCLK12
AB	I/O L60P_3	VCCO_3	GND ▽	VCCAUX ▽	VCCAUX	INPUT VREF_2	I/O L14N_2	VCCO_2	I/O L15P_2	GND ▽	VCCAUX	I/O L21P_2	INPUT
AC	I/O L60N_3	I/O L64P_3	I/O L64N_3	I/O L01P_2 M1	GND ▽	I/O L08P_2	GND ▽	I/O L14P_2	I/O L15N_2	INPUT VREF_2	I/O L23N_2	I/O L21N_2	INPUT
AD	I/O L65P_3	I/O L65N_3	GND	I/O L01N_2 M0	GND ▽	I/O L08N_2	I/O L11P_2	GND	INPUT	INPUT	I/O L23P_2	INPUT VREF_2	GND
AE	INPUT L66P_3	INPUT L66N_3 VREF_3	I/O L06P_2	I/O L07P_2	VCCO_2	I/O L10N_2	I/O L11N_2	I/O L18P_2	I/O L19P_2 VS1	I/O L22P_2 D7	VCCO_2	I/O L24N_2 D4	I/O L26N_2 GCLK15
AF	GND	VCCAUX ▽	I/O L06N_2	I/O L07N_2	I/O L10P_2	GND	VCCO_2 ▽	I/O L18N_2	I/O L19N_2 VS0	I/O L22N_2 D6	GND	I/O L24P_2 D5	I/O L26P_2 GCLK14

Bank 3

Bank 2

Figure 17: **FG676 Package Footprint for XC3SD3400A FPGA (Top View–Left Half)**

Right Half of FG676 Package (Top View)

Figure 17: **FG676 Package Footprint for XC3SD3400A FPGA (Top View–Right Half)**

Footprint Migration Differences

There are multiple migration footprint differences between the XC3SD1800A and the XC3SD3400A in the FG676 package. These migration footprint differences are shown in Table 70. Migration from the XC3S1400A Spartan-3A device in the FG676 package to a Spartan-3A DSP device in the FG676 package is also possible. The XC3S1800A pin migration differences have been added to Table 70 for designs migrating between these devices.

Table 70: **FG676 Footprint Migration Differences**

FG676 Ball	Spartan-3A		Spartan-3A DSP		Spartan-3A DSP		FG676 Ball
	XC3S1400A Type	XC3S1400A Bank	XC3SD1800A Type	XC3SD1800A Bank	XC3SD3400A Type	XC3SD3400A Bank	
G16	IP_0	0	IP_0	0	GND	GND	G16
G18	N.C.	N.C.	IP_0	0	VCCINT	VCCINT	G18
F9	N.C.	N.C.	IP_0	0	VCCAUX	VCCAUX	F9
F10	IP_0	0	IP_0	0	VCCINT	VCCINT	F10
F18	N.C.	N.C.	IP_0	0	VCCINT	VCCINT	F18
E6	N.C.	N.C.	IP_0	0	VCCINT	VCCINT	E6
E9	N.C.	N.C.	IP_0	0	GND	GND	E9
E20	IP_0	0	IP_0	0	VCCAUX	VCCAUX	E20
D5	N.C.	N.C.	IP_0	0	VCCINT	VCCINT	D5
D15	IP_0	0	IP_0	0	GND	GND	D15
D19	IP_0	0	IP_0	0	GND	GND	D19
C4	IP_0	0	IP_0	0	VCCINT	VCCINT	C4
B24	N.C.	N.C.	IP_0	0	GND	GND	B24
A5	IP_0	0	IP_0	0	GND	GND	A5
A7	IP_0	0	IP_0	0	VCCO_0	0	A7
A23	IP_0	0	IP_0	0	GND	GND	A23
A24	N.C.	N.C.	IP_0	0	VCCAUX	VCCAUX	A24
Y26	IP_L16N_1	1	IP_L16N_1	1	IP_1	1	Y26
W25	IP_L16P_1	1	IP_L16P_1	1	GND	GND	W25
W26	IP_L20P_1	1	IP_L20P_1	1	VCCAUX	VCCAUX	W26
V26	IP_L20N_1/ VREF_1	1	IP_L20N_1/ VREF_1	1	IP_1/VREF_1	1	V26
U25	IP_L24P_1	1	IP_L24P_1	1	GND	GND	U25
U26	IP_L24N_1/ VREF_1	1	IP_L24N_1/ VREF_1	1	IP_1/VREF_1	1	U26
H23	IP_L48P_1	1	IP_L48P_1	1	VCCAUX	VCCAUX	H23
H24	IP_L48N_1	1	IP_L48N_1	1	IP_1	1	H24
H25	IP_L44N_1	1	IP_L44N_1	1	VCCO_1	1	H25
H26	IP_L44P_1/ VREF_1	1	IP_L44P_1/ VREF_1	1	IP_1/VREF_1	1	H26
G25	IP_L52N_1/ VREF_1	1	IP_L52N_1/ VREF_1	1	IP_1/VREF_1	1	G25
G26	IP_L52P_1	1	IP_L52P_1	1	VCCAUX	VCCAUX	G26
B25	IP_L65N_1	1	IP_L65N_1	1	GND	GND	B25
B26	IP_L65P_1/ VREF_1	1	IP_L65P_1/ VREF_1	1	IP_1/VREF_1	1	B26

Table 70: **FG676 Footprint Migration Differences *(Cont'd)***

FG676 Ball	Spartan-3A		Spartan-3A DSP		Spartan-3A DSP		FG676 Ball
	XC3S1400A Type	XC3S1400A Bank	XC3SD1800A Type	XC3SD1800A Bank	XC3SD3400A Type	XC3SD3400A Bank	
Y8	N.C.	N.C.	IP_2	2	VCCINT	VCCINT	Y8
Y11	IP_2	2	IP_2	2	VCCINT	VCCINT	Y11
Y18	N.C.	N.C.	IP_2	2	VCCINT	VCCINT	Y18
Y19	N.C.	N.C.	IP_2/VREF_2	2	VCCINT	VCCINT	Y19
W18	N.C.	N.C.	IP_2	2	VCCINT	VCCINT	W18
AF2	IP_2	2	IP_2	2	VCCAUX	VCCAUX	AF2
AF7	IP_2	2	IP_2	2	VCCO_2	2	AF7
AD5	N.C.	N.C.	IP_2	2	GND	GND	AD5
AD23	N.C.	N.C.	IP_2	2	GND	GND	AD23
AC5	N.C.	N.C.	IP_2	2	GND	GND	AC5
AC7	IP_2	2	IP_2	2	GND	GND	AC7
AC18	IP_2	2	IP_2	2	GND	GND	AC18
AB10	IP_2/VREF_2	2	IP_2/VREF_2	2	GND	GND	AB10
AB17	IP_2	2	IP_2	2	VCCAUX	VCCAUX	AB17
AB20	IP_2	2	IP_2	2	GND	GND	AB20
AA8	N.C.	N.C.	IP_2	2	VCCINT	VCCINT	AA8
AA19	IP_2	2	IP_2	2	GND	GND	AA19
AC22	N.C.	N.C.	IO_2	2	IO_2	2	AC22
Y3	IP_L54P_3	3	IP_L54P_3	3	IP_3	3	Y3
Y4	IP_L54N_3	3	IP_L54N_3	3	VCCINT	VCCINT	Y4
H4	IP_L12N_3/ VREF_3	3	IP_L12N_3/ VREF_3	3	IP_3/VREF_3	3	H4
G1	IP_L16N_3	3	IP_L16N_3	3	IP_3	3	G1
G2	IP_L16P_3	3	IP_L16P_3	3	GND	GND	G2
G5	IP_L12P_3	3	IP_L12P_3	3	GND	GND	G5
D1	IP_L08N_3	3	IP_L08N_3	3	VCCAUX	VCCAUX	D1
D2	IP_L08P_3	3	IP_L08P_3	3	GND	GND	D2
C1	IP_L04N_3/ VREF_3	3	IP_L04N_3/ VREF_3	3	IP_3/VREF_3	3	C1
C2	IP_L04P_3	3	IP_L04P_3	3	VCCO_3	3	C2
AB3	IP_L62P_3	3	IP_L62P_3	3	GND	GND	AB3
AB4	IP_L62N_3	3	IP_L62N_3	3	VCCAUX	VCCAUX	AB4
AA4	IP_L58P_3	3	IP_L58P_3	3	GND	GND	AA4
AA5	IP_L58N_3/ VREF_3	3	IP_L58N_3/ VREF_3	3	IP_3/VREF_3	3	AA5

Migration Recommendations

There are multiple pinout differences between the XC3SD1800A and the XC3SD3400A FPGAs in the FG676 package. Please note the differences between the two devices from Table 70 and take the necessary precautions.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
04/02/07	1.0	Initial Xilinx release.
05/25/07	1.1	Updates to Table 59, Table 63, Table 64, Table 65, Table 66, Table 67, Table 68, Table 69. Corrected VREF pins in XC3S1800A FG676 (Table 70). Updated FG676 package footprints for XC3SD1800A FPGA (Figure 16) and XC3SD3400A FPGA (Figure 17). Minor edits.
06/18/07	1.2	Updated for Production release.
07/16/07	2.0	Added Low-power options. Added advance thermal data to Table 62.
06/02/08	2.1	Added Package Overview section. Updated Thermal Characteristics in Table 62. Corrected name for AB14 in CS484 in Table 63. Updated links.
03/11/09	2.2	Corrected bank designation for SUSPEND to VCCAUX.
10/04/10	3.0	Revision update to match other data sheet modules.

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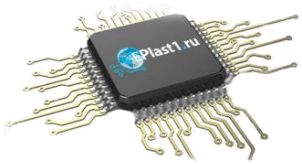

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