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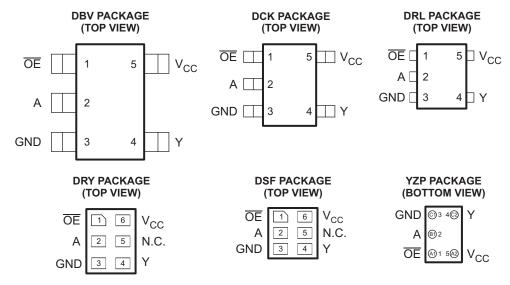
## SINGLE BUS BUFFER GATE WITH 3-STATE OUTPUT

Check for Samples: SN74LVC1G125

#### **FEATURES**

- Available in the Texas Instruments NanoFree<sup>™</sup> Package
- Supports 5-V V<sub>CC</sub> Operation
- Inputs Accept Voltages to 5.5 V
- Max t<sub>pd</sub> of 3.7 ns at 3.3 V
- Low Power Consumption, 10-μA Max I<sub>CC</sub>
- ±24-mA Output Drive at 3.3 V
- I<sub>off</sub> Supports Partial-Power-Down Mode Operation

- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)



N.C. - No internal connection

See mechanical drawings for dimensions.

#### DESCRIPTION/ORDERING INFORMATION

This bus buffer gate is designed for 1.65-V to 5.5-V  $V_{CC}$  operation.

The SN74LVC1G125 is a single line driver with a 3-state output. The output is disabled when the output-enable (OE) input is high.

NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using I<sub>off</sub>. The I<sub>off</sub> circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

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Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



### **DESCRIPTION/ORDERING INFORMATION (CONTINUED)**

#### **ORDERING INFORMATION**

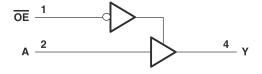
T <sub>A</sub>	PACKAGE <sup>(1)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING (2)
	NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)	Reel of 3000	SN74LVC1G125YZPR	CM
	SON – DRY	Reel of 5000	SN74LVC1G125DRYR	CM
	μQFN – DSF	Reel of 5000	SN74LVC1G125DSFR	CM
	SOT (SOT-23) – DBV	Reel of 3000	SN74LVC1G125DBVR	C25
-40°C to 85°C		Reel of 250	SN74LVC1G125DBVT	G25_
		Reel of 3000	SN74LVC1G125DCKR	
	SOT (SC-70) – DCK	Reel of 250	SN74LVC1G125DCKT	CM
	201 (00 10) 2011	Jumbo Reel of 10000	SN74LVC1G125DCKJ	o.m_
	SOT (SOT-553) – DRL	Reel of 4000	SN74LVC1G125DRLR	CM_

- (1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.
- (2) DBV/DCK/DRL'DRY: The actual top-side marking has one additional character that designates the assembly/test site. YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, = Pb-free).

**Table 1. FUNCTION TABLE** 

INPU	JTS	OUTPUT
ŌĒ	Α	Y
L	Н	Н
L	L	L
Н	Χ	Z

### **LOGIC DIAGRAM (POSITIVE LOGIC)**



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### **ABSOLUTE MAXIMUM RATINGS**(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range		-0.5	6.5	V
VI	Input voltage range <sup>(2)</sup>		-0.5	6.5	V
Vo	Voltage range applied to any output in the	he high-impedance or power-off state (2)	-0.5	6.5	V
Vo	Voltage range applied to any output in the	he high or low state <sup>(2)</sup> (3)	-0.5	V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0		-50	mA
lok	Output clamp current	V <sub>O</sub> < 0		-50	mA
lo	Continuous output current			±50	mA
	Continuous current through V <sub>CC</sub> or GND	)		±100	mA
		DBV package		206	
		DCK package		252	
$\theta_{JA}$	Package thermal impedance (4)	DRL package		142	°C/W
		DRY package		234	
		YZP package		132	
T <sub>stg</sub>	Storage temperature range		-65	150	°C

<sup>(1)</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

<sup>(2)</sup> The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

<sup>3)</sup> The value of V<sub>CC</sub> is provided in the recommended operating conditions table.

<sup>(4)</sup> The package thermal impedance is calculated in accordance with JESD 51-7.



### RECOMMENDED OPERATING CONDITIONS(1)

$V_{CC} = 1.65 \text{ V} \\ V_{CC} = 2.3 \text{ V} \\ V_{CC} = 3 \text{ V} \\ V_{CC} = 4.5 \text{ V} \\ V_{CC} = 4.5 \text{ V} \\ V_{CC} = 2.3 \text{ V} \\ O_{CC} = 3.3 \text{ V} \\ O_{CC} = 4.5 \text{ V} \\ O_{CC} = 3.3 \text{ V} \\ O_{CC} $				MIN	MAX	UNIT		
Data retention only   1.5   V <sub>CC</sub> = 1.65 V to 1.95 V   0.65 × V <sub>CC</sub>   V <sub>CC</sub> = 2.3 V to 2.7 V   1.7   V <sub>CC</sub> = 3.0 to 3.6 V   0.7 × V <sub>CC</sub>   V <sub>CC</sub> = 2.3 V to 5.5 V   0.7 × V <sub>CC</sub>   V <sub>CC</sub> = 2.3 V to 5.5 V   0.7 × V <sub>CC</sub>   V <sub>CC</sub> = 2.3 V to 5.5 V   0.7 × V <sub>CC</sub>   V <sub>CC</sub> = 2.3 V to 5.5 V   0.7 × V <sub>CC</sub>   V <sub>CC</sub> = 2.3 V to 5.5 V   0.7 × V <sub>CC</sub>   V <sub>CC</sub> = 2.3 V to 5.5 V   0.35 × V <sub>CC</sub>   V <sub>CC</sub> = 3.0 V to 5.5 V   0.35 × V <sub>CC</sub>   V <sub>CC</sub> = 3.0 V to 5.5 V   0.3 × V <sub>CC</sub>   V <sub>CC</sub> = 3.0 V to 5.5 V   0.3 × V <sub>CC</sub>   V <sub>CC</sub> = 3.0 V to 5.5 V   0.3 × V <sub>CC</sub>   V <sub>CC</sub> = 3.0 V to 5.5 V   0.3 × V <sub>CC</sub>   V <sub>CC</sub> = 2.3 V   V <sub>CC</sub> = 2.3 V   0.7 × V <sub>CC</sub>   V <sub>CC</sub> = 2.3 V   0.7 × V <sub>CC</sub>   V <sub>CC</sub> = 2.3 V   0.7 × V <sub>CC</sub>   V <sub>CC</sub> = 3.0 V   0.7 × V <sub>CC</sub>   V <sub>CC</sub> = 2.3 V   0.7 × V <sub>CC</sub>   V <sub>CC</sub> = 2.3 V   0.7 × V <sub>CC</sub>   V <sub>CC</sub> = 2.3 V   0.7 × V <sub>CC</sub>   V <sub>CC</sub> = 2.3 V   0.7 × V <sub>CC</sub>   0.7 × V <sub>CC</sub>   V <sub>CC</sub> = 2.3 V   0.7 × V <sub>CC</sub>   0.7 × V <sub>CC</sub>	.,	Overally and to an	Operating	1.65	5.5			
$V_{\text{III}}  \text{High-level input voltage}  \begin{array}{c ccccccccccccccccccccccccccccccccccc$	vcc	Supply voltage	Data retention only	1.5		V		
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$			V <sub>CC</sub> = 1.65 V to 1.95 V	0.65 × V <sub>CC</sub>				
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	. ,	LP ob Java Parant value	V <sub>CC</sub> = 2.3 V to 2.7 V	1.7		.,		
$V_{IL} \  \   \text{Low-level input voltage} \  \   \begin{array}{c ccccccccccccccccccccccccccccccccccc$	VIH	High-level input voltage	V <sub>CC</sub> = 3 V to 3.6 V	2		V		
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$			V <sub>CC</sub> = 4.5 V to 5.5 V	0.7 × V <sub>CC</sub>				
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$			V <sub>CC</sub> = 1.65 V to 1.95 V		0.35 × V <sub>CC</sub>			
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	. ,	Law Israel Country alterna	V <sub>CC</sub> = 2.3 V to 2.7 V		0.7	.,		
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	VIL	Low-level input voltage	V <sub>CC</sub> = 3 V to 3.6 V		0.8	V		
$V_{CC} = 1.65 \text{ V} \\ V_{CC} = 2.3 \text{ V} \\ V_{CC} = 3 \text{ V} \\ V_{CC} = 4.5 \text{ V} \\ V_{CC} = 4.5 \text{ V} \\ V_{CC} = 2.3 \text{ V} \\ O_{CC} = 3.3 \text{ V} \\ O_{CC} = 4.5 \text{ V} \\ O_{CC} = 3.3 \text{ V} \\ O_{CC} $			V <sub>CC</sub> = 4.5 V to 5.5 V		0.3 × V <sub>CC</sub>			
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	V <sub>I</sub>	Input voltage		0	5.5	V		
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	Vo	Output voltage		0	$V_{CC}$	V		
High-level output current			V <sub>CC</sub> = 1.65 V		-4			
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$			V <sub>CC</sub> = 2.3 V		-8			
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	Юн	High-level output current	nh-level output current		-16	mA		
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$			$V_{CC} = 3 \text{ V}$		-24			
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$			V <sub>CC</sub> = 4.5 V		-32			
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$			V <sub>CC</sub> = 1.65 V		4			
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$			V <sub>CC</sub> = 2.3 V		8			
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	$I_{OL}$	Low-level output current	V 0V		16	mA		
$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}, 2.5 \text{ V} \pm 0.2 \text{ V}$ $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$ 20  NSΛ			$V_{CC} = 3 \text{ V}$		24			
$\Delta t/\Delta v$ Input transition rise or fall rate $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ 10 ns/ $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$ 5			V <sub>CC</sub> = 4.5 V		32			
$V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$ 5			V <sub>CC</sub> = 1.8 V ± 0.15 V, 2.5 V ± 0.2 V		20			
	Δt/Δν	Input transition rise or fall rate	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		10	ns/V		
Γ <sub>A</sub> Operating free-air temperature –40 85 °C			$V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$		5	5		
	T <sub>A</sub>	Operating free-air temperature		-40	85	°C		

<sup>(1)</sup> All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

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#### **ELECTRICAL CHARACTERISTICS**

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>cc</sub>	MIN	TYP <sup>(1)</sup>	MAX	UNIT
	$I_{OH} = -100 \ \mu A$	1.65 V to 5.5 V	V <sub>CC</sub> - 0.1			
	$I_{OH} = -4 \text{ mA}$	1.65 V	1.2			
	$I_{OH} = -8 \text{ mA}$	2.3 V	1.9			V
V <sub>OH</sub>	$I_{OH} = -16 \text{ mA}$	2 \/	2.4			V
	$I_{OH} = -24 \text{ mA}$	3 V	2.3			
	$I_{OH} = -32 \text{ mA}$	4.5 V	3.8			
	$I_{OL} = 100 \mu A$	1.65 V to 5.5 V			0.1	
	I <sub>OL</sub> = 4 mA	1.65 V			0.45	
V	$I_{OL} = 8 \text{ mA}$	2.3 V			0.3	V
$V_{OL}$	I <sub>OL</sub> = 16 mA	3 V			0.4	V
	I <sub>OL</sub> = 24 mA	3 V			0.55	
	I <sub>OL</sub> = 32 mA	4.5 V			0.55	
I <sub>I</sub> A or $\overline{\text{OE}}$ inputs	V <sub>I</sub> = 5.5 V or GND	0 to 5.5 V			±5	μΑ
I <sub>off</sub>	$V_I$ or $V_O = 5.5 \text{ V}$	0			±10	μA
I <sub>OZ</sub>	$V_0 = 0 \text{ to } 5.5 \text{ V}$	3.6 V			10	μA
I <sub>CC</sub>	$V_I = 5.5 \text{ V or GND}, \qquad I_O = 0$	1.65 V to 5.5 V			10	μΑ
$\Delta I_{CC}$	One input at $V_{CC}$ – 0.6 V, Other inputs at $V_{C\ C}$ or GND	3 V to 5.5 V	·	·	500	μΑ
C <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V		4		pF

<sup>(1)</sup> All typical values are at  $V_{CC}$  = 3.3 V,  $T_A$  = 25°C.



#### **SWITCHING CHARACTERISTICS**

over recommended operating free-air temperature range,  $C_L = 15 \text{ pF}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = ± 0.1		V <sub>CC</sub> = 0.2		V <sub>CC</sub> = ± 0.3		V <sub>CC</sub> = ± 0.5		UNIT
	(INFOT)	(001701)	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	A	Υ	1.9	6.9	0.7	4.6	0.6	3.7	0.5	3.4	ns

#### **SWITCHING CHARACTERISTICS**

over recommended operating free-air temperature range,  $C_L = 30 \text{ pF}$  or 50 pF (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = ± 0.1		V <sub>CC</sub> = 1 ± 0.2		V <sub>CC</sub> = ± 0.3		V <sub>CC</sub> = ± 0.5		UNIT
	(INFOI)	(001701)	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	Α	Υ	2.8	9	1.2	5.5	1	4.5	1	4	ns
t <sub>en</sub>	ŌĒ	Υ	3.3	10.1	1.5	6.6	1	5.3	1	5	ns
t <sub>dis</sub>	ŌĒ	Y	1.3	9.2	1	5	1	5	1	4.2	ns

### **OPERATING CHARACTERISTICS**

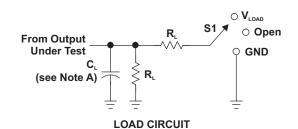
 $T_A = 25^{\circ}C$ 

	PARAMETI	ΕR	TEST CONDITIONS	V <sub>CC</sub> = 1.8 V TYP	V <sub>CC</sub> = 2.5 V TYP	V <sub>CC</sub> = 3.3 V TYP	V <sub>CC</sub> = 5 V TYP	UNIT
0	Power dissipation	Outputs enabled	f 40 MUZ	18	18	19	21	~F
$C_{pd}$	capacitance	Outputs disabled	f = 10 MHZ	2	2	2	4	pF

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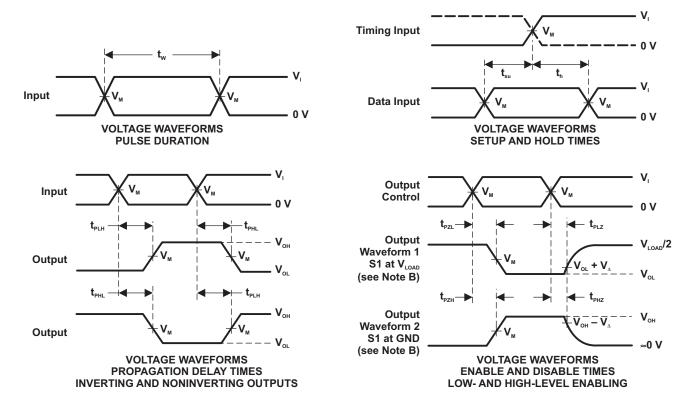


#### PARAMETER MEASUREMENT INFORMATION



TEST	S1
t <sub>PLH</sub> /t <sub>PHL</sub>	Open
t <sub>PLZ</sub> /t <sub>PZL</sub>	<b>V</b> <sub>LOAD</sub>
t <sub>PHZ</sub> /t <sub>PZH</sub>	GND

.,	IN	PUTS	.,	.,		-	.,
V <sub>cc</sub>	V,	t,/t,	V <sub>M</sub>	<b>V</b> <sub>LOAD</sub>	C <sub>L</sub>	$R_{\scriptscriptstyle L}$	V <sub>A</sub>
1.8 V ± 0.15 V	V <sub>cc</sub>	≤2 ns	V <sub>cc</sub> /2	2 × V <sub>cc</sub>	15 pF	<b>1 M</b> Ω	0.15 V
2.5 V ± 0.2 V	$V_{cc}$	≤2 ns	V <sub>cc</sub> /2	2 × V <sub>cc</sub>	15 pF	1 M $\Omega$	0.15 V
3.3 V ± 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	15 pF	1 M $\Omega$	0.3 V
5 V ± 0.5 V	$V_{cc}$	≤2.5 ns	V <sub>cc</sub> /2	2 × V <sub>cc</sub>	15 pF	1 M $\Omega$	0.3 V



NOTES: A.  $C_L$  includes probe and jig capacitance.

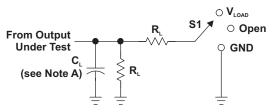
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_o = 50 \Omega$ .
- D. The outputs are measured one at a time, with one transition per measurement.
- E.  $t_{\text{PLZ}}$  and  $\dot{t}_{\text{PHZ}}$  are the same as  $t_{\text{dis}}$ .
- F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
- G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
- H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

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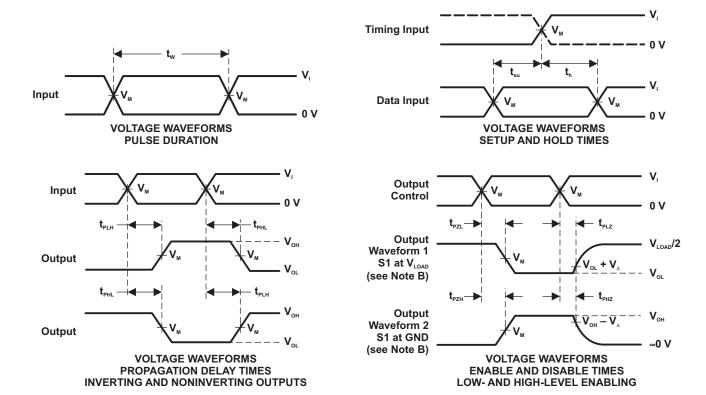
#### PARAMETER MEASUREMENT INFORMATION (continued)



TEST	S1
t <sub>PLH</sub> /t <sub>PHL</sub>	Open
$t_{_{\mathrm{PLZ}}}/t_{_{\mathrm{PZL}}}$	<b>V</b> <sub>LOAD</sub>
t <sub>PHZ</sub> /t <sub>PZH</sub>	GND

ΔΙΙ	2	TILLE

.,	INI	PUTS	.,	.,		_	.,
V <sub>cc</sub>	V,	t,/t,	V <sub>M</sub>	<b>V</b> <sub>LOAD</sub>	C <sub>L</sub>	R <sub>⊾</sub>	V <sub>A</sub>
1.8 V ± 0.15 V	V <sub>cc</sub>	≤2 ns	V <sub>cc</sub> /2	2 × V <sub>cc</sub>	30 pF	<b>1 k</b> Ω	0.15 V
2.5 V ± 0.2 V	V <sub>cc</sub>	≤2 ns	V <sub>cc</sub> /2	2 × V <sub>cc</sub>	30 pF	500 Ω	0.15 V
3.3 V ± 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
5 V ± 0.5 V	V <sub>cc</sub>	≤2.5 ns	V <sub>cc</sub> /2	2 × V <sub>cc</sub>	50 pF	500 Ω	0.3 V



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_{\odot}$  = 50  $\Omega$ .
- D. The outputs are measured one at a time, with one transition per measurement.
- E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
- G.  $t_{\text{PLH}}$  and  $t_{\text{PHL}}$  are the same as  $t_{\text{pd}}$ .
- H. All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms



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### **REVISION HISTORY**

Changes from Revision O (February 2007) to Revision P	Page
Added DSF package option to datasheet.	1
Changes from Revision P (March 2012) to Revision Q	Page
Added Jumbo Reel to ORDERING INFORMATION TABLE.	2

Product Folder Links: SN74LVC1G125





26-Mar-2013

#### **PACKAGING INFORMATION**

Orderable Device	Status	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Top-Side Markings	Samples
74LVC1G125DBVRE4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(C252 ~ C255 ~ C25F ~ C25K ~ C25R ~ C25T)	Samples
74LVC1G125DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(C252 ~ C255 ~ C25F ~ C25K ~ C25R ~ C25T)	Samples
74LVC1G125DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(C255 ~ C25F ~ C25K ~ C25R)	Samples
74LVC1G125DCKRE4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(CM5 ~ CMF ~ CMK ~ CMR ~ CMT)	Samples
74LVC1G125DCKRG4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(CM5 ~ CMF ~ CMK ~ CMR ~ CMT)	Samples
74LVC1G125DCKTE4	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(CM5 ~ CMF ~ CMK ~ CMR ~ CMT)	Samples
74LVC1G125DCKTG4	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(CM5 ~ CMF ~ CMK ~ CMR ~ CMT)	Samples
74LVC1G125DRLRG4	ACTIVE	SOT	DRL	5	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(CM7 ~ CMR)	Samples
74LVC1G125DRYRG4	ACTIVE	SON	DRY	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	СМ	Samples
74LVC1G126DBVTE4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(C265 ~ C26F ~ C26K ~ C26R)	Samples
SN74LVC1G125DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(C252 ~ C255 ~ C25F ~ C25K ~ C25R ~ C25T)	Samples
SN74LVC1G125DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(C255 ~ C25F ~ C25K ~ C25R)	Samples
SN74LVC1G125DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(CM5 ~ CMF ~ CMK ~ CMR ~ CMT)	Samples
SN74LVC1G125DCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(CM5 ~ CMF ~ CMK ~ CMR ~ CMT)	Samples
SN74LVC1G125DRLR	ACTIVE	SOT	DRL	5	4000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(CM7 ~ CMR)	Samples
SN74LVC1G125DRYR	ACTIVE	SON	DRY	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	СМ	Samples



### PACKAGE OPTION ADDENDUM

26-Mar-2013

Orderable Device	Status	Package Type	_	Pins	_	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Top-Side Markings	Samples
	(1)		Drawing		Qty	(2)		(3)		(4)	
SN74LVC1G125DSFR	ACTIVE	SON	DSF	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	СМ	Samples
SN74LVC1G125YZPR	ACTIVE	DSBGA	YZP	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	(CM2 ~ CM7 ~ CMN)	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free** (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes. **Pb-Free** (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between

the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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#### OTHER QUALIFIED VERSIONS OF SN74LVC1G125:

Automotive: SN74LVC1G125-Q1



### **PACKAGE OPTION ADDENDUM**

26-Mar-2013

● Enhanced Product: SN74LVC1G125-EP

NOTE: Qualified Version Definitions:

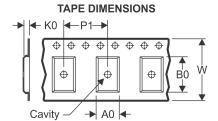
- Automotive Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product Supports Defense, Aerospace and Medical Applications

### PACKAGE MATERIALS INFORMATION

www.ti.com 17-Jan-2013

### TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



#### \*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC1G125DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G125DBVR	SOT-23	DBV	5	3000	178.0	9.2	3.3	3.2	1.55	4.0	8.0	Q3
SN74LVC1G125DBVR	SOT-23	DBV	5	3000	180.0	9.2	3.17	3.23	1.37	4.0	8.0	Q3
SN74LVC1G125DBVT	SOT-23	DBV	5	250	178.0	9.2	3.3	3.2	1.55	4.0	8.0	Q3
SN74LVC1G125DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G125DCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G125DCKR	SC70	DCK	5	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74LVC1G125DCKR	SC70	DCK	5	3000	180.0	9.2	2.3	2.55	1.2	4.0	8.0	Q3
SN74LVC1G125DCKT	SC70	DCK	5	250	180.0	9.2	2.3	2.55	1.2	4.0	8.0	Q3
SN74LVC1G125DCKT	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G125DCKT	SC70	DCK	5	250	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74LVC1G125DRLR	SOT	DRL	5	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
SN74LVC1G125DRLR	SOT	DRL	5	4000	180.0	9.5	1.78	1.78	0.69	4.0	8.0	Q3
SN74LVC1G125DRYR	SON	DRY	6	5000	179.0	8.4	1.2	1.65	0.7	4.0	8.0	Q1
SN74LVC1G125DSFR	SON	DSF	6	5000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
SN74LVC1G125YZPR	DSBGA	YZP	5	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1

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\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC1G125DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74LVC1G125DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74LVC1G125DBVR	SOT-23	DBV	5	3000	205.0	200.0	33.0
SN74LVC1G125DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
SN74LVC1G125DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
SN74LVC1G125DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
SN74LVC1G125DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
SN74LVC1G125DCKR	SC70	DCK	5	3000	205.0	200.0	33.0
SN74LVC1G125DCKT	SC70	DCK	5	250	205.0	200.0	33.0
SN74LVC1G125DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74LVC1G125DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74LVC1G125DRLR	SOT	DRL	5	4000	202.0	201.0	28.0
SN74LVC1G125DRLR	SOT	DRL	5	4000	180.0	180.0	30.0
SN74LVC1G125DRYR	SON	DRY	6	5000	203.0	203.0	35.0
SN74LVC1G125DSFR	SON	DSF	6	5000	180.0	180.0	30.0
SN74LVC1G125YZPR	DSBGA	YZP	5	3000	220.0	220.0	35.0

# DBV (R-PDSO-G5)

## PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
  - D. Falls within JEDEC MO-178 Variation AA.



# DBV (R-PDSO-G5)

## PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.



# DCK (R-PDSO-G5)

# PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Falls within JEDEC MO-203 variation AA.



# DCK (R-PDSO-G5)

## PLASTIC SMALL OUTLINE



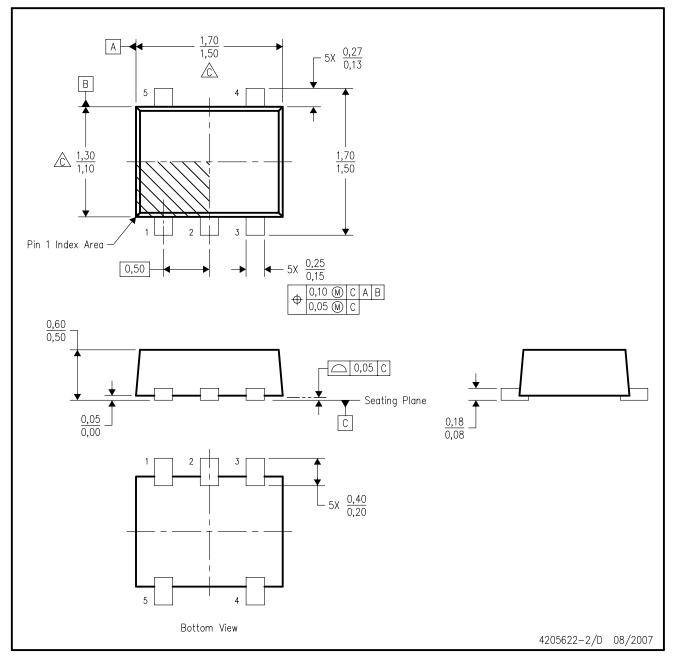
NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.



# DRL (R-PDSO-N5)

# PLASTIC SMALL OUTLINE



NOTES:

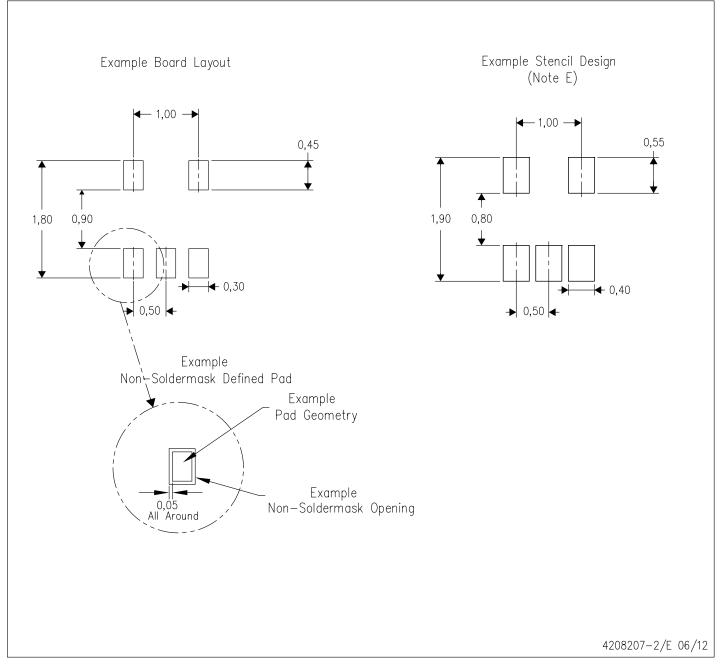
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
- B. This drawing is subject to change without notice.
- Body dimensions do not include mold flash, interlead flash, protrusions, or gate burrs.

  Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0,15 per end or side.
- D. JEDEC package registration is pending.



# DRL (R-PDSO-N5)

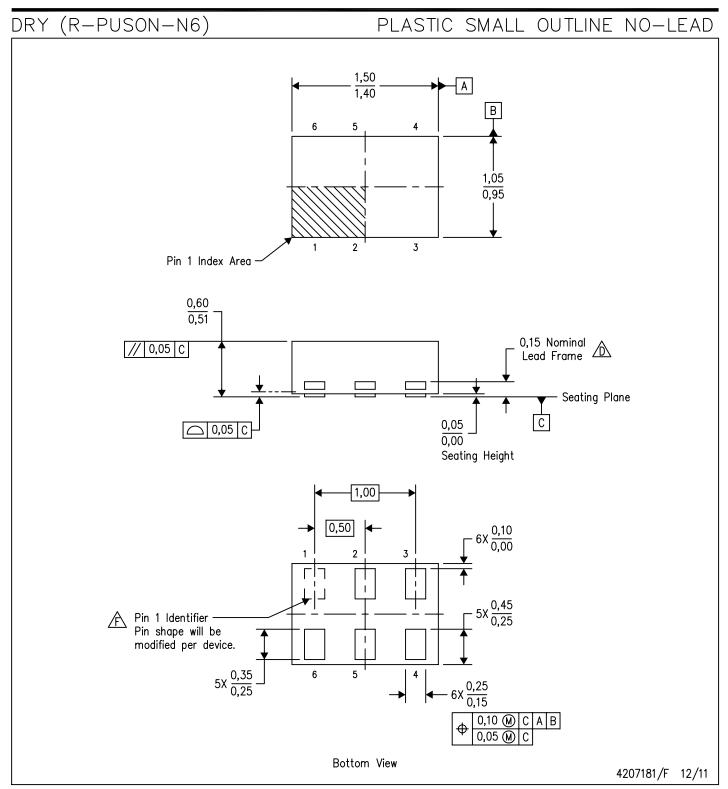
### PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
- E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
- F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- G. Side aperture dimensions over—print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.





NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. SON (Small Outline No-Lead) package configuration.

The exposed lead frame feature on side of package may or may not be present due to alternative lead frame designs.

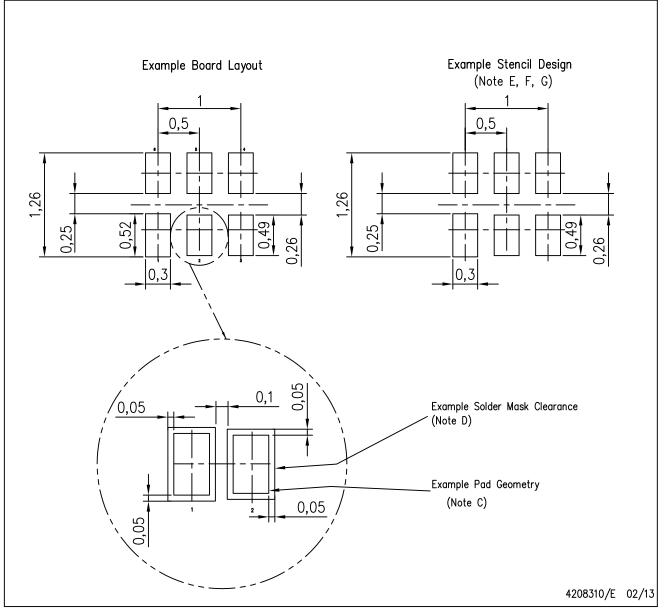
E. This package complies to JEDEC MO-287 variation UFAD.

 $frac{f}{K}$  See the additional figure in the Product Data Sheet for details regarding the pin 1 identifier shape.



### DRY (R-PUSON-N6)

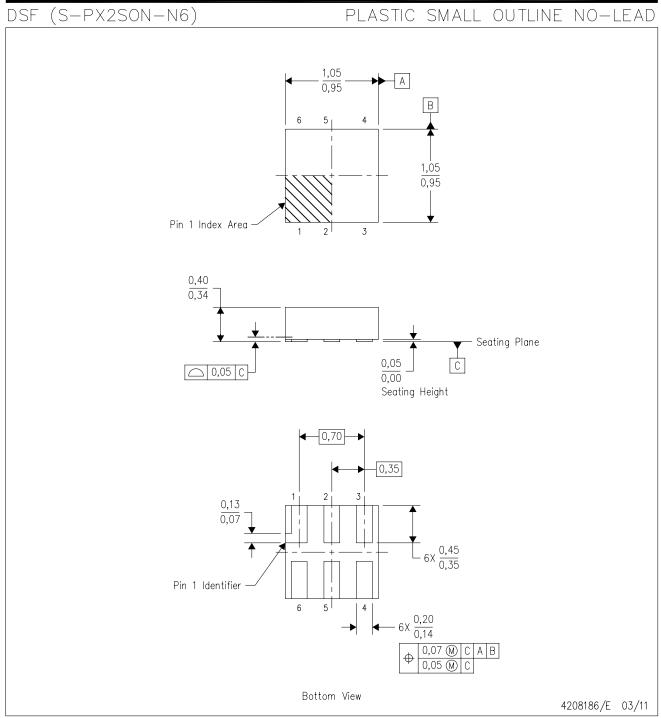
### PLASTIC SMALL OUTLINE NO-LEAD



NOTES: A.

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
- E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
- F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- G. Side aperture dimensions over—print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.





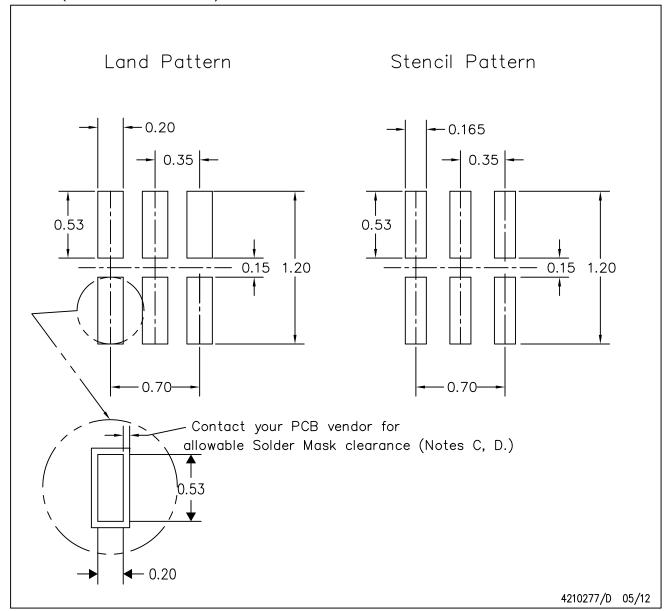
NOTES: All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.

- B. This drawing is subject to change without notice.
  C. SON (Small Outline No-Lead) package configuration.
  D. This package complies to JEDEC MO-287 variation X2AAF.



DSF (S-PX2SON-N6)

PLASTIC SMALL OUTLINE NO-LEAD



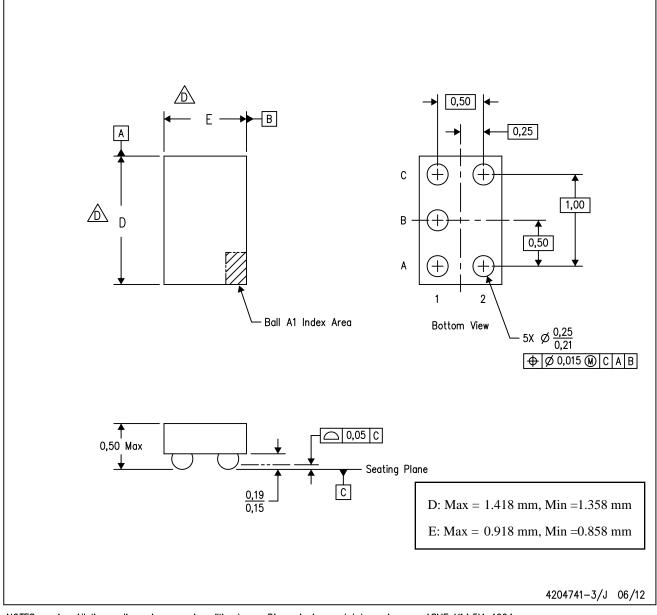
NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads. If 2 mil solder mask is outside PCB vendor capability, it is advised to omit solder mask.
- E. Maximum stencil thickness 0,1016 mm (4 mils). All linear dimensions are in millimeters.
- F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- G. Suggest stencils cut with lasers such as Fiber Laser that produce the greatest positional accuracy.
- H. Component placement force should be minimized to prevent excessive paste block deformation.



YZP (R-XBGA-N5)

DIE-SIZE BALL GRID ARRAY



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.

- B. This drawing is subject to change without notice.
- C. NanoFree™ package configuration.
- The package size (Dimension D and E) of a particular device is specified in the device Product Data Sheet version of this drawing, in case it cannot be found in the product data sheet please contact a local TI representative.
- E. This package is a Pb-free solder ball design. Refer to the 5 YEP package (drawing 4204725) for tin-lead (SnPb).

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**Телефон:** 8 (812) 309 58 32 (многоканальный)

Факс: 8 (812) 320-02-42

Электронная почта: org@eplast1.ru

Адрес: 198099, г. Санкт-Петербург, ул. Калинина,

дом 2, корпус 4, литера А.