TOSHIBA Field Effect Transistor Silicon N Channel MOS Type (U-MOS III)

SSM3K15ACT

Load Switching Applications

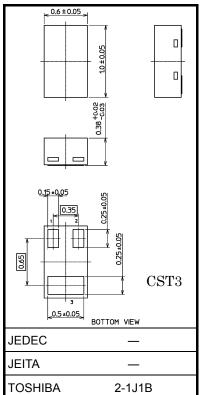
- 2.5 V drive
- Low ON-resistance: $R_{DS(ON)} = 3.6 \Omega \text{ (max)} (@V_{GS} = 4 \text{ V})$ $R_{DS(ON)} = 6.0 \Omega \text{ (max)} (@V_{GS} = 2.5 \text{ V})$

Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit	
Drain-Source voltage		V _{DSS}	30	V	
Gate-Source voltage		V _{GSS}	±20	V	
Drain current	DC	I _D	100	mA	
	Pulse	I _{DP}	400		
Power dissipation		P _D (Note 1)	100	mW	
Channel temperature		T _{ch}	150	°C	
Storage temperature range		T _{stg}	–55 to 150	°C	

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

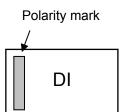


Weight: 0.75 mg (typ.)

Note 1: Mounted on FR4 board

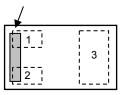
 $(10 \text{ mm} \times 10 \text{ mm} \times 1.0 \text{ mm}, \text{Cu Pad: } 100 \text{ mm}^2)$

Marking (Top View)



Pin Condition (Top View)

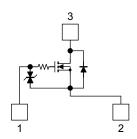
Polarity mark (on the top)



- 1. Gate
- 2. Source
- 3. Drain

*Electrodes: On the bottom

Equivalent Circuit



Start of commercial production 2010-11



Electrical characteristics (Ta = 25°C)

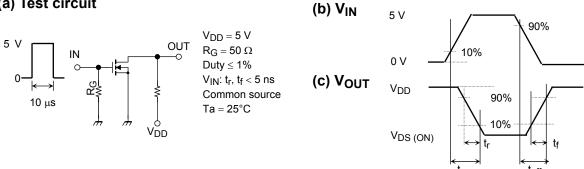
Chara	cteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Drain-Source breakdown voltage		V (BR) DSS	$I_D = 0.1 \text{ mA}, V_{GS} = 0 \text{ V}$	30	_	_	v
		V (BR) DSX	$I_D = 0.1 \text{ mA}, V_{GS} = -10 \text{ V}$ (Note 3)	16		_	v
Drain cut-off curren	ıt	I _{DSS}	$V_{DS} = 30 \text{ V}, \text{ V}_{GS} = 0 \text{ V}$	_		1	μA
Gate leakage curre	ent	I _{GSS}	$V_{GS} = \pm 16 \text{ V}, \text{ V}_{DS} = 0 \text{ V}$	_		±1	μA
Gate threshold volt	age	V _{th}	$V_{DS} = 3 \text{ V}, \text{ I}_{D} = 0.1 \text{ mA}$	0.8		1.5	V
Forward transfer ac	dmittance	Y _{fs}	$V_{DS} = 3 \text{ V}, \text{ I}_{D} = 10 \text{ mA} \qquad (\text{Note 2})$	35		_	mS
Drain-Source ON-resistance		R _{DS (ON)}	$I_D = 10 \text{ mA}, V_{GS} = 4 \text{ V}$ (Note 2)	_	2.3	3.6	Ω
			$I_D = 10 \text{ mA}, V_{GS} = 2.5 \text{ V}$ (Note 2)	_	3.5	6.0	
Input capacitance		C _{iss}	V _{DS} = 3 V, V _{GS} = 0 V, f = 1 MHz		13.5		pF
Output capacitance Reverse transfer capacitance		C _{oss}			8.0		
		C _{rss}			6.5	_	
Switching time	Turn-on time	t _{on}	$V_{DD} = 5 \text{ V}, \text{ I}_D = 10 \text{ mA}$ $V_{GS} = 0 \text{ to } 5 \text{ V}, \text{ R}_G = 50 \Omega$		5.5	_	ns
	Turn-off time	t _{off}			35	_	
Drain-source forward voltage		V _{DSF}	$I_D = -100 \text{ mA}, V_{GS} = 0 \text{ V}$ (Note 2)	—	-0.85	-1.2	V

Note 2: Pulse test

Note 3: If a reverse bias is applied between gate and source, this device enters V(BR)DSX mode. Note that the drain-source breakdown voltage is lowered in this mode.

Switching Time Test Circuit

(a) Test circuit



Precaution

Vth can be expressed as voltage between gate and source when low operating current value is ID = 0.1 mA for this product. For normal switching operation, V_{GS} (on) requires higher voltage than V_{th} and V_{GS} (off) requires lower voltage than V_{th}. (Relationship can be established as follows: $V_{GS (off)} < V_{th} < V_{GS (on)}$)

Please take this into consideration for using the device.

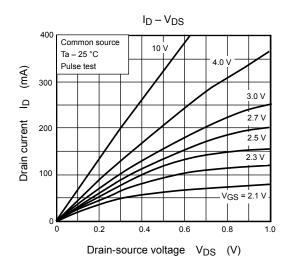
Do not use this device under avalanche mode. It may cause the device to break down.

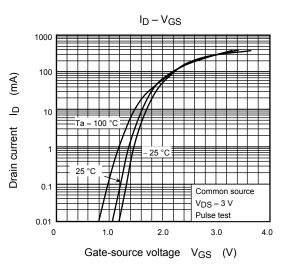
Handling Precaution

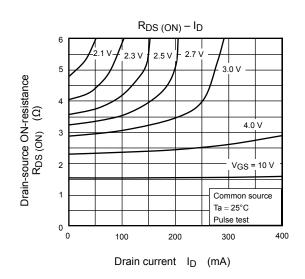
When handling individual devices (which are not yet mounting on a circuit board), be sure that the environment is protected against electrostatic electricity. Operators should wear anti-static clothing, and containers and other objects that come into direct contact with devices should be made of anti-static materials.

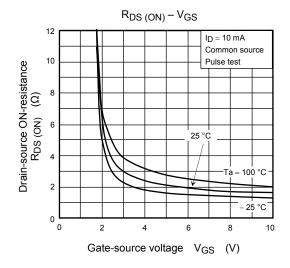
Thermal resistance Rth (ch-a) and power dissipation PD vary depending on board material, board area, board thickness and pad area. When using this device, please take heat dissipation into consideration

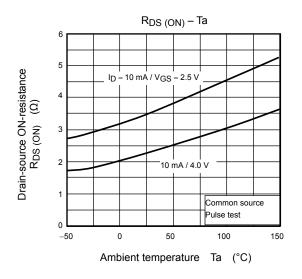
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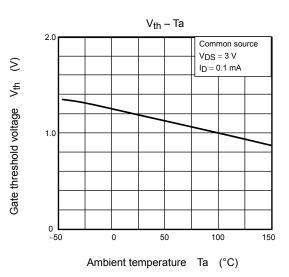




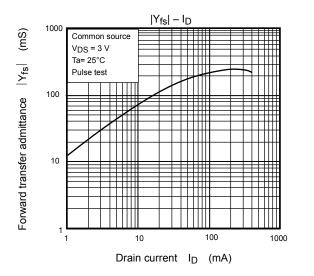


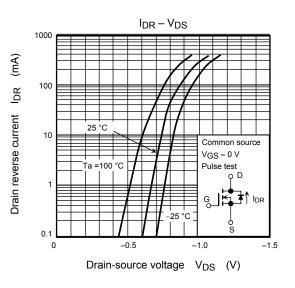


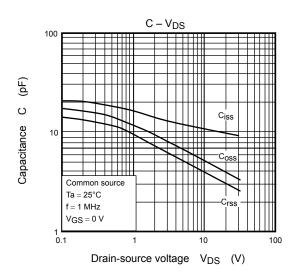


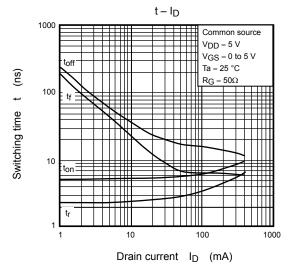


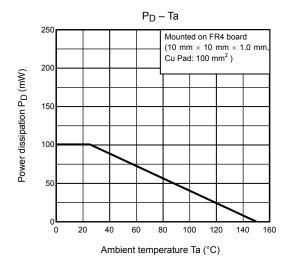
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