Document Number: MC34845
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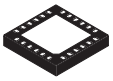
Low cost six channel led backlight driver with integrated power supply

34845

LED DRIVER



98ASA00602D
24-PIN QFN-EP

The 34845 series represents high efficiency LED drivers for use in backlighting LCD displays from 10” to 17”. Operating from supplies of 5.0 V to 21 V, the 34845 series is capable of driving up to 16 LEDs in series in six separate strings. The LED current tolerance in the six strings is within ±2% maximum and is set using a resistor to GND.

PWM dimming is performed by applying a PWM input signal to the PWM pin which modulates the LED channels directly. An Enable Pin (EN) provides for low power standby. Alternatively, a single wire scheme selects power down when PWM is connected to the Wake pin and held low.

The integrated boost converter uses dynamic headroom control to automatically set the output voltage. There are three device versions for boost frequency; 34845C is 600 kHz, and the 34845D is 300 kHz. External compensation allows the use of different inductor/ capacitor combinations.

The 34845 includes fault protection modes for LED short and open, overtemperature, overcurrent and overvoltage errors. It features an internally fixed OVP value of 60 V (typical) which protects the device in the event of a failure in the externally programmed OVP. The OVP level can be set by using an external resistor divider. This device is powered using SMARTMOS technology.

Features

- Input voltage of 5.0 V to 21 V
- Boost output voltage up to 60 V
- 2.0 A integrated boost FET
- Fixed boost frequency - 300 kHz or 600 kHz
- OTP, OCP, UVLO fault detection
- LED short/open protection
- Programmable LED current between 3.0 mA and 30 mA

Applications

- PC notebooks
- Netbooks
- GPS screens
- Portable DVD players
- Picture frames
- Smaller screen televisions
- Industrial/instrumentation displays
- Health care device displays

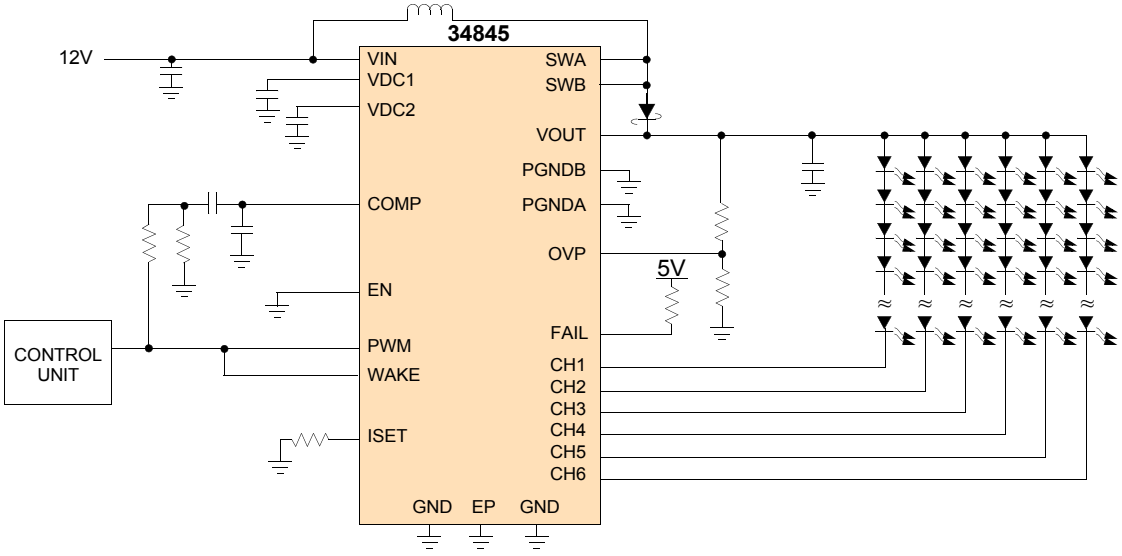


Figure 1. 34845 simplified application diagram

1 Orderable parts

Table 1. Device variations

Part number [1]	Temperature (T_A)	Package	Boost switch current limit I_{BOOST_LIMIT} (A)			Switching frequency f_S (kHz)			Slope compensation V_{SLOPE} (V/µs)		
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.
MC34845CEP	-40 to 85 °C	24 QFN-EP	1.9	2.1	2.3	540	600	660	-	0.52	-
MC34845DEP			2.1	2.35	2.6	270	300	330		0.22	

Notes

1. To order parts in Tape and Reel, add the R2 suffix to the part number.

2 Internal block diagram

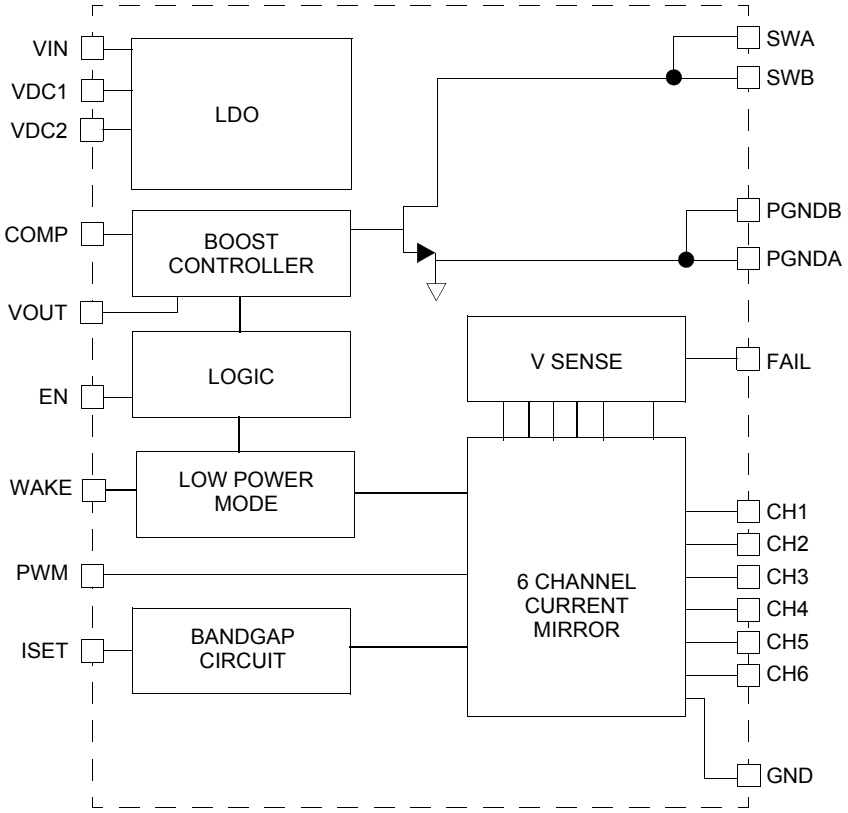


Figure 2. 34845 simplified internal block diagram

3 Pin connections

3.1 Pinout diagram

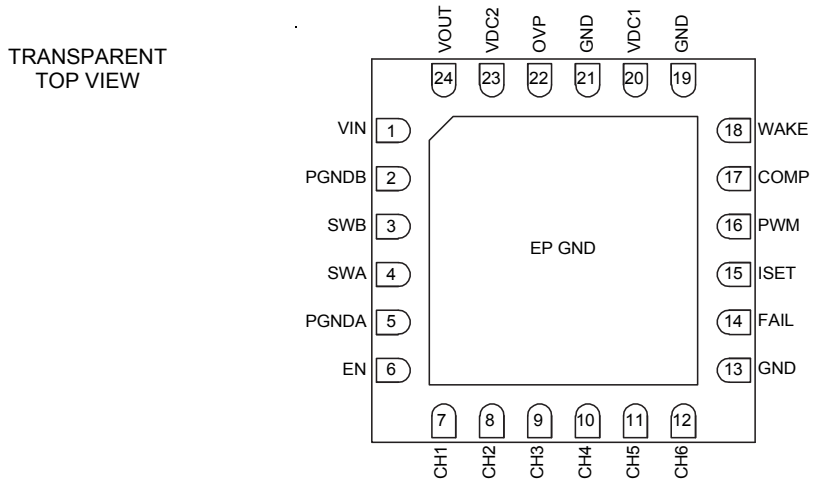


Figure 3. 34845 pin connections

3.2 Pin definitions

Table 2. 34845 Pin definitions

Pin number	Pin name	Definition
1	VIN	Main voltage supply Input. IC Power input supply voltage, is used internally to produce internal voltage regulation for logic functioning, and also as an input voltage for the boost regulator.
2	PGNDB	Power ground. This is the ground pin for the internal Boost FET.
3	SWB	Boost switch node connection B. Switching node of boost converter.
4	SWA	Boost switch node connection A. Switching node of boost converter.
5	PGNDA	Power ground. This is the ground pin for the internal Boost FET.
6	EN	Enable pin (active high, internal pull-down).
7 - 12	CH1 - CH6	LED string connections 1 to 6. LED current drivers. Each line has the capability of driving up to 30 mA.
13, 19, 21	GND	Ground Reference for all internal circuits other than the Boost FET. The Exposed Pad (EP) should be used for thermal heat dissipation.
14	FAIL	Fault detected pin (open drain): • No Failure = Low-impedance pull-down • Failure = High-impedance When a fault situation is detected, this pin goes into high-impedance.
15	ISET	LED current setting. The maximum current is set using a resistor from this pin to GND.
16	PWM	External PWM control signal.
17	COMP	Boost compensation component connection. This passive pin is used to compensate the boost converter. Add a capacitor and a resistor in series to GND to stabilize the system as well as a shunt capacitor.
18	WAKE	Low power consumption mode for single wire control. This is achieved by connecting the WAKE and PWM pins together and grounding the ENABLE (EN) pin.
20	VDC1	2.5 V internal voltage decoupling. This pin is for internal use only, and not to be used for other purposes. A capacitor of 2.2 μF should be connected between this pin and ground.
22	OVP	External boost overvoltage setting. Requires a resistor divider from VOUT to GND. If no external OVP setting is desired, this pin should be grounded.

Table 2. 34845 Pin definitions (continued)

Pin number	Pin name	Definition
23	VDC2	6.0 V internal voltage decoupling. This pin is for internal use only, and not to be used for other purposes. A capacitor of 2.2 μF should be connected between this pin and ground.
24	VOUT	Boost voltage output feedback.
EP	EP	Ground and thermal enhancement pad

4 Electrical characteristics

4.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Ratings	Value	Unit	Notes
Electrical ratings				
V_{MAX}	Maximum Pin Voltages • SWA, SWB, VOUT • CH1, CH2, CH3, CH4, CH5, CH6 (Off state) • CH1, CH2, CH3, CH4, CH5, CH6 (On state) • FAIL • OVP • COMP, ISET • PWM, WAKE • EN, VIN	 -0.3 to 65 -0.3 to 45 -0.3 to 20 -0.3 to 7.0 -0.3 to 7.75 -0.3 to 2.7 -0.3 to 5.5 -0.3 to 24	V	
I_{LED_MAX}	Maximum LED Current per Channel	33	mA	
V_{ESD}	ESD Voltage Human Body Model (HBM) Machine Model (MM)	 ±2000 ±200	V	(2)
Thermal ratings				
T_A	Operating Ambient Temperature Range	-40 to 85	°C	
T_J	Maximum Junction Temperature	150	°C	
TS	Storage Temperature Range	-40 to 150	°C	
T_{PPRT}	Peak Package Reflow Temperature During Reflow	Note 4	°C	(3), (4)
$T_{\theta JA}$	Thermal Resistance Junction to Ambient	36	°C/W	(5)
$T_{\theta JC}$	Thermal Resistance Junction to Case	3.1	°C/W	(6)
P_D	Power Dissipation • T_A = 25 °C • T_A = 85 °C	 3.4 1.8	W	(5)

Notes

2. ESD testing is performed in accordance with the Human Body Model (HBM) (AEC-Q100-2) (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω), and the Machine Model (MM) (C_{ZAP} = 200 pF, R_{ZAP} = 0 Ω).
3. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
4. NXP's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), Go to www.nxp.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxxD enter 33xxx), and review parametrics.
5. Per JEDEC51-8 Standard for Multilayer PCB.
6. Theoretical thermal resistance is from the die junction to the exposed pad.

4.2 Static and dynamic electrical characteristics

Table 4. Static and dynamic electrical characteristics

Characteristics noted under conditions V_{IN} = 12 V, V_{OUT} = 35 V, I_{LED} = 30 mA, f_S = 600 kHz, f_{PWM} = 600 Hz - 40 °C ≤ T_A ≤ 85 °C, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
Supply						
V_{IN}	Supply Voltage	5.0	10	21	V	
$I_{SHUTDOWN}$	Supply Current when in Shutdown Mode • EN = Low, PWM = Low	-	2.0	10	µA	
$I_{OPERATIONAL}$	Supply Current when Operational Mode • Boost = Pulse Skipping, Channels = 1% of Duty Cycle EN = High, PWM = Low	-	5.0	6.5	mA	
UVLO	Undervoltage Lockout • V_{IN} Rising	4.0	-	4.4	V	
$UVLO_{HYST}$	Undervoltage Hysteresis • V_{IN} Falling	-	0.25	-	V	
V_{DC1}	VDC1 Voltage • C_{VDC1} = 2.2 µF	2.4	2.5	2.6	V	(7)
V_{DC2}	VDC2 Voltage (V_{IN} between 7.0 V and 21 V) • C_{VD2C} = 2.2 µF	5.7	6.0	6.3	V	(7)
Boost						
V_{OUT1} V_{OUT2}	Output Voltage Range • VIN = 5.0 V • VIN = 21 V	8.0 24	- -	43 60	V	(8)
I_{BOOST_LIMIT}	Boost Switch Current Limit • 34845C • 34845D	1.9 2.1	2.1 2.35	2.3 2.6	A	
t_{BOOST_TIME}	Boost Switch Current Limit Timeout	-	10	-	ms	
$R_{DS(on)}$	RDSON of Internal FET • I_{DRAIN}= 1.0 A	-	300	520	mW	
I_{BOOST_LEAK}	Boost Switch Off State Leakage Current • $V_{SWA,SWB}$ = 60 V	-	-	1.0	mA	
$VOUT_{LEAK}$	Feedback pin Off State Leakage Current • V_{OUT} = 60 V	-	-	500	mA	
EFF_{BOOST}	Peak Boost Efficiency • V_{OUT} = 33 V, RL = 330 Ω	-	90	-	%	(9)
I_{LED}/V_{IN}	Line Regulation • V_{IN} = 7.0 V to 21 V, I_{CH} = 30 mA	-0.2	-	0.2	%/V	
I_{LED}/V_{LED}	Load Regulation • V_{LED} = 24 V to 40 V (all Channels), I_{CH} = 30 mA	-0.2	-	0.2	%/V	
D_{MIN}	Minimum Duty Cycle	-	10	15	%	
D_{MAX}	Maximum Duty Cycle	88	90	-	%	
V_{OVP_INT}	OVP Internally Fixed Value • (no external voltage resistor divider)	56	60	64	V	

Notes

7. This output is for internal use only and not to be used for other purposes.
8. Minimum and maximum output voltages are dependent on Min/Max duty cycle condition.
9. Boost efficiency test is performed under the following conditions: f_{SW} = 600 kHz, V_{IN} = 12 V, V_{OUT} = 33 V and R_L = 330 Ω. The following external components are used: L = 10 µH, DCR = 0.1 Ω, C_{OUT} = 3x1 µF (ceramic), Schottky diode V_F = 0.35 V.

Table 4. Static and dynamic electrical characteristics (continued)

Characteristics noted under conditions V_{IN} = 12 V, V_{OUT} = 35 V, I_{LED} = 30 mA, f_S = 600 kHz, f_{PWM} = 600 Hz - 40 °C ≤ T_A ≤ 85 °C, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
Boost (continued)						
V_{OVP_EXT}	OVP Programming Range • (set through an external resistor divider)	15	-	60	V	(10)
V_{REF_OVP}	OVP Reference Voltage	6.3	6.9	7.5	V	
I_{SINK_OVP}	OVP Sink Current	-	0.2	-	µA	
f_S	Switching Frequency • 34845C • 34845D	 540 270	 600 300	 660 330	kHz	
t_{SS}	Soft Start Time (f_s = 600 kHz, 100% PWM duty)	-	3.0	-	ms	
SS_VOUT	Soft Start V_{OUT} Overshoot (f_s = 600 kHz, 100% PWM duty)	-	-	OVP	V	
BOOST_t_R	Boost Switch Rise Time	-	8.0	-	ns	
BOOST_t_F	Boost Switch Fall Time	-	6.0	-	ns	
A_{CSA}	Current sense Amplifier Gain	-	9.0	-		
G_M	OTA Transconductance	-	200	-	µS	
I_{SS}	Transconductance Sink and Source Current Capability	-	100	-	µA	
V_{SLOPE}	Slope Compensation • 34845C • 34845D	 - -	 0.52 0.22	 - -	V/µs	
LED driver						
I_{LED}	LED Driver Sink Current • R_{ISET} = 51 kΩ 0.1%, PWM = 3.3 V • R_{ISET} = 5.1 kΩ 0.1%, PWM = 3.3 V	 2.88 29.4	 3.0 30	 3.12 30.6	mA	
V_{ISET}	ISET Pin Voltage • R_{ISET} = 5.1 kΩ 0.1%	2.011	2.043	2.074	V	
V_{MIN}	Regulated Minimum Voltage Across LED Drivers • Pulse Width > 400 ns	0.675	0.75	0.825	V	
$I_{TOLERANCE}$	LED Current Channel to Channel Tolerance • 10 mA ≤ I_{LED} ≤ 30 mA • 3.0 mA ≤ I_{LED} < 10 mA	 -2.0 -4.0	 - -	 2.0 4.0	%	
I_{CH_LEAK}	Off State leakage Current, All Channels • V_{CH} = 45 V	-	-	1.0	µA	
t_R/t_F	LED Channels Rise and Fall Time	-	50	75	ns	
O_{FDV}	LED Open Protection, Channel Disabled if $V_{CH} \le O_{FDV}$	-	-	0.55	V	
S_{FDV}	LED Short Protection Voltage, Channel Disabled if $V_{CH} \ge S_{FDV}$ (channel on time ≥ 10 µs)	6.5	7.0	7.5	V	
Fail pin						
I_{FAIL_LEAK}	Off State Leakage Current • V_{FAIL} = 5.5 V	-	-	5.0	µA	
V_{OL}	On State Voltage Drop • I_{SINK} = 4.0 mA	-	-	0.4	V	
Overtemperature shutdown						
$OTT_{SHUTDOWN}$	Over-temperature Threshold (shutdown mode) • Rising • Hysteresis	 150 -	 165 25	 - -	°C	

Notes

10. The OVP level must be set 5.0 V above the worst-case LED string voltage.

Table 4. Static and dynamic electrical characteristics (continued)

Characteristics noted under conditions V_{IN} = 12 V, V_{OUT} = 35 V, I_{LED} = 30 mA, f_S = 600 kHz, f_{PWM} = 600 Hz - 40 °C ≤ T_A ≤ 85 °C, unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25 °C under nominal conditions, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
PWM input						
$PWM_{CONTROL}$	PWM Dimming Mode LED Current Control • PWM = 3.3 V, f_{PWM} = 600 Hz 10% duty; • PWM = 3.3 V, f_{PWM} = 600 Hz 50% duty • PWM = 3.3 V, f_{PWM} = 600 Hz 100% duty	 9.9 49.5 -	 10 50 100	 10.1 50.5 -	%	
t_{PWM_IN}	Input Minimum Pulse PWM Pin (V_{PWM} = 3.3 V) • Start-up (Wake mode) • Operational (Wake mode) • Start-up (Enable mode) • operational (Enable mode)	 1.6 - 0.4 -	 - 0.2 - 0.2	 - - - -	µs	
f_{PWM}	Input Frequency Range for PWM Pin	DC	-	100	kHz	
Wake						
$t_{SHUTDOWN}$	Shutdown Mode Timeout	27	30	33	ms	
Logic inputs (PWM)						
V_{ILL}	Input Low Voltage	-0.3	-	0.5	V	
V_{IHL}	Input High Voltage	1.5	-	5.5	V	
I_{SINK}	Input Current	-1.0	-	1.0	µA	
Logic inputs (EN)						
V_{ILL}	Input Low Voltage	-0.3	-	0.5	V	
V_{IHL}	Input High Voltage	2.1	-	21	V	
I_{SINK}	Input Current (V_{EN} = 12 V)	-	6.0	10	µA	
Logic inputs (Wake)						
V_{ILL}	Input Low Voltage	-0.3	-	0.5	V	
V_{IHL}	Input High Voltage	2.1	-	5.5	V	
I_{SINK}	Input Current	-1.0	-	1.0	µA	

5 Functional description

5.1 Introduction

LED backlighting has been popular for use in small LCD displays for many years. This technology is now rapidly replacing the incumbent Cold Cathode Fluorescent Lamp (CCFL) in mid-size displays such as those used use in notebooks, monitors, and industrial/ consumer displays. LEDs offer a number of advantages compared to the CCFL, including lower power, thinner, longer lifetime, low voltage drive, accurate wide-range dimming control, and advanced architectures for improved image quality. LEDs are also void of hazardous materials such as mercury which is used in CCFL.

LED backlights use different architecture depending on the size of the display and features required. For displays in the 10” to 17” + range such as those used in notebooks, edge-lit backlights offer very thin designs down to 2.0 mm or less. The efficiency of the LED backlight also extends battery life in portable equipment compared to CCFL. In large size panels, direct backlights support advanced architectures such as local dimming, in which power consumption and contrast ratio are drastically improved. Edge lighting can also be used in large displays when low cost is the driving factor.

The 34845 targets mid size panel applications in the 10” to 17” + range with edge-lit backlights. The device supports LED currents up to 30 mA and supports up to six strings of LEDs. This enables backlights up to 10 W to be driven from a single device. The device includes a boost converter to deliver the required LED voltage from either a two or three cell Li-ion battery, or a direct 12 V input supply. The current drivers match the current between devices to provide superior uniformity across the display. The 34845 provides for a wide range of PWM dimming from a direct PWM control input.

5.2 Functional device operation

5.2.1 Power supply

The 34845 supports 5.0 V to 21 V at the VIN input pin. Two internal regulators generate internal rails for internal operation. Both rails are de-coupled using capacitors on the VDC1 and VDC2 pins. The VIN, VDC1, and VDC2 supplies each have their own UVLO mechanisms. When any voltage is below the UVLO threshold, the device stops operating. All UVLO comparators have hysteresis to ensure constant on/off cycling does not occur.

The power up sequence for applying V_{IN} respect to the ENABLE and PWM signals is important since the 34845 device behaves differently depending on how the sequence of these signals is applied. For the case where VIN is applied before the ENABLE and PWM signals, the device has no limitation in terms of how fast the V_{IN} ramp should be. However for the case where the PWM and ENABLE signals are applied before V_{IN}, the ramp up time of V_{IN} between 0 V and 5.0 V should be no longer than 2.0 ms. Figure 4 and Figure 5 illustrate the two different power up conditions.

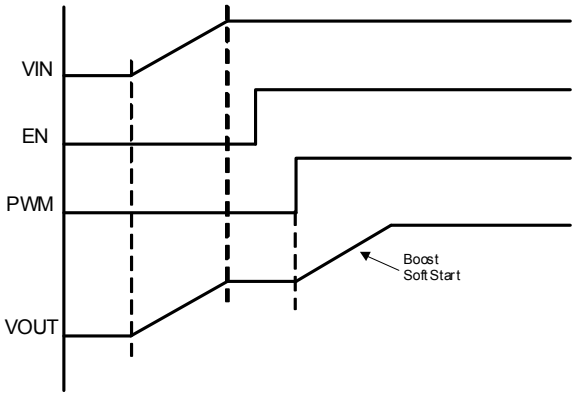


Figure 4. Power up sequence case 1, VIN applied before the ENABLE and PWM signals. No limitation for VIN ramp up time.

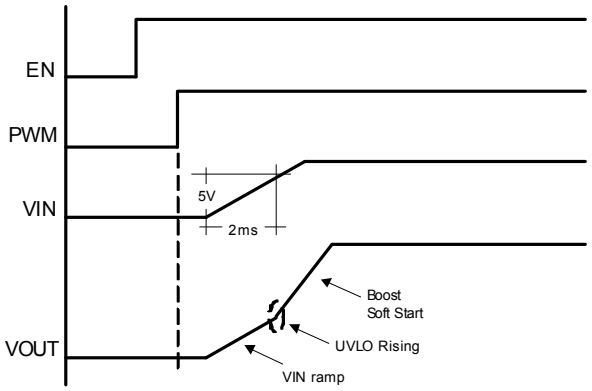


Figure 5. Power up sequence case 2, VIN applied after the ENABLE and PWM signals. VIN ramp up time between 0 V and 5.0 V should be not higher than 2.0 ms

5.2.2 Boost converter

The boost converter uses a Dynamic Headroom Control (DHC) loop to automatically set the output voltage needed to drive the LED strings. The DHC is designed to operate under specific pulse width conditions in the LED drivers. It operates for pulse widths higher than 400 ns. If the pulse widths are shorter than specified, the DHC circuit does not operate and the voltage across the LED drivers increase to a value given by the OVP, minus the total LED voltage in the LED string. It is therefore imperative to select the proper OVP level to avoid exceeding the max off state voltage of the LED drivers (45 V).

The boost operates in current mode and is compensated externally through a type 2 network on the COMP pin. A modification of the compensation network is suggested to minimize the amplitude of the ripple at V_{OUT}. The details of the suggested compensation network are shown in Figure 10 and Figure 11.

An integrated 2.0 A minimum FET supplies the required output current. An overcurrent protection circuit limits the output current cycle-by-cycle to I_{OCP}. If the condition exists longer than 10 ms, then the device shuts down. The frequency of the boost converter is internally set to 300 kHz or 600 kHz, depending on the device's version.

The boost also includes a soft start circuit. Each time the IC comes out of shutdown mode, the soft start period lasts for t_{SS}.

Overvoltage protection is also included. The device has an internally fixed OVP value of 60 V (typical) which serves as a secondary fault protection mechanism, in the event the externally programmed OVP fails (i.e. resistor divider opens up). While the internal 60 V OVP detector can be used exclusively without the external OVP network, this is only recommended for applications where the LED string voltage approaches 55 V or more. The OVP level can be set by using an external resistor divider connected between the output voltage and ground with its output connected to the OVP pin. The OVP can be set up to 60 V by varying the resistor divider to match the OVP internal reference of 6.9 V (typical).

5.2.3 LED driver

The six channel LED driver provides current matching for six LED strings to within ±2% maximum. The current in the strings is set using a resistor tied to GND from the ISET pin. The LED current level is given by the equation: $R_{SET} = 153/ I_{LED}$. The accuracy of the R_{SET} resistor should be 0.1% for best performance.

5.2.4 LED error detect

If an LED is open, the output voltage ramps to the OVP level. If there is still no current in the LED string, the LED channel is turned off and the output voltage ramps back down to normal operating level.

If LEDs are shorted and the voltage in any of the channels is greater than the SFDV threshold (7.0 V typical), then the device turns off this channel. However if the on-time of the channels is less than 10 μs, the SFDV circuit does not disable any of the channels, regardless of the voltage across them. All the LED errors can be cleared by recycling the EN pin or applying a complete power-on-reset (POR).

5.2.5 WAKE operation

The WAKE pin provides the means to set the device for low power consumption (shutdown mode) without the need of an extra logic signal for enable. This is achieved by connecting the WAKE and PWM pins together, and tying the EN pin to ground. In this configuration, the PWM signal is used to control the LED channels, while allowing low power consumption by setting the device into its shutdown mode every time the PWM signal is kept low for longer time than the WAKE time out of 27 ms.

5.2.6 Overtemperature shutdown and temperature control circuits

The 34845 includes over-temperature protection. If the internal temperature exceeds the over-temp threshold $OTT_{SHUTDOWN}$, then the device shuts down all functions. Once the temperature falls below the low level threshold, the device is re-enabled.

5.2.7 FAIL pin

The FAIL pin is at its low-impedance state when no error is detected. However, if an error such as an LED channel open or boost overcurrent is detected, the FAIL pin goes into high-impedance. Once a failure is detected, the FAIL pin can be cleared by recycling the EN pin or applying a complete power-on-reset (POR). If the detected failure is an Over-current time-out, the EN pin or a POR must be cycled/executed to restart the part.

5.3 Typical performance curves

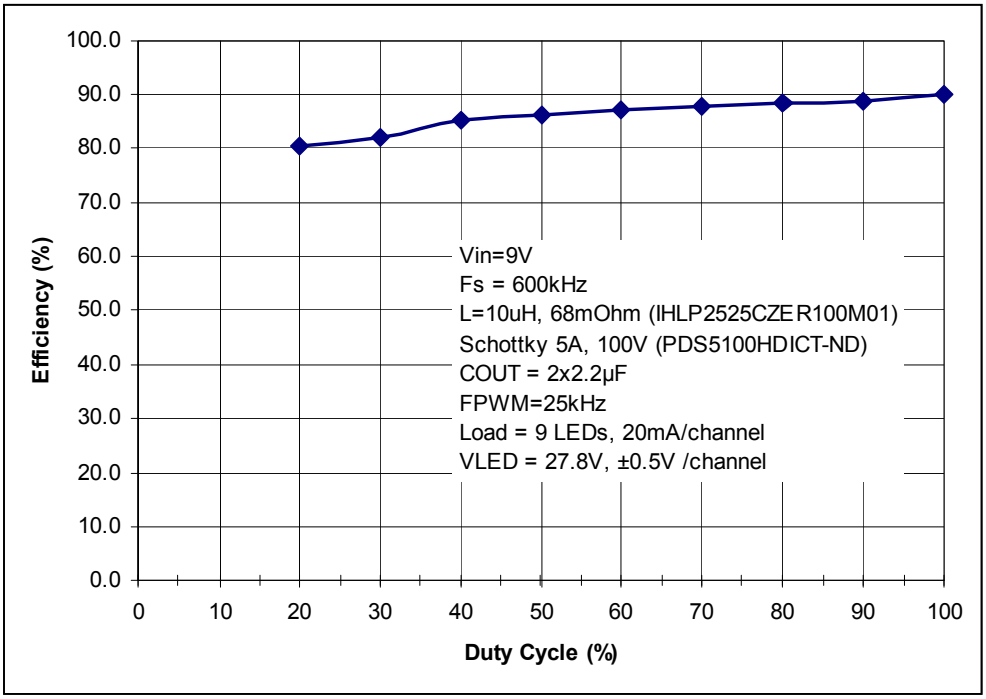


Figure 6. Typical system efficiency vs duty cycle (FPWM = 25 kHz)

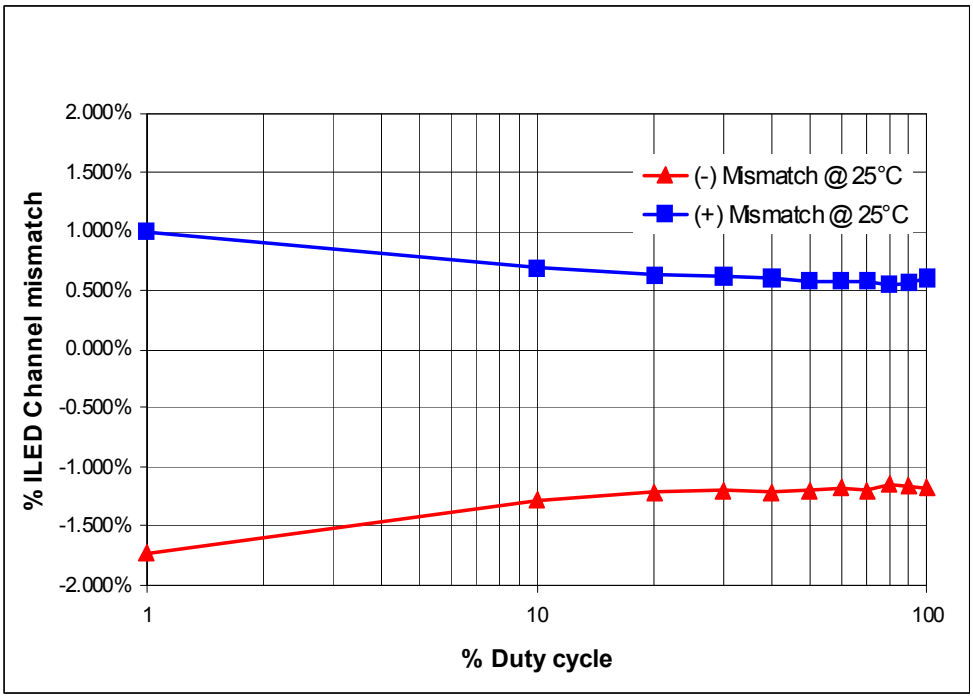


Figure 7. Typical ILED dimming linearity (FPWM = 25 kHz)

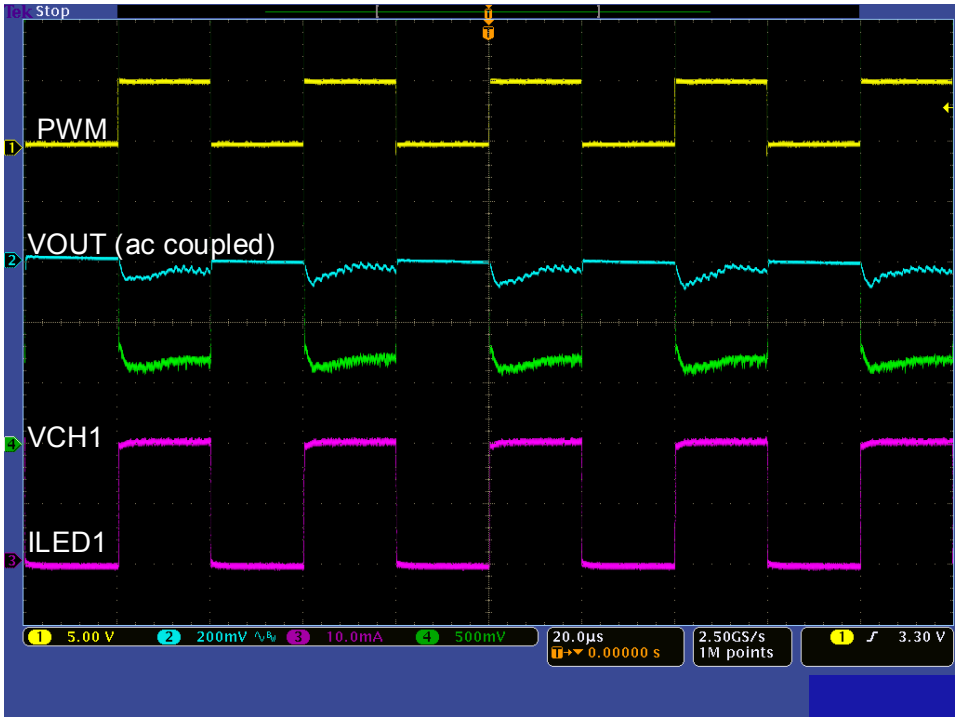


Figure 8. Typical operating waveforms (FPWM = 25 kHz, 50% duty)

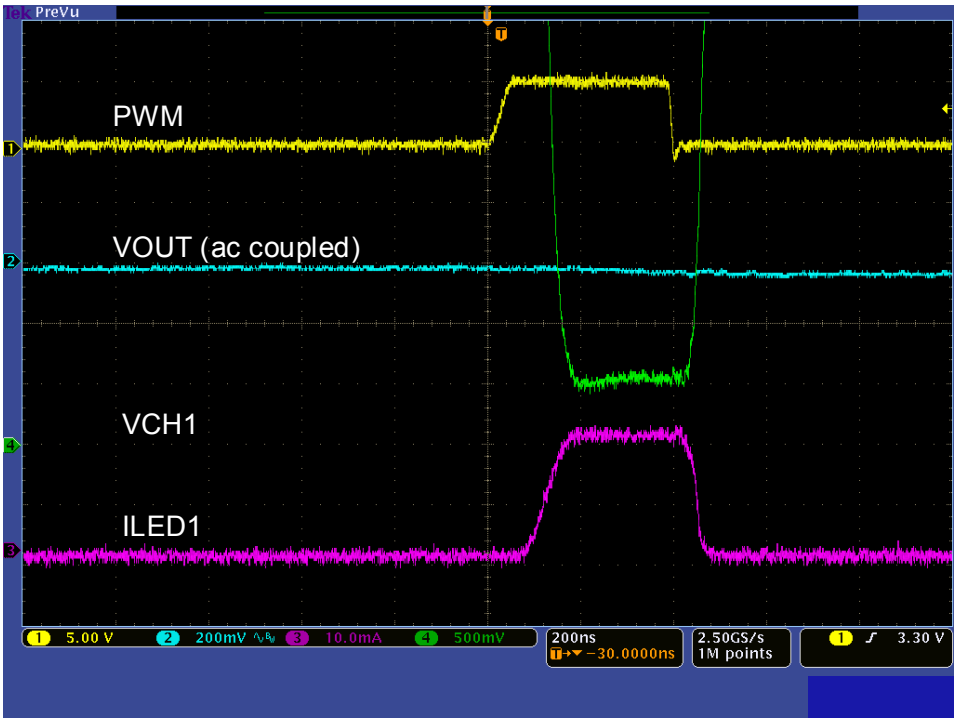


Figure 9. Low duty dimming operation waveforms (FPWM = 25 kHz, 1% duty)

6 Typical applications

6.1 Application diagram

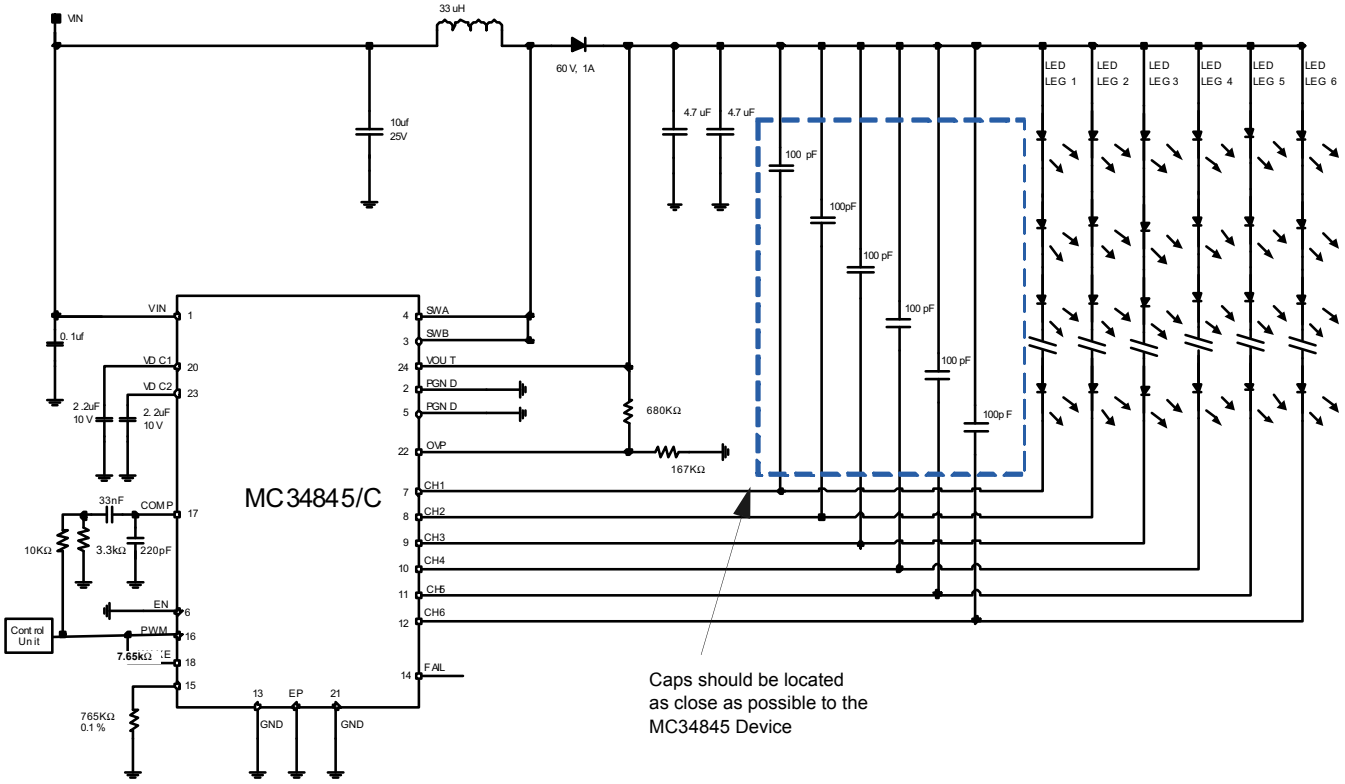


Figure 10. Typical application circuit for single wire control, f_S = 600 KHz (V_{IN} = 9.0 V, I_{LED}/channel = 20 mA/channel, 10 LEDs/channel, OVP = 35 V, V_{PWM} = 3.3 V)

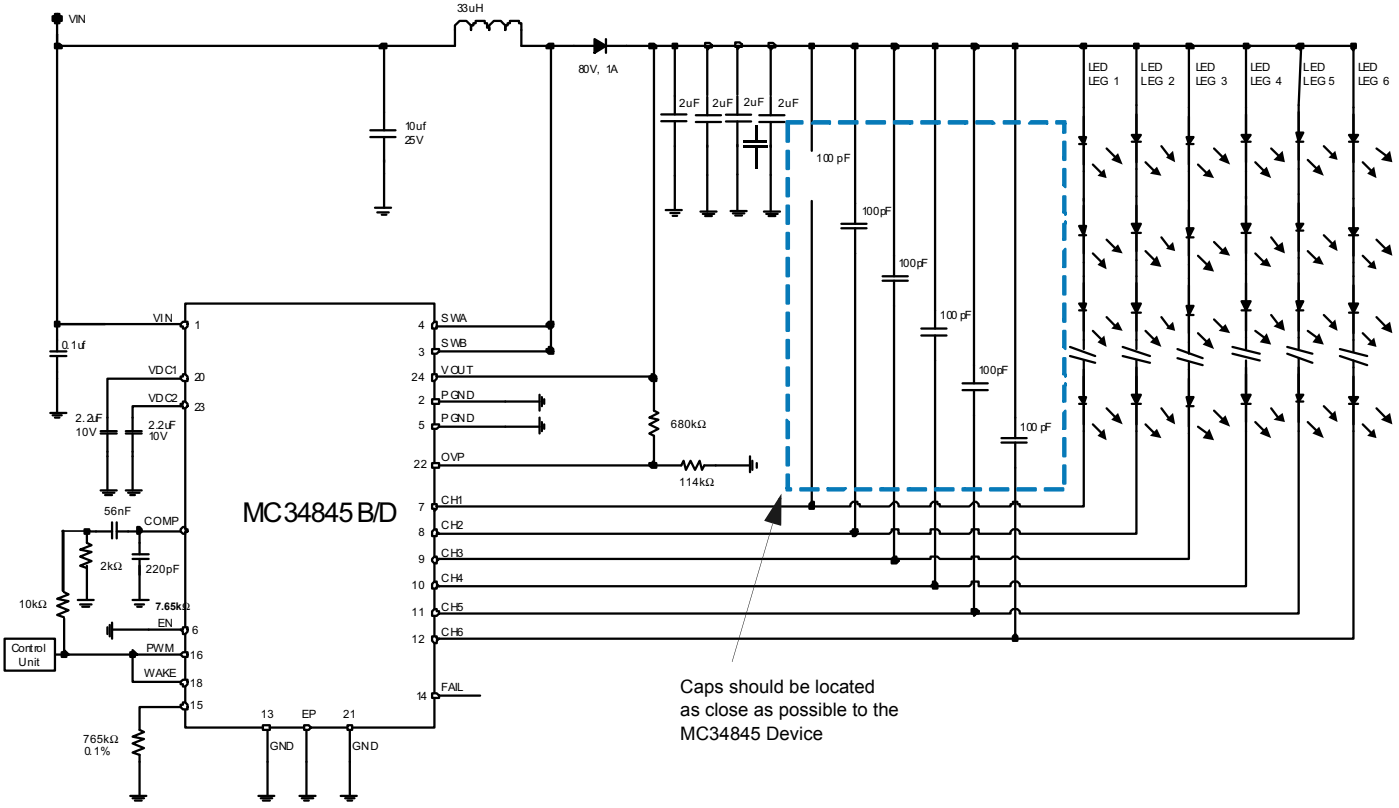


Figure 11. Typical application circuit for single wire control, f_S = 300 kHz (V_{IN} = 8.0V, I_{LED} = 20 mA/channel, 14 LEDs/channel, OVP = 49V, V_{PWM} = 3.3V)

6.2 Components calculation

The following formulas are intended for the calculation of all external components related with the boost converter and network compensation. To calculate the duty cycle, the internal losses of the MOSFET and diode should be taken into consideration:

$$D = \frac{V_{OUT} + V_D - V_{IN}}{V_{OUT} + V_D - V_{SW}}$$

The average input current depends directly on the output current when the internal switch is off.

$$I_{IN-AVG} = \frac{I_{OUT}}{1 - D}$$

6.2.1 Inductor

For calculating the Inductor, consider the losses of the internal switch and winding resistance of the inductor:

$$L = \frac{(V_{IN} - V_{SW} - (I_{IN-AVG} \times R_{INDUCTOR})) \times D}{I_{IN-AVG} \times r \times F_{SW}}$$

It is important to look for an inductor rated at least for the maximum input current:

$$I_{IN-MAX} = I_{IN-AVG} + \frac{V_{IN} \times (V_{OUT} - V_{IN})}{2 \times L \times F_{SW} \times V_{OUT}}$$

6.2.2 Input capacitor

The input capacitor should handle at least the following RMS current.

$$I_{RMS-C_{IN}} = \left(\frac{V_{IN} \times (V_{OUT} - V_{IN})}{2 \times L \times F_{SW} \times V_{OUT}}\right) \times 0.3$$

6.2.3 Output capacitor

For the output capacitor selection the transconductance should be taken in consideration.

$$C_{OUT} = \frac{R_{COMP} \times 5 \times G_M \times I_{OUT} \times L}{(1 - D) \times V_{OUT} \times 0.35}$$

The output voltage ripple (ΔV_{OUT}) depends on the ESR of the Output capacitor. For a low output voltage ripple, it is recommended to use ceramic capacitors which have a very low ESR. Since ceramic capacitor are costly, electrolytic or tantalum capacitors can be mixed with ceramic capacitors for a less expensive solution.

$$ESR_{C_{OUT}} = \frac{V_{OUT} \times \Delta V_{OUT} \times F_{SW} \times L}{V_{OUT} \times (1 - D)}$$

The output capacitor should at least handle the following RMS current.

$$I_{RMS-C_{OUT}} = I_{OUT} \times \sqrt{\frac{D}{1 - D}}$$

6.2.4 Network compensation

Since this Boost converter is current controlled, a Type II compensation is needed. Note that before calculating the network compensation, all boost converter components need to be known. For this type of compensation it is recommended to push out the Right Half Plane Zero to higher frequencies where it does not significantly affect the overall loop.

$$f_{RHPZ} = \frac{V_{OUT} \times (1 - D)^2}{I_{OUT} \times 2\pi \times L}$$

The crossover frequency must be set much lower than the location of the Right half plane zero:

$$f_{CROSS} = \frac{f_{RHPZ}}{5}$$

Since the system has a fixed slope compensation, R_{COMP} should be fixed for all configurations, i.e. R_{COMP} = 2.0 kΩ

C_{COMP1} and C_{COMP2} should be calculated as follows:

$$C_{COMP1} = \frac{2}{\pi \times f_{CROSS} \times R_{COMP}}$$

$$C_{COMP2} = \frac{2G_M}{6.28 \times F_{SW}}$$

The recommended values of these capacitors for an acceptable performance of the system in different operating conditions are C_{COMP1} = 33 nF and C_{COMP2} = 220 pF.

A resistor network can be implemented from the PWM pin to ground with a connection to the compensation network, to improve the transient response of the boost. This configuration should inject a 1.0 V signal to the COMP pin and the equivalent Thevenin resistance of the divider should be close to R_{COMP}, (i.e. for 2.0 kΩ COMP resistor, R_{COMP} = 3.3 kΩ and R_{SHUNT} = 10 kΩ. See Figure 10 and Figure 11 for implementation guidelines.

If a faster transient response is needed, a higher voltage (e.g. 1.3V) should be injected to the COMP pin; so the resistor divider should be modified accordingly, but keeping the equivalent Thevenin resistance of the divider close to R_{COMP}.

6.2.5 Variable definition

D = Duty cycle
V_{OUT} = Output voltage
V_D = Diode voltage
V_{IN} = Input voltage
V_{SW} = Internal switch voltage drop.
ΔV_{OUT} = Output voltage ripple
$I_{IN\text{-}AVG}$ = Average input current = $I_{L\text{-}AVG}$
I_{OUT} = Output current
$I_{IN\text{-}MAX}$ = Maximum input current
r = Current ripple ratio at the inductor = $\Delta I_L / I_{L\text{-}AVG}$
$I_{RMS\text{-}CIN}$= RMS current for the input capacitor
$I_{RMS\text{-}COUT}$= RMS current for output capacitor
L = Inductor.
$R_{INDUCTOR}$= Inductor winding resistor
F_{SW}= Boost switching frequency
C_{OUT} = Output capacitor
R_{COMP} = Compensation resistor
G_M= OTA transconductance
ESR_{COUT}= ESR of the output capacitor
f_{RHPZ}= Right half plane zero frequency
f_{CROSS}= Crossover frequency
C_{COMP1}= Compensation capacitor
C_{COMP2}= Shunt compensation capacitor

6.2.6 Component suggestions

The Component Suggestions only apply to the conditions shown. Therefore, adjustments are necessary for different application conditions.

Table 5. Component Suggestion Table

Application Case	V_{IN}(min)	V_{IN}(Max)	V_O(max)	VOVP	f_{BOOST}	ILED per channel	R_{OVP_UPPER}	R_{OVP_LOWER}
1	9.0 V	12 V	30 V	35 V	600 kHz	20 mA	680 kΩ	167 kΩ
2	6.0 V	12 V	43 V	48 V	300 kHz	23 mA	680 kΩ	114 kΩ

Application Case	L(min)	L(min) Continuous mode	C_{IN}(min)	C_{OUT}(min)	R_{COMP} at $V_{PWM\ =3.3V}$	R_{SHUNT} at $V_{PWM\ =3.3\ V}$	C_{COMP1}	C_{COMP2}
1	22 µH	33 µH	1x10 µF; X7R; 25 V	2 x 4.7 µF; X7R; 50 V	3.3 kΩ	10 kΩ	33 nF	220 pF
2	22 µH	33 µH	1x10 µF; X7R; 25 V	4 x 2.2 µF; X7R; 100 V	2.0 kΩ	16 kΩ	56 nF	220 pF
	I_{SAT} min = 2.6 A							

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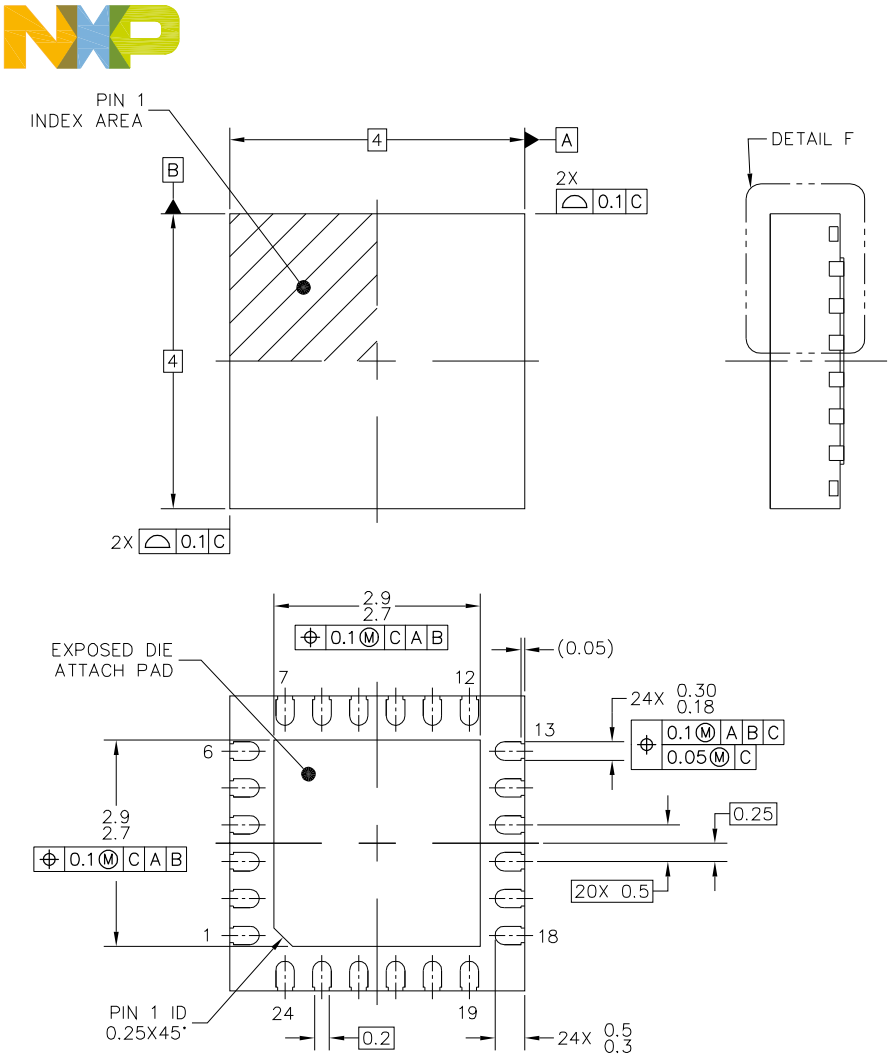
7 Packaging

7.1 Package mechanical dimensions

Package dimensions are provided in package drawings. To find the most current package outline drawing, go to www.nxp.com and perform a keyword search for the drawing's document number.

Table 6. Packaging Information

Package	Suffix	Package outline drawing number
24-Pin QFN-EP	EP	98ASA00602D



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TITLE: QFN, THERMALLY ENHANCED, 4 X 4 X 0.58, 0.5 PITCH, 24 TERMINAL	DOCUMENT NO: 98ASA00602D	REV: A
	STANDARD: NON-JEDEC	
	SOT1585-1	12 JAN 2016

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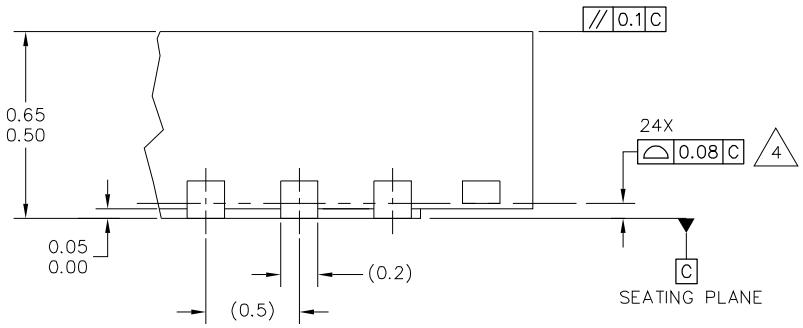

DETAIL F
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	STANDARD: NON-JEDEC	
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NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. THIS IS A NON–JEDEC REGISTERED PACKAGE.
4. COPLANARITY APPLIES TO LEADS AND DIE ATTACH FLAG.
5. MIN. METAL GAP SHOULD BE 0.2 MM.

MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

TITLE: QFN, THERMALLY ENHANCED, 4 X 4 X 0.58, 0.5 PITCH, 24 TERMINAL	DOCUMENT NO: 98ASA00602D REV: A
	STANDARD: NON–JEDEC
	SOT1585–1 12 JAN 2016

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8 Revision history

Revision	Date	Description of changes
6.0	12/2011	• Changed the max rating for the OVP pin from 7.0V to 7.75V in the Absolute Maximum Ratings Table on page 6. • Updated Freescale form and style.
7.0	6/2014	• No technical changes. Revised back page. Updated document properties. Added SMARTMOS sentence to first paragraph.
8.0	5/2015	• Removed obsolete part numbers from Orderable parts • Updated Packaging • Updated Freescale form and style
	8/2016	• Updated to NXP document form and style

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Rev. 8.0
8/2016

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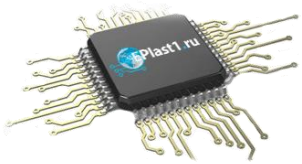

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