# ISL68127

Digital Dual Output, 7-Phase Configurable, PWM Controller with PMBus

FN8748
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The ISL68127 is a digital dual output, flexible multiphase (X+Y ≤ 7) PWM controller supporting the latest PMBus V1.3 specifications. The ISL68127can be configured to support any desired phase assignments up to a maximum of seven phases across the two outputs (X+Y). For example, 6+1, 5+2, 4+2, 3+3, 3+2, or even a single output operation as a 7+0 configuration are supported. The ISL68127 uses the Renesas proprietary linear synthetic digital current modulation scheme to achieve the industry's best combination of transient response and ease of tuning while addressing the challenges of modern multiphase designs.

You can configure the device and monitor telemetry using the intuitive Renesas PowerNavigator GUI. The ISL68127 device supports on-chip nonvolatile memory to store various configuration settings that are user-selectable through pin-strap, giving system designers increased power density to configure and deploy multiple configurations. The automatic phase add/drop feature allows maximum efficiency across all load ranges. Thresholds for automatic phase add/drop are user-programmable using PowerNavigator.

The ISL68127 supports a comprehensive fault management system to enable the design of highly reliable systems. From a multitiered overcurrent protection scheme to the configurable power-good and output overvoltage/undervoltage fault thresholds and temperature monitoring, almost any need is accommodated.

With minimal external components, easy configuration, robust fault management, and highly accurate regulation capability, implementing a high-performance, multiphase regulator has never been easier.

## Applications

- Networking equipment
- Telecom and datacom equipment
- Server and storage equipment
- Point-of-load power supply (Memory, DSP, ASIC, FPGA)

## Features

- Advanced linear digital modulation scheme
  - Zero latency synthetic current control for excellent HF current balance
  - Dual edge modulation for fastest transient response
- Auto phase add/drop for excellent load vs efficiency profile
- PMBus V1.3 support
  - Telemetry: $V_{IN}$, $V_{OUT}$, $I_{OUT}$, power IN/OUT, temperature, and various fault status registers
  - Up to 1MHz bus interface
- Flexible phase configuration
  - 7+0, 6+1, 5+2, and 4+3 phase operation
  - Operation using fewer than seven phases between two outputs is also supported
- Diode braking for overshoot reduction
- Differential remote voltage sensing supports ±0.5% closed loop system accuracy over load, line, and temperature
- Highly accurate current sensing for excellent load line regulation and accurate OCP
  - Supports the ISL99227 60A smart power stage
  - Supports DCR sense with integrated temperature compensation
- Comprehensive fault management enables high reliability systems
  - Pulse-by-pulse phase current limiting
  - Total output current protection
  - Output and input OV/UV
  - Open voltage sense detect
  - Black box recording capability for faults
- Intuitive configuration using PowerNavigator
  - NVM to store up to eight configurations
- Pb-free (RoHS compliant)

## Related Literature

For a full list of related documents, visit our web page:

- ISL68127 product page

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# Ordering Information

| PART NUMBER (Notes 2, 3) | PART MARKING | TEMP. RANGE (°C) | TAPE AND REEL (UNITS) (Note 1) | PACKAGE (RoHS COMPLIANT) | PKG. DWG. # |
|---|---|---|---|---|---|
| ISL68127IRAZ | ISL68127 IRZ | -40 to +85 | - | 48 Ld 6x6 QFN | L48.6x6B |
| ISL68127IRAZ-T | ISL68127 IRZ | -40 to +85 | 4k | 48 Ld 6x6 QFN | L48.6x6B |
| ISL68127IRAZ-T7A | ISL68127 IRZ | -40 to +85 | 250 | 48 Ld 6x6 QFN | L48.6x6B |

NOTES:

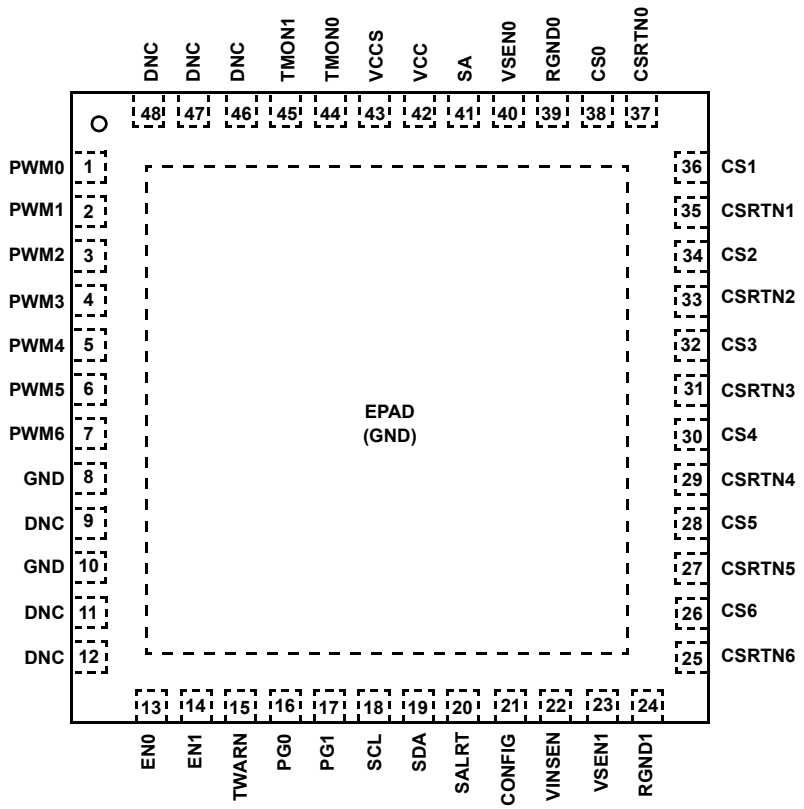
1. Refer to TB347 for details about reel specifications.
2. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), see the ISL68127 device page. For more information about MSL, see TB363.

**TABLE 1. KEY DIFFERENCES BETWEEN FAMILY OF PARTS**

| PART NUMBER | PHASE CONFIGURATION OUTPUT X/OUTPUT Y | SPECIFICATION SUPPORTED | PACKAGE |
|---|---|---|---|
| ISL68127 | X+Y ≤ 7 | PMBus | QFN 48 Ld, 6x6mm |
| ISL68137 | X+Y ≤ 7 | PMBus/AVSBus | QFN 48 Ld, 6x6mm |
| ISL68134 | X+Y ≤ 4 | PMBus/AVSBus | TQFN 40 Ld, 5x5mm |
| ISL68124 | X+Y ≤ 4 | PMBus | TQFN 40 Ld, 5x5mm |

# Pin Configuration

48 LD QFN
TOP VIEW



# Functional Pin Descriptions

Refer to Table 4 on page 19 for design layout considerations.

| PIN NUMBER | PIN NAME | DESCRIPTION |
|---|---|---|
| 1, 2, 3, 4, 5, 6, 7 | PWM[6:0] | Pulse-width modulation (PWM) outputs. Connect these pins to the PWM input pins of 3.3V logic-compatible Renesas smart power stages, driver IC(s), or power stages. |
| 8, 10 | GND | Ground pins. Connect directly to a system GND plane. |
| 9, 11, 12, 46, 47, 48 | DNC | Do not connect any signals to these pins. |
| 13 | EN0 | Input pin used as the Output 0 enable control. Active high. Connect to ground if not used. |
| 14 | EN1 | Input pin used as the Output 1 enable control. Active high. Connect to ground if not used. |
| 15 | TWARN | Thermal warning flag. This open-drain output is pulled low without disabling the regulators if the TMON pins sense an over-temperature event. Maximum pull-up voltage is $V_{CC}$. |
| 16 | PG0 | Open-drain, power-good indicators for Output 0. Maximum pull-up voltage is $V_{CC}$. |
| 17 | PG1 | Open-drain, power-good indicators for Output 1. Maximum pull-up voltage is $V_{CC}$. |
| 18 | SCL | Serial clock signal pin for the SMBus interface. Maximum pull-up voltage is $V_{CC}$. |
| 19 | SDA | Serial data signal pin for the SMBus interface. Maximum pull-up voltage is $V_{CC}$. |
| 20 | SALRT | Serial alert signal pin for the SMBus interface. Maximum pull-up voltage is $V_{CC}$. |
| 21 | CONFIG | Configuration ID selection pin. See Table 3 on page 16 for more details. |
| 22 | VINSEN | Input voltage sense pin. Connect to VIN through a resistor divider (typically 40.2k/10k) with a 10nF decoupling capacitor. |
| 23 | VSEN1 | Positive differential voltage sense input for Output 1. Connect to a positive remote sensing point. Connect to ground if not used. |
| 24 | RGND1 | Negative differential voltage sense input for Output 1. Connect to a negative remote sensing point. Connect to ground if not used. |
| 25, 27, 29, 31, 33, 35, 37 | CSRTN[6:0] | The CS and CSRTN pins are current sense inputs to individual phase differential amplifiers. Ground the current sense input of unused phases. The ISL68127 supports smart power stage, DCR, and resistor sensing. Connection details depend on the current sense method chosen. |
| 26, 28, 30, 32, 34, 36, 38 | CS[6:0] | |
| 39 | RGND0 | Negative differential voltage sense input for Output 0. Connect to a negative remote sensing point. Connect to ground if not used. |
| 40 | VSEN0 | Positive differential voltage sense input for for Output 0. Connect to a positive remote sensing point. Connect to ground if not used. |
| 41 | SA | PMBus address selection pin. See Table 2 on page 12 for more details. |
| 42 | VCC | Chip primary bias input. Connect this pin directly to a +3.3V supply with a high quality MLCC bypass capacitor. |
| 43 | VCCS | Internally generated 1.2V LDO logic supply from VCC. Decouple with a 4.7µF or greater MLCC (X5R or better). |
| 44 | TMON0 | Input pin for external temperature measurement at Output 0. Supports diode-based temperature sensing and smart power stage sensing. Refer to "Temperature Compensation" on page 15 for more information. |
| 45 | TMON1 | Input pin for external temperature measurement at Output 1. Supports diode-based temperature sensing and smart power stage sensing. Refer to "Temperature Compensation" on page 15 for more information. |
| EPAD | GND | The package pad serves as the GND return for all chip functions. Connect directly to the system GND plane with multiple thermal vias. |

# Driver, DrMOS, and Smart Power Stage Recommendations

| PART NUMBER | QUIESCENT CURRENT (mA) | GATE DRIVE VOLTAGE (V) | NUMBER OF DRIVERS | COMMENTS |
|---|---|---|---|---|
| ISL99227 | 4.85 | 5 | Single | 60A, 5x5 smart power stage |
| ISL99140 | 0.19 | 5 | Single | 40A, 6x6 DrMOS |
| ISL6596 | 0.19 | 5 | Single | Connect ISL6596 VCTRL to 3.3V |
| ISL6617A | 5 | N/A | N/A | Phase Doubler with 5V PWM output to be compatible with 60A DrMOS or with 60A smart power stage. Supports up to a 14-phase design. |

# Internal Block Diagram

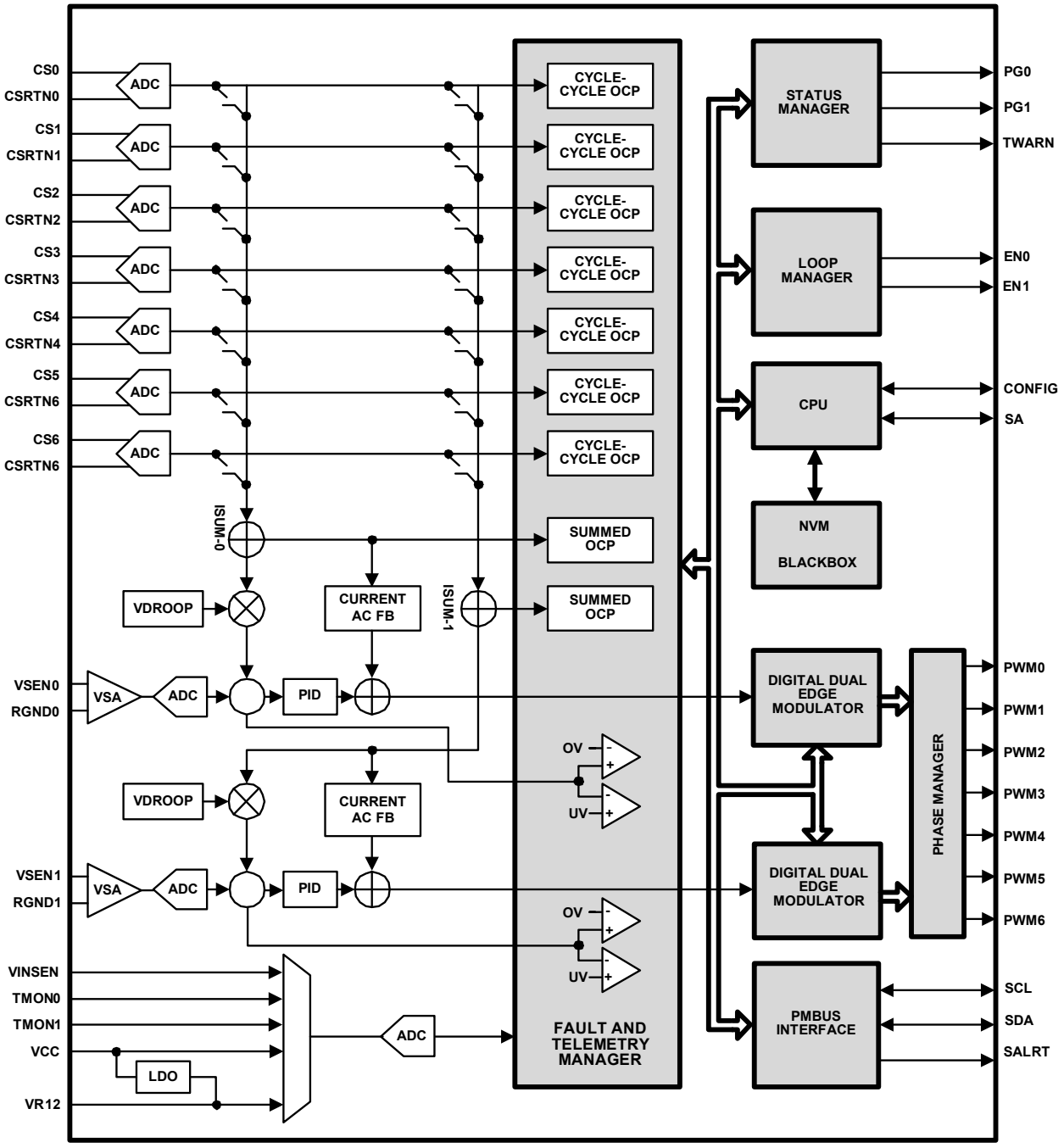



FIGURE 1. INTERNAL BLOCK DIAGRAM

# Typical Application: 6+1 Configuration with ISL99227 SPS

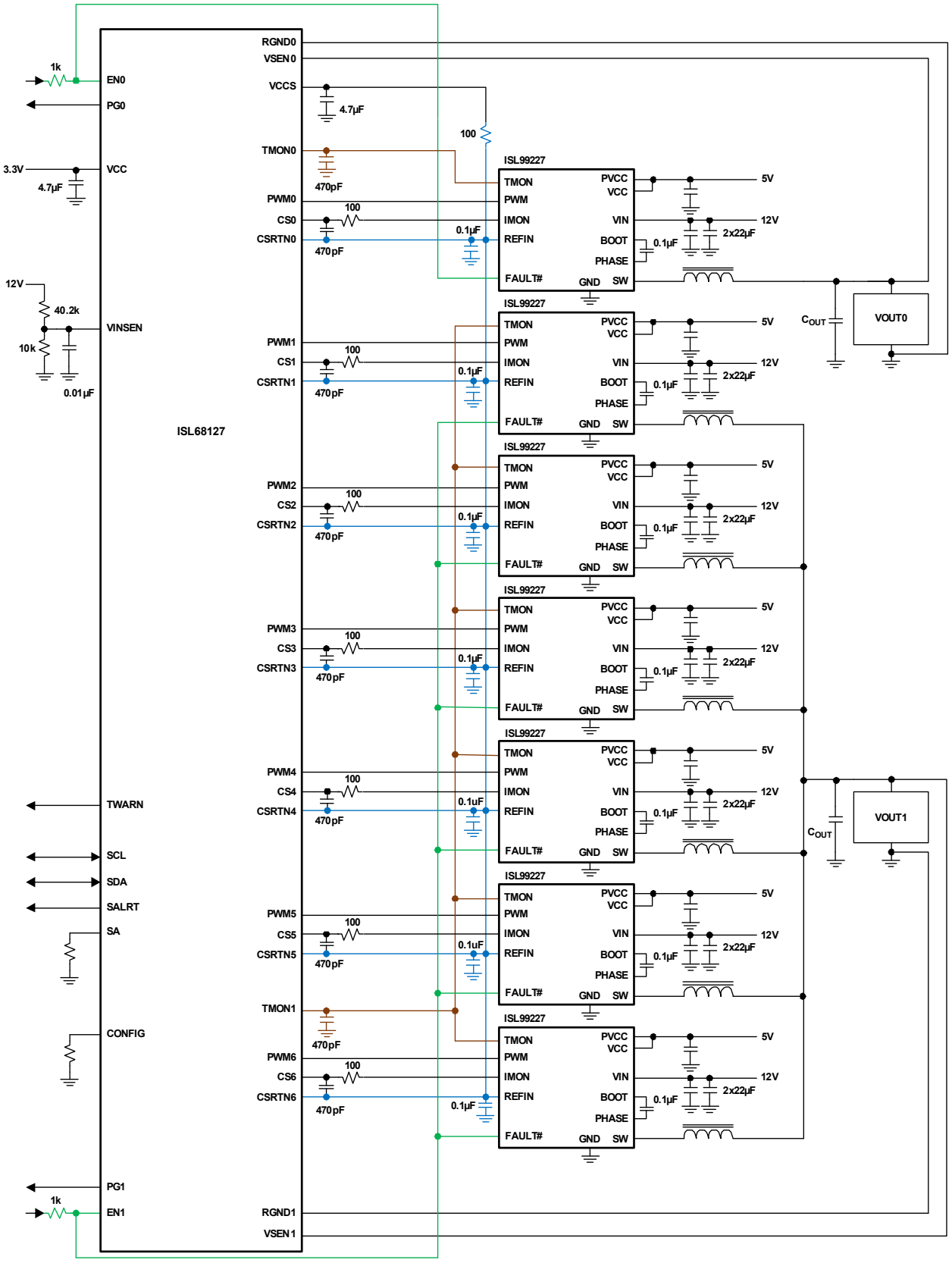



FIGURE 2. TYPICAL APPLICATION: 6+1 CONFIGURATION WITH ISL99227 SPS

# Typical Application: 4+3 Configuration with ISL99227 SPS

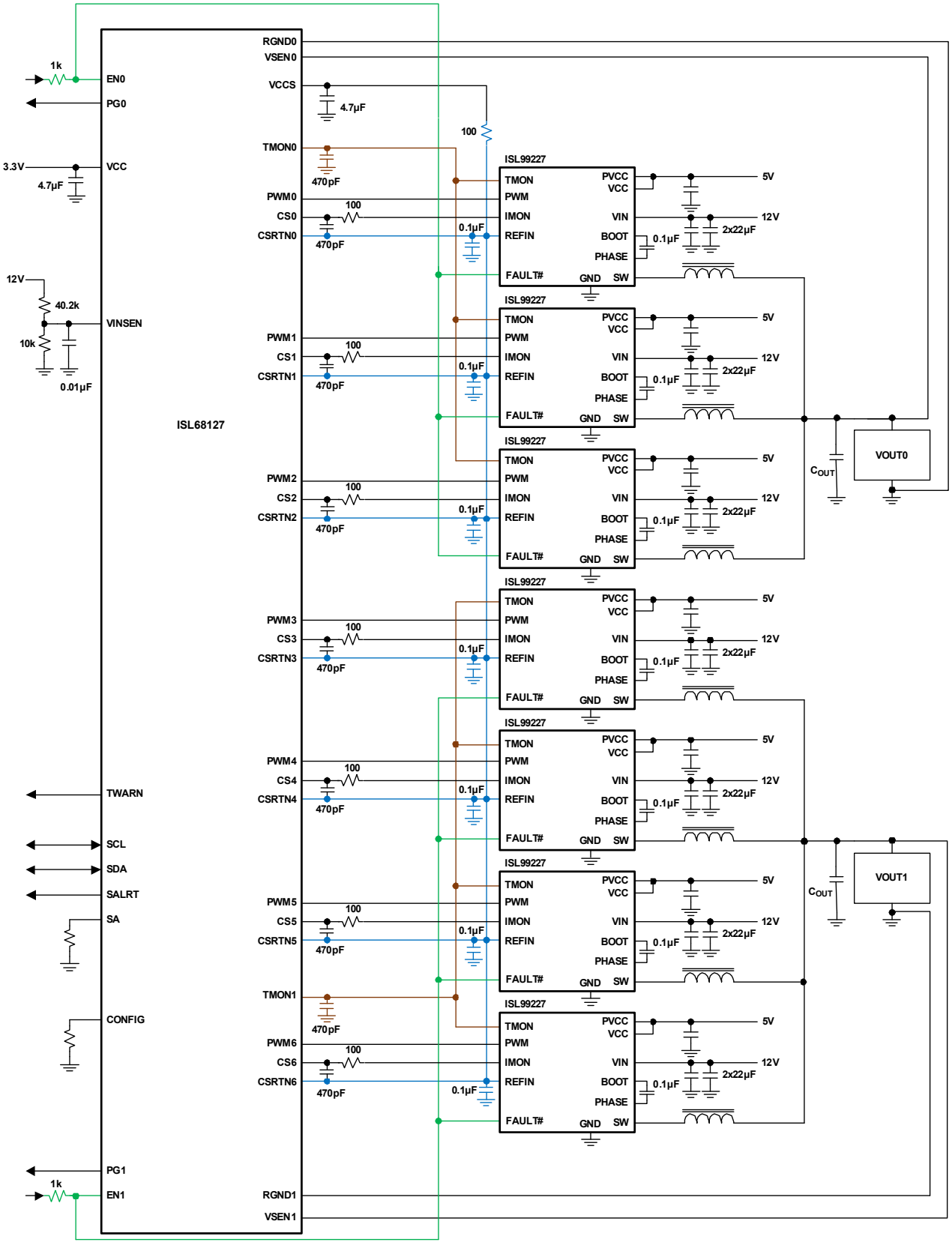



FIGURE 3. TYPICAL APPLICATION: 4+3 CONFIGURATION WITH ISL99227 SPS

# Typical Application: 5+2 Configuration with DCR Sensing

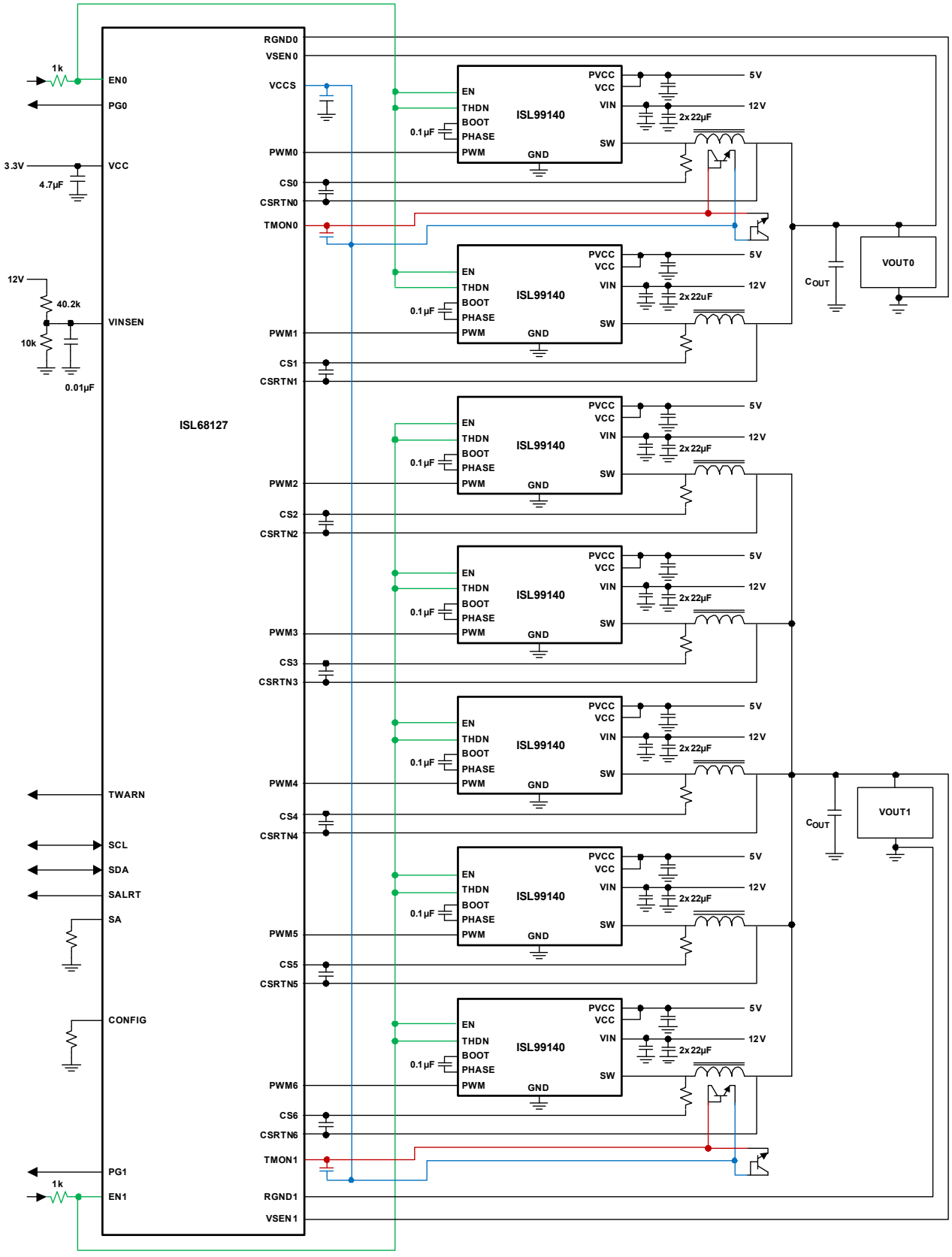



FIGURE 4. TYPICAL APPLICATION: 5+2 CONFIGURATION WITH DCR SENSING

# Typical Application: Phase Doubler 14-Phase VR with ISL6617A+SPS

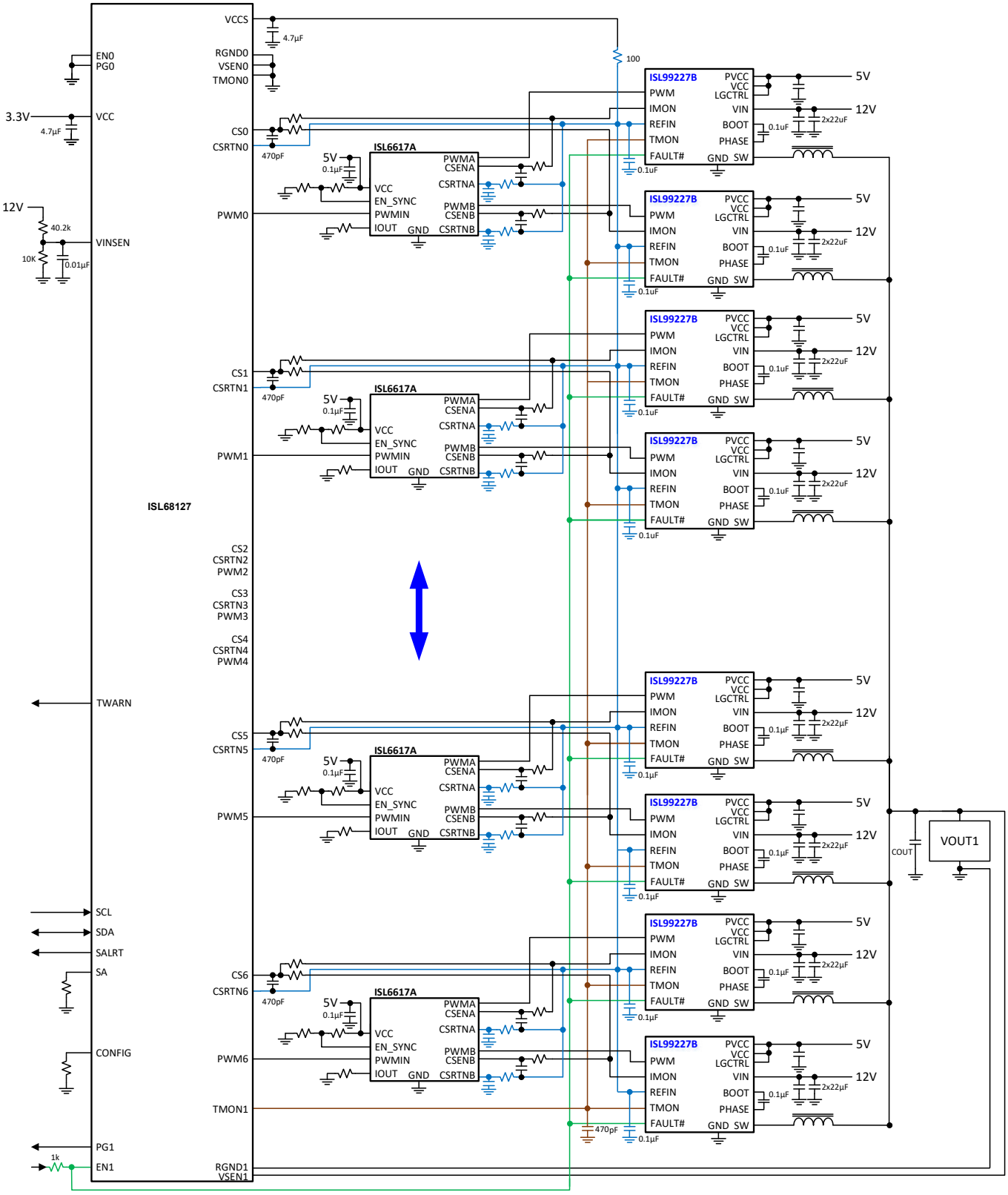



**FIGURE 5. PHASE DOUBLER 14-PHASE VR WITH ISL6617A+SMART POWER STAGE**

## Absolute Maximum Ratings

VCC . . . . . +4.3V
VCCS . . . . . +1.6V
All Other Pins . . . . . (GND - 0.3V) to VCC + 0.3V
ESD Rating:
Human Body Model (Tested per JS-001-2014) . . . . . 2kV
Charged Device Model (Tested per JS-001-2014) . . . . . 1kV
Latch-Up (Tested per JESD-78D; Class 2, Level A) . . . . . 100mA

## Thermal Information

| Thermal Resistance (Notes 4, 5) | $\theta_{JA}$ (°C/W) | $\theta_{JC}$ (°C/W) |
|---|---|---|
| 48 Ld 6x6 QFN Package | 27 | 1 |

Maximum Junction Temperature . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . see TB493

## Recommended Operating Conditions

Supply Voltage, $V_{CC}$ . . . . . +3.3V ±5%
Ambient Temperature . . . . . -40°C to +85°C
Output Voltage . . . . . 0V to 3.05V

*CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.*

NOTES:

4. $\theta_{JA}$ is measured in free air with the component mounted on a high-effective thermal conductivity test board with "direct attach" features. See TB379.
5. For $\theta_{JC}$, the "case temp" location is the center of the exposed metal pad on the package underside.

## Electrical Specifications

Recommended operating conditions, $V_{CC}$ = 3.3V, unless otherwise specified. **Boldface limits apply across the operating temperature range -40°C to +85°C.**

| PARAMETER | TEST CONDITIONS | MIN (Note 7) | TYP | MAX (Note 7) | UNIT |
|---|---|---|---|---|---|
| **$V_{CC}$ SUPPLY CURRENT** | | | | | |
| Nominal Supply Current | $V_{CC}$ = 3.3VDC; EN1/2 = $V_{IH}$, $f_{SW}$ = 400kHz | | 90.5 | | mA |
| Shutdown Supply Current | $V_{CC}$ = 3.3VDC; EN1/2 = 0V, no switching | | 11.4 | | mA |
| **VCCS LDO SUPPLY** | | | | | |
| Output Voltage | | **1.20** | 1.25 | **1.30** | V |
| Maximum Current Capability | Excluding internal load | **50** | | | mA |
| **POWER-ON RESET AND INPUT VOLTAGE LOCKOUT** | | | | | |
| $V_{CC}$ Rising POR Threshold | | | 2.7 | **2.9** | V |
| $V_{CC}$ Falling POR Threshold | | **1.0** | | | V |
| Enable (EN0 and EN1) Input High Level | | **2.55** | | | V |
| Enable (EN0 and EN1) Input Low Level | | | | **0.8** | |
| Enable (EN0 and EN1) Input LOW to HIGH Ramp Delay (TON_DELAY) | | **200** | | | µs |
| POR to Initialization Complete Time | | | 30 | **40** | ms |
| **OUTPUT VOLTAGE CHARACTERISTICS (Note 6)** | | | | | |
| Output Voltage Adjustment Range | | **0.25** | | **3.05** | V |
| Output Voltage Set-Point Accuracy | Set-point 0.8V to 3.05V | **-0.5** | | **0.5** | % |
| | Set-point 0.25V to <0.8V | **-5** | | **5** | mV |
| **VOLTAGE SENSE AMPLIFIER** | | | | | |
| Open Sense Current | During open pin check of initialization only | | 22 | | µA |
| Input Impedance (VSEN - RGND) | | | 200 | | kΩ |
| Maximum Common-Mode Input | | | $V_{CC}$ - 0.2 | | V |
| Maximum Differential Input (VSEN - RGND) | | | | **3.05** | V |
| **CURRENT SENSE AND OVERCURRENT PROTECTION** | | | | | |
| Maximum Common-Mode Input (SPS mode) | CSRTNx - GND | | 1.6 | | V |
| Maximum Common-Mode Input (DCR mode) | CSRTNx - GND | | 3.3 | | V |
| Current Sense Accuracy | ISEN to ADC accuracy | **-2** | | **2** | % |
| Average Overcurrent Threshold Resolution | | | 0.1 | | A |
| Cycle-by-Cycle Current Limiting Threshold Accuracy | | | 0.1 | | A |

## Electrical Specifications

Recommended operating conditions, $V_{CC}$ = 3.3V, unless otherwise specified. **Boldface limits apply across the operating temperature range -40°C to +85°C. (Continued)**

| PARAMETER | TEST CONDITIONS | MIN (Note 7) | TYP | MAX (Note 7) | UNIT |
|---|---|---|---|---|---|
| **DIGITAL DROOP** | | | | | |
| Droop Resolution | | | 0.01 | | mV/A |
| **OSCILLATORS** | | | | | |
| Accuracy of Switching Frequency Setting | When set to 500kHz | **480** | 500 | **520** | kHz |
| | | **-4** | | **+4** | % |
| Switching Frequency Range | | **200** | | **1000** | kHz |
| **SOFT-START RATE AND VOLTAGE TRANSITION RATE** | | | | | |
| Minimum Soft-Start Ramp Rate | Programmable minimum rate | | 20 | | µs |
| Maximum Soft-Start Ramp Rate | Programmable maximum rate | | 10 | | ms |
| Soft-Start Ramp Rate Accuracy | | **-4** | | **4** | % |
| Minimum Transition Rate | Programmable minimum rate | | 0.1 | | mV/µs |
| Maximum Transition Rate | Programmable maximum rate | | 100 | | mV/µs |
| Transition Rate Accuracy | | **-4** | | **4** | % |
| **PWM OUTPUT** | | | | | |
| PWMx Output High Level | $I_{OUT}$ = 4mA | **$V_{CC}$ - 0.4** | | | V |
| PWMx Output Low Level | $I_{OUT}$ = 4mA | | | **0.4** | V |
| PWMx Output Tri-State $I_{OL}$ | $V_{OH}$ = $V_{CC}$ | | | **1** | µA |
| PWMx Output Tri-State $I_{OH}$ | $V_{OL}$ = 0V | **-1** | | | µA |
| **THERMAL MONITORING AND PROTECTION** | | | | | |
| Temperature Sensor Range | | **-50** | | **150** | °C |
| Temperature Sensor Accuracy | TMON to ADC accuracy | **-4.5** | | **4.5** | % |
| TWARN Output Low Impedance | | **4** | 9 | **13** | Ω |
| TWARN Hysteresis | | | 3 | | °C |
| **POWER-GOOD AND PROTECTION MONITORS** | | | | | |
| PG Output Low Voltage | $I_{OUT}$ = 8mA load | | | **0.4** | V |
| PG Leakage Current | With pull-up resistor externally connected to VCC | | 0.5 | **1** | µA |
| Overvoltage Protection Threshold Resolution | | | 1 | | mV |
| Undervoltage Protection Threshold Resolution | | | 1 | | mV |
| Overvoltage Protection Threshold When Disabled | | | $V_{CC}$ - 0.2 | | V |
| **INPUT VOLTAGE SENSE** | | | | | |
| Input Voltage Accuracy | VINSEN to ADC accuracy | **-2.5** | | **2.5** | % |
| Input Voltage Protection Threshold Resolution | | | 1 | | mV |
| **SMBus/PMBus** | | | | | |
| SALERT, SDA Output Low Level | $I_{OUT}$ = 4mA | | | **0.4** | V |
| SCL, SDA Input High Level | | **1.55** | | | V |
| SCL, SDA Input Low Level | | | | **0.8** | V |
| SCL, SDA Input Hysteresis | | | 2 | | mV |
| SCL Frequency Range | | **0.05** | | **2** | MHz |

NOTES:

6. These parts are designed and adjusted for accuracy with all errors in the voltage loop included.
7. Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.

# Typical Performance Curves

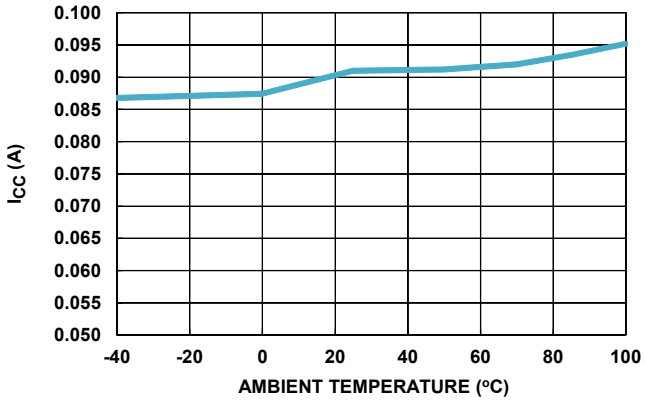



FIGURE 6. NOMINAL SUPPLY CURRENT vs TEMPERATURE

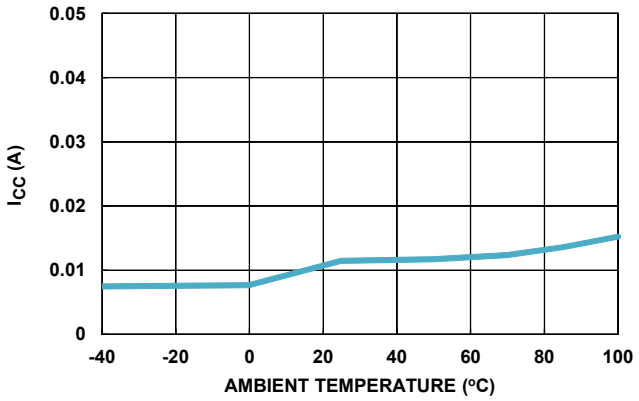



FIGURE 7. SHUTDOWN SUPPLY CURRENT vs TEMPERATURE

# Functional Description

## Overview

The ISL68127 is a digital dual output 7-phase PWM controller that can be programmed for a single output 7+0, dual output 6+1, 5+2, or 4+3 phase operation. Operation using fewer than seven phases between two outputs is also supported. Existing digital multiphase solutions use nonlinear analog comparator based schemes to bolster the inadequate transient response common to many digital multiphase solutions. The ISL68127 uses a linear voltage regulation scheme to address transient loads. As a result, it is much easier for users to configure and validate designs compared to nonlinear schemes. By combining a proprietary low noise and zero latency digital current sense scheme with cutting edge digital design techniques, Renesas can meet transient demands without resorting to nonlinear schemes. In addition, the ISL68127 can store up to eight user configurations in NVM and allows you to select the desired configuration through pin-strap (CONFIG). The result is a system that is easy to configure and deploy.

The ISL68127 includes performance enhancing features such diode braking, automatic phase dropping, DCR/resistor/smart power stage current sense support, load line regulation, and multiple temperature sensing options.

To facilitate configuration development, the PowerNavigator GUI provides a step-by-step arrangement for setup and parametric adjustment. After setting a configuration, you can use PowerNavigator to monitor telemetry or use the PMBus interface based on the supported command set.

## PWM Modulation Scheme

The ISL68127 uses the Renesas proprietary linear synthetic current modulation scheme to improve transient performance. This unique, constant frequency, dual-edge PWM modulation scheme moves both the PWM leading and trailing edges independently to give the best response to transient loads. Current balance is an inherent part of the regulation scheme. The modulation scheme is capable of overlapping pulses if the load profile requires it. The modulator can also add or remove pulses from a given cycle in response to regulation demands while still managing maximum average frequency to safe levels. The operating frequency is constant for DC load conditions.

## PMBus Address Selection

When communicating with multiple PMBus devices on a single bus, each device must have its own unique address so the host can distinguish between the devices. Set the device address using a 1% resistor on the SA pin according to the pin-strap options listed in Table 2.

TABLE 2. RESISTOR VALUES TO ADDRESS MAPPING

| R SA (Ω) | PMBus ADDRESS | R SA (Ω) | PMBus ADDRESS |
|---|---|---|---|
| 0 | 60h | 1500 | 50h |
| 180 | 61h | 1800 | 51h |
| 330 | 64h | 2200 | 54h |
| 470 | 65h | 2700 | 55h |
| 680 | 40h | 3300 | 58h |
| 820 | 41h | 3900 | 59h |
| 1000 | 44h | 4700 | 5Ch |
| 1200 | 45h | 5600 | 5Dh |

## Phase Configuration

The ISL68127 supports up to two regulated outputs through seven configurable phases. Either output is capable of controlling up to seven phases in any arbitrary mix. Phase assignments are accomplished using PowerNavigator.

Although the device supports arbitrary phase assignment, it is good practice to assign phases to Output 1 in descending sequential numerical order starting from Phase 6. For example, a 4-phase rail should consist of Phases 6, 5, 4, and 3. For Output 0, assign phases starting from Phase 0 in ascending sequential numerical order.

## Automatic Phase Add and Drop

Automatic phase adding and dropping produces the most optimal efficiency across a wide range of output loading. The automatic phase dropping feature is optional. If automatic phase dropping is enabled, the number of active phases at any time is determined solely by load current. During operation, the Output 1 Phases drop beginning with the lowest phase number assigned. Phase dropping begins with the highest assigned phase number. Figure 8 illustrates the typical characteristic of efficiency vs load current vs phase count.

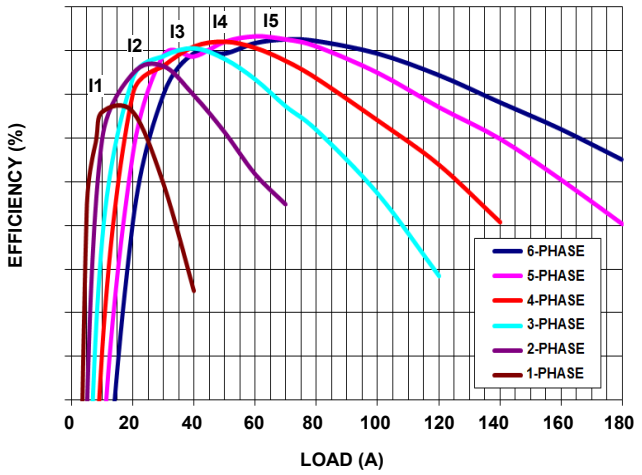



FIGURE 8. EFFICIENCY vs PHASE NUMBER

Phases are dropped one at a time with a user-programmed drop delay between drop events. As an example, suppose the delay is set to 1ms and three phases are active. If the load suddenly drops to a level needing only one phase, the ISL68127 begins by dropping a phase after 1ms. The ISL68127 then drops an additional phase each 1ms until only one phase remains.

### FAST PHASE ADD FUNCTION

The fast phase add function provides a very rapid response to transient load conditions. The ISL68127 continuously monitors the system regulation error and readies all dropped phases for use if the system regulation error exceeds the user set threshold. There is no delay if all phases are needed to support a load transient. The fast phase add threshold is set in PowerNavigator. You can also configure the output current threshold for adding and dropping phases in PowerNavigator.

To ensure dropped phases have sufficient boot capacitor charge to turn on the high-side MOSFET after a long period of disable, a boot refresh circuit turns on the low-side MOSFET of each dropped phase to refresh the boot capacitor. The boot refresh frequency is programmable in PowerNavigator.

## Output Voltage Configuration

Configure the output voltage set points and thresholds for each output in PowerNavigator. You can configure parameters such as output voltage, $V_{OUT}$ margin high/low, and $V_{OUT}$ OV/UV fault thresholds.You can also adjust output voltage and margin high/low during regulation using the PMBus commands VOUT_COMMAND, VOUT_MARGIN_HIGH, and VOUT_MARGIN_LOW for further tuning.

Maintain the following $V_{OUT}$ relationships for correct operation: VOUT_OV_FAULT_LIMIT > VOUT_COMMAND (VOUT_MARGIN_HIGH and VOUT_MARGIN_LOW, if used) > VOUT_UV_FAULT_LIMIT. Additionally, the $V_{OUT}$ commands are bounded by VOUT_MAX and VOUT_MIN to provide protection against incorrect set points being sent to the device.

## Switching Frequency

The switching frequency is user-configurable over a range of 200kHz to 1MHz.

## Current Sensing

The ISL68127 supports DCR, resistor, and smart power stage current sensing. Connect to the various sense elements using the CS and CSRTN pins. Current sensing inputs are high impedance differential inputs to reject noise and ground related inaccuracies.

To accommodate a wide range of effective sense resistance, PowerNavigator uses information about the effective sense resistance and required per phase current capability to properly configure the current sense circuitry.

### INDUCTOR DCR SENSING

DCR sensing takes advantage of the fact that an inductor winding has a resistive component (DCR) that drops a voltage proportional to the inductor current. Figure 9 shows that the DCR is treated as a lumped element with one terminal inaccessible for measurement.

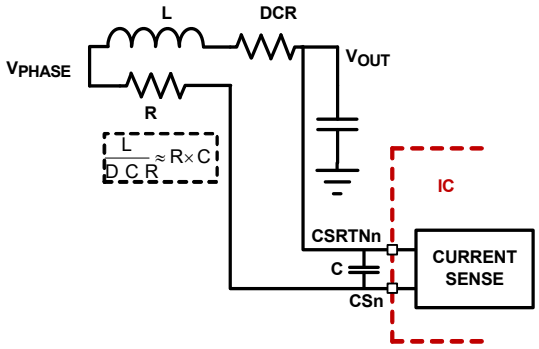



FIGURE 9. DCR SENSING CONFIGURATION

Fortunately, a simple R-C network as shown in Figure 10 on page 14 can reproduce the hidden DCR voltage. By matching the R-C time constant to the L/DCR time constant, you can precisely recreate the DCR voltage across the capacitor. This means that VDCR(t) = VC(t), preserving even the high frequency characteristic of the DCR voltage.

Modern inductors often have such low DCR values that the resulting signal is <10mV. To avoid noise problems, take care in the PCB layout to properly place the R-C components and route the differential lines between the controller and inductor. Figure 9 shows one PCB design method that places the R component near the inductor $V_{PHASE}$ and the C component very close to the IC pins. This minimizes routing of the noisy $V_{PHASE}$ and maximizes filtering near the IC. Route the lines between the inductor and IC as a pair on a single layer directly to the controller. Avoid routing the pair near any switching signals such

as Phase and PWM. This is the method used by Renesas on evaluation board designs.

This method senses the resistance of a metal winding in which the DCR value increases with temperature. The temperature must be compensated or the sensed (and reported) current increases with temperature. To compensate the temperature effect, the ISL68127 provides temperature sensing options and an internal methodology to apply the correction.

## RESISTIVE SENSING

For more accurate current sensing, a dedicated current sense resistor, $R_{SENSE}$, in series with each output inductor can serve as the current sense element. However, this technique reduces the overall converter efficiency due to the additional power loss on the current sense element, $R_{SENSE}$. A current sensing resistor has a distributed parasitic inductance, known as Equivalent Series Inductance (ESL), typically less than 4nH. Consider the ESL as a separate lumped quantity, as shown in Figure 10

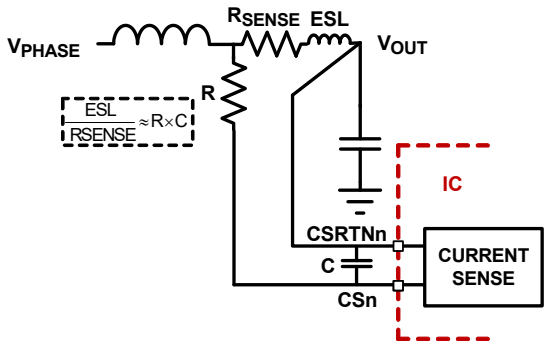



FIGURE 10. SENSE RESISTOR IN SERIES WITH INDUCTOR

The phase current $I_L$, flowing through the inductor, also passes through the ESL. Similar to "Inductor DCR Sensing" on page 13, a simple R-C network across the current sense resistor extracts the $R_{SENSE}$ voltage. Match the ESL/$R_{SENSE}$ time constant to the R-C time constant.

Figure 11 shows the sensed waveforms with and without matching RC when using resistive sense. The PCB layout should be similar to that described in "Inductor DCR Sensing".

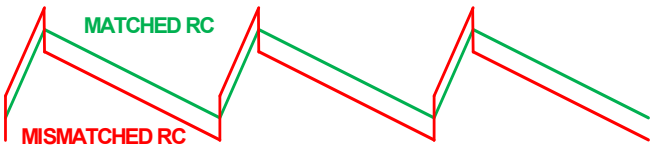



FIGURE 11. VOLTAGE ACROSS R WITH AND WITHOUT R-C

## L/DCR OR ESL/$R_{SEN}$ MATCHING

If the compensator design is correct, Figure 12 shows the expected load transient response waveforms if L/DCR or ESL/$R_{SEN}$ is matching the R-C time constant.

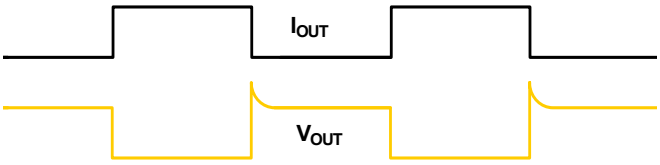



FIGURE 12. DESIRED LOAD TRANSIENT RESPONSE WAVEFORMS

When the load current $I_{OUT}$ has a square change, the output voltage $V_{OUT}$ also has a square response, except for the potential overshoot at load release. However, there is always some uncertainty in the true parameter values involved in the time constant matching and therefore fine-tuning is generally required.

If the R-C time constant is too large or too small, $V_C(t)$ does not accurately represent real-time $I_{OUT}(t)$ and reduces the transient response. Figure 13 shows the load transient response when the R-C timing constant is too small.

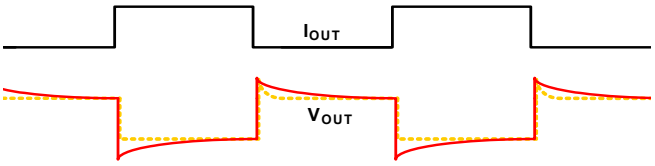



FIGURE 13. LOAD TRANSIENT RESPONSE WHEN R-C TIME CONSTANT IS TOO SMALL

In this condition, $V_{OUT}$ sags excessively at load insertion and can create a system failure or early overcurrent trip. Figure 14 shows the transient response when the R-C timing constant is too large. $V_{OUT}$ is sluggish in drooping to its final value. Use these general guides if fine-tuning is needed.

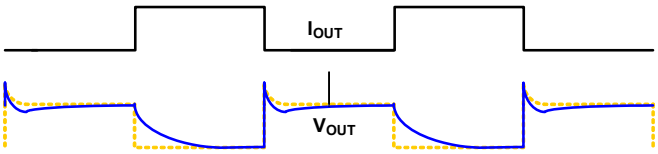



FIGURE 14. LOAD TRANSIENT RESPONSE WHEN R-C TIME CONSTANT IS TOO LARGE

## SPS CURRENT SENSING

SPS current is sensed by sensing each SPS IMON output individually using VCCS as a common reference. Complete the following steps to sense SPS current.

1. Connect all SPS IREF input pins and all ISL68127 CSRTNn input pins together and tie them to VCCS.
2. Connect the SPS IMONn output pins to the corresponding ISL68127 CSn input pins. The signals should be run as differential pairs from the SPS back to the ISL68127.

## Temperature Sensing

The ISL68127 supports temperature sensing through BJT or smart power stage sense elements. Support for BJT sense elements uses the delta Vbe method and allows up to two sensors (MMBT3906 or similar) on each temperature sense input, TMON0 and TMON1. Support for smart power stage uses a linear conversion algorithm and allows one sensor reading per pin. The conversion from voltage to temperature for smart power stage sensing is user-programmable in PowerNavigator.

SPS temperature sensing measures the temperature-dependent voltage output on the SPS TMON pin. All of the SPS devices attached to the Output 0 rail have their TMON pins connected to the ISL68127 TMON0 pin. All of the SPS devices attached to the Output 1 rail have their TMON pins connected to the ISL68127 TMON1 pin. The reported temperature is that of the highest temperature SPS of the group.

In addition to the external temperature sense, the IC senses its own die temperature, which can be monitored in PowerNavigator.

Sensed temperature is used in the system for faults, telemetry, and sensed current temperature compensation.

## Temperature Compensation

The ISL68127 supports inductor DCR sensing, which generally requires temperature compensation due to the copper wire used to form inductors. Copper has a positive temperature coefficient of approximately 0.39%/°C. Because the voltage across the inductor is sensed for the output current information, the sensed current has the same positive temperature coefficient as the inductor DCR.

Compensating current sense for temperature variation generally requires that the current sensing element temperature and its temperature coefficient is known. Although the temperature coefficient is generally obtained easily, actual current sense element temperature is essentially impossible to measure directly. Instead, a temperature sensor (a BJT for the ISL68127) placed near the inductors is measured and the current sense element (DCR) temperature is calculated from that measurement. Calculating current sense element temperature is equivalent to applying gain and offset corrections to the temperature sensor measurement. The ISL68127 supports both corrections.

Figure 15 shows the temperature compensation block diagram.

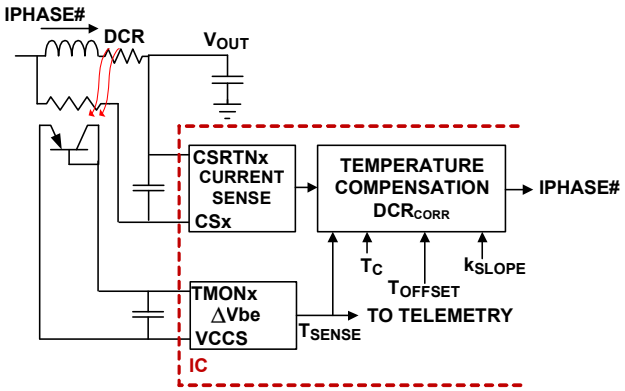



FIGURE 15. TEMPERATURE COMPENSATION BLOCK DIAGRAM

The IC monitors a BJT near the inductors used for DCR sensing using the delta Vbe temperature sensing method. $T_{SENSE}$ is the direct measured temperature of the BJT. Because the BJT is not directly sensing DCR, corrections must be made so that $T_{DCR}$ reflects the true DCR temperature. Corrections are applied according to the relationship shown in Equation 1, where $k_{SLOPE}$ represents a gain scaling and $T_{OFFSET}$ represents an offset correction. Configure these parameters in PowerNavigator:

$$T_{DCR} = k_{SLOPE} \bullet T_{SENSE} + T_{OFFSET} \quad \text{(EQ. 1)}$$

After calculating $T_{DCR}$, determine the compensated DCR value with Equation 2, where $DCR_{25}$ is the DCR at +25°C and $T_C$ is the temperature coefficient of copper (3900 ppm/°C).
$T_{DCR} = T_{ACTUAL}$:

$$DCR_{CORR} = DCR_{25} \bullet (1 + T_C \bullet (T_{ACTUAL} - 25)) \quad \text{(EQ. 2)}$$

The temperature-compensated DCR is now used to determine the actual value of current in the DCR sense element.

In the physical PCB design, place the temperature sense diode (BJT) close to the inductor of the phase that is never dropped during automatic phase drop operation. Additionally, add a filter capacitor no larger than 500pF near the IC between each TMONx pin and VCCS (see Figure 16).

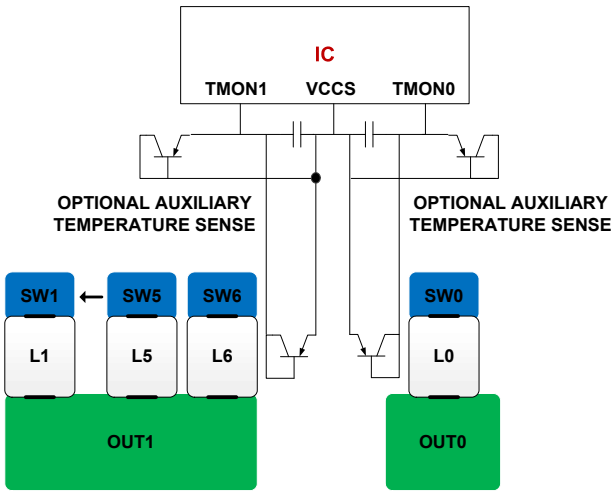



FIGURE 16. RECOMMENDED PLACEMENT OF TEMPERATURE SENSORS

## Lossless Input Current and Power Sensing

Input current telemetry is provided through an input current synthesizer. By using the IC's ability to precisely determine its operational conditions, the input current can be synthesized to a high degree of accuracy without the need for a lossy sense resistor. You can fine-tune offset and gain in PowerNavigator. Note that input current sense must be fine-tuned after the output current sense setup is finalized. You can calculate input power with a precise knowledge of input current and voltage.

Input current and power telemetry is accessed through PMBus and easily monitored in PowerNavigator. $V_{IN}$ is monitored directly by the VINSEN pin through a 1:5 resistor divider as shown in Figure 17.

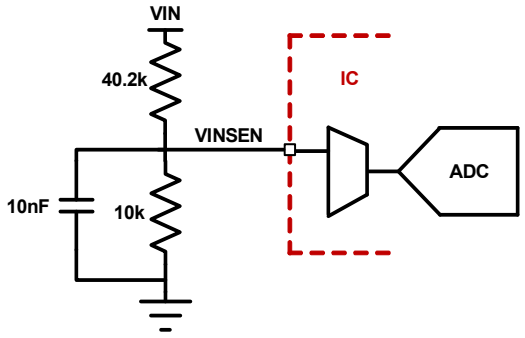



FIGURE 17. INPUT VOLTAGE SENSE CONFIGURATION

## Voltage Regulation

The remote sense amplifier senses and digitizes the output voltage. After digitization, the regulation loop is entirely digital. The ISL68127 uses traditional PID controls and several enhanced methods to compensate the voltage regulation loop and tune the transient response.

## Current Feedback

Current feedback in a voltage regulator is often used to ease the stability design of the voltage feedback path. Additionally, many microprocessors require the voltage regulator to have a controlled output resistance (known as load line or droop regulation), which is accomplished using current feedback.

For applications requiring droop regulation, specify the output resistance in PowerNavigator.

Current feedback stability benefits are available for rails that do not specify droop regulation, such as system agent. For these applications, you can enable AC current feedback in PowerNavigator. With this configuration, the DC output voltage is steady regardless of load current.

## Power-On Reset (POR)

ISL68127 initialization begins after $V_{CC}$ crosses its rising POR threshold. When POR conditions are met, the internal 1.2V LDO is enabled and basic digital subsystem integrity checks begin. During this process, the controller loads the selected user configuration from NVM as indicated by the CONFIG pin resistor value, read $V_{IN}$ UVLO thresholds from memory, and start the telemetry subsystem. With telemetry enabled, you can monitor $V_{IN}$ determine when it exceeds its user-programmable rising UVLO threshold. When $V_{CC}$ and $V_{IN}$ satisfy their respective voltage conditions, the controller is in its shutdown mode. The controller transitions to its active state and begins soft-start when the EN0/EN1 command is at start-up. In shutdown mode, the PWM outputs are held in a high-impedance state to ensure the drivers remain off.

## Soft-Start Delay and Ramp Times

It may be necessary to set a delay from when an enable signal is received until the output voltage starts to ramp to its target value. In addition, you can precisely set the time required for an output to ramp to its target value after the delay period has expired. These features can be used as part of an overall inrush current management strategy or to precisely control how fast a load IC is turned on. The ISL68127 provides several options for precisely and independently controlling both the delay and ramp time periods. The soft-start delay period begins when the EN pin is asserted and ends when the delay time expires.

Use PowerNavigator to configure the soft-start delay and ramp-up/down times. The device needs approximately 200µs after enable to initialize before starting to ramp up. When the soft-start ramp period is set to 0ms, the output ramps up as quickly as the output load capacitance and loop settings allow. Renesas recommends setting the ramps to a non-zero value to prevent inadvertent fault conditions due to excessive inrush current.

## Stored Configuration Selection

You can store and use up to eight configurations at any time using the on-board nonvolatile memory. Configurations are assigned an identifier number between 0 and 7 at power-up. The device loads the configuration indicated by the 1% resistor value detected on the CONFIG pin. Resistor values indicate use of one of the eight possible configurations. See Table 3 for the resistor value corresponding to each configuration identifier.

TABLE 3. RESISTOR VALUES TO CONFIGURATION MAPPING

| R CONFIG (Ω) | CONFIG ID |
|---|---|
| 6800 | 0 |
| 1800 | 1 |
| 2200 | 2 |
| 2700 | 3 |
| 3300 | 4 |
| 3900 | 5 |
| 4700 | 6 |
| 5600 | 7 |

Only the most recent configuration with a given number can be loaded. The device supports a total of eight stored operations. For example, a configuration with the identifier 0 can be saved eight times, or configurations with all eight identifiers can be stored one time each for a total of eight save operations.

PowerNavigator provides a simple interface to save and load configurations.

# Fault Monitoring and Protection

The ISL68127 actively monitors temperature, input voltage, output voltage, and output current to detect and report fault conditions. Fault monitors trigger configurable protective measures to prevent damage to a load. The power-good indicators, PG0/PG1, can linkto external system monitors.

A high level of flexibility is provided in the ISL68127 fault logic. Faults can be enabled or disabled individually. Each fault type can also be configured to either latch off or retry indefinitely.

## Power-Good Signals

The PG0/PG1 pins are open-drain, power-good outputs that indicate completion of the soft-start sequence and output voltage of the associated rail within the expected regulation range.

The PG pins can be associated or disassociated with a number of the available fault types. This allows a system design to be tailored for virtually any condition. In addition, these power-good indicators are pulled low when a fault (OCP or OVP) condition or UV condition is detected on the associated rail.

## Output Voltage Protection

Output voltage is measured at the load sensing points differentially for regulation and the same measurement is used for OVP and UVP. The fault thresholds are set using PMBus commands. Figure 18 shows a simplified OVP/UVP block diagram. The output voltage comparisons occur in the digital domain.

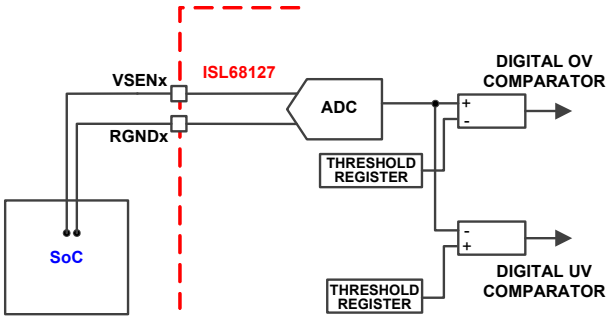



FIGURE 18. OVP, UVP COMPARATORS

The device responds to an output overvoltage condition by disabling the output, declaring a fault, setting the SALRT pin, setting the PG pin, and pulsing the LFET until the output voltage drops below the threshold. Similarly, the device responds to an output undervoltage condition by disabling the output, declaring a fault, setting the SALRT pin, and setting the PG pin. The output does not restart until the EN pin is cycled (unless the device is configured to retry).

The ISL68127 also features open pin sensing protection to detect an open of the output voltage sensing circuit. Controller operation is suspended if an open of the output voltage sensing circuit is detected.

## Output Current Protection

The ISL68127 provides a comprehensive overcurrent protection scheme. Each phase is protected from both excessive peak current and sustained current and the system is protected from sustained total output overcurrent.

Figure 19 shows a block diagram of the system total output current protection scheme. In this scheme, the phase currents are summed to form ISUM. ISUM is then fed to dual response paths allowing you to program separate LPF, threshold, and response time.

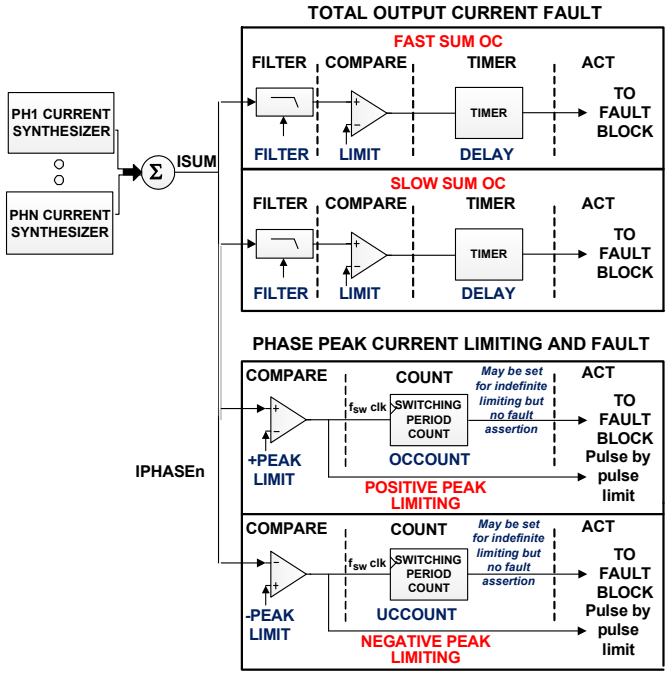



FIGURE 19. OCP FUNCTIONAL DIAGRAM

The Fast Sum OC path responds more quickly than the Slow Sum OC path. With this system, you can allow high peak total current for a short time and a lower level of current for a sustained time. Note that neither of these paths affect PWM activity on a cycle-by-cycle basis. Set the characteristics of each path in PowerNavigator.

In addition to total output current, the ISL68127 provides an individual phase peak current limit that acts on PWM in a cycle-by-cycle manner. If a phase current exceeds the OC threshold, the phase PWM signal is inverted to move current away from the threshold. In addition to limiting positive or negative peak current on a cycle-by-cycle basis, the individual phase OC can be configured to limit current indefinitely or to declare a fault after a programmable number of consecutive OC cycles. This feature is useful for applications in which a fault shutdown of the system is not acceptable but some ability to limit phase currents is required. Figures 22 and 23 on page 18 show this operation.

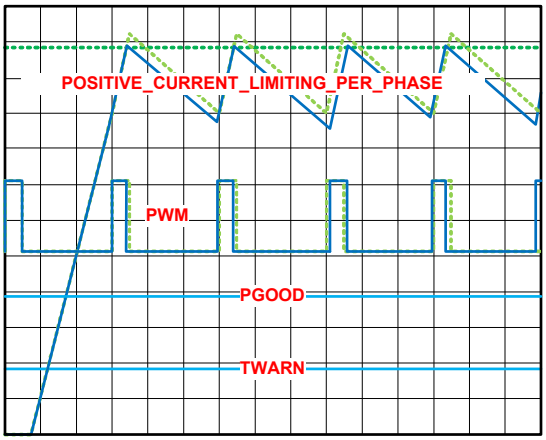



FIGURE 20. POSITIVE PEAK PHASE CURRENT LIMITING

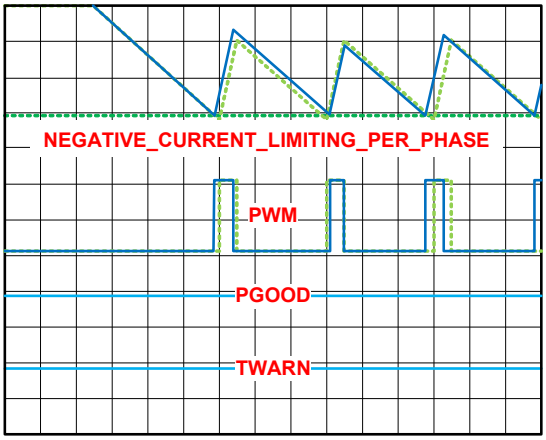



FIGURE 21. NEGATIVE PEAK PHASE CURRENT LIMITING

If configured for indefinite current limit, the converter acts as a current source and $V_{OUT}$ does not remain at its regulation point. Note that in this case, $V_{OUT}$ OV or UV protection action may occur, which can shut the regulator down.

Figure 22 shows an example OCP_Fast waveform and Figure 23 shows an example OCP_Slow waveform.

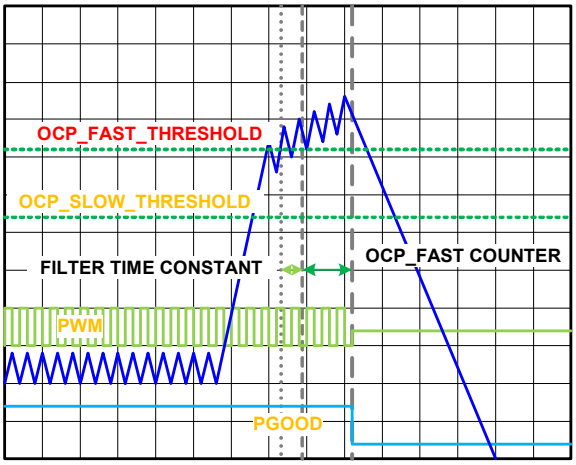



FIGURE 22. OCP_FAST

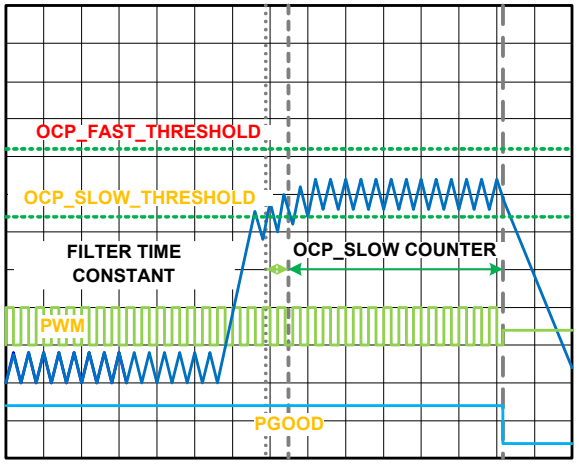



FIGURE 23. OCP_SLOW

## Smart Power Stage OC Fault Detect

Renesas Smart Power Stage (SPS) devices output a large signal on their IMON lines if peak current exceeds their preprogrammed threshold (for more information about this functionality, refer to the relevant SPS datasheet). The ISL68127 is equipped to detect this fault flag and immediately shut down. This detector is enabled on the PowerNavigator Overcurrent Fault setup screen.

This feature detects signals that exceed the current sense ADC full scale range. If this detector is disabled while using a Renesas SPS, the SPS Fault# signal must be connected to the controller Enable pin of the associated rail, ensuring that SPS OC events are detected and the converter shuts down.

## Thermal Monitoring and Protection

The TWARN pin indicates the voltage regulator temperature status. The TWARN pin is an open-drain output and an external pull-up resistor is required. This signal is valid only after the controller is enabled.

The TWARN signal can inform the system that the voltage regulator temperature is too high and the load should reduce its power consumption. TWARN only indicates a thermal warning, not a fault.

Figure 24 shows the thermal monitoring function block diagram.

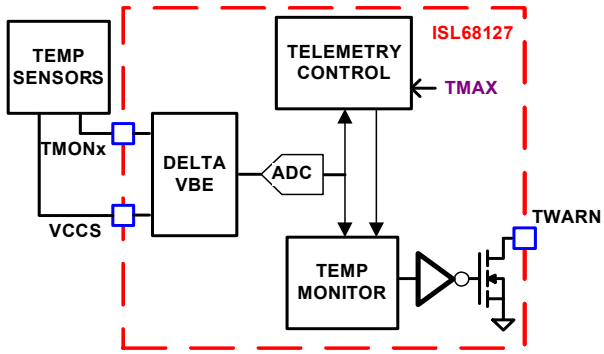



FIGURE 24. BLOCK DIAGRAM OF THERMAL MONITORING FUNCTION

The ISL68127 has two over-temperature thresholds that allow both warning and fault indications. Each temperature sensor threshold can be independently programmed in PowerNavigator. Figure 25 shows the thermal warning to TWARN and Figure 26 shows the over-temperature fault to shutdown. You can configure PGOOD and TWARN to indicate these warning and fault thresholds using PowerNavigator.

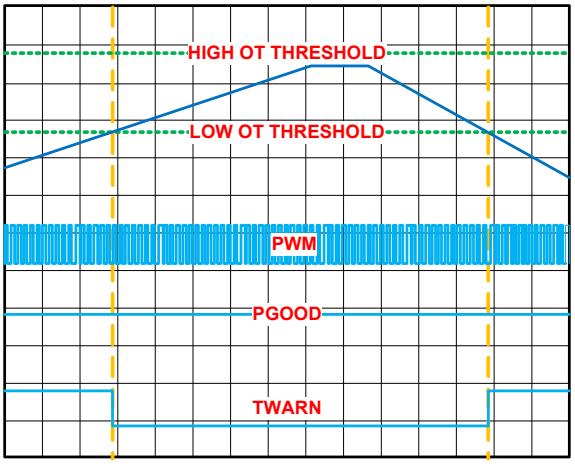



FIGURE 25. THERMAL WARNING TO TWARN

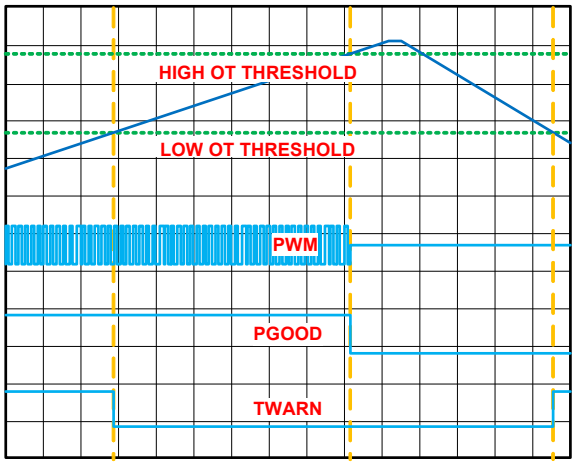



FIGURE 26. OVER-TEMPERATURE FAULT

# Layout and Design Considerations

The following PCB layout and design strategies minimize noise coupling and the impact of board parasitic impedances on converter performance, and optimize the heat dissipation capabilities of the PCB. See TB379 for more information. Follow these important practices during the layout process.

Table 4 provides general guidance on best practices related to pin noise sensitivity. Good engineering judgment is required to implement designs based on criteria specific to the situation.

TABLE 4. PIN DESIGN AND/OR LAYOUT CONSIDERATIONS

| PIN NAME | NOISE SENSITIVE | DESCRIPTION |
|---|---|---|
| VINSEN | Yes | Connects to the resistor divider between VIN and GND (see Figure 17). Filter VINSEN with 10nF to GND. |
| RGNDx VSENx | Yes | Treat each of the remote voltage sense pairs as differential signals in the PCB layout. Route the pairs side by side on the same layer. Do not route the pairs in close proximity to noisy signals such as PWM or Phase. Tie to ground when not used. |
| PGx | No | Open-drain, 3.3V maximum pull-up voltage. Tie to ground when not used. |
| SCL, SDA, SALRT | Yes | 50kHz to 2MHz signal during communication. Pair with SALRT and route carefully. Provide 20 mils spacing within SDA, SALRT, and SCL; and more than 30 mils spacing to all other signals. Refer to the SMBus design guidelines and place proper termination resistance for impedance matching. Tie to ground when not used. |
| $TMON^X$ | Yes | When diode sensing is used, VCCS is the return path for the delta Vbe currents. Use a separate VCCS route specifically for diode temp sense. Place a filter capacitor no greater than 500pF between each TMON pin and at the VCCS pin near the IC. Tie to ground when not used. |
| TWARN | No | Open-drain. 3.3V maximum pull-up voltage. |
| VCC | Yes | Place a MLCC decoupling capacitor (at least 2.2µF) directly at the pin. |
| VCCS | Yes | Place a 4.7µF MLCC decoupling capacitor directly at the pin. |
| PWM | No | Avoid routing near noise sensitive analog lines such as current sense or voltage sense. |
| CSx CSRTNx | Yes | Treat each of the current sense pairs as differential signals in the PCB layout. Route the pairs side by side on the same layer. DO not route the pairs in close proximity to noisy signals such as PWM or Phase.<br>**Note:** Proper current sense routing is perhaps the most critical of all the layout tasks. |
| GND | Yes | This EPAD is the return of the PWM output drivers. Use four or more vias to directly connect the EPAD to the power ground plane. |
| General Comments | | The layer next to the top or bottom layer should be a ground layer. The signal layers should be sandwiched in the ground layers if possible. |

# PMBus Operation

The ISL68127 PMBus slave address is pin selectable using the SA pin and resistor value described in Table 2 on page 12. For proper operation, follow the PMBus protocol in "PMBus Protocol" on page 21. The supported PMBus addresses are in 8-bit format , including the write and read bit (see Table 5). The least significant bit of the 8-bit address is for write (0h) and read (1h). PMBus commands are in the range from 0x00h to 0xFFh. Page 0 corresponds to Output 0 and Page 1 corresponds to Output 1. For reference purposes, the 7-bit format addresses are also summarized in Table 5.

**TABLE 5. PMBus 8-BIT AND 7-BIT FORMAT ADDRESS (HEX)**

| 8-BIT | 7-BIT | 8-BIT | 7-BIT | 8-BIT | 7-BIT | 8-BIT | 7-BIT |
|---|---|---|---|---|---|---|---|
| 80/81 | 40 | A0/A1 | 50 | B0/B1 | 58 | C0/C1 | 60 |
| 82/83 | 41 | A2/A3 | 51 | B2/B3 | 59 | C2/C3 | 61 |
| 88/89 | 44 | A8/A9 | 54 | B8/B9 | 5C | C8/C9 | 64 |
| 8A/8B | 45 | AA/AB | 55 | BA/BB | 5D | CA/CB | 65 |

The PMBus data formats follow PMBus specification V1.3 and SMBus V2.0.

The basic PMBus telemetry commands are summarized in "PMBus Command Summary" on page 22.

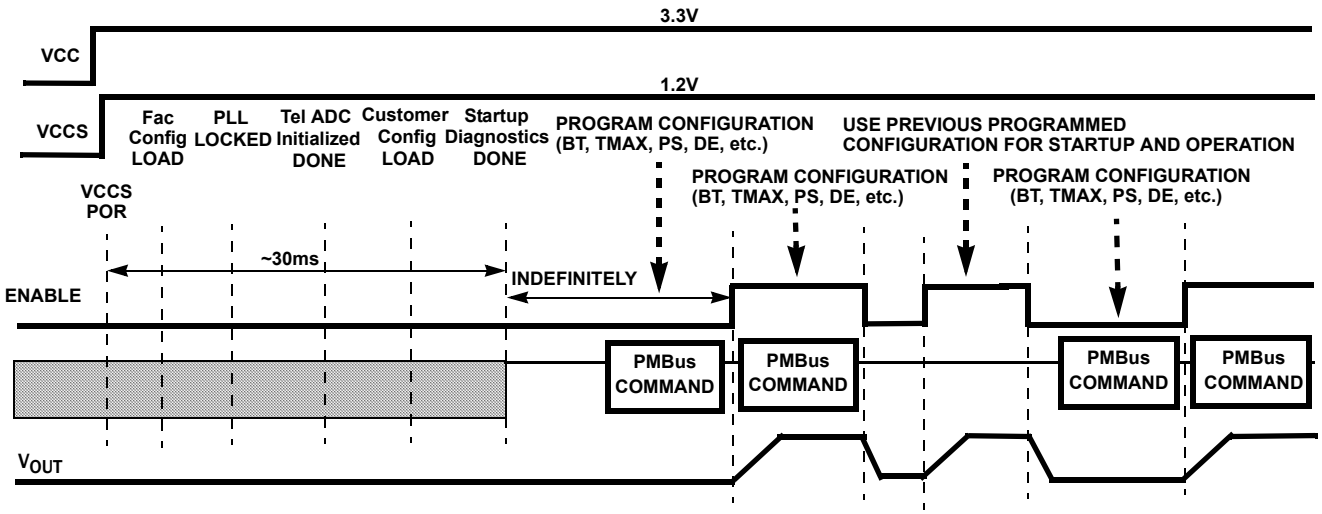
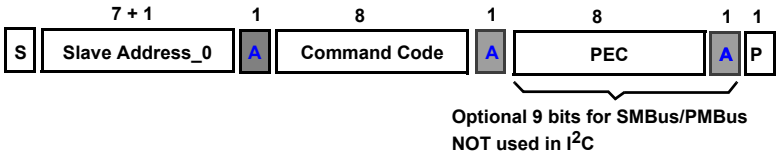



**FIGURE 27. SIMPLIFIED PMBus INITIALIZATION TIMING DIAGRAM**

# PMBus Protocol

### 1. Send Byte Protocol

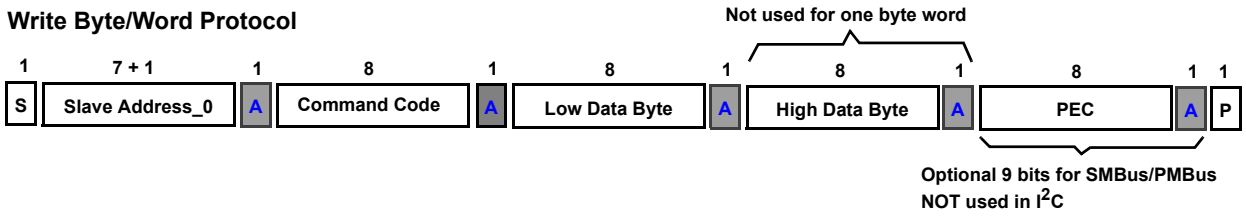



S: Start Condition
A: Acknowledge (“0”)
N: Not Acknowledge (“1”)
W: Write (“0”)
RS: Repeated Start Condition
R: Read (“1”)
PEC: Packet Error Checking
P: Stop Condition

Acknowledge or DATA from Slave, ISL68127 Controller

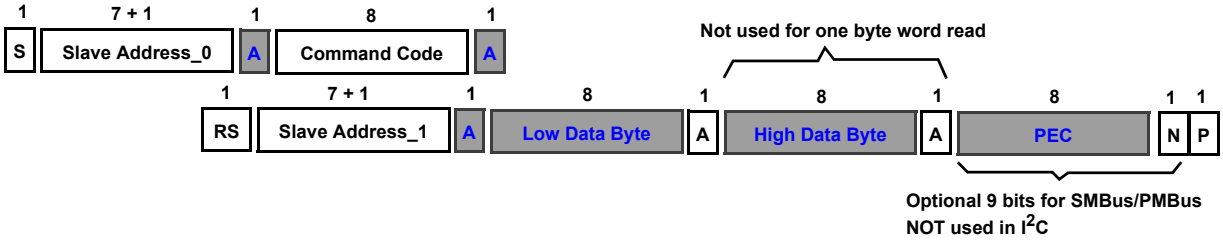
Example command: 03h Clear Faults
(This clears all of the bits in Status Byte for the selected rail)

### 2. Write Byte/Word Protocol




Example command: 21h VOUT_COMMAND

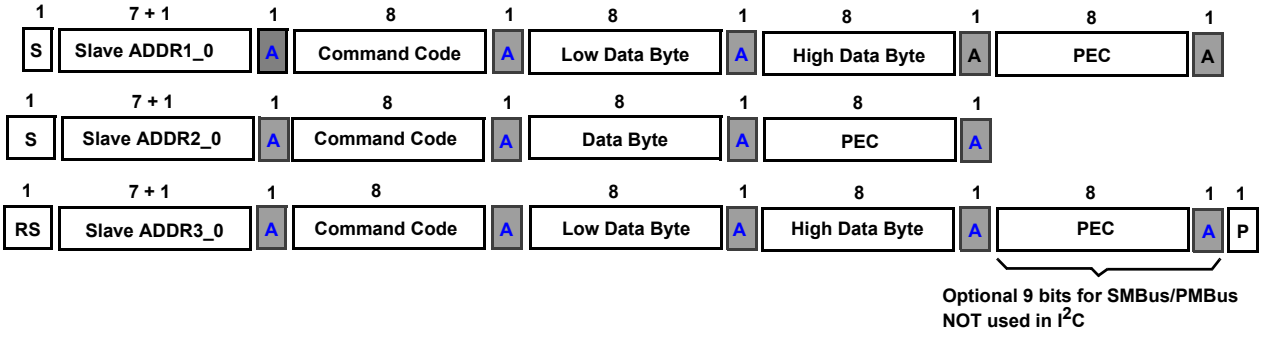
### 3. Read Byte/Word Protocol



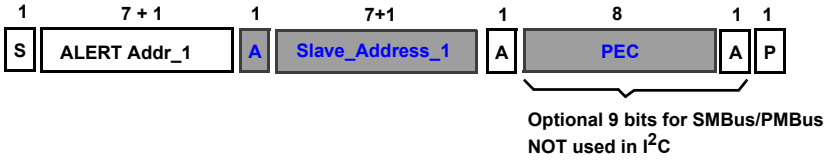

Example command: 8B READ_VOUT (Two words, read voltage of the selected rail).

The STOP (P) bit is NOT allowed before the repeated START condition when “reading” contents of a register.

### 4. Group Command Protocol - No more than one command can be sent to the same Address




### 5. Alert Response Address (ARA, 0001_1001, 25h) for SMBus and PMBus, not used for $I^2C$



# PMBus Command Summary

| CODE | COMMAND NAME | DESCRIPTION | TYPE | DATA FORMAT | DEFAULT VALUE | DEFAULT SETTING |
|---|---|---|---|---|---|---|
| 00h | PAGE | Selects Output 0, 1, or both | R/W | Bit Field | 00h | Page 0 |
| 01h | OPERATION | Enable/disable, margin settings | R/W | Bit Field | 08h | Off |
| 02h | ON_OFF_CONFIG | On/off configuration settings | R/W | Bit Field | 16h | ENABLE pin control |
| 03h | CLEAR_FAULTS | Clears all fault bits in all registers and releases the SALRT pin | Write | N/A | N/A | |
| 10h | WRITE_PROTECT | Gives write protection to sets of commands | R/W | Bit Field | 00h | No write protection |
| 20h | VOUT_MODE | Defines the format for output voltage related commands | Read | Bit Field | 40h | Direct format |
| 21h | VOUT_COMMAND | Sets the nominal $V_{OUT}$ target | R/W | Direct | 0384h | 900mV |
| 22h | VOUT_TRIM | Applies trim voltage to $V_{OUT}$ set-point | R/W | Direct | 0000h | 0mV |
| 24h | VOUT_MAX | Absolute maximum voltage setting | R/W | Direct | 08FCh | 2300mV |
| 25h | VOUT_MARGIN_HIGH | Sets $V_{OUT}$ target during margin high | R/W | Direct | 0640h | 1600mV |
| 26h | VOUT_MARGIN_LOW | Sets $V_{OUT}$ target during margin low | R/W | Direct | 00FAh | 250mV |
| 27h | VOUT_TRANSITION_RATE | Slew rate setting for $V_{OUT}$ changes | R/W | Direct | 0064h | 10mV/µs |
| 28h | VOUT_DROOP | Sets the load line (V/I slope) resistance for the output | R/W | Direct | 0000h | 0µV/A |
| 2Bh | VOUT_MIN | Absolute minimum target voltage setting | R/W | Direct | 0000h | 0mV |
| 40h | VOUT_OV_FAULT_LIMIT | Sets the $V_{OUT}$ overvoltage fault threshold | R/W | Direct | 076Ch | 1900mV |
| 44h | VOUT_UV_FAULT_LIMIT | Sets the $V_{OUT}$ undervoltage fault threshold | R/W | Direct | 0000h | 0mV |
| 4Fh | OT_FAULT_LIMIT | Sets the over-temperature fault threshold | R/W | Direct | 007Dh | +125°C |
| 51h | OT_WARN_LIMIT | Sets the over-temperature warn threshold | R/W | Direct | 07D0h | +2000°C |
| 55h | VIN_OV_FAULT_LIMIT | Sets the $V_{IN}$ overvoltage fault threshold | R/W | Direct | 36B0h | 14,000mV |
| 59h | VIN_UV_FAULT_LIMIT | Sets the $V_{IN}$ undervoltage fault threshold | R/W | Direct | 1F40h | 8,000mV |
| 5Bh | IIN_OC_FAULT_LIMIT | Sets the $I_{IN}$ overcurrent fault threshold | R/W | Direct | 0032h | 50A |
| 60h | TON_DELAY | Sets the delay time from enable to $V_{OUT}$ rise | R/W | Direct | 0014h | 200µs |
| 61h | TON_RISE | Turn-on rise time | R/W | Direct | 01F4h | 500µs |
| 64h | TOFF_DELAY | Turn-off delay time | R/W | Direct | 0000h | 0µs |
| 65h | TOFF_FALL | Turn-off fall time | R/W | Direct | 01F4h | 500µs |
| 78h | STATUS_BYTE | First byte of STATUS_WORD | Read | Bit Field | N/A | N/A |
| 79h | STATUS_WORD | Summary of critical faults | Read | Bit Field | N/A | N/A |
| 7Ah | STATUS_VOUT | Reports $V_{OUT}$ faults | Read | Bit Field | N/A | N/A |
| 7Bh | STATUS_IOUT | Reports $I_{OUT}$ faults | Read | Bit Field | N/A | N/A |
| 7Ch | STATUS_INPUT | Reports input faults | Read | Bit Field | N/A | N/A |
| 7Dh | STATUS_TEMPERATURE | Reports temperature warnings/faults | Read | Bit Field | N/A | N/A |
| 7Eh | STATUS_CML | Reports communication, memory, and logic errors | Read | Bit Field | N/A | N/A |
| 80h | STATUS_MFR_SPECIFIC | Reports specific events | Read | Bit Field | N/A | N/A |
| 88h | READ_VIN | Reports input voltage measurement | Read | Direct | N/A | N/A |
| 89h | READ_IIN | Reports input current measurement | Read | Direct | N/A | N/A |
| 8Bh | READ_VOUT | Reports output voltage measurement | Read | Direct | N/A | N/A |
| 8Ch | READ_IOUT | Reports output current measurement | Read | Direct | N/A | N/A |

# PMBus Command Summary (Continued)

| CODE | COMMAND NAME | DESCRIPTION | TYPE | DATA FORMAT | DEFAULT VALUE | DEFAULT SETTING |
|---|---|---|---|---|---|---|
| 8Dh | READ_TEMPERATURE_1 | Reports power stage temperature measurement | Read | Direct | N/A | N/A |
| 8Eh | READ_TEMPERATURE_2 | Reports TMON0 temperature measurement | Read | Direct | N/A | N/A |
| 8Fh | READ_TEMPERATURE_3 | Reports TMON1 temperature measurement | Read | Direct | N/A | N/A |
| 96h | READ_POUT | Reports output power | Read | Direct | N/A | N/A |
| 97h | READ_PIN | Reports input power | Read | Direct | N/A | N/A |
| 98h | PMBUS_REVISION | Reports specific events | Read | Bit Field | 33h | Revision 1.3 |
| ADh | IC_DEVICE_ID | Reports device identification information | Block Read | Bit Field | 49D22800h | ISL68127 |
| AEh | IC_DEVICE_REV | Reports device revision information | Block Read | Bit Field | N/A | N/A |
| E7h | APPLY_SETTINGS | Instructs device to apply PMBus configuration changes | Write | Bit Field | N/A | N/A |
| F2h | RESTORE_CONFIG | Allows selection of configurations from NVM | Write | Bit Field | N/A | N/A |

## PMBus Use Guidelines

All commands can be read at any time.

Always disable the outputs when writing commands that change device settings. Exceptions to this rule are commands intended to be written while the device is enabled, for example, OPERATION.

## PMBus Data Formats

### Direct (D)

The Direct data format is a 2-byte two's complement binary integer.

### Bit Field (BIT)

A description of Bit Field is provided in "PMBus Command Detail" on page 24.

# PMBus Command Detail

## PAGE (00h)

**Definition:** Selects Controller 0, Controller 1, or both Controllers 0 and 1 to receive commands. All commands following this command are received and acted on by the selected controller or controllers.

**Data Length in Bytes:** 1

**Data Format:** Bit Field

**Type:** R/W

**Default Value:** 00h

| COMMAND | PAGE (00h) | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Format | Bit Field | | | | | | | |
| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | See Following Table | | | | | | | |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| BITS 7:4 | BITS 3:0 | PAGE |
|---|---|---|
| 0000 | 0000 | 0 |
| 0000 | 0001 | 1 |
| 1111 | 1111 | Both |

## OPERATION (01h)

**Definition:** Sets the enable state when configured for PMBus enable. Sets output voltage margin settings. The device always acts on faults during margin. The following table reflects the valid settings for the device.

**Paged or Global:** Paged

**Data Length in Bytes**: 1

**Data Format**: Bit Field

**Type**: R/W

**Default Value**: 08h

| COMMAND | OPERATION (01h) | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Format | Bit Field | | | | | | | |
| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | See Following Table | | | | | | | |
| Default Value | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |

| BIT NUMBER | PURPOSE | BIT VALUE | MEANING |
|---|---|---|---|
| Bits 7:6 | Enable/Disable | 00 | Immediate off (decay) |
| | | 01 | Soft-off (Use TOFF_DELAY and TOFF_FALL) |
| | | 10 | On |
| Bits 5:4 | $V_{OUT}$ Source | 00 | VOUT_COMMAND |
| | | 01 | VOUT_MARGIN_LOW |
| | | 10 | VOUT_MARGIN_HIGH |
| | | 11 | Not used |
| Bits 3:2 | Margin Response | 10 | Act on faults |
| Bit 1:0 | Not Used | 0 | Not used |

## ON_OFF_CONFIG (02h)

**Definition:** Configures the interpretation of the "OPERATION (01h)" command and the ENABLE pin (EN).

**Paged or Global:** Global

**Data Length in Bytes:** 1

**Data Format:** Bit Field

**Type:** R/W

**Default Value:** 16h (ENABLE pin control)

| COMMAND | ON_OFF_CONFIG (02h) | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Format | Bit Field | | | | | | | |
| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | See Following Table | | | | | | | |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| BIT NUMBER | PURPOSE | BIT VALUE | MEANING |
|---|---|---|---|
| 7:5 | Not Used | 000 | Not Used |
| 4:2 | Sets the Source of Enable | 000 | Device always enabled regardless of pin or OPERATION command state |
| | | 101 | Device starts from Enable pin only |
| | | 110 | Device starts from OPERATION command only |
| | | 111 | Device starts from OPERATION command AND Enable pin |
| 1 | Enable Pin Polarity | 1 | Active high only |
| 0 | Enable Pin Turn-Off Action | 1 | Turns off immediately with decay |
| | | 0 | Uses programmed "TOFF_DELAY (64h)" and "TOFF_FALL (65h)" settings |

## CLEAR_FAULTS (03h)

**Definition:** Clears all fault bits in all registers and releases the SALRT pin (if asserted) simultaneously. If a fault condition still exits, the bit reasserts immediately. This command does not restart a device if it is shut down, it only clears the faults.

**Paged or Global:** Global

**Data Length in Bytes:** 0

**Data Format:** N/A

**Type:** Write Only

**Default Value:** N/A

## WRITE_PROTECT (10h)

**Definition:** Sets the write protection of certain configuration commands.
**Paged or Global:** Global
**Data Length in Bytes:** 1
**Data Format:** Bit Field
**Type:** R/W
**Default Value:** 00h (Enable all writes)

| COMMAND | WRITE_PROTECT (10h) | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Format | Bit Field | | | | | | | |
| Bit Position | 7 | 6 | 5 | 4 | 3:0 | 2 | 1 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | See Following Table | | | | | | | |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| SETTINGS | PROTECTION |
|---|---|
| 40h | Disables all writes except to WRITE_PROTECT, "OPERATION (01h)", "CLEAR_FAULTS (03h)", and "PAGE (00h)" |
| 20h | Disables all writes except all above plus "ON_OFF_CONFIG (02h)", "VOUT_COMMAND (21h)", and "VOUT_TRIM (22h)" |
| 00h | Enables all writes |

NOTE: Any settings other than the three shown in the table cause an invalid data fault.

## VOUT_MODE (20h)

**Definition:** Returns the supported $V_{OUT}$ mode. This device supports absolute direct mode only.
**Paged or Global:** Global
**Data Length in Bytes:** 1
**Data Format:** Bit Field
**Type:** Read Only
**Default Value:** 40h
**Units:** N/A
**Equation:** N/A

## VOUT_COMMAND (21h)

**Definition:** Sets the value of $V_{OUT}$ when the "OPERATION (01h)" command is configured for nominal operation.
**Paged or Global:** Paged
**Data Length in Bytes:** 2
**Data Format:** Direct
**Type:** R/W
**Default Value:** 0384h (900mV)
**Units:** mV
**Equation:** VOUT_COMMAND = (Direct value)
**Range:** "VOUT_MIN (2Bh)" to "VOUT_MAX (24h)"

| COMMAND | VOUT_COMMAND (21h) | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | Unsigned Integer | | | | | | | | | | | | | | | |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

## VOUT_TRIM (22h)

**Definition:** Sets a fixed trim voltage to the output voltage command value. This command is typically used to calibrate a device in the application circuit.

**Paged or Global:** Paged

**Data Length in Bytes:** 2

**Data Format:** Direct

**Type:** R/W

**Default Value:** 0000h (0mV)

**Units:** mV

**Equation:** VOUT_TRIM = (Direct value)

**Range**: ±250mV

| COMMAND | VOUT_TRIM (22h) | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | Two's Complement Integer | | | | | | | | | | | | | | | |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

## VOUT_MAX (24h)

**Definition:** Sets the maximum allowed $V_{OUT}$ target regardless of any other commands or combinations.

**Paged or Global:** Paged

**Data Length in Bytes:** 2

**Data Format:** Direct

**Type**: R/W

**Default Value:** 08FCh (2300mV)

**Units:** mV

**Equation:** VOUT_MAX = (Direct value)

**Range**: 0mV to 3300mV

| COMMAND | VOUT_MAX (24h) | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | Unsigned Integer | | | | | | | | | | | | | | | |
| Default Value | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |

## VOUT_MARGIN_HIGH (25h)

**Definition:** Sets the value of $V_{OUT}$ when the "OPERATION (01h)" command is configured for margin high.
**Paged or Global:** Paged
**Data Length in Bytes:** 2
**Data Format:** Direct
**Type**: R/W
**Default Value:** 0640h (1600mV)
**Units:** mV
**Equation:** VOUT_MARGIN_HIGH = (Direct value)
**Range**: "VOUT_MIN (2Bh)" to "VOUT_MAX (24h)"

| COMMAND | VOUT_MARGIN_HIGH (25h) | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | Unsigned Integer | | | | | | | | | | | | | | | |
| Default Value | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |

## VOUT_MARGIN_LOW (26h)

**Definition:** Sets the value of $V_{OUT}$ when the "OPERATION (01h)" command is configured for margin low.
**Paged or Global:** Paged
**Data Length in Bytes:** 2
**Data Format:** Direct
**Type**: R/W
**Default Value:** 00FAh (250mV)
**Units:** mV
**Equation:** VOUT_MARGIN_LOW = (Direct value)
**Range**: "VOUT_MIN (2Bh)" to "VOUT_MAX (24h)"

| COMMAND | VOUT_MARGIN_LOW (26h) | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | Unsigned Integer | | | | | | | | | | | | | | | |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 |

## VOUT_TRANSITION_RATE (27h)

**Definition:** Sets the output voltage rate of change during regulation. Changes to this setting require a write to the "APPLY_SETTINGS (E7h)" command before the change takes effect.

**Paged or Global:** Paged

**Data Length in Bytes:** 2

**Data Format:** Direct

**Type**: R/W

**Default Value:** 0064h (10mV/µs)

**Units:** µV/µs

**Equation:** VOUT_TRANSITION_RATE = (Direct value) x 100

**Range**: 100µV/µs to 100mV/µs

| COMMAND | VOUT_TRANSITION_RATE (27h) | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | Unsigned Integer | | | | | | | | | | | | | | | |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 |

## VOUT_DROOP (28h)

**Definition**: Sets the output voltage rate of change during regulation. Changes to this setting require a write to the "APPLY_SETTINGS (E7h)" command before the change takes effect.

**Paged or Global:** Paged

**Data Length in Bytes:** 2

**Data Format:** Direct

**Type**: R/W

**Default Value:** 0000h (0µV/A)

**Units:** µV/A

**Equation:** VOUT_DROOP = (Direct value) x 10

**Range**: 0mV/A to 16mV/A

| COMMAND | VOUT_DROOP (28h) | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | Unsigned Integer | | | | | | | | | | | | | | | |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

## VOUT_MIN (2Bh)

**Definition:** Sets the minimum allowed $V_{OUT}$ target regardless of any other commands or combinations.

**Paged or Global:** Paged

**Data Length in Bytes:** 2

**Data Format:** Direct

**Type**: R/W

**Default Value:** 0000h (0mV)

**Units:** mV

**Equation:** VOUT_MIN = (Direct value)

**Range**: 0V to "VOUT_MAX (24h)"

| COMMAND | VOUT_MIN (2Bh) | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | Unsigned Integer | | | | | | | | | | | | | | | |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

## VOUT_OV_FAULT_LIMIT (40h)

**Definition:** Sets the output overvoltage fault threshold. Changes to this setting require a write to the APPLY_SETTINGS command before the change takes effect.

**Paged or Global:** Paged

**Data Length in Bytes:** 2

**Data Format:** Direct

**Type**: R/W

**Default Value:** 076Ch (1900mV)

**Units:** mV

**Equation:** VOUT_OV_FAULT_LIMIT = (Direct value)

**Range**: 0V to "VOUT_MAX (24h)"

| COMMAND | VOUT_OV_FAULT_LIMIT (40h) | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | Unsigned Integer | | | | | | | | | | | | | | | |
| Default Value | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 |

## VOUT_UV_FAULT_LIMIT (44h)

**Definition:** Sets the $V_{OUT}$ undervoltage fault threshold. This fault is masked during ramp or when disabled.

**Paged or Global:** Paged

**Data Length in Bytes:** 2

**Data Format:** Direct

**Type**: R/W

**Default Value:** 0000h (0mV)

**Units:** mV

**Equation:** VOUT_UV_FAULT_LIMIT = (Direct value)

**Range**: 0V to "VOUT_MAX (24h)"

| COMMAND | VOUT_UV_FAULT_LIMIT (44h) | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | Unsigned Integer | | | | | | | | | | | | | | | |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

## OT_FAULT_LIMIT (4Fh)

**Definition:** Sets the power stage over-temperature fault limit.

**Paged or Global:** Paged

**Data Length in Bytes:** 2

**Data Format:** Direct

**Type**: R/W

**Default Value:** 007Dh (+125°C)

**Units:** °C

**Equation:** OT_FAULT_LIMIT = (Direct value)

**Range**: 0°C to +2000°C

| COMMAND | OT_FAULT_LIMIT (4Fh) | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | Two's Complement Integer | | | | | | | | | | | | | | | |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 |

## OT_WARN_LIMIT (51h)

**Definition:** Sets the system over-temperature warn limit. If any measured temperature exceeds this value, the device does the following:

- Sets the TEMPERATURE bit in "STATUS_BYTE (78h)" and "STATUS_WORD (79h)"
- Sets the OT_WARNING bit in "STATUS_TEMPERATURE (7Dh)"
- Sets the SALRT pin
- Sets the TWARN pin

**Paged or Global:** Paged
**Data Length in Bytes:** 2
**Data Format:** Direct
**Type**: R/W
**Default Value:** 07D0h (+2000°C)
**Units:** °C
**Equation:** OT_WARN_LIMIT = (Direct value)
**Range**: 0°C to +2000°C

| COMMAND | OT_WARN_LIMIT (51h) | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | Two's Complement Integer | | | | | | | | | | | | | | | |
| Default Value | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 |

## VIN_OV_FAULT_LIMIT (55h)

**Definition:** Sets the $V_{IN}$ overvoltage fault threshold. Changes to this setting require a write to the "APPLY_SETTINGS (E7h)" command before the change takes effect.
**Paged or Global:** Global
**Data Length in Bytes:** 2
**Data Format:** Direct
**Type:** R/W
**Default Value:** 36B0h (14000mV)
**Units:** mV
**Equation:** VIN_OV_FAULT_LIMIT = (Direct value)
**Range**: 0mV to 16000mV

| COMMAND | VIN_OV_FAULT_LIMIT (55h) | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | Unsigned Integer | | | | | | | | | | | | | | | |
| Default Value | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

## VIN_UV_FAULT_LIMIT (59h)

**Definition:** Sets the $V_{IN}$ undervoltage fault threshold. Also referred to as Undervoltage Lockout (UVLO). Changes to this setting require a write to the "APPLY_SETTINGS (E7h)" command before the change takes effect.

**Paged or Global:** Global

**Data Length in Bytes:** 2

**Data Format:** Direct

**Type:** R/W

**Default Value:** 1F40h (8,000mV)

**Units:** mV

**Equation:** VIN_UV_FAULT_LIMIT = (Direct value)

**Range**: 0mV to 16000mV

| COMMAND | VIN_UV_FAULT_LIMIT (59h) | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | Unsigned Integer | | | | | | | | | | | | | | | |
| Default Value | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |

## IIN_OC_FAULT_LIMIT (5Bh)

**Definition:** Sets the $I_{IN}$ overcurrent fault threshold. Changes to this setting require a write to the "APPLY_SETTINGS (E7h)" command before the change takes effect.

**Paged or Global:** Global

**Data Length in Bytes:** 2

**Data Format:** Direct

**Type:** R/W

**Default Value:** 0032h (50A)

**Units:** A

**Equation:** IIN_OC_FAULT_LIMIT = (Direct value)

**Range**: 0A to 50A

| COMMAND | IIN_OC_FAULT_LIMIT (5Bh) | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | Unsigned Integer | | | | | | | | | | | | | | | |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 |

## TON_DELAY (60h)

**Definition:** Sets the delay time of $V_{OUT}$ during enable.

**Paged or Global:** Paged

**Data Length in Bytes:** 2

**Data Format:** Direct

**Type**: R/W

**Default Value:** 0014h (200µs)

**Units:** µs

**Equation:** TON_DELAY = (Direct value) x 10

**Range**: 200µs to 655340µs

| COMMAND | TON_DELAY (60h) | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | Unsigned Integer | | | | | | | | | | | | | | | |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 |

## TON_RISE (61h)

**Definition:** Sets the rise time of $V_{OUT}$ during enable. Changes to this setting require a write to the "APPLY_SETTINGS (E7h)" command before the change takes effect. This function uses the value of $V_{OUT}$ to calculate rise time, so APPLY_SETTINGS must be sent after any change to the $V_{OUT}$ target for accurate rise time.

**Paged or Global:** Paged

**Data Length in Bytes:** 2

**Data Format:** Direct

**Type**: R/W

**Default Value:** 01F4h (500µs)

**Units:** µs

**Equation:** TON_RISE = (Direct value)

**Range**: 0µs to 10000µs

| COMMAND | TON_RISE (61h) | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | Unsigned Integer | | | | | | | | | | | | | | | |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 |

## TOFF_DELAY (64h)

**Definition:** Sets the delay time of $V_{OUT}$ during disable.

**Paged or Global:** Paged

**Data Length in Bytes:** 2

**Data Format:** Direct

**Type**: R/W

**Default Value:** 0000h (0µs)

**Units:** µs

**Equation:** TOFF_DELAY = (Direct value) x10

**Range**: 0µs to 10000µs

| COMMAND | TOFF_DELAY (64h) | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | Unsigned Integer | | | | | | | | | | | | | | | |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

## TOFF_FALL (65h)

**Definition:** Sets the fall time of $V_{OUT}$ during disable. Changes to this setting require a write to the "APPLY_SETTINGS (E7h)" command before the change takes effect. This function uses the value of $V_{OUT}$ to calculate fall time, so APPLY_SETTINGS must be sent after any change to the $V_{OUT}$ target for accurate fall time.

**Paged or Global:** Paged

**Data Length in Bytes:** 2

**Data Format:** Direct

**Type**: R/W

**Default Value:** 01F4h (500µs)

**Units:** µs

**Equation:** TOFF_FALL = (Direct value)

**Range**: 0 to 10000µs

| COMMAND | TOFF_FALL (65h) | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | Unsigned Integer | | | | | | | | | | | | | | | |
| Default Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 |

## STATUS_BYTE (78h)

**Definition:** Returns a summary of the unit's fault status. Based on the information in this byte, the host can get more information by reading the appropriate status registers. A fault in either output is reported in this register.

**Paged or Global:** Global

**Data Length in Bytes:** 2

**Data Format:** Bit Field

**Type**: Read Only

**Default Value:** N/A

| COMMAND | STATUS_BYTE (78h) | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Format | Bit Field | | | | | | | |
| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R | R | R | R | R | R | R | R |
| Function | See Following Table | | | | | | | |

| BIT NUMBER | STATUS BIT NAME | MEANING |
|---|---|---|
| 7 | Not Used | Not used. |
| 6 | OFF | This bit is asserted if the unit is not providing power to the output, regardless of the reason, including simply not being enabled. |
| 5 | VOUT_OV_FAULT | An output overvoltage fault occurred. |
| 4 | IOUT_OC_FAULT | An output overcurrent fault occurred. |
| 3 | VIN_UV_FAULT | An input undervoltage fault occurred. |
| 2 | TEMPERATURE | A temperature fault or warning occurred. |
| 1 | CML | A communications, memory, or logic fault occurred. |
| 0 | None of the Above | A status change other than those listed above occurred. |

## STATUS_WORD (79h)

**Definition:** Returns a summary of the device's fault status. Based on the information in these bytes, the host can get more information by reading the appropriate status registers. A fault in either output is reported in this register. The low byte of STATUS_WORD contains the same information as the "STATUS_BYTE (78h)" command.

**Paged or Global:** Global

**Data Length in Bytes:** 2

**Data Format:** Bit Field

**Type**: Read Only

**Default Value:** N/A

| COMMAND | STATUS_WORD (79h) | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Format | Bit Field | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R |
| Function | See Following Table | | | | | | | | | | | | | | | |

| BIT NUMBER | STATUS BIT NAME | MEANING |
|---|---|---|
| 15 | $V_{OUT}$ | An output voltage fault occurred. |
| 14 | IOUT | An output current fault occurred. |
| 13 | INPUT | An input voltage fault occurred. |
| 12 | MFR_SPECIFIC | A manufacturer specific event occurred. |
| 11 | POWER_GOOD # | The POWER_GOOD signal, if present, is negated (Note 8). |
| 10:7 | Not Used | Not used. |
| 6 | OFF | This bit is asserted if the unit is not providing power to the output, regardless of the reason, including simply not being enabled. |
| 5 | VOUT_OV_FAULT | An output overvoltage fault occurred. |
| 4 | IOUT_OC_FAULT | An output overcurrent fault occurred. |
| 3 | VIN_UV_FAULT | An input undervoltage fault occurred. |
| 2 | TEMPERATURE | A temperature fault or warning occurred. |
| 1 | CML | A communications, memory, or logic fault occurred. |
| 0 | None of the Above | A status change other than those listed above occurred. |

NOTE:

8. If the POWER_GOOD# bit is set, this status indicates that the POWER_GOOD signal, if present, is signaling that the output power is not good.

## STATUS_VOUT (7Ah)

**Definition:** Returns a summary of output voltage faults.
**Paged or Global:** Paged
**Data Length in Bytes:** 1
**Data Format:** Bit Field
**Type**: Read Only
**Default Value:** N/A

| COMMAND | STATUS_VOUT (7Ah) | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Format | Bit Field | | | | | | | |
| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R | R | R | R | R | R | R | R |
| Function | See Following Table | | | | | | | |

| BIT NUMBER | STATUS BIT NAME | MEANING |
|---|---|---|
| 7 | VOUT_OV_FAULT | Indicates an output overvoltage fault. |
| 6:5 | Not Used | Not used. |
| 4 | VOUT_UV_FAULT | Indicates an output undervoltage fault. |
| 3 | VOUT_MAX Warning | Indicates an output voltage maximum warning. |
| 2:0 | Not Used | Not used. |

## STATUS_IOUT (7Bh)

**Definition:** Returns a summary of output current faults.
**Paged or Global:** Paged
**Data Length in Bytes:** 1
**Data Format:** Bit Field
**Type**: Read Only
**Default Value:** N/A

| COMMAND | STATUS_IOUT (7Bh) | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Format | Bit Field | | | | | | | |
| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R | R | R | R | R | R | R | R |
| Function | See Following Table | | | | | | | |

| BIT NUMBER | MEANING |
|---|---|
| 7 | An output overcurrent fault has occurred. |
| 6 | An output overcurrent and undervoltage fault has occurred. |
| 5:4 | Not used. |
| 3 | A current share fault has occurred. |
| 2:0 | Not used. |

## STATUS_INPUT (7Ch)

**Definition:** Returns a summary of input voltage faults.
**Paged or Global:** Global
**Data Length in Bytes:** 1
**Data Format:** Bit Field
**Type**: Read Only
**Default Value:** N/A

| COMMAND | STATUS_INPUT (7Ch) | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Format | Bit Field | | | | | | | |
| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R | R | R | R | R | R | R | R |
| Function | See Following Table | | | | | | | |

| BIT NUMBER | MEANING |
|---|---|
| 7 | An input overvoltage fault occurred. |
| 6:5 | Not used. |
| 4 | An input undervoltage fault occurred. This fault is initially masked until $V_{IN}$ exceeds the UV threshold. |
| 3 | Not used. |
| 2 | An input overcurrent fault occurred. |
| 1:0 | Not used. |

## STATUS_TEMPERATURE (7Dh)

**Definition:** Returns a summary of temperature related faults.
**Paged or Global:** Global
**Data Length in Bytes:** 1
**Data Format:** Bit Field
**Type**: Read Only
**Default Value:** N/A

| COMMAND | STATUS_TEMPERATURE (7Dh) | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Format | Bit Field | | | | | | | |
| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R | R | R | R | R | R | R | R |
| Function | See Following Table | | | | | | | |

| BIT NUMBER | MEANING |
|---|---|
| 7 | An over-temperature fault occurred. |
| 6 | An over-temperature warning occurred. |
| 5 | Not used. |
| 4 | An under-temperature fault occurred. |
| 3:0 | Not used. |

## STATUS_CML (7Eh)

**Definition:** Returns a summary of any communications, logic, and/or memory errors.

**Paged or Global:** Global

**Data Length in Bytes:** 1

**Data Format:** Bit Field

**Type**: Read Only

**Default Value:** N/A

| COMMAND | STATUS_CML (7Eh) | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Format | Bit Field | | | | | | | |
| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R | R | R | R | R | R | R | R |
| Function | See Following Table | | | | | | | |

| BIT NUMBER | MEANING |
|---|---|
| 7 | An invalid or unsupported PMBus Command was received. |
| 6 | The PMBus command was sent with invalid or unsupported data. |
| 5 | A packet error was detected in the PMBus command. |
| 4 | Memory fault detected. |
| 3 | Processor fault detected. |
| 2 | Not used. |
| 1 | A communication fault other than the ones listed in this table occurred. |
| 0 | A memory or logic fault not listed above was detected. |

## STATUS_MFR_SPECIFIC (80h)

**Definition:** Returns the status of specific information detailed as follows.

**Paged or Global:** Global

**Data Length in Bytes:** 1

**Data Format:** Bit Field

**Type:** Read Only

**Default Value:** N/A

| COMMAND | STATUS_MFR_SPECIFIC (80h) | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Format | Bit Field | | | | | | | |
| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R | R | R | R | R | R | R | R |
| Function | See Following Table | | | | | | | |

| BIT | MEANING |
|---|---|
| 7:2 | Not used |
| 1 | OTP NVM memory is full. |
| 0 | Not used |

## READ_VIN (88h)

**Definition:** Returns the input voltage reading.
**Paged or Global:** Global
**Data Length in Bytes:** 2
**Data Format:** Direct
**Type:** Read Only
**Default Value:** N/A
**Units:** mV
**Equation:** READ_VIN = (Direct value)

| COMMAND | READ_VIN (88h) | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R |
| Function | Two's Complement Integer | | | | | | | | | | | | | | | |

## READ_IIN (89h)

**Definition:** Returns the input current reading.
**Paged or Global:** Global
**Data Length in Bytes:** 2
**Data Format:** Direct
**Type:** Read Only
**Default Value:** N/A
**Units:** A
**Equation:** READ_IIN = (Direct value)/100

| COMMAND | READ_IIN (89h) | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R |
| Function | Two's Complement Integer | | | | | | | | | | | | | | | |

## READ_VOUT (8Bh)

**Definition:** Returns the output voltage reading.
**Paged or Global:** Paged
**Data Length in Bytes:** 2
**Data Format:** Direct
**Type:** Read Only
**Default Value:** N/A
**Units:** mV
**Equation:** READ_VOUT = (Direct value)

| COMMAND | READ_VOUT (8Bh) | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R |
| Function | Two's Complement Integer | | | | | | | | | | | | | | | |

## READ_IOUT (8Ch)

**Definition:** Returns the output current reading.
**Paged or Global:** Paged
**Data Length in Bytes:** 2
**Data Format:** Direct
**Type:** Read Only
**Default Value:** N/A
**Units:** A
**Equation:** READ_IOUT = (Direct value)/10

| COMMAND | READ_IOUT (8Ch) | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R |
| Function | Two's Complement Integer | | | | | | | | | | | | | | | |

## READ_TEMPERATURE_1 (8Dh)

**Definition:** Returns the temperature reading of the power stage.
**Paged or Global:** Paged
**Data Length in Bytes:** 2
**Data Format:** Direct
**Type:** Read Only
**Default Value:** N/A
**Units:** °C
**Equation:** READ_TEMPERATURE_1 = (Direct value)

| COMMAND | READ_TEMPERATURE_1 (8Dh) | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R |
| Function | Two's Complement Integer | | | | | | | | | | | | | | | |

## READ_TEMPERATURE_2 (8Eh)

**Definition:** Returns the temperature reading from a remote diode connected to TMON0 when configured for diode sensing.
**Paged or Global:** Global
**Data Length in Bytes:** 2
**Data Format:** Direct
**Type:** Read Only
**Default Value:** N/A
**Units:** °C
**Equation:** READ_TEMPERATURE_2 = (Direct value)

| COMMAND | READ_TEMPERATURE_2 (8Eh) | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R |
| Function | Two's Complement Integer | | | | | | | | | | | | | | | |

## READ_TEMPERATURE_3 (8Fh)

**Definition:** Returns the temperature reading from a remote diode connected to TMON1 when configured for diode sensing.
**Paged or Global:** Global
**Data Length in Bytes:** 2
**Data Format:** Direct
**Type:** Read Only
**Default Value:** N/A
**Units:** °C
**Equation:** READ_TEMPERATURE_3 = (Direct value)

| COMMAND | READ_TEMPERATURE_3 (8Fh) | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R |
| Function | Two's Complement Integer | | | | | | | | | | | | | | | |

## READ_POUT (96h)

**Definition:** Returns the output power.
**Paged or Global:** Paged
**Data Length in Bytes:** 2
**Data Format:** Direct
**Type:** Read Only
**Default Value:** N/A
**Units:** W
**Equation:** READ_POUT = (Direct value)

| COMMAND | READ_POUT (96h) | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R |
| Function | Two's Complement Integer | | | | | | | | | | | | | | | |

## READ_PIN (97h)

**Definition:** Returns the input power.
**Paged or Global:** Global
**Data Length in Bytes:** 2
**Data Format:** Direct
**Type:** Read Only
**Default Value:** N/A
**Units:** W
**Equation:** READ_PIN = (Direct value)

| COMMAND | READ_PIN (97h) | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit Position | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R |
| Function | Two's Complement Integer | | | | | | | | | | | | | | | |

## PMBUS_REVISION (98h)

**Definition:** Returns the revision of the PMBus Specification to which the device is compliant.

**Data Length in Bytes:** 1

**Data Format:** Bit Field

**Type:** Read Only

**Default Value:** 33h (Part 1 Revision 1.3, Part 2 Revision 1.3)

| COMMAND | PMBUS_REVISION (98h) | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Format | Bit Field | | | | | | | |
| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R | R | R | R | R | R | R | R |
| Function | See Following Table | | | | | | | |
| Default Value | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |

| BITS 7:4 | PART 1 REVISION | BITS 3:0 | PART 2 REVISION |
|---|---|---|---|
| 0000 | 1.0 | 0000 | 1.0 |
| 0001 | 1.1 | 0001 | 1.1 |
| 0010 | 1.2 | 0010 | 1.2 |
| 0011 | 1.3 | 0011 | 1.3 |

## IC_DEVICE_ID (ADh)

**Definition:** Returns device identification information.

**Paged or Global:** Global

**Data Length in Bytes:** 4

**Data Format:** Bit Field

**Type:** Block Read

**Default Value:** 49D22800h

| COMMAND | IC_DEVICE_ID (ADh) | | | |
|---|---|---|---|---|
| Format | Block Read | | | |
| Byte Position | 3 | 2 | 1 | 0 |
| Function | MFR Code | ID High Byte | ID Low Byte | Reserved |
| Default Value | 49h | D2h | 28h | 00h |

## IC_DEVICE_REV (AEh)

**Definition:** Returns device revision information.

**Paged or Global:** Global

**Data Length in Bytes:** 4

**Data Format:** Bit Field

**Type:** Block Read

**Default Value:** N/A

| COMMAND | IC_DEVICE_REV (AEh) | | | |
|---|---|---|---|---|
| Format | Block Read | | | |
| Bit Position | 23:16 | 15:8 | 7:4 | 3:0 |
| Function | Firmware Revision | Factory Configuration | Chip Foundry Site | IC Revision |
| Default Value | N/A | N/A | N/A | N/A |

## APPLY_SETTINGS (E7h)

**Definition:** Instructs the controller to use new PMBus parameters. Send 01h to this command after making one or more changes to certain PMBus threshold commands that require rescaling of operational values. The commands that require this are:

- "VOUT_TRANSITION_RATE (27h)"
- "VOUT_DROOP (28h)"
- "VOUT_OV_FAULT_LIMIT (40h)"
- "VIN_OV_FAULT_LIMIT (55h)"
- "VIN_UV_FAULT_LIMIT (59h)"
- "IIN_OC_FAULT_LIMIT (5Bh)"
- "TON_RISE (61h)"
- "TOFF_FALL (65h)"

**Paged or Global:** Global
**Data Length in Bytes:** 2
**Data Format:** Bit Field
**Type:** Write Only
**Default Value:** 01h

## RESTORE_CONFIG (F2h)

**Definition:** Identifies the configuration to be restored from NVM and loads the store's settings into the device's active memory. This command must only be sent while the outputs are disabled.

**Paged or Global:** Global
**Data Length in Bytes:** 1
**Data Format:** BIT
**Type:** Write Only
**Default Value:** N/A

| COMMAND | RESTORE_CONFIG (F2h) | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Format | Bit Field | | | | | | | |
| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | See Following Table | | | | | | | |
| Default Value | N/A | N/A | N/A | N/A | N/A | N/A | N/A | N/A |

| BIT NUMBER | STATUS BIT NAME | MEANING |
|---|---|---|
| 7:4 | Reserved | Reserved |
| 3:0 | CONFIG | Selected configuration to restore |

# Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please visit our website to make sure you have the latest revision.

| DATE | REVISION | CHANGE |
|---|---|---|
| Jul 12, 2019 | FN8748.2 | On page 3, updated Ordering Information table by adding tape and reel parts, Tape and Reel column, and updating Note 1.<br>On page 4, changed the suggested typical resistor divider value for the VINSEN (pin 22) from 402k to 40.2k.<br>On page 13, added “Fast Phase Add Function” heading.<br>Removed About Intersil section.<br>Updated Renesas disclaimer. |
| Jun 26, 2017 | FN8748.1 | Applied new header and footer.<br>Updated “READ_PIN (97h)” on page 43, changed “Paged” to “Global”.<br>Updated the “Package Outline Drawing” section.<br>Updated Figure 5 on page 9.<br>Updated “Enable (EN0 and EN1) Input High Level” on page 10. Removed the typical value and added a minimum value of 2.55V.<br>Added an entry for “Enable (EN0 and EN1) Input Low Level” on page 10 with a maximum of 0.8V.<br>Added an entry for “SCL, SDA Input High Level” on page 11 with a minimum value of 1.55V.<br>Removed the entry for “SCL, SDA Input High/Low Threshold”.<br>Added an entry for “SCL, SDA Input Low Level” on page 11 with a maximum value of 0.8V.<br>Changed “STATUS_CML” on page 22, bit 1 from “PMBus command tried to write to a read only or protected command, or a communication fault other than the ones listed in this table has occurred” to “A communication fault other than the ones listed in this table has occurred”.<br>Changed “Two’s Complement Integer” to “Unsigned Integer” for the following PMBus commands:<br>- VOUT_COMMAND<br>- VOUT_MAX<br>- VOUT_MARGIN_HIGH<br>- VOUT_MARGIN_LOW<br>- VOUT_TRANSITION_RATE<br>- VOUT_DROOP<br>- VOUT_MIN<br>- VOUT_OV_FAULT_LIMIT<br>- VOUT_UV_FAULT_LIMIT<br>- VIN_OV_FAULT_LIMIT<br>- VIN_UV_FAULT_LIMIT<br>- IIN_OC_FAULT_LIMIT<br>- TON_DELAY<br>- TON_RISE<br>- TOFF_DELAY<br>- TOFF_FALL |
| Sep 28, 2016 | FN8748.0 | Initial release |

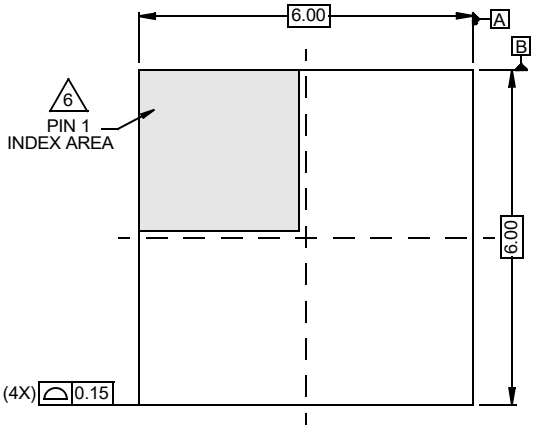
# Package Outline Drawing

For the most recent package outline drawing, see L48.6x6B.

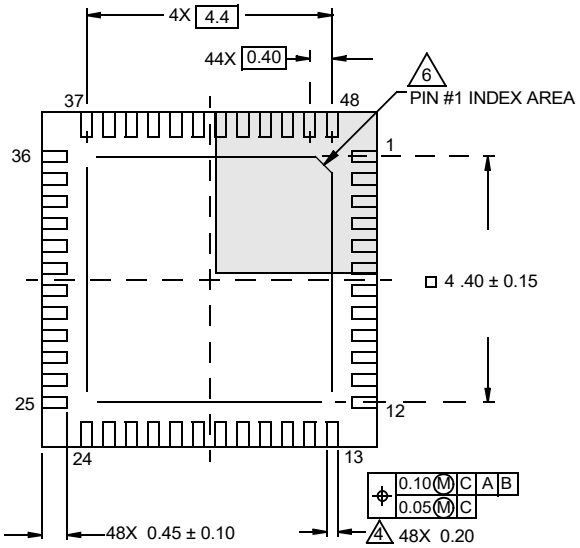
## L48.6x6B

**48 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE**

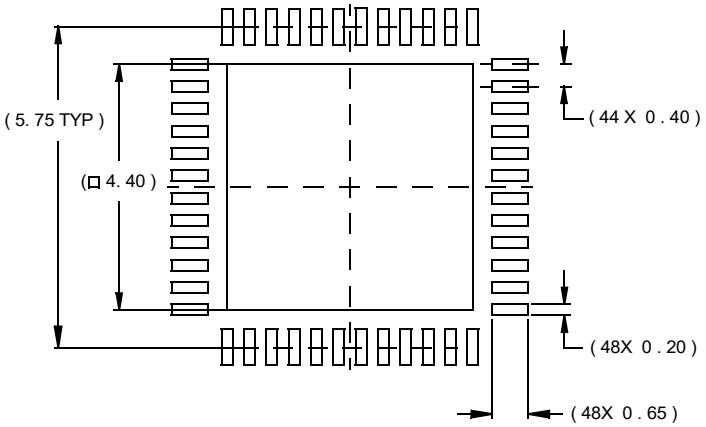
**Rev 0, 9/09**



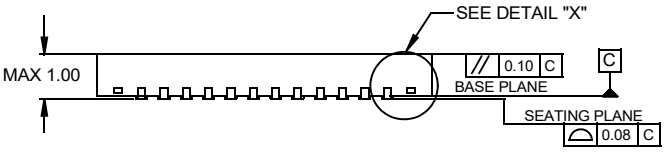

TOP VIEW



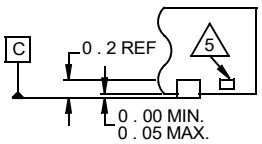

BOTTOM VIEW




TYPICAL RECOMMENDED LAND PATTERN




SIDE VIEW




DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

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(Rev.4.0-1 November 2017)

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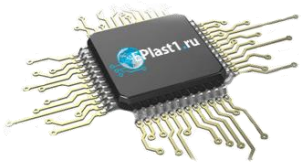


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