ZL81000
Dual BITS Transceiver and CC Receiver
Data Sheet

August 2018

General Description

ZL81000 provides two DS1/E1/2048kHz transceivers (transmitters plus receivers) specifically designed for BITS/SSU timing in carrier-class telecommunications equipment. Each transceiver provides full support for DS1, E1 and G.703 2048kHz synchronization signals in and out and includes SSM message insertion and extraction. The device also includes two composite clock (CC) receivers and two general-purpose CMOS clock inputs to provide additional support as needed for legacy interfaces.

Features

- **Two Independent Multi-Protocol BITS/SSU Transmitters and Receivers**
  - Receive and transmit DS1, E1, 2048 kHz, and 6312 kHz timing signals
  - Insert and extract SSM messages (DS1, E1)
  - DS1 SF or ESF formats
  - E1 FAS, CAS and/or CRC-4 framing
  - J1 support (DS1 with Japanese CRC-6 & RAI)
  - Short-haul and long-haul line interfaces
  - Internal software-selectable termination (75Ω, 100Ω, 110Ω, or 120Ω) or external termination
  - High-impedance receive inputs and transmit outputs for no-relay redundancy
  - Local and remote loopbacks
  - Jitter attenuator with configurable buffer depth, can be inserted into Tx path or Rx path
  - Receiver automatic receive sensitivity adjustment and signal level indication
  - Receiver LOS, OOF, RAI and AIS status
  - Transmitter flexible waveform generation
  - Transmitter DSX-1 line build-outs
  - Transmitter E1 waveforms include G.703 waveshapes for both 75Ω coax and 120Ω twisted pair cables
  - Transmitter AIS and alternating ones and zeros generation
  - Transmitter and receiver power-down controls
  - Transmitter and receiver short-circuit detection
  - Transmitter open-circuit detection
  - Internal loopbacks between transmitter and receiver for fault detection

Ordering Information

ZL81000GGG2	256 Pin CSBGA	Trays

Package size: 17 x 17 mm

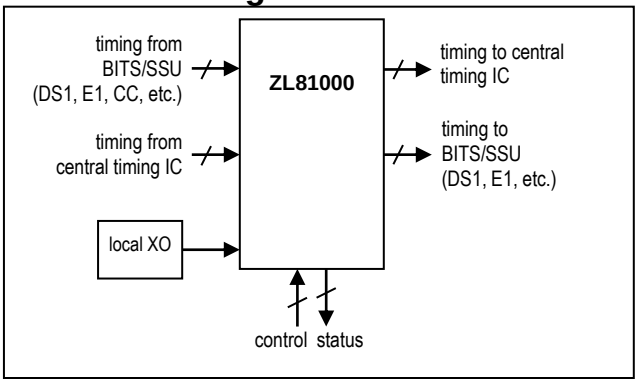
-40°C to +85°C

- **Two Composite Clock Receivers**
  - Compliant with Telcordia GR-378 composite clock, G.703 centralized clock, and G.703 Appendix II.1) Japanese sync interfaces
  - Configurable for 50% or 5/8 duty cycle, 1V or 3V pulse amplitude, and 110Ω/120Ω/133Ω termination
  - Monitored for LOS, AMI violations, presence or absence of 8 kHz component, and optionally the Japanese 400 Hz component
  - Followed by DPLL+APLL for jitter filtering and optional frequency conversion
- Two programmable-frequency inputs
- Operates from a single 12.8MHz local oscillator
- Processor interface: 8-bit Parallel or SPI serial
- 1.8V operation with 3.3V I/O (5V tolerant)
- Industrial operating temperature range

Applications

SONET/SDH ADMs, MSPPs, and MSSPs
Digital Cross-Connects
Service Provider Routers
Any carrier-grade telecom equipment with DS1, E1, 2048kHz or CC external timing interfaces

Functional Diagram



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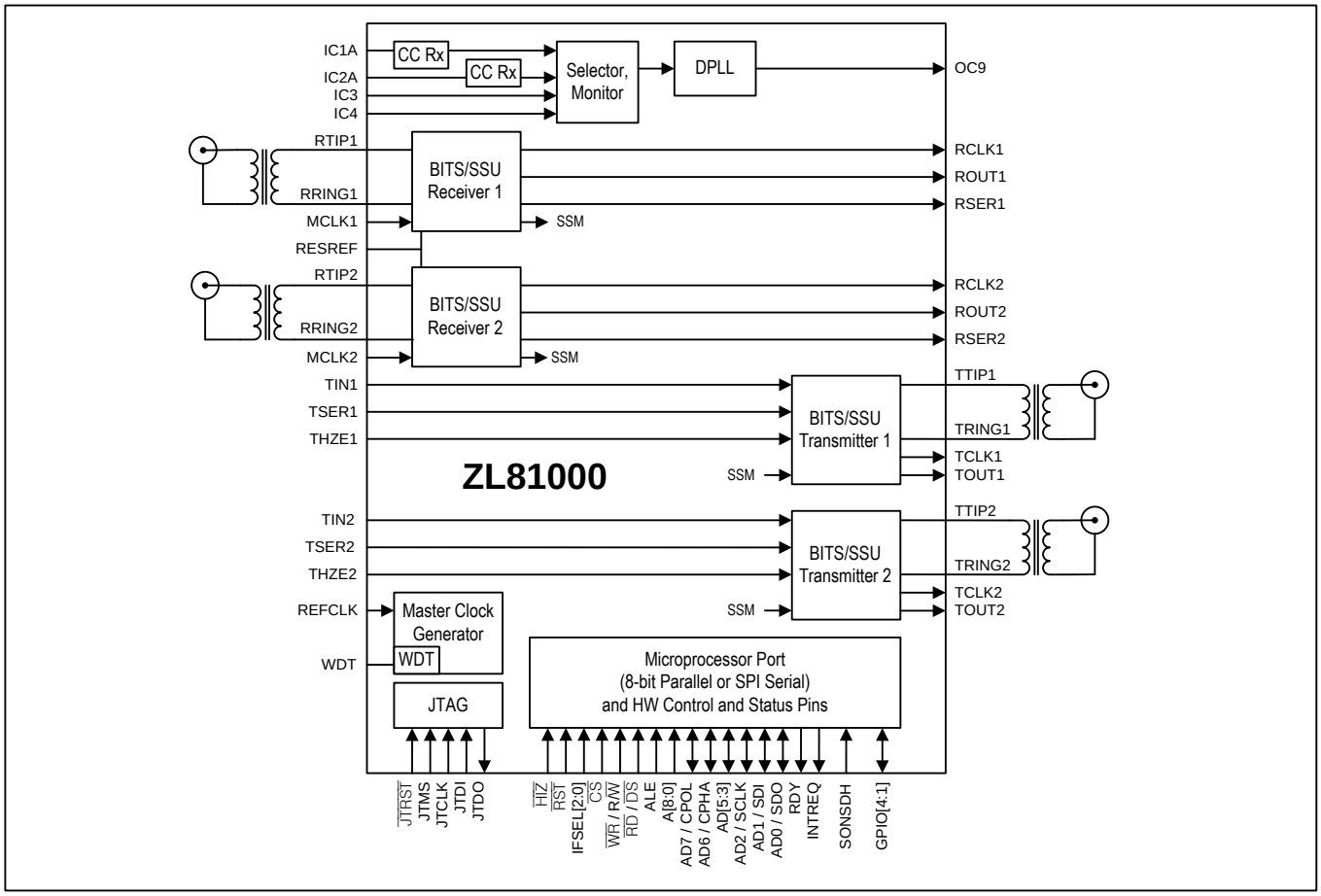
1. STANDARDS COMPLIANCE

Table 1-1. Applicable Telecom Standards

SPECIFICATION	SPECIFICATION TITLE
ANSI	
T1.101	*Synchronization Interface Standard*, 1999
T1.102	*Digital Hierarchy—Electrical Interfaces*, 1993
T1.107	*Digital Hierarchy—Formats Specification*, 1995
T1.231.02	*Digital Hierarchy—Layer 1 In-Service Digital Transmission Performance Monitoring*, 2003
T1.403	*Network and Customer Installation Interfaces—DS1 Electrical Interface*, 1999
AT&T	
TR62411	*ACCUNET® T1.5 Service Description and Interface Specification* (12/1990)
ETSI	
EN 300 417-6-1	*Transmission and Multiplexing (TM); Generic Requirements of Transport Functionality of Equipment; Part 6-1: Synchronization Layer Functions*, v1.1.3 (1999-05)
EN 300 462-3-1	*Transmission and Multiplexing (TM); Generic Requirements for Synchronization Networks; Part 3-1: The Control of Jitter and Wander within Synchronization Networks*, v1.1.1 (1998-05)
EN 300 462-5-1	*Transmission and Multiplexing (TM); Generic Requirements for Synchronization Networks; Part 5-1: Timing Characteristics of Slave Clocks Suitable for Operation in Synchronous Digital Hierarchy (SDH) Equipment*, v1.1.1 (1998-05)
IEEE	
IEEE 1149.1	*Standard Test Access Port and Boundary-Scan Architecture*, 1990
ITU-T	
G.703	*Physical/Electrical Characteristics of Hierarchical Digital Interfaces* (11/2001)
G.704	*Synchronous Frame Structures Used at 1544, 6312, 2048, 8448 and 44736 kbit/s Hierarchical Levels* (10/1998)
G.706	*Frame Alignment and Cyclic Redundancy Check (CRC) Procedures Relating to Basic Frame Structures Defined in Recommendation G.704* (1991)
G.775	*Loss of Signal (LOS) and Alarm Indication Signal (AIS) and Remote Defect Indication (RD) Defect Detection and Clearance Criteria for PDH Signals* (10/1998)
G.783	*ITU G.783 Characteristics of Synchronous Digital Hierarchy (SDH) Equipment Functional Blocks* (10/2000 plus Amendment 1 06/2002 and Corrigendum 2 03/2003)
G.823	*The Control of Jitter and Wander within Digital Networks which are Based on the 2048kbps Hierarchy* (03/2000)
G.824	*The Control of Jitter and Wander within Digital Networks which are Based on the 1544kbps Hierarchy* (03/2000)
G.825	*The Control of Jitter and Wander within Digital Networks which are Based on the Synchronous Digital Hierarchy (SDH)* (03/2000)
O.162	*Equipment to Perform In-Service Monitoring on 2048, 8448, 34,368 and 139,264 kbit/s Signals* (10/1992)
TELCORDIA	
GR-378-CORE	*Generic Requirements for Timing Signal Generators*, Issue 2, February 1999
GR-499-CORE	*Transport Systems Generic Requirements (TSGR) Common Requirements,* Issue 2, December 1998

2. BLOCK DIAGRAM

Figure 2-1. ZL81000 Block Diagram



See Figure 6-2 on page 26 for a detailed view of the BITS Receiver and BITS Transmitter blocks.

3. DETAILED DESCRIPTION

Figure 2-1 illustrates the blocks described in this section and how they relate to one another. Section 4 provides a detailed feature list.

The ZL81000 can directly receive up to two 64kHz composite clock signals on its IC1A and IC2A pins and up to two DS1, E1, 2048kHz, or 6312kHz synchronization signals using its BITS receivers. These signals typically come from a nearby BITS Timing Signal Generator or SSU to provide external timing to the system. The BITS receivers are full-featured LIU receivers and framers capable of recovering clock and data from both short-haul and long-haul signals, finding DS1/E1 frame, extracting incoming SSM messages, and reporting both SSMs and performance defects (LOS, OOF, AIS, RAI) to system software. The analog front-ends of the BITS receivers are state-of-the-art LIU receivers with software-selectable termination and high-impedance inputs to support redundant timing cards without relays in the signal path.

In addition to creating digital clock signals for use within the system, the ZL81000 can also directly transmit up to two DS1, E1, or 2048kHz synchronization signals using its BITS transmitters. These signals typically convey the recovered timing from one SONET/SDH port to a nearby BITS timing-signal generator or SSU which in turn distributes timing to the whole central office.The BITS transmitters are full-featured frame formatters and LIU

transmitters capable of generating DS1/E1 frames, inserting incoming SSM messages, and driving both short-haul and long-haul signals. The analog front-ends of the BITS transmitters are state-of-the-art LIU transmitters with software-selectable termination and high-impedance outputs to support redundant timing cards without relays in the signal path.

The entire chip is clocked from the external oscillator connected to the REFCLK pin. The 12.8MHz clock from the external oscillator is multiplied by 16 by the Master Clock Generator block to create the 204.8MHz master clock used by the rest of the device. Since every block on the device depends on the master clock and therefore the local oscillator clock for proper operation, the master clock generator has a watchdog timer (WDT) function that can be used to signal a local microprocessor in the event of a local oscillator clock failure.

4. DETAILED FEATURES

4.1 BITS Transceiver Features

4.1.1 General

- Two independent transceivers with fully independent transmitter and receiver
- DS1 synchronization interface in SF or ESF format
- E1 synchronization interface with FAS, CAS and/or CRC-4 framing
- J1 support (DS1 with Japanese CRC-6 and RAI)
- 2048 kHz synchronization interface (G.703)
- 6312 kHz Japanese synchronization interface (G.703 appendix II)
- Short-haul and long-haul line interface unit
- Internal software-selectable termination (75Ω, 100Ω, 110Ω, or 120Ω) or external termination
- High-impedance receive inputs and transmit outputs for no-relay redundancy
- Local and remote loopbacks

4.1.2 Receiver

- Automatic receive sensitivity adjustment
- DS1 receive sensitivity configurable for 0 to -36 dB (long-haul) or 0 to -15 dB (short-haul)
- E1 receive sensitivity configurable for 0 to -43dB (long-haul) or 0 to -12 dB (short-haul)
- Receive signal level indication in 2.5 dB steps from -2.5 dB to -34 dB (DS1) and -2.5 dB to -43 dB (E1)
- Monitor mode gain settings of 14 dB, 20 dB, 26 dB and 32 dB
- LOS, OOF, RAI and AIS status
- Extraction and validation of SSM messages from DS1 ESF data link or E1 Sa bits
- Receiver data output pin (RSER) for access to DS1/E1 payload
- Optional receiver frame sync output pins (ROUT) for special applications
- Receiver power-down control
- Short circuit detection

4.1.3 Transmitter

- Transmitter data input pin (TSER) for access to DS1/E1 payload
- Optional transmitter pins (TCLK, TOUT) for special applications
- Insertion of SSM messages into DS1 ESF data link or E1 Sa bits
- Flexible transmit waveform generation
- DSX-1 line build-outs
- E1 waveforms include G.703 waveshapes for both 75Ω coax and 120Ω twisted pair cables
- AIS and alternating ones and zeros generation
- Transmitter power-down control
- Short circuit detection/limit
- Open circuit detection

4.1.4 Jitter Attenuator

- Configurable buffer depth: 16, 32, 64 or 128 bits
- Can be inserted into the receiver path, the transmitter path, or disabled
- Available in DS1, E1 and 2048 kHz modes
- Buffer overflow and underflow status indication

4.2 Composite Clock Receiver Features

- Two composite clock receivers (AMI format), IC1A and IC2A
- Compliant with Telcordia GR-378 composite clock, G.703 centralized clock, and G.703 Appendix II.1) Japanese synchronization interfaces
- Configurable for 50% or 5/8 duty cycle, 1V or 3V pulse amplitude, and 110Ω/120Ω/133Ω termination
- Received signals are monitored for LOS, AMI violations, presence/absence of the 8 kHz component, and presence/absence of the 400 Hz component (for G.703 Appendix II.1 option b)
- Composite clock receiver inputs can be configured as programmable-frequency CMOS/TTL inputs if composite clock support is not needed
- Composite clock receivers followed by DPLL with 18, 35 or 70Hz bandwidth and frequency-multiplier APLL
- OC9 CMOS/TTL output clock can be configured for 1.544MHz or 2.048MHz

4.3 General Features

- Two general-purpose input clocks, IC3 and IC4
- Operates from a single external 12.800 MHz local oscillator (TCXO or OCXO)
- On-chip local oscillator watchdog circuit
- Microprocessor interface can be 8-bit parallel (Intel or Motorola, multiplexed or non-multiplexed) or SPI
- Register set can be write-protected

5. PIN DESCRIPTIONS

Table 5-1. Input Clock Pin Descriptions

PIN	NAME(1)	TYPE(2)	FUNCTION
H1	REFCLK	I	**Reference Clock.** Connect to a 12.800MHz, high-accuracy, high-stability, low-noise local oscillator (TCXO or OCXO). See Section 6.3.
P6	IC1A	I	**Input Clock 1 AMI.** AMI 64kHz composite clock. Enabled when MCR5:IC1SF = 0. See Section 6.10.1, Table 9-6, and Table 9-3.
P7	IC2A	I	**Input Clock 2 AMI.** AMI 64kHz composite clock. Enabled when MCR5:IC2SF = 0. See Section 6.10.1, Table 9-6, and Table 9-3.
C10	IC3	I_{PD}	**Input Clock 3.** CMOS/TTL. Programmable frequency (default 8kHz).
A11	IC4	I_{PD}	**Input Clock 4.** CMOS/TTL. Programmable frequency (default 8kHz).

Table 5-2. Output Clock Pin Descriptions

PIN	NAME(1)	TYPE(2)	FUNCTION
A9	OC9	O_3	**Output Clock 9.** CMOS/TTL. 1.544/2.048MHz.

Table 5-3. BITS Receiver Pin Descriptions

PIN	NAME[1]	TYPE[2]	PIN DESCRIPTION
F2	MCLK1	I_{PD}	**Master Clock for BITS Transceiver 1.** In most applications, the device's 204.8MHz master clock (see Section 6.3) is divided by 100 to get the BITS transceiver master clock. For special applications, BCCR3:MCLKS can be set to 1 to source the master clock for BITS transceiver 1 from the MCLK1 pin. The clock applied to MCLK1 can be 1X, 2X, 4X or 8X 2.048MHz for any BITS transceiver mode. For DS1 mode only, MCLK1 can be 1X, 2X, 4X, or 8X 1.544MHz. When BCCR3:MCLKS = 0, the MCLK1 pin is ignored and should be wired high or low. See Section 6.9.1.
T10	MCLK2	I_{PD}	**Master Clock for BITS Transceiver 2.** In most applications, the device's 204.8MHz master clock (see Section 6.3) is divided by 100 to get the BITS transceiver master clock. For special applications, BCCR3:MCLKS can be set to 1 to source the master clock for BITS transceiver 2 from the MCLK2 pin. The clock applied to MCLK2 can be 1X, 2X, 4X or 8X 2.048MHz for any BITS transceiver mode. For DS1 mode only, MCLK1 can be 1X, 2X, 4X or 8X 1.544MHz. When BCCR3:MCLKS = 0, the MCLK2 pin is ignored and should be wired high or low. See Section 6.9.1.
K1	RCLK1	O_3	**Receiver Clock Output for BITS Transceiver 1.** This pin presents the recovered clock from BITS receiver 1. This output is enabled/disabled by BCCR3:RCEN. When disabled, RCLK1 can function as a general-purpose output whose value is controlled by BCCR3:RCINV. See Section 6.9.2.
R10	RCLK2	O_3	**Receiver Clock Output for BITS Transceiver 2.** This pin presents the recovered clock from BITS receiver 2. This output is enabled/disabled by BCCR3:RCEN. When disabled, RCLK2 can function as a general-purpose output whose value is controlled by BCCR3:RCINV. See Section 6.9.2.
K2	ROUT1	O_3	**Receiver Multipurpose Output Pin for BITS Transceiver 1.** This output is enabled/disabled by BCCR3:ROEN. Its signal source is specified by BCCR3:ROUTS. Possible sources are the DS1/E1 frame sync and the DS1/E1 multiframe sync. When disabled, ROUT1 can function as a general-purpose output whose value is controlled by BCCR3:ROINV. See Section 6.9.2.
P10	ROUT2	O_3	**Receiver Multipurpose Output Pin for BITS Transceiver 2.** This output is enabled/disabled by BCCR3:ROEN. Its signal source is specified by BCCR3:ROUTS. Possible sources are the DS1/E1 frame sync and the DS1/E1 multiframe sync. When disabled, ROUT2 can function as a general-purpose output whose value is controlled by BCCR3:ROINV. See Section 6.9.2.
J3	RSER1	O_3	**Receiver Serial Data Output for BITS Transceiver 1.** When BITS receiver 1 is in DS1 or E1 mode (i.e., when BMCR:RMODE = 0x), this pin presents the received DS1/E1 data stream in NRZ format. RSER1 is updated on the RCLK1 edge specified by BCCR3:RCINV. RSER1 is enabled/disabled by the BCCR3:RSEN control bit. This pin is disabled (low) in other BITS receiver modes. See Sections 6.9.5.1 and 6.9.6.1.
T11	RSER2	O_3	**Receiver Serial Data Output for BITS Transceiver 2.** When BITS receiver 2 is in DS1 or E1 mode (i.e., when BMCR:RMODE = 0x), this pin presents the received DS1/E1 data stream in NRZ format. RSER2 is updated on the RCLK2 edge specified by BCCR3:RCINV. RSER2 is enabled/disabled by the BCCR3:RSEN control bit. This pin is disabled (low) in other BITS receiver modes. See Sections 6.9.5.1 and 6.9.6.1.
T5	RTIP1	I_A	**Differential Receiver Inputs for BITS Transceiver 1.** These pins connect to the receive cable through a 1:1 transformer. These pins are high impedance when the receiver is powered down (BLCR4:RPD = 1). See Section 6.9.4 for details.
R5	RRING1		
L16	RTIP2	I_A	**Differential Receiver Inputs for BITS Transceiver 2.** These pins connect to the receive cable through a 1:1 transformer. These pins are high impedance when the receiver is powered down (BLCR4:RPD = 1). See Section 6.9.4 for details.
L15	RRING2		

Table 5-4. BITS Transmitter Pin Descriptions

PIN	NAME[1]	TYPE[2]	FUNCTION
L2	TCLK1	O_3	**Transmit Clock Output for BITS Transceiver 1.** This pin presents the TCLK signal output from the Tx Clock Mux block. This output is enabled/disabled by BCCR4:TCEN. The TSER1 pin is sampled on the TCLK1 edge specified by BCCR4:TCINV. See Section 6.9.3.
T12	TCLK2	O_3	**Transmit Clock Output for BITS Transceiver 2.** This pin presents the TCLK signal output from the Tx Clock Mux block. This output is enabled/disabled by BCCR4:TCEN. The TSER2 pin is sampled on the TCLK2 edge specified by BCCR4:TCINV. See Section 6.9.3.
M1	TOUT1	O_3	**Transmit Multipurpose Output Pin for BITS Transceiver 1.** This output is enabled/disabled by BCCR4:TOEN. Its signal source is specified by BCCR4:TOUTS. Possible sources are the DS1/E1 frame sync and the DS1/E1 multiframe sync. See Section 6.9.3.
P11	TOUT2	O_3	**Transmit Multipurpose Output Pin for BITS Transceiver 2.** This output is enabled/disabled by BCCR4:TOEN. Its signal source is specified by BCCR4:TOUTS. Possible sources are the DS1/E1 frame sync and the DS1/E1 multiframe sync. See Section 6.9.3.
L1	TIN1	I_{PD}	**Transmitter Multipurpose Input for BITS Transceiver 1.** BCCR1:TCLKS can be set to 0000 to the enable the transmitter clock to be sourced from the TIN1 pin. Optionally TIN1 can source the frame or multiframe sync in DS1 and E1 modes. In these latter cases, TIN1 is sampled on the TCLK1 edge specified by BCCR4:TCINV. See Section 6.9.3.
R12	TIN2	I_{PD}	**Transmitter Multipurpose Input for BITS Transceiver 2.** BCCR1:TCLKS can be set to 0000 to the enable the transmitter clock to be sourced from the TIN2 pin. Optionally TIN2 can source the frame or multiframe sync in DS1 and E1 modes. In these latter cases, TIN2 is sampled on the TCLK2 edge specified by BCCR4:TCINV. See Section 6.9.3.
L3	TSER1	I_{PU}	**Transmitter Serial Data Input for BITS Transceiver 1.** When the BITS transmitter is in DS1 or E1 mode (i.e., when BMCR:TMODE = 0x), this pin is the source for the DS1/E1 data stream in NRZ format. TSER1 is sampled on the TCLK1 edge specified by BCCR4:TCINV. Payload bits and optionally some overhead bits are sampled. Normally, this pin is wired high to achieve an all-ones payload. This pin is ignored in other BITS transmitter modes and should be held high or low. See Sections 6.9.5.2 and 6.9.6.2.
T13	TSER2	I_{PU}	**Transmitter Serial Data Input for BITS Transceiver 2.** When the BITS transmitter is in DS1 or E1 mode (i.e., when BMCR:TMODE = 0x), this pin is the source for the DS1/E1 data stream in NRZ format. TSER2 is sampled on the TCLK2 edge specified by BCCR4:TCINV. Payload bits and optionally some overhead bits are sampled. Normally, this pin is wired high to achieve an all-ones payload. This pin is ignored in other BITS transmitter modes and should be held high or low. See Sections 6.9.5.2 and 6.9.6.2.
R3, T3	TTIP1	O_A	**Differential Transmitter Outputs for BITS Transceiver 1.** These pins drive the outgoing signal onto the transmit cable through a 1:2 step-up transformer. They can be placed in a high-impedance state by pulling the THZE1 pin high or setting BLCR4:TE = 0 in BITS transceiver 1. These pins are also high impedance when the transmitter is powered down (BLCR4:TPD = 1). The two TTIP1 pins should be externally wired together, and the two TRING1 pins should be externally wired together. See Section 6.9.4.
R2, T2	TRING1		
N15, N16	TTIP2	O_A	**Differential Transmitter Outputs for BITS Transceiver 2.** These pins drive the outgoing signal onto the transmit cable through a 1:2 step-up transformer. They can be placed in a high-impedance state by pulling the THZE2 pin high or setting BLCR4:TE = 0 in BITS transceiver 2. These pins are also high impedance when the transmitter is powered down (BLCR4:TPD = 1). The two TTIP2 pins should be externally wired together, and the two TRING2 pins should be externally wired together. See Section 6.9.4.
P15, P16	TRING2		
K3	THZE1	I_{PU}	**Transmit High-Impedance Enable for BITS Transceiver 1.** See Section 6.9.4.2.3. 0 = TTIP1/TRING1 transmit data normally (must also have BLCR4:TE = 1 in BITS transceiver 1) 1 = TTIP1/TRING1 high impedance
T14	THZE2	I_{PU}	**Transmit High-Impedance Enable for BITS Transceiver 2.** See Section 6.9.4.2.3. 0 = TTIP2/TRING2 transmit data normally (must also have BLCR4:TE = 1 in BITS transceiver 2) 1 = TTIP2/TRING2 high impedance

Table 5-5. Global Pin Descriptions

PIN	NAME[1]	TYPE[2]	FUNCTION
B6	$\overline{RST}$	I_{PU}	**Active-Low Reset.** When this global asynchronous reset is pulled low, all internal circuitry is reset to default values. The device is held in reset as long as $\overline{RST}$ is low. $\overline{RST}$ should be held low for at least two REFCLK cycles.
R14	$\overline{HIZ}$	I_{PU}	**Acitve-Low High-Impedance Enable Input.** The $\overline{JTRST}$ pin must be low to activate this function. 0 = Put all output pins in a high-impedance state 1 = Normal operation
N1	IFSEL0	I_{PD}	**Microprocessor Interface Select.** During reset, the value on these pins is latched into the IFSEL field of the IFCR register. See Section 6.11. 010 = Intel bus mode (multiplexed) 011 = Intel bus mode (nonmultiplexed) 100 = Motorola mode (nonmultiplexed) 101 = SPI mode (address and data transmitted LSB first) 110 = Motorola mode (multiplexed) 111 = SPI mode (address and data transmitted MSB first) 000, 001 = {unused value}
N2	IFSEL1		
P1	IFSEL2		
R11	MASTSLV	I_{PU}	**Master/Slave Select Input.** This pin should be wired to VDDIO.
T7	RESREF	I_A	**Resistor Reference.** This pin must be tied to V_{SS} through a 10kΩ ±1% resistor. The BITS transceivers use this reference resistor to tune internal termination impedance values. The resistor should be placed as close as possible to the device, and capacitance on the RESREF node must be < 10pF.
M3	SONSDH	I_{PD}	**SONET/SDH Frequency Select Input.** Sets the reset-default state of the SONSDH bit in MCR3 and the OC9SON bit in T4CR1. 0 = SDH rates (N x 2.048MHz) 1 = SONET rates (N x 1.544MHz)
C5	WDT	I_A	**Watchdog Timer.** Analog node for the REFCLK watchdog timer. Connect to a resistor (R) to V_{DDIO} and a capacitor (C) to ground. Suggested values are R = 20kΩ and C = 0.01µF. See Section 6.3.

Table 5-6. Parallel Interface Pin Descriptions

Note: *These pins are active in Intel and Motorola bus modes. See Section 6.11.1 for functional description and Section 9.4 for timing specifications.*

PIN	NAME[1]	TYPE[2]	FUNCTION
K14	ALE	I_{PD}	**Address Latch Enable.** This signal controls the address latch. In nonmultiplexed bus modes, the address is latched from A[8:0]. In these modes, ALE is typically wired high to make the latch transparent. In multiplexed bus modes, the address is latched from A[8] and AD[7:0].
J16	$\overline{CS}$	I_{PU}	**Active-Low Chip Select.** This pin must be asserted (low) to read or write internal registers.
J15	$\overline{WR}$/R/$\overline{W}$	I_{PU}	**Active-Low Write Enable or Read/Active-Low Write Select.** For Intel bus modes, $\overline{WR}$ is asserted to write internal registers. For Motorola bus modes, R/$\overline{W}$ = 1 indicates a read and R/$\overline{W}$ = 0 indicates a write.
J14	$\overline{RD}$/$\overline{DS}$	I_{PU}	**Active-Low Read Enable or Active-Low Data Strobe.** For the Intel-style interface modes, $\overline{RD}$ is asserted (low) to read internal registers. For the Motorola-style interface modes, the falling edge of $\overline{DS}$ enables data output on AD[7:0] during reads while the rising edge of $\overline{DS}$ latches data from AD[7:0] during writes.
E16	A[8]	I_{PD}	**Address Bus.** In nonmultiplexed bus modes, these inputs specify the address of the internal register to be accessed. In multiplexed bus modes, the address is specified on A[8] and AD[7:0], while A[7:0] are not used and should be wired high or low.
F15	A[7]		
G14	A[6]		
F16	A[5]		
G15	A[4]		
H14	A[3]		
G16	A[2]		
H15	A[1]		
H16	A[0]		
C14	AD[7]	I/O	**Address/Data Bus.** In both multiplexed and nonmultiplexed bus modes, these pins are an 8-bit data bus. In multiplexed bus modes, these pins also convey the lower 8 bits of the register address.
D14	AD[6]		
E14	AD[5]		
C15	AD[4]		
D15	AD[3]		
C16	AD[2]		
D16	AD[1]		
E15	AD[0]		
B15	$\overline{RDY}$	O	**Active-Low Ready/Data Acknowledge.** This pin is asserted when the device has completed a read or write operation.
A15	INTREQ	O	**Interrupt Request.** The behavior of this pin is configured in the INTCR register. Polarity can be active high or active low. Drive action can be push-pull or open drain. The pin can also be configured as a general-purpose output if the interrupt request function is not needed.

Table 5-7. SPI Bus Mode Pin Descriptions

Note: *These pins are active in SPI interface modes. See Section 6.11.2 for functional description and Section 9.5 for timing specifications.*

PIN	NAME(1)	TYPE(2)	FUNCTION
J16	$\overline{CS}$	I_{PU}	**Active-Low Chip Select.** This pin must be asserted to read or write internal registers.
C16	SCLK	I	**Serial Clock.** SCLK is always driven by the SPI bus master.
D16	SDI	I	**Serial Data Input.** The SPI bus master transmits data to the device on this pin.
E15	SDO	O	**Serial Data Output.** The device transmits data to the SPI bus master on this pin.
D14	CPHA	I	**Clock Phase.** See Figure 6-13. 0 = data is latched on the leading edge of the SCLK pulse 1 = data is latched on the trailing edge of the SCLK pulse
C14	CPOL	I	**Clock Polarity.** See Figure 6-13. 0 = SCLK is normally low and pulses high during bus transactions 1 = SCLK is normally high and pulses low during bus transactions
A15	INTREQ	O	**Interrupt Request.** The behavior of this pin is configured in the INTCR register. Polarity can be active high or active low. Drive action can be push-pull or open drain. The pin can also be configured as a general-purpose output if the interrupt request function is not needed.

Table 5-8. JTAG Interface Pin Descriptions

Note: *See Section 8 for functional description and Section 9.6 for timing specifications.*

PIN	NAME(1)	TYPE(2)	FUNCTION
T8	$\overline{JTRST}$	I_{PU}	**Active-Low JTAG Test Reset.** Asynchronously resets the test access port (TAP) controller. $\overline{JTRST}$ should be held low during device power-up. If not used, $\overline{JTRST}$ can be held low or high after power-up.
R8	JTCLK	I	**JTAG Clock.** Shifts data into JTDI on the rising edge and out of JTDO on the falling edge. If not used, JTCLK can be held low or high.
R9	JTDI	I_{PU}	**JTAG Test Data Input.** Test instructions and data are clocked in on this pin on the rising edge of JTCLK. If not used, JTDI can be held low or high.
P9	JTDO	O	**JTAG Test Data Output.** Test instructions and data are clocked out on this pin on the falling edge of JTCLK. If not used, leave floating.
T9	JTMS	I_{PU}	**JTAG Test Mode Select.** Sampled on the rising edge of JTCLK and is used to place the port into the various defined IEEE 1149.1 states. If not used, connect to V_{DDIO} or leave floating.

Table 5-9. General-Purpose I/O Pin Descriptions

PIN	NAME(1)	TYPE(2)	FUNCTION
E2	GPIO1	I/O	**General-Purpose I/O Pin 1.** GPCR:GPIO1D configures this pin as an input or an output. GPCR:GPIO1O specifies the output value. GPSR:GPIO1 indicates the state of the pin.
F3	GPIO2	I/O	**General-Purpose I/O Pin 2.** GPCR:GPIO2D configures this pin as an input or an output. GPCR:GPIO2O specifies the output value. GPSR:GPIO2 indicates the state of the pin.
H2	GPIO3	I/O	**General-Purpose I/O Pin 3.** GPCR:GPIO3D configures this pin as an input or an output. GPCR:GPIO3O specifies the output value. GPSR:GPIO3 indicates the state of the pin.
J1	GPIO4	I/O	**General-Purpose I/O Pin 4.** GPCR:GPIO4D configures this pin as an input or an output. GPCR:GPIO4O specifies the output value. GPSR:GPIO4 indicates the state of the pin.

Table 5-10. Power-Supply Pin Descriptions

PIN	NAME[1]	TYPE[2]	FUNCTION
D6, D8, D9, D11, E6, E11, F4, F5, F12, F13, H4, H13, J4, J13, L4, L5, L12, L13, M6, M11, N6, N8, N9, N11	V_{DD}	P	**Core Power Supply.** 1.8V ±10%
B1, B16, D7, D10, E7–E10, G4, G5, G12, G13, H5, H12, J5, J12, K4, K5, K12, K13, M7, M8, M9, M10, N7, N10, R1, R16	V_{DDIO}	P	**I/O Power Supply.** 3.3V ±10%
A1, A16, D4, D5, D12, D13, E4, E5, E12, E13, F6–F11, G6–G11, H6–H11, J6–J11, K6–K11, L6–L11, M4, M5, M12, M13, N4, N5, N12, N13, T1, T16	V_{SS}	P	**Ground Reference**
A6	VDD_ICDIFF	P	**Power Supply.** 3.3V ±10%
C4	VSS_ICDIFF	P	**Return for VDD_ICDIFF.**
B2	VDD_OC6	P	**Power Supply.** 1.8V ±10%
A2	VSS_OC6	P	**Return for VDD_OC6.**
C3	VDD_OC7	P	**Power Supply.** 1.8V ±10%
D3	VSS_OC7	P	**Return for VDD_OC7.**
T4	RVDD_P1	P	**Power Supply for BITS Receiver 1.** 3.3V ±10%
P5	RVSS_P1	P	**Return for BITS Receiver 1**
M15	RVDD_P2	P	**Power Supply for BITS Receiver 2.** 3.3V ±10%
M14	RVSS_P2	P	**Return for BITS Receiver 2**
R4	TVDD_P1	P	**Power Supply for BITS Transmitter 1.** 3.3V ±10%
P4	TVSS_P1	P	**Return for BITS Transmitter 1**
M16	TVDD_P2	P	**Power Supply for BITS Transmitter 2.** 3.3V ±10%
N14	TVSS_P2	P	**Return for BITS Transmitter 2**
D1	AVDD_PLL1	P	**Power Supply.** 1.8V ±10%
D2	AVSS_PLL1	P	**Return for AVDD_PLL1**
E1	AVDD_PLL2	P	**Power Supply for APLL.** 1.8V ±10%
E3	AVSS_PLL2	P	**Return for AVDD_PLL2**
F1	AVDD_PLL3	P	**Power Supply.** 1.8V ±10%
G2	AVSS_PLL3	P	**Return for AVDD_PLL3.**
G1	AVDD_PLL4	P	**Power Supply for Master Clock Generator APLL.** 1.8V ±10%

PIN	NAME(1)	TYPE(2)	FUNCTION
G3	AVSS_PLL4	P	**Return for Master Clock Generator APLL**
H3	DV_{DD}	P	**Power Supply for BITS Transceiver LIU Digital Logic.** 3.3V ±10%
P8	DV_{SS}	P	**Return for BITS Transceiver LIU Digital Logic**
R13	TM1	—	**Connect to V_{SS}**
T15	TM2		
A3, A4, A5, A7, A8, A10, A12, A13, A14, B3, B4, B5, B7, B8, B9, B10, B11, B12, B13, B14, C1, C2, C6, C7, C8, C9, C11, C12, C13, F14, M2, P12	N.C.	—	**NoConnection**
R6	TST_RA1		
T6	TST_RB1		
R7	TST_RC1		
L14	TST_RA2		
K16	TST_RB2		
K15	TST_RC2		
P2	TST_TA1		
N3	TST_TB1		
P3	TST_TC1		
R15	TST_TA2		
P13	TST_TB2		
P14	TST_TC2		

Note 1: All pin names with an overbar (e.g., $\overline{CS}$) are active low.

Note 2: All pins, except power and analog pins, are CMOS/TTL, unless otherwise specified in the pin description.

I = input pin

I_A = analog input pin

I_{PD} = input pin with internal 50kΩ pulldown

I_{PU} = input pin with internal 50kΩ pullup to approx.2.2V

I/O = input/output pin

O = output pin

O_A = analog output pin (can be placed in a high-impedance state)

O_3 = output pin that can tri-stated (i.e., placed in a high-impedance state)

P = power-supply pin

Note 3: All digital pins are I/O pins in JTAG mode.

Note 4: When ramping power supplies up or down, the voltage on any 1.8V power supply pin must not exceed the voltage on any 3.3V power-supply pin.

6. FUNCTIONAL DESCRIPTION

6.1 Overview

The ZL81000 has two multiprotocol BITS/SSU receivers, and two multiprotocol BITS/SSU transmitters plus four input clocks, IC1A, IC2, IC3 and IC4.

The two BITS receivers can receive several synchronization signals including DS1, E1, 2048kHz, and 6312kHz. In DS1 and E1 modes, a built-in framer finds frame sync and extracts the incoming SSM message for inspection by system software.

The two BITS transmitters can transmit DS1, E1, and 2048kHz synchronization signals. In DS1 and E1 modes, a built-in frame formatter frames the signal and inserts the outgoing SSM message.

The IC1A and IC2A input clocks are 64kHz composite clock receivers, and the IC3 and IC4 inputs are CMOS/TTL (5V tolerant). The IC3 and IC4 CMOS/TTL inputs can accept signals from 2kHz to 125MHz.

Each input clock can be monitored continually for activity and/or frequency. Frequency can be compared to both a hard limit and a soft limit. Inputs outside the hard limit are declared invalid, while inputs inside the hard limit but outside the soft limit are merely flagged. Each input can be marked unavailable or given a priority number. Except in special modes, the highest priority valid input is automatically selected as the reference for the DPLL.

The DPLL can directly lock to many common telecom frequencies, including, but not limited to 8kHz, DS1, E1, 19.44MHz, and 38.88MHz. The DPLLs can also lock to any multiple of 8kHz up to 125MHz.

The DPLL has these features:

- Automatic reference selection based on input quality and priority
- Optional manual reference selection/forcing
- Configurable quality thresholds for each input
- Adjustable PLL characteristics, including bandwidth, pull-in range, and damping factor
- Ability to lock to several common telecom frequencies plus multiples of 8kHz up to 125MHz
- Frequency conversion between input and output using digital frequency synthesis
- Combined performance of a stable, consistent digital PLL and a low-jitter analog output PLL

The output of the DPLL is connected to a high-speed APLL that multiplies the DPLL clock rate and filters DPLL output jitter. The output of the APLL is the OC9 pin, which is configurable for1544kHz or 2048kHz.

6.2 Device Identification and Protection

The 16-bit read-only ID field in the ID1 and ID2 registers is set to 8C1Ch. The device revision can be read from the REV register. Contact the factory to interpret this value and determine the latest revision. The register set can be protected from inadvertent writes using the PROT register.

6.3 Local Oscillator and Master Clock Configuration

The device operates from a 204.8MHz master clock. The master clock is synthesized from a 12.800MHz clock originating from a local oscillator attached to the REFCLK pin.

The ZL81000 implements a stand-alone watchdog circuit that causes an interrupt on the INTREQ pin when the local oscillator attached to the REFCLK pin is significantly off frequency. The watchdog interrupt is not maskable, but *is* subject to the INTCR register settings. When the watchdog circuit activates, reads of any and all registers in the device will return 00h to indicate the failure. In response to the activation of the INTREQ pin or during periodic polling, if system software ever reads 00h from the ID registers (which are hard-coded to 8C1C) then it can conclude that the local oscillator attached to that ZL81000 has failed. For proper operation of the watchdog timer, connect the WDT pin to a resistor (R) to V_{DDIO} and a capacitor (C) to ground. Suggested values are R = 20kΩ and C = 0.01µF.

6.4 Input Clock Configuration

The ZL81000 four input clocks: IC1A, IC2A, IC3 and IC4. Table 6-1 provides summary information about each clock, including signal format and available frequencies. The device tolerates a wide range of duty cycles on the IC3 and IC4 input clocks, out to a minimum high time or minimum low time of 3ns or 30% of the clock period, which ever is smaller.

6.4.1 Signal Format Configuration

IC3 and IC4 accept both TTL and 3.3V CMOS levels. One key configuration bit that affects the available frequencies is the SONSDH bit in MCR3. When SONSDH = 1 (SONET mode), the 1.544MHz frequency is available. When SONSDH = 0 (SDH mode), the 2.048MHz frequency is available. During reset, the default value of this bit is latched from the SONSDH pin.

Input clocks IC1A and IC2A are 64kHz composite clock receivers (see Section 6.10). The composite clock signal is a 64kHz AMI clock with an embedded 8kHz clock indicated by deliberate bipolar violations (BPVs) every 8 clock cycles. The 8kHz component is the clock that is forwarded to the DPLLs. The AMI composite clock electrical specifications are shown in Table 9-6, and the recommended external components are shown in Table 9-3.

Table 6-1. Input Clock Capabilities

INPUT CLOCK	SIGNAL FORMATS	FREQUENCIES	DEFAULT FREQUENCY
IC1A	AMI	64kHz composite clock	8kHz
IC2A	AMI	64kHz composite clock	8kHz
IC3	CMOS/TTL	Up to 125MHz(1)	8kHz
IC4	CMOS/TTL	Up to 125MHz	8kHz

Note 1: Available frequencies for IC3 and IC4 CMOS/TTL input clocks are 2kHz, 4kHz, 8kHz, 1.544MHz (SONET mode), 2.048MHz (SDH mode), 6.312MHz, 6.48MHz, 19.44MHz, 25.92MHz, 38.88MHz, 51.84MHz, 77.76MHz, and N x 8kHz for $2 \leq N \leq 15{,}625$.

6.4.2 Frequency Configuration

Input clock frequencies for IC3 and IC4 are configured in the FREQ field of the ICR registers. The DIVN and LOCK8K bits of these same registers specify the locking frequency mode, as shown in Table 6-2.

Table 6-2. Locking Frequency Modes

DIVN	LOCK8K	LOCKING FREQUENCY MODE
0	0	Direct lock mode
0	1	LOCK8K mode
1	X	DIVN mode

6.4.2.1 Direct Lock Mode

In direct lock mode, the DPLL locks to the selected reference at the frequency specified in the corresponding ICR register. When the DPLL is configured for 77.76MHz operation direct lock mode can only be used for input clocks

with these specific frequencies: 2kHz, 4kHz, 8kHz, 1.544MHz, 2.048MHz, 6.312MHz, 6.48MHz, 19.44MHz, 25.92MHz, 38.88MHz, 51.84MHz and 77.76MHz. When configured for *non*-77.76MHz operation, the DPLL can direct-lock to any of the specific frequencies listed above from 2kHz to 6.48MHz, but for the specific frequencies of 19.44MHz and higher, the input must be configured for LOCK8K or DIVN mode.

MTIE may be somewhat lower in direct lock mode because the higher frequencies allow more frequent phase updates.

6.4.2.2 LOCK8K Mode

In LOCK8K mode, an internal divider is configured to divide the selected reference down to 8kHz. The DPLL locks to the 8kHz output of the divider. LOCK8K mode can only be used for input clocks with these frequencies: 8kHz, 1.544MHz, 2.048MHz, 6.312MHz, 6.48MHz, 19.44MHz, 25.92MHz, 38.88MHz, 51.84MHz, and 77.76MHz. LOCK8K mode is enabled for a particular input clock by setting the LOCK8K bit in the corresponding ICR register. LOCK8K mode gives a greater tolerance to input jitter because it uses lower frequencies for phase comparisons. The clock edge to lock to on the selected reference can be configured using the 8KPOL bit in the TEST1 register. For 2kHz and 4kHz clocks, the LOCK8K bit is ignored and direct-lock mode is used.

6.4.2.3 DIVN Mode

In DIVN mode, the internal divider is configured from the value stored in the DIVN registers. The DIVN value must be chosen so that when the selected reference is divided by DIVN+1 the output clock is 8kHz. The DPLL locks to the 8kHz output of the divider. DIVN mode can only be used for input clocks whose frequency is an integer multiple of 8 kHz and less than or equal to 125MHz. The DIVN register field can range from 1 to 15,624 inclusive. The same DIVN+1 factor is used for all input clocks configured for DIVN mode. When DIVN = 1 in an ICR register, the FREQ field of that register is ignored.

6.5 Input Clock Quality Monitoring

Each input clock is continuously monitored for frequency accuracy and activity. Frequency monitoring is described in Section 6.5.1, while activity monitoring is described in Sections 6.5.2 and 6.5.3. Any input clock that has a frequency out-of-band alarm or activity alarm is automatically declared invalid. The valid/invalid state of each input clock is reported in the corresponding real-time status bit in register VALSR1. When the valid/invalid state of a clock changes, the corresponding latched status bit is set in register MSR1, and an interrupt request occurs if the corresponding interrupt enable bit is set in registers IER1. Input clocks marked invalid cannot be selected as the reference for the DPLL. If the DPLL does not have any valid input clocks available, the T4NOIN status bit is set to 1 in MSR3.

6.5.1 Frequency Monitoring

The ZL81000 monitors the frequency of each input clock and invalidates any clock whose frequency is outside of specified limits. Two frequency limits can be specified: a soft limit and a hard limit.These limits are specified in the ILIMIT register. When the frequency of an input clock is greater than or equal to the soft limit, the corresponding SOFT alarm bit is set to 1 in the ISR registers. The soft limit is only for monitoring; triggering it does not invalidate the clock. When the frequency of an input clock is greater than or equal to the hard limit, the corresponding HARD alarm bit is set to 1 in the ISR registers, and the clock is marked invalid in the VALSR registers. Monitoring according to the hard and soft limits is enabled/disabled using the HARDEN and SOFTEN bits in the MCR10 register. The ILIMIT register has a default soft limit of ±11.43ppm and a default hard limit of ±15.24ppm. Limits can be set from ±3.81ppm to ±60.96ppm in 3.81ppm steps. Both the SOFT and HARD alarm limits have hysteresis as required by GR-1244. Frequency monitoring is only done on an input clock when the clock does not have an activity alarm.

Frequency measurement is done with respect to the internal 204.8MHz master clock. Measured frequency can be read from any frequency monitor by specifying the input clock in the FMEASIN field of MCR11 and reading the frequency from the FMEAS register.

6.5.2 Activity Monitoring

Each input clock is monitored for activity and proper behavior using a leaky bucket accumulator. A leaky bucket accumulator is similar to an analog integrator: the output amplitude increases in the presence of input events and gradually decays in the absence of events. When events occur infrequently, the accumulator value decays fully

between events and no alarm is declared. When events occur close enough together, the accumulator increments faster than it can decay and eventually reaches the alarm threshold. After an alarm has been declared, if events occur infrequently enough, the accumulator can decay faster than it is incremented and eventually reaches the alarm clear threshold.

The leaky bucket accumulator for each input clock can be assigned one of four configurations (0 through 3) in the BUCKET field of the ICR registers. Each leaky bucket configuration has programmable size, alarm declare threshold, alarm clear threshold, and decay rate, all of which are specified in the LBxy registers at addresses 50h through 5Fh.

Activity monitoring is divided into 128ms intervals. The accumulator is incremented once for each 128ms interval in which the input clock is inactive for more than two cycles. Thus the “fill” rate of the bucket is at most 1 unit per 128ms, or approximately 8 units/second. During each period of 1, 2, 4 or 8 intervals (programmable), the accumulator decrements if no irregularities occur. Thus the “leak” rate of the bucket is approximately 8, 4, 2, or 1 units/second. A leak is prevented when a fill event occurs in the same interval.

When the value of an accumulator reaches the alarm threshold (LBxU register), the corresponding ACT alarm bit is set to 1 in the ISR registers, and the clock is marked invalid in the VALSR registers. When the value of an accumulator reaches the alarm clear threshold (LBxL register), the activity alarm is cleared by clearing the clock’s ACT bit. The accumulator cannot increment past the size of the bucket specified in the LBxS register. The decay rate of the accumulator is specified in the LBxD register. The values stored in the leaky bucket configuration registers must have the following relationship at all times: LBxS ≥ LBxU > LBxL.

When the leaky bucket is empty, the minimum time to declare an activity alarm in seconds is LBxU / 8 (where the “x” in “LbxU” is the leaky bucket configuration number, 0 to 3). The minimum time to clear an activity alarm in seconds is [2^{LBxD} x (LBxS - LBxL) / 8]. For example, assume LBxU = 8, LBxL = 1, LBxS = 10, and LBxD = 0. The minimum time to declare an activity alarm would be 8 / 8 = 1 second. The minimum time to clear the activity alarm would be [2^0 x (10 - 1) / 8 = 1.125 seconds].

For input clocks IC1A and IC2A, if MCR5:BITERR = 1, then the accumulator is also incremented whenever a violation of the one-BPV-in-eight pattern is detected.

6.5.3 Selected Reference Activity Monitoring

The input clock that the DPLL is currently locked to is called the selected reference. The quality of the DPLL’s selected reference is exceedingly important, since missing cycles and other anomalies on the selected reference can cause unwanted jitter, wander or frequency offset on the output clock. When anomalies occur on the selected reference they must be detected as soon as possible to give the DPLL opportunity to temporarily disconnect from the reference until the reference is available again. By design, the regular input clock activity monitor (Section 6.5.2) is too slow to be suitable for monitoring the selected reference. Instead, the DPLL has its own fast activity monitor that detects inactivity within approximately two missing reference clock cycles.

When the DPLL detects a no-activity event, it immediately enters mini-holdover mode to isolate itself from the selected reference. When PHLIM1:NALOL = 0 (default), the DPLL does not declare loss-of-lock during no-activity events. If the selected reference becomes available again before any alarms are declared by the activity monitor or frequency monitor, then the DPLL continues to track the selected reference using nearest-edge locking (±180°) to avoid cycle slips. When NALOL = 1, the DPLL clears the OPSTATE:T4LOCK status bit, which sets MSR3:T4LOCK and causes an interrupt request if enabled.. If the selected reference becomes available again before any alarms are declared by the activity monitor or frequency monitor, then the DPLL tracks the selected reference until phase lock is reestablished.

6.5.4 Composite Clock Inputs

Input clocks IC1A and IC2A are also monitored for various defects (AMI error, LOS, etc.) See Section 6.10.1 for further details.

6.6 Input Clock Priority, Selection, and Switching

6.6.1 Priority Configuration

During normal operation, the selected reference for the DPLL is chosen automatically based on the priority rankings assigned to the input clocks in the input priority registers (IPR1 to IPR2). Each of these registers has priority fields for two input clocks. The default input clock priorities are shown in Table 6-3.

Any unused input clock should be given the priority value 0, which disables the clock and marks it as unavailable for selection. Priority 1 is highest while priority 15 is lowest. The same priority can be given to two or more clocks.

Table 6-3. Default Input Clock Priorities

INPUT CLOCK	DEFAULT PRIORITY
IC1	2
IC2	3
IC3	4
IC4	5

6.6.2 Automatic Selection Algorithm

The real-time valid/invalid state of each input clock is maintained in the VALSR1 register. The selected reference can be marked invalid for phase, frequency or activity. Other input clocks can be invalidated for frequency or activity.

The reference selection algorithm for the DPLL chooses the highest-priority valid input clock to be the selected reference. To select the proper input clock based on these criteria, the selection algorithm maintains a priority table of valid inputs. The top three entries in this table and the selected reference are displayed in the PTAB1 and PTAB2 registers.

If two or more input clocks are given the same priority number then those inputs are prioritized among themselves using a fixed circular list. If one equal-priority clock is the selected reference but becomes invalid then the next equal-priority clock in the list becomes the selected reference. If an equal-priority clock that is not the selected reference becomes invalid, it is simply skipped over in the circular list. The selection among equal-priority inputs is inherently nonrevertive in the case where multiple equal-priority inputs have the highest priority. Otherwise the switching behavior of the DPLL is revertive. In revertive mode switching, if an input clock with a higher priority than the selected reference becomes valid, the higher-priority reference immediately becomes the selected reference.

In most systems redundant timing cards are required, with one functioning as the master and the other as the slave. In such systems the priority tables of the master and slave must match. The ZL81000's register set makes it easy for the slave's priority table to track the master's table. At system start-up, the same priorities must be assigned to the input clocks in the master and slave devices. During operation, if an input clock becomes valid or invalid in one device (master or slave), the change is flagged in that device's MSR1 register, which can drive an interrupt request on the INTREQ pin if needed. The real-time valid/invalid state of the input clocks can then be read from that device's VALSR1 register. Once the nature of the state change is understood, the control bits of the other device's VALCR1 register can be manipulated to mark clocks invalid in the other device as well.

6.7 DPLL Architecture and Configuration

The DPLL has an analog PLL (APLL) at the output stage. This architecture combines the benefits of both PLL types.

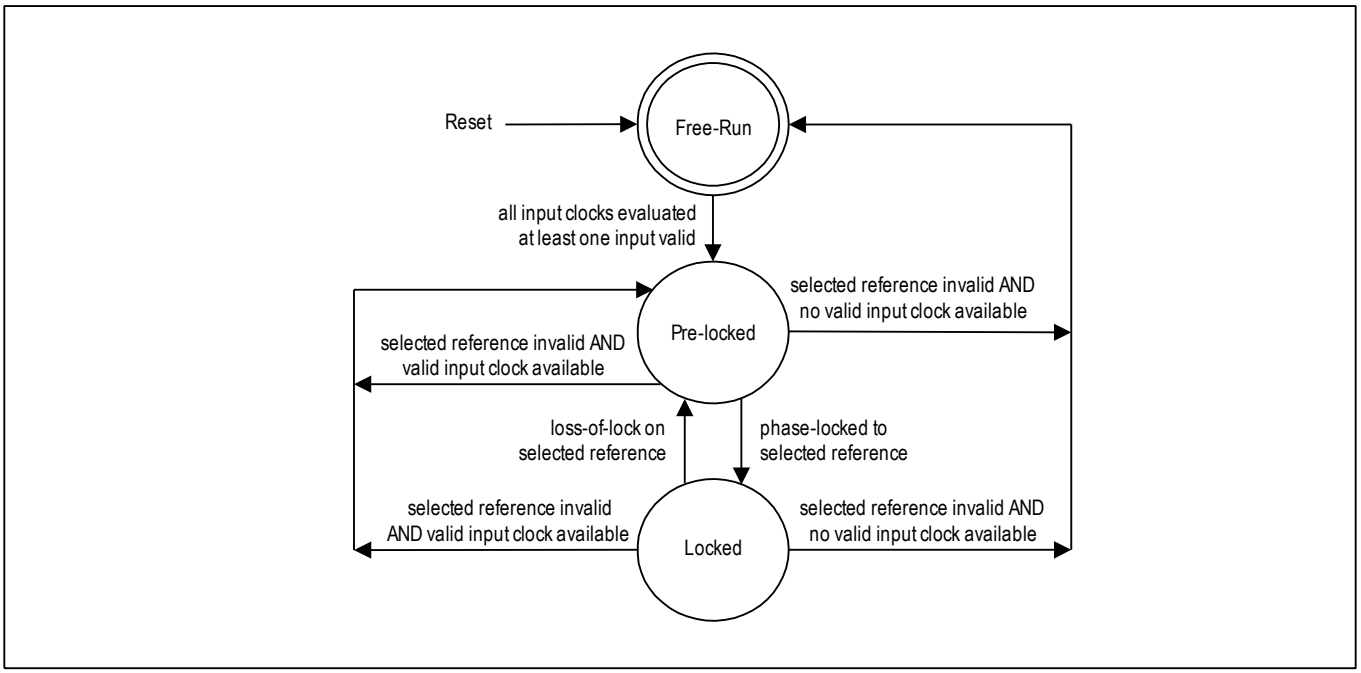
Digital PLLs have two key benefits: (1) stable, repeatable performance that is insensitive to process variations, temperature and voltage, and (2) flexible behavior that is easily programmed via configuration registers. DPLLs use digital frequency synthesis (DFS) to generate various clocks. In DFS, a high-speed master clock (204.8MHz) is multiplied up from the 12.800MHz local oscillator clock applied to the REFCLK pin. This master clock is then digitally divided down to the desired output frequency. Since the resolution of the DFS process is one master clock cycle or 4.88ns, the DFS output clock has jitter of up to 1 master clock UI (4.88ns) pk-pk.

The analog PLL filtesr the jitter from the DPLL, reducing the 4.88ns pk-pk jitter to 0.5ns pk-pk and 60ps RMS, typical, measured broadband (10Hz to 1GHz).

6.7.1 DPLL State Machine

The DPLL has a simple state machine, as shown in Figure 6-1.

Figure 6-1. DPLL State Transition Diagram



6.7.2 Bandwidth

The bandwidth of the DPLL is configured in the T4BW register to be 18Hz, 35Hz, or 70Hz. This bandwidth value is used for both acquisition and locked mode.

6.7.3 Damping Factor

The damping factor for the DPLL is configured in the DAMP field of the T4CR2 register. The reset default damping factors for DPLL is chosen to give a maximum wander gain peak of approximately 0.1dB. Available settings are a function of DPLL bandwidth (configured in the T4BW register). See Table 6-4.

Table 6-4. Damping Factors and Peak Jitter/Wander Gain

BANDWIDTH	DAMP[2:0] VALUE	DAMPING FACTOR	GAIN PEAK (dB)
0.5mHz to 4Hz	1, 2, 3, 4, 5	5	0.1
8Hz	1	2.5	0.2
	2, 3, 4, 5	5	0.1
18 Hz	1	1.2	0.4
	2	2.5	0.2
	3, 4, 5	5	0.1
35 Hz	1	1.2	0.4
	2	2.5	0.2
	3	5	0.1
	4, 5	10	0.06
70 Hz	1	1.2	0.4
	2	2.5	0.2
	3	5	0.1
	4	10	0.06
	5	20	0.03

6.7.4 Phase Detectors

Phase detectors are used to compare a PLL's feedback clock with its input clock. Two phase detectors are available in the DPLL:

- Phase/frequency detector (PFD)
- Multicycle phase detector (MCPD) for large input jitter tolerance

These detectors can be used in combination to give fine phase resolution combined with large jitter tolerance. As with the rest of the DPLL logic, the phase detectors operate at input frequencies up to 77.76MHz. The multicycle phase detector detects and remembers phase differences of many cycles (up to 8191UI).

The phase detectors can be configured for normal phase/frequency locking (±360° capture) or nearest-edge phase locking (±180° capture). With nearest-edge detection the phase detectors are immune to occasional missing clock cycles. The DPLL automatically switches to nearest-edge locking when the multi-cycle phase detector is disabled and the other phase detectors determine that phase lock has been achieved. Setting D180 = 1 in the TEST1 register disables nearest-edge locking and forces the DPLL to use phase/frequency locking.

The multicycle phase detector is enabled by setting MCPDEN=1 in the PHLIM2 register. The range of the MCPD—from ±1UI up to ±8191UI—is configured in the COARSELIM field of PHLIM2. The MCPD tracks phase position over many clock cycles, giving high jitter tolerance. Thus the use of the MCPD is an alternative to the use of LOCK8K mode for jitter tolerance.

When USEMCPD = 1 in PHLIM2, the MCPD is used in the DPLL loop, giving faster pull-in but more overshoot. In this mode the loop has similar behavior to LOCK8K mode. In both cases large phase differences contribute to the dynamics of the loop. When enabled by MCPDEN = 1, the MCPD tracks the phase position whether or not it is used in the DPLL loop.

6.7.5 Loss of Phase Lock Detection

Loss of phase lock is triggered by any of the following:

- The fine phase lock detector (measures phase between input and feedback clocks)
- The coarse phase lock detector (measures whole cycle slips)
- Hard frequency limit detector
- Inactivity detector

The fine phase lock detector is enabled by setting FLEN = 1 in the PHLIM1 register. The fine phase limit is configured in the FINELIM field of PHLIM1.

The coarse phase lock detector is enabled by setting CLEN = 1 in the PHLIM2 register. The coarse phase limit is configured in the COARSELIM field of PHLIM2. This coarse phase lock detector is part of the multi-cycle phase detector (MCPD) described in Section 6.7.4. the COARSELIM fields sets both the MCPD range and the coarse phase limit, since the two are equivalent. If loss of phase lock should not be declared for multiple-UI input jitter then the fine phase lock detector should be disabled and the coarse phase lock detector should be used instead.

The hard frequency limit detector is enabled by setting FLLOL = 1 in the DLIMIT3 register. The DPLL hard limit is fixed at ±80ppm. When the DPLL frequency reaches the hard limit, loss-of-lock is declared. The DLIMIT3 register also has the SOFTLIM field to specify a soft frequency limit. Exceeding the soft frequency limit does not cause loss-of-lock to be declared. When the DPLL frequency exceeds the soft limit the T4SOFT status bit is set in OPSTATE. Both the SOFT and HARD alarm limits have hysteresis as required by GR-1244.

The inactivity detector is enabled by setting NALOL = 1 in the PHLIM1 register. When this detector is enabled the DPLL declares loss-of-lock after one or two missing clock cycles on the selected reference. See Section 6.5.3.

When the DPLL declares loss of phase lock, the T4LOCK bit is cleared in the OPSTATE register, which sets the T4LOCK bit in the MSR3 register and requests an interrupt if enabled.

6.7.6 Frequency and Phase Measurement

Standard input clock frequency monitoring is described in Section 6.5.1. The input clock monitors report measured frequency with 3.8ppm resolution. More accurate measurement of frequency and phase can be accomplished using the DPLL.

DPLL frequency measurements can be read from the FREQ field spanning registers FREQ1, FREQ2 and FREQ3. This field indicates the frequency of the selected reference for the DPLL, This frequency measurement has a resolution of 0.0003068ppm over a ±80ppm range. The value read from the FREQ field is the DPLL's integral path value, which is an averaged measurement with an averaging time inversely proportional to DPLL bandwidth.

DPLL phase measurements can be read from the PHASE field spanning registers PHASE1 and PHASE2. This field indicates the phase difference seen by the phase detector. This phase measurement has a resolution of approximately 0.7 degrees and is internally averaged with a -3dB attenuation point of approximately 100Hz. Thus, for low DPLL bandwidths the PHASE field gives input phase wander in the frequency band from the DPLL corner frequency up to 100Hz. This information could be used by software to compute a crude MTIE measurement up to an observation time of approximately 1000 seconds.

6.8 Output Clock Configuration

The OC9 output clock signal is always CMOS/TTL signal format.

OC9 is always a DS1 or E1 clock. OC9 is enabled by setting OC9EN = 1 in the OCR4 register, and it is configured for DS1 or E1 with the OC9SON bit in T4CR1. OC9 must synthesized, rather than directly divided down, from the source DFS block's input clock. The jitter on OC9 is therefore a function of the jitter on the input clock and the jitter generated during synthesis. OC9 jitter can range from 11ns to 20ns.

6.9 Multiprotocol BITS Transceivers

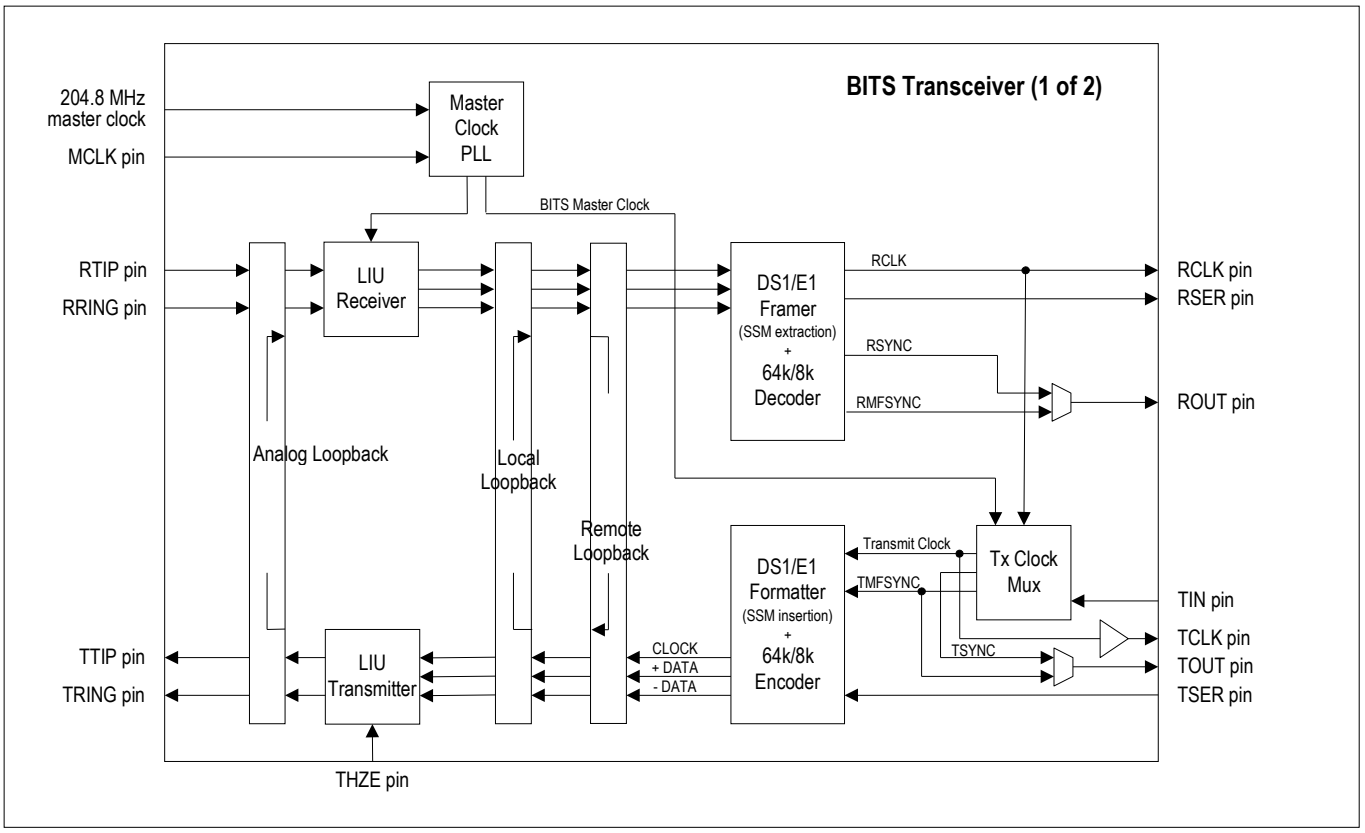
The ZL81000 has two identical, independent BITS transceivers, each of which support the following synchronization protocols:

- DS1 (also configurable for J1)
- E1
- 2048kHz (G.703)
- 6312kHz (G.703)*

*The BITS receivers can receive the 6312kHz signal, but the transmitters do not transmit this protocol.

The BMCR register description and accompanying footnotes give additional details on these synchronization protocols and the telecom standards with which they comply. Figure 6-2 shows the BITS transceiver block diagram.

Figure 6-2. BITS Transceiver Block Diagram



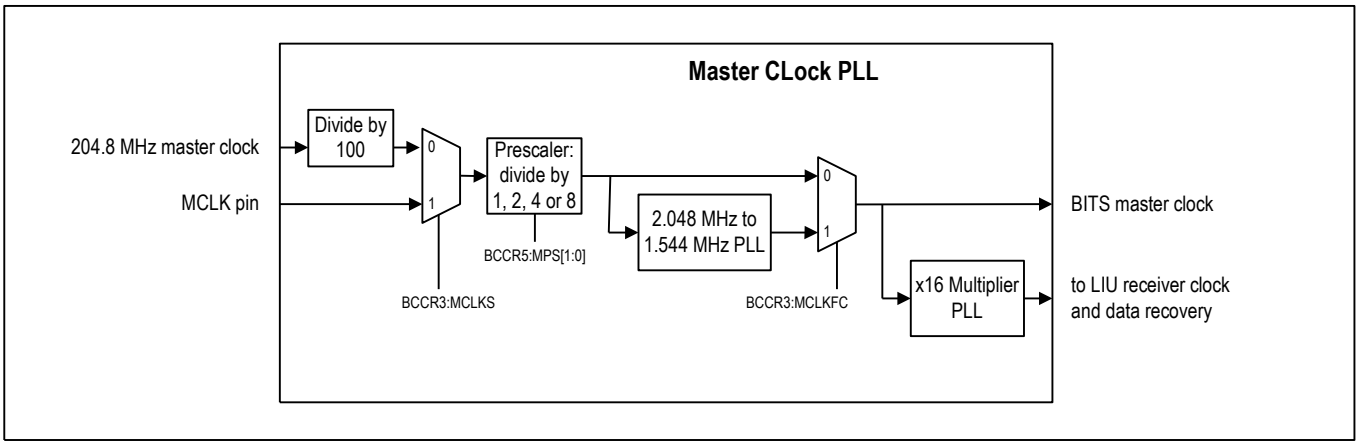
Note: The ZL81000 BITS transceivers are full-featured DS1/E1 LIUs and framers. To keep configuration as simple as possible, only the features most commonly used for clock synchronization applications are made visible in this data sheet. If your application requires LIU or framer features not described in this document, contact Microsemi timing products technical support for additional information.

6.9.1 Master Clock Connections

See Figure 6-2 and Figure 6-3. The master clock PLL block produces two clocks: (1) a 16X line rate oversampling clock for the receiver, and (2) the BITS master clock, which can optionally be used by the transmitter. Both of these clocks are made from the same BITS transceiver master clock. There are two possible sources for the BITS master clock: the 204.8MHz master clock and the MCLK input pin. Normally BCCR3:MCLKS is set to 0, to select the 204.8MHz master clock (see Section 6.3) divided by 100. The resulting 2.048MHz clock can be used as-is for E1 and 2048kHz synchronization or fed into a 2.048MHz to 1.544MHz frequency converter PLL for DS1 synchronization.

For special applications, MCLKS can be set to 1 to source the BITS transceiver master clock from the MCLK pin. When MCLKS = 1, the signal on the MCLK pin is divided by 1, 2, 4, or 8 (as specified by BCCR5:MPS[1:0]) and optionally passed through the 2.048MHz to 1.544MHz frequency-converter PLL (as specified by BCCR3:MCLKFC). For any BITS receiver mode, the signal on the MCLK pin can be 1, 2, 4, or 8 times 2.048MHz. For DS1 mode only, MCLK can be 1, 2, 4, or 8 times 1.544MHz. When MCLKS = 0, the MCLK pin is ignored and should be wired high or low.

Figure 6-3. BITS Transceiver Master Clock PLL Block Diagram



6.9.2 Receiver Clock Connections

See Figure 6-2. The BITS receiver typically outputs its recovered clock on its RCLK pin by setting BCCR3:RCEN = 1 to enable the pin. Also, the DS1/E1 frame sync or multiframe sync can be output on the ROUT pin by setting BCCR3:ROUTS appropriately and setting BCCR3:ROEN = 1 to enable the pin. The frame sync signal is normally low and pulses high for one RCLK cycle during the framing bit (DS1) or the first FAS bit (E1). The multiframe sync signal is normally low and pulses high for one RCLK cycle on the first bit of the multiframe. In E1 modes, the type of multiframe sync (CAS or CRC-4) can be specified in BRCR5:RMFS. The polarity of RCLK and ROUT can be inverted by setting BCCR3:RCINV and ROINV, respectively.

RCLK and RSYNC are automatically squelched by the BITS receiver during LOS. RCLK is squelched in the path to the RCLK output pin, but it is not squelched in the receive framer clock tree so that the framer continues to operate.

Figure 9-4 and Table 9-8 show the timing relationships among RCLK, ROUT, and RSER.

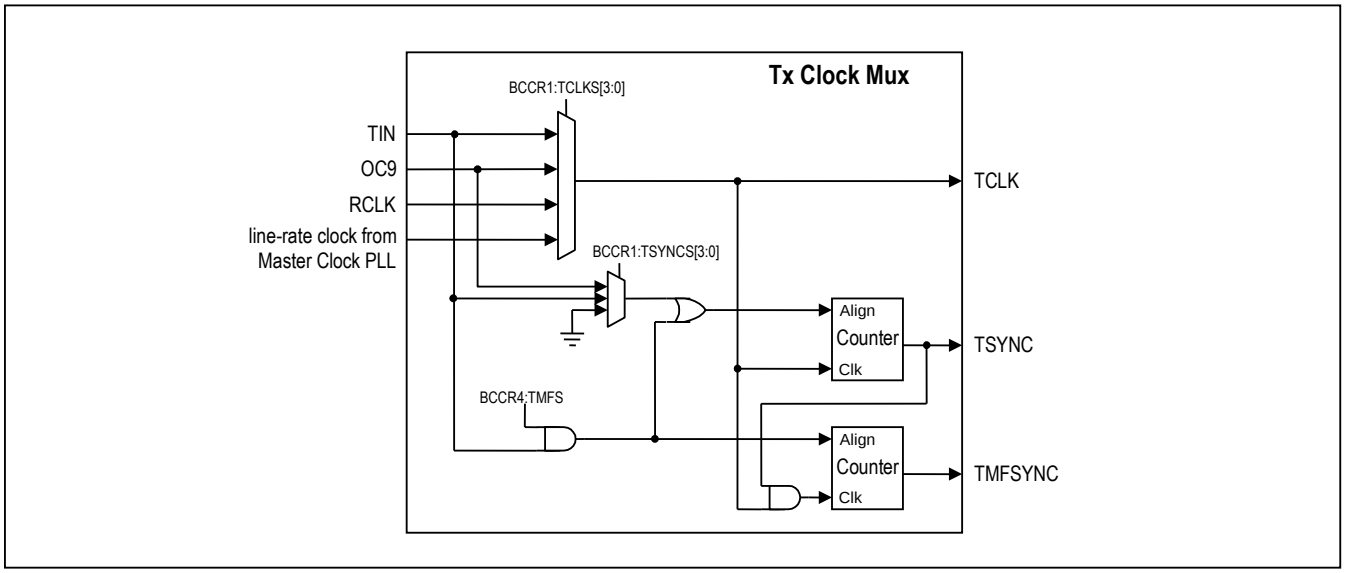
6.9.3 Transmitter Clock Connections

See Figure 6-2 and Figure 6-4. The BCCR1:TCLKS field specifies the source for the BITS transmitter clock (TCLK). Typically TCLK is sourced the TIN pin or the BITS master clock PLL.

In DS1 and E1 modes the BITS transmitter also requires a frame sync and/or multiframe sync signal to specify the start of the frame or multiframe. The frame sync signal is normally low and pulses high for one TCLK cycle on the first bit of the frame. The multiframe sync signal is normally low and pulses high for one TCLK cycle on the first bit

of the multiframe. The frame sync (TSYNC) signal is created in the Tx Clock Mux block by a counter circuit that outputs a signal that is normally low and pulses high for one TCLK cycle out of every 193 (DS1 mode) or 256 (E1 mode). The multiframe sync (TMFSYNC) signal is then created by another counter circuit that outputs a signal that is normally low and pulses high coincident with one TSYNC pulse out of every 12 (DS1 SF mode), 24 (DS1 ESF mode, or 16 (E1 mode). In many applications the DS1/E1 frame sync and multiframe sync signals are not required to be aligned with any other signal (other than rising-edge aligned to TCLK and each other), and therefore, by default, the TSYNC and TMFSYNC counter circuits are allowed to free-run without being aligned by an input signal (BCCR1:TSYNCS = 1111, BCCR4:TMFS = 0).

Figure 6-4. BITS Transmitter Clock Mux Block Diagram



For applications that require it, the leading edge of the TSYNC pulse can be aligned with a clock edge from the BITS transmitter's TIN input pin. The BCCR1:TSYNCS field specifies the source of the clock used to align TSYNC. For proper operation, the TSYNC source and the TCLK source must be frequency locked. Because the TSYNC counter circuit free-runs when not being actively aligned by an input signal, the TSYNC source clock can pulse just one time to establish TSYNC alignment or it can be a steady clock with a frequency of 8kHz or any integer divider of 8kHz. Duty cycle is not important for the TSYNC source clock.

For applications that require it, the TMFSYNC pulse can be aligned with a clock edge from the BITS transmitter's TIN input pin by setting BCCR4:TMFS = 1. Because the TMFSYNC counter circuit free-runs when not being actively aligned by an input signal, the TMFSYNC source clock can pulse just one time to establish TMFSYNC alignment or it can be a steady clock with a frequency of 8kHz / X (where X is 12 for DS1 SF mode, 24 for DS1 ESF mode, and 16 for E1 mode) or any integer divider of 8kHz / X. When the TMFSYNC pulse is aligned by a clock edge on the TIN pin, the TSYNC signal is automatically aligned as well to maintain frame/multiframe alignment (see the OR gate in Figure 6-4). Duty cycle is not important for the TMFSYNC source clock.

The TCLK signal can be output on the TCLK pin by setting BCCR4:TCEN = 1 to enable the pin. Optionally, the TSYNC signal or the TMFSYNC signal can be output on the TOUT pin by specifying the signal with BCCR4:TOUTS and setting BCCR4:TOEN = 1 to enable the pin. The polarity of the TIN, TCLK and TOUT pins can be inverted by setting BCCR4:TIINV, TCINV and TOINV, respectively. Finally, the data content of the DS1 or E1 frame can be sourced from the TSER pin if needed. Figure 9-5 and Table 9-9 show the timing relationships among TCLK, TIN, TOUT, and TSER.

6.9.4 Line Interface Unit

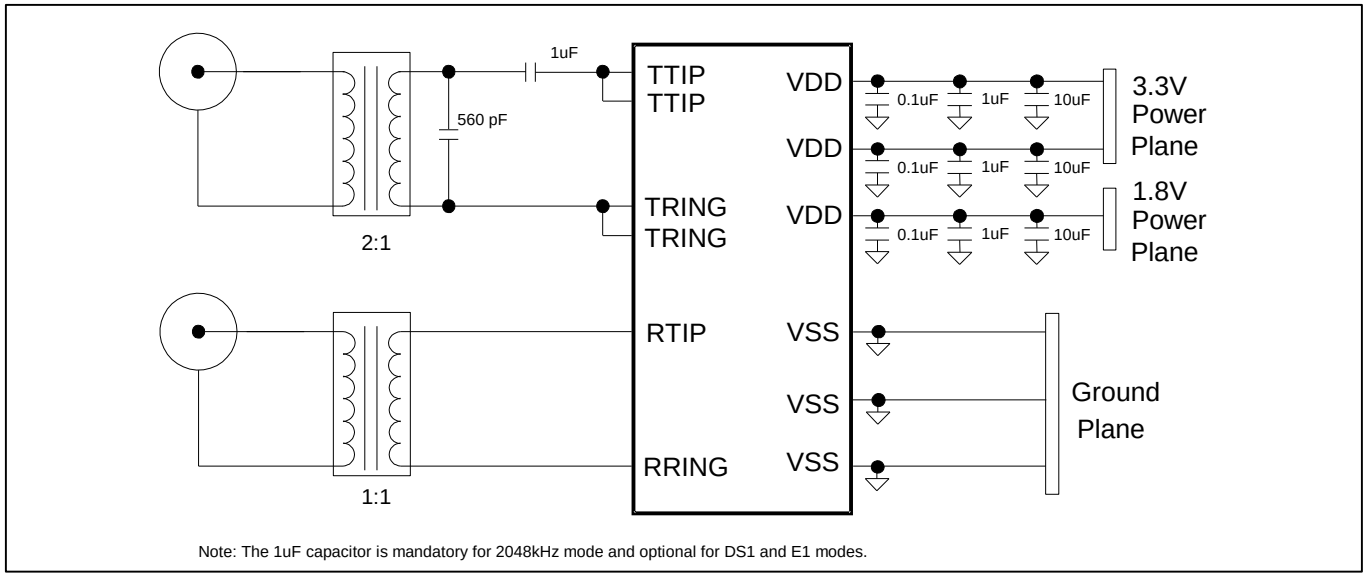
The line interface unit (LIU) contains the receiver, which recovers clock and data from the inbound cable, and the transmitter, which wave-shapes and drives the signal onto the outbound cable. These sections are controlled by the line interface control registers, BLCR1 through BLCR4.

The receiver has a usable receive sensitivity of 0dB to -43dB for E1 and 0dB to -36dB for DS1, which allows the device to operate on 0.63mm (22AWG) cables up to 2.5 km (E1) and 6000 feet (DS1) in length. The transmitter line driver can handle both CEPT 30/ISDN-PRI lines for E1 and long-haul (CSU) or short-haul (DSX-1) lines for DS1.

The receiver and transmitter can switch among the supported synchronization signal types without changing external components. Figure 6-5 shows the minimum set of external components required. Both the receiver and the transmitter can adjust their termination impedance to provide high return loss characteristics for 75Ω, 100Ω, 110Ω, and 120Ω lines. Other components may be added to this configuration in order to meet safety and network protection requirements, if required.

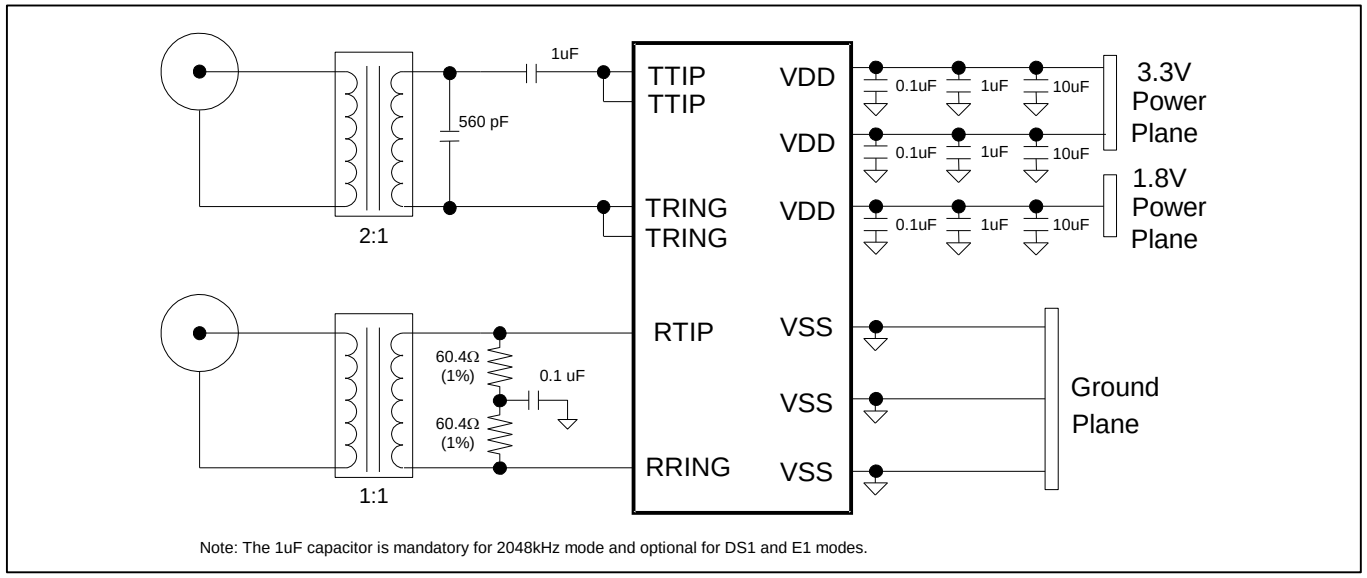
Figure 6-5. BITS Transceiver External Components

Internal Receiver Termination Enabled



Note: The 1uF capacitor is mandatory for 2048kHz mode and optional for DS1 and E1 modes.

Internal Receiver Termination Disabled



Note: The 1uF capacitor is mandatory for 2048kHz mode and optional for DS1 and E1 modes.

6.9.4.1 Receiver

6.9.4.1.1 Interfacing to the Line

The receiver can be transformer-coupled or capacitor-coupled to the line. Typically, the receiver interfaces to the incoming coaxial cable or twisted-pair wiring through a 1:1 isolation transformer. Figure 6-5 shows the arrangement of the transformer with either internal termination or external termination. For internal termination, set BLCR3:RION = 1 and set BLCR3:RIMP[1:0] to specify the termination impedance. For external termination, set BLCR3:RION = 0 and use external termination resistors as shown in Figure 6-5. Table 6-5 specifies the required characteristics of the transformer.

6.9.4.1.2 Receive Sensitivity

Receive sensitivity can be adjusted in DS1, E1, and 2048kHz modes using BLCR3:RSMS[1:0]. In 6312kHz mode, receive sensitivity is fixed at approximately -24dB.

6.9.4.1.3 Receive Level Indicator

The signal strength at RTIP/RRING is reported in 2.5dB increments in BLIR2:RL[3:0]. This feature is helpful when troubleshooting line performance problems.

6.9.4.1.4 Optional Monitor Mode

The receiver can be used in monitoring applications, which typically have flat losses from the use of series resistors. In these applications a pre-amp stage in the receiver can be configured to apply 14dB, 20dB, 26dB, or 32dB of flat gain to compensate for the resistive losses. The monitor mode preamp is enabled by setting BLCR3:RMONEN = 1 and configured by BLCR3:RSMS[1:0].

6.9.4.1.5 Clock and Data Recovery

The BITS receiver has an active filter that reconstructs the received analog signal for the nonlinear losses that occur in transmission. The BITS master clock (Section 6.9.1) is multiplied by 16 and used as the master clock for the APLL used in the receiver to recover clock and data. The receiver has excellent jitter tolerance as shown in Figure 6-6 and Figure 6-7.

Figure 6-6. Jitter Tolerance, DS1 Mode

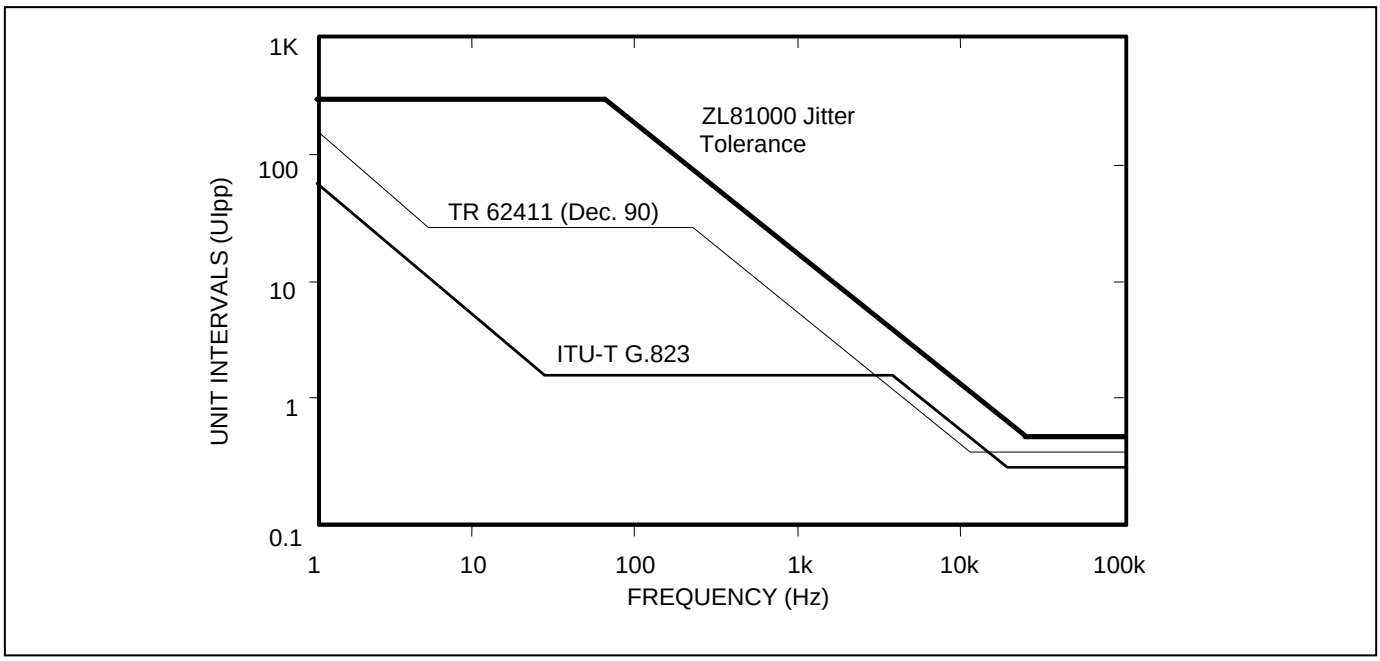
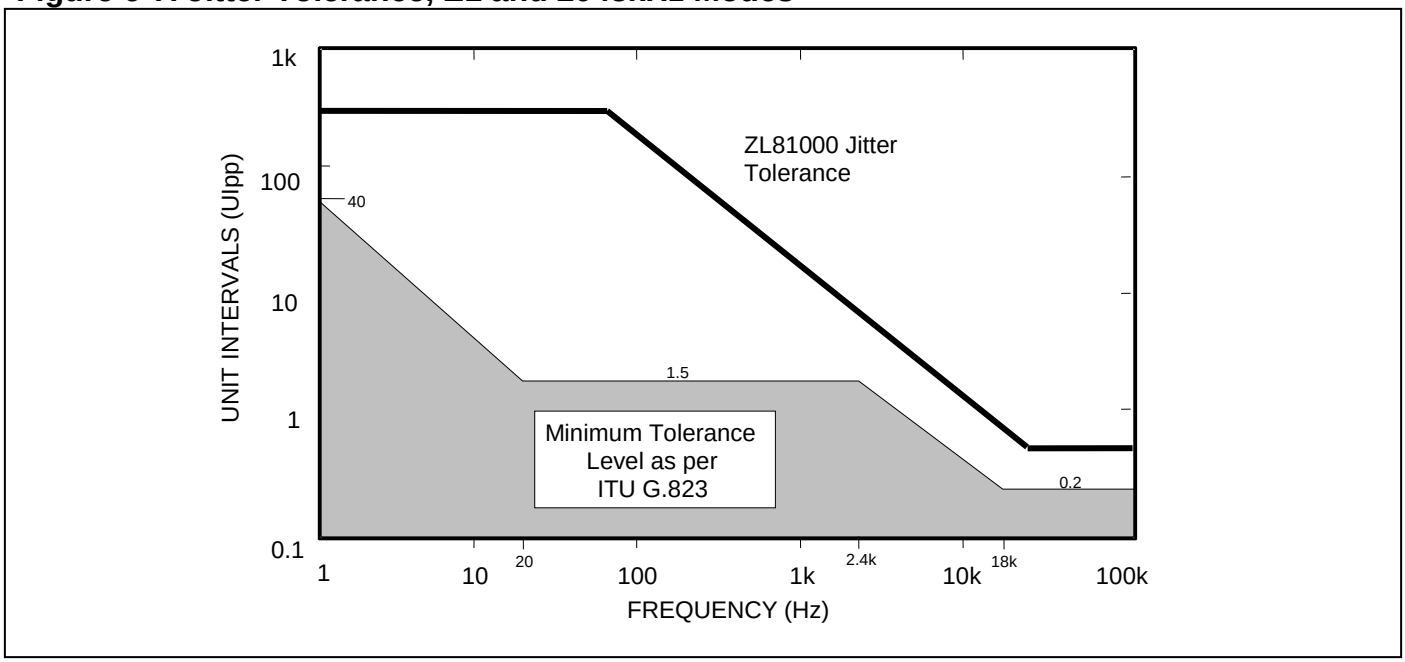


Figure 6-7. Jitter Tolerance, E1 and 2048kHz Modes



6.9.4.1.6 Loss-of-Signal Detection

In DS1 mode, LOS is declared when no pulses are detected (i.e., when the signal level is 6dB below the receive sensitivity level set by BLCR3:RSMS[1:0]) in a window of 192 consecutive pulse intervals. When LOS occurs, the receiver sets the real-time LOS status bit in BLIR1 and the latched LOS status bit in BLSR1. BLSR1:LOS in turn can cause and interrupt request on the INTREQ pin if enabled by BLIER1:LOS. LOS is cleared when 24 or more pulses are detected (amplitude greater than receive sensitivity minus 4dB) in a 192-bit period (pulse density above 12.5%) and there are no occurrences of 100 or more consecutive zeros during that period. This algorithm meets the requirements of ANSI T1.231. For example, if receive sensitivity is set at 18dB below nominal (BLCR3:RSMS[1:0], the LOS set threshold is 24dB below nominal, and the LOS clear threshold is 22dB below nominal.

In E1 and 2048kHz modes, if BLCR1:LCS = 0 the receiver is configured for ITU G.775 LOS detection. When configured in this manner, LOS is declared when no pulses are detected (i.e., when the signal level is 6dB below the receive sensitivity level set by BLCR3:RSMS[1:0]) in a window of 255 consecutive pulse intervals. When LOS occurs, the receiver sets the real-time LOS status bit in BLIR1 and the latched LOS status bit in BLSR1. BLSR1:LOS in turn can cause and interrupt request on the INTREQ pin if enabled by BLIER1:LOS. LOS is cleared when at least 32 pulses are detected (amplitude greater than receive sensitivity minus 4dB) in a window of 255 consecutive pulse intervals.

In E1 and 2048kHz modes, if BLCR1:LCS = 1 the receiver is configured for ETSI 300 233 LOS detection. When configured in this manner, LOS is declared when no pulses are detected (i.e., when the signal level is 6dB below the receive sensitivity level set by BLCR3:RSMS[1:0]) in a window of 2048 consecutive pulse intervals. When LOS occurs, the receiver sets the real-time LOS status bit in BLIR1 and the latched LOS status bit in BLSR1. BLSR1:LOS in turn can cause and interrupt request on the INTREQ pin if enabled by BLIER1:LOS. LOS is cleared when at least one pulse is detected (amplitude greater than receive sensitivity minus 4dB) in a window of 255 consecutive pulse intervals.

In 6312kHz mode, LOS is declared when the signal level is below -24dBm for a 32µs period.

6.9.4.1.7 Receiver Power-Down

The receiver can be powered down to reduce power consumption by setting BLCR4:RPD = 1. When the receiver is powered down, all digital outputs from the receiver are held low, and RTIP and RRING become high impedance.

6.9.4.2 Transmitter

6.9.4.2.1 Waveshaping

The BITS LIU transmitter uses a phase-locked loop along with a precision digital-to-analog converter (DAC) to create the waveforms that are transmitted onto the outbound cable. The waveforms meet the latest ANSI, ETSI, ITU and Telcordia specifications (see Figure 6-8, Figure 6-9, and Figure 6-10). The BMCR:TMODE[1:0] field specifies the waveform to be generated, along with the line build out field in BLCR2:LBO[2:0], if applicable. Due to the nature of its design, the transmitter adds very little jitter (less than $0.005UI_{P-P}$ broadband from 10Hz to 100kHz) to the transmit signal. Also, the waveforms created are independent of the duty cycle of TCLK.

6.9.4.2.2 Line Build-Out

The transmitter line driver can handle both CEPT 30/ISDN-PRI lines for E1 and long-haul (CSU) or short-haul (DSX-1) lines for DS1. The LBO[2:0] field in BLCR2 specifies the line build-out for DS1 and E1.

6.9.4.2.3 Line Driver Enable/Disable

When the THZE pin is high or when BLCR4:TE = 0, the transmitter line driver is disabled, and TTIP/TRING are put in a high-impedance state. When the THZE pin is low and BLCR4:TE = 1, the line driver is enabled.

6.9.4.2.4 Interfacing to the Line

The transmitter is transformer-coupled to the line. Typically, the transmitter interfaces to the outgoing coaxial cable or twisted-pair wiring through a 1:2 isolation transformer. Figure 6-5 shows the arrangement of the transformer with respect to the TTIP and TRING pins. On the ZL81000 the transmitter termination is always internal. Set BLCR2:TION = 1 and set BLCR2:TIMP[1:0] to specify the termination impedance. Table 6-5 specifies the required characteristics of the transformer.

6.9.4.2.5 AIS Generation

When BLCR4:TAIS = 1, the transmitter generates AIS (unframed all ones) using the BITS master clock as the timing reference.

6.9.4.2.6 Short-Circuit Detector

The BITS transmitter has an automatic short-circuit detector that activates when the short-circuit resistance is approximately 25Ω or less. BLIR1:SC provides a real-time indication of when the short-circuit limit has been exceeded. Latched status bits BLSR1:SC and SCC are set when BLIR1:SC changes state from low-to-high and high-to-low, respectively. These latched status bits can cause an interrupt request if enabled by the corresponding bits in BLIER1. The short-circuit detector is disabled for CSU modes (i.e., when BLCR2:LBO[2:0] = 101, 110, or 111).

6.9.4.2.7 Open-Circuit Detector

The BITS transmitter can also detect when TTIP and TRING are open circuited. BLIR1:OC provides a real-time indication of when the open-circuit limit has been exceeded. Latched status bits BLSR1:OC and OCC are set when BLIR1:OC changes state from low-to-high and high-to-low, respectively. These latched status bits can cause an interrupt request if enabled by the corresponding bits in BLIER1. The open-circuit detector is disabled for CSU modes (i.e., when BLCR2:LBO[2:0] = 101, 110, or 111).

6.9.4.2.8 Transmitter Power-Down

The transmitter can be powered down to reduce power consumption by setting BLCR4:TPD = 1. When the transmitter is powered down, TTIP and TRING are high impedance.

Figure 6-8. Transmit Pulse Template, DS1 Mode

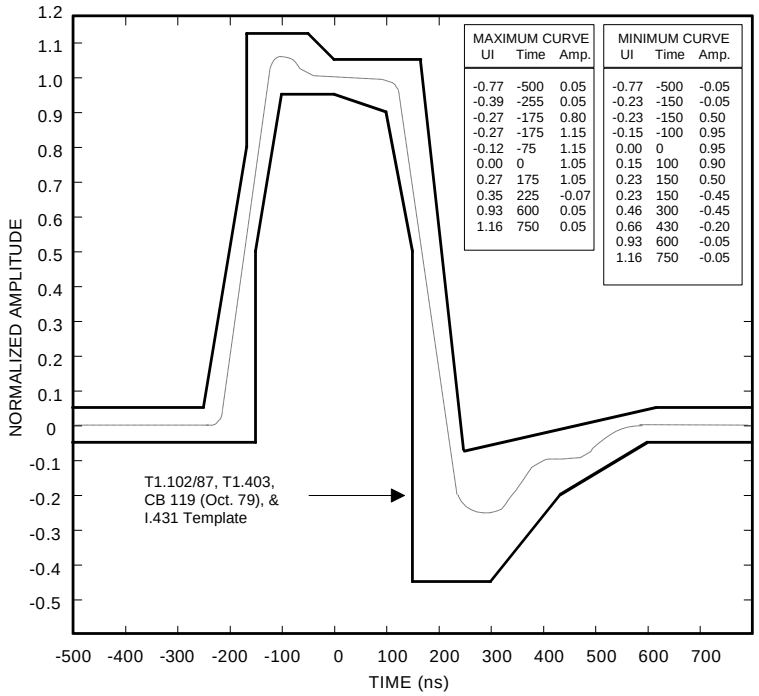


Figure 6-9. Transmit Pulse Template, E1 Mode

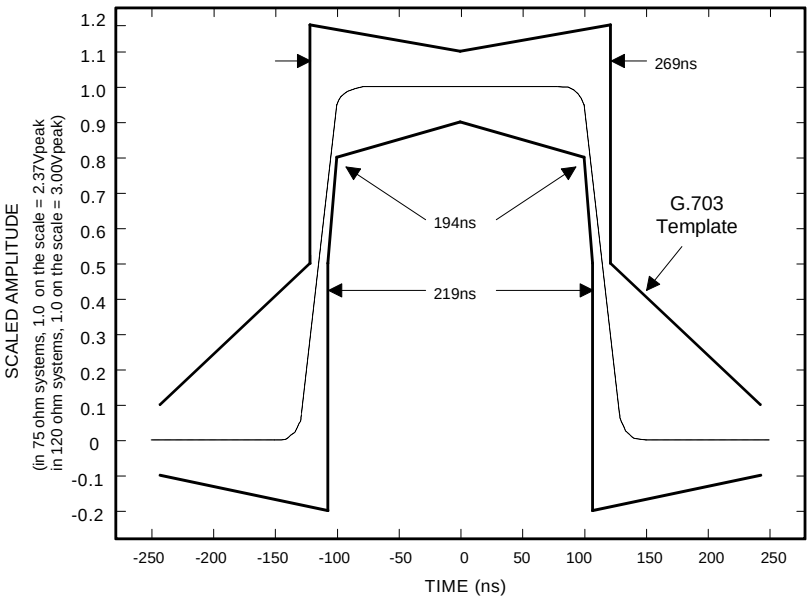
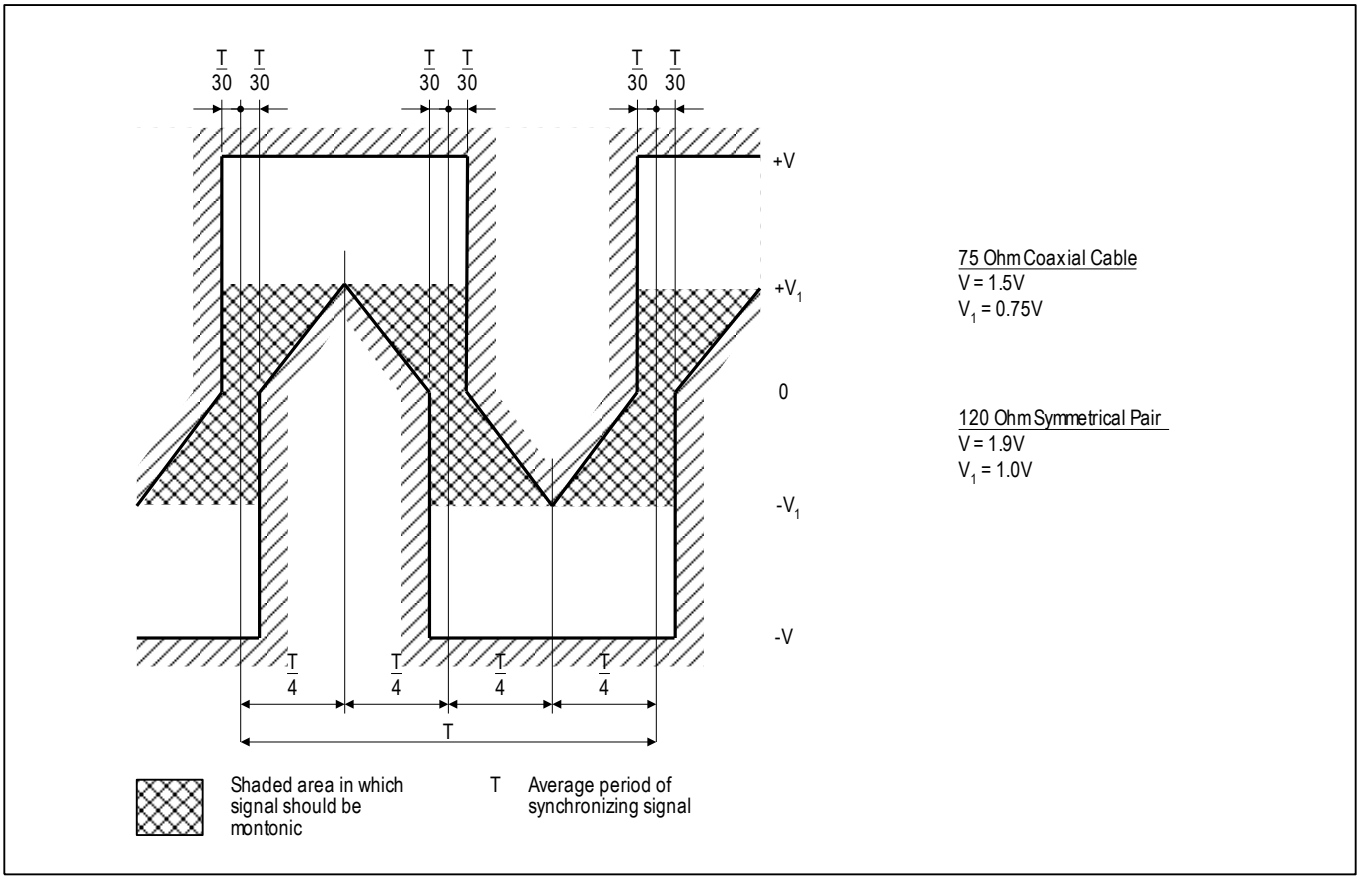


Figure 6-10. Transmit Pulse Template, 2048kHz Mode



6.9.4.3 LIU Loopbacks

The BITS LIU provides three loopbacks for diagnostic purposes: analog loopback, local loopback, and remote loopback. See Figure 6-2. These loopback are enabled by the ALB, LLB, and RLB bits in BLCR4.

6.9.4.4 Component Specifications

Table 6-5. Transformer Specifications

SPECIFICATION		RECOMMENDED VALUE
Turns Ratio	Receiver	1:1 or 2:1 (±2%)
	Transmitter	1:2 (±2%)
Primary Inductance		600µH minimum
Leakage Inductance		1.0µH maximum
Intertwining Capacitance		40pF maximum
Transmit Transformer DC Resistance	Primary (Device Side)	1.2Ω maximum
	Secondary	1.2Ω maximum
Receive Transformer DC Resistance	Primary (Device Side)	1.2Ω maximum
	Secondary	1.2Ω maximum
Isolation Voltage		1500 V_{RMS} (min)

Note: *Recommended transformers include the Pulse Engineering PE-68678 (0°C to +70°C) and T1094 (-40°C to +85°C), both of which are surface-mount dual transformers (1:1 and 1:2).*

6.9.5 DS1 Synchronization Interface

Each BITS transceiver receives and transmits standards-compliant DS1 synchronization signals. As a configuration option of DS1, the BITS transceivers can also be configured for the Japanese J1 interface.

6.9.5.1 Receive Framer

In the receive direction, the BITS transceiver recovers clock and data, does B8ZS decoding, finds frame alignment, and extracts incoming SSM messages. Each BITS receiver can be configured for DS1 mode by following these steps:

1) Set the overall mode of the receiver to DS1 by setting BMCR:RMODE = 00.
2) Configure and enable the DS1/E1 framer in the BRMMR register as follows:
   (a) toggle RRST high then low,
   (b) set RT1E1 = 0 to configure the framer for DS1 mode,
   (c) set registers BRCR1, BRCR2 and BRCR5 as needed,
   (d) set REN = 1 to enable the framer, and
   (e) set RID = 1 to start the framer.
3) Configure and enable the LIU receiver as described in Section 6.9.4.1.

Registers BRCR1, BRCR2 and BRCR5 configure the receive framer in DS1 mode. BRCR1:RFM specifies superframe or extended superframe mode. BRCR1:RB8ZS enables B8ZS decoding. The receive framer can be configured for J1 operation by setting BRCR1:RJC = 1 and BRCR2:RSFRAI = 1. Status register BRIR1 has real-time status bits to indicate the presence of RAI, AIS, LOS and OOF conditions, while status register BRSR1 has latched versions of these same status bits. (See Table 6-6 for alarm set and clear criteria.) The onset or clearing of any of these events can cause an interrupt request on the INTREQ pin if enabled to do so by the corresponding enable bits in the BRIER1 register. Status registers BRSR2 and BRSR4 provide additional status information.

The entire received DS1 data stream is available on the RSER pin for additional processing by external hardware, if needed. RSER is updated on the rising edge of the RCLK pin by default, but this can be changed to the falling edge by setting BCCR3:RCINV = 1.

Table 6-6. DS1 Alarm Criteria

ALARM		SET CRITERIA	CLEAR CRITERIA
AIS (Note 1)		Four or fewer 0s are received during a 3ms window.	Five or more 0s are received during a 3 ms window.
RAI	SF Bit-2 Mode (Note 2)	Bit 2 is set to zero in at least 254 of 256 consecutive channel time slots.	Bit 2 is set to zero in less than 254 of 256 consecutive channel time slots.
	SF 12th F-Bit Mode (Note 2)	The 12th framing bit is set to 1 for two consecutive occurrences.	The 12th framing bit is set to 0 for two consecutive occurrences.
	ESF Mode	16 consecutive patterns of 00FFh appear in the FDL.	14 or fewer patterns of 00FFh appear in 16 consecutive opportunities in the FDL.
LOS		192 consecutive zeros received	14 or more ones received out of 112 possible bit positions, starting with the first one received.
OOF		Two or more errored-frame bits out of every four, five, or six frame bits. (Configured by BRCR2:OOFC[1:0].)	Fewer than two errored-frame bits out of every four, five, or six frame bits. (Configured by BRCR2:OOFC{1:0].)

Note 1: AIS is an unframed all-ones signal. AIS detectors should be able to operate properly in the presence of a 10^{-3} error rate and must not declare AIS in the presence of a *framed* all-ones signal. The BITS transceiver block has been designed to achieve this performance.

Note 2: In SF framing mode, the RAI type is configured by the RSFRAI bit in the BRCR2 register. The method of indicating RAI using the 12th F-Bit in SF mode is also known as Japanese Yellow Alarm.

6.9.5.2 Transmit Formatter

In the transmit direction, the BITS transceiver formats the outgoing data stream, inserts SSM messages, does B8ZS encoding, and drives the outgoing cable with standards-compliant waveshapes. Each BITS transmitter can be configured for DS1 mode by following these steps:

1) Set the overall mode of the transmitter to DS1 by setting BMCR:TMODE = 00.
2) Configure and enable the DS1/E1 framer in the BTMMR register as follows:
   (a) toggle TRST high then low,
   (b) set TT1E1 = 0 to configure the framer for DS1 mode,
   (c) set registers BTCR1, BTCR2, and BTCR3 as needed,
   (d) set TEN = 1 to enable the framer, and
   (e) set TID = 1 to start the framer.
3) Configure and enable the LIU transmitter as described in Section 6.9.4.2.

Registers BTCR1, BTCR2, and BTCR3 configure the transmit formatter in DS1 mode. BTCR3:TFM specifies superframe or extended superframe mode. BTCR1:TB8ZS enables B8ZS encoding. The transmit formatter can be configured for J1 operation by setting BTCR1:TJC = 1 and BTCR2:TSFRAI = 1. In register BTCR1, fields TAIS and TRAI control the transmission of AIS and RAI signals, respectively. Status register BTSR1 provides latched status information from the transmit formatter.

Payload is sourced from the TSER pin. GR-1244-CORE Section 2.4 recommends an all-ones payload, which can be achieved be wiring TSER high. TSER is sampled on the falling edge of the TCLK pin by default, but this can be changed to the rising edge by setting BCCR4:TCINV = 1.

6.9.5.3 DS1 SSM Extraction and Insertion

Although synchronization DS1s can have superframe (SF) or extended superframe (ESF) framing format, only DS1s in ESF format can carry SSMs. Therefore, BTCR3:TFM must be set for ESF mode to support SSMs in outgoing derived DS1s, while BRCR1:RFM must be set for ESF mode to support SSMs in incoming DS1s from the timing signal generator. In an ESF DS1, SSMs are transmitted in the data link as a bit-oriented code (BOC) (T1.403: “bit-patterned message”). SSMs have the format 0xxxxxx011111111 (right-to-left), where xxxxxx are the six information bits of the message. ANSI standard T1.101 lists the SSM codes carried by DS1 timing signals.

On the receive side, the BITS transceivers each have a dedicated bit-oriented code (BOC) detector, which is always enabled. When the incoming SSM changes, the BOC detector validates it according to the criteria specified by the RBF field in BRBCR) before declaring it valid. Once validated, the six information bits of the new SSM are written to the lower six bits of the BRBOC register, and the BD status bit in BRSR4 is set to indicate that a new SSM has arrived.

The procedure to receive SSMs is as follows:

1) Set the validation filter in BRBCR:RBF.
2) (Optional) Enable the BD status bit to cause interrupt requests by setting BD = 1 in BRIER4.
3) Wait for an interrupt request or poll BRSR4 for BD = 1.
4) Read the SSM from the lower six bits of the BRBOC register.

If the incoming DS1 signal no longer has a valid BOC, the BOC detector waits for the number of message bits specified by BRBCR:RBD[1:0] before declaring that a valid BOC is no longer detected by setting BRSR4:BC = 1. The BC field can cause an interrupt request if BRIER4:BC = 1.

On the transmit side, the BITS transceivers each have a dedicated BOC generator. When SBOC = 1 in BTBCR the BOC generator uses the lower six bits of the BTBOC register to continually insert SSMs into the ESF data link. BTCR1:TFPT must be set to zero when SBOC = 1.

The procedure to transmit SSMs is as follows:

1) Write the 6 information bits of the SSM to the BTBOC register.
2) Set SBOC = 1 in BTBCR.

6.9.6 E1 Synchronization Interface

Each BITS transceiver receives and transmits standards-compliant E1 synchronization signals.

6.9.6.1 Receive Framer

In the receive direction, the BITS transceiver recovers clock and data, does HDB3 decoding, finds frame alignment, and extracts incoming SSM messages. Each BITS receiver can be configured for E1 mode by following these steps:

1) Set the overall mode of the receiver to E1 by setting BMCR:RMODE = 01.
2) Configure and enable the DS1/E1 framer in the BRMMR register as follows:
   (a) toggle RRST high then low,
   (b) set RT1E1 = 1 to configure the framer for E1 mode,
   (c) set registers BRCR3, BRCR4 and BRCR5 as needed,
   (d) set REN = 1 to enable the framer, and
   (e) set RID = 1 to start the framer.
3) Configure and enable the LIU receiver as described in Section 6.9.4.1.

Registers BRCR3, BRCR4 and BRCR5 configure the receive framer in E1 mode. BRCR3:RCRC4 enables CRC-4 framing mode. BRCR3:RHDB3 enables HDB3 decoding. Status register BRIR1 has real-time status bits to indicate the presence of RAI, AIS, LOS and OOF conditions, while status register BRSR1 has latched versions of these same status bits. (See Table 6-6 for alarm set and clear criteria.) The onset or clearing of any of these events can cause an interrupt request on the INTREQ pin if enabled to do so by the corresponding enable bits in the BRIER1 register. Additional FAS/CAS/CRC-4 frame sync status information is available in register BRSR3. See Table 6-8 for E1 sync and resync criteria.

The entire received E1 data stream is available on the RSER pin for additional processing by external hardware, if needed. RSER is updated on the rising edge of the RCLK pin by default, but this can be changed to the falling edge by setting BCCR3:RCINV = 1.

Table 6-7. E1 Alarm Criteria

ALARM	SET CRITERIA	CLEAR CRITERIA	ITU SPEC
AIS	Fewer than three zeros in two frames (512 bits)	Three or more zeros in two frames (512 bits)	O.162 1.6.1.2
RAI	Bit 3 of non-FAS frame set to one three consecutive occasions	Bit 3 of non-FAS frame set to zero for three consecutive occasions	O.162 2.1.4
LOS	255 or 2048 consecutive zeros received (determined by BRCR4:RLOSC)	At least 32 ones received in 255 bit times	G.775 4.2
OOF	See Table 6-8.	See Table 6-8.	—

Table 6-8. E1 Sync and Resync Criteria

FRAME OR MULTIFRAME TYPE	SYNC CRITERIA	RESYNC CRITERIA	ITU SPEC
FAS	FAS present in frames N and N+2 and FAS not present in frame N+1.	If BRCR3:FRC = 0, three consecutive incorrect FAS. If BRCR3:FRC = 1, three consecutive incorrect FAS or three consecutive incorrect bit 2 of non-FAS frame	G.706 4.1.1 4.1.2
CRC-4	Two valid multiframe alignment words found within 8ms.	915 or more errored CRC-4 blocks out of 1000.	G.706 4.2 and 4.3.2
CAS	Valid multiframe alignment word found.	Two consecutive multiframe alignment words received in error or, for a period of one multiframe, all the bits in time slot 16 are zero.	G.732 5.2

6.9.6.2 Transmit Formatter

In the transmit direction, the BITS transceiver formats the outgoing data stream, inserts SSM messages, does HDB3 encoding, and drives the outgoing cable with standards-compliant waveshapes. Each BITS transmitter can be configured for E1 mode by following these steps:

1) Set the overall mode of the receiver to E1 by setting BMCR:TMODE = 01.
2) Configure and enable the DS1/E1 framer in the BTMMR register as follows:
   (a) toggle TRST high then low,
   (b) set TT1E1 = 1 to configure the framer for E1 mode,
   (c) set registers BTCR3 and BTCR4 as needed,
   (d) set TEN = 1 to enable the framer, and
   (e) set TID = 1 to start the framer.
3) Configure and enable the LIU transmitter as described in Section 6.9.4.2.
4) Configure BTAF=1Bh and BTNAF=40h to set up the transmit E1 framing overhead.

Registers BTCR3 and BTCR4 configure the transmit formatter in E1 mode. BTCR4:TCRC4 enables CRC-4 framing mode. BTCR4:THDB3 enables HDB3 encoding. BTCR4:TAIS controls the transmission of the AIS signal. Status register BTSR1 provides latched status information from the transmit formatter.

Payload, and optionally overhead bits, can be sourced on the TSER pin from external hardware, if needed. TSER is sampled on the falling edge of the TCLK pin by default, but this can be changed to the rising edge by setting BCCR4:TCINV = 1.

6.9.6.3 Basic FAS/Si/RAI/Sa Insertion and Extraction

The most basic E1 framing is a double frame consisting of an align frame followed by a non-align frame. The align frame is the E1 frame containing the frame alignment signal (FAS) while the non-align frame is the E1 frame that does not contain the FAS.

On the receive side, the BRAF and BRNAF registers always report the contents of the first eight bits of the align frame and the non-align frame, respectively. Both registers are updated at the start of the align frame, which is indicated by the RAF status bit in BRSR3. After RAF is set to 1, software has 250µs to read the registers before they are overwritten by the bits from the next double-frame.

On the transmit side, the BTAF and BTNAF registers can source the first eight bits of the align frame and the non-align frame, respectively. Data is sampled from these registers at the start of the align frame, which is indicated by the TAF status bit in BTSR1. After TAF is set to 1, software has 250µs to update the registers with new values (if needed) before they are sampled again for the next double-frame. BTAF and BTNAF are the default sources for the FAS, Si, RAI and Sa bits. However, various control fields can cause some of these bits to be sourced from elsewhere. Figure 6-11 shows the possible sources and their relative priorities.

6.9.6.4 CRC-4 Multiframe Si/RAI/Sa Insertion and Extraction

On the receive side, the eight registers BRSa4 through BRSa8, BRSiAF, BRSiNAF and BRRAI report the corresponding overhead bits of the CRC-4 multiframe as they are received. These registers are updated at the start of the next CRC-4 multiframe, which is indicated by the RCMF status bit in BRSR3. After RCMF is set to 1, software has 2ms to read the registers before they are overwritten by the bits from the next multiframe.

On the transmit side, the eight registers BTSa4 through BTSa8, BTSiAF, BRSiNAF and BTRAI can source the corresponding overhead bits of the multiframe. The control bits in the BTOCR register enable the sourcing of Si/RAI/Sa bits from these registers. Data is sampled from these registers at the start of the multiframe, which is indicated by the TMF status bit in BTSR1. After TMF is set to 1, software has 2ms to update the registers (if needed) before they are sampled again for the next multiframe.

6.9.6.5 SSM Extraction and Insertion

G.704 specifies that synchronization status messages (SSMs) are transmitted in one of the Sa bit channels of the CRC-4 multiframe. All eight instances of the chosen Sa bit within the multiframe are used for the SSM. The four instances of the chosen Sa bit within the first sub-multiframe carry one copy of the SSM, and the four instances within the second sub-multiframe carry another copy. Each copy of the SSM is sent MSB first and is aligned with the start of the sub-multiframe. ITU recommendation G.704 lists the SSM codes carried by E1 signals.

To extract SSMs from the incoming E1 data stream, the receive framer should be configured for CRC-4 multiframing (BRCR3:RCRC4 = 1). Once in this mode, system software can read incoming SSMs from the appropriate BRSaX register (X = 4, 5, 6, 7, or 8) at any time. See Section 6.9.6.4. When an incoming SSM changes, the BITS receiver validates the new value according to the criteria specified in BRMCR:SSMF. When a new SSM is validated in one of the Sa-bit channels, the corresponding status bit is set in the BRMSR register, which can cause an interrupt if enabled by the corresponding interrupt enable bit in the BRMIER register. The most recently validated SSM message in an Sa-bit channel can be read by specifying the channel in BRMCR:SSMCH and reading the SSM message from the BRSSM register.

To insert SSMs into the outgoing E1 data stream, the transmit formatter should be configured for CRC-4 multiframing (BTCR4:TCRC4 = 1), and the appropriate bit(s) in the BTOCR register should be set to enable the sourcing of the selected Sa bit(s) from the corresponding BTSaX register(s). See Section 6.9.6.4.

Figure 6-11. FAS/Si/RAI/Sa Source Logic

```
FAS bits
if BTCR4.TFPT=1 then source from TSER pin
    else source from BTAF register

Si bits, align frame
if BTOCR.SiAF=1 then source from BTSiAF register
    else if BTCR4:TCRC4=1 then source from CRC-4 generator
        else if BTCR4.TSiS=0 then source from TSER pin
            else if BTCR4.TFPT=1 then source from TSER pin
                else source from BTAF register

Si bits, non-align frame
if BTOCR.SiNAF=1 then source from BTSiNAF register
    else if BTCR4:TCRC4=1 then source from CRC-4 generator
        else if BTCR4.TSiS=0 then source from TSER pin
            else if BTCR4.TFPT=1 then source from TSER pin
                else source from BTNAF register

SaX bit (X=4, 5, 6, 7 or 8)
if BTOCR.SaX=1 then source from BTSaX register
    else if BTCR4.TFPT=1 then source from TSER pin
            else source from BTNAF register
```

6.9.7 G.703 2048kHz Synchronization Interface

The G.703 2048kHz synchronization interface is an unframed all-ones signal with specifications shown in Table 6-9. Figure 6-5 shows the external components required to operate the receiver and/or transmitter in this mode.

6.9.7.1 Receiver

The BITS receiver is configured for 2048kHz mode when RMODE = 10 in BMCR. The receiver line impedance must be configured for 75Ω or 120Ω by setting BLCR3:RIMP[2:0] = 00 or 11. The LIU receiver declares loss of signal (BLIR1:LOS) as described in Section 6.9.4.1.6.

6.9.7.2 Transmitter

The BITS transmitter is configured for 2048kHz mode when BMCR:TMODE = 10. In this mode, the transmitter line impedance must be configured for 75Ω or 120Ω by setting BLCR2:TIMP[2:0] = 00 or 11. In addition, the transmitter line build-out must be configured for 75Ω or 120Ω by setting BLCR2:LBO[2:0] = 000 or 001.

After configuring the transmitter for 2048kHz mode and 75Ω as described above, the following write sequence must be done to optimize the LIU transmitter:

write 01h to address 1FFh
write F8h to address 195h (BITS1) or 1A5h for (BITS2)
write 00h to address 199h (BITS1) or 1A9h (BITS2)
write 00h to address 1FFh

After configuring the transmitter for 2048kHz mode and 120Ω as described above, the following write sequence must be done to optimize the LIU transmitter:

write 01h to address 1FFh
write F8h to address 195h (BITS1) or 1A5h (BITS2)
write 09h to address 199h (BITS1) or 1A9h (BITS2)
write 00h to address 1FFh

When switching the BITS transmitter from 2048kHz to some other mode, the following write sequence must be done after writing BMCR:TMODE≠10:

write 01h to address 1FFh
write 00h to address 195 h (BITS1) or 1A5h (BITS2)
write 00h to address 199h (BITS1) or 1A9h (BITS2)
write 00h to address 1FFh

The output signal meets the template of G.703, shown in Figure 6-10. The nominal output amplitude is 1.2V typical for 75Ω LBO and 1.5V typical for 120Ω LBO.

Table 6-9. 2048kHz Synchronization Interface Specification

PARAMETER	COAX SPECIFICATION	TWISTED PAIR SPECIFICATION
Pulse Shape	Must conform with mask of G.703 Figure 20	
Transmission Media	Coaxial pair	Symmetrical pair
Test Load Impedance	75Ω resistive	120Ω resistive
Maximum Peak Voltage	1.5V	1.9V
Minimum Peak Voltage	0.75V	1.0V

6.9.8 G.703 Appendix II 6312kHz Japanese Synchronization Interface

The 6312kHz synchronization interface in G.703 Appendix II is a Japanese timing signal with the specifications shown in Table 6-10.

6.9.8.1 Receiver

The BITS receiver is configured for 6312kHz mode when RMODE = 11 in BMCR. The receiver line termination must be configured for 75Ω by setting RIMP[2:0] = 00 in BLCR3. The LIU receiver declares loss of signal (BLIR1:LOS=1) when the incoming signal level is below -24dBm. The receiver accepts both sine-wave and square-wave signals.

6.9.8.2 Transmitter

The BITS transmitter does not transmit the 6312 kHz signal.

Table 6-10. 6312kHz Synchronization Interface Specification

PARAMETER	SPECIFICATION
Frequency	6312kHz
Signal Format	Sinusoidal wave
Transmission Medium	Coaxial cable
Load Impedance	75Ω resistive
Amplitude	0 ± 3dBm
Alarm Condition for Received Signal Amplitude	No alarm for amplitudes between -16dBm and + 3dBm

6.10 Composite Clock Receivers

Input clocks IC1A and IC2A are composite clock receivers. These inputs support the following composite clock variations:

- GR-378 composite clock (Note 1)
- G.703 centralized clock (Note 2)
- G.703 Japanese synchronization interface (Note 3)

Note 1: Complies with Telcordia GR-378 composite clock and G.703 Section 4.2.2 centralized clock option b).

Note 2: Complies with ITU_T G.703 Section 4.2.2 centralized clock options a) and G.703 Section 4.2.3 contradirectional interface clock.

Note 3: Complies with ITU_T G.703 Appendix II.1 options a) and option b) Japanese synchronization interfaces.

Composite clock (CC) signals provide both bit and byte synchronization for equipment with DS0 connections. In all CC variations, the signal is a 64kHz AMI signal with an embedded 8kHz clock indicated by a deliberate bipolar violation (BPV) every 8 clock cycles. The option b) Japanese synchronization interface in G.703 Appendix II.1 also has an embedded 400Hz clock indicated by a BPV *removed* every 400Hz. Details about the several composite clock variations are described in the following paragraphs and summarized in Table 6-11.

GR-378 Composite Clock. As shown in Table 6-12 and Figure 6-12, the GR-378 composite clock signal has a 5/8 duty-cycle square pulse and a 133Ω line impedance. The G.703 Section 4.2.2 option b) centralized clock specifications are nearly identical to the GR-378 composite clock, with the exception of line termination impedance (110Ω for G.703 vs. 133Ω for GR-378).

G.703 Centralized Clock and other 64kHz + 8kHz Timing Signals. G.703 Section 4.2.2 defines two centralized clock types, option a) and option b). Option b) is discussed in the GR-378 paragraph above. As shown in Table 6-13, the option a) centralized clock has a 50% duty cycle and a 110Ω line impedance. G.703 also specifies three other timing signals that have characteristics and specifications that are nearly identical to those of centralized clock option a). These other signals are (1) the timing signal in the 64kbps contradirectional interface defined in G.703 Section 4.2.3, (2) the 64kHz + 8kHz Japanese timing signal defined in G.703 Appendix II.1, and (3) the 64kHz + 8kHz + 400Hz Japanese timing signal defined in G.703 Appendix II.1 (which has the 8kHz BPV removed every 400Hz). Table 6-13 tabulates the requirements for each of these signals.

Table 6-11. Composite Clock Variations

VARIATION	LINE IMPEDANCE (Ω0)	PULSE AMPLITUDE (V)	NOMINAL DUTY CYCLE	BPVs
Composite Clock, GR-378	133	2.7 to 5.5	5/8	8kHz
Centralized Clock, G.703 4.2.2 option b)	110	3.0 ± 0.5	5/8	8kHz
Centralized Clock, G.703 4.2.2 option a)	110	1.0 ± 0.1V	50%	8kHz
Japanese Sync Interface, G.703 Appendix II.1 option a)	110	≤ 1 ± 0.1	50%	8kHz
Japanese Sync Interface, G.703 Appendix II.1 option b)	110	≤ 1 ± 0.1	50%	8kHz, but removed at 400Hz
Contradirectional Interface Clock, G.703 4.2.3	120	1.0 ± 0.1	50%	8kHz

6.10.1 IC1A and IC2A Receivers

Input clocks IC1A and IC2A are composite clock receivers. These inputs can directly receive incoming AMI-coded 64kHz CC signals, including those with the pre-emphasis described in GR-378 Section 4.2. See the electrical specifications in Table 9-6, and the recommended external components in Figure 9-3.

Each CC receiver derives an 8kHz clock from the 8kHz component of the incoming CC signal. It is this 8kHz clock that is forwarded to the input clock monitoring and selection circuitry. The falling edge of this 8kHz clock can be configured to coincide with the leading edge of the 8kHz BPV or the leading edge of the pulse following the BPV, as specified by the CCEDGE field in the MCR5 register.

Incoming composite clock signals are monitored for loss-of-signal and AMI violations. When either of these signal conditions occurs, a corresponding latched status bit is set in register MSR3. When set, these status bits can cause an interrupt request on the INTREQ pin if enabled by the corresponding bits in IER3. Loss of signal is declared when no pulses are detected in the incoming signal in a 32µs period (i.e., after two missing pulses, voltage threshold V_{LOS} = 0.2V typical). The amplitude threshold for detecting a pulse is 0.2V. An AMI violation is declared when a deviation from the expected pattern of seven ones followed by a BPV occurs in each of two consecutive 8-bit periods. When MCR5:BITERR = 1, single-bit violations of the one-BPV-in-eight pattern are considered irregularities by the corresponding activity monitor and increment the leaky bucket accumulator. When MCR5:AMI = 1, the detection of an AMI violation automatically invalidates the offending clock. When MCR5:LOS = 1, the detection of loss-of-signal automatically invalidates the offending clock.

In addition, register MSR4 has latched status bits that indicate the absence of the 8kHz component and the 400Hz component. In some networks the 8kHz component is removed to signal an alarm condition. If the BPVs that indicate the 8kHz component cannot be found in the incoming signal in a 500µs period (four 8kHz cycles), then MSR4:ICxNO8 is set to indicate the fact. This can cause an interrupt on the INTREQ pin if enabled by the corresponding bit in IER4. This logic is always active. If the lack of the 8kHz component is not an alarm signal in the synchronization network, then IER4:ICxNO8 can be set to 0 to disable the interrupt, and MSR4:ICxNO8 can be ignored. If the 8kHz component is not present in the signal, then the CC receiver does not forward an 8kHz clock to the input monitoring logic. The input monitoring logic then declares that input clock invalid.

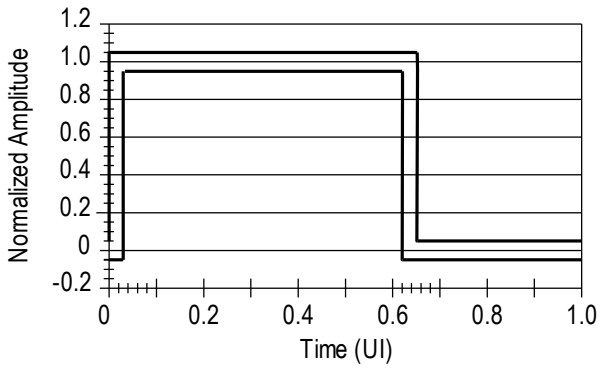
If the missing BPVs that indicate the 400Hz component cannot be found in a 5ms period (two 400Hz cycles), then MSR4:ICxNO4 is set. This can cause an interrupt on the INTREQ pin if enabled by the corresponding bit in IER4. This logic is always active. If the 400Hz component is not expected to be present in the signal, then IER4:ICxNO4 can be set to 0 to disable the interrupt, and MSR4:ICxNO4 can be ignored.

When the 8kHz component is entirely missing from the incoming signal, the AMI status bit in MSR3 is continually set, and can cause repeated interrupts if enabled. Therefore, in networks where the lack of the 8kHz component is used as an alarm signal, after MSR4:ICxNO8 is set to indicate that the 8kHz component is missing, the interrupt for MSR3:AMIx should be disabled until ICxNO8 goes low, indicating the 8kHz component is present again. Also, since the 8kHz component is the clock that is forwarded to the input clock monitor, if the 8kHz component is missing in the incoming signal, the input clock monitor automatically invalidates the clock. If the 400Hz component is missing, however, the AMI status bit is not set and the clock is not invalidated.

Table 6-12. GR-378 Composite Clock Interface Specification

PARAMETER	SPECIFICATION
Nominal Line Rate	64kHz with 8kHz bipolar violation.
Line-Rate Accuracy	Accuracy of the network clock.
Line Code	Bipolar (AMI), return-to-zero, with 5/8 duty cycle.
Medium	A shielded, balanced twisted pair.
Test Load Impedance	The resistive test load of 133Ω (±5%) shall be used at the interface for evaluation of the pulse shape and the electrical parameters.
Pulse Amplitude	The amplitude of an isolated pulse shall be between 2.7V and 5.5V.
Pulse Shape	The shape of an isolated pulse shall be rectangular with rise and fall times less than 0.5µs such that the pulse fits the shape of the mask in Figure 6-12.
Pulse Imbalance	The ratio of the amplitudes of the positive and negative pulses shall be from 0.95 to 1.05. The ratio of the widths of the positive and negative pulses shall be from 0.95 to 1.05.
DC Power	No DC power shall be applied to the interface.

Figure 6-12. GR-378 Composite Clock Pulse Mask



Time (UI)	Minimum Normalized Amplitude	Minimum Normalized Amplitude
0	-0.05	1.05
0.032	0.95	1.05
0.625	-0.05	1.05
0.657	-0.05	0.05
1	-0.05	0.05

Table 6-13. G.703 Synchronization Interfaces Specification

PARAMETER	SPECIFICATION
Pulse Shape	Nominally rectangular, with rise and fall times less than 1µs.
Transmission Media	Symmetric pair cable.
Nominal Test Load Impedance	110Ω resistive (centralized clock and appendix II Japanese signals). 120Ω resistive (contradirectional interface).
Peak Voltage of a Mark (Pulse)	1.0V ± 0.1V
Peak Voltage of a Space (No Pulse)	0V ± 0.1V
Nominal Pulse Width	7.8µs ± 0.78µs
Pulse Imbalance	The ratio of the amplitudes of the positive and negative pulses shall be from 0.95 to 1.05. The ratio of the widths of the positive and negative pulses shall be from 0.95 to 1.05.
Alarm Condition for Received Signal Amplitude	No alarm for pulse amplitudes between $0.63V_{0\text{-}P.}$ and $1.1V_{0\text{-}P}$.

6.11 Microprocessor Interfaces

The ZL81000 microprocessor interface can be configured for 8-bit parallel or SPI serial operation. During reset, the device determines its interface mode by latching the state of the IFSEL[2:0] pins into the IFSEL field of the IFCR register. Table 6-14 shows possible values of IFSEL.

Table 6-14. Microprocessor Interface Modes

IFSEL[2:0]	MODE
010	Intel bus mode (multiplexed)
011	Intel bus mode (nonmultiplexed)
100	Motorola mode (nonmultiplexed)
101	SPI mode (LSB first)
110	Motorola mode (multiplexed)
111	SPI mode (MSB first)
000, 001	{unused value}

6.11.1 Parallel Interface Modes

In the Motorola interface modes, the interface is Motorola-style with $\overline{CS}$, R/$\overline{W}$, and $\overline{DS}$ control lines. In the Intel modes, the interface is Intel-style with $\overline{CS}$, $\overline{RD}$, and $\overline{WR}$ control lines. For multiplexed bus modes, the A[8], AD[7:0], and ALE pins are wired to the corresponding pins on the microprocessor, and the falling edge of ALE latches the address on A[8] and AD[7:0]. For nonmultiplexed bus modes, the A[8:0] and AD[7:0] pins are wired to the corresponding pins on the micro, and the falling edge of ALE latches the address on A[8:0]. In nonmultiplexed bus modes, ALE is typically wired high to make the latch transparent. See Section 9.4 for AC timing details.

6.11.2 SPI Interface Mode

In the SPI modes, the device presents an SPI interface on the $\overline{CS}$, SCLK, SDI, and SDO pins. SPI is a widely used master/slave bus protocol that allows a master device and one or more slave devices to communicate over a serial bus. The ZL81000 is always a slave device. Masters are typically microprocessors, ASICs, or FPGAs. Data transfers are always initiated by the master device, which also generates the SCLK signal. The ZL81000 receives serial data on the SDI pin and transmits serial data on the SDO pin. SDO is high impedance except when the ZL81000 is transmitting data to the bus master.

Bit Order. When IFCR:IFSEL = 101, the register address and all data bytes are transmitted LSB first on both SDI and SDO. When IFSEL = 111, the register address and all data bytes are transmitted MSB first on both SDI and SDO. The Motorola SPI convention is MSB first.

Clock Polarity and Phase. The CPOL pin defines the polarity of SCLK. When CPOL = 0, SCLK is normally low and pulses high during bus transactions. When CPOL = 1, SCLK is normally high and pulses low during bus transactions. The CPHA pin sets the phase (active edge) of SCLK. When CPHA = 0, data is latched in on SDI on the leading edge of the SCLK pulse and updated on SDO on the trailing edge. When CPHA = 1, data is latched in on SDI on the trailing edge of the SCLK pulse and updated on SDO on the following leading edge. SCLK does not have to toggle between access, i.e., when $\overline{CS}$ is high. See Figure 6-13.

Device Selection. Each SPI device has its own chip-select line. To select the ZL81000, pull its $\overline{CS}$ pin low.

Control Word. After $\overline{CS}$ is pulled low, the bus master transmits the control word during the first 16 SCLK cycles. In MSB-first mode, the control word has the form:

R/$\overline{W}$ A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0 BURST

where A[13:0] is the register address, R/$\overline{W}$ is the data direction bit (1 = read, 0 = write), and BURST is the burst bit (1 = burst access, 0 = single-byte access). In LSB-first mode, the order of the 14 address bits is reversed. In the discussion that follows, a control word with R/$\overline{W}$ = 1 is a read control word, while a control word with R/$\overline{W}$ = 0 is a write control word.

Single-Byte Writes. See Figure 6-14. After $\overline{CS}$ goes low, the bus master transmits a write control word with BURST = 0 followed by the data byte to be written. The bus master then terminates the transaction by pulling $\overline{CS}$ high.

Single-Byte Reads. See Figure 6-14. After $\overline{CS}$ goes low, the bus master transmits a read control word with BURST = 0. The ZL81000 then responds with the requested data byte. The bus master then terminates the transaction by pulling $\overline{CS}$ high.

Burst Writes. See Figure 6-14. After $\overline{CS}$ goes low, the bus master transmits a write control word with BURST = 1 followed by the first data byte to be written. The ZL81000 receives the first data byte on SDI, writes it to the specified register, increments its internal address register, and prepares to receive the next data byte. If the master continues to transmit, the ZL81000 continues to write the data received and increment its address counter. After the address counter reaches 3FFFh, it rolls over to address 0000h and continues to increment.

Burst Reads. See Figure 6-14. After $\overline{CS}$ goes low, the bus master transmits a read control word with BURST = 1. The ZL81000 then responds with the requested data byte on SDO, increments its address counter, and prefetches the next data byte. If the bus master continues to demand data, the ZL81000 continues to provide the data on SDO, increment its address counter, and prefetch the following byte. After the address counter reaches 3FFFh, it rolls over to address 0000h and continues to increment.

Early Termination of Bus Transactions. The bus master can terminate SPI bus transactions at any time by pulling $\overline{CS}$ high. In response to early terminations, the ZL81000 resets its SPI interface logic and waits for the start of the next transaction. If a write transaction is terminated prior to the SCLK edge that latches the LSB of a data byte, the data byte is not written.

Design Option: Wiring SDI and SDO Together. Because communication between the bus master and the ZL81000 is half-duplex, the SDI and SDO pins can be wired together externally to reduce wire count. To support this option, the bus master must not drive the SDI/SDO line when the ZL81000 is transmitting.

AC Timing. See Table 9-11 and Figure 9-8 for AC timing specifications for the SPI interface.

Figure 6-13. SPI Clock Polarity and Phase Options

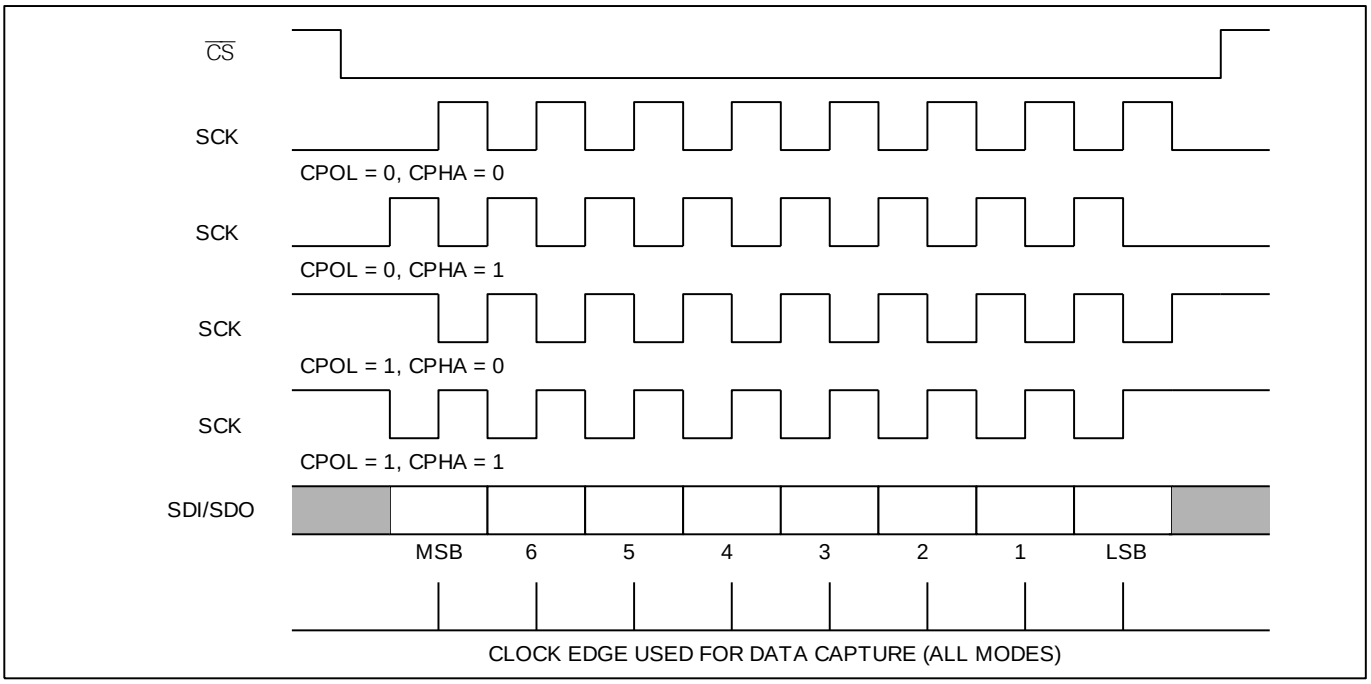
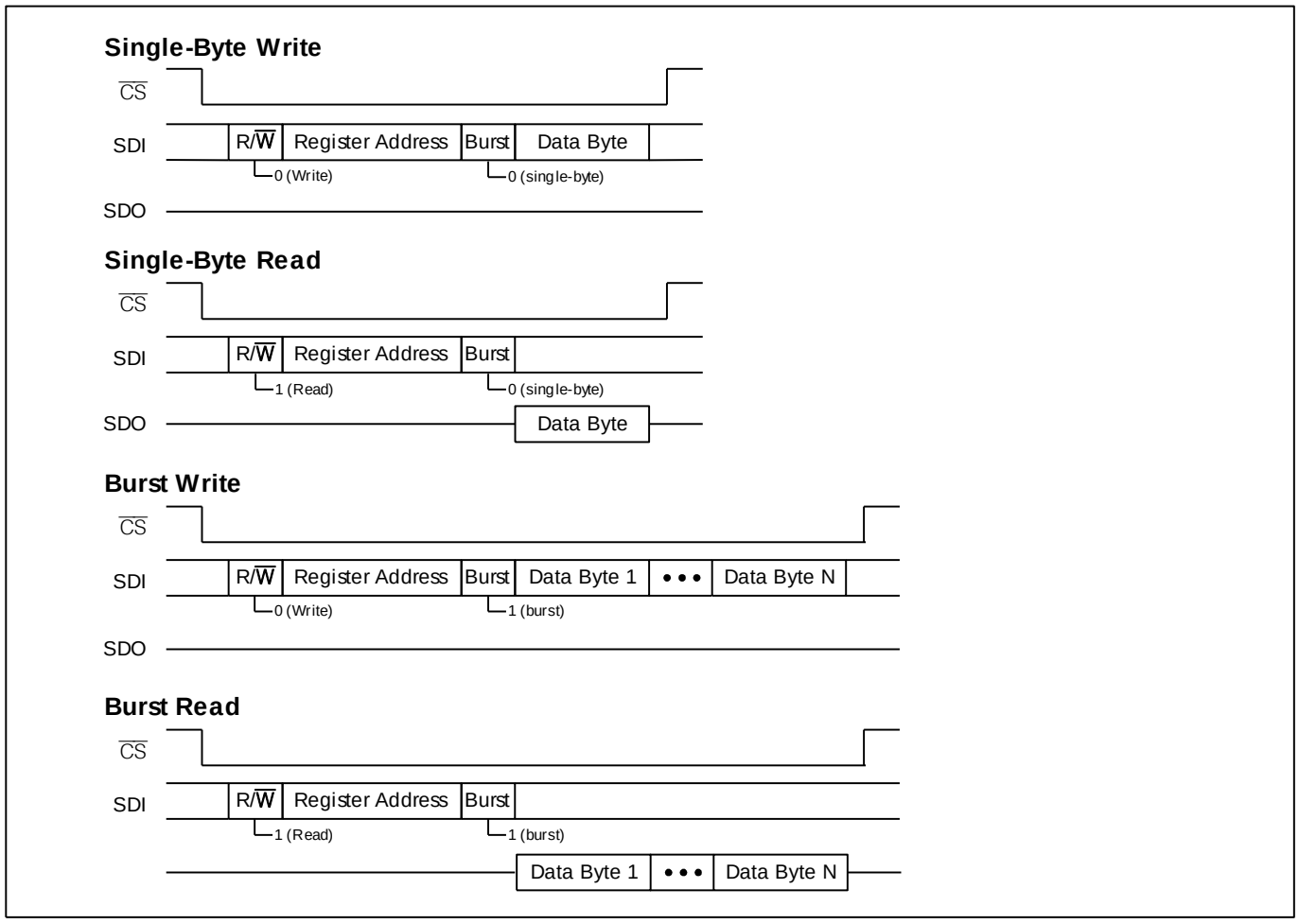


Figure 6-14. SPI Bus Transactions



6.12 Reset Logic

The device has three reset controls: the $\overline{RST}$ pin, the RST bit in MCR1, and the JTAG reset pin, $\overline{JTRST}$. The $\overline{RST}$ pin asynchronously resets the entire device, except for the JTAG logic. When the $\overline{RST}$ pin is low, all internal registers are reset to their default values, including those fields that latch their default values from, or based on, the states of input pins when the $\overline{RST}$ pin goes high (such as IFCR:IFSEL[2:0]). **The $\overline{RST}$ pin must be asserted once after power-up while the external oscillator is stabilizing.**

The MCR1:RST bit resets the entire device (except for the microprocessor interface, the JTAG logic, and the RST bit itself), but when RST is active, the register fields with pin-programmed defaults do not latch their values from, or based on, the corresponding input pins. Instead, these fields are reset to the default values that were latched when the $\overline{RST}$ pin was last active.

Systems should hold $\overline{RST}$ low while the external oscillator starts up and stabilizes. Some OCXOs take 250ms or more to start up and stabilize their output signals to valid logic levels and pulse widths. An incorrect reset condition could result if $\overline{RST}$ is released before the oscillator has started up completely.

Important: System software must wait at least 100µs after reset ($\overline{RST}$ pin or RST bit) is deasserted before initializing the device as described in Section 6.14.

6.13 Power-Supply Considerations

Due to the dual-power-supply nature of the ZL81000, some I/Os have parasitic diodes between a 1.8V supply and a 3.3V supply. When ramping power supplies up or down, care must be taken to avoid forward-biasing these diodes because it could cause latchup. Two methods are available to prevent this. The first method is to place a Schottky diode external to the device between the 1.8V supply and the 3.3V supply to force the 3.3V supply to be less than one parasitic diode drop below the 1.8V supply. The second method is to ramp up the 3.3V supply first and then ramp up the 1.8V supply.

6.14 Initialization

After power-up or reset, a series of writes must be done to the ZL81000 to tune it for optimal performance. This series of writes is called the initialization script. Each die revision of the ZL81000 has a different initialization script. For the latest initialization scripts contact Microsemi timing products technical support.

Note that following bits have reset-default values that must be changed during initialization for proper device operation: MCR10 bit 7 and MCR11 bit 4.

7. REGISTER DESCRIPTIONS

The top-level memory map is shown in Table 7-1.

Table 7-1. Top-Level Memory Map

ADDRESS RANGE	FUNCTIONAL BLOCK
0000–007Fh	IC1-IC4, DPLL, OC9
0080–00FFh	BITS Transceiver 1 (BITS1)
0100–017Fh	BITS Transceiver 2 (BITS2)
0180–01FFh	Reserved

Note: Systems must be able to access the entire address range from 0 to 01FFh. Proper device initialization requires a sequence of writes to addresses in the range 0180-01FFh.

Table 7-2 in Section 7.4 shows the register map for the core timing block, while Table 7-3 in Section 7.5 shows the register map for the BITS transceivers. In each register, bit 7 is the MSB and bit 0 is the LSB. Register addresses not listed and bits marked "—" are reserved and must be written with 0. Writing other values to these registers may put the device in a factory test mode, resulting in undefined operation. Bits labeled "0" or "1" must be written with that value for proper operation. Register fields with underlined names are read-only fields; writes to these fields have no effect. All other fields are read-write. Register fields are described in detail in the register descriptions that follow Table 7-2.

7.1 Status Bits

The device has two types of status bits. Real-time status bits are read-only and indicate the state of a signal at the time it is read. Latched status bits are set when a signal changes state (low-to-high, high-to-low, or both, depending on the bit) and cleared when written with a logic 1 value. Writing a 0 has no effect. When set, some latched status bits can cause an interrupt request on the INTREQ pin if enabled to do so by corresponding interrupt enable bits.

7.2 Configuration Fields

Configuration fields are read-write. During reset, each configuration field reverts to the default value shown in the register definition. Configuration register bits marked "—" are reserved and must be written with 0.

7.3 Multiregister Fields

Multiregister fields—such as FREQ[18:0] in registers FREQ1, FREQ2, and FREQ3—must be handled carefully to ensure that the bytes of the field remain consistent. A write access to a multiregister field is accomplished by writing all the registers of the field in any order, with no other accesses to the device in between. If the write sequence is interrupted by another access, none of the bytes are written and the MSR4:MRAA bit is set to indicate the write was aborted. A read access from a multiregister field is accomplished by reading the registers of the field in any order, with no other accesses to the device in between. When one register of a multiregister field is read, the other register(s) in the field are frozen until after they are all read. If the read sequence is interrupted by another access, the registers of the multibyte field are unfrozen and the MSR4:MRAA bit is set to indicate the read was aborted. For best results, interrupt servicing should be disabled in the microprocessor before a multiregister access and then enabled again after the access is complete. The multiregister fields are:

FIELD	REGISTERS	ADDRESSES	TYPE
FREQ[18:0]	FREQ1, FREQ2, FREQ3	07, 0C, 0D	read-only
MCLKFREQ[15:0]	MCLK1, MCLK2	3C, 3D	read/write
DIVN[14:0]	DIVN1, DIVN2	46, 47	read/write
PHASE[15:0]	PHASE1, PHASE2	77, 78	read-only

7.4 IC1-IC4, DPLL and OC9 Register Definitions

Table 7-2. IC1-IC4, DPLL and OC9 Register Map

Note: *Register names are hyperlinks to register definitions. Underlined fields are read-only.*

ADDR	REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
00h	ID1	ID[7:0]							
01	ID2	ID[15:8]							
02	REV	REV[7:0]							
03	TEST1	—	—	—	—	0	8KPOL	0	0
05	MSR1	—	—	—	—	IC4	IC3	IC2	IC1
07	FREQ3	—	—	—	—	—	FREQ[18:16]		
08	MSR3	—	T4LOCK	—	T4NOIN	AMI2	LOS2	AMI1	LOS1
09	OPSTATE	—	T4LOCK	—	T4SOFT	—	—	—	—
0A	PTAB1	REF1[3:0]				SELREF[3:0]			
0B	PTAB2	REF3[3:0]				REF2[3:0]			
0C	FREQ1	FREQ[7:0]							
0D	FREQ2	FREQ[15:8]							
0E	VALSR1	—	—	—	—	IC4	IC3	IC2	IC1
10	ISR1	SOFT2	HARD2	ACT2	—	SOFT1	HARD1	ACT1	—
11	ISR2	SOFT4	HARD4	ACT4	—	SOFT3	HARD3	ACT3	—
17	MSR4	—	—	MRAA	—	IC2NO4	IC1NO4	IC2NO8	IC1NO8
18	IPR1	PRI2[3:0]				PRI1[3:0]			
19	IPR2	PRI4[3:0]				PRI3[3:0]			
20	ICR1	DIVN	LOCK8K	BUCKET[1:0]		FREQ[3:0]			
21	ICR2	DIVN	LOCK8K	BUCKET[1:0]		FREQ[3:0]			
22	ICR3	DIVN	LOCK8K	BUCKET[1:0]		FREQ[3:0]			
23	ICR4	DIVN	LOCK8K	BUCKET[1:0]		FREQ[3:0]			
30	VALCR1	—	—	—	—	IC4	IC3	IC2	IC1
32	MCR1	RST	—	—	—	—	—	—	—
34	MCR3	—	—	XOEDGE	—	—	SONSDH	MASTSLV	—
36	MCR5	CCEDGE	BITERR	AMI	LOS	—	—	—	—
37	IFSR	—	—	—	—	—	IFSEL[2:0]		
3C	MCLK1	MCLKFREQ[7:0]							
3D	MCLK2	MCLKFREQ[15:8]							
43	IER1	—	—	—	—	IC4	IC3	IC2	IC1
45	IER3	—	T4LOCK	—	T4NOIN	AMI2	LOS2	AMI1	LOS1
46	DIVN1	DIVN[7:0]							
47	DIVN2	—	DIVN[14:8]						
48	MCR10	FMONCLK	—	—	—	—	—	SOFTEN	HARDEN
49	ILIMIT	SOFT[3:0]				HARD[3:0]			
4B	MCR11	—	—	—	T4	FMEASIN[3:0]			
4C	FMEAS	FMEAS[7:0]							
4D	DLIMIT3	FLLOL	SOFTLIM[6:0]						
4E	IER4	—	—	—	—	IC2NO4	IC1NO4	IC2NO8	IC1NO8
50	LB0U	LB0U[7:0]							
51	LB0L	LB0L[7:0]							
52	LB0S	LB0S[7:0]							
53	LB0D	—	—	—	—	—	—	LB0D[1:0]	
54	LB1U	LB1U[7:0]							
55	LB1L	LB1L[7:0]							
56	LB1S	LB1S[7:0]							
57	LB1D	—	—	—	—	—	—	LB1D[1:0]	
58	LB2U	LB2U[7:0]							

ADDR	REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
59	LB2L	LB2L[7:0]							
5A	LB2S	LB2S[7:0]							
5B	LB2D	—	—	—	—	—	—	LB2D[1:0]	
5C	LB3U	LB3U[7:0]							
5D	LB3L	LB3L[7:0]							
5E	LB3S	LB3S[7:0]							
5F	LB3D	—	—	—	—	—	—	LB3D[1:0]	
63	OCR4	—	—	OC9EN	—	—	—	—	—
64	T4CR1	—	ASQUEL	—	OC9SON	T4FREQ[3:0]			
66	T4BW	—	—	—	—	—	—	T4BW[1:0]	
6A	T4CR2	—	—	—	—	—	DAMP[2:0]		
6E	GPCR	GPIO4D	GPIO3D	GPIO2D	GPIO1D	GPIO4O	GPIO3O	GPIO2O	GPIO1O
6F	GPSR	—	—	—	—	GPIO4	GPIO3	GPIO2	GPIO1
73	PHLIM1	FLEN	NALOL	1	—	—	FINELIM[2:0]		
74	PHLIM2	CLEN	MCPDEN	USEMCPD	—	COARSELIM[3:0]			
77	PHASE1	PHASE[7:0]							
78	PHASE2	PHASE[15:8]							
7D	INTCR	—	—	—	—	—	GPO	OD	POL
7E	PROT	PROT[7:0]							
7F	IFCR	—	—	—	—	—	IFSEL[2:0]		

IC, DPLL and OC Register Map Color Coding

	Device Identification and Protection
	Local Oscillator and Master Clock Configuration
	Input Clock Configuration
	Input Clock Monitoring
	Input Clock Selection
	DPLL Configuration
	DPLL State
	Output Clock Configuration
	Microprocessor Interface Configuration

Register Name: ID1
Register Description: Device Identification Register, LSB
Register Address: 00h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	ID[7:0]							
Default	0	0	0	1	1	1	0	0

Bits 7 to 0: Device ID (ID[7:0]). ID[15:0] = 8C1Ch.

Register Name: ID2
Register Description: Device Identification Register, MSB
Register Address: 01h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	ID[15:8]							
Default	1	0	0	0	1	1	0	0

Bits 7 to 0: Device ID (ID[15:8]). See the ID1 register description.

Register Name: REV
Register Description: Device Revision Register
Register Address: 02h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	REV[7:0]							
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: Device Revision (REV[7:0]). Contact the factory to interpret this value and determine the latest revision.

Register Name: TEST1
Register Description: Test Register 1 (Not Normally Used)
Register Address: 03h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	—	—	—	0	8KPOL	0	0
Default	0	0	0	1	0	1	0	0

Bit 3: Leave set to zero (test control).

Bit 2: 8kHz Edge Polarity (8KPOL). Specifies the input clock edge to lock to on the selected reference when it is configured for LOCK8K mode. See Section 6.4.2.

0 = Falling edge
1 = Rising edge

Bit 1: Leave set to zero (test control).

Bit 0: Leave set to zero (test control).

Register Name: MSR1
Register Description: Master Status Register 1
Register Address: 05h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	—	—	—	IC4	IC3	IC2	IC1
Default	1	1	1	1	1	1	1	1

Bits 3 to 0: Input Clock Status Change (IC4 to IC1). Each of these latched status bits is set to 1 when the corresponding VALSR1 status bit changes state (set or cleared). If soft frequency limit alarms are enabled (MCR10:SOFTEN = 1), then each of these latched status bits is also set to 1 when the corresponding SOFT bit in the ISR registers changes state (set or cleared). Each bit is cleared when written with a 1 and not set again until either the VALSR1 bit or the SOFT bit changes state again. When one of these latched status bits is set it can cause an interrupt request on the INTREQ pin if the corresponding interrupt enable bit is set in the IER1 register. See Section 6.5 for input clock validation/invalidation criteria.

Register Name: FREQ3
Register Description: Frequency Register 3
Register Address: 07h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	—	—	—	—	FREQ[18:16]		
Default	0	0	0	0	0	0	0	0

Bits 2 to 0: Current DPLL Frequency (FREQ[18:16]). See the FREQ1 register description.

Register Name: MSR3
Register Description: Master Status Register 3
Register Address: 08h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	T4LOCK	—	T4NOIN	AMI2	LOS2	AMI1	LOS1
Default	0	1	0	1	0	0	0	0

Bit 6: DPLL Lock Status Change (T4LOCK). This latched status bit is set to 1 when the lock status of the DPLL (OPSTATE:T4LOCK) changes (becomes locked when previously unlocked or becomes unlocked when previously locked). T4LOCK is cleared when written with a 1 and not set again until the DPLL lock status changes again. When T4LOCK is set it can cause an interrupt request on the INTREQ pin if the T4LOCK interrupt enable bit is set in the IER3 register. See Section 6.7.5.

Bit 4: DPLL No Valid Inputs Alarm (T4NOIN). This latched status bit is set to 1 when the DPLL has no valid inputs available. T4NOIN is cleared when written with a 1 unless the DPLL still has no valid inputs available. When T4NOIN is set it can cause an interrupt request on the INTREQ pin if the T4NOIN interrupt enable bit is set in the IER3 register. See Section 6.5.

Bit 3: AMI Violation on IC2A (AMI2). This latched status bit is set to 1 when a deviation from the expected pattern of seven ones followed by a BPV occurs on the IC2A input in each of two consecutive 8-bit periods. However, if the composite clock receiver can detect the presence of the 400 Hz component required by G.703 Appendix II.1 option b), then the missing BPVs that indicate the 400 Hz component are not considered AMI violations. AMI2 is cleared when written with a 1 and not set again until another AMI violation occurs. When AMI2 is set it can cause an interrupt request on the INTREQ pin if the AMI2 interrupt enable bit is set in the IER3 register. See Section 6.10.1.

Bit 2: LOS Error on IC2A (LOS2). This latched status bit is set to 1 when no pulses are detected on the IC2A input in a 32µs period (i.e., after two missing pulses). LOS2 is cleared when written with a 1 and is not set again until IC2A transitions from valid signal to loss-of-signal again. When LOS2 is set it can cause an interrupt request on the INTREQ pin if the LOS2 interrupt enable bit is set in the IER3 register. See Section 6.10.1.

Bit 1: AMI Violation on IC1A (AMI1). This latched status bit is set to 1 when a deviation from the expected pattern of seven ones followed by a BPV occurs on the IC1A input in each of two consecutive 8-bit periods. However, if the composite clock receiver can detect the presence of the 400Hz component required by G.703 Appendix II.1 option b), then the missing BPVs that indicate the 400Hz component are not considered AMI violations. AMI1 is cleared when written with a 1 and not set again until another AMI violation occurs. When AMI1 is set it can cause an interrupt request on the INTREQ pin if the AMI1 interrupt enable bit is set in the IER3 register. See Section 6.10.1.

Bit 0: LOS Error on IC1A (LOS1). This latched status bit is set to 1 when no pulses are detected on the IC1A input in a 32 µs period (i.e., after two missing pulses). LOS1 is cleared when written with a 1 and is not set again until IC1A transitions from valid signal to loss-of-signal again. When LOS1 is set it can cause an interrupt request on the INTREQ pin if the LOS1 interrupt enable bit is set in the IER3 register. See Section 6.10.1.

Register Name: OPSTATE
Register Description: Operating State Register
Register Address: 09h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	T4LOCK	—	T4SOFT	—	—	—	—
Default	0	1	0	0	0	0	0	1

Bit 6: DPLL Lock Status (T4LOCK). This real-time status bit indicates the current phase lock status of the DPLL. See Sections 6.5.3 and 6.7.5.

0 = not locked to selected reference
1 = locked to selected reference

Bit 4: DPLL Frequency Soft Alarm (T4SOFT). This real-time status bit indicates whether or not the DPLL is tracking its reference within the soft alarm limits specified in the SOFT[6:0] field of the DLIMIT3 register. See Section 6.7.5.

0 = No alarm; frequency is within the soft alarm limits
1 = Soft alarm; frequency is outside the soft alarm limits

Register Name: PTAB1
Register Description: Priority Table Register 1
Register Address: 0Ah

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	REF1[3:0]				SELREF[3:0]			
Default	0	0	0	0	0	0	0	0

Bits 7 to 4: Highest Priority Valid Reference (REF1[3:0]). This real-time status field indicates the highest-priority valid input reference. Note that an input reference cannot be indicated in this field if it has been marked invalid in the VALCR1 egister. See Section 6.6.2.

0000 = No valid input reference available
0001 = Input IC1
0010 = Input IC2
0011 = Input IC3
0100 = Input IC4
0101-1111 = {unused value}

Bits 3 to 0: Selected Reference (SELREF[3:0]). This real-time status field indicates the current selected reference. Note that an input clock cannot be indicated in this field if it has been marked invalid in the VALCR1 register. See Section 6.6.2.

0000 = No valid input reference available
0001 = Input IC1
0010 = Input IC2
0011 = Input IC3
0100 = Input IC4
0101-1111 = {unused value}

Register Name: PTAB2
Register Description: Priority Table Register 2
Register Address: 0Bh

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	REF3[3:0]				REF2[3:0]			
Default	0	0	0	0	0	0	0	0

Bits 7 to 4: Third Highest Priority Valid Reference (REF3[3:0]). This real-time status field indicates the third highest priority validated input reference. Note that an input reference cannot be indicated in this field if it has been marked invalid in the VALCR1 register. See Section 6.6.2.

0000 = No valid input reference available
0001 = Input IC1
0010 = Input IC2
0011 = Input IC3
0100 = Input IC4
0101-1111 = {unused value}

Bits 3 to 0: Second Highest Priority Valid Reference (REF2[3:0]). This real-time status field indicates the second highest priority validated input reference. Note that an input reference cannot be indicated in this field if it has been marked invalid in the VALCR1 register. See Section 6.6.2.

0000 = No valid input reference available
0001 = Input IC1
0010 = Input IC2
0011 = Input IC3
0100 = Input IC4
0101-1111 = {unused value}

Register Name: FREQ1
Register Description: Frequency Register 1
Register Address: 0Ch

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	FREQ[7:0]							
Default	0	0	0	0	0	0	0	0

The FREQ1, FREQ2 and FREQ3 registers must be read consecutively. See Section 7.3.

Bits 7 to 0: Current DPLL Frequency (FREQ[7:0]). The full 19-bit FREQ[18:0] field spans this register, FREQ2 and FREQ3. FREQ is a two's-complement signed integer that expresses the current frequency as an offset with respect to the master clock frequency (see Section 6.3). Because the value in this register field is derived from the DPLL integral path, it can be considered an average frequency with a rate of change inversely proportional to the DPLL bandwidth. The frequency offset in ppm is equal to FREQ[18:0] x 0.0003068..

Register Name: FREQ2
Register Description: Frequency Register 2
Register Address: 0Dh

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	FREQ[15:8]							
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: Current DPLL Frequency (FREQ[15:8]). See the FREQ1 register description.

Register Name: VALSR1
Register Description: Input Clock Valid Status Register 1
Register Address: 0Eh

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	—	—	—	IC4	IC3	IC2	IC1
Default	0	0	0	0	0	0	0	0

Bits 3 to 0: Input Clock Valid Status (IC4 to IC1). Each of these real-time status bits is set to 1 when the corresponding input clock is valid. An input is valid if it has no active alarms (HARD = 0, ACT = 0 in the corresponding ISR register). See also the MSR1 register and Section 6.5.

0 = Invalid
1 = Valid

Register Name: ISR1
Register Description: Input Status Register 1
Register Address: 10h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	SOFT2	HARD2	ACT2	—	SOFT1	HARD1	ACT1	—
Default	0	1	1	0	0	1	1	0

Bit 7: Soft Frequency Limit Alarm for Input Clock 2 (SOFT2). This real-time status bit indicates a soft frequency limit alarm for input clock 2. SOFT2 is set to 1 when the frequency of IC2A is greater than or equal to the soft limit set in the ILIMIT register. Soft alarms are disabled by default but can be enabled by setting SOFTEN = 1 in the MCR10 register. A soft alarm does not invalidate an input clock. See Section 6.5.1.

Bit 6: Hard Frequency Limit Alarm for Input Clock 2 (HARD2). This real-time status bit indicates a hard frequency limit alarm for input clock 2. HARD2 is set to 1 when the frequency of IC2A is greater than or equal to the hard limit set in the ILIMIT register. Hard alarms are enabled by default but can be disabled by setting HARDEN = 0 in the MCR10 register. A hard alarm clears the IC2 status bit in the VALSR1 register, invalidating the IC2A clock. See Section 6.5.1.

Bit 5: Activity Alarm for Input Clock 2 (ACT2). This real-time status bit is set to 1 when the leaky bucket accumulator for IC2A reaches the alarm threshold specified in the LBxU register (where 'x' in 'LBxU' is specified in the BUCKET field of ICR2). An activity alarm clears the IC2 status bit in the VALSR1 register, invalidating the IC2A clock. See Section 6.5.2.

Bit 3: Soft Frequency Limit Alarm for Input Clock 1 (SOFT1). This bit has the same behavior as the SOFT2 bit but for the IC1A input clock.

Bit 2: Hard Frequency Limit Alarm for Input Clock 1 (HARD1). This bit has the same behavior as the HARD2 bit but for the IC1A input clock.

Bit 1: Activity Alarm for Input Clock 1 (ACT1). This bit has the same behavior as the ACT2 bit but for the IC1A input clock.

Register Name: ISR2
Register Description: Input Status Register 2
Register Address: 11h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	SOFT4	HARD4	ACT4	—	SOFT3	HARD3	ACT3	—
Default	0	1	1	0	0	1	1	0

This register has the same behavior as ISR1 but for the IC3 and IC4 input clocks.

Register Name: MSR4
Register Description: Master Status Register 4
Register Address: 17h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	—	MRAA	—	IC2NO4	IC1NO4	IC2NO8	IC1NO8
Default	0	0	0	0	0	0	0	0

Bit 5: Multi-Register Access Aborted (MRAA). This latched status bit is set to 1 when a multi-byte access (read or write) is interrupted by another access to the device. MRAA is cleared when written with a 1. MRAA cannot cause an interrupt to occur. See Section 7.3.

Bit 3: Input Clock 2 Has No 400Hz Component (IC2NO4). This latched status bit is set to 1 when the missing BPVs that indicate the 400Hz component cannot be found in a 5ms period (two 400Hz cycles). IC2NO4 is cleared when written with a 1 unless the 400Hz component is still not present. When IC2NO4 is set it can cause an interrupt request on the INTREQ pin if the IC2NO4 interrupt enable bit is set in the IER4 register. See Section 6.10.1.

Bit 2: Input Clock 1 Has No 400Hz Component (IC1NO4). This latched status bit is set to 1 when the missing BPVs that indicate the 400Hz component cannot be found in a 5ms period (two 400Hz cycles). IC1NO4 is cleared when written with a 1 unless the 400Hz component is still not present. When IC1NO4 is set it can cause an interrupt request on the INTREQ pin if the IC1NO4 interrupt enable bit is set in the IER4 register. See Section 6.10.1.

Bit 1: Input Clock 2 Has No 8kHz Component (IC2NO8). This latched status bit is set to 1 when the BPVs that indicate the 8kHz component cannot be found in the incoming signal in a 500µs period (four 8kHz cycles). IC2NO8 is cleared when written with a 1 unless the 8kHz component is still not present. When IC2NO8 is set it can cause an interrupt request on the INTREQ pin if the IC2NO8 interrupt enable bit is set in the IER4 register. See Section 6.10.1.

Bit 0: Input Clock 1 Has No 8kHz Component (IC1NO8). This latched status bit is set to 1 when the BPVs that indicate the 8kHz component cannot be found in the incoming signal in a 500µs period (four 8kHz cycles). IC1NO8 is cleared when written with a 1 unless the 8kHz component is still not present. When IC1NO8 is set it can cause an interrupt request on the INTREQ pin if the IC1NO8 interrupt enable bit is set in the IER4 register. See Section 6.10.1.

Register Name: IPR1
Register Description: Input Priority Register 1
Register Address: 18h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	PRI2[3:0]				PRI1[3:0]			
Default	0	0	0	0	0	0	0	0

Bits 7 to 4: Priority for Input Clock 2 (PRI2). Priority 0001 is highest; priority 1111 is lowest. See Section 6.6.1.
0000 = IC2A unavailable for selection.
0001–1111= IC2A relative priority

Bits 3 to 0: Priority for Input Clock 1 (PRI1). Priority 0001 is highest; priority 1111 is lowest. See Section 6.6.1.
0000 = IC1A unavailable for selection.
0001–1111 = IC1A relative priority

Register Name: IPR2
Register Description: Input Priority Register 2
Register Address: 19h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	PRI4[3:0]				PRI3[3:0]			
Default	0	0	0	0	0	0	0	0

This register has the same behavior as IPR1 but for the IC3 and IC4 input clocks.

Register Name: ICR1, ICR2, ICR3, ICR4
Register Description: Input Configuration Register 1, 2, 3, 4
Register Address: 20h, 21h, 22h, 23h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	DIVN	LOCK8K	BUCKET[1:0]		FREQ[3:0]			
Default	0	0	0	0	0	0	0	0

These registers are identical in function. ICRx is the control register for input clock ICx.

Bit 7: DIVN Mode (DIVN). When DIVN is set to 1, the input clock is divided down by a programmable pre-divider. The resulting output clock is then passed to the DPLL and frequency monitor. All input clocks for which DIVN = 1 are divided by the factor specified in DIVN1 and DIVN2. When DIVN = 1 in an ICR register, the FREQ field of that register must be set to 8kHz. See Section 6.4.2.3.

0 = Disabled
1 = Enabled

Bit 6: LOCK8K Mode (LOCK8K). When LOCK8K is set to 1, the input clock is divided down by a preset predivider. The resulting output clock, which is always 8kHz, is then passed to the DPLL. LOCK8K is ignored when DIVN = 1. LOCK8K is also ignored when DIVN=0 and FREQ[3:0] = 1001 (2kHz) or 1010 (4kHz). See Section 6.4.2.2.

0 = Disabled
1 = Enabled

Bits 5 to 4: Leaky Bucket Configuration (BUCKET[1:0]). Each input clock has leaky bucket accumulator logic in its activity monitor. The LBxy registers at addresses 50h to 5Fh specify four different leaky bucket configurations. Any of the four configurations can be specified for the input clock. See Section 6.5.2.

00 = leaky bucket configuration 0
01 = leaky bucket configuration 1
10 = leaky bucket configuration 2
11 = leaky bucket configuration 3

Bits 3 to 0: Input Clock Nominal Frequency (FREQ[3:0]). This field specifies the input clock's nominal frequency. FREQ must be set to 0000 if DIVN = 1. See Section 6.4.2.

0000 = 8kHz
0001 = 1544kHz or 2048kHz (as determined by SONSDH bit in the MCR3 register)
0010 = 6.48MHz
0011 = 19.44MHz
0100 = 25.92MHz
0101 = 38.88MHz
0110 = 51.84MHz
0111 = 77.76MHz
1000 = {unused value}
1001 = 2kHz
1010 = 4kHz
1011 = 6312kHz
1100–1111 {unused values}

Register Name: VALCR1
Register Description: Input Clock Valid Control Register 1
Register Address: 30h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	—	—	—	IC4	IC3	IC2	IC1
Default	1	1	1	1	1	1	1	1

Bits 3 to 0: Input Clock Valid Control (IC4 to IC1). These control bits can be used to force input clocks to be considered invalid. If a clock is invalidated by one of these control bits it will not appear in the priority table in the PTAB1 and PTAB2 registers, even if the clock is otherwise valid. Note that setting a VALCR bit low has no effect on the corresponding bit in the VALSR registers. See Sections 6.6.2.

0 = Force invalid
1 = Do not force invalid; determine validity normally

Register Name: MCR1
Register Description: Master Configuration Register 1
Register Address: 32h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	RST	—	—	—	—	—	—	—
Default	0	0	0	0	0	0	0	0

Bit 7: Device Reset (RST). When this bit is high the entire device is held in reset, and all register fields, except the RST bit itself, are reset to their default states. When RST is active, the register fields with pin-programmed defaults do not latch their values from the corresponding input pins. Instead these fields are reset to the default values that were latched from the pins when the $\overline{\text{RST}}$ pin was last active. See Section 6.12.

0 = Normal operation
1 = Reset

Register Name: MCR3
Register Description: Master Configuration Register 3
Register Address: 34h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	—	XOEDGE	—	—	SONSDH	MASTSLV	—
Default	1	1	0	0	0	see below	see below	0

Bit 5: Local Oscillator Edge (XOEDGE). This bit specifies the significant clock edge of the local oscillator clock signal on the REFCLK input pin. The faster edge should be selected for best jitter performance. See Section 6.3.

0 = Rising edge
1 = Falling edge

Bit 2: SONET or SDH Frequencies (SONSDH). This bit specifies the clock rate for input clocks with FREQ=0001 in the ICR registers. During reset the default value of this bit is latched from the SONSDH pin. See Section 6.4.2.

0 = 2048kHz
1 = 1544 Hz

Bit 1: MASTSLV. This read-only bit indicates the state of the MASTSLV pin. This bit therefore does not have a fixed default value. This bit and the MASTSLV pin have no function in ZL81000.

Register Name: MCR5
Register Description: Master Configuration Register 5
Register Address: 36h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	CCEDGE	BITERR	AMI	LOS	—	—	—	—
Default	0	0	0	0	0	0	1	0

Bit 7: Composite Clock 8kHz Edge (CCEDGE). This bit specifies the 8kHz clock edge in the incoming composite clock signals on inputs IC1A and IC2A. See Section 6.10.1.

0 = The leading edge of the pulse following the BPV
1 = The leading edge of the BPV

Bit 6: Increment the Activity Monitor on Bit Errors (BITERR). If this bit is set to 1, then the detection of a deviation from the one-BPV-in-eight pattern on IC1A or IC2A is considered an irregularity by the corresponding activity monitor. The activity monitors increment their leaky bucket accumulators once for each 128ms interval in which irregularities occur. See Section 6.10.1.

0 = Bit errors do not increment the input clock activity monitors
1 = Bit errors do increment the input clock activity monitors

Bit 5: Invalidate on AMI Violation (AMI). If this bit is set to 1, then the detection of a deviation from the one-BPV-in-eight pattern in each of two consecutive 8-bit periods on IC1A or IC2A automatically invalidates the offending clock. See Section 6.10.1.

0 = Do not invalidate on AMI violation
1 = Invalidate on incorrect AMI violation

Bit 4: Invalidate on Loss of Signal (LOS). If this bit is set to 1, then the detection of two consecutive zeros on IC1A or IC2A automatically invalidates the offending clock. See Section 6.10.1.

0 = Do not invalidate on LOS
1 = Invalidate on LOS

Register Name: IFSR
Register Description: Microprocessor Interface Selection Status Register
Register Address: 37h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	—	—	—	—	IFSEL[2:0]		
Default	0	0	0	0	0	set by IFSEL[2:0] pins when $\overline{RST}$ = 0		

Bits 2 to 0: Microprocessor Interface Selection (IFSEL[2:0]). This read-only field shows the current state of the IFSEL[2:0] pins. When $\overline{RST}$ = 0 the state of the IFSEL pins is latched into the microprocessor interface control register (IFCR). After $\overline{RST}$ is brought high, the IFSEL pins are ignored by the interface control logic and can be used as general-purpose inputs whose values are shown in this register field. See Section 6.11.

Register Name: MCLK1
Register Description: Master Clock Frequency Adjustment Register 1
Register Address: 3Ch

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	MCLKFREQ[7:0]							
Default	1	0	0	1	1	0	0	1

The MCLK1 and MCLK2 registers must be read consecutively and written consecutively. See Section 7.3.

Bits 7 to 0: Master Clock Frequency Adjustment (MCLKFREQ[7:0]). The full 16-bit MCLKFREQ[15:0] field spans this register and MCLK2. MCLKFREQ is an unsigned integer that adjusts the frequency of the internal 204.8MHz master clock with respect to the frequency of the local oscillator clock on the REFCLK pin by up to +514ppm and -771ppm. The master clock adjustment has the effect of speeding up the master clock with a positive adjustment and slowing it down with a negative adjustment. For example, if the oscillator connected to REFCLK has an offset of +1ppm then the adjustment should be -1ppm to correct the offset.

The formulas below translate adjustments to register values and vice versa. The default register value of 39,321 corresponds to 0ppm. See Section 6.3.

MCLKFREQ[15:0] = adjustment_in_ppm / 0.0196229 + 39,321

adjustment_in_ppm = (MCLKFREQ[15:0] - 39,321) x 0.0196229

Register Name: MCLK2
Register Description: Master Clock Frequency Adjustment Register 2
Register Address: 3Dh

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	MLCKFREQ[15:8]							
Default	1	0	0	1	1	0	0	1

Bits 7 to 0: Master Clock Frequency Adjustment (MCLKFREQ[15:8]). See the MCLK1 register description.

Register Name: IER1
Register Description: Interrupt Enable Register 1
Register Address: 43h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	—	—	—	IC4	IC3	IC2	IC1
Default	0	0	0	0	0	0	0	0

Bits 3 to 0: Interrupt Enable for Input Clock Status Change (IC4 to IC1). Each of these bits is an interrupt enable control for the corresponding bit in the MSR1 register.

0 = Mask the interrupt
1 = Enable the interrupt

Register Name: IER3
Register Description: Interrupt Enable Register 3
Register Address: 45h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	T4LOCK	—	T4NOIN	AMI2	LOS2	AMI1	LOS1
Default	0	0	0	0	0	0	0	0

Bit 6: Interrupt Enable for DPLL Lock Status Change (T4LOCK). This bit is an interrupt enable for the T4LOCK bit in the MSR3 register.

0 = Mask the interrupt
1 = Enable the interrupt

Bit 4: Interrupt Enable for DPLL No Valid Inputs Alarm (T4NOIN). This bit is an interrupt enable for the T4NOIN bit in the MSR3 register.

0 = Mask the interrupt
1 = Enable the interrupt

Bit 3: Interrupt Enable for AMI Violation on IC2A (AMI2). This bit is an interrupt enable for the AMI2 bit in the MSR3 register.

0 = Mask the interrupt
1 = Enable the interrupt

Bit 2: Interrupt Enable for LOS Error on IC2A (LOS2). This bit is an interrupt enable for the LOS2 bit in the MSR3 register.

0 = Mask the interrupt
1 = Enable the interrupt

Bit 1: Interrupt Enable for AMI Violation on IC1A (AMI1). This bit is an interrupt enable for the AMI1 bit in the MSR3 register.

0 = Mask the interrupt
1 = Enable the interrupt

Bit 0: Interrupt Enable for LOS Error on IC1A (LOS1). This bit is an interrupt enable for the LOS1 bit in the MSR3 register.

0 = Mask the interrupt
1 = Enable the interrupt

Register Name: DIVN1
Register Description: DIVN Register 1
Register Address: 46h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	DIVN[7:0]							
Default	1	1	1	1	1	1	1	1

The DIVN1 and DIVN2 registers must be read consecutively and written consecutively. See Section 7.3.

Bits 7 to 0: DIVN Factor (DIVN[7:0]). The full 15-bit DIVN[14:0] field spans this register and DIVN2. This field contains the integer value used to divide the frequency of input clocks that are configured for DIVN mode (DIVN = 1 in registers ICR1 through ICR4). The frequency is divided by DIVN[14:0] + 1.

DIVN mode supports a maximum input frequency of 125MHz; therefore, the maximum value of DIVN[14:0] is 15,624 (i.e., 125MHz / 8kHz - 1). Performance with DIVN values greater than 15,624 is undefined. See Section 6.4.2.3.

Register Name: DIVN2
Register Description: DIVN Register 2
Register Address: 47h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	DIVN[14:8]						
Default	0	0	1	1	1	1	1	1

Bits 6 to 0: DIVN Factor (DIVN [14:8]). See the DIVN1 register description.

Register Name: MCR10
Register Description: Master Configuration Register 10
Register Address: 48h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	1	—	—	—	—	—	SOFTEN	HARDEN
Default	0	0	0	0	0	1	0	1

Bit 7: This bit defaults to 0 but must be set to 1 for proper operation of ZL81000.

Bit 1: Soft Frequency Alarm Enable (SOFTEN). This bit enables input clock frequency monitoring with the soft alarm limit set in the ILIMIT register. Soft alarms are reported in the SOFT status bits of the ISR registers. See Section 6.5.1.

0 = Disabled
1 = Enabled

Bit 0: Hard Frequency Limit Enable (HARDEN). This bit enables input clock frequency monitoring with the hard alarm limit set in the ILIMIT register. Hard alarms are reported in the HARD status bits of the ISR registers. See Section 6.5.1.

0 = Disabled
1 = Enabled

Register Name: ILIMIT
Register Description: Input Clock Frequency Limit Register
Register Address: 49h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	SOFT[3:0]				HARD[3:0]			
Default	0	0	1	0	0	0	1	1

Bits 7 to 4: Soft Frequency Alarm Limit (SOFT[3:0]). This field is an unsigned integer that specifies the soft frequency alarm limit. The soft alarm limit is only used for monitoring; soft alarms do not invalidate input clocks. The limit in ppm is ±(SOFT[3:0] + 1) x 3.81. The default limit is ±11.43ppm. Soft alarms are reported in the SOFT status bits of the ISR registers. See Section 6.5.1.

Bits 3 to 0: Hard Frequency Alarm Limit (HARD[3:0]). This field is an unsigned integer that specifies the hard frequency alarm limit. Hard alarms invalidate input clocks. The limit in ppm is ±(HARD[3:0] + 1) x 3.81. The default limit is ±15.24ppm. Hard alarms are reported in the HARD status bits of the ISR registers. See Section 6.5.1.

Register Name: MCR11
Register Description: Master Configuration Register 11
Register Address: 4Bh

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	—	—	1	FMEASIN[3:0]			
Default	0	0	0	0	0	0	0	0

Bit 4: This bit defaults to 0 but must be set to 1 for proper operation of ZL81000.

Bits 3 to 0: Frequency Measurement Input Select (FMEASIN[3:0]). This field specifies the input clock for the frequency measurement reported in the FMEAS register. See Section 6.5.1.

0000 = {unused value}
0001 = IC1
0010 = IC2
0011 = IC3
0100 = IC4
0101-1111 = {unused value}

Register Name: FMEAS
Register Description: Frequency Measurement Register
Register Address: 4Ch

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	FMEAS[7:0]							
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: Measured Frequency (FMEAS[7:0]). This read-only field indicates the measured frequency of the input clock specified in the FMEASIN field of the MCR11 register. FMEAS is a two's-complement signed integer that expresses the frequency as an offset with respect to the internal master clock. The measured frequency is FMEAS[7:0] x 3.81ppm. See Section 6.5.1.

Register Name: DLIMIT3
Register Description: DPLL Frequency Limit Register 3
Register Address: 4Dh

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	FLLOL	SOFTLIM[6:0]						
Default	1	0	0	0	1	1	1	0

Bit 7: Frequency Limit Loss of Lock (FLLOL). When this bit is set to 1, the DPLL internally declares loss-of-lock when its hard limit is reached. The DPLL hard frequency limit is fixed at ±80ppm. See Section 6.7.5.

0 = DPLL declares loss-of-lock normally
1 = DPLL also declares loss-of-lock when the hard frequency limit is reached

Bits 6 to 0: DPLL Soft Frequency Limit (SOFTLIM6:0]). This field is an unsigned integer that specifies the soft frequency limit for the DPLL. The soft limit is only used for monitoring; exceeding this limit does not cause loss-of-lock. The limit in ppm is ±SOFTLIM[6:0] x 0.628. The default value is ±8.79ppm. When the DPLL frequency exceeds the soft limit the T4SOFT status bit is set in OPSTATE. See Section 6.7.5.

Register Name: IER4
Register Description: Interrupt Enable Register 4
Register Address: 4Eh

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	—	—	—	IC2NO4	IC1NO4	IC2NO8	IC1NO8
Default	0	0	0	0	0	0	0	0

Bit 3: Interrupt Enable for Input Clock 2 Has No 400Hz Component (IC2NO4). This bit is an interrupt enable for the IC2NO4 bit in the MSR4 register.

0 = Mask the interrupt
1 = Enable the interrupt

Bit 2: Interrupt Enable for Input Clock 1 Has No 400Hz Component (IC1NO4). This bit is an interrupt enable for the IC1NO4 bit in the MSR4 register.

0 = Mask the interrupt
1 = Enable the interrupt

Bit 1: Interrupt Enable for Input Clock 2 Has No 8kHz Component (IC2NO8). This bit is an interrupt enable for the IC2NO8 bit in the MSR4 register.

0 = Mask the interrupt
1 = Enable the interrupt

Bit 0: Interrupt Enable for Input Clock 1 Has No 8kHz Component (IC1NO8). This bit is an interrupt enable for the IC1NO8 bit in the MSR4 register.

0 = Mask the interrupt
1 = Enable the interrupt

Register Name: LB0U
Register Description: Leaky Bucket 0 Upper Threshold Register
Register Address: 50h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	LB0U[7:0]							
Default	0	0	0	0	0	1	1	0

Bits 7 to 0: Leaky Bucket 0 Upper Threshold (LB0U[7:0]). When the leaky bucket accumulator is equal to the value stored in this field, the activity monitor declares an activity alarm by setting the input clock's ACT bit in the appropriate ISR register. Registers LB0U, LB0L, LB0S, and LB0D together specify leaky bucket configuration 0. See Section 6.5.2.

Register Name: LB0L
Register Description: Leaky Bucket 0 Lower Threshold Register
Register Address: 51h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	LB0L[7:0]							
Default	0	0	0	0	0	1	0	0

Bits 7 to 0: Leaky Bucket 0 Lower Threshold (LB0L[7:0]). When the leaky bucket accumulator is equal to the value stored in this field, the activity monitoring logic clears the activity alarm (if previously declared) by clearing the input clock's ACT bit in the appropriate ISR register. Registers LB0U, LB0L, LB0S, and LB0D together specify leaky bucket configuration 0. See Section 6.5.2.

Register Name: LB0S
Register Description: Leaky Bucket 0 Size Register
Register Address: 52h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	LB0S[7:0]							
Default	0	0	0	0	1	0	0	0

Bits 7 to 0: Leaky Bucket 0 Size (LB0S[7:0]). This field specifies the maximum value of the leaky bucket. The accumulator cannot increment past this value. Registers LB0U, LB0L, LB0S, and LB0D together specify leaky bucket configuration 0. See Section 6.5.2.

Register Name: LB0D
Register Description: Leaky Bucket 0 Decay Rate Register
Register Address: 53h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	—	—	—	—	—	LB0D[1:0]	
Default	0	0	0	0	0	0	0	1

Bits 1 to 0: Leaky Bucket 0 Decay Rate (LB0D[1:0]). This field specifies the decay or “leak” rate of the leaky bucket accumulator. For each period of 1, 2, 4, or 8 128ms intervals in which no irregularities are detected on the input clock, the accumulator decrements by 1. Registers LB0U, LB0L, LB0S, and LB0D together specify leaky bucket configuration 0. See Section 6.5.2.

00 = decrement every 128ms (8 units/second)
01 = decrement every 256ms (4 units/second)
10 = decrement every 512ms (2 units/second)
11 = decrement every 1024ms (1 unit/second)

Register Name: LB1U, LB2U, LB3U
Register Description: Leaky Bucket 1/2/3 Upper Threshold Register
Register Address: 54h, 58h, 5Ch

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	LBxU[7:0]							
Default	0	0	0	0	0	1	1	0

Bits 7 to 0: Leaky Bucket 'x' Upper Threshold (LBxU[7:0]). See the LB0U register description.
Registers LB1U, LB1L, LB1S, and LB1D together specify leaky bucket configuration 1.
Registers LB2U, LB2L, LB2S, and LB2D together specify leaky bucket configuration 2.
Registers LB3U, LB3L, LB3S, and LB3D together specify leaky bucket configuration 3.

Register Name: LB1L, LB2L, LB3L
Register Description: Leaky Bucket 1/2/3 Lower Threshold Register
Register Address: 55h, 59h, 5Dh

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	LBxL[7:0]							
Default	0	0	0	0	0	1	0	0

Bits 7 to 0: Leaky Bucket 'x' Lower Threshold (LBxL[7:0]). See the LB0L register description.
Registers LB1U, LB1L, LB1S, and LB1D together specify leaky bucket configuration 1.
Registers LB2U, LB2L, LB2S, and LB2D together specify leaky bucket configuration 2.
Registers LB3U, LB3L, LB3S, and LB3D together specify leaky bucket configuration 3.

Register Name: LB1S, LB2S, LB3S
Register Description: Leaky Bucket 1/2/3 Size Register
Register Address: 56h, 5Ah, 5Eh

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	LBxS[7:0]							
Default	0	0	0	0	1	0	0	0

Bits 7 to 0: Leaky Bucket 'x' Size (LBxS[7:0]). See the LB0S register description.
Registers LB1U, LB1L, LB1S, and LB1D together specify leaky bucket configuration 1.
Registers LB2U, LB2L, LB2S, and LB2D together specify leaky bucket configuration 2.
Registers LB3U, LB3L, LB3S, and LB3D together specify leaky bucket configuration 3.

Register Name: LB1D, LB2D, LB3D
Register Description: Leaky Bucket 1/2/3 Decay Rate Register
Register Address: 57h, 5Bh, 5Fh

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	—	—	—	—	—	LBxD[1:0]	
Default	0	0	0	0	0	0	0	1

Bits 1 to 0: Leaky Bucket 'x' Decay Rate (LBxD[1:0]). See the LB0D register description.
Registers LB1U, LB1L, LB1S, and LB1D together configure leaky bucket algorithm 1.
Registers LB2U, LB2L, LB2S, and LB2D together configure leaky bucket algorithm 2.
Registers LB3U, LB3L, LB3S, and LB3D together configure leaky bucket algorithm 3.

Register Name: OCR4
Register Description: Output Configuration Register 4
Register Address: 63h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	—	OC9EN	—	—	—	—	—
Default	1	1	1	1	0	1	1	0

Bit 5: OC9 Enable (OC9EN). This configuration bit enables the 1.544/2.048MHz output on OC9.
0 = Disabled (low)
1 = Enabled

Register Name: T4CR1
Register Description: DPLL Configuration Register 1
Register Address: 64h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	ASQUEL	—	OC9SON	T4FREQ[3:0]			
Default	0	0	0	see below	0	0	0	1

Bit 6: Auto-Squelch (ASQUEL). This configuration bit enables automatic squelching of OC9 whenever the DPLL has no valid input references. When an output is squelched it is forced low.
0 = Disable automatic squelching
1 = Enable automatic squelching of OC9 when DPLL has no valid input references

Bit 4: OC9 SONET/SDH (OC9SON). This bit controls the frequency of clock output OC9. During reset the default value of this bit is latched from the SONSDH pin.
0 = 2048kHz (SDH)
1 = 1544kHz (SONET)

Bits 3 to 0: DPLL Frequency (T4FREQ[3:0]). This field must be left at its default value of 0001.

Register Name: T4BW
Register Description: DPLL Bandwidth Register
Register Address: 66h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	—	—	—	—	—	T4BW[1:0]	
Default	0	0	0	0	0	0	0	0

Bits 1 to 0: DPLL Bandwidth (T4BW[1:0]). See Section 6.7.2.
00 = 18 Hz
01 = 35 Hz
10 = 70 Hz
11 = {unused value}

Register Name: T4CR2
Register Description: DPLL Configuration Register 2
Register Address: 6Ah

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	—	—	—	—	DAMP[2:0]		
Default	0	0	0	1	0	0	1	1

Bits 2 to 0: Damping Factor (DAMP[2:0]). This field configures the damping factor of the DPLL. Damping factor is a function of both DAMP[2:0] and the DPLL bandwidth (T4BW register). The default value corresponds to a damping factor of 5. See Section 6.7.3.

	18 Hz	35 Hz	70 Hz
001 =	1.2	1.2	1.2
010 =	2.5	2.5	2.5
011 =	5	5	5
100 =	5	10	10
101 =	5	10	20

000, 110 and 111 = {unused values}

The gain peak for each damping factor is shown below:

Damping Factor	Gain Peak
1.2	0.4 dB
2.5	0.2 dB
5	0.1 dB
10	0.06 dB
20	0.03 dB

Register Name: GPCR
Register Description: GPIO Configuration Register
Register Address: 6Eh

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	GPIO4D	GPIO3D	GPIO2D	GPIO1D	GPIO4O	GPIO3O	GPIO2O	GPIO1O
Default	0	0	0	0	0	0	0	0

Bit 7: GPIO4 Direction (GPIO4D). This bit configures the data direction for the GPIO4 pin. When GPIO4 is an input its current state can be read from GPSR:GPIO4. When GPIO4 is an output, its value is controlled by the GPIO4O configuration bit.
0 = Input
1 = Output

Bit 6: GPIO3 Direction (GPIO3D). This bit configures the data direction for the GPIO3 pin. When GPIO3 is an input its current state can be read from GPSR:GPIO3. When GPIO3 is an output, its value is controlled by the GPIO3O configuration bit.
0 = Input
1 = Output

Bit 5: GPIO2 Direction (GPIO2D). This bit configures the data direction for the GPIO2 pin. When GPIO2 is an input its current state can be read from GPSR:GPIO2. When GPIO2 is an output, its value is controlled by the GPIO2O configuration bit.
0 = Input
1 = Output

Bit 4: GPIO1 Direction (GPIO1D). This bit configures the data direction for the GPIO1 pin. When GPIO1 is an input its current state can be read from GPSR:GPIO1. When GPI13 is an output, its value is controlled by the GPIO1O configuration bit.
0 = Input
1 = Output

Bit 3: GPIO4 Output Value (GPIO4O). When GPIO4 is configured as an output (GPIO4D=1) then this bit specifies the output value.
0 = Low
1 = High

Bit 2: GPIO3 Output Value (GPIO3O). When GPIO3 is configured as an output (GPIO3D=1) then this bit specifies the output value.
0 = Low
1 = High

Bit 1: GPIO2 Output Value (GPIO2O). When GPIO2 is configured as an output (GPIO2D=1) then this bit specifies the output value.
0 = Low
1 = High

Bit 0: GPIO1 Output Value (GPIO1O). When GPIO1 is configured as an output (GPIO1D=1) then this bit specifies the output value.
0 = Low
1 = High

Register Name: GPSR
Register Description: GPIO Status Register
Register Address: 6Fh

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	—	—	—	GPIO4	GPIO3	GPIO2	GPIO1
Default	0	0	0	0	0	0	0	0

Bit 3: GPIO4 State (GPIO4). This bit indicates the current state of the GPIO4 pin.
0 = low
1 = high

Bit 2: GPIO3 State (GPIO3). This bit indicates the current state of the GPIO3 pin.
0 = low
1 = high

Bit 2: GPIO2 State (GPIO2). This bit indicates the current state of the GPIO2 pin.
0 = low
1 = high

Bit 1: GPIO1 State (GPIO1). This bit indicates the current state of the GPIO1 pin.
0 = low
1 = high

Register Name: PHLIM1
Register Description: Phase Limit Register 1
Register Address: 73h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	FLEN	NALOL	1	—	—	FINELIM[2:0]		
Default	1	0	1	0	0	0	1	0

Bit 7: Fine Phase Limit Enable (FLEN). This configuration bit enables the DPLL fine phase limit specified in the FINELIM[2:0] field. The fine limit must be disabled for multi-UI jitter tolerance (see PHLIM2 fields). See Section 6.7.5.
0 = Disabled
1 = Enabled

Bit 6: No-Activity Loss of Lock (NALOL). The DPLL can detect that an input clock has no activity very quickly (within two clock cycles). When NALOL=0, loss-of-lock is not declared when clock cycles are missing, and nearest edge locking (±180°) is used when the clock recovers. This gives tolerance to missing cycles. When NALOL=1, loss-of-lock is indicated as soon as no activity is detected, and the device switches to phase/frequency locking (±360°). See Sections 6.5.3 and 6.7.5.
0 = No activity does not trigger loss-of-lock
1 = No activity does trigger loss-of-lock

Bit 5: Leave set to 1 (test control).

Bits 2 to 0: Fine Phase Limit (FINELIM[2:0]). This field specifies the fine phase limit window, outside of which loss-of-lock is declared. The FLEN bit enables this feature. The phase of the input clock has to be inside the fine limit window for two seconds before phase lock is declared. Loss-of-lock is declared immediately if the phase of the input clock is outside the phase limit window. The default value of 010 is appropriate for most situations. See Section 6.7.5.
000 = Always indicates loss of phase lock—do not use
001 = Small phase limit window, ±45 to ±90°

010 = Normal phase limit window, ±90 to ±180° (default)
100, 101, 110, 111 = Proportionately larger phase limit window

Register Name: PHLIM2
Register Description: Phase Limit Register 2
Register Address: 74h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	CLEN	MCPDEN	USEMCPD	—	COARSELIM[3:0]			
Default	1	0	0	0	0	1	0	1

Bit 7: Coarse Phase Limit Enable (CLEN). This configuration bit enables the DPLL coarse phase limit specified in the COARSELIM[3:0] field. See Section 6.7.5.
0 = Disabled
1 = Enabled

Bit 6: Multi-Cycle Phase Detector Enable (MCPDEN). This configuration bit enables the DPLL multi-cycle phase detector and allows the DPLL to tolerate large-amplitude jitter and wander. The range of this phase detector is the same as the coarse phase limit specified in the COARSELIM[3:0] field. See Section 6.7.4.
0 = Disabled
1 = Enabled

Bit 5: Use Multi-Cycle Phase Detector in the DPLL Algorithm (USEMCPD). This configuration bit enables the DPLL algorithm to use the multi-cycle phase detector so that a large phase measurement drives faster DPLL pull-in. When USEMCPD=0, phase measurement is limited to ±360°, giving slower pull-in at higher frequencies but with less overshoot. When USEMCPD=1, phase measurement is set as specified in the COARSELIM[3:0] field, giving faster pull-in. MCPDEN should be set to 1 when USEMCPD=1. See Section 6.7.4.
0 = Disabled
1 = Enabled

Bits 3 to 0: Coarse Phase Limit (COARSELIM[3:0]). This field specifies the DPLL coarse phase limit and the tracking range of the multi-cycle phase detector. The CLEN bit enables this feature. If jitter tolerance greater than 0.5 UI is required and the input clock is a high frequency signal then the DPLL can be configured to track phase errors over many UI using the multi-cycle phase detector. See Section 6.7.4 and 6.7.5.
0000 = ±1 UI
0001 = ±3 UI
0010 = ±7 UI
0011 = ±15 UI
0100 = ±31 UI
0101 = ±63 UI
0110 = ±127 UI
0111 = ±255 UI
1000 = ±511 UI
1001 = ±1023 UI
1010 = ±2047 UI
1011 = ±4095 UI
1100 to 1111 = ±8191 UI

Register Name: PHASE1
Register Description: Phase Register 1
Register Address: 77h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	PHASE[7:0]							
Default	0	0	0	0	0	0	0	0

The PHASE1 and PHASE2 registers must be read consecutively. See Section 7.3.

Bits 7 to 0: Current DPLL Phase (PHASE[7:0]). The full 16-bit PHASE[15:0] field spans this register and the PHASE2 register. PHASE is a 2's-complement signed integer that indicates the current value of the DPLL phase detector. The value is the output of the phase averager. The averaged phase difference in degrees is equal to PHASE * 0.707. See Section 6.7.6.

Register Name: PHASE2
Register Description: Phase Register 2
Register Address: 78h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	PHASE[15:8]							
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: Current DPLL Phase (PHASE[15:8]). See the PHASE1 register description.

Register Name: INTCR
Register Description: Interrupt Configuration Register
Register Address: 7Dh

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	—	—	—	—	GPO	OD	POL
Default	0	0	0	0	0	0	1	0

Bit 2: INTREQ Pin General-Purpose Output Enable (GPO). When set to 1 this bit configures the interrupt request pin to be a general-purpose output whose value is set by the POL bit.

0 = INTREQ is used for interrupts
1 = INTREQ is a general-purpose output

Bit 1: INTREQ Pin Open-Drain Enable (OD).

When GPO = 0:
0 = INTREQ is driven in both inactive and active states
1 = INTREQ is open-drain, i.e., it is driven in the active state but is high impedance in the inactive state
When GPO = 1:
0 = INTREQ is driven as specified by POL
1 = INTREQ is high impedance and POL has no effect

Bit 0: INTREQ Pin Polarity (POL).

When GPO = 0:
0 = INTREQ goes low to signal an interrupt (active low)
1 = INTREQ goes high to signal an interrupt (active high)
When GPO = 1:
0 = INTREQ driven low
1 = INTREQ driven high

Register Name: PROT
Register Description: Protection Register
Register Address: 7Eh

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	PROT[7:0]							
Default	1	0	0	0	0	1	0	1

Bits 7 to 0: Protection Control (PROT[7:0]). This field can be used to protect the rest of the register set from inadvertent writes. In protected mode writes to all other registers are ignored. In single unprotected mode, one register (other than PROT) can be written, but after that write the device reverts to protected mode (and the value of PROT is internally changed to 00h). In fully unprotected mode all register can be written without limitation. See Section 6.2.

1000 0101 = Fully unprotected mode
1000 0110 = Single unprotected mode
all other values = Protected mode

Register Name: IFCR
Register Description: Microprocessor Interface Configuration Register
Register Address: 7Fh

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	—	—	—	—	IFSEL[2:0]		
Default	0	0	0	0	0	reset value of IFSEL[2:0] pins		

Bits 2:0 Microprocessor Interface Selection (IFSEL[2:0]). This read-only field specifies the microprocessor interface mode. The value of this register is latched from the IFSEL[2:0] pins during reset. After reset the state of the IFSEL[2:0] pins has no effect on this register but is shown in the IFSR register. See Section 6.11.

010 = Intel bus mode (multiplexed)
011 = Intel bus mode (nonmultiplexed)
100 = Motorola mode (nonmultiplexed)
101 = SPI mode (address and data transmitted LSB first)
110 = Motorola mode (multiplexed)
111 = SPI mode (address and data transmitted MSB first)
000, 001 = {unused value}

7.5 BITS Transceiver Register Definitions

The ZL81000 has two identical, independent BITS transceivers, BITS1 and BITS2. The registers for BITS1 start at 80h while those for BITS2 start at 100h. The register map shown in Table 7-3 applies to both transceivers. The address offsets in the table are added to the base addresses (Table 7-1) for the BITS transceivers to form a full address. For example, the BLSR1 register in the BITS1 transceiver is located at address 080h + 1Ah = 9Ah.

Table 7-3. BITS Transceiver Register Map

Note: *Register names are hyperlinks to register definitions. Underlined fields are read-only.*

ADDR OFFSET	REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
04	BMCR	—	—	TMODE[1:0]		—	—	RMODE[1:0]	
08	BCCR1	TCLKS[3:0]				TSYNCS[3:0]			
09	BCCR2	RCLKD[3:0]				RSYNCD[3:0]			
0A	BCCR3	MCLKS	MCLKFC	ROUTS	ROINV	RCINV	ROEN	RCEN	RSEN
0B	BCCR4	TMFS	—	TOUTS	TOINV	TCINV	TOEN	TCEN	TIINV
0C	BCCR5	MPS[1:0]		ZEROS[1:0]		—	—	—	—
10	BLCR1	LIRST	—	—	—	—	—	—	LCS
11	BLCR2	—	TION	TIMP[1:0]		0	LBO[2:0]		
12	BLCR3	0	RION	RIMP[1:0]		RTR	RMONEN	RSMS[1:0]	
13	BLCR4	TAIS	—	LLB	ALB	RLB	TPD	RPD	TE
18	BLIR1	—	RFAIL	OEQ	UEQ	—	OC	SC	LOS
19	BLIR2	RL[3:0]				—	—	—	—
1A	BLSR1	—	OCC	SCC	LOSC	—	OC	SC	LOS
1B	BLIER1	—	OCC	SCC	LOSC	—	OC	SC	LOS
20	BRMMR	REN	RID	—	—	—	—	RRST	RT1E1
21	BTMMR	TEN	TID	—	—	—	—	TRST	TT1E1
22	BRCR1	SYNCT	RB8ZS	RFM	ARC	SYNCC	RJC	SYNCD	RESYNC
23	BRCR2	—	—	—	—	OOFC[1:0]		RAIIE	RSFRAI
24	BRCR3	—	RHDB3	RSIGM	—	RCRC4	FRC	SYNCD	RESYNC
25	BRCR4	—	—	—	—	—	—	—	RLOSC
26	BRCR5	—	—	—	—	—	—	RMFS	1
27	BTCR1	TJC	TFPT	TCPT	—	—	TB8ZS	TAIS	TRAI
28	BTCR2	—	—	—	FBCT2	FBCT1	TSFRAI	TPDE	TB7ZS
29	BTCR3	—	—	—	—	—	TFM	IBPV	—
2A	BTCR4	TFPT	—	—	TSiS	—	THDB3	TAIS	TCRC4
30	BRIIR	—	BRSR4	—	—	—	—	BRSR3	BRSR1
31	BRIR1	—	—	—	—	RAI	AIS	LOS	OOF
32	BRIR2	CSC[5:2,0]					CRC4SA	CASSA	FASSA
33	BRSR1	RAIC	AISC	LOSC	OOFC	RAI	AIS	LOS	OOF
34	BRIER1	RAIC	AISC	LOSC	OOFC	RAI	AIS	LOS	OOF
35	BRSR2	RPDV	—	COFA	8ZD	16ZD	SEFE	B8ZS	FBE
36	BRSR3	—	CRCRC	CASRC	FASRC	RSA1	RSA0	RCMF	RAF
37	BRIER3	—	—	—	—	RSA1	RSA0	RCMF	RAF
38	BRSR4	—	—	—	—	—	—	BC	BD
39	BRIER4	—	—	—	—	—	—	BC	BD
3A	BTSR1	—	—	—	—	TPDV/TAF	TMF	LOTCC	LOTC
3B	BTIER1	—	—	—	—	TPDV/TAF	TMF	LOTCC	LOTC
40	BRBCR	RBR	—	RBD[1:0]		RBF[2:0]			—
41	BTBCR	—	SBOC	—	—	—	—	—	—
42	BRBOC	—	—	RBOC[5:0]					
43	BTBOC	—	—	TBOC[5:0]					
50	BRAF	Si	FAS[6:0]						
51	BRNAF	Si	1	RAI	Sa4	Sa5	Sa6	Sa7	Sa8
52	BRSiAF	SiF0	SiF2	SiF4	SiF6	SiF8	SiF10	SiF12	SiF14

ADDR OFFSET	REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
53	BRSiNAF	SiF1	SiF3	SiF5	SiF7	SiF9	SiF11	SiF13	SiF15
54	BRRAI	RAIF1	RAIF3	RAIF5	RAIF7	RAIF9	RAIF11	RAIF13	RAIF15
55	BRSa4	Sa4F1	Sa4F3	Sa4F5	Sa4F7	Sa4F9	Sa4F11	Sa4F13	Sa4F15
56	BRSa5	Sa5F1	Sa5F3	Sa5F5	Sa5F7	Sa5F9	Sa5F11	Sa5F13	Sa5F15
57	BRSa6	Sa6F1	Sa6F3	Sa6F5	Sa6F7	Sa6F9	Sa6F11	Sa6F13	Sa6F15
58	BRSa7	Sa7F1	Sa7F3	Sa7F5	Sa7F7	Sa7F9	Sa7F11	Sa7F13	Sa7F15
59	BRSa8	Sa8F1	Sa8F3	Sa8F5	Sa8F7	Sa8F9	Sa8F11	Sa8F13	Sa8F15
5A	BRMCR	—	SSMCH[2:0]			—	—	SSMF[1:0]	
5B	BRMSR	—	—	Sa8	—	Sa7	Sa6	Sa5	Sa4
5C	BRMIER	—	—	Sa8	—	Sa7	Sa6	Sa5	Sa4
5D	BRSSM	—	SSMCH[2:0]			SSM[3:0]			
60	BTAF	Si	FAS[6:0]						
61	BTNAF	Si	1	RAI	Sa4	Sa5	Sa6	Sa7	Sa8
62	BTSiAF	SiF0	SiF2	SiF4	SiF6	SiF8	SiF10	SiF12	SiF14
63	BTSiNAF	SiF1	SiF3	SiF5	SiF7	SiF9	SiF11	SiF13	SiF15
64	BTRAI	RAIF1	RAIF3	RAIF5	RAIF7	RAIF9	RAIF11	RAIF13	RAIF15
65	BTSa4	Sa4F1	Sa4F3	Sa4F5	Sa4F7	Sa4F9	Sa4F11	Sa4F13	Sa4F15
66	BTSa5	Sa5F1	Sa5F3	Sa5F5	Sa5F7	Sa5F9	Sa5F11	Sa5F13	Sa5F15
67	BTSa6	Sa6F1	Sa6F3	Sa6F5	Sa6F7	Sa6F9	Sa6F11	Sa6F13	Sa6F15
68	BTSa7	Sa7F1	Sa7F3	Sa7F5	Sa7F7	Sa7F9	Sa7F11	Sa7F13	Sa7F15
69	BTSa8	Sa8F1	Sa8F3	Sa8F5	Sa8F7	Sa8F9	Sa8F11	Sa8F13	Sa8F15
6A	BTOCR	SiAF	SiNAF	RAI	Sa4	Sa5	Sa6	Sa7	Sa8

BITS Transceiver Register Map Color Coding

	BITS Global Registers
	BITS LIU Registers
	BITS DS1/E1 Framer Registers
	BITS DS1 BOC Controller
	BITS E1 Si/Sa Registers

Register Name: BMCR
Register Description: BITS Mode Configuration Register
Register Address: 04h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	—	TMODE[1:0]		—	—	RMODE[1:0]	
Default	0	0	0	0	0	0	0	0

Bits 5 to 4: Transmitter Mode Configuration (TMODE[1:0]). This field configures the operating mode of the BITS transmitter. Note that in DS1 and E1 modes the transmit formatter must also be enabled and configured for DS1 or E1. See Sections 6.9.5.2 (DS1) and 6.9.6.2 (E1) for step-by-step configuration instructions. Table 9-2 indicates the reduction in supply current when the transmitter is powered down. See Section 6.9.7.2 for write sequences that must be done when entering or leaving the 2048 kHz mode.

00 = DS1
01 = E1
10 = 2048 kHz[1]
11 = {unused value}

Bits 1 to 0: Receiver Mode Configuration (RMODE[1:0]). This field configures the operating mode of the BITS receiver. Note that in DS1 and E1 modes the receive framer must also be enabled and configured for DS1 or E1. See Sections 6.9.5.1 (DS1) and 6.9.6.1 (E1) for step-by-step configuration instructions. Table 9-2 indicates the reduction in supply current when the receiver is powered down. Values not listed are undefined.

00 = DS1
01 = E1
10 = 2048 kHz[1]
11 = 6312 kHz[2]

Notes
1. Complies with G.703 Section 13.
2. Complies with G.703 appendix II.2 Japanese synchronization interface.
3. TMODE and RMODE can be set to different frequencies.

Register Name: BCCR1
Register Description: BITS Clock Configuration Register 1
Register Address: 08h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	TCLKS[3:0]				TSYNCS[3:0]			
Default	1	0	0	1	1	1	1	1

Bits 7 to 4: Transmit CLK Source (TCLKS[3:0]). See Figure 6-2 and Figure 6-4. This field specifies the source for the 1544 kHz or 2048 kHz clock for the Tx Clock Mux block. See Section 6.9.3.

0000 = TIN input pin
0001 – 1000 = {unused values}
1001 = Output clock OC9
1010 – 1101 = {unused values}
1110 = RCLK from the BITS receiver
1111 = BITS master clock from the BITS master clock PLL

Bits 3 to 0: Transmit SYNC Source (TSYNCS[3:0]). , See Figure 6-2 and Figure 6-4. In DS1 and E1 BITS transmitter modes, this field specifies the source of the alignment signal for the 8 kHz frame sync signal (TSYNC). In other BITS transmitter modes this field has no effect. See Section 6.9.3.

0000 = TIN input pin
0001 – 1110 = {unused values}
1111 = TCLK signal divided by 193 (DS1 mode) or 256 (E1 mode)

Register Name: BCCR2
Register Description: BITS Clock Configuration Register 2
Register Address: 09h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	RCLKD[3:0]				RSYNCD[3:0]			
Default	0	0	0	0	0	0	0	0

Bits 7 to 4: RCLK Destination (RCLKD[3:0]). This field specifies an internal destination for the BITS receiver's recovered clock, RCLK. For values other than 0000, the RCLKD setting must be coordinated with the configuration of the selected input clock (Section 6.4) and the BITS receiver mode (BMCR:RMODE). The RCLK signal can also be output on the RCLK pin when RCEN=1 in BCCR3. See Section 6.9.2.

0000 = No internal destination
0001 = Input clock IC1
0010 = Input clock IC2
0011 = Input clock IC3
0100 = Input clock IC4
0101 - 1110 = {unused values]
1111 = No internal destination

Bits 3 to 0: RSYNC Destination (RSYNCD[3:0]). This field specifies an internal the destination for the RSYNC signal (Figure 6-2). In DS1 and E1 modes, RSYNC is the recovered 8 kHz frame sync. In other BITS receiver modes RSYNC is inactive and this field has no effect. The RSYNCD setting must be coordinated with the configuration of the selected input clock (Section 6.4) and the BITS receiver mode (BMCR:RMODE). See Section 6.9.2.

0000 = No internal destination
0001 = Input clock IC1
0010 = Input clock IC2
0011 = Input clock IC3
0100 = Input clock IC4
0101 - 1110 = {unused values]
1111 = No internal destination

Register Name: BCCR3
Register Description: BITS Clock Configuration Register 3
Register Address: 0Ah

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	MCLKS	MCLKFC	ROUTS	ROINV	RCINV	ROEN	RCEN	RSEN
Default	0	0	0	0	0	0	0	0

Bit 7: MCLK Source (MCLKS). This bit specifies the source for the master clock for both BITS transceivers. When MCLKS=0, BCCR5:MPS[1:0] must be set to 00. See Section 6.9.1.

0 = Source from 204.8 MHz master clock (divided by 100)
1 = Source from MCLK pin

Bit 6: MCLK Frequency Converter (MCLKFC). This bit specifies whether or not to use the 2.048 kHz to 1.544 kHz frequency conversion PLL in the BITS master clock PLL block. See Figure 6-3 and Section 6.9.1.

0 = bypass the frequency converter PLL
1 = use the output of the frequency converter PLL

Bit 5: ROUT Source (ROUTS). This field specifies the signal source for the ROUT output pin, either RSYNC or RMFSYNC (see Figure 6-2). In DS1 and E1 modes, the RSYNC signal is the received 8 kHz frame sync, and the RMFSYNC signal is the receive multiframe sync, with E1 multiframe type specified by BRCR5:RMFS. In 2048 kHz and 6312 kHz modes, RSYNC is held low. See Section 6.9.2.

0 = RSYNC signal
1 = RMFSYNC signal

Bit 4: ROUT Invert (ROINV). When ROEN=1, this bit specifies the polarity of ROUT. When ROEN=0, the ROUT pin can function as a general-purpose output controlled by this bit. See Section 6.9.2.

ROEN=1
0 = Normal: ROUT normally low, pulses high
1 = Inverted ROUT normally high, pulses low

ROEN=0
0 = ROUT pin forced low
1 = ROUT pin forced high

Bit 3: RCLK Invert (RCINV). When RCEN=1, this bit specifies the RCLK edge on which data is updated on the RSER pin (DS1 and E1 modes only). When RCEN=0, the RCLK pin can function as a general-purpose output pin whose value is specified by this bit. See Sections 6.9.5.1 and 6.9.6.1.

RCEN=1
0 = Normal: RSER updated on the rising edge of RCLK
1 = Inverted: RSER updated on the falling edge of RCLK

RCEN=0
0 = RCLK pin forced low
1 = RCLK pin forced high

Bit 2: ROUT Enable (ROEN). This bit enables/disables the ROUT output pin. When enabled, ROUT presents the signal specified by BCCR3:ROUTS. When disabled, ROUT can function as a general-purpose output controlled by the ROINV configuration bit. See Section 6.9.2.

0 = Disabled
1 = Enabled

Bit 1: RCLK Enable (RCEN). This bit enables/disables the RCLK output pin. When enabled, RCLK presents the recovered clock from the BITS receiver. When disabled, RCLK can function as a general-purpose output controlled by the RCINV configuration bit. See Section 6.9.2.

0 = Disabled
1 = Enabled

Bit 0: RSER Enable (RSEN). This bit enables/disables the RSER output pin. In DS1 and E1 receiver modes (BMCR:RMODE=0x), RSER presents the entire received data stream, both payload and overhead. In all other BITS receiver modes RSER is disabled and this bit has no effect. See Section 6.9.2.

0 = Disabled (low)
1 = Enabled

Register Name: BCCR4
Register Description: BITS Clock Configuration Register 4
Register Address: 0Bh

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	TMFS	—	TOUTS	TOINV	TCINV	TOEN	TCEN	TIINV
Default	0	0	0	0	0	0	0	0

Bit 7: Transmit Multiframe Sync Source (TMFS). In DS1 and E1 modes, this field specifies the source of the transmit multiframe signal (TMFSYNC). In other BITS transmitter modes this field has no effect. When the TIN pin is specified, the signal on TIN must be frequency locked to the TCLK source specified by BCCR1:TCLKS[3:0]. See Section 6.9.3.

0 = TSYNC signal divided by 12 (DS1 SF), 24 (DS1 ESF), or 16 (E1)
1 = TIN input pin

Bit 5: TOUT Source (TOUTS). This field specifies the signal source for the TOUT output pin. See Figure 6-2. In DS1 and E1 modes, the TSYNC signal is the transmit 8 kHz frame sync, and the TMFSYNC signal is the transmit multiframe sync. In other BITS transmitter modes this bit has no effect. See Section 6.9.3

0 = TSYNC signal
1 = TMFSYNC signal

Bit 4: TOUT Invert (TOINV). See Section 6.9.3.

0 = Normal: TOUT normally low, pulses high
1 = Inverted: TOUT normally high, pulses low

Bit 3: TCLK Invert (TCINV). Specifies the TCLK clock edge on which data is sampled from TSER and TIN. This bit only has an effect in DS1 and E1 BITS transmitter modes (BMCR:TMODE=0x). See Sections 6.9.5.2 and 6.9.6.2.

0 = Normal: TSER and TIN updated on the falling edge of TCLK
1 = Inverted: TSER and TIN updated on the rising edge of TCLK

Bit 2: TOUT Enable (TOEN). This bit enables/disables the TOUT output pin. When enabled, TOUT presents the signal specified by TOUTS. In 2048 kHz mode this bit has no effect, and TOUT remains low. See Section 6.9.3.

0 = Disabled (low)
1 = Enabled

Bit 1: TCLK Enable (TCEN). This bit enables/disables the TCLK output pin. See Section 6.9.3.

0 = Disabled (low)
1 = Enabled

Bit 0: TIN Invert (TIINV). When high See Section 6.9.3.

0 = Normal: TIN normally low, pulses high
1 = Inverted: TIN normally high, pulses low

Register Name: BCCR5
Register Description: BITS Clock Configuration Register 5
Register Address: 0Ch

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	MPS[1:0]		ZEROS[1:0]		—	—	—	—
Default	0	0	0	0	0	0	0	0

Bits 7 to 6: MCLK Prescaler (MPS[1:0]). This field configures the divider in the MCLK prescaler block. When BCCR3:MCLKS=0, MPS[1:0] must be set to 00. See Figure 6-3 and Section 6.9.1.

00 = Divide by 1 (pass through MCLK signal unchanged)
01 = Divide by 2
10 = Divide by 4
11 = Divide by 8

Bits 5 to 4: Squelch and Increment on Zeros (ZEROS[1:0]). If this field is set to a non-zero value in any mode and the specified number of consecutive zeros are detected (prior to B8ZS/HDB3 decoding), then the BITS receiver automatically squelches its output clock. See Sections 6.5 and 6.9.2.

00 = Do not invalidate on zeros
01 = Invalidate on a string of 4 consecutive zeros
10 = Invalidate on a string of 8 consecutive zeros
11 = Invalidate on a string of 16 consecutive zeros

Register Name: BLCR1
Register Description: BITS LIU Configuration Register 1
Register Address: 10h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	LIRST	—	—	—	—	—	—	LCS
Default	0	0	0	0	0	0	0	1

Bit 7: Line Interface Reset (LIRST). A zero-to-one transition resets the clock recovery state machine. Normally this bit is only toggled after power-up. LIRST must be cleared and set again for a subsequent reset.

Bit 0: LOS Criteria Selection (LCS). In E1 mode this bit specifies the loss of signal criteria to use. In DS1 mode, LOS criteria is always based on ANSTI T1.231, and this bit has no effect. See Section 6.9.4.1.

0 = G.775 criteria (192-bit window)
1 = ETSI 300 233 criteria (2048-bit window)

Register Name: BLCR2
Register Description: BITS LIU Configuration Register 2
Register Address: 11h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	TION	TIMP[1:0]		0	LBO[2:0]		
Default	0	0	0	0	0	0	0	0

Bit 6: Transmitter Impedance On (TION). See Section 6.9.4.2.

0 = Disable internal transmitter termination
1 = Enable internal transmitter termination with impedance set by TIMP[1:0]

Bits 5 to 4: Transmit Impedance (TIMP[1:0]). This field specifies the transmit cable impedance. The actual transmit cable impedance must be specified by this field for proper operation, regardless of the value of the TION bit. For J1 applications, use 110Ω. See Section 6.9.4.1.6.

00 = 75Ω
01 = 100Ω
10 = 110Ω
11 = 120Ω

Bit 3: Leave set to zero (test control).

Bits 2 to 0: Transmitter Line Build-Out (LBO[2:0]). This field specifies the line build-out setting for the BITS transmitter. Values not listed are undefined. This field is ignored in BITS modes other than DS1 and E1. See Section 6.9.4.1.6.

DS1 Mode

000 = DSX-1 (0 to 133 feet) / 0 dB CSU
001 = DSX-1 (133 to 266 feet)
010 = DSX-1 (266 to 399 feet)
011 = DSX-1 (399 to 533 feet)
100 = DSX-1 (533 to 655 feet)
101 = -7.5 dB CSU
110 = -15 dB CSU
111 = -22.5 dB CSU

E1 Mode

000 = 75Ω, nominal voltage = 2.37V
001 = 120Ω, nominal voltage = 3.0V

Register Name: BLCR3
Register Description: BITS LIU Configuration Register 3
Register Address: 12h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	0	RION	RIMP[1:0]		RTR	RMONEN	RSMS[1:0]	
Default	0	0	0	0	0	0	0	0

Bit 7: Leave set to zero (test control).

Bit 6: Receiver Impedance On (RION). See Section 6.9.4.1.
0 = Disable internal receiver termination, RTIP/RRING are high-impedance
1 = Enable internal receiver termination with impedance set by RIMP[1:0]

Bits 5 to 4: Receive Impedance (RIMP[1:0]). This field specifies the receive cable impedance. When internal termination impedance is enabled (RION=1), the internal impedance is set to the value specified by this field. When internal termination impedance is disabled (RION=0), the actual receive cable impedance must be specified by this field for proper operation. See Section 6.9.4.1.
00 = 75Ω
01 = 100Ω
10 = 110Ω
11 = 120Ω

Bit 3: Receiver Turns Ratio (RTR). See Section 6.9.4.1.
0 = Receiver transformer turns ratio is 1:1
1 = Receiver transformer turns ratio is 2:1. This option should only be used in short haul applications.

Bit 2 : Receiver Monitor Mode Enable (RMONEN). In DS1, E1 and 2048 kHz modes this field enables and disables monitor mode. In 6312 kHz mode, this field has no effect. See Section 6.9.4.1.
0 = Disable receive monitor mode
1 = Enable receiver monitor mode. Flat gain is added with the maximum sensitivity. The receiver sensitivity is determined by RSMS[1:0].

Bits 1 to 0: Receiver Sensitivity / Monitor Select (RSMS[1:0]. In DS1, E1 and 2048 kHz modes, this field controls the receiver sensitivity level and additional gain in monitoring applications. The monitor mode (RMONEN=1) adds flat gain to compensate for the signal loss caused by isolation resistors. In 6312 kHz mode this field has no effect. See Section 6.9.4.1.

RMONEN	RSMS [1:0]	RECEIVER MONITOR MODE GAIN (dB)	DS1/E1 RECEIVER SENSITIVITY (MAX CABLE LOSS ALLOWED) (dB)
0	00	0	12
0	01	0	18
0	10	0	30
0	11	0	36 (DS1), 43 (E1)
1	00	14	30
1	01	20	22.5
1	10	26	17.5
1	11	32	12

In 2048kHz mode, the receiver sensitivity numbers are approximately 8dB lower than the E1 values shown in the table.

Register Name: BLCR4
Register Description: BITS LIU Configuration Register 4
Register Address: 13h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	TAIS	—	LLB	ALB	RLB	TPD	RPD	TE
Default	0	0	0	0	0	1	1	0

Bit 7: Transmit AIS (TAIS). This field is ignored in BITS modes other than DS1 and E1. See Section 6.9.4.1.6.
0 = Transmit data normally
1 = Transmit AIS (unframed all-ones) on TTIP and TRING

Bit 5: Local Loopback (LLB). Local loopback loops the output of the transmit formatter back to the input of the receive framer. During this loopback transmit data propagates through the transmit side of the BITS transceiver as it normally would, but the recovered clock and data from the LIU receiver is ignored. See Figure 6-2 for the exact loopback path.
0 = Disabled
1 = Enabled

Bit 4: Analog Loopback (ALB). Analog loopback loops the output of the LIU transmitter back to the input of the LIU receiver. During this loopback transmit data propagates through the transmit side of the BITS transceiver as it normally would, but the incoming signal on RTIP/RRING is ignored. See Figure 6-2 for the exact loopback path.
0 = Disabled
1 = Enabled

Bit 3: Remote Loopback (RLB). Remote loopback loops the output of the LIU receiver back to the input of the LIU transmitter. During this loopback received data propagates through the receive side of the BITS transceiver as it normally would, but the output from the transmit formatter is ignored. See Figure 6-2 for the exact loopback path. (Note: A remote loopback of the recovered clock can also be accomplished by setting BCCR1:TCLKS[3:0] = 1110 to connect RCLK to TCLK. See Figure 6-2 and Figure 6-4.)
0 = Disabled
1 = Enabled

Bit 2: Transmitter Power Down (TPD). Table 9-2 indicates the reduction in supply current when the transmitter is powered down. Note that the transmitter takes approximately 50ms to stabilize after TPD is set to 0. See Section 6.9.4.2.
0 = Normal transmitter operation
1 = Power down the transmitter and put TTIP and TRING pins in a high-impedance state (default)

Bit 1: Receiver Power Down (RPD). Table 9-2 indicates the reduction in supply current when the receiver is powered down. Note that the receiver takes approximately 50ms to stabilize after RPD is set to 0. See Section 6.9.4.1.
0 = Normal receiver operation
1 = Power down the receiver (default)

Bit 0: Transmit Enable (TE). See Section 6.9.4.2.3.
0 = Transmitter output driver disabled; TTIP and TRING pins in a high-impedance state
1 = Transmitter output driver enabled; TTIP and TRING active (THZE1 or THZE2 pin must be low)

Register Name: BLIR1
Register Description: BITS LIU Information Register 1
Register Address: 18h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	RFAIL	OEQ	UEQ	—	OC	SC	LOS
Default	0	0	0	0	0	0	0	0

Bit 6: Receiver Failure (RFAIL). This real-time status bit is set to 1 when the a short-circuit (less than 25Ω) is detected on RTIP and/or RRING.

0 = Normal operation
1 = Short-circuit detected on RTIP and/or RRING

Bit 5: Receive Over-Equalized (OEQ). This real-time status bit is set to 1 when the equalizer in the LIU receiver is over-equalized. This can happen if there is a very large unexpected resistive loss, such as when the device is placed in a monitor mode application without being configured for monitor mode (BLCR3:RMONEN). This indicator provides additional information when the receiver is indicating loss-of-signal in the LOS status bit. See Section 6.9.4.1.

Bit 4: Receive Under-Equalized (UEQ). This real-time status bit is set to 1 when the equalizer in the LIU receiver is under-equalized. A signal with a very high resistive gain is being applied. This indicator provides additional information when the receiver is indicating loss-of-signal in the LOS status bit. See Section 6.9.4.1.

Bit 2: Transmit Open Circuit (OC). This real-time status bit is set to 1 when the LIU detects that the TTIP and TRING outputs are open-circuited. Register BLSR1 has latched status bits that are set when OC changes state, both low-to-high and high-to-low. See Section 6.9.4.1.6.

Bit 1: Transmit Short Circuit (SC). This real-time status bit is set to 1 when the LIU detects that the TTIP and TRING outputs are short-circuited. The short circuit resistance has to be 25Ω (typically) or less for short circuit detection. Register BLSR1 has latched status bits that are set when SC changes state, both low-to-high and high-to-low. See Section 6.9.4.1.6.

Bit 0: Receive Loss of Signal (LOS). This real-time status bit is set to 1 when the LIU receiver detects an LOS condition at RTIP and RRING. Register BLSR1 has latched status bits that are set when LOS changes state, both low-to-high and high-to-low. See Section 6.9.4.1.

Register Name: BLIR2
Register Description: BITS LIU Information Register 2
Register Address: 19h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	RL[3:0]				—	—	—	—
Default	0	0	0	0	0	0	0	0

Bits 7 to 4: Receive Level (RL[3:0]). This real-time field indicates the pulse amplitude of the signal coming into the BITS LIU receiver. A value of 0 dB means 3.0V for DS1 and 2.37V for E1 and 2048 kHz. In 6312 kHz mode, a value of 0 means 0 dBm. See Section 6.9.4.1.

RL[3:0]	RECEIVE LEVEL (dB)
0000	> -2.5
0001	-2.5 to -5.0
0010	-5.0 to -7.5
0011	-7.5 to -10.0
0100	-10.0 to -12.5
0101	-12.5 to -15.0
0110	-15.0 to -17.5
0111	-17.5 to -20.0
1000	-20 to -22.5
1001	-22.5 to –25.0
1010	-25.0 to –27.5
1011	-27.5 to –30.0
1100	-30.0 to –32.5
1101	-32.5 to –35.0
1110	-35.0 to –37.5
1111	<-37.5

Register Name: BLSR1
Register Description: BITS LIU Status Register 1
Register Address: 1Ah

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	OCC	SCC	LOSC	—	OC	SC	LOS
Default	0	0	0	0	0	0	0	0

Bit 6: Transmit Open Circuit Clear (OCC). This latched status bit is set to 1 when BLIR1:OC changes state from high to low. OCC is cleared when written with a 1. When OCC is set it can cause an interrupt request on the INTREQ pin if the OCC interrupt enable bit is set in the BLIER1 register. See Section 6.9.4.1.6.

Bit 5: Transmit Short Circuit Clear (SCC). This latched status bit is set to 1 when BLIR1:SC changes state from high to low. SCC is cleared when written with a 1. When SCC is set it can cause an interrupt request on the INTREQ pin if the SCC interrupt enable bit is set in the BLIER1 register. See Section 6.9.4.1.6.

Bit 4: Receive Loss of Signal Clear (LOSC). This latched status bit is set to 1 when BLIR1:LOS changes state from high to low. LOSC is cleared when written with a 1. When LOSC is set it can cause an interrupt request on the INTREQ pin if the LOSC interrupt enable bit is set in the BLIER1 register. See Section 6.9.4.1.

Bit 2: Transmit Open Circuit Detect (OC). This latched status bit is set to 1 when BLIR1:OC changes state from low to high. OC is cleared when written with a 1. When OC is set it can cause an interrupt request on the INTREQ pin if the OC interrupt enable bit is set in the BLIER1 register. See Section 6.9.4.2.7.

Bit 1: Transmit Short Circuit Detect (SC). This latched status bit is set to 1 when BLIR1:SC changes state from low to high. SC is cleared when written with a 1. When SC is set it can cause an interrupt request on the INTREQ pin if the SC interrupt enable bit is set in the BLIER1 register. See Section 6.9.4.2.6.

Bit 0: Receive Loss of Signal Detect (LOS). This latched status bit is set to 1 when BLIR1:LOS changes state from low to high. LOS is cleared when written with a 1. When LOS is set it can cause an interrupt request on the INTREQ pin if the LOS interrupt enable bit is set in the BLIER1 register. See Section 6.9.4.1.6.

Register Name: BLIER1
Register Description: BITS LIU Interrupt Enable Register 1
Register Address: 1Bh

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	OCC	SCC	LOSC	—	OC	SC	LOS
Default	0	0	0	0	0	0	0	0

Bit 6: Interrupt Enable for Transmit Open Circuit Clear (OCC). This bit is an interrupt enable for the OCC bit in the BLSR1 register.
0 = Mask the interrupt
1 = Enable the interrupt

Bit 5: Interrupt Enable for Transmit Short Circuit Clear (SCC). This bit is an interrupt enable for the SCC bit in the BLSR1 register.
0 = Mask the interrupt
1 = Enable the interrupt

Bit 4: Interrupt Enable for Receive Loss of Signal Clear (LOSC). This bit is an interrupt enable for the LOSC bit in the BLSR1 register.
0 = Mask the interrupt
1 = Enable the interrupt

Bit 2: Interrupt Enable for Transmit Open Circuit Detect (OC). This bit is an interrupt enable for the OC bit in the BLSR1 register.
0 = Mask the interrupt
1 = Enable the interrupt

Bit 1: Interrupt Enable for Transmit Short Circuit Detect (SC). This bit is an interrupt enable for the SC bit in the BLSR1 register.
0 = Mask the interrupt
1 = Enable the interrupt

Bit 0: Interrupt Enable for Receive Loss of Signal (LOS). This bit is an interrupt enable for the LOS bit in the BLSR1 register.
0 = Mask the interrupt
1 = Enable the interrupt

Register Name: BRMMR
Register Description: BITS Receive Master Mode Register
Register Address: 20h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	REN	RID	—	—	—	—	RRST	RT1E1
Default	0	0	0	0	0	0	0	0

These register fields affect the receive framer only. See Sections 6.9.5.1 and 6.9.6.1.

Bit 7: Receive Framer Enable (REN). This bit must be written with the desired value prior to setting the RID bit.
0 = Receive framer disabled (held in low-power state)
1 = Receive framer enabled (all features active)

Bit 6: Receive Initialization Done (RID). System software must set the RT1E1 and REN bits prior to setting this bit. Once RID is set, the receiver is enabled if REN = 1.

Bit 1: Receive Soft Reset (RRST). Level-sensitive reset. Should be set to 1, then to 0 to reset and initialize the receive framer.
0 = Normal operation
1 = Hold the receive framer in reset

Bit 0: Receive T1/E1 Mode Select (RT1E1). This bit specifies the operating mode for the receive framer only. The BTMMR:TT1E1 bit specifies the operating mode for the transmit formatter. This bit must be set to the desired value before setting the RID bit.
0 = T1 (DS1) operation
1 = E1 operation

Register Name: BTMMR
Register Description: BITS Transmit Master Mode Register
Register Address: 21h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	TEN	TID	—	—	—	—	TRST	TT1E1
Default	0	0	0	0	0	0	0	0

These register fields affect the transmit formatter only. See Sections 6.9.5.2 and 6.9.6.2.

Bit 7: Transmit Formatter Enable (TEN). This bit must be written with the desired value prior to setting the TID bit.

0 = Transmit formatter disabled (held in low-power state)
1 = Transmit formatter enabled (all features active)

Bit 6: Transmit Initialization Done (TID). System software must set the TT1E1 and TEN bits prior to setting this bit. Once TID is set, the transmitter is enabled if TEN = 1.

Bit 1: Transmit Soft Reset (TRST). Level-sensitive reset. Should be set to 1, then to 0 to reset and initialize the transmit formatter.

0 = Normal operation
1 = Hold the transmit formatter in reset

Bit 0: Transmit T1/E1 Mode Select (TT1E1). This bit specifies the operating mode for the transmit formatter only. The BRMMR:RT1E1 bit specifies the operating mode for the receive framer. This bit must be set to the desired value before setting the TID bit.

0 = T1 (DS1) operation
1 = E1 operation

Register Name: BRCR1
Register Description: BITS Receive Configuration Register 1 (DS1 only)
Register Address: 22h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	SYNCT	RB8ZS	RFM	ARC	SYNCC	RJC	SYNCD	RESYNC
Default	0	0	0	0	0	0	0	0

The fields of this register configure the receive framer when it is in DS1 mode only (BRMMR:RT1E1=0). In E1 mode this register is reserved and should not be written. See Section 6.9.5.1.

Bit 7: Sync Time (SYNCT). This bit specifies the number of framing bits to quality. The type of framing bits to qualify is specified by the SYNCC configuration bit.

0 = Qualify 10 bits
1 = Qualify 24 bits

Bit 6: Receive B8ZS Enable (RB8ZS).

0 = B8ZS decoding disabled
1 = B8ZS decoding enabled

Bit 5: Receive Frame Mode Select (RFM).

0 = ESF framing mode
1 = SF (D4) framing mode

Bit 4: Auto Resync Criteria (ARC).

0 = Resync on OOF or LOS event
1 = Resync on OOF only

Bit 3: Sync Criteria (SYNCC).

Superframe (SF) mode
0 = Search for Ft pattern then search for Fs pattern
1 = Cross-couple Ft and Fs pattern

Extended Superframe (ESF) framing mode
0 = Search for FPS pattern only
1 = Search for FPS and verify with CRC6

Bit 2: Receive Japanese CRC-6 Enable (RJC).

0 = use ANSI/AT&T/ITU CRC-6 calculation (normal DS1 operation)
1 = use Japanese standard JT-G704 CRC-6 calculation (for J1 operation)

Bit 1: Sync Disable (SYNCD). The bit specifies whether or not the receive framer automatically attempts to resynchronize to (i.e. search for the start-of-frame in) the incoming signal.

0 = Auto resync enabled
1 = Auto resync disabled

Bit 0: Resynchronize (RESYNC). A zero-to-one transition causes the receive framer to resynchronize to (i.e. search for the start of frame in) the incoming signal. RESYNC must be cleared and set again for a subsequent resync.

Register Name: BRCR2
Register Description: BITS Receive Configuration Register 2 (DS1 only)
Register Address: 23h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	—	—	—	OOFC[1:0]		RAIIE	RSFRAI
Default	0	0	0	0	0	0	0	0

The fields of this register configure the receive framer when it is in DS1 mode only (BRMMR:RT1E1=0). In E1 mode this register is reserved and should not be written. See Section 6.9.5.1.

Bits 3 to 2: Out of Frame Criteria (OOFC[1:0]). This field specifies the criteria for declaring an out-of-frame (OOF) defect in BRIR1:OOF.

00 = 2/4 frame bits in error
01 = 2/5 frame bits in error
10 = 2/6 frame bits in error
11 = 2/6 frame bits in error

Bit 1: Receive RAI Integration Enable (RAIIE). The ESF RAI indication can be interrupted for a period not to exceed 100 ms per interruption (T1.403). In ESF mode, setting RAIIE causes the RAI status to be integrated for 200ms. The RAI defect is indicated in BRIR1:RAI.

0 = RAI declared when 16 consecutive patterns of 00FFh appear in the FDL.
RAI cleared when 14 or less patterns of 00FFh out of 16 possible appear in the FDL.
1 = RAI declared when the condition has been present for greater than 200ms.
RAI cleared when the condition has been absent for greater than 200ms.

Bit 0: Receive Superframe RAI Select (RSFRAI). When the receive framer is in superframe mode this bit specifies the type of RAI signal to detect.

0 = Zeros in bit 2 of all channels (normal DS1 operation)
1 = A one in the Fs bit position of frame 12 (J1 operation)

Register Name: BRCR3
Register Description: BITS Receive Configuration Register 3 (E1 only)
Register Address: 24h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	RHDB3	RSIGM	—	RCRC4	FRC	SYNCD	RESYNC
Default	0	0	0	0	0	0	0	0

The fields of this register configure the receive framer when it is in E1 mode only (BRMMR:RT1E1=1). In DS1 mode this register is reserved and should not be written. See Section 6.9.6.1.

Bit 6: Receive HDB3 Enable (RHDB3).
0 = HDB3 decoding disabled
1 = HDB3 decoding enabled

Bit 5 : Receive Signaling Mode Select (RSIGM).
0 = CAS signaling mode
1 = CCS signaling mode

Bit 3: Receive CRC-4 Enable (RCRC4).
0 = CRC-4 framing disabled
1 = CRC-4 framing enabled

Bit 2: Frame Resync Criteria (FRC).
0 = Resync if FAS is received in error three consecutive times
1 = Resync if either FAS or bit 2 of non-FAS is received in error three consecutive times

Bit 1: Sync Disable (SYNCD). The bit specifies whether or not the receive framer automatically attempts to resynchronize to (i.e. search for the start-of-frame in) the incoming signal.
0 = Auto resync enabled
1 = Auto resync disabled

Bit 0: Resynchronize (RESYNC). A zero-to-one transition causes the receive framer to resynchronize to (i.e. search for the start of frame in) the incoming signal. RESYNC must be cleared and set again for a subsequent resync.

Register Name: BRCR4
Register Description: BITS Receive Configuration Register 4 (E1 only)
Register Address: 25h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	—	—	—	—	—	—	RLOSC
Default	0	0	0	0	0	0	0	0

The fields of this register configure the receive framer when it is in E1 mode only (BRMMR:RT1E1=1). In DS1 mode this register is reserved and should not be written. See Section 6.9.6.1.

Bit 0: Receive Loss of Signal Criteria (RLOSC).
0 = RLOS declared upon 255 consecutive zeros (125 μs)
1 = RLOS declared upon 2048 consecutive zeros (1 ms)

Register Name: BRCR5
Register Description: BITS Receive Configuration Register 5 (DS1 and E1)
Register Address: 26h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	—	—	—	—	—	RMFS	1
Default	0	0	0	0	0	0	0	1

Bit 1: Receive Multiframe Sync Mode (RMFS). In E1 mode, this bit specifies the type of multiframe sync that comes out of the receive framer on the RMFSYNC node (Figure 6-2). In DS1 mode this bit must be set to 0. See Section 6.9.2.

0 = Pulse on CAS multiframe boundary
1 = Pulse on CRC-4 multiframe boundary

Bit 0: Leave set to one (test control).

Register Name: BTCR1
Register Description: BITS Transmit Configuration Register 1 (DS1 only)
Register Address: 27h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	TJC	TFPT	TCPT	—	—	TB8ZS	TAIS	TRAI
Default	0	0	0	0	0	0	0	0

The fields of this register configure the transmit formatter when it is in DS1 mode only (BTMMR:TT1E1=0). In E1 mode this register is reserved and should not be written. See Section 6.9.5.2.

Bit 7: Transmit Japanese CRC-6 Enable (TJC).
0 = Use ANSI/AT&T/ITU CRC-6 calculation (normal DS1 operation)
1 = Use Japanese standard JT-G704 CRC-6 calculation (J1 operation)

Bit 6: Transmit F-Bit Pass-Through (TFPT).
0 = F bits sourced internally
1 = F bits sourced from TSER pin

Bit 5: Transmit CRC Pass-Through (TCPT).
0 = CRC-6 bits sourced internally
1 = CRC-6 bits sourced from TSER pin during F-bit time

Bit 2: Transmit B8ZS Enable (TB8ZS).
0 = B8ZS encoding disabled
1 = B8ZS encoding enabled

Bit 1: Transmit Alarm Indication Signal (TAIS).
0 = Do not transmit AIS
1 = Transmit AIS (unframed all-ones)

Bit 0: Transmit Remote Alarm Indication (TRAI).
0 = Do not transmit RAI
1 = Transmit RAI

Register Name: BTCR2
Register Description: BITS Transmit Configuration Register 2 (DS1 only)
Register Address: 28h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	—	—	FBCT2	FBCT1	TSFRAI	TPDE	TB7ZS
Default	0	0	0	0	0	0	0	0

The fields of this register configure the transmit formatter when it is in DS1 mode only (BTMMR:TT1E1=0). In E1 mode this register is reserved and should not be written. See Section 6.9.5.2.

Bit 4: F-Bit Corruption Type 2 (FBCT2). Setting this bit to 1 enables the corruption of one out of every 128 Ft bits (SF framing mode) or one out of every 128 FPS bits (ESF framing mode). F-bit corruption continues as long as FBCT2=1.

Bit 3: F-Bit Corruption Type 1 (FBCT1). A zero-to-one transition causes the next three consecutive Ft bits (SF framing mode) or FPS bits (ESF framing mode) to be corrupted. This corruption is sufficient to cause the remote end to experience a loss of frame synchronization.

Bit 2: Transmit Superframe RAI Select (TSFRAI). When the transmit formatter is in superframe mode this bit specifies the type of RAI signal to transmit.

0 = Zeros in bit 2 of all channels (normal DS1 operation)
1 = A one in the Fs bit position of frame 12 (J1 operation)

Bit 1: Pulse Density Enforcer Enable (TPDE). The framer always examines both the transmit and receive data streams for violations of the ANSI T1.403 pulse density rules: no more than 15 consecutive zeros and at least N ones in each and every time window of 8 x (N +1) bits where N = 1 through 23. Violations for the transmit and receive data streams are reported in the BTSR1:TPDV and BRSR2:RPDV bits respectively. When this bit is set to one, the transmit formatter will force the transmitted stream to meet this requirement no matter the content of the transmitted stream. When B8ZS encoding is enabled (BTCR1:TB8ZS=1), this bit should be set to zero since B8ZS-encoded data streams cannot violate the pulse density requirements.

0 = Disable transmit pulse density enforcer
1 = Enable transmit pulse density enforcer

Bit 0: Transmit Bit 7 Zero-Suppression Enable (TB7ZS).

0 = No stuffing occurs
1 = Bit 7 forced to 1 in channels with all zeros

Register Name: BTCR3
Register Description: BITS Transmit Configuration Register 3 (DS1 and E1)
Register Address: 29h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	—	—	—	—	TFM	IBPV	—
Default	0	0	0	0	0	0	0	0

Bit 2: Transmit Frame Mode Select (TFM). In DS1 mode, this field specifies the DS1 framing mode. In E1 mode this field is unused and must be written with 0. See Section 6.9.5.2.

0 = ESF framing mode
1 = SF (D4) framing mode

Bit 1: Insert BPV (IBPV). A zero-to-one transition on this bit will cause a single bipolar violation (BPV) to be inserted into the transmit data stream. After this bit has been toggled from a 0 to a 1, the device waits for the next occurrence of three consecutive ones to insert the BPV. This bit must be cleared and set again for a subsequent error to be inserted. See Sections 6.9.5.2 and 6.9.6.2.

Register Name: BTCR4
Register Description: BITS Transmit Configuration Register 4 (E1 only)
Register Address: 2Ah

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	TFPT	—	—	TSiS	—	THDB3	TAIS	TCRC4
Default	0	0	0	0	0	0	0	0

The fields of this register configure the transmit formatter when it is in E1 mode only (BTMMR:TT1E1=1). In DS1 mode this register is reserved and should not be written. See Section 6.9.6.2.

Bit 7: Transmit Time Slot 0 Formatter Pass-Through (TFPT). See Figure 6-11 for the relative priority of this control bit vs. other control fields.

0 = FAS bits/Si bits/Sa bits/RAI sourced internally from the BTAF and BTNAF registers
1 = FAS bits/Si bits/Sa bits/RAI sourced from TSER pin

Bit 4: Transmit International Bit Select (TSiS). See Figure 6-11 for the relative priority of this control bit vs. other transmit formatter control fields.

0 = Sample Si bits at TSER pin
1 = Source Si bits from the BTAF and BTNAF registers (in this mode, TFPT must be set to 0)

Bit 2: Transmit HDB3 Enable (THDB3).

0 = HDB3 encoding disabled
1 = HDB3 encoding enabled

Bit 1: Transmit Alarm Indication Signal (TAIS).

0 = Do not transmit AIS
1 = Transmit AIS (unframed all-ones)

Bit 0: Transmit CRC-4 Enable (TCRC4).

0 = CRC-4 framing mode disabled
1 = CRC-4 framing mode enabled

Register Name: BRIIR
Register Description: BITS Receive Interrupt Information Register
Register Address: 30h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	BRSR4	—	—	—	—	BRSR3	BRSR1
Default	0	0	0	0	0	0	0	0

This register provide an indication of which BITS receive status registers have status bits set. When an interrupt request occurs, software can read BRIIR to quickly identify which of the BITS receive status registers might be causing the interrupt request. These bits clear once the appropriate interrupt request source has been serviced and cleared, as long as no other interrupt condition is present in the associated status register. Status bits that have been masked via the interrupt enable registers have no effect on these interrupt information bits.

Bit 6: BITS Receive Status Register 4 (BRSR4).
0 = No status bits set
1 = Status bits set

Bit 1: BITS Receive Status Register 3 (BRSR3).
0 = No status bits set
1 = Status bits set

Bit 0: BITS Receive Status Register 1 (BRSR1).
0 = No status bits set
1 = Status bits set

Register Name: BRIR1
Register Description: BITS Receive Information Register 1 (DS1 and E1)
Register Address: 31h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	—	—	—	RAI	AIS	LOS	OOF
Default	0	0	0	0	0	0	0	0

These fields provide real-time status information from the receive framer. See Table 6-6 (DS1) and Table 6-7 (E1) for set and clear criteria for RAI, AIS, LOS and OOF. The BRSR1 register has corresponding latched status registers.

Bit 3: Remote Alarm Indication Condition (RAI).
0 = RAI not detected
1 = RAI detected

Bit 2: Alarm Indication Signal Condition (AIS).
0 = AIS not detected
1 = AIS detected

Bit 1: Loss of Signal Condition (LOS).
0 = LOS not detected
1 = LOS detected

Bit 0: Out of Frame Condition (OOF).
0 = OOF not detected
1 = OOF detected

Register Name: BRIR2
Register Description: BITS Receive Information Register 2 (E1 only)
Register Address: 32h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	CSC[5:2,0]					CRC4SA	CASSA	FASSA
Default	0	0	0	0	0	0	0	0

The fields of this register provide real-time status information from the receive framer when it is in E1 mode only (BRMMR:RT1E1=1). In DS1 mode these fields are undefined. See Section 6.9.6.1.

Bits 7 to 3: CRC-4 Sync Counter bits (CSC[5:2] and CSC[0]). The CRC-4 sync counter increments each time the 8 ms CRC-4 multi-frame search times out. The counter is cleared when the framer has successfully obtained CRC-4 multiframe synchronization. The counter can also be cleared by disabling the CRC4 mode (BRCR3:RCRC4 = 0). This counter is useful for determining the amount of time the framer has been searching for synchronization at the CRC-4 level. ITU G.706 suggests that if synchronization at the CRC-4 level cannot be obtained within 400 ms, then the search should be abandoned and proper action taken. The CRC-4 sync counter rolls over when it reaches its maximum value. CSC[0] is the LSB of the 6-bit counter. (Note**:** The second LSB, CSC[1], is not accessible in this register to allow resolution to >400ms using 5 bits.)

Bit 2: FAS Sync Active (FASSA). This real-time information bit is set while the synchronizer is searching for alignment at the FAS level.

Bit 1: CAS MF Sync Active (CASSA). This real-time information bit is set while the synchronizer is searching for the CAS multi-frame alignment word.

Bit 0: CRC-4 MF Sync Active (CRC4SA). This real-time information bit is set while the synchronizer is searching for the CRC-4 multi-frame alignment word.

Register Name: BRSR1
Register Description: BITS Receive Status Register 1 (DS1 and E1)
Register Address: 33h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	RAIC	AISC	LOSC	OOFC	RAI	AIS	LOS	OOF
Default	0	0	0	0	0	0	0	0

See Table 6-6 (DS1) and Table 6-7 (E1) for set and clear criteria for RAI, AIS, LOS and OOF.

Bit 7: Remote Alarm Indication Clear (RAIC). This latched status bit is set to 1 when BRIR1:RAI changes state from high to low. RAIC is cleared when written with a 1. When RAIC is set it can cause an interrupt request on the INTREQ pin if the RAIC interrupt enable bit is set in the BRIER1 register.

Bit 6: Alarm Indication Signal Clear (AISC). This latched status bit is set to 1 when BRIR1:AIS changes state from high to low. AISC is cleared when written with a 1. When AISC is set it can cause an interrupt request on the INTREQ pin if the AISC interrupt enable bit is set in the BRIER1 register.

Bit 5: Loss of Signal Clear (LOSC). This latched status bit is set to 1 when BRIR1:LOS changes state from high to low. LOSC is cleared when written with a 1. When LOSC is set it can cause an interrupt request on the INTREQ pin if the LOSC interrupt enable bit is set in the BRIER1 register.

Bit 4: Out of Frame Clear (OOFC). This latched status bit is set to 1 when BRIR1:OOF changes state from high to low. OOFC is cleared when written with a 1. When OOFC is set it can cause an interrupt request on the INTREQ pin if the OOFC interrupt enable bit is set in the BRIER1 register.

Bit 3: Remote Alarm Indication (RAI). This latched status bit is set to 1 when BRIR1:RAI changes state from low to high. RAI is cleared when written with a 1. When RAI is set it can cause an interrupt request on the INTREQ pin if the RAI interrupt enable bit is set in the BRIER1 register.

Bit 2: Alarm Indication Signal (AIS). This latched status bit is set to 1 when BRIR1:AIS changes state from low to high. AIS is cleared when written with a 1. When AIS is set it can cause an interrupt request on the INTREQ pin if the AIS interrupt enable bit is set in the BRIER1 register.

Bit 1: Loss of Signal (LOS). This latched status bit is set to 1 when BRIR1:LOS changes state from low to high. LOS is cleared when written with a 1. When LOS is set it can cause an interrupt request on the INTREQ pin if the LOS interrupt enable bit is set in the BRIER1 register. See also the Receive Sensitivity paragraph in Section 6.9.4.1.6.

Bit 0: Out of Frame (OOF). This latched status bit is set to 1 when BRIR1:OOF changes state from low to high. OOF is cleared when written with a 1. When OOF is set it can cause an interrupt request on the INTREQ pin if the OOF interrupt enable bit is set in the BRIER1 register.

Register Name: BRIER1
Register Description: BITS Receive Interrupt Enable Register 1 (DS1 and E1)
Register Address: 34h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	RAIC	AISC	LOSC	OOFC	RAI	AIS	LOS	OOF
Default	0	0	0	0	0	0	0	0

Bit 7: Interrupt Enable for Remote Alarm Indication Clear (RAIC). This bit is an interrupt enable for the RAIC bit in the BRSR1 register.
0 = Mask the interrupt
1 = Enable the interrupt

Bit 6: Interrupt Enable for Alarm Indication Signal Clear (AISC). This bit is an interrupt enable for the AISC bit in the BRSR1 register.
0 = Mask the interrupt
1 = Enable the interrupt

Bit 5: Interrupt Enable for Loss of Signal Clear (LOSC). This bit is an interrupt enable for the LOSC bit in the BRSR1 register.
0 = Mask the interrupt
1 = Enable the interrupt

Bit 4: Interrupt Enable for Out of Frame Clear (OOFC). This bit is an interrupt enable for the OOFC bit in the BRSR1 register.
0 = Mask the interrupt
1 = Enable the interrupt

Bit 3: Interrupt Enable for Remote Alarm Indication (RAI). This bit is an interrupt enable for the RAI bit in the BRSR1 register.
0 = Mask the interrupt
1 = Enable the interrupt

Bit 2: Interrupt Enable for Alarm Indication Signal (AIS). This bit is an interrupt enable for the AIS bit in the BRSR1 register.
0 = Mask the interrupt
1 = Enable the interrupt

Bit 1: Interrupt Enable for Loss of Signal (LOS). This bit is an interrupt enable for the LOS bit in the BRSR1 register.
0 = Mask the interrupt
1 = Enable the interrupt

Bit 0: Interrupt Enable for Out of Frame (OOF). This bit is an interrupt enable for the OOF bit in the BRSR1 register.
0 = Mask the interrupt
1 = Enable the interrupt

Register Name: BRSR2
Register Description: BITS Receive Status Register 2 (DS1 only)
Register Address: 35h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	RPDV	—	COFA	8ZD	16ZD	SEFE	B8ZS	FBE
Default	0	0	0	0	0	0	0	0

The fields of this register provide latched status information from the receive framer when it is in DS1 mode (BRMMR:RT1E1=0). In E1 mode these fields are undefined. None of these latched status bits can cause an interrupt request. See Section 6.9.5.1.

Bit 7: Receive Pulse Density Violation Event (RPDV). This latched status bit is set to 1 when the incoming receive data stream does not meet the pulse density requirements of T1.403: no more than 15 consecutive zeros and at least N ones in each and every time window of 8 x (N +1) bits where N = 1 through 23. RPDV is cleared when written with a 1.

Bit 5: Change-of-Frame Alignment Event (COFA). This latched status bit is set to 1 when the last resync resulted in a change of frame or multiframe alignment. COFA is cleared when written with a 1.

Bit 4: Eight Zero Detect Event (8ZD). This latched status bit is set to 1 when a string of at least eight consecutive zeros (regardless of the length of the string) have been received in the incoming signal. 8ZD is cleared when written with a 1.

Bit 3: Sixteen Zero Detect Event (16ZD). This latched status bit is set to 1 when a string of at least 16 consecutive zeros (regardless of the length of the string) have been received in the incoming signal. 16ZD is cleared when written with a 1.

Bit 2: Severely Errored Framing Event (SEFE). This latched status bit is set to 1 when 2 out of 6 framing bits (Ft or FPS) are received in error. SEFE is cleared when written with a 1.

Bit 1: B8ZS Codeword Detect Event (B8ZS). This latched status bit is set to 1 when a B8ZS codeword is detected in the incoming signal, regardless of whether the B8ZS mode is selected or not. This bit enables systems to automatically setting the line coding. B8ZS is cleared when written with a 1.

Bit 0: Frame Bit Error Event (FBE). This latched status bit is set to 1 when an Ft (D4) or FPS (ESF) framing bit is received in error. FBE is cleared when written with a 1.

Register Name: BRSR3
Register Description: BITS Receive Status Register 3 (E1 only)
Register Address: 36h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	CRCRC	CASRC	FASRC	RSA1	RSA0	RCMF	RAF
Default	0	0	0	0	0	0	0	0

The fields of this register provide latched status information from the receive framer when it is in E1 mode only (BRMMR:RT1E1=1). In DS1 mode these fields are undefined. See Section 6.9.6.1.

Bit 6: CRC-4 Resync Criteria Met (CRCRC). This latched status bit is set to 1 when 915 out of 1000 CRC-4 multiframe alignment words are received in error. CRCRC is cleared when written with a 1 and not set again until the CRC resync criteria is met again. CRCRC cannot cause an interrupt request.

Bit 5: CAS Resync Criteria Met (CASRC). This latched status bit is set to 1 when two consecutive CAS multi-frame alignment words are received in error. CASRC is cleared when written with a 1 and not set again until the CAS resync criteria is met again. CASRC cannot cause an interrupt request.

Bit 4: FAS Resync Criteria Met (FASRC). This latched status bit is set to 1 when three consecutive FAS words are received in error. FASRC is cleared when written with a 1 and not set again until the FAS resync criteria is met again. FASRC cannot cause an interrupt request.

Bit 3: Receive Signaling All Ones Event (RSA1). This latched status bit is set to 1 when timeslot 16 contains fewer than three zeros for 16 consecutive frames. RSA1 is cleared when written with a 1. When RSA1 is set it can cause an interrupt request on the INTREQ pin if the RSA1 interrupt enable bit is set in the BRIER3 register. In all other modes RSA1 remains set to 0.

Bit 2: Receive Signaling All Zeros Event (RSA0). This latched status bit is set to 1 when timeslot 16 contains all zeros over a full multi-frame. RSA0 is cleared when written with a 1. When RSA0 is set it can cause an interrupt request on the INTREQ pin if the RSA0 interrupt enable bit is set in the BRIER3 register. In all other modes RSA0 remains set to 0.

Bit 1: Receive CRC-4 Multi-Frame (RCMF). This latched status bit is set to 1 every 2 ms on CRC-4 multiframe boundaries. RCMF is cleared when written with a 1. When RCMF is set it can cause an interrupt request on the INTREQ pin if the RCMF interrupt enable bit is set in the BRIER3 register. In all other modes RCMF remains set to 0. See Section 6.9.6.4.

Bit 0: Receive Align Frame (RAF). This latched status bit is set to 1 every 250 µs at the beginning of align frames. RAF is cleared when written with a 1. When RAF is set it can cause an interrupt request on the INTREQ pin if the RAF interrupt enable bit is set in the BRIER3 register. In all other modes RAF remains set to 0. See Section 6.9.6.3.

Register Name: BRIER3
Register Description: BITS Receive Interrupt Enable Register 3 (E1 only)
Register Address: 37h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	—	—	—	RSA1	RSA0	RCMF	RAF
Default	0	0	0	0	0	0	0	0

The fields of this register configure interrupt masking for the corresponding bits in the BRSR3 register when the receive framer is in E1 mode only (BRMMR:RT1E1=1). In DS1 mode this register is reserved and should not be written. See Section 6.9.6.1.

Bit 3: Interrupt Enable for Receive Signaling All Ones Event (RSA1). This bit is an interrupt enable for the RSA1 bit in the BRSR3 register.
0 = Mask the interrupt
1 = Enable the interrupt

Bit 2: Interrupt Enable for Receive Signaling All Zeros Event (RSA0). This bit is an interrupt enable for the RSA0 bit in the BRSR3 register.
0 = Mask the interrupt
1 = Enable the interrupt

Bit 1: Interrupt Enable for Receive CRC-4 Multi-Frame (RCMF). This bit is an interrupt enable for the RCMF bit in the BRSR3 register.
0 = Mask the interrupt
1 = Enable the interrupt

Bit 0: Interrupt Enable for Receive Align Frame (RAF). This bit is an interrupt enable for the RAF bit in the BRSR3 register.
0 = Mask the interrupt
1 = Enable the interrupt

Register Name: BRSR4
Register Description: BITS Receive Status Register 4 (DS1 only)
Register Address: 38h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	—	—	—	—	—	BC	BD
Default	0	0	0	0	0	0	0	0

The fields of this register provide latched status information from the receive framer when it is in DS1 mode (BRMMR:RT1E1=0). In E1 mode these fields are undefined. See Section 6.9.5.3.

Bit 1: Receive BOC Clear (BC). This latched status bit is set to 1 when a valid BOC is no longer detected, with the disintegration filter applied as specified in BRBCR:RBD[1:0]. BC is cleared when written with a 1. When BC is set it can cause an interrupt request on the INTREQ pin if the BC interrupt enable bit is set in the BRIER4 register.

Bit 0: Receive BOC Detected (BD). This latched status bit is set to 1 when a valid BOC has been detected, with the validation filter applied as specified in BRBCR:RBF. BD is cleared when written with a 1. When BD is set it can cause an interrupt request on the INTREQ pin if the BD interrupt enable bit is set in the BRIER4 register.

Register Name: BRIER4
Register Description: BITS Interrupt Enable Register 4 (DS1 only)
Register Address: 39h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	—	—	—	—	—	BC	BD
Default	0	0	0	0	0	0	0	0

Bit 1: Interrupt Enable for Receive BOC Clear (BC). This bit is an interrupt enable for the BC bit in the BRSR4 register.

0 = Mask the interrupt
1 = Enable the interrupt

Bit 0: Interrupt Enable for Receive BOC Detected (BD). This bit is an interrupt enable for the BD bit in the BRSR4 register.

0 = Mask the interrupt
1 = Enable the interrupt

Register Name: BTSR1
Register Description: BITS Transmit Status Register 1 (DS1 and E1)
Register Address: 3Ah

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	—	—	—	TPDV/TAF	TMF	LOTCC	LOTC
Default	0	0	0	0	0	0	0	0

Bit 3: Transmit Pulse Density Violation (TPDV) / Transmit Align Frame (TAF). In DS1 mode this latched status bit functions as TPDV and is set to 1 when the transmit data stream does not meet the ANSI T1.403 requirements for pulse density: no more than 15 consecutive zeros and at least N ones in each and every time window of 8 x (N +1) bits where N = 1 through 23. In E1 mode this bit functions as TAF and is set to 1 every 250 μs at the beginning of align frames. TPDV/TAF is cleared when written with a 1. When TPDV/TAF is set it can cause an interrupt to occur on the INTREQ pin if the TPDV/TAF interrupt enable bit is set in the BTIER1 register. See Section 6.9.6.3.

Bit 2: Transmit Multi-Frame (TMF). In DS1 mode this latched status bit is set to 1 every 1.5 ms on superframe boundaries (SF mode) or every 3 ms on extended superframe boundaries (ESF mode). In E1 mode this bit is set every 2 ms on multiframe boundaries. TMF is cleared when written with a 1. When TMF is set it can cause an interrupt to occur on the INTREQ pin if the TMF interrupt enable bit is set in the BTIER1 register. See Section 6.9.6.4.

Bit 1: Loss of Transmit Clock Clear (LOTCC). This latched status bit is set to 1 when the transmit clock source has transitioned for approximately 15 MCLK periods. LOTCC is cleared when written with a 1. When LOTCC is set it can cause an interrupt request on the INTREQ pin if the LOTCC interrupt enable bit is set in the BTIER1 register.

Bit 0: Loss of Transmit Clock (LOTC). This latched status bit is set to 1 when the transmit clock source has not transitioned for approximately 15 MCLK periods. LOTC is cleared when written with a 1. When LOTC is set it can cause an interrupt request on the INTREQ pin if the LOTC interrupt enable bit is set in the BTIER1 register.

Register Name: BTIER1
Register Description: BITS Transmit Interrupt Enable Register 1 (DS1 and E1)
Register Address: 3Bh

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	—	—	—	TPDV/TAF	TMF	LOTCC	LOTC
Default	0	0	0	0	0	0	0	0

Bit 3: Interrupt Enable for Transmit Pulse Density Violation (TPDV) / Transmit Align Frame (TAF). This bit is an interrupt enable for the TPDV/TMF bit in the BTSR1 register.
0 = Mask the interrupt
1 = Enable the interrupt

Bit 2: Interrupt Enable for Transmit Multi-Frame (TMF). This bit is an interrupt enable for the TMF bit in the BTSR1 register.
0 = Mask the interrupt
1 = Enable the interrupt

Bit 1: Interrupt Enable for Loss of Transmit Clock Clear (LOTCC). This bit is an interrupt enable for the LOTCC bit in the BTSR1 register.
0 = Mask the interrupt
1 = Enable the interrupt

Bit 0: Interrupt Enable for Loss of Transmit Clock (LOTC). This bit is an interrupt enable for the LOTC bit in the BTSR1 register.
0 = Mask the interrupt
1 = Enable the interrupt

Register Name: BRBCR
Register Description: BITS Receive BOC Control Register (DS1 only)
Register Address: 40h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	RBR	—	RBD[1:0]		RBF[2:0]			—
Default	0	0	0	0	0	0	0	0

When the BITS receive framer is in DS1 ESF mode this register configures the receive BOC controller. In E1 mode this register is reserved and should not be written. See Section 6.9.5.3.

Bit 7: Receive BOC Reset (RBR). A zero-to-one transition resets the BOC circuitry. RBR must be cleared and set again for a subsequent reset. Modifications to the RBF and RBD fields are not applied to the BOC controller until a BOC reset has been completed.

Bits 5 to 4: Receive BOC Disintegration Bits (RBD[1:0]). The receive BOC logic must examine the number of message bits specified by RBD[1:0] before declaring that a valid BOC is no longer detected. The BC bit in BRSR4 is set to indicate that a valid BOC is no longer present.

RBD[1:0]	Consecutive Message Bits for BOC Clear
00	16
01	32
10	48
11	64

Bits 3 to 1: Receive BOC Filter Bits (RBF[2:0]). The receive BOC logic uses the criteria specified by this field to validate incoming BOC codes. The BD bit in BRSR4 is set to indicate the detection of a validated BOC code.

RBF[2:0]	Validation Criteria for BOC Detected
000	1
001	3 in a row
010	5 in a row
011	7 in a row
100	7 out of 10

Register Name: BTBCR
Register Description: BITS Transmit BOC Control Register (DS1 only)
Register Address: 41h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	SBOC	—	—	—	—	—	—
Default	0	0	0	0	0	0	0	0

When the BITS transmitter is in DS1 mode ESF mode this register configures the transmit BOC controller. In all other modes this register is reserved and should not be written. See Section 6.9.5.3.

Bit 6: Send BOC (SBOC).
0 = Do not transmit BOC codes
1 = Repeatedly transmit the BOC code stored in the BTBOC register

Register Name: BRBOC
Register Description: BITS Receive BOC Register (DS1 only)
Register Address: 42h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	—	RBOC[5:0]					
Default	0	0	0	0	0	0	0	0

Bits 5 to 0: Receive BOC (RBOC[5:0]). DS1 ESF mode only. After a BOC has been validated per the criteria specified by BRBCR:RBF, the BOC is stored in this field where it can be read by software. The device notifies software that a valid BOC is available by setting the BD bit in BRSR4. Setting BD can optionally drive an interrupt request on the INTREQ pin. Bit 0 is the first bit received. See Section 6.9.5.3.

Register Name: BTBOC
Register Description: BITS Transmit BOC Register (DS1 only)
Register Address: 43h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	—	TBOC[5:0]					
Default	0	0	0	0	0	0	0	0

Bits 5 to 0: Transmit BOC (TBOC[5:0]). DS1 ESF mode only. This field specifies the six data bits of the 16-bit BOC message to be transmitted in the ESF data link. When SBOC=1 in BTBCR the BOC is repeatedly transmitted on the data link. When SBOC=0, the data link idle code (01111110b = 7Eh) is transmitted continuously on the data link. Bit 0 is the first bit transmitted. See Section 6.9.5.3.

Register Name: BRAF
Register Description: BITS Receive Align Frame Register (E1 only)
Register Address: 50h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Si	FAS[6:0]						
Default	0	0	0	0	0	0	0	0

The align frame is the E1 frame containing the frame alignment signal (FAS). The bits of this register indicate the first eight bits received in the most recent align frame. The bits are latched into this register at the start of the align frame. The start of the align frame is indicated by the RAF status bit in BRSR3. See Section 6.9.6.3.

Bit 7: International Bit (Si).

Bits 6 to 0: Frame Alignment Signal (FAS[6:0]. When a normal E1 signal is being received, FAS[6:0]=0011011.

Register Name: BRNAF
Register Description: BITS Receive Non-Align Frame Register (E1 only)
Register Address: 51h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Si	1	RAI	Sa4	Sa5	Sa6	Sa7	Sa8
Default	0	0	0	0	0	0	0	0

The non-align frame is the E1 frame that does not contain the frame alignment signal (FAS). The bits of this register indicate the first eight bits received in the most recent non-align frame. The bits are latched into this register at the start of the align frame. The start of the align frame is indicated by the RAF status bit in BRSR3. See Section 6.9.6.3.

Bit 7: International Bit (Si).

Bit 6: Non-Align Frame Signal Bit. Set to 1 in a normal E1 double frame.

Bit 5: Remote Alarm Indication (RAI). This is the normal status bit for detecting RAI in the incoming E1 signal.
0 = No alarm condition
1 = Alarm condition

Bits 4 to 0: Additional Spare Bits (Sa4 to Sa8).

Register Name: BRSiAF
Register Description: BITS Receive Si Bits of the Align Frame (E1 only)
Register Address: 52h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	SiF14	SiF12	SiF10	SiF8	SiF6	SiF4	SiF2	SiF0
Default	0	0	0	0	0	0	0	0

The align frame is the E1 frame containing the frame alignment signal (FAS). The bits of this register indicate the Si bits received in the align frames of the most recent CRC-4 multiframe. The Si bits received in each multiframe are saved in internal registers and latched into this register at the start of the next CRC-4 multiframe. The CRC-4 multiframe boundary is indicated by the RCMF status bit in BRSR3. See Section 6.9.6.4.

Bit 7: Si Bit from Frame 14 (SiF14).
Bit 6: Si Bit from Frame 12 (SiF12).
Bit 5: Si Bit from Frame 10 (SiF10).
Bit 4: Si Bit from Frame 8 (SiF8).
Bit 3: Si Bit from Frame 6 (SiF6).
Bit 2: Si Bit from Frame 4 (SiF4).
Bit 1: Si Bit from Frame 2 (SiF2).
Bit 0: Si Bit from Frame 0 (SiF0).

Register Name: BRSiNAF
Register Description: BITS Receive Si Bits of the Non-Align Frame (E1 only)
Register Address: 53h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	SiF15	SiF13	SiF11	SiF9	SiF7	SiF5	SiF3	SiF1
Default	0	0	0	0	0	0	0	0

The non-align frame is the E1 frame that does not contain the frame alignment signal (FAS). The bits of this register indicate the Si bits received in the non-align frames of the most recent CRC-4 multiframe. The Si bits received in each multiframe are saved in internal registers and latched into this register at the start of the next CRC-4 multiframe. The CRC-4 multiframe boundary is indicated by the RCMF status bit in BRSR3. See Section 6.9.6.4.

Bit 7: Si Bit from Frame 15 (SiF15).
Bit 6: Si Bit from Frame 13 (SiF13).
Bit 5: Si Bit from Frame 11 (SiF11).
Bit 4: Si Bit from Frame 9 (SiF9).
Bit 3: Si Bit from Frame 7 (SiF7).
Bit 2: Si Bit from Frame 5 (SiF5).
Bit 1: Si Bit from Frame 3 (SiF3).
Bit 0: Si Bit from Frame 1 (SiF1).

Register Name: BRRAI
Register Description: BITS Receive Remote Alarm Indication Bits (E1 only)
Register Address: 54h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	RAIF15	RAIF13	RAIF11	RAIF9	RAIF7	RAIF5	RAIF3	RAIF1
Default	0	0	0	0	0	0	0	0

The RAI bits received in each multiframe are saved in internal registers and latched into this register at the start of the next CRC-4 multiframe. The CRC-4 multiframe boundary is indicated by the RCMF status bit in BRSR3. See Section 6.9.6.4.

Bit 7: RAI Bit from Frame 15 (RAIF15).
Bit 6: RAI Bit from Frame 13 (RAIF13).
Bit 5: RAI Bit from Frame 11 (RAIF11).
Bit 4: RAI Bit from Frame 9 (RAIF9).
Bit 3: RAI Bit from Frame 7 (RAIF7).
Bit 2: RAI Bit from Frame 5 (RAIF5).
Bit 1: RAI Bit from Frame 3 (RAIF3).
Bit 0: RAI Bit from Frame 1 (RAIF1).

Register Name: BRSa4
Register Description: BITS Receive Sa4 Bits (E1 only)
Register Address: 55h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Sa4F15	Sa4F13	Sa4F11	Sa4F9	Sa4F7	Sa4F5	Sa4F3	Sa4F1
Default	0	0	0	0	0	0	0	0

The Sa4 bits received in each multiframe are saved in internal registers and latched into this register at the start of the next CRC-4 multiframe. The CRC-4 multiframe boundary is indicated by the RCMF status bit in BRSR3. See Section 6.9.6.4.

Bit 7: Sa4 Bit from Frame 15 (Sa4F15).
Bit 6: Sa4 Bit from Frame 13 (Sa4F13).
Bit 5: Sa4 Bit from Frame 11 (Sa4F11).
Bit 4: Sa4 Bit from Frame 9 (Sa4F9).
Bit 3: Sa4 Bit from Frame 7 (Sa4F7).
Bit 2: Sa4 Bit from Frame 5 (Sa4F5).
Bit 1: Sa4 Bit from Frame 3 (Sa4F3).
Bit 0: Sa4 Bit from Frame 1 (Sa4F1).

Register Name: BRSa5
Register Description: BITS Receive Sa5 Bits (E1 only)
Register Address: 56h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Sa5F15	Sa5F13	Sa5F11	Sa5F9	Sa5F7	Sa5F5	Sa5F3	Sa5F1
Default	0	0	0	0	0	0	0	0

The Sa5 bits received in each multiframe are saved in internal registers and latched into this register at the start of the next CRC-4 multiframe. The CRC-4 multiframe boundary is indicated by the RCMF status bit in BRSR3. See Section 6.9.6.4.

Bit 7: Sa5 Bit from Frame 15 (Sa5F15).
Bit 6: Sa5 Bit from Frame 13 (Sa5F13).
Bit 5: Sa5 Bit from Frame 11 (Sa5F11).
Bit 4: Sa5 Bit from Frame 9 (Sa5F9).
Bit 3: Sa5 Bit from Frame 7 (Sa5F7).
Bit 2: Sa5 Bit from Frame 5 (Sa5F5).
Bit 1: Sa5 Bit from Frame 3 (Sa5F3).
Bit 0: Sa5 Bit from Frame 1 (Sa5F1).

Register Name: BRSa6
Register Description: BITS Receive Sa6 Bits (E1 only)
Register Address: 57h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Sa6F15	Sa6F13	Sa6F11	Sa6F9	Sa6F7	Sa6F5	Sa6F3	Sa6F1
Default	0	0	0	0	0	0	0	0

The Sa6 bits received in each multiframe are saved in internal registers and latched into this register at the start of the next CRC-4 multiframe. The CRC-4 multiframe boundary is indicated by the RCMF status bit in BRSR3. See Section 6.9.6.4.

Bit 7: Sa6 Bit from Frame 15 (Sa6F15).
Bit 6: Sa6 Bit from Frame 13 (Sa6F13).
Bit 5: Sa6 Bit from Frame 11 (Sa6F11).
Bit 4: Sa6 Bit from Frame 9 (Sa6F9).
Bit 3: Sa6 Bit from Frame 7 (Sa6F7).
Bit 2: Sa6 Bit from Frame 5 (Sa6F5).
Bit 1: Sa6 Bit from Frame 3 (Sa6F3).
Bit 0: Sa6 Bit from Frame 1 (Sa6F1).

Register Name: BRSa7
Register Description: BITS Receive Sa7 Bits (E1 only)
Register Address: 58h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Sa7F15	Sa7F13	Sa7F11	Sa7F9	Sa7F7	Sa7F5	Sa7F3	Sa7F1
Default	0	0	0	0	0	0	0	0

The Sa7 bits received in each multiframe are saved in internal registers and latched into this register at the start of the next CRC-4 multiframe. The CRC-4 multiframe boundary is indicated by the RCMF status bit in BRSR3. See Section 6.9.6.4.

Bit 7: Sa7 Bit from Frame 15 (Sa7F15).
Bit 6: Sa7 Bit from Frame 13 (Sa7F13).
Bit 5: Sa7 Bit from Frame 11 (Sa7F11).
Bit 4: Sa7 Bit from Frame 9 (Sa7F9).
Bit 3: Sa7 Bit from Frame 7 (Sa7F7).
Bit 2: Sa7 Bit from Frame 5 (Sa7F5).
Bit 1: Sa7 Bit from Frame 3 (Sa7F3).
Bit 0: Sa7 Bit from Frame 1 (Sa7F1).

Register Name: BRSa8
Register Description: BITS Receive Sa8 Bits (E1 only)
Register Address: 59h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Sa8F15	Sa8F13	Sa8F11	Sa8F9	Sa8F7	Sa8F5	Sa8F3	Sa8F1
Default	0	0	0	0	0	0	0	0

The Sa8 bits received in each multiframe are saved in internal registers and latched into this register at the start of the next CRC-4 multiframe. The CRC-4 multiframe boundary is indicated by the RCMF status bit in BRSR3. See Section 6.9.6.4.

Bit 7: Sa8 Bit from Frame 15 (Sa8F15).
Bit 6: Sa8 Bit from Frame 13 (Sa8F13).
Bit 5: Sa8 Bit from Frame 11 (Sa8F11).
Bit 4: Sa8 Bit from Frame 9 (Sa8F9).
Bit 3: Sa8 Bit from Frame 7 (Sa8F7).
Bit 2: Sa8 Bit from Frame 5 (Sa8F5).
Bit 1: Sa8 Bit from Frame 3 (Sa8F3).
Bit 0: Sa8 Bit from Frame 1 (Sa8F1).

Register Name: BRMCR
Register Description: BITS Receive Message Control Register (E1 only)
Register Address: 5Ah

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	SSMCH[2:0]			—	—	SSMF[1:0]	
Default	0	0	0	0	0	0	0	0

Bits 6 to 4: Receive SSM Channel (SSMCH[2:0]). This field specifies the Sa-bit channel to look at when reading the most recently validated SSM message from BRSSM:SSM[3:0]. After this field is changed, the SSM for the newly selected Sa bit channel does not appear in BRSSM:SSM[3:0] for approximately 250µs. See Section 6.9.6.5.

000 = Sa4
001 = Sa5
010 = Sa6
011 = Sa7
100 = Sa8

Bits 1 to 0: Receive SSM Filter (SSMF[1:0]). The logic that detects new SSM messages in the E1 Sa bits uses the criteria specified by this field to validate incoming SSM codes. The Sa4 through Sa8 fields in the BRMSR register are set to indicate the detection of a validated SSM code. See Section 6.9.6.5.

00 = Validate new SSM when present for 1 multiframe
01 = Validate new SSM when present for 2 multiframes in a row
10 = Validate new SSM when present for 3 multiframes in a row
11 = Validate new SSM when present in 3 out of 4 consecutive multiframes

Register Name: BRMSR
Register Description: BITS Receive Message Status Register (E1 only)
Register Address: 5Bh

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—		Sa8	—	Sa7	Sa6	Sa5	Sa4
Default	0	0	0	0	0	0	0	0

Bit 5: New Validated SSM in the Sa8 Bits (Sa8). This latched status bit is set to 1 when a new SSM message has been validated in the Sa8 channel according the criteria specified by BRMCR:SSMF. When Sa8 is set it can cause an interrupt request on the INTREQ pin if the Sa8 interrupt enable bit is set in the BRMCR register. Sa8 is cleared when written with a 1 and not set again until another SSM change is validated in the Sa8 channel. See Section 6.9.6.5.

Bit 3: New Validated SSM in the Sa7 Bits (Sa7). This latched status bit is set to 1 when a new SSM message has been validated in the Sa7 channel according the criteria specified by BRMCR:SSMF. When Sa7 is set it can cause an interrupt request on the INTREQ pin if the Sa7 interrupt enable bit is set in the BRMCR register. Sa7 is cleared when written with a 1 and not set again until another SSM change is validated in the Sa7 channel. See Section 6.9.6.5.

Bit 2: New Validated SSM in the Sa6 Bits (Sa6). This latched status bit is set to 1 when a new SSM message has been validated in the Sa6 channel according the criteria specified by BRMCR:SSMF. When Sa6 is set it can cause an interrupt request on the INTREQ pin if the Sa6 interrupt enable bit is set in the BRMCR register. Sa6 is cleared when written with a 1 and not set again until another SSM change is validated in the Sa6 channel. See Section 6.9.6.5.

Bit 1: New Validated SSM in the Sa5 Bits (Sa5). This latched status bit is set to 1 when a new SSM message has been validated in the Sa5 channel according the criteria specified by BRMCR:SSMF. When Sa5 is set it can cause an interrupt request on the INTREQ pin if the Sa5 interrupt enable bit is set in the BRMCR register. Sa5 is cleared when written with a 1 and not set again until another SSM change is validated in the Sa5 channel. See Section 6.9.6.5.

Bit 0: New Validated SSM in the Sa4 Bits (Sa4). This latched status bit is set to 1 when a new SSM message has been validated in the Sa4 channel according the criteria specified by BRMCR:SSMF. When Sa4 is set it can cause an interrupt request on the INTREQ pin if the Sa4 interrupt enable bit is set in the BRMCR register. Sa4 is cleared when written with a 1 and not set again until another SSM change is validated in the Sa4 channel. See Section 6.9.6.5.

Register Name: BRMIER
Register Description: BITS Receive Message Interrupt Enable Register (E1 only)
Register Address: 5Ch

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	—	Sa8	—	Sa7	Sa6	Sa5	Sa4
Default	0	0	0	0	0	0	0	0

Bit 5: Interrupt Enable for Sa8 (Sa8). This bit is an interrupt enable for the Sa8 status bit in the BRMSR register.
0 = Mask the interrupt
1 = Enable the interrupt

Bit 3: Interrupt Enable for Sa7 (Sa7). This bit is an interrupt enable for the Sa7 status bit in the BRMSR register.
0 = Mask the interrupt
1 = Enable the interrupt

Bit 2: Interrupt Enable for Sa6 (Sa6). This bit is an interrupt enable for the Sa6 status bit in the BRMSR register.
0 = Mask the interrupt
1 = Enable the interrupt

Bit 1: Interrupt Enable for Sa5 (Sa5). This bit is an interrupt enable for the Sa5 status bit in the BRMSR register.
0 = Mask the interrupt
1 = Enable the interrupt

Bit 0: Interrupt Enable for Sa4 (Sa4). This bit is an interrupt enable for the Sa4 status bit in the BRMSR register.
0 = Mask the interrupt
1 = Enable the interrupt

Register Name: BRSSM
Register Description: BITS Receive SSM Register (E1 only)
Register Address: 5Dh

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	SSMCH[2:0]			SSM[3:0]			
Default	0	0	0	0	0	0	0	0

Bits 6 to 4: Receive SSM Channel (SSMCH[2:0]). This field specifies the Sa-bit channel for which the SSM bits are being displayed in the SSM[3:0] field. The value in this field matches the value in BRMCR:SSMCH[2:0] after a delay of approximately 250µs. See Section 6.9.6.5.
000 = Sa4
001 = Sa5
010 = Sa6
011 = Sa7
100 = Sa8

Bits 3 to 0: Receive SSM (SSM[3:0]). This read-only field contains the most recently validated SSM message from the Sa-bit channel indicated in BRSSM:SSMCH[2:0]. The Sa bit channel to display in this field is specified by BRMCR:SSMCH[2:0]. See Section 6.9.6.5.

Register Name: BTAF
Register Description: BITS Transmit Align Frame Register (E1 only)
Register Address: 60h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Si	FAS[6:0]						
Default	0	0	0	1	1	0	1	1

The align frame is the E1 frame containing the frame alignment signal (FAS). The bits of this register specify the first eight bits of the align frame. The bits are sampled from this register at the start of the align frame, which is indicated by the TAF status bit in BTSR1. Various control fields can cause some of these bits to be sourced from elsewhere. See Section 6.9.6.3.

Bit 7: International Bit (Si).

Bits 6 to 0: Frame Alignment Signal (FAS[6:0]. Should be set to 0011011 for normal E1 operation.

Register Name: BTNAF
Register Description: BITS Transmit Non-Align Frame Register (E1 only)
Register Address: 61h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Si	1	RAI	Sa4	Sa5	Sa6	Sa7	Sa8
Default	0	1	0	0	0	0	0	0

The non-align frame is the E1 frame that does not contain the frame alignment signal (FAS). The bits of this register specify the first eight bits of the non-align frame.. The bits are sampled from this register at the start of the align frame, which is indicated by the TAF status bit in BTSR1. Various control fields can cause some of these bits to be sourced from elsewhere. See Section 6.9.6.3.

Bit 7: International Bit (Si).

Bit 6: Non-Align Frame Signal Bit. Should be set to 1 for normal E1 operation.

Bit 5: Remote Alarm Indication (RAI). This is the normal control bit for manipulating the RAI bit in the outgoing E1 frames.

0 = No alarm condition
1 = Alarm condition

Bits 4 to 0: Additional Spare Bits (Sa4 to Sa8).

Register Name: BTSiAF
Register Description: BITS Transmit Si Bits of the Align Frame (E1 only)
Register Address: 62h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	SiF14	SiF12	SiF10	SiF8	SiF6	SiF4	SiF2	SiF0
Default	0	0	0	0	0	0	0	0

The align frame is the E1 frame containing the frame alignment signal (FAS). When SiAF=1 in BTOCR, the bits of this register specify the Si bits to be transmitted in the align frames of outgoing multiframes. The Si bits are sampled from this register at the start of the multiframe. The multiframe boundary is indicated by the TMF status bit in BTSR1. See Section 6.9.6.4.

Bit 7: Si Bit of Frame 14 (SiF14).
Bit 6: Si Bit of Frame 12 (SiF12).
Bit 5: Si Bit of Frame 10 (SiF10).
Bit 4: Si Bit of Frame 8 (SiF8).
Bit 3: Si Bit of Frame 6 (SiF6).
Bit 2: Si Bit of Frame 4 (SiF4).
Bit 1: Si Bit of Frame 2 (SiF2).
Bit 0: Si Bit of Frame 0 (SiF0).

Register Name: BTSiNAF
Register Description: BITS Transmit Si Bits of the Non-Align Frame (E1 only)
Register Address: 63h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	SiF15	SiF13	SiF11	SiF9	SiF7	SiF5	SiF3	SiF1
Default	0	0	0	0	0	0	0	0

The non-align frame is the E1 frame that does not contain the frame alignment signal (FAS). When SiNAF=1 in BTOCR, the bits of this register specify the Si bits to be transmitted in the non-align frames of outgoing multiframes. The Si bits are sampled from this register at the start of the multiframe. The multiframe boundary is indicated by the TMF status bit in BTSR1. See Section 6.9.6.4.

Bit 7: Si Bit of Frame 15 (SiF15).
Bit 6: Si Bit of Frame 13 (SiF13).
Bit 5: Si Bit of Frame 11 (SiF11).
Bit 4: Si Bit of Frame 9 (SiF9).
Bit 3: Si Bit of Frame 7 (SiF7).
Bit 2: Si Bit of Frame 5 (SiF5).
Bit 1: Si Bit of Frame 3 (SiF3).
Bit 0: Si Bit of Frame 1 (SiF1).

Register Name: BTRAI
Register Description: BITS Transmit Remote Alarm Indication Bits (E1 only)
Register Address: 64h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	RAIF15	RAIF13	RAIF11	RAIF9	RAIF7	RAIF5	RAIF3	RAIF1
Default	0	0	0	0	0	0	0	0

When RAI=1 in BTOCR, the bits of this register specify the RAI bits to be transmitted in outgoing multiframes. The RAI bits are sampled from this register at the start of the multiframe. The multiframe boundary is indicated by the TMF status bit in BTSR1. See Section 6.9.6.4.

Bit 7: RAI Bit of Frame 15 (RAIF15).
Bit 6: RAI Bit of Frame 13 (RAIF13).
Bit 5: RAI Bit of Frame 11 (RAIF11).
Bit 4: RAI Bit of Frame 9 (RAIF9).
Bit 3: RAI Bit of Frame 7 (RAIF7).
Bit 2: RAI Bit of Frame 5 (RAIF5).
Bit 1: RAI Bit of Frame 3 (RAIF3).
Bit 0: RAI Bit of Frame 1 (RAIF1).

Register Name: BTSa4
Register Description: BITS Transmit Sa4 Bits (E1 only)
Register Address: 65h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Sa4F15	Sa4F13	Sa4F11	Sa4F9	Sa4F7	Sa4F5	Sa4F3	Sa4F1
Default	0	0	0	0	0	0	0	0

When Sa4=1 in BTOCR, the bits of this register specify the Sa4 bits to be transmitted in outgoing multiframes. The Sa4 bits are sampled from this register at the start of the multiframe. The multiframe boundary is indicated by the TMF status bit in BTSR1. See Section 6.9.6.4.

Bit 7: Sa4 Bit of Frame 15 (Sa4F15).
Bit 6: Sa4 Bit of Frame 13 (Sa4F13).
Bit 5: Sa4 Bit of Frame 11 (Sa4F11).
Bit 4: Sa4 Bit of Frame 9 (Sa4F9).
Bit 3: Sa4 Bit of Frame 7 (Sa4F7).
Bit 2: Sa4 Bit of Frame 5 (Sa4F5).
Bit 1: Sa4 Bit of Frame 3 (Sa4F3).
Bit 0: Sa4 Bit of Frame 1 (Sa4F1).

Register Name: BTSa5
Register Description: BITS Transmit Sa5 Bits (E1 only)
Register Address: 66h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Sa5F15	Sa5F13	Sa5F11	Sa5F9	Sa5F7	Sa5F5	Sa5F3	Sa5F1
Default	0	0	0	0	0	0	0	0

When Sa5=1 in BTOCR, the bits of this register specify the Sa5 bits to be transmitted in outgoing multiframes. The Sa5 bits are sampled from this register at the start of the multiframe. The multiframe boundary is indicated by the TMF status bit in BTSR1. See Section 6.9.6.4.

Bit 7: Sa5 Bit of Frame 15 (Sa5F15).
Bit 6: Sa5 Bit of Frame 13 (Sa5F13).
Bit 5: Sa5 Bit of Frame 11 (Sa5F11).
Bit 4: Sa5 Bit of Frame 9 (Sa5F9).
Bit 3: Sa5 Bit of Frame 7 (Sa5F7).
Bit 2: Sa5 Bit of Frame 5 (Sa5F5).
Bit 1: Sa5 Bit of Frame 3 (Sa5F3).
Bit 0: Sa5 Bit of Frame 1 (Sa5F1).

Register Name: BTSa6
Register Description: BITS Transmit Sa6 Bits (E1 only)
Register Address: 67h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Sa6F15	Sa6F13	Sa6F11	Sa6F9	Sa6F7	Sa6F5	Sa6F3	Sa6F1
Default	0	0	0	0	0	0	0	0

When Sa6=1 in BTOCR, the bits of this register specify the Sa6 bits to be transmitted in outgoing multiframes. The Sa6 bits are sampled from this register at the start of the multiframe. The multiframe boundary is indicated by the TMF status bit in BTSR1. See Section 6.9.6.4.

Bit 7: Sa6 Bit of Frame 15 (Sa6F15).
Bit 6: Sa6 Bit of Frame 13 (Sa6F13).
Bit 5: Sa6 Bit of Frame 11 (Sa6F11).
Bit 4: Sa6 Bit of Frame 9 (Sa6F9).
Bit 3: Sa6 Bit of Frame 7 (Sa6F7).
Bit 2: Sa6 Bit of Frame 5 (Sa6F5).
Bit 1: Sa6 Bit of Frame 3 (Sa6F3).
Bit 0: Sa6 Bit of Frame 1 (Sa6F1).

Register Name: BTSa7
Register Description: BITS Transmit Sa7 Bits (E1 only)
Register Address: 68h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Sa7F15	Sa7F13	Sa7F11	Sa7F9	Sa7F7	Sa7F5	Sa7F3	Sa7F1
Default	0	0	0	0	0	0	0	0

When Sa7=1 in BTOCR, the bits of this register specify the Sa7 bits to be transmitted in outgoing multiframes. The Sa7 bits are sampled from this register at the start of the multiframe. The multiframe boundary is indicated by the TMF status bit in BTSR1. See Section 6.9.6.4.

Bit 7: Sa7 Bit of Frame 15 (Sa7F15).
Bit 6: Sa7 Bit of Frame 13 (Sa7F13).
Bit 5: Sa7 Bit of Frame 11 (Sa7F11).
Bit 4: Sa7 Bit of Frame 9 (Sa7F9).
Bit 3: Sa7 Bit of Frame 7 (Sa7F7).
Bit 2: Sa7 Bit of Frame 5 (Sa7F5).
Bit 1: Sa7 Bit of Frame 3 (Sa7F3).
Bit 0: Sa7 Bit of Frame 1 (Sa7F1).

Register Name: BTSa8
Register Description: BITS Transmit Sa8 Bits (E1 only)
Register Address: 69h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	Sa8F15	Sa8F13	Sa8F11	Sa8F9	Sa8F7	Sa8F5	Sa8F3	Sa8F1
Default	0	0	0	0	0	0	0	0

When Sa8=1 in BTOCR, the bits of this register specify the Sa8 bits to be transmitted in outgoing multiframes. The Sa8 bits are sampled from this register at the start of the multiframe. The multiframe boundary is indicated by the TMF status bit in BTSR1. See Section 6.9.6.4.

Bit 7: Sa8 Bit of Frame 15 (Sa8F15).
Bit 6: Sa8 Bit of Frame 13 (Sa8F13).
Bit 5: Sa8 Bit of Frame 11 (Sa8F11).
Bit 4: Sa8 Bit of Frame 9 (Sa8F9).
Bit 3: Sa8 Bit of Frame 7 (Sa8F7).
Bit 2: Sa8 Bit of Frame 5 (Sa8F5).
Bit 1: Sa8 Bit of Frame 3 (Sa8F3).
Bit 0: Sa8 Bit of Frame 1 (Sa8F1).

Register Name: BTOCR
Register Description: BITS Transmit Overhead Control Register (E1 only)
Register Address: 6Ah

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	SiAF	SiNAF	RAI	Sa4	Sa5	Sa6	Sa7	Sa8
Default	0	0	0	0	0	0	0	0

When set to 1 these control bits have precedence over any other source of Si/RAI/Sa bits, including the CRC-4 Si bit generation logic. See Section 6.9.6.

Bit 7: Si In Align Frame Data Source (SiAF).
0 = Do not source the Si bits in the align frame from the BTSiAF register
1 = Source the Si bits in the align frame from the BTSiAF register

Bit 6: Si In Non-Align Frame Data Source (SiNAF).
0 = Do not source the Si bits in the non-align frame from the BTSiNAF register
1 = Source the Si bits in the non-align frame from the BTSiNAF register

Bit 5: RAI Data Source (RAI).
0 = Do not source the RAI bits from the BTRAI register
1 = Source the RAI bits from the BTRAI register

Bit 4: Sa4 Data Source (Sa4).
0 = Do not source the Sa4 bits from the BTSa4 register
1 = Source the Sa4 bits from the BTSa4 register

Bit 3: Sa5 Data Source (Sa5).
0 = Do not source the Sa5 bits from the BTSa5 register
1 = Source the Sa5 bits from the BTSa5 register

Bit 2: Sa6 Data Source (Sa6).
0 = Do not source the Sa6 bits from the BTSa6 register
1 = Source the Sa6 bits from the BTSa6 register

Bit 1: Sa7 Data Source (Sa7).
0 = Do not source the Sa7 bits from the BTSa7 register
1 = Source the Sa7 bits from the BTSa7 register

Bit 0: Sa8 Data Source (Sa8).
0 = Do not source the Sa8 bits from the BTSa8 register
1 = Source the Sa8 bits from the BTSa8 register

8. JTAG TEST ACCESS PORT AND BOUNDARY SCAN

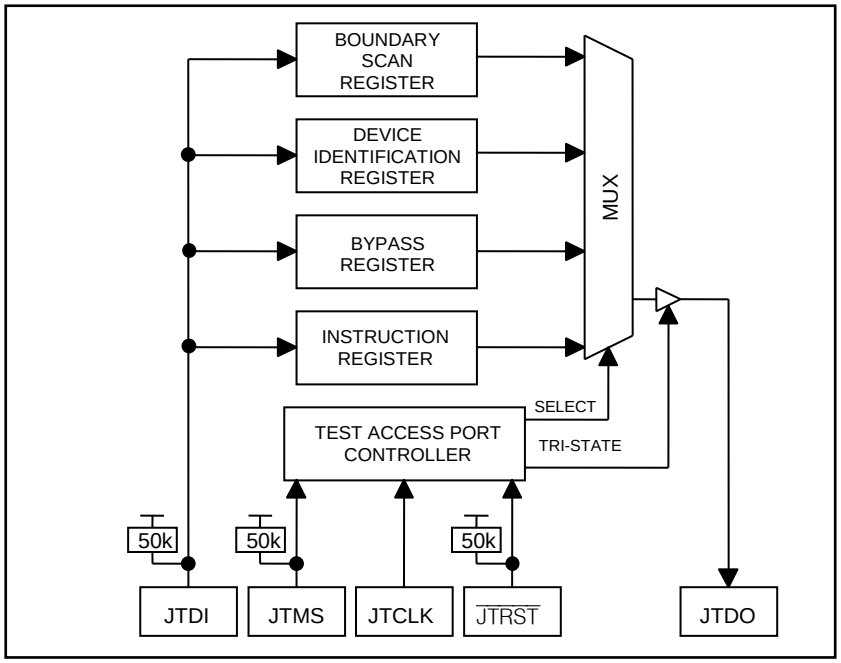
8.1 JTAG Description

The ZL81000 supports the standard instruction codes SAMPLE/PRELOAD, BYPASS, and EXTEST. Optional public instructions included are HIGHZ, CLAMP, and IDCODE. Figure 8-1 shows a block diagram. The ZL81000 contains the following items, which meet the requirements set by the IEEE 1149.1 Standard Test Access Port and Boundary Scan Architecture:

Test Access Port (TAP)	Bypass Register
TAP Controller	Boundary Scan Register
Instruction Register	Device Identification Register

The TAP has the necessary interface pins, namely JTCLK, $\overline{\text{JTRST}}$, JTDI, JTDO, and JTMS. Details on these pins can be found in Table 5-8. Details about the boundary scan architecture and the TAP can be found in IEEE 1149.1-1990, IEEE 1149.1a-1993, and IEEE 1149.1b-1994.

Figure 8-1. JTAG Block Diagram



8.2 JTAG TAP Controller State Machine Description

This section discusses the operation of the TAP controller state machine. The TAP controller is a finite state machine that responds to the logic level at JTMS on the rising edge of JTCLK. Each of the states denoted in Figure 8-2 are described in the following paragraphs.

Test-Logic-Reset. Upon device power-up, the TAP controller starts in the Test-Logic-Reset state. The instruction register contains the IDCODE instruction. All system logic on the device operates normally.

Run-Test-Idle. Run-Test-Idle is used between scan operations or during specific tests. The instruction register and all test registers remain idle.

Select-DR-Scan. All test registers retain their previous state. With JTMS low, a rising edge of JTCLK moves the controller into the Capture-DR state and initiates a scan sequence. JTMS high moves the controller to the Select-IR-SCAN state.

Capture-DR. Data can be parallel-loaded into the test register selected by the current instruction. If the instruction does not call for a parallel load or the selected test register does not allow parallel loads, the register remains at its current value. On the rising edge of JTCLK, the controller goes to the Shift-DR state if JTMS is low or to the Exit1-DR state if JTMS is high.

Shift-DR. The test register selected by the current instruction is connected between JTDI and JTDO and data is shifted one stage toward the serial output on each rising edge of JTCLK. If a test register selected by the current instruction is not placed in the serial path, it maintains its previous state.

Exit1-DR. While in this state, a rising edge on JTCLK with JTMS high puts the controller in the Update-DR state, which terminates the scanning process. A rising edge on JTCLK with JTMS low puts the controller in the Pause-DR state.

Pause-DR. Shifting of the test registers is halted while in this state. All test registers selected by the current instruction retain their previous state. The controller remains in this state while JTMS is low. A rising edge on JTCLK with JTMS high puts the controller in the Exit2-DR state.

Exit2-DR. While in this state, a rising edge on JTCLK with JTMS high puts the controller in the Update-DR state and terminates the scanning process. A rising edge on JTCLK with JTMS low puts the controller in the Shift-DR state.

Update-DR. A falling edge on JTCLK while in the Update-DR state latches the data from the shift register path of the test registers into the data output latches. This prevents changes at the parallel output because of changes in the shift register. A rising edge on JTCLK with JTMS low puts the controller in the Run-Test-Idle state. With JTMS high, the controller enters the Select-DR-Scan state.

Select-IR-Scan. All test registers retain their previous state. The instruction register remains unchanged during this state. With JTMS low, a rising edge on JTCLK moves the controller into the Capture-IR state and initiates a scan sequence for the instruction register. JTMS high during a rising edge on JTCLK puts the controller back into the Test-Logic-Reset state.

Capture-IR. The Capture-IR state is used to load the shift register in the instruction register with a fixed value. This value is loaded on the rising edge of JTCLK. If JTMS is high on the rising edge of JTCLK, the controller enters the Exit1-IR state. If JTMS is low on the rising edge of JTCLK, the controller enters the Shift-IR state.

Shift-IR. In this state, the instruction register's shift register is connected between JTDI and JTDO and shifts data one stage for every rising edge of JTCLK toward the serial output. The parallel register and the test registers remain at their previous states. A rising edge on JTCLK with JTMS high moves the controller to the Exit1-IR state. A rising edge on JTCLK with JTMS low keeps the controller in the Shift-IR state, while moving data one stage through the instruction shift register.

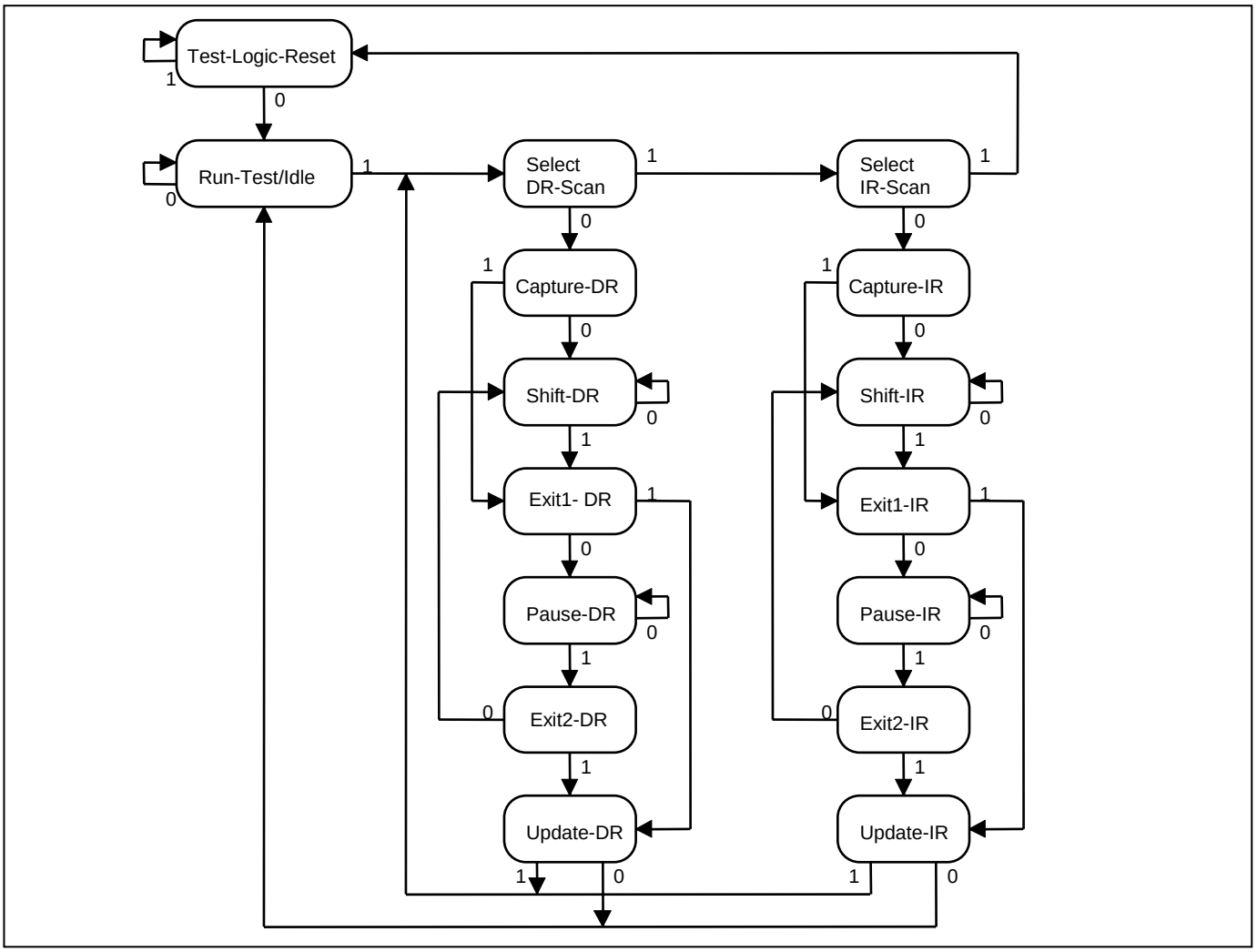
Exit1-IR. A rising edge on JTCLK with JTMS low puts the controller in the Pause-IR state. If JTMS is high on the rising edge of JTCLK, the controller enters the Update-IR state and terminates the scanning process.

Pause-IR. Shifting of the instruction register is halted temporarily. With JTMS high, a rising edge on JTCLK puts the controller in the Exit2-IR state. The controller remains in the Pause-IR state if JTMS is low during a rising edge on JTCLK.

Exit2-IR. A rising edge on JTCLK with JTMS high puts the controller in the Update-IR state. The controller loops back to the Shift-IR state if JTMS is low during a rising edge of JTCLK in this state.

Update-IR. The instruction shifted into the instruction shift register is latched into the parallel output on the falling edge of JTCLK as the controller enters this state. Once latched, this instruction becomes the current instruction. A rising edge on JTCLK with JTMS low puts the controller in the Run-Test-Idle state. With JTMS high, the controller enters the Select-DR-Scan state.

Figure 8-2. JTAG TAP Controller State Machine



8.3 JTAG Instruction Register and Instructions

The instruction register contains a shift register as well as a latched parallel output and is 3 bits in length. When the TAP controller enters the Shift-IR state, the instruction shift register is connected between JTDI and JTDO. While in the Shift-IR state, a rising edge on JTCLK with JTMS low shifts data one stage toward the serial output at JTDO. A rising edge on JTCLK in the Exit1-IR state or the Exit2-IR state with JTMS high moves the controller to the Update-IR state. The falling edge of that same JTCLK latches the data in the instruction shift register to the instruction parallel output. Table 8-1 shows the instructions supported by the ZL81000 and their respective operational binary codes.

Table 8-1. JTAG Instruction Codes

INSTRUCTIONS	SELECTED REGISTER	INSTRUCTION CODES
SAMPLE/PRELOAD	Boundary Scan	010
BYPASS	Bypass	111
EXTEST	Boundary Scan	000
CLAMP	Bypass	011
HIGHZ	Bypass	100
IDCODE	Device Identification	001

SAMPLE/PRELOAD. SAMPLE/RELOAD is a mandatory instruction for the IEEE 1149.1 specification. This instruction supports two functions. First, the digital I/Os of the device can be sampled at the boundary scan register, using the Capture-DR state, without interfering with the device's normal operation. Second, data can be shifted into the boundary scan register through JTDI using the Shift-DR state.

EXTEST. EXTEST allows testing of the interconnections to the device. When the EXTEST instruction is latched in the instruction register, the following actions occur: (1) Once the EXTEST instruction is enabled through the Update-IR state, the parallel outputs of the digital output pins are driven. (2) The boundary scan register is connected between JTDI and JTDO. (3) The Capture-DR state samples all digital inputs into the boundary scan register.

BYPASS. When the BYPASS instruction is latched into the parallel instruction register, JTDI is connected to JTDO through the 1-bit bypass register. This allows data to pass from JTDI to JTDO without affecting the device's normal operation.

IDCODE. When the IDCODE instruction is latched into the parallel instruction register, the device identification register is selected. The device ID code is loaded into the device identification register on the rising edge of JTCLK, following entry into the Capture-DR state. Shift-DR can be used to shift the ID code out serially through JTDO. During Test-Logic-Reset, the ID code is forced into the instruction register's parallel output.

HIGHZ. All digital outputs are placed into a high-impedance state. The bypass register is connected between JTDI and JTDO.

CLAMP. All digital output pins output data from the boundary scan parallel output while connecting the bypass register between JTDI and JTDO. The outputs do not change during the CLAMP instruction.

8.4 JTAG Test Registers

IEEE 1149.1 requires a minimum of two test registers—the bypass register and the boundary scan register. An optional test register, the identification register, has been included in the device design. It is used with the IDCODE instruction and the Test-Logic-Reset state of the TAP controller.

Bypass Register. This is a single 1-bit shift register used with the BYPASS, CLAMP, and HIGHZ instructions to provide a short path between JTDI and JTDO.

Boundary Scan Register. This register contains a shift register path and a latched parallel output for control cells and digital I/O cells. BSDL files are available on the ZL81000 page of Microsemi's website.

Identification Register. This register contains a 32-bit shift register and a 32-bit latched parallel output. It is selected during the IDCODE instruction and when the TAP controller is in the Test-Logic-Reset state. The device identification code for the ZL81000 is shown in Table 8-2.

Table 8-2. JTAG ID Code

DEVICE	REVISION	DEVICE CODE	MANUFACTURER CODE	REQUIRED
ZL81000	Consult factory	1000 0000 0001 1100	0001 0100 001	1

9. ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Pin with Respect to V_{SS} (except V_{DD}).....-0.3V to +5.5V
Supply Voltage Range (V_{DD}) with Respect to V_{SS}.....-0.3V to +1.98V
Supply Voltage Range (V_{DDIO}) with Respect to V_{SS}.....-0.3V to +3.63V
Ambient Operating Temperature Range.....-40°C to +85°C (**Note 1**)
Junction Operating Temperature Range.....-40°C to +125°C
Storage Temperature Range.....-55°C to +125°C
Soldering Temperature.....See IPC/JEDEC J-STD-020 Specification

Note 1: Specifications to -40°C are guaranteed by design and not production tested.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to the absolute maximum rating conditions for extended periods may affect device. Ambient operating temperature range when device is mounted on a four-layer JEDEC test board with no airflow.

9.1 DC Characteristics

Table 9-1. Recommended DC Operating Conditions

(T_A = -40°C to +85°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage, Core	V_{DD}		1.62	1.8	1.98	V
Supply Voltage, I/O	V_{DDIO}		3.135	3.3	3.465	V
Ambient Temperature Range	T_A		-40		+85	°C

Table 9-2. DC Characteristics

(V_{DD} = 1.8V ±10%, V_{DDIO} = 3.3V ±5%, T_A = -40°C to +85°C.)

PARAMETER		SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	1.8V	I_{DD18}	(Note 2)		129	152	mA
	1.8V	I_{DD18}	(Note 3)		130	154	
	3.3V	I_{DD33}	(Note 2)		36	53	
	3.3V	I_{DD33}	(Note 3)		124	145	
Supply Current Reduction When One BITS Transmitter is Powered Down		I_{DDR1}	BLCR4:TPD = 1		35		mA
Supply Current Reduction When One BITS Receiver is Powered Down		I_{DDR2}	BLCR4:RPD = 1		9		mA
Input Capacitance		C_{IN}			5		pF
Output Capacitance		C_{OUT}			7		pF

Note 2: 12.800MHz clock applied to REFCLK. Both BITS transceivers shut down, 19.44MHz clock applied to one CMOS/TTL input clock pin. OC9 output clock pin driving 100pF load; all other inputs at V_{DDIO} or grounded; all other outputs open.

Note 3: 12.800MHz clock applied to REFCLK. Both BITS transceivers enabled in E1 mode, transmitting and receiving over 75Ω cables through recommended transformers and external circuitry. 19.44MHz clock applied to one CMOS/TTL input clock pin. OC9 output clock pin driving 100pF load; all other inputs at V_{DDIO} or grounded; all other outputs open.

Table 9-3. CMOS/TTL Pins

(V_{DD} = 1.8V ±10%, V_{DDIO} = 3.3V ±5%, T_A = -40°C to +85°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		2.0		5.5	V
Input Low Voltage	V_{IL}		-0.3		+0.8	V
Input Leakage	I_{IL}	(Note 1)	-10		+10	µA
Input Leakage, Pins with Internal Pullup Resistor (50kΩ typical)	I_{ILPU}	(Note 1)	-85		+10	µA
Input Leakage, Pins with Internal Pulldown Resistor (50kΩ typical)	I_{ILPD}	(Note 1)	-10		+85	µA
Output Leakage (when High Impedance)	I_{LO}	(Note 1)	-10		+10	µA
Output High Voltage (I_O = -4.0mA)	V_{OH}		2.4		V_{DDIO}	V
Output Low Voltage (I_O = +4.0mA)	V_{OL}		0		0.4	V

Note 1: 0V < V_{IN} < V_{DDIO} for all other digital inputs.

Table 9-4. LVDS Pins

(V_{DD} = 1.8V ±10%, V_{DDIO} = 3.3V ±5%, T_A = -40°C to +85°C.) (See Figure 9-1.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage Range	V_{INLVDS}	V_{IDLVDS} = 100mV	0		2.4	V
Differential Input Voltage	V_{IDLVDS}		0.1		1.4	V
Differential Input Logic Threshold	V_{THLVDS}		-100		+100	mV
Output High Voltage	V_{OHLVDS}	(Note 1)		1.45	1.65	V
Output Low Voltage	V_{OLLVDS}	(Note 1)	0.885	1.1		V
Differential Output Voltage	V_{ODLVDS}		250		450	mV
Output Offset Voltage (Common Mode Voltage)	V_{OSLVDS}	+25°C (Note 1)	1.08	1.28	1.45	V
Difference in Magnitude of Output Differential Voltage for Complementary States	$V_{DOSLVDS}$				25	mV

Note 1: With 100Ω load across the differential outputs.

Note 2: The ZL81000's LVDS output pins can easily be interfaced to LVPECL and CML inputs on neighboring ICs using a few external passive components. See App Note HFAN-1.0 for details.

Figure 9-1. Recommended Termination for LVDS Pins

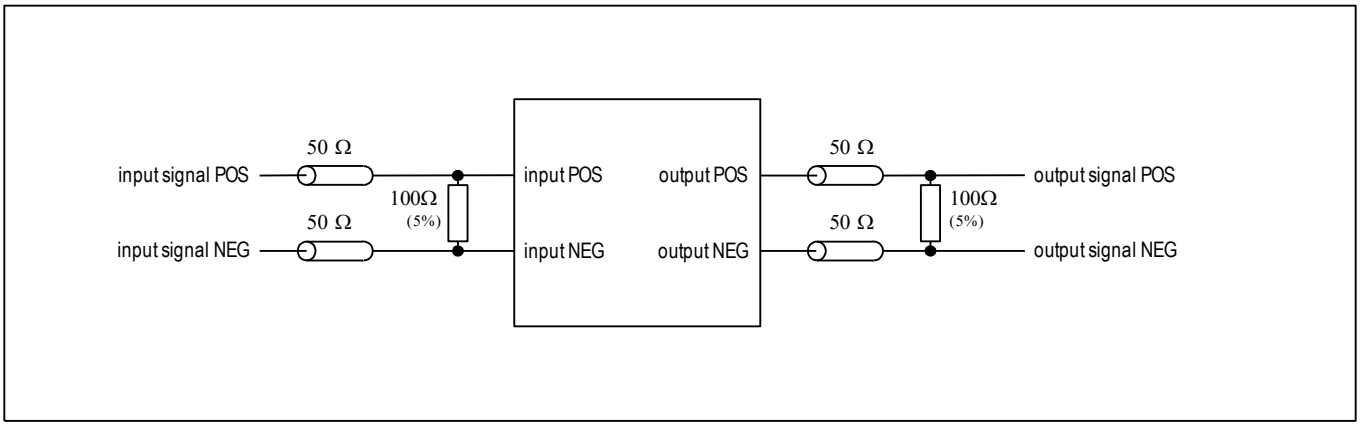


Table 9-5. LVPECL Pins

(V_{DD} = 1.8V ±10%, V_{DDIO} = 3.3V ±5%, T_A = -40°C to +85°C) (See Figure 9-2.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage, Differential Inputs	V_{IHPECL}	(Note 1)	V_{DDIO} - 2.4		V_{DDIO} - 0.4	V
Input Low Voltage, Differential Inputs	V_{ILPECL}	(Note 1)	V_{DDIO} - 2.5		V_{DDIO} - 0.5	V
Input Differential Voltage	V_{IDPECL}		0.1		1.4	V
Input High Voltage, Single-Ended Inputs	$V_{IHPECL,S}$	(Note 2)	V_{DDIO} - 1.3		V_{DDIO} - 0.5	V
Input Low Voltage, Single-Ended Inputs	$V_{ILPECL,S}$	(Note 2)	V_{DDIO} - 2.4		V_{DDIO} - 1.5	V

Note 1: For a differential input voltage ≥ 100mV.

Note 2: With the unused differential input tied to V_{DDIO} - 1.4V.

Note 3: Although the ZL81000's differential outputs do not directly drive standard LVPECL signals, these output pins can easily be interfaced to LVPECL and CML inputs on neighboring ICs using a few external passive components. See App Note HFAN-1.0 for details.

Figure 9-2. Recommended Termination for LVPECL Pins

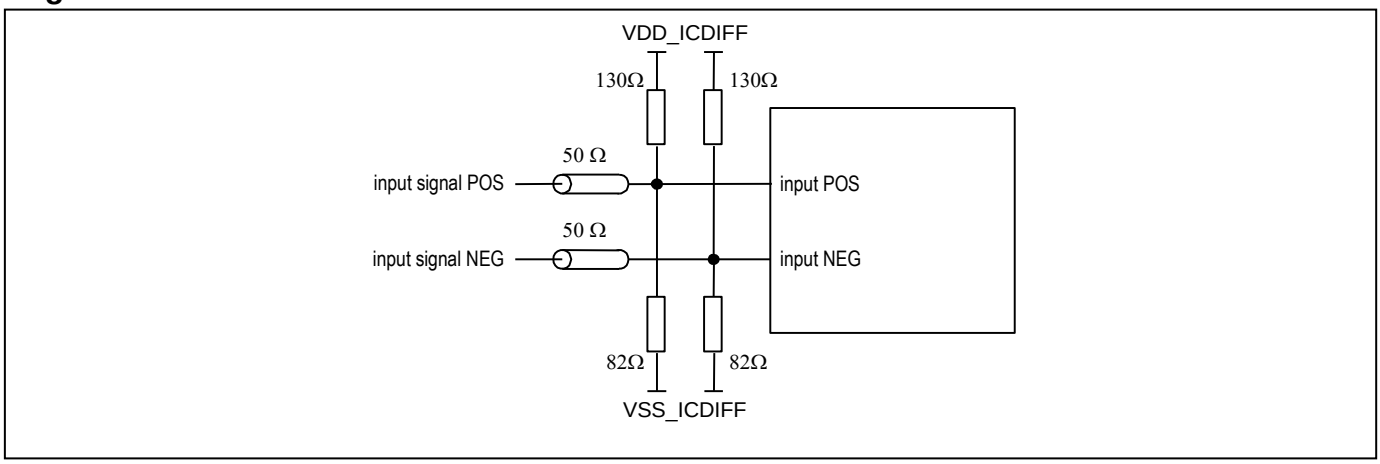


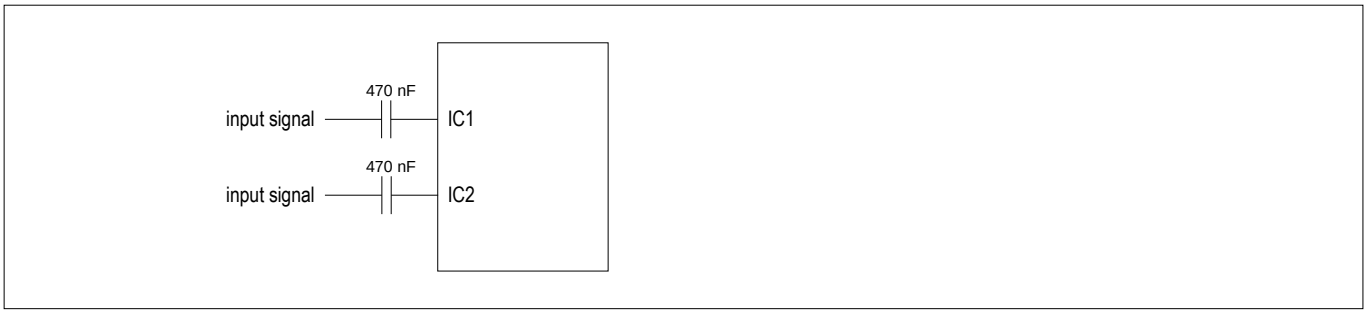
Table 9-6. AMI Composite Clock Pins

(V_{DD} = 1.8V ±10%, V_{DDIO} = 3.3V ±5%, T_A = -40°C to +85°C.) (Note 1) (See Figure 9-3.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IHAMI}		2.2		V_{DDIO} + 0.3	V
Input Middle Voltage	V_{IMAMI}		1.5	1.65	1.8	V
Input Low Voltage	V_{ILAMI}		-0.3		1.1	V
Input LOS Threshold	V_{LOS}	At the IC1A or IC2A pin		0.2		V
Input Pulse Width	t_{PW}		1.6	7.8	14	µs
Input Rise/Fall Time	t_R, t_F				0.5	µs

Note 1: The timing parameters in this table are guaranteed by design (GBD).

Figure 9-3. Recommended External Components for AMI Composite Clock Pins



For input CC signals compliant with Telcordia GR-378 (amplitude 2.7V to 5.5V) or ITU G.703 Section 4.2.2 option b) (3V±0.5V), the signal should be attenuated by a factor of 3 (or more) before being presented to IC1A or IC2A. Input CC signals with a 1V nominal pulse amplitude can be presented unattenuated.

9.2 Input Clock Timing

Table 9-7. Input Clock Timing

(V_{DD} = 1.8V ±10%, V_{DDIO} = 3.3V ±5%, T_A = -40°C to +85°C.)

PARAMETER	SYMBOL	MIN	TYP	MAX
Input Clock Period, CMOS/TTL Input Pins	t_{CYC}	8ns (125MHz)		500µs (2kHz)
Input Clock High, Low Time	t_H, t_L	3ns or 30% of t_{CYC}, whichever is smaller		

9.3 BITS Transceiver Timing

Table 9-8. BITS Receiver Timing

(V_{DD} = 1.8V ±10%, V_{DDIO} = 3.3V ±5%, T_A = -40°C to +85°C.) (Note 1) (See Figure 9-4.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
RCLK Period	t_{CP}	(Note 2)		488		ns
		(Note 3)		648		
		(Note 4)		158.4		
RCLK Duty Cycle			45%	50%	55%	ns
RCLK to RSER Delay	t_{OD1}				50	ns
RCLK to ROUT Delay	t_{OD2}				50	ns
RCLK, RSER and ROUT Rise and Fall Times	t_R, t_F	(Note 5)			10	ns
ROUT Pulse Width	t_{ROPW}		50			ns

Note 1: The timing parameters in this table are guaranteed by design (GBD).
Note 2: E1 or 2048kHz mode.
Note 3: DS1mode.
Note 4: 6312kHz mode.
Note 5: 100pF load.

Figure 9-4. BITS Receiver Timing Diagram

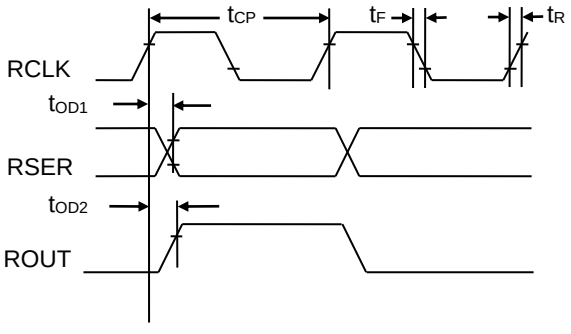


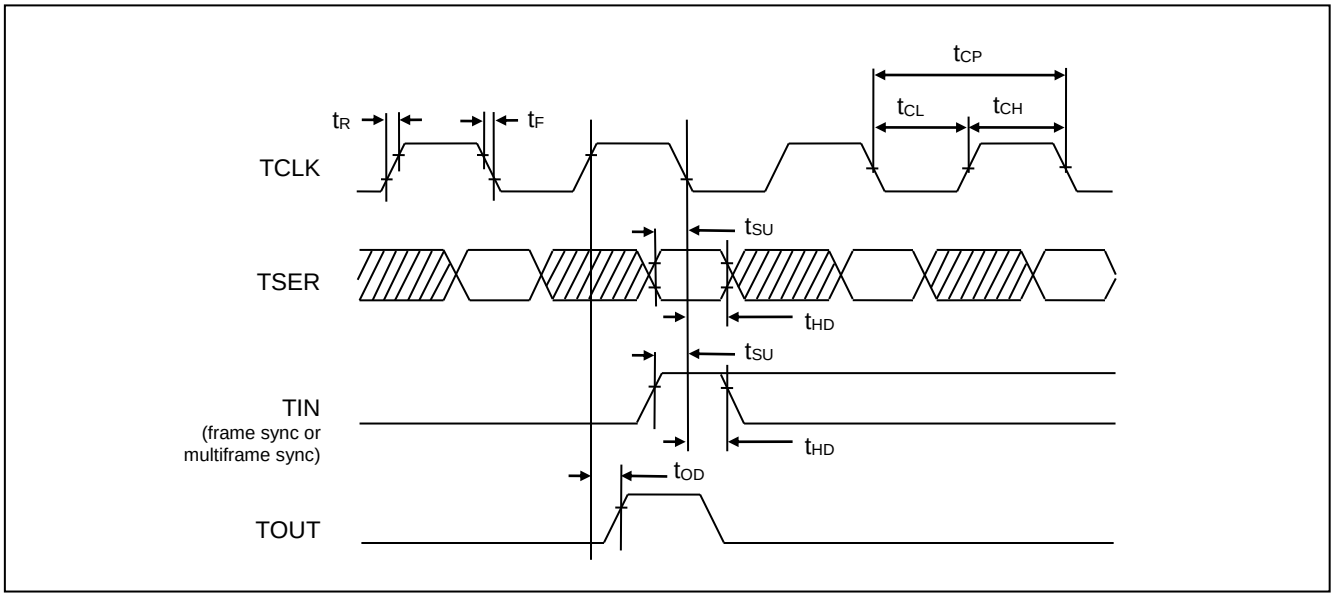
Table 9-9. BITS Transmitter Timing

(V_{DD} = 1.8V ±10%, V_{DDIO} = 3.3V ±5%, T_A = -40°C to +85°C.) (Note 1) (See Figure 9-5.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TCLK Period	t_{CP}	(Note 2)		488		ns
		(Note 3)		648		
TCLK High Time	t_{CH}		125			ns
TCLK Low Time	t_{CL}		125			ns
TSER, TIN Rise and Fall Times	t_R, t_F				20	ns
TSER, TIN to TCLK Setup Time	t_{SU}		20		t_{CH} - 5	ns
TSER, TIN to TCLK Hold Time	t_{HD}		20			ns
TCLK to TOUT Delay	t_{OD}				50	ns
TCLK, TOUT Rise and Fall Times	t_R, t_F	(Note 4)			10	ns

Note 1: The timing parameters in this table are guaranteed by design (GBD).
Note 2: E1 or 2048kHz mode.
Note 3: DS1mode.
Note 4: 100pF load.

Figure 9-5. BITS Transmitter Timing Diagram



9.4 Parallel Interface Timing

Table 9-10. Parallel Interface Timing

(V_{DD} = 1.8V ±10%, V_{DDIO} = 3.3V ±5%, T_A = -40°C to +85°C.) (Note 1) (See Figure 9-6 and Figure 9-7.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Address Setup to $\overline{RD}$, $\overline{WR}$, $\overline{DS}$ Active	t1a	(Note 2)	10			ns
ALE Setup to $\overline{RD}$, $\overline{WR}$, $\overline{DS}$ Active	t1b	(Notes 2, 3)	10			ns
Address Setup to ALE Inactive	t2	(Notes 2, 3)	2			ns
Address Hold from ALE Inactive	t3	(Notes 2, 3)	2			ns
ALE Pulse Width	t4	(Notes 2, 3)	5			ns
Address Hold from $\overline{RD}$, $\overline{WR}$, $\overline{DS}$ Inactive	t5	(Note 2)	0			ns
$\overline{CS}$ Setup to $\overline{RD}$, $\overline{WR}$, $\overline{DS}$ Active	t6	(Note 2)	0			ns
Data Valid from $\overline{RD}$, $\overline{DS}$ Active	t8	(Note 2)			80	ns
$\overline{RD}$, $\overline{WR}$, $\overline{DS}$ Pulse Width if not Using $\overline{RDY}$ Handshake	t9a	(Notes 2, 4)	90			ns
$\overline{RD}$, $\overline{WR}$, $\overline{DS}$ Delay from $\overline{RDY}$ Active	t9b	(Note 2)	15			ns
Data Output High Impedance from $\overline{RD}$, $\overline{DS}$ Inactive	t10	(Notes 2, 5)	2		10	ns
Data Output Enabled from $\overline{RD}$, $\overline{DS}$ Active	t11	(Note 2)	2			ns
$\overline{CS}$ Hold from $\overline{RD}$, $\overline{WR}$, $\overline{DS}$ Inactive	t12	(Note 2)	0			ns
Data Setup to $\overline{WR}$, $\overline{DS}$ Inactive	t13	(Note 2)	10			ns
Data Hold from $\overline{WR}$, $\overline{DS}$ inactive	t14	(Note 2)	5			ns
$\overline{RDY}$ Active from $\overline{RD}$, $\overline{WR}$, $\overline{DS}$ Active	t15	(Note 2)	10			ns
$\overline{RDY}$ Inactive from $\overline{RD}$, $\overline{WR}$, $\overline{DS}$ Inactive	t16	(Note 2)	0		10	ns
$\overline{RDY}$ Output Enabled from $\overline{CS}$ Active	t17	(Note 2)			10	ns
$\overline{RDY}$ Output High Impedance from $\overline{CS}$ Inactive	t18	(Note 2)			10	ns
$\overline{RDY}$ Ending High Pulse Width	t19	(Note 2)	2			ns
R/$\overline{W}$ Setup to $\overline{DS}$ Active	t20	(Note 2)	2			ns
R/$\overline{W}$ Hold from $\overline{DS}$ Inactive	t21	(Note 2)	2			ns

Note 1: The timing parameters in this table are guaranteed by design (GBD).
Note 2: The input/output timing reference level for all signals is VDD/2. Transition time (80/20%) on $\overline{RD}$, $\overline{WR}$, and $\overline{CS}$ inputs is 5ns max.
Note 3: Multiplexed mode timing only.
Note 4: Timing required if not using $\overline{RDY}$ handshake.
Note 5: D[7:0] output valid until not driven.

Figure 9-6. Parallel Interface Timing Diagram (Nonmultiplexed)

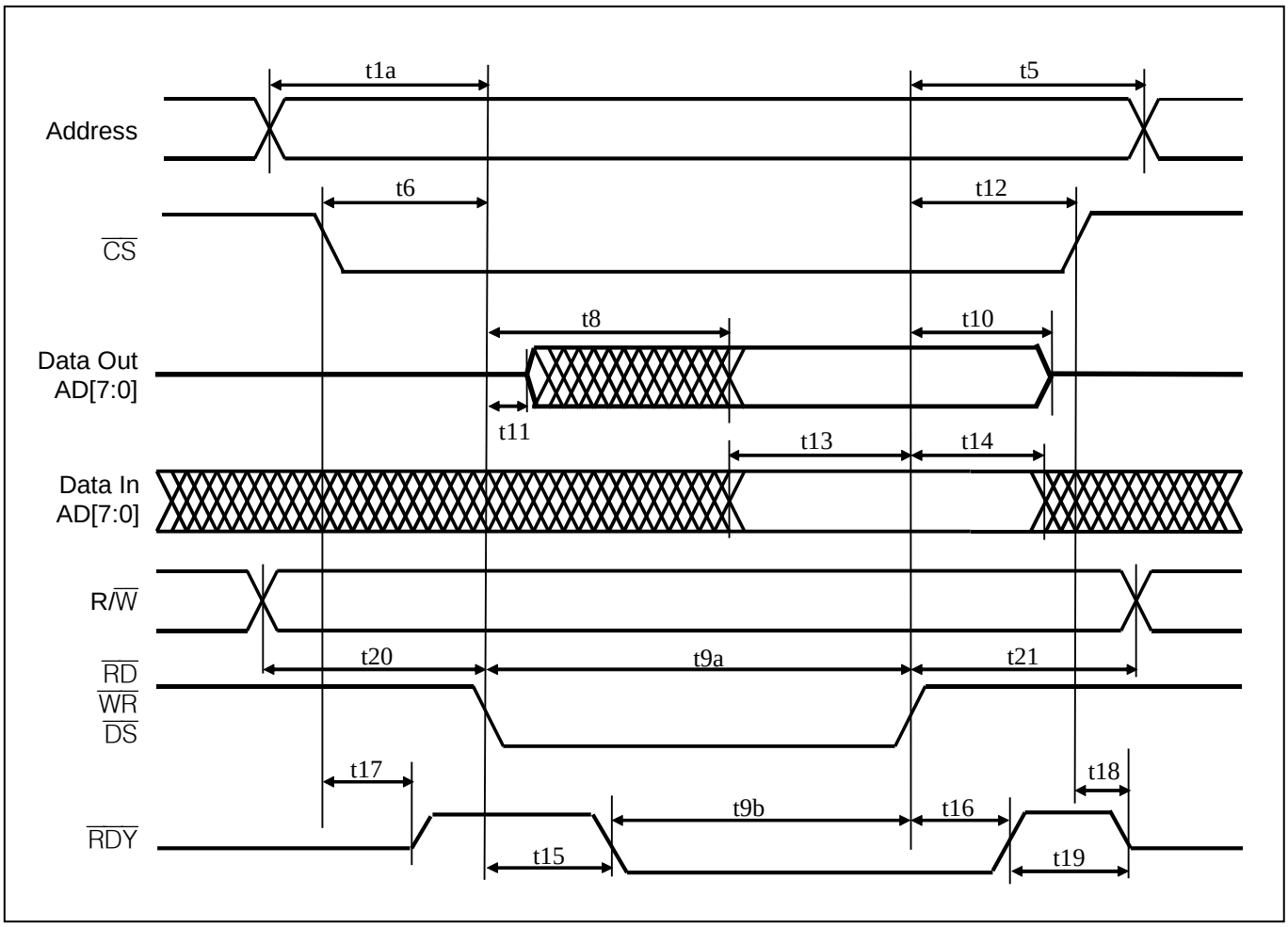
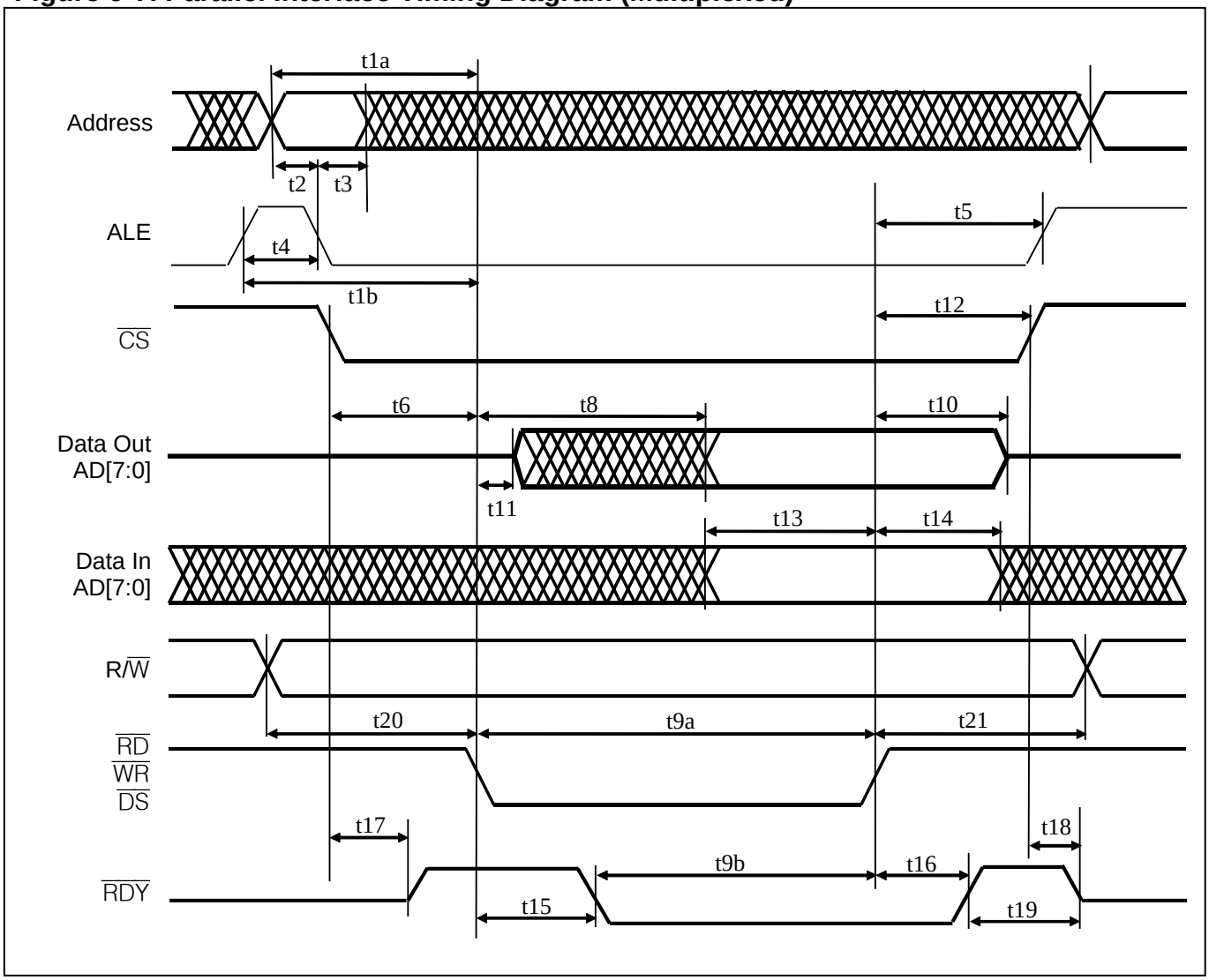


Figure 9-7. Parallel Interface Timing Diagram (Multiplexed)



9.5 SPI Interface Timing

Table 9-11. SPI Interface Timing

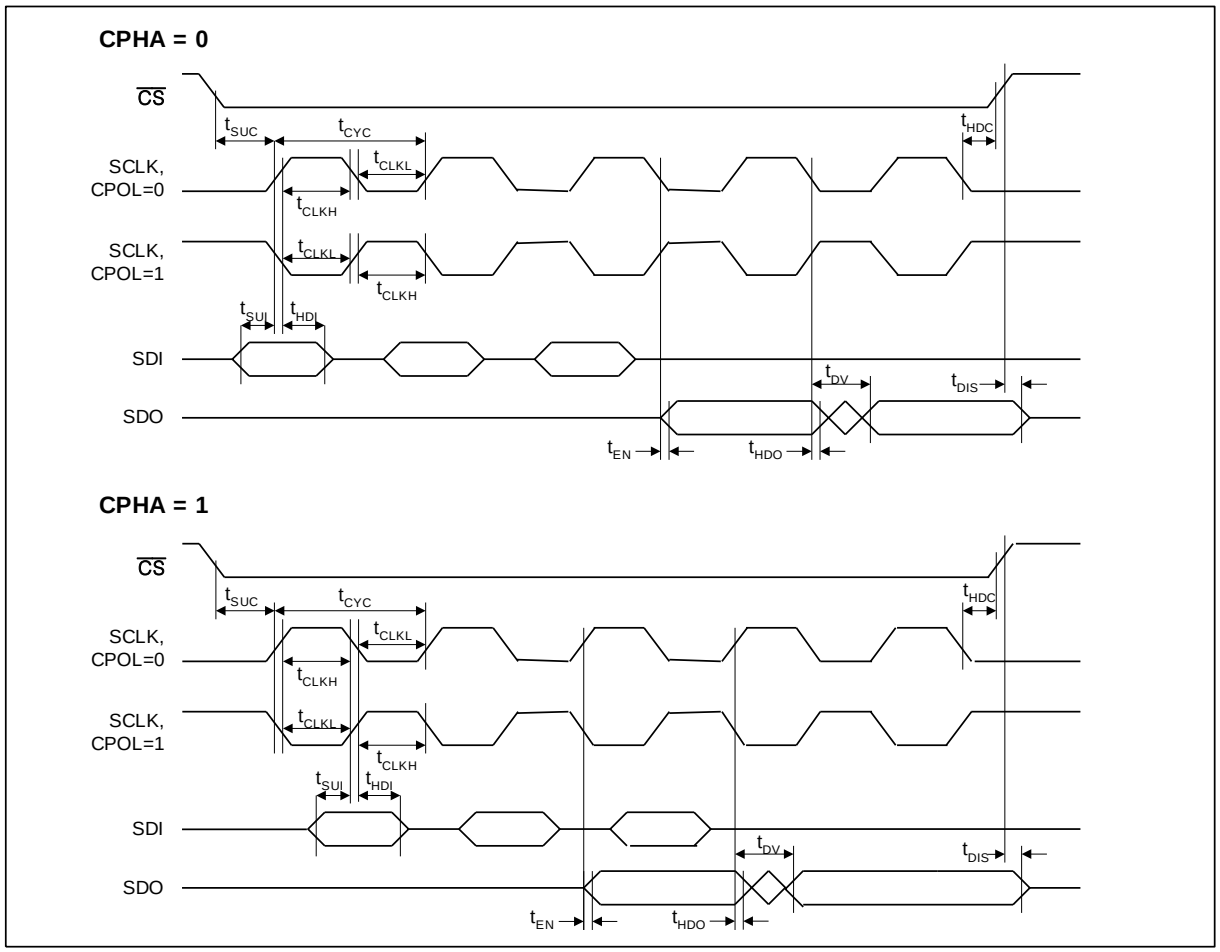
(V_{DD} = 1.8V ±10%, V_{DDIO} = 3.3V ±5%, T_A = -40°C to +85°C.) (Note 1) (See Figure 9-8.)

PARAMETER (Note 2)	SYMBOL	MIN	TYP	MAX	UNITS
SCLK Frequency	f_{BUS}			6	MHz
SCLK Cycle Time	t_{CYC}	166			ns
$\overline{CS}$ Setup to First SCLK Edge	t_{SUC}	15			ns
$\overline{CS}$ Hold time After Last SCLK Edge	t_{HDC}	15			ns
SCLK High Time	t_{CLKH}	80			ns
SCLK Low Time	t_{CLKL}	80			ns
SDI Data Setup Time	t_{SUI}	5			ns
SDI Data Hold Time	t_{HDI}	15			ns
SDO Enable Time (High-Impedance to Output Active)	t_{EN}	0			ns
SDO Disable Time (Output Active to High Impedance)	t_{DIS}			25	ns
SDO Data Valid Time	t_{DV}			40	ns
SDO Data Hold Time After Update SCLK Edge	t_{HDO}	5			ns

Note 1: The timing parameters in this table are guaranteed by design (GBD).

Note 2: All timing is specified with 100 pF load on all SPI pins.

Figure 9-8. SPI Interface Timing Diagram



9.6 JTAG Interface Timing

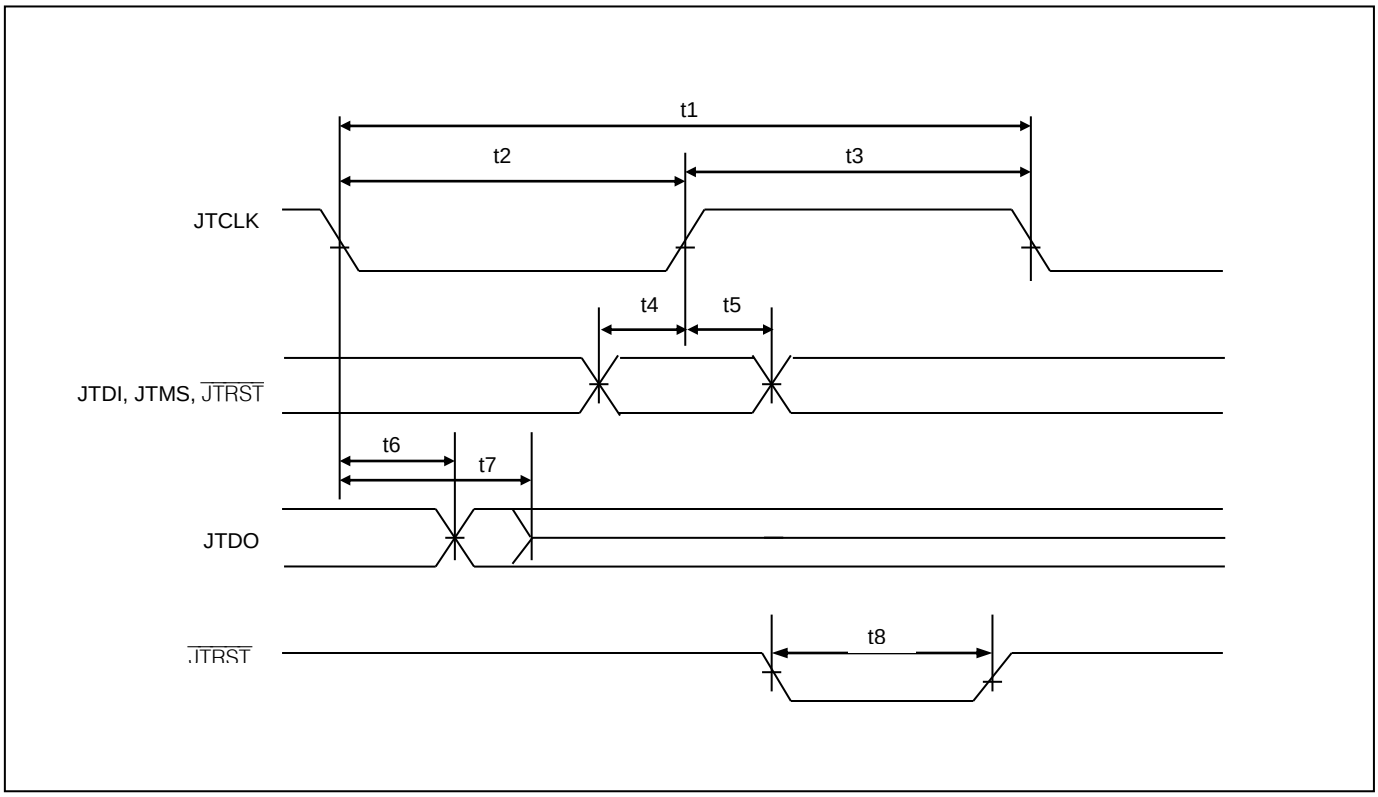
Table 9-12. JTAG Interface Timing

(V_{DD} = 1.8V ±10%, V_{DDIO} = 3.3V ±5%, T_A = -40°C to +85°C.) (Note 1) (See Figure 9-9.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
JTCLK Clock Period	t1		1000		ns
JTCLK Clock High/Low Time (Note 2)	t2/t3	50	500		ns
JTCLK to JTDI, JTMS Setup Time	t4	50			ns
JTCLK to JTDI, JTMS Hold Time	t5	50			ns
JTCLK to JTDO Delay	t6	2		50	ns
JTCLK to JTDO High-Impedance Delay (Note 3)	t7	2		50	ns
$\overline{\text{JTRST}}$ Width Low Time	t8	100			ns

Note 1: The timing parameters in this table are guaranteed by design (GBD).
Note 2: Clock can be stopped high or low.
Note 3: Not tested during production test.

Figure 9-9. JTAG Timing Diagram



10. PIN ASSIGNMENTS

Table 10-1 lists the ZL81000 pin assignments sorted in alphabetical order by pin name. Figure 10-1 and Figure 10-2 show pin assignments arranged by pin number.

Table 10-1. Pin Assignments Sorted by Signal Name

PIN NAME	PIN NUMBER	BUS MODES	SIGNAL TYPE
A[0]	H16	Parallel-Only	High-Speed Digital
A[1]	H15	Parallel-Only	High-Speed Digital
A[2]	G16	Parallel-Only	High-Speed Digital
A[3]	H14	Parallel-Only	High-Speed Digital
A[4]	G15	Parallel-Only	High-Speed Digital
A[5]	F16	Parallel-Only	High-Speed Digital
A[6]	G14	Parallel-Only	High-Speed Digital
A[7]	F15	Parallel-Only	High-Speed Digital
A[8]	E16	Parallel-Only	High-Speed Digital
AD[0]	E15	Parallel-Only	High-Speed Digital
AD[1]	D16	Parallel-Only	High-Speed Digital
AD[2]	C16	Parallel-Only	High-Speed Digital
AD[3]	D15	Parallel-Only	High-Speed Digital
AD[4]	C15	Parallel-Only	High-Speed Digital
AD[5]	E14	Parallel-Only	High-Speed Digital
AD[6]	D14	Parallel-Only	High-Speed Digital
AD[7]	C14	Parallel-Only	High-Speed Digital
ALE	K14	Parallel-Only	High-Speed Digital
AVDD_PLL1	D1	All	Power Supply
AVDD_PLL2	E1	All	Power Supply
AVDD_PLL3	F1	All	Power Supply
AVDD_PLL4	G1	All	Power Supply
AVSS_PLL1	D2	All	Power Supply
AVSS_PLL2	E3	All	Power Supply
AVSS_PLL3	G2	All	Power Supply
AVSS_PLL4	G3	All	Power Supply
CPHA	D14	SPI-Only	Low-Speed Digital
CPOL	C14	SPI-Only	Low-Speed Digital
$\overline{CS}$	J16	All	High-Speed Digital
$\overline{DS}$	J14	Parallel-Only	High-Speed Digital
DV_{DD}	H3	All	Power Supply
DV_{SS}	P8	All	Power Supply
GPIO1	E2	All	Low-Speed Digital
GPIO2	F3	All	Low-Speed Digital
GPIO3	H2	All	Low-Speed Digital
GPIO4	J1	All	Low-Speed Digital
$\overline{HIZ}$	R14	All	Low-Speed Digital
IC1A	P6	All	Low-Speed Analog
IC2A	P7	All	Low-Speed Analog
IC3	C10	All	High-Speed Digital

PIN NAME	PIN NUMBER	BUS MODES	SIGNAL TYPE
IC4	A11	All	High-Speed Digital
IFSEL[0]	N1	All	Low-Speed Digital
IFSEL[1]	N2	All	Low-Speed Digital
IFSEL[2]	P1	All	Low-Speed Digital
INTREQ	A15	All	Low-Speed Digital
JTCLK	R8	All	Low-Speed Digital
JTDI	R9	All	Low-Speed Digital
JTDO	P9	All	Low-Speed Digital
JTMS	T9	All	Low-Speed Digital
$\overline{\text{JTRST}}$	T8	All	Low-Speed Digital
MASTSLV	R11	All	Low-Speed Digital
MCLK1	F2	All	Low-Speed Digital
MCLK2	T10	All	Low-Speed Digital
N.C.	A3, A4, A5, A7, A8, A10, A12, A13, A14, B3, B4, B5, B7, B8, B9, B10, B11, B12, B13, B14, C1, C2, C6, C7, C8, C9, C11, C12, C13, F14, M2, P12	All	No Connection
OC9	A9	All	Low-Speed Digital
R/$\overline{\text{W}}$	J15	Parallel-Only	High-Speed Digital
RCLK1	K1	All	Low-Speed Digital
RCLK2	R10	All	Low-Speed Digital
$\overline{\text{RD}}$	J14	Parallel-Only	High-Speed Digital
$\overline{\text{RDY}}$	B15	Parallel-Only	High-Speed Digital
REFCLK	H1	All	Low-Speed Digital
RESREF	T7	All	Low-Speed Analog
ROUT1	K2	All	Low-Speed Digital
ROUT2	P10	All	Low-Speed Digital
RRING1	R5	All	Low-Speed Analog
RRING2	L15	All	Low-Speed Analog
RSER1	J3	All	Low-Speed Digital
RSER2	T11	All	Low-Speed Digital
$\overline{\text{RST}}$	B6	All	Low-Speed Digital
RTIP1	T5	All	Low-Speed Analog
RTIP2	L16	All	Low-Speed Analog
RVDD_P1	T4	All	Power Supply
RVDD_P2	M15	All	Power Supply
RVSS_P1	P5	All	Power Supply
RVSS_P2	M14	All	Power Supply
SCLK	C16	SPI-Only	Low-Speed Digital
SDI	D16	SPI-Only	Low-Speed Digital
SDO	E15	SPI-Only	Low-Speed Digital
SONSDH	M3	All	Low-Speed Digital
TCLK1	L2	All	Low-Speed Digital
TCLK2	T12	All	Low-Speed Digital
THZE1	K3	All	Low-Speed Digital
THZE2	T14	All	Low-Speed Digital

PIN NAME	PIN NUMBER	BUS MODES	SIGNAL TYPE
TIN1	L1	All	Low-Speed Digital
TIN2	R12	All	Low-Speed Digital
TM1	R13	All	Test, Wire Low
TM2	T15	All	Test, Wire Low
TOUT1	M1	All	Low-Speed Digital
TOUT2	P11	All	Low-Speed Digital
TRING1	R2, T2	All	Low-Speed Analog
TRING2	P15, P16	All	Low-Speed Analog
TSER1	L3	All	Low-Speed Digital
TSER2	T13	All	Low-Speed Digital
TST_RA1	R6	All	Test, Do Not Connect
TST_RA2	L14	All	Test, Do Not Connect
TST_RB1	T6	All	Test, Do Not Connect
TST_RB2	K16	All	Test, Do Not Connect
TST_RC1	R7	All	Test, Do Not Connect
TST_RC2	K15	All	Test, Do Not Connect
TST_TA1	P2	All	Test, Do Not Connect
TST_TA2	R15	All	Test, Do Not Connect
TST_TB1	N3	All	Test, Do Not Connect
TST_TB2	P13	All	Test, Do Not Connect
TST_TC1	P3	All	Test, Do Not Connect
TST_TC2	P14	All	Test, Do Not Connect
TTIP1	R3, T3	All	Low-Speed Analog
TTIP2	N15, N16	All	Low-Speed Analog
TVDD_P1	R4	All	Power Supply
TVDD_P2	M16	All	Power Supply
TVSS_P1	P4	All	Power Supply
TVSS_P2	N14	All	Power Supply
V_{DD}	D6, D8, D9, D11, E6, E11, F4, F5, F12, F13, H4, H13, J4, J13, L4, L5, L12, L13, M6, M11, N6, N8, N9, N11	All	Power Supply
VDD_ICDIFF	A6	All	Power Supply
VDD_OC6	B2	All	Power Supply
VDD_OC7	C3	All	Power Supply
V_{DDIO}	B1, B16, D7, D10, E7–E10, G4, G5, G12, G13, H5, H12, J5, J12, K4, K5, K12, K13, M7, M8, M9, M10, N7, N10, R1, R16	All	Power Supply
V_{SS}	A1, A16, D4, D5, D12, D13, E4, E5, E12, E13, F6–F11, G6–G11, H6–H11, J2, J6–J11, K6–K11, L6–L11, M4, M5, M12, M13, N4, N5, N12, N13, T1, T16	All	Power Supply
VSS_ICDIFF	C4	All	Power Supply
VSS_OC6	A2	All	Power Supply
VSS_OC7	D3	All	Power Supply
WDT	C5	All	Low-Speed Analog

PIN NAME	PIN NUMBER	BUS MODES	SIGNAL TYPE
$\overline{WR}$	J15	Parallel-Only	High-Speed Digital

Figure 10-1. ZL81000 Pin Assignment—Left Half

	1	2	3	4	5	6	7	8
A	V_{SS}	VSS_OC6	N.C.	N.C.	N.C.	VDD_ICDIFF	N.C.	N.C.
B	V_{DDIO}	VDD_OC6	N.C.	N.C.	N.C.	$\overline{RST}$	N.C.	N.C.
C	N.C.	N.C.	VDD_OC7	VSS_ICDIFF	WDT	N.C.	N.C.	N.C.
D	AVDD_PLL1	AVSS_PLL1	VSS_OC7	V_{SS}	V_{SS}	V_{DD}	V_{DDIO}	V_{DD}
E	AVDD_PLL2	GPIO1	AVSS_PLL2	V_{SS}	V_{SS}	V_{DD}	V_{DDIO}	V_{DDIO}
F	AVDD_PLL3	MCLK1	GPIO2	V_{DD}	V_{DD}	V_{SS}	V_{SS}	V_{SS}
G	AVDD_PLL4	AVSS_PLL3	AVSS_PLL4	V_{DDIO}	V_{DDIO}	V_{SS}	V_{SS}	V_{SS}
H	REFCLK	GPIO3	DV_{DD}	V_{DD}	V_{DDIO}	V_{SS}	V_{SS}	V_{SS}
J	GPIO4	V_{SS}	RSER1	V_{DD}	V_{DDIO}	V_{SS}	V_{SS}	V_{SS}
K	RCLK1	ROUT1	THZE1	V_{DDIO}	V_{DDIO}	V_{SS}	V_{SS}	V_{SS}
L	TIN1	TCLK1	TSER1	V_{DD}	V_{DD}	V_{SS}	V_{SS}	V_{SS}
M	TOUT1	N.C.	SONSDH	V_{SS}	V_{SS}	V_{DD}	V_{DDIO}	V_{DDIO}
N	IFSEL[0]	IFSEL[1]	TST_TB1	V_{SS}	V_{SS}	V_{DD}	V_{DDIO}	V_{DD}
P	IFSEL[2]	TST_TA1	TST_TC1	TVSS_P1	RVSS_P1	IC1A	IC2A	DV_{SS}
R	V_{DDIO}	TRING1	TTIP1	TVDD_P1	RRING1	TST_RA1	TST_RC1	JTCLK
T	V_{SS}	TRING1	TTIP1	RVDD_P1	RTIP1	TST_RB1	RESREF	$\overline{JTRST}$
	1	2	3	4	5	6	7	8

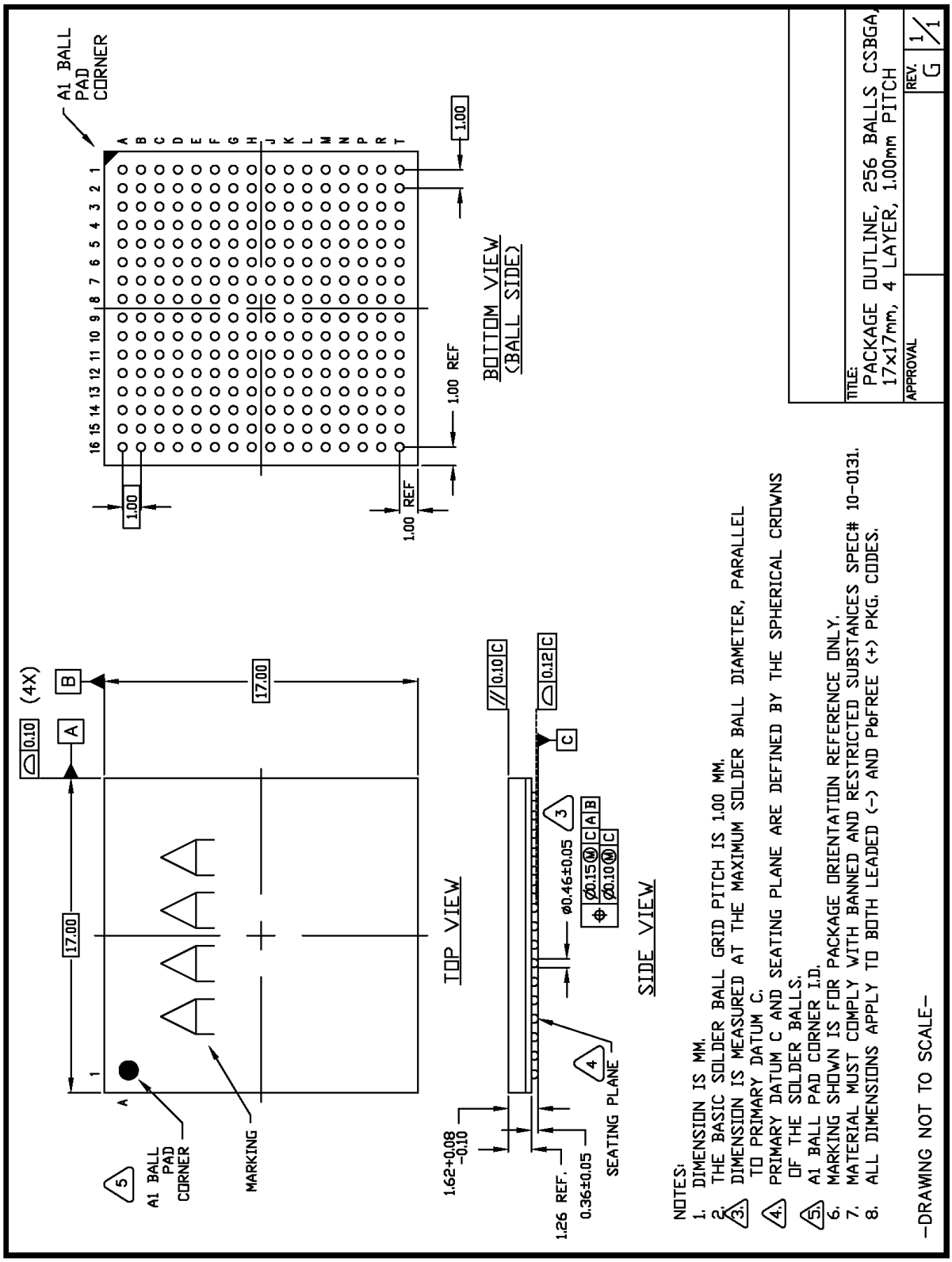
- High-Speed Analog
- Low-Speed Analog
- High-Speed Digital
- Low-Speed Digital
- V_{DD} 3.3V
- V_{DD} 1.8V
- Analog V_{DD} 3.3V
- Analog V_{DD} 1.8V
- V_{SS}
- Analog V_{SS}
- N.C. = No Connection. Lead is not connected to anything inside the device.

Figure 10-2. ZL81000 Pin Assignment—Right Half

9	10	11	12	13	14	15	16	
OC9	N.C.	IC4	N.C.	N.C.	N.C.	INTREQ	VSS	A
N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	$\overline{RDY}$	VDDIO	B
N.C.	IC3	N.C.	N.C.	N.C.	AD[7]/CPOL	AD[4]	AD[2]/SCLK	C
V_{DD}	V_{DDIO}	V_{DD}	V_{SS}	V_{SS}	AD[6]/CPHA	AD[3]	AD[1] / SDI	D
V_{DDIO}	V_{DDIO}	V_{DD}	V_{SS}	V_{SS}	AD[5]	AD[0]/SDO	A[8]	E
V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DD}	N.C.	A[7]	A[5]	F
V_{SS}	V_{SS}	V_{SS}	V_{DDIO}	V_{DDIO}	A[6]	A[4]	A[2]	G
V_{SS}	V_{SS}	V_{SS}	V_{DDIO}	V_{DD}	A[3]	A[1]	A[0]	H
V_{SS}	V_{SS}	V_{SS}	V_{DDIO}	V_{DD}	$\overline{RD}/\overline{DS}$	$\overline{WR}$/R/$\overline{W}$	$\overline{CS}$	J
V_{SS}	V_{SS}	V_{SS}	V_{DDIO}	V_{DDIO}	ALE	TST_RC2	TST_RB2	K
V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DD}	TST_RA2	RRING2	RTIP2	L
V_{DDIO}	V_{DDIO}	V_{DD}	V_{SS}	V_{SS}	RVSS_P2	RVDD_P2	TVDD_P2	M
V_{DD}	V_{DDIO}	V_{DD}	V_{SS}	V_{SS}	TVSS_P2	TTIP2	TTIP2	N
JTDO	ROUT2	TOUT2	N.C.	TST_TB2	TST_TC2	TRING2	TRING2	P
JTDI	RCLK2	MASTSLV	TIN2	TM1	$\overline{HIZ}$	TST_TA2	V_{DDIO}	R
JTMS	MCLK2	RSER2	TCLK2	TSER2	THZE2	TM2	V_{SS}	T
9	10	11	12	13	14	15	16	

- Low-Speed Analog
- High-Speed Digital
- Low-Speed Digital
- V_{DD} 3.3V
- V_{DD} 1.8V
- Analog V_{DD} 3.3V
- Analog V_{DD} 1.8V
- V_{SS}
- Analog V_{SS}
- N.C. = No Connection. Lead is not connected to anything inside the device.

11. PACKAGE INFORMATION



12. THERMAL INFORMATION

Table 12-1. Thermal Properties, Natural Convection

PARAMETER	MIN	TYP	MAX	UNITS
Ambient Temperature (Note 1)	-40		+85	°C
Junction Temperature	-40		+125	°C
Theta-JA (θ_{JA}), Still Air (Note 2)		26.7		°C/W
Theta-JB (θ_{JB}), Still Air		14.0		°C/W
Theta-JC (θ_{JC}), Still Air		11.0		°C/W
Psi-JB		13.5		°C/W
Psi-JT		0.7		°C/W

Note 1: The package is mounted on a four-layer JEDEC standard test board with no airflow and dissipating maximum power.

Note 2: Theta-JA (θ_{JA}) is the junction to ambient thermal resistance, when the package is mounted on a four-layer JEDEC standard test board with no airflow and dissipating maximum power.

13. GLOSSARY

Local Oscillator The 12.800MHz TCXO, OCXO, or other crystal oscillator connected to the REFCLK pin.

Master Clock A 204.8MHz clock synthesized from the local oscillator and frequency adjusted by the XOFREQ register setting.

Input Clock One of the four input clocks labeled IC1A, IC2A, IC3, IC4.

Output Clock Signal OC9

Selected Reference The input clock to which the DPLL is currently phase locked.

Valid Clock An input clock that has no alarms declared in the corresponding ISR register. A clock whose frequency is within the hard limit set in ILIMIT or CLIMIT and that does not have an inactivity alarm.

Invalid Clock An input clock that has one or more alarms declared in the corresponding ISR register.

14. ACRONYMS AND ABBREVIATIONS

AIS	Alarm Indication Signal
AMI	Alternate Mark Inversion
APLL	Analog Phase-Locked Loop
BITS	Building Integrated Timing Supply
BPV	Bipolar Violation
DFS	Digital Frequency Synthesis
DPLL	Digital Phase Locked Loop
ESF	Extended Superframe
EXZ	Excessive Zeros
GbE	Gigabit Ethernet
I/O	Input/Output
LOS	Loss of Signal
LVDS	Low-Voltage-Differential Signal
LVPECL	Low-Voltage Positive Emitter-Coupled Logic
MTIE	Maximum Time Interval Error
OCXO	Oven-Controlled Crystal Oscillator
OOF	Out-of-Frame Alignment
PBO	Phase Build-Out
PFD	Phase/Frequency Detector
PLL	Phase-Locked Loop
ppb	Parts per Billion
ppm	Parts per Million
pk-pk	Peak-to-Peak
RMS	Root-Mean-Square
RAI	Remote Alarm Indication
RO	Read-Only
R/W	Read/Write
SDH	Synchronous Digital Hierarchy
SEC	SDH Equipment Clock
SETS	Synchronous Equipment Timing Source
SF	Superframe
SONET	Synchronous Optical Network
SSM	Synchronization Status Message
SSU	Synchronization Supply Unit
STM	synchronous Transport Module
TDEV	Time Deviation
TCXO	Temperature-Compensated Crystal Oscillator
UI	Unit Interval
UI_{P-P}	Unit Interval, Peak to Peak

15. TRADEMARK ACKNOWLEDGEMENTS

16. DATA SHEET REVISION HISTORY

REVISION DATE	DESCRIPTION
17-Oct-2016	First general release
29-Mar-2018	In BCCR1:TCLKS register definition, added the missing 1001=OC9 decode. In Table 10-1 and Figure 10-1 changed J2 to VSS.
29-May-2018	In Table 5-10 moved TM1 and TM2 to the Name column and R13 and T15 to the Pin column. In Table 10-1 deleted the SYNC2K B14 row that did not belong. In Figure 10-2 corrected the name of pin K14 from $\overline{\text{ALE}}$ to ALE.
28-Aug-2018	Added BCCR2 register definition.

Microsemi Headquarters
One Enterprise
Aliso Viejo, CA 92656 USA

Within the USA: +1 (800) 713-4113
Outside the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996

E-mail: sales.support@microsemi.com

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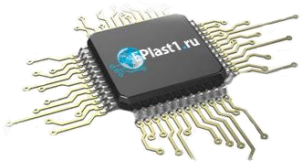
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



Как с нами связаться

Телефон: 8 (812) 309 58 32 (многоканальный)
Факс: 8 (812) 320-02-42
Электронная почта: org@eplast1.ru
Адрес: 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.