

### FEATURES

- Very low noise density of 5 nV/ $\sqrt{\text{Hz}}$  at 1 kHz maximum**
- Excellent input offset voltage of 75  $\mu\text{V}$  maximum**
- Low offset voltage drift of 1  $\mu\text{V}/^\circ\text{C}$  maximum**
- Very high gain of 1500 V/mV minimum**
- Outstanding CMR of 106 dB minimum**
- Slew rate of 2.4 V/ $\mu\text{s}$  typical**
- Gain bandwidth product of 5 MHz typical**
- Industry-standard 8-lead dual pinout**

### FUNCTIONAL BLOCK DIAGRAMS

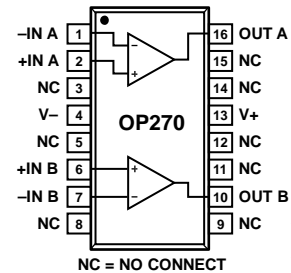


Figure 1. 16-Lead SOIC  
(S-Suffix)

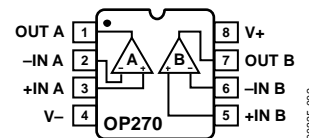


Figure 2. 8-Lead PDIP (P-Suffix)  
8-Lead CERDIP  
(Z-Suffix)

### GENERAL DESCRIPTION

The OP270 is a high performance, monolithic, dual operational amplifier with exceptionally low voltage noise density (5 nV/ $\sqrt{\text{Hz}}$  maximum at 1 kHz). It offers comparable performance to the industry-standard [OP27](#) from Analog Devices, Inc.

The OP270 features an input offset voltage of less than 75  $\mu\text{V}$  and an offset drift of less than 1  $\mu\text{V}/^\circ\text{C}$ , guaranteed over the full military temperature range. Open-loop gain of the OP270 is more than 1,500,000 into a 10 k $\Omega$  load, ensuring excellent gain accuracy and linearity, even in high gain applications. The input bias current is less than 20 nA, which reduces errors due to signal source resistance. With a common-mode rejection (CMR) of greater than 106 dB and a power supply rejection ratio (PSRR) of less than 3.2  $\mu\text{V}/\text{V}$ , the OP270 significantly reduces errors due to ground noise and power supply fluctuations. The power consumption of the dual OP270 is one-third less than two OP27

devices, a significant advantage for power conscious applications. The OP270 is unity-gain stable with a gain bandwidth product of 5 MHz and a slew rate of 2.4 V/ $\mu\text{s}$ .

The OP270 offers excellent amplifier matching, which is important for applications such as multiple gain blocks, low noise instrumentation amplifiers, dual buffers, and low noise active filters.

The OP270 conforms to the industry-standard 8-lead DIP pinout. It is pin compatible with the MC1458, SE5532/A, RM4558, and HA5102 dual op amps, and can be used to upgrade systems using those devices.

For higher speed applications, the [ADA4004-2](#) or the [AD8676](#) are recommended. For a quad op amp, see the [OP470](#) data sheet.

#### Rev. E

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective owners.

## TABLE OF CONTENTS

|   |    |  |    |
|---|----|--|----|
| Features .....                            | 1  | Voltage and Current Noise .....                            | 12 |
| Functional Block Diagrams.....            | 1  | Total Noise and Source Resistance.....                     | 12 |
| General Description .....                 | 1  | Noise Measurements.....                                    | 14 |
| Revision History .....                    | 2  | Capacitive Load Driving and Power Supply Considerations .. | 15 |
| Specifications.....                       | 3  | Unity-Gain Buffer Applications .....                       | 15 |
| Electrical Specifications.....            | 4  | Low Phase Error Amplifier .....                            | 16 |
| Absolute Maximum Ratings.....             | 5  | Five-Band, Low Noise, Stereo Graphic Equalizer .....       | 16 |
| ESD Caution.....                          | 5  | Digital Panning Control .....                              | 17 |
| Typical Performance Characteristics ..... | 6  | Dual Programmable Gain Amplifier .....                     | 17 |
| Test Circuits.....                        | 11 | Outline Dimensions .....                                   | 19 |
| Applications Information .....            | 12 | Ordering Guide .....                                       | 20 |

## REVISION HISTORY

### 2/10—Rev. D to Rev. E

|  |    |
|--|----|
| Change to General Description Section .....                    | 1  |
| Change to Input Noise Current Density Parameter, Table 1 ..... | 3  |
| Change to Figure 18 .....                                      | 8  |
| Changes to Total Noise and Source Resistance Section .....     | 13 |
| Changes to Figure 41 .....                                     | 16 |

### 2/09—Rev. C to Rev. D

|                                    |           |
|------------------------------------|-----------|
| Updated Format .....               | Universal |
| Reorganized Layout.....            | Universal |
| Changes to Figure 7 .....          | 6         |
| Changes to Figure 22.....          | 9         |
| Deleted Applications Heading ..... | 11        |
| Changes to Figure 44.....          | 17        |
| Changes to Figure 46.....          | 18        |
| Updated Outline Dimensions .....   | 19        |
| Changes to Ordering Guide .....    | 20        |

### 4/03—Rev. B to Rev. C

|   |           |
|---|-----------|
| Deletion of OP270A model.....                           | Universal |
| Edits to Features.....                                  | 1         |
| Changes to Specifications.....                          | 2         |
| Deletion of Wafer Limits and Dice Characteristics ..... | 4         |
| Changes to Absolute Maximum Ratings.....                | 4         |
| Changes to Ordering Guide .....                         | 4         |
| Changes to Equations in Noise Measurements section..... | 10        |
| Change to Figure 10 .....                               | 11        |
| Updated Outline Dimensions .....                        | 14        |

### 11/02—Rev. A to Rev. B

|                              |    |
|------------------------------|----|
| Updated Ordering Guide ..... | 15 |
|------------------------------|----|

### 9/02—Rev. 0 to Rev. A

|   |    |
|---|----|
| Edits to Absolute Maximum Ratings ..... | 5  |
| Edits to Ordering Guide .....           | 15 |

### 2/01—Revision 0: Initial Version

# SPECIFICATIONS

$V_S = \pm 15\text{ V}$ ,  $T_A = 25^\circ\text{C}$ , unless otherwise noted.

Table 1.

| Parameter                                | Symbol    | Test Conditions  | OP270E   |            |     | OP270F   |            |     | OP270G   |            |                        | Unit            |
|--|-----------|--|----------|------------|-----|----------|------------|-----|----------|------------|------------------------|-----------------|
|  |           |  | Min      | Typ        | Max | Min      | Typ        | Max | Min      | Typ        | Max                    |                 |
| Input Offset Voltage                     | $V_{OS}$  |  | 10       | 75         |     | 20       | 150        |     | 50       | 250        | $\mu\text{V}$          |                 |
| Input Offset Current                     | $I_{OS}$  | $V_{CM} = 0\text{ V}$                                  | 1        | 10         |     | 3        | 15         |     | 5        | 20         | nA                     |                 |
| Input Bias Current                       | $I_B$     | $V_{CM} = 0\text{ V}$                                  | 5        | 20         |     | 10       | 40         |     | 15       | 60         | nA                     |                 |
| Input Noise Voltage <sup>1</sup>         | $e_n$ p-p | 0.1 Hz to 10 Hz  | 80       | 200        |     | 80       | 200        |     | 80       |            | nV p-p                 |                 |
| Input Noise Voltage Density <sup>2</sup> | $e_n$     | $f_o = 10\text{ Hz}$                                   | 3.6      | 6.5        |     | 3.6      | 6.5        |     | 3.6      |            | nV/ $\sqrt{\text{Hz}}$ |                 |
|  | $e_n$     | $f_o = 100\text{ Hz}$                                  | 3.2      | 5.5        |     | 3.2      | 5.5        |     | 3.2      |            | nV/ $\sqrt{\text{Hz}}$ |                 |
|  | $e_n$     | $f_o = 1\text{ kHz}$                                   | 3.2      | 5.0        |     | 3.2      | 5.0        |     | 3.2      |            | nV/ $\sqrt{\text{Hz}}$ |                 |
| Input Noise Current Density              | $i_n$     | $f_o = 10\text{ Hz}$                                   | 1.1      |            |     | 1.1      |            |     | 1.1      |            | pA/ $\sqrt{\text{Hz}}$ |                 |
|  | $i_n$     | $f_o = 100\text{ Hz}$                                  | 0.7      |            |     | 0.7      |            |     | 0.7      |            | pA/ $\sqrt{\text{Hz}}$ |                 |
|  | $i_n$     | $f_o = 1\text{ kHz}$                                   | 0.6      |            |     | 0.6      |            |     | 0.6      |            | pA/ $\sqrt{\text{Hz}}$ |                 |
| Large-Signal Voltage Gain                | $A_{VO}$  | $V_O = \pm 10\text{ V}$ ,<br>$R_L = 10\text{ k}\Omega$ | 1500     | 2300       |     | 1000     | 1700       |     | 750      | 1500       | V/mV                   |                 |
|  |           | $V_O = \pm 10\text{ V}$ ,<br>$R_L = 2\text{ k}\Omega$  | 750      | 1200       |     | 500      | 900        |     | 350      | 700        | V/mV                   |                 |
| Input Voltage Range <sup>3</sup>         | IVR       |  | $\pm 12$ | $\pm 12.5$ |     | $\pm 12$ | $\pm 12.5$ |     | $\pm 12$ | $\pm 12.5$ | V                      |                 |
| Output Voltage Swing                     | $V_O$     | $R_L \geq 2\text{ k}\Omega$                            | $\pm 12$ | $\pm 13.5$ |     | $\pm 12$ | $\pm 13.5$ |     | $\pm 12$ | $\pm 13.5$ | V                      |                 |
| Common-Mode Rejection                    | CMR       | $V_{CM} = \pm 11\text{ V}$                             | 106      | 125        |     | 100      | 120        |     | 90       | 110        | dB                     |                 |
| Power Supply Rejection Ratio             | PSRR      | $V_S = \pm 4.5\text{ V}$<br>to $\pm 18\text{ V}$       |          | 0.56       | 3.2 |          | 1.0        | 5.6 |          | 1.5        | 5.6                    | $\mu\text{V/V}$ |
| Slew Rate                                | SR        |  | 1.7      | 2.4        |     | 1.7      | 2.4        |     | 1.7      | 2.4        | V/ $\mu\text{s}$       |                 |
| Supply Current<br>(All Amplifiers)       | $I_{SY}$  | No load  |          | 4          | 6.5 |          | 4          | 6.5 |          | 4          | 6.5                    | mA              |
| Gain Bandwidth Product                   | GBP       |  |          | 5          |     |          | 5          |     |          | 5          | MHz                    |                 |
| Channel Separation <sup>1</sup>          | CS        | $V_O = \pm 20\text{ V p-p}$ ,<br>$f_o = 10\text{ Hz}$  | 125      | 175        |     | 125      | 175        |     |          | 175        | dB                     |                 |
| Input Capacitance                        | $C_{IN}$  |  |          | 3          |     |          | 3          |     |          | 3          | pF                     |                 |
| Input Resistance                         | $R_{IN}$  | Differential Mode                                      |          | 0.4        |     |          | 0.4        |     |          | 0.4        | M $\Omega$             |                 |
|  |           | Common Mode  |          | 20         |     |          | 20         |     |          | 20         | G $\Omega$             |                 |
| Settling Time                            | $t_S$     | $A_V = +1, 10\text{ V}$ ,<br>step to 0.01%             |          | 5          |     |          | 5          |     |          | 5          | $\mu\text{s}$          |                 |

<sup>1</sup> Guaranteed but not 100% tested.

<sup>2</sup> Sample tested.

<sup>3</sup> Guaranteed by CMR test.

# OP270

## ELECTRICAL SPECIFICATIONS

$V_S = \pm 15\text{ V}$ ,  $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$ , unless otherwise noted.

Table 2.

| Parameter                          | Symbol     | Test Conditions  | OP270E   |            |     | OP270F   |            |     | OP270G   |            |     | Unit                         |
|------------------------------------|------------|--|----------|------------|-----|----------|------------|-----|----------|------------|-----|------------------------------|
|                                    |            |  | Min      | Typ        | Max | Min      | Typ        | Max | Min      | Typ        | Max |                              |
| Input Offset Voltage               | $V_{OS}$   |  | 25       | 150        |     | 45       | 275        |     | 100      | 400        |     | $\mu\text{V}$                |
| Average Input Offset Voltage Drift | $TCV_{OS}$ |  | 0.2      | 1          |     | 0.4      | 2          |     | 0.7      | 3          |     | $\mu\text{V}/^\circ\text{C}$ |
| Input Offset Current               | $I_{OS}$   | $V_{CM} = 0\text{ V}$                                  | 1.5      | 30         |     | 5        | 40         |     | 15       | 50         |     | nA                           |
| Input Bias Voltage                 | $I_B$      | $V_{CM} = 0\text{ V}$                                  | 6        | 60         |     | 15       | 70         |     | 19       | 80         |     | nA                           |
| Large-Signal Voltage Gain          | $A_{VO}$   | $V_O = \pm 10\text{ V}$ ,<br>$R_L = 10\text{ k}\Omega$ | 1000     | 1800       |     | 600      | 1400       |     | 400      | 1250       |     | V/mV                         |
|                                    | $A_{VO}$   | $V_O = \pm 10\text{ V}$ ,<br>$R_L = 2\text{ k}\Omega$  | 500      | 900        |     | 300      | 700        |     | 225      | 670        |     | V/mV                         |
| Input Voltage Range <sup>1</sup>   | IVR        |  | $\pm 12$ | $\pm 12.5$ |     | $\pm 12$ | $\pm 12.5$ |     | $\pm 12$ | $\pm 12.5$ |     | V                            |
| Output Voltage Swing               | $V_O$      | $R_L \geq 2\text{ k}\Omega$                            | $\pm 12$ | $\pm 13.5$ |     | $\pm 12$ | $\pm 13.5$ |     | $\pm 12$ | $\pm 13.5$ |     | V                            |
| Common-Mode Rejection              | CMR        | $V_{CM} = \pm 11\text{ V}$                             | 100      | 120        |     | 94       | 115        |     | 90       | 100        |     | dB                           |
| Power Supply Rejection Ratio       | PSRR       | $V_S = \pm 4.5\text{ V to } \pm 18\text{ V}$           | 0.7      | 5.6        |     | 1.8      | 10         |     | 2.0      | 1.5        |     | $\mu\text{V}/\text{V}$       |
| Supply Current (All Amplifiers)    | $I_{SY}$   | No load  | 4.4      | 7.2        |     | 4.4      | 7.2        |     | 4.4      | 7.2        |     | mA                           |

<sup>1</sup> Guaranteed by CMR test.

## ABSOLUTE MAXIMUM RATINGS

Table 3.

| Parameter                                  | Rating          |
|--|-----------------|
| Supply Voltage                             | 18 V            |
| Differential Input Voltage <sup>1</sup>    | 1.0 V           |
| Differential Input Current <sup>1</sup>    | ±25 mA          |
| Input Voltage                              | Supply voltage  |
| Output Short-Circuit Duration              | Continuous      |
| Storage Temperature Range                  | –65°C to +150°C |
| Lead Temperature Range (Soldering, 60 sec) | 300°C           |
| Junction Temperature (T <sub>j</sub> )     | –65°C to +150°C |
| Operating Temperature Range                | –40°C to +85°C  |

<sup>1</sup> The OP270 inputs are protected by back-to-back diodes. To achieve low noise performance, current-limiting resistors are not used. If the differential voltage exceeds +10 V, the input current should be limited to ±25 mA.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

For military processed devices, refer to the Standard Micro-circuit Drawing (SMD) available at the Defense Logistics Agency website.

Table 4. Analog Devices Equivalent to SMD

| SMD Part Number | Analog Devices Equivalent |
|-----------------|---------------------------|
| 5962-8872101PA  | OP270AZMDA                |

### ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

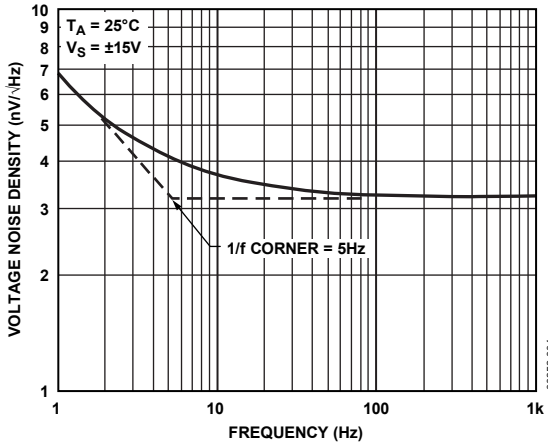


Figure 3. Voltage Noise Density vs. Frequency

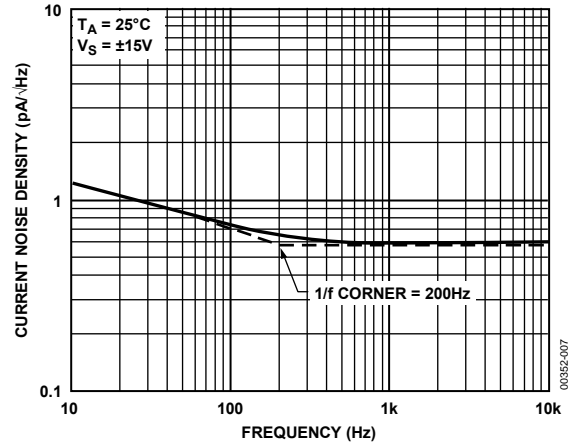


Figure 6. Current Noise Density vs. Frequency

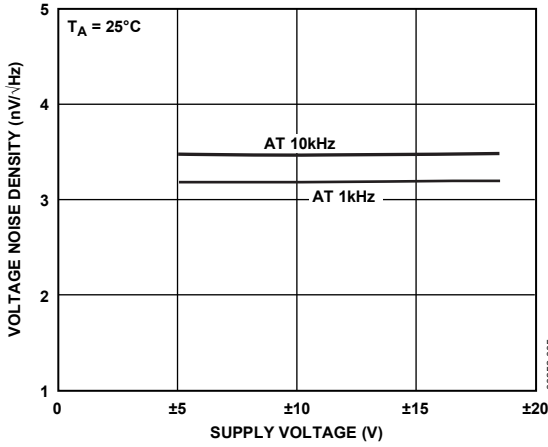


Figure 4. Voltage Noise Density vs. Supply Voltage

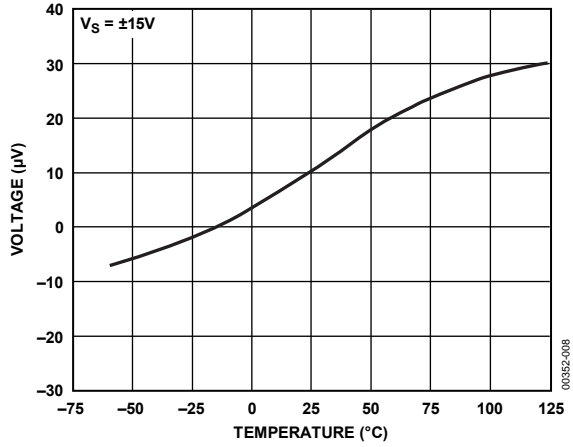


Figure 7. Input Offset Voltage vs. Temperature

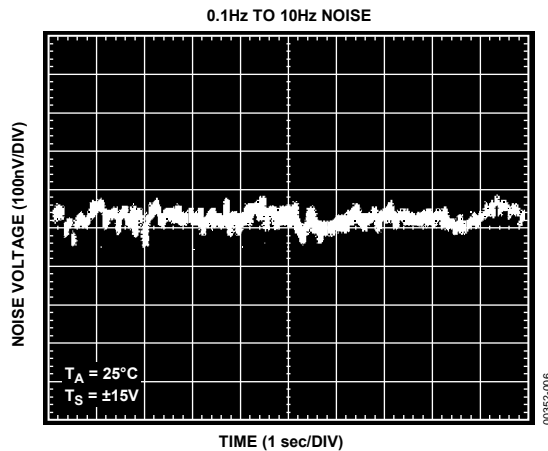


Figure 5. 0.1 Hz to 10 Hz Input Voltage Noise

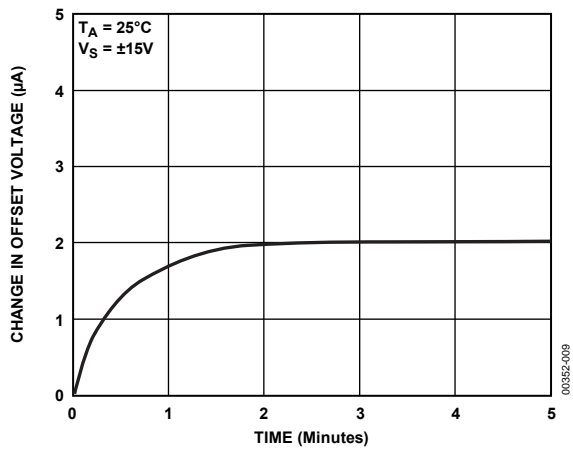


Figure 8. Warm-Up Offset Voltage Drift

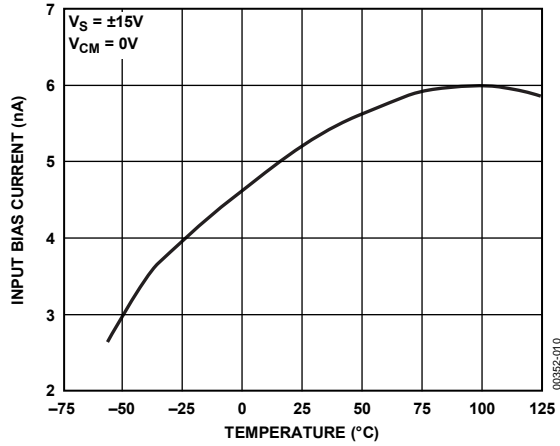


Figure 9. Input Bias Current vs. Temperature

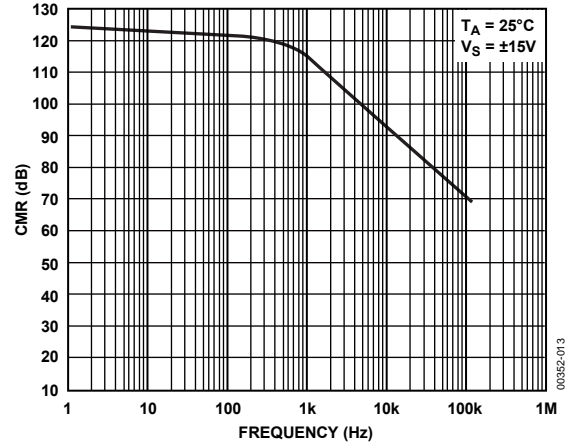


Figure 12. CMR vs. Frequency

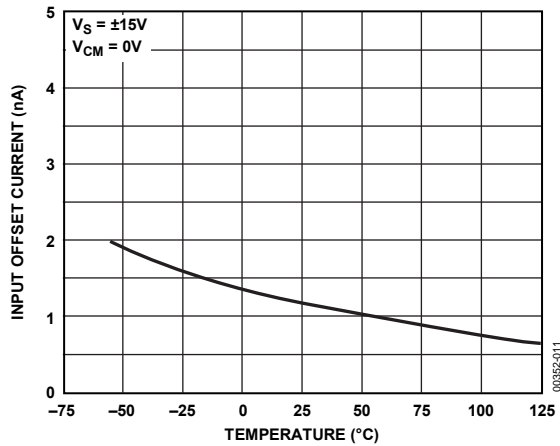


Figure 10. Input Offset Current vs. Temperature

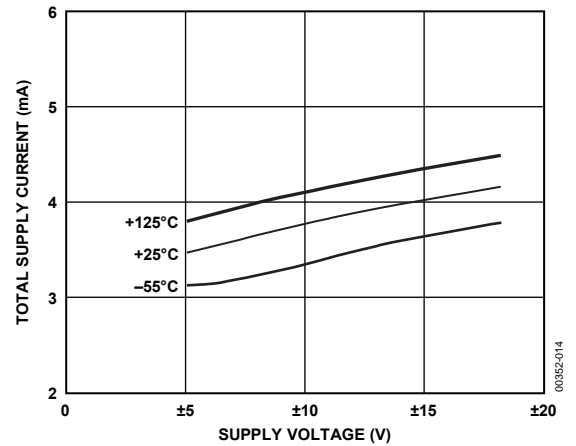


Figure 13. Total Supply Current vs. Supply Voltage

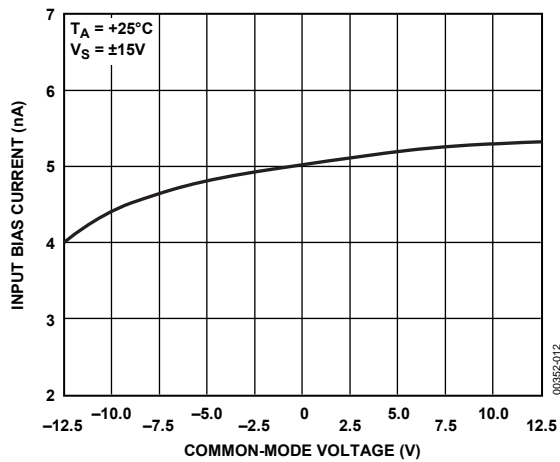


Figure 11. Input Bias Current vs. Common-Mode Voltage

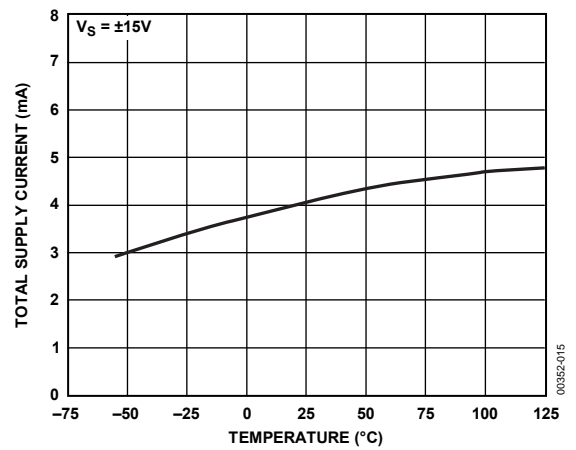


Figure 14. Total Supply Current vs. Temperature

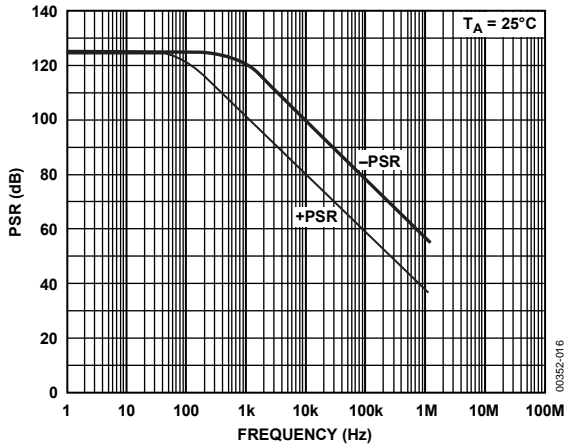


Figure 15. PSR vs. Frequency

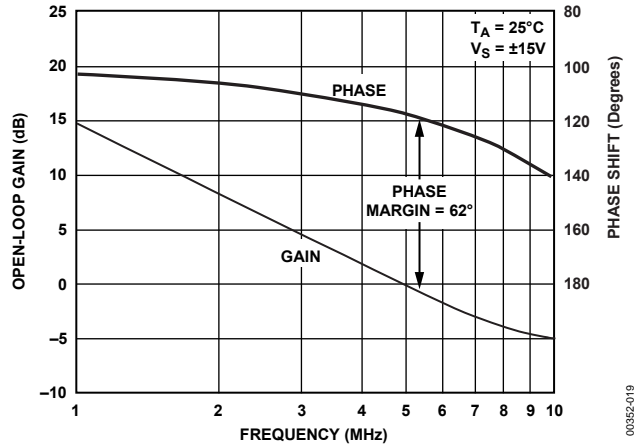


Figure 18. Open-Loop Gain and Phase Shift vs. Frequency

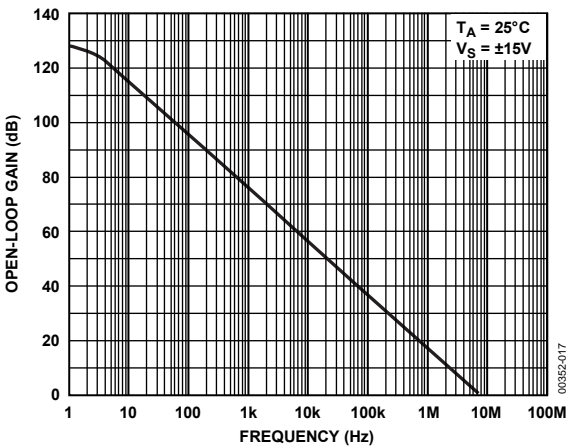


Figure 16. Open-Loop Gain vs. Frequency

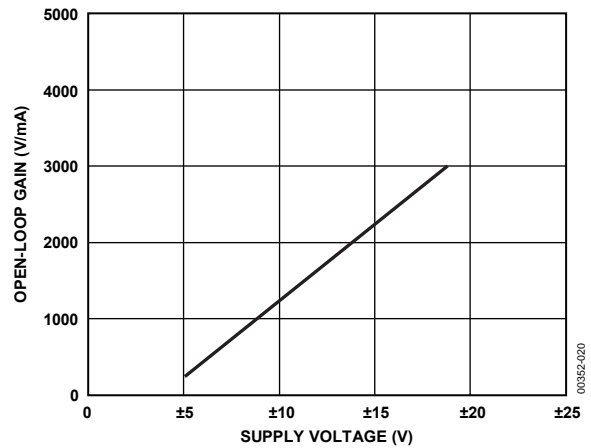


Figure 19. Open-Loop Gain vs. Supply Voltage

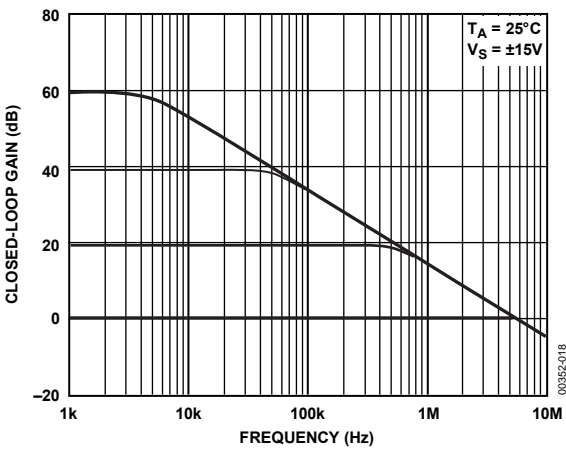


Figure 17. Closed-Loop Gain vs. Frequency

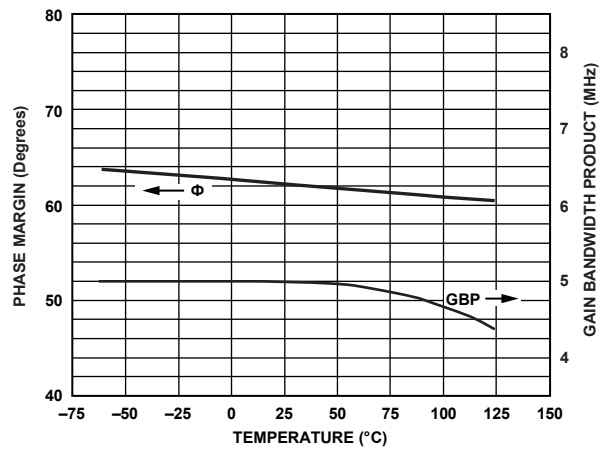


Figure 20. Phase Margin and Gain Bandwidth Product vs. Temperature



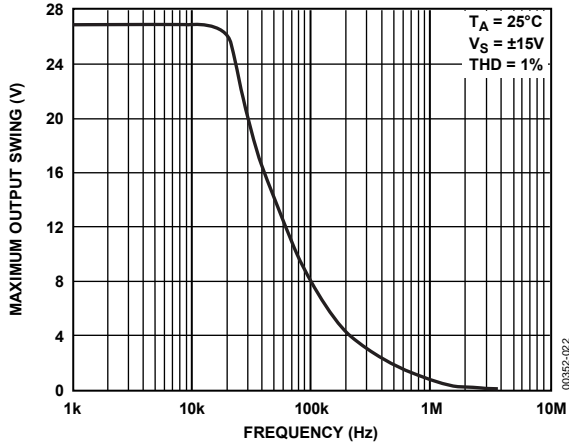


Figure 21. Maximum Output Swing vs. Frequency

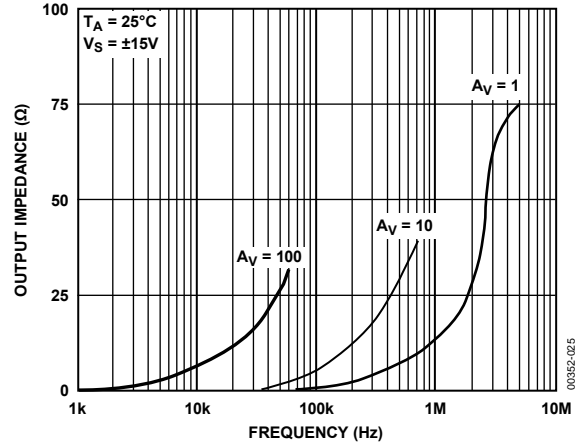


Figure 24. Output Impedance vs. Frequency

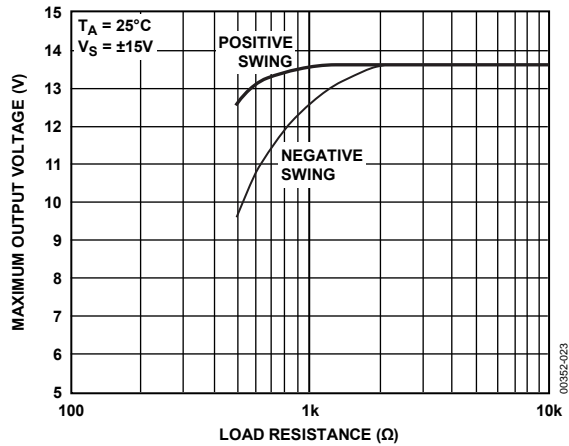


Figure 22. Maximum Output Voltage vs. Load Resistance

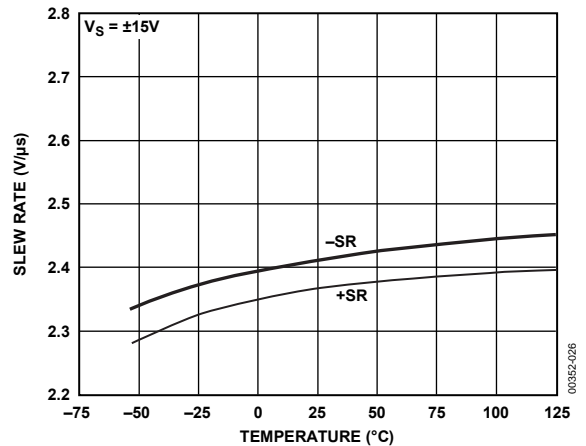


Figure 25. Slew Rate vs. Temperature

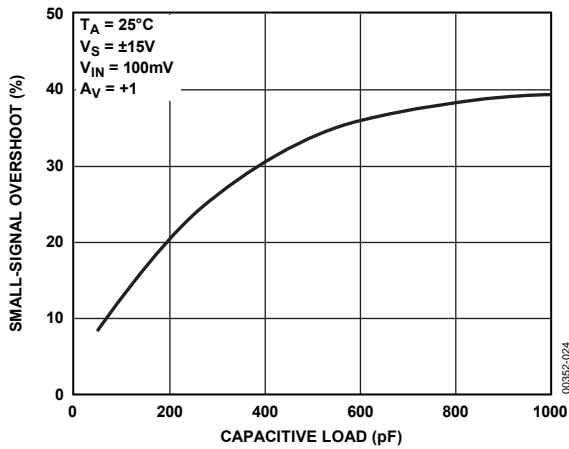


Figure 23. Small-Signal Overshoot vs. Capacitive Load

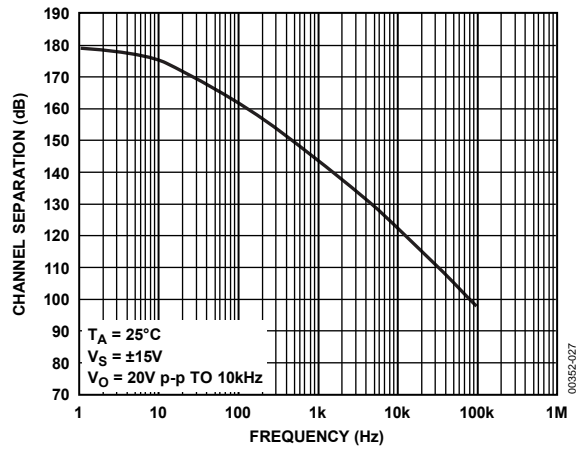


Figure 26. Channel Separation vs. Frequency

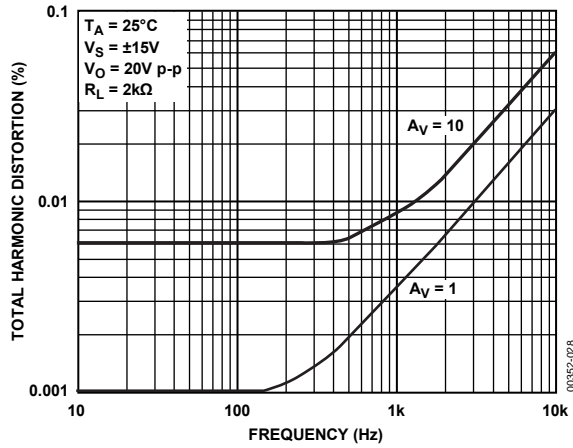


Figure 27. Total Harmonic Distortion vs. Frequency

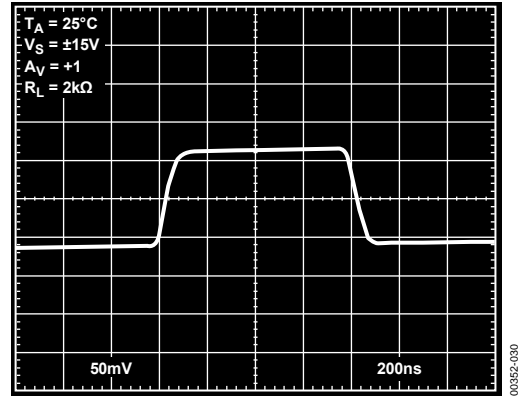


Figure 29. Small-Signal Transient Response

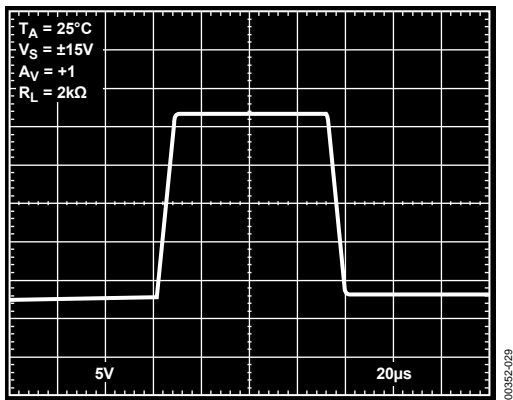


Figure 28. Large-Signal Transient Response

TEST CIRCUITS

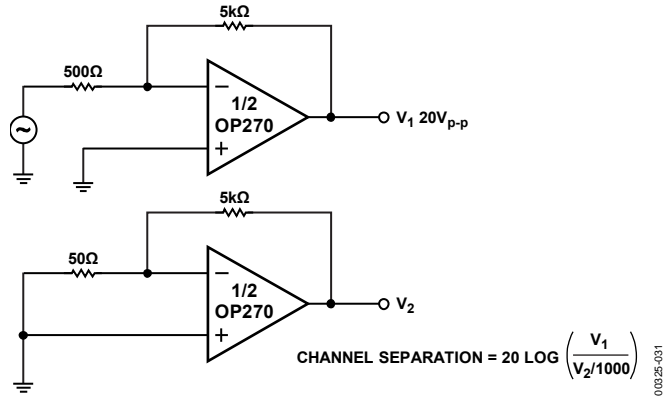


Figure 30. Channel Separation Test Circuit

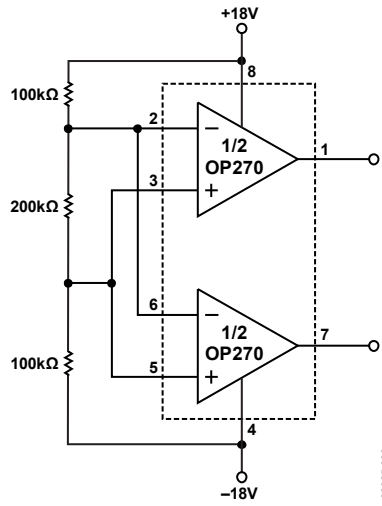


Figure 31. Burn-In Circuit

## APPLICATIONS INFORMATION

### VOLTAGE AND CURRENT NOISE

The OP270 is a very low noise dual op amp, exhibiting a typical voltage noise density of only 3.2 nV/ $\sqrt{\text{Hz}}$  at 1 kHz. Because the voltage noise is inversely proportional to the square root of the collector current, the exceptionally low noise characteristic of the OP270 is achieved in part by operating the input transistors at high collector currents. Current noise, however, is directly proportional to the square root of the collector current. As a result, the outstanding voltage noise density performance of the OP270 is gained at the expense of current noise performance, which is normal for low noise amplifiers.

To obtain the best noise performance in a circuit, it is vital to understand the relationships among voltage noise ( $e_n$ ), current noise ( $i_n$ ), and resistor noise ( $e_t$ ).

### TOTAL NOISE AND SOURCE RESISTANCE

The total noise of an op amp can be calculated by

$$E_n = \sqrt{(e_n)^2 + (i_n R_s)^2 + (e_t)^2}$$

where:

$E_n$  is the total input-referred noise.

$e_n$  is the op amp voltage noise.

$i_n$  is the op amp current noise.

$e_t$  is the source resistance thermal noise.

$R_s$  is the source resistance.

The total noise is referred to the input and at the output is amplified by the circuit gain.

Figure 32 shows the relationship between total noise at 1 kHz and source resistance. When  $R_s$  is less than 1 k $\Omega$ , the total noise is dominated by the voltage noise of the OP270. As  $R_s$  rises above 1 k $\Omega$ , total noise increases and is dominated by resistor noise rather than by the voltage or current noise of the OP270. When  $R_s$  exceeds 20 k $\Omega$ , the current noise of the OP270 becomes the major contributor to total noise.

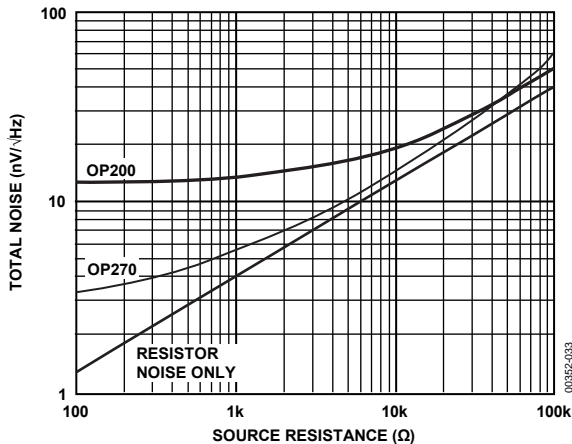


Figure 32. Total Noise vs. Source Resistance (Including Resistor Noise) at 1 kHz

Figure 33 also shows the relationship between total noise and source resistance, but at 10 Hz. Total noise increases more quickly than shown in Figure 32 because current noise is inversely proportional to the square root of frequency. In Figure 33, the current noise of the OP270 dominates the total noise when  $R_s$  is greater than 5 k $\Omega$ .

Figure 32 and Figure 33 show that to reduce total noise, source resistance must be kept to a minimum. In applications with a high source resistance, the OP200, with lower current noise than the OP270, can provide lower total noise.

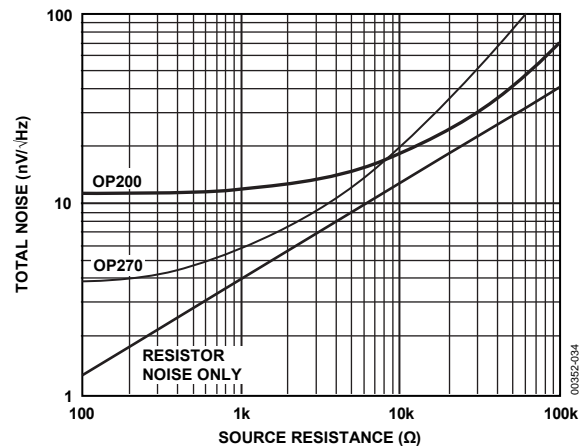


Figure 33. Total Noise vs. Source Resistance (Including Resistor Noise) at 10 Hz

Figure 34 shows peak-to-peak noise vs. source resistance over the 0.1 Hz to 10 Hz range. At low values of  $R_s$ , the voltage noise of the OP270 is the major contributor to peak-to-peak noise, with current noise becoming the major contributor as  $R_s$  increases. The crossover point between the OP270 and the OP200 for peak-to-peak noise is at a source resistance of 17 k $\Omega$ .

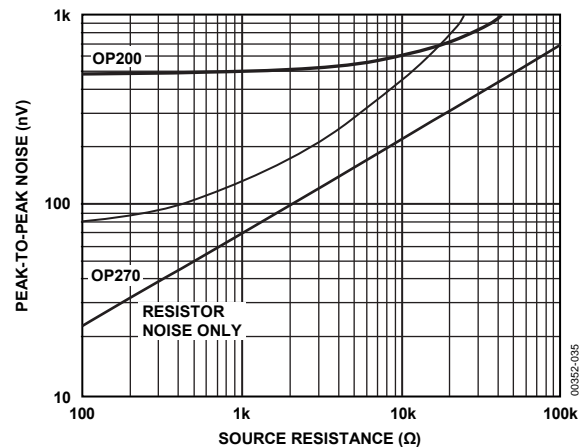


Figure 34. Peak-to-Peak Noise (0.1 Hz to 10 Hz) vs. Source Resistance (Including Resistor Noise)

For reference, typical source resistances of some signal sources are listed in Table 5.

**Table 5. Typical Source Resistances**

| Device                                   | Source Impedance | Comments  |
|--|------------------|---|
| Strain Gage                              | <500 Ω           | Typically used in low frequency applications.   |
| Magnetic Tapehead, Microphone            | <1500 Ω          | Low I <sub>B</sub> is very important to reduce self-magnetization problems when direct coupling is used. OP270 I <sub>B</sub> can be disregarded.               |
| Magnetic Phonograph Cartridge            | <1500 Ω          | Low I <sub>B</sub> is important to reduce self-magnetization problems in direct-coupled applications. OP270 does not introduce any self-magnetization problems. |
| Linear Variable Differential Transformer | <1500 Ω          | Used in rugged servo-feedback applications. The bandwidth of interest is 400 Hz to 5 kHz.   |

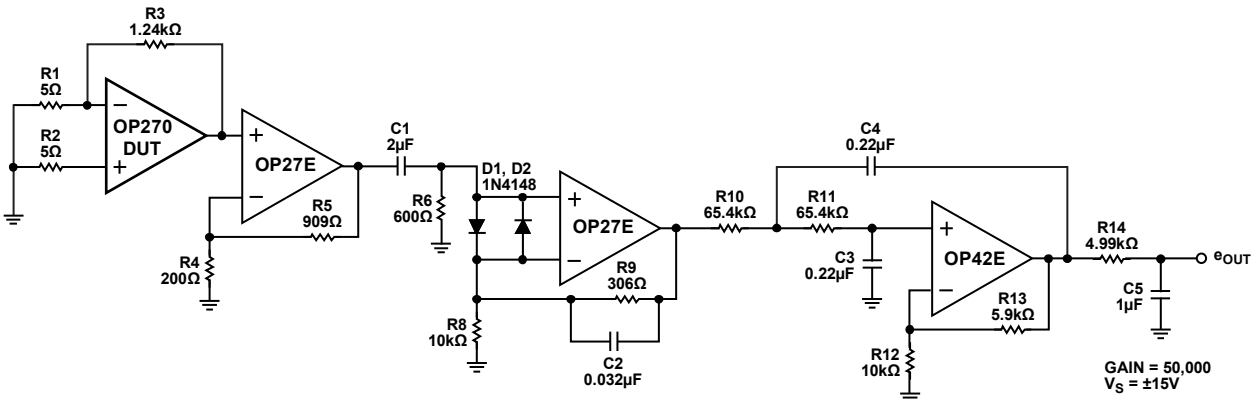


Figure 35. Peak-to-Peak Voltage Noise Test Circuit (0.1 Hz to 10 Hz)

000325-036

## NOISE MEASUREMENTS

### Peak-to-Peak Voltage Noise

The circuit of Figure 35 is a test setup for measuring peak-to-peak voltage noise. To measure the 200 nV peak-to-peak noise specification of the OP270 in the 0.1 Hz to 10 Hz range, the following precautions must be observed:

- The device has to be warmed up for at least five minutes. As shown in the warm-up drift curve (see Figure 8), the offset voltage typically changes 2 μV due to increasing chip temperature after power-up. In the 10 sec measurement interval, these temperature-induced effects can exceed tens of nanovolts.
- For similar reasons, the device has to be well shielded from air currents. Shielding also minimizes thermocouple effects.
- Sudden motion in the vicinity of the device can also feed through to increase the observed noise.
- The test time to measure noise of 0.1 Hz to 10 Hz should not exceed 10 sec. As shown in the noise-tester frequency response curve of Figure 36, the 0.1 Hz corner is defined by only one pole. The test time of 10 sec acts as an additional pole to eliminate noise contribution from the frequency band below 0.1 Hz.
- A noise voltage density test is recommended when measuring noise on several units. A 10 Hz noise voltage density measurement correlates well with a 0.1 Hz to 10 Hz peak-to-peak noise reading because both results are determined by the white noise and the location of the 1/f corner frequency.
- Power should be supplied to the test circuit by well bypassed low noise supplies, such as batteries. Such supplies will minimize output noise introduced via the amplifier supply pins.

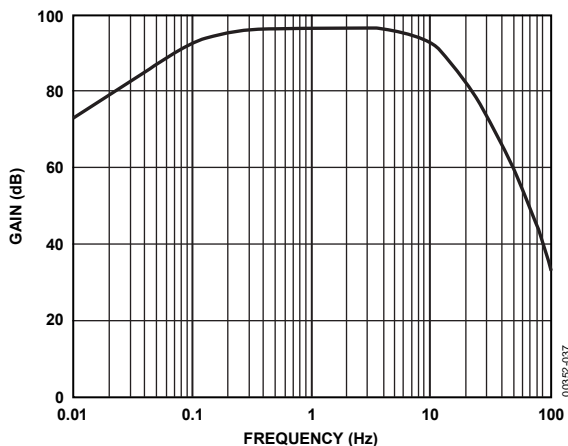


Figure 36. 0.1 Hz to 10 Hz Peak-to-Peak Voltage Noise Test Circuit Frequency Response

### Noise Measurement—Noise Voltage Density

The circuit of Figure 37 shows a quick and reliable method for measuring the noise voltage density of dual op amps. The first amplifier is in unity gain, with the final amplifier in a noninverting gain of 101. Because the noise voltages of the amplifiers are uncorrelated, they add in rms to yield

$$e_{OUT} = 101 \sqrt{(e_{nA})^2 + (e_{nB})^2}$$

The OP270 is a monolithic device with two identical amplifiers. Therefore, the noise voltage densities of the amplifiers match, giving

$$e_{OUT} = 101 (\sqrt{2e_n^2}) = 101 (\sqrt{2}e_n)$$

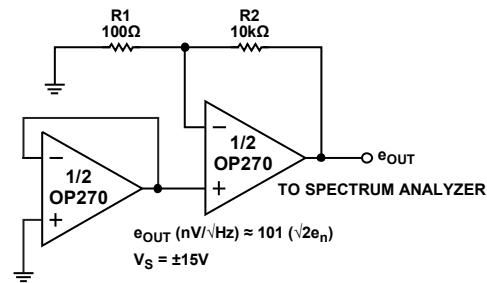


Figure 37. Noise Voltage Density Test Circuit

### Noise Measurement—Current Noise Density

The test circuit shown in Figure 38 can be used to measure current noise density. The formula relating the voltage output to the current noise density is

$$i_n = \frac{\sqrt{\left(\frac{e_{nOUT}}{G}\right)^2 - (40 \text{ nV} / \sqrt{\text{Hz}})^2}}{R_S}$$

where:

G is a gain of 10,000.

R<sub>S</sub> = 100 kΩ source resistance.

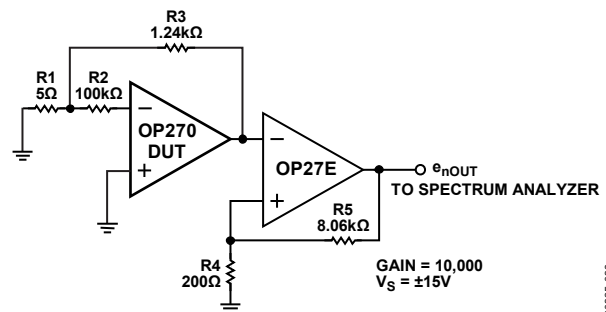


Figure 38. Current Noise Density Test Circuit

**CAPACITIVE LOAD DRIVING AND POWER SUPPLY CONSIDERATIONS**

The OP270 is unity-gain stable and capable of driving large capacitive loads without oscillating. Nonetheless, good supply bypassing is highly recommended. Proper supply bypassing reduces problems caused by supply line noise and improves the capacitive load driving capability of the OP270.

In the standard feedback amplifier, the output resistance of the op amp combines with the load capacitance to form a low-pass filter that adds phase shift in the feedback network and reduces stability. A simple circuit to eliminate this effect is shown in Figure 39. The components C1 and R3 decouple the amplifier from the load capacitance and provide additional stability. The values of C1 and R3 shown in Figure 39 are for a load capacitance of up to 1000 pF when used with the OP270.

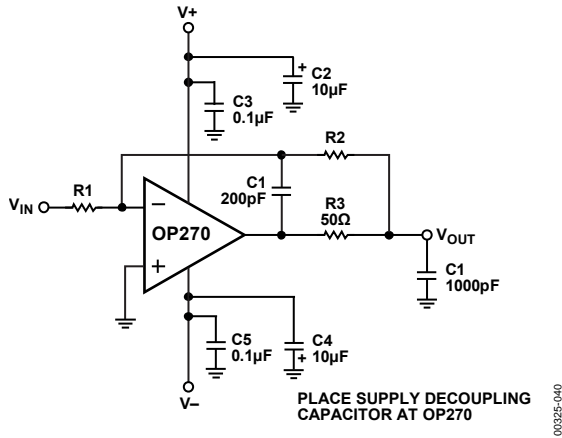


Figure 39. Driving Large Capacitive Loads

**UNITY-GAIN BUFFER APPLICATIONS**

When  $R_f \leq 100 \Omega$  and the input is driven with a fast, large signal pulse ( $>1 \text{ V}$ ), the output waveform looks like the one in Figure 40.

During the fast feedthrough-like portion of the output, the input protection diodes effectively short the output to the input, and a current, limited only by the output short-circuit protection, is drawn by the signal generator. With  $R_f \geq 500 \Omega$ , the output is capable of handling the current requirements ( $I_L \leq 20 \text{ mA}$  at  $10 \text{ V}$ ); the amplifier stays in its active mode and a smooth transition occurs.

When  $R_f > 3 \text{ k}\Omega$ , a pole created by  $R_f$  and the input capacitance ( $3 \text{ pF}$ ) of the amplifier creates additional phase shift and reduces phase margin. A small capacitor ( $20 \text{ pF}$  to  $50 \text{ pF}$ ) in parallel with  $R_f$  helps eliminate this problem.

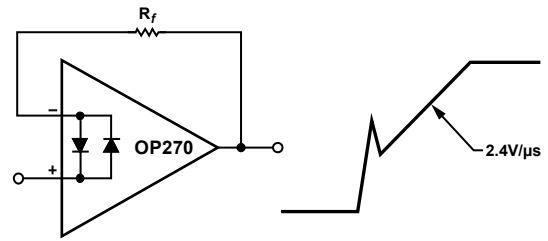


Figure 40. Pulsed Operation

**LOW PHASE ERROR AMPLIFIER**

The simple amplifier depicted in Figure 41 utilizes a monolithic dual operational amplifier and a few resistors to substantially reduce phase error compared with conventional amplifier designs. At a given gain, the frequency range for a specified phase accuracy is more than a decade greater than that of a standard single op amp amplifier.

The low phase error amplifier performs second-order frequency compensation through the response of Op Amp A2 in the feedback loop of A1. Both op amps must be extremely well matched in frequency response. At low frequencies, the A1 feedback loop forces  $V_2/(K_1 + 1) = V_{IN}$ . The A2 feedback loop forces  $V_O/(K_1 + 1) = V_2/(K_1 + 1)$ , yielding an overall transfer function of  $V_O/V_{IN} = K_1 + 1$ . The dc gain is determined by the resistor divider at the output,  $V_O$ , and is not directly affected by the resistor divider around A2. Note that, like a conventional single op amp amplifier, the dc gain is set by resistor ratios only. Minimum gain for the low phase error amplifier is 10.

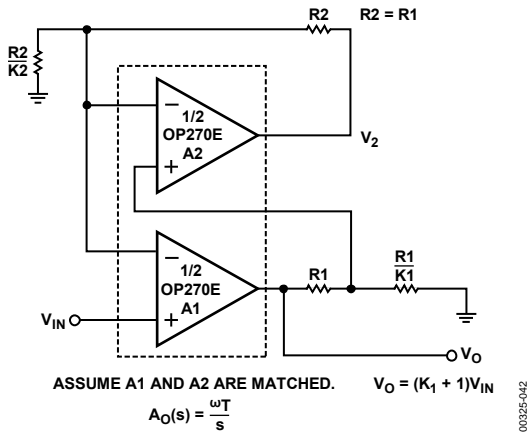


Figure 41. Low Phase Error Amplifier

Figure 42 compares the phase error performance of the low phase error amplifier with a conventional single op amp amplifier and a cascaded two-stage amplifier. The low phase error amplifier shows a much lower phase error, particularly for frequencies where  $\omega/\beta\omega_T < 0.1$ . For example, a phase error of  $-0.1^\circ$  occurs at  $0.002 \omega/\beta\omega_T$  for the single op amp amplifier, but at  $0.11 \omega/\beta\omega_T$  for the low phase error amplifier.

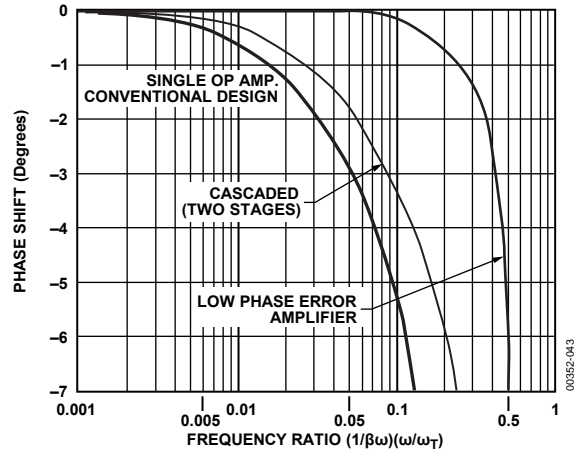


Figure 42. Phase Error Comparison

**FIVE-BAND, LOW NOISE, STEREO GRAPHIC EQUALIZER**

The graphic equalizer circuit shown in Figure 43 provides 15 dB of boost or cut over a five-band range. Signal-to-noise ratio over a 20 kHz bandwidth is better than 100 dB and referred to a 3 V rms input. Larger inductors can be replaced by active inductors, but consequently reduces the signal-to-noise ratio.

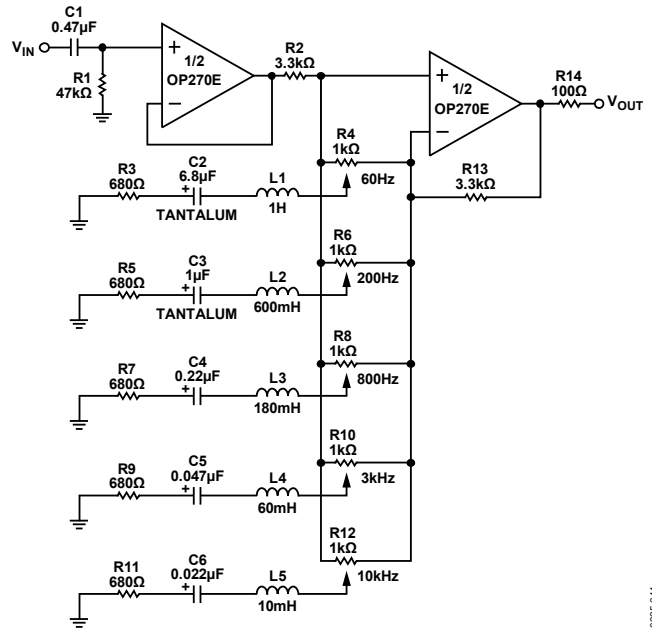


Figure 43. Five-Band, Low Noise Graphic Equalizer



**DIGITAL PANNING CONTROL**

Figure 44 uses a DAC8221 (a dual 12-bit CMOS DAC) to pan a signal between two channels. One channel is formed by the current output of DAC A driving one-half of an OP270 in a current-to-voltage converter configuration. The other channel is formed by the complementary output current of DAC A, which normally flows to ground through the AGND pin. This complementary current is converted to a voltage by the other half of the OP270, which also holds AGND at virtual ground.

Gain error due to mismatching between the internal DAC ladder resistors and the current-to-voltage feedback resistors is eliminated by using feedback resistors internal to the DAC8221. Only DAC A passes a signal; DAC B provides the second feedback resistor. With V<sub>REFB</sub> unconnected, the current-to-voltage converter, using R<sub>FBB</sub>, is accurate and not influenced by digital data reaching DAC B. Distortion of the digital panning control is less than 0.002% over the 20 Hz to 20 kHz audio range. Figure 45 shows the complementary outputs for a 1 kHz audio input signal and a digital ramp applied to the DAC data input.

**DUAL PROGRAMMABLE GAIN AMPLIFIER**

The dual OP270 and the DAC8221 (a dual 12-bit CMOS DAC) can be combined to form a space-saving, dual programmable amplifier. The digital code present at the DAC, which is easily set by a microprocessor, determines the ratio between the internal feedback resistor and the resistance that the DAC ladder presents to the op amp feedback loop. Gain of each amplifier is

$$\frac{V_O}{V_{IN}} = -\frac{4096}{n}$$

where *n* is the decimal equivalent of the 12-bit digital code present at the DAC.

If the digital code present at the DAC consists of all 0s, the feedback loop opens, causing the op amp output to saturate. A 20 MΩ resistor placed in parallel with the DAC feedback loop eliminates this problem with only a very small reduction in gain accuracy.

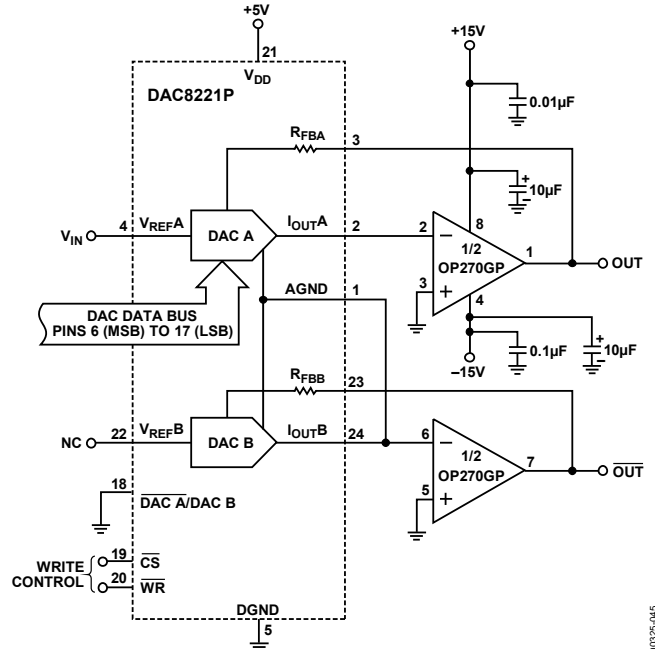


Figure 44. Digital Panning Control

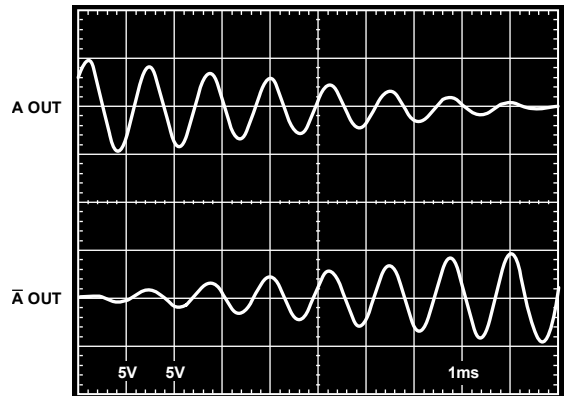


Figure 45. Digital Panning Control Output

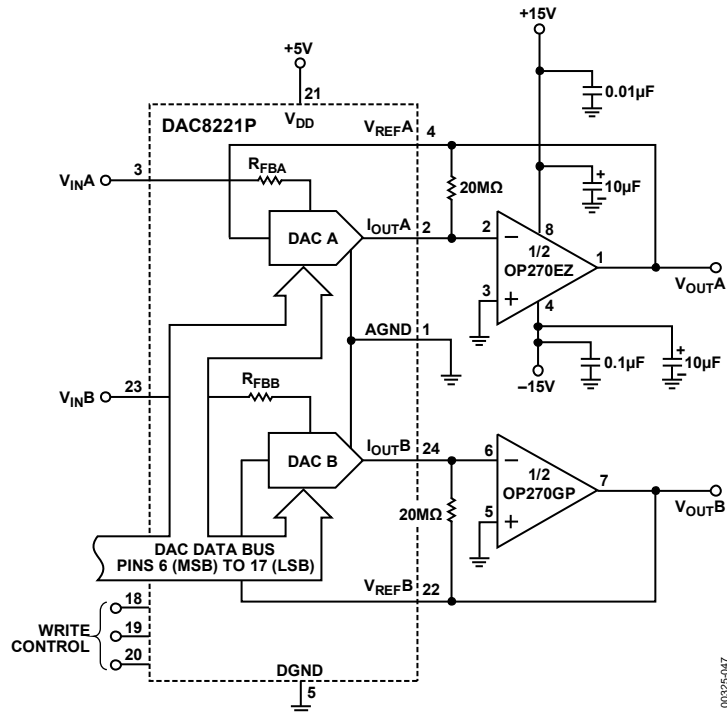


Figure 46. Dual Programmable Gain Amplifier

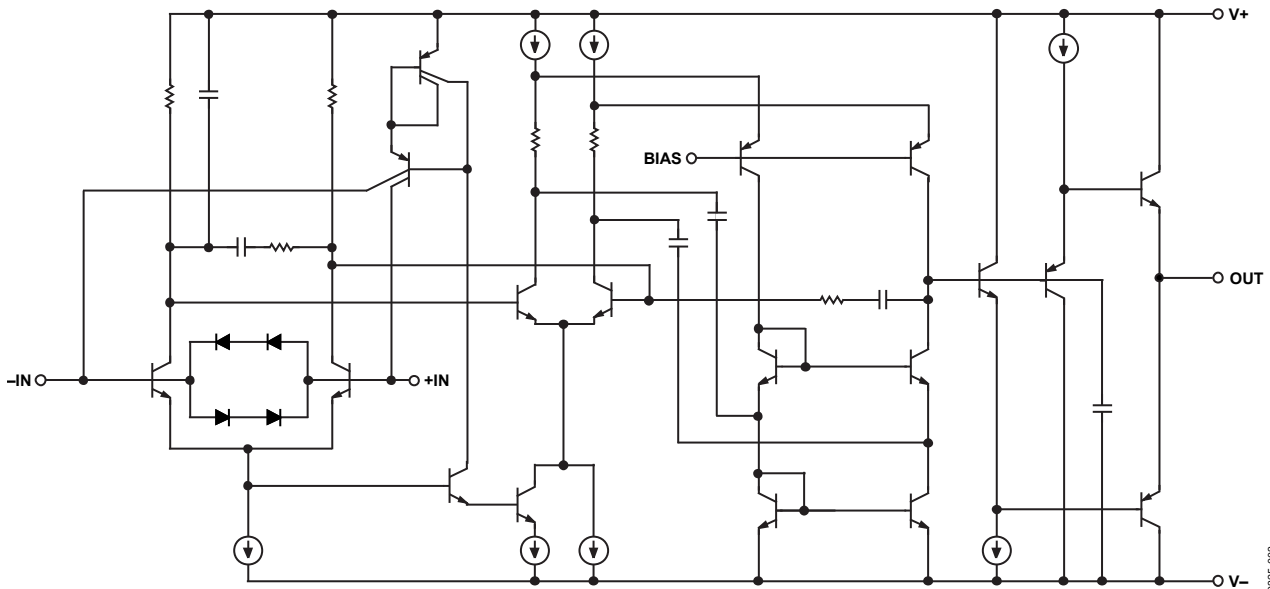
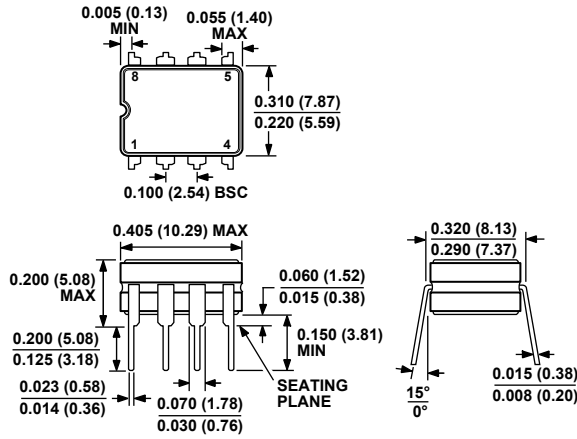


Figure 47. Simplified Schematic  
(One of Two Amplifiers Is Shown)

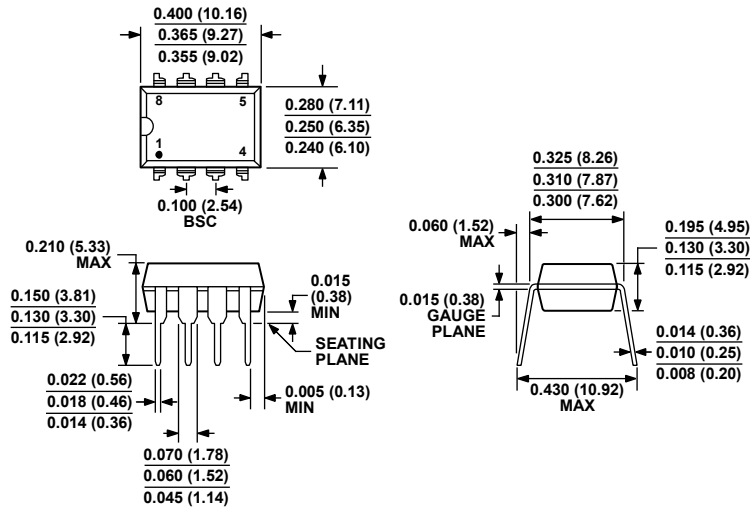
# OUTLINE DIMENSIONS



CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 48. 8-Lead Ceramic Dual In-Line Package [CERDIP]  
Z-Suffix  
(Q-8)

Dimensions shown in inches and (millimeters)



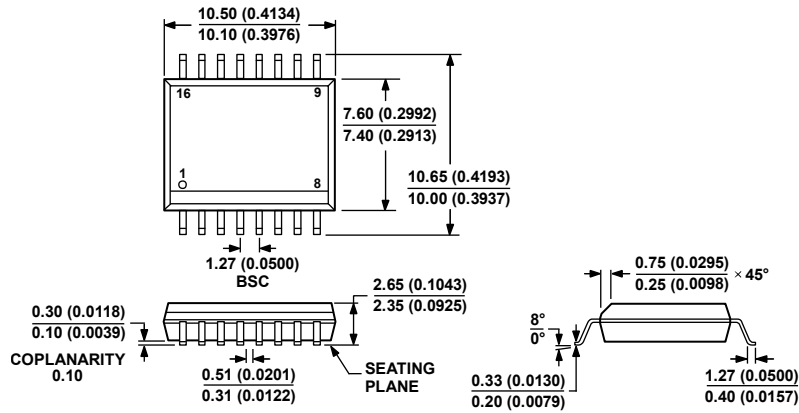
COMPLIANT TO JEDEC STANDARDS MS-001  
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN. CORNER LEADS MAY BE CONFIGURED AS WHOLE OR HALF LEADS.

Figure 49. 8-Lead Plastic Dual In-Line Package [PDIP]  
Narrow Body  
P-Suffix  
(N-8)

Dimensions shown in inches and (millimeters)

070806-A

# OP270



COMPLIANT TO JEDEC STANDARDS MS-013-AA  
 CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS  
 (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR  
 REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 50. 16-Lead Standard Small Outline Package [SOIC\_W]  
 Wide Body  
 S-Suffix  
 (RW-16)

Dimensions shown in millimeters and (inches)

032707-B

## ORDERING GUIDE

| Model                      | $T_A = +25^\circ\text{C}$<br>$V_{os\ Max}$ ( $\mu\text{V}$ ) | $\theta_{JC}$<br>( $^\circ\text{C}/\text{W}$ ) | $\theta_{JA}^1$<br>( $^\circ\text{C}/\text{W}$ ) | Temperature Range | Package Description | Package Option   |
|----------------------------|--|--|--|-------------------|---------------------|------------------|
| OP270EZ                    | 75   | 12   | 134  | -40°C to +85°C    | 8-Lead Cerdip       | Q-8 (Z-Suffix)   |
| OP270FZ                    | 150  | 12   | 134  | -40°C to +85°C    | 8-Lead Cerdip       | Q-8 (Z-Suffix)   |
| OP270GP                    | 250  | 37   | 96   | -40°C to +85°C    | 8-Lead PDIP         | N-8 (P-Suffix)   |
| OP270GPZ <sup>2</sup>      |  |  |  | -40°C to +85°C    | 8-Lead PDIP         | N-8 (P-Suffix)   |
| OP270GS                    | 250  | 27   | 92   | -40°C to +85°C    | 16-Lead SOIC_W      | RW-16 (S-Suffix) |
| OP270GS-REEL               |  |  |  | -40°C to +85°C    | 16-Lead SOIC_W      | RW-16 (S-Suffix) |
| OP270GSZ <sup>2</sup>      |  |  |  | -40°C to +85°C    | 16-Lead SOIC_W      | RW-16 (S-Suffix) |
| OP270GSZ-REEL <sup>2</sup> |  |  |  | -40°C to +85°C    | 16-Lead SOIC_W      | RW-16 (S-Suffix) |

<sup>1</sup>  $\theta_{JA}$  is specified for worst-case mounting conditions, that is,  $\theta_{JA}$  is specified for device in socket for Cerdip and PDIP packages;  $\theta_{JA}$  is specified for device soldered to printed circuit board for SOIC package.

<sup>2</sup> Z = RoHS Compliant Part.



Компания «ЭлектроПласт» предлагает заключение долгосрочных отношений при поставках импортных электронных компонентов на взаимовыгодных условиях!

Наши преимущества:

- Оперативные поставки широкого спектра электронных компонентов отечественного и импортного производства напрямую от производителей и с крупнейших мировых складов;
- Поставка более 17-ти миллионов наименований электронных компонентов;
- Поставка сложных, дефицитных, либо снятых с производства позиций;
- Оперативные сроки поставки под заказ (от 5 рабочих дней);
- Экспресс доставка в любую точку России;
- Техническая поддержка проекта, помощь в подборе аналогов, поставка прототипов;
- Система менеджмента качества сертифицирована по Международному стандарту ISO 9001;
- Лицензия ФСБ на осуществление работ с использованием сведений, составляющих государственную тайну;
- Поставка специализированных компонентов (Xilinx, Altera, Analog Devices, Intersil, Interpoint, Microsemi, Aeroflex, Peregrine, Syfer, Eurofarad, Texas Instrument, Miteq, Cobham, E2V, MA-COM, Hittite, Mini-Circuits, General Dynamics и др.);

Помимо этого, одним из направлений компании «ЭлектроПласт» является направление «Источники питания». Мы предлагаем Вам помощь Конструкторского отдела:

- Подбор оптимального решения, техническое обоснование при выборе компонента;
- Подбор аналогов;
- Консультации по применению компонента;
- Поставка образцов и прототипов;
- Техническая поддержка проекта;
- Защита от снятия компонента с производства.



#### Как с нами связаться

**Телефон:** 8 (812) 309 58 32 (многоканальный)

**Факс:** 8 (812) 320-02-42

**Электронная почта:** [org@eplast1.ru](mailto:org@eplast1.ru)

**Адрес:** 198099, г. Санкт-Петербург, ул. Калинина, дом 2, корпус 4, литера А.